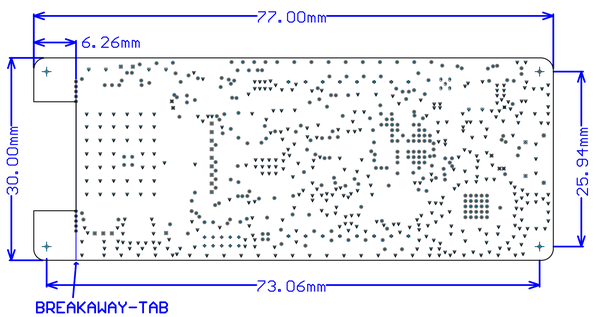
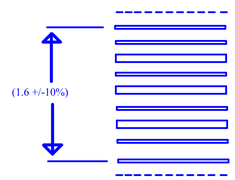
| REV | ECO | Comments | Date |
|---|---|---|---|
| | | | |




## LAYER STACK-UP




| Layer Description | Thickness after Lamination (mils) | DIFF IMP (ohm) +/-10% | DIFF TRACE WIDTH/ SPACING | Reference layer |
|---|---|---|---|---|
| PRIMARY SIDE, SILK SCREEN | | | | |
| PRIMARY SIDE, SOLDER MASK | 0.7 | | | |
| PRIMARY SIDE, LAYER1(TOP LAYER) | 1.78 | 90 | 6/ 5mils | L2 |
| DIELECTRIC | 5 | | | |
| INNER PLANE LAYER, LAYER2(GND) | 1.4 | | | |
| DIELECTRIC | 46 | | | |
| INNER PLANE LAYER, LAYER3(VCC) | 1.4 | | | |
| DIELECTRIC | 5 | | | |
| SECONDARY SIDE, LAYER4(BOTTOM LAYER) | 1.78 | 90 | 6/ 5mils | L3 |
| SECONDARY SIDE, SOLDER MASK | 0.7 | | | |
| SECONDARY SIDE, SILK SCREEN | | | | |

| Symbol | Count | Hole Size | Plated | Hole Type | Drill Layer Pair |
|---|---|---|---|---|---|
| | 274 | 0.203mm (8.00mil) | PTH | Round | Top Layer - Bottom Layer |
| | 10 | 0.254mm (10.00mil) | NPTH | Round | Top Layer - Bottom Layer |
| | 371 | 0.254mm (10.00mil) | PTH | Round | Top Layer - Bottom Layer |
| G | 5 | 0.300mm (11.81mil) | PTH | Round | Top Layer - Bottom Layer |
| | 5 | 0.305mm (12.00mil) | PTH | Round | Top Layer - Bottom Layer |
| | 15 | 0.400mm (15.75mil) | PTH | Round | Top Layer - Bottom Layer |
| | 1 | 0.406mm (16.00mil) | PTH | Round | Top Layer - Bottom Layer |
| | 10 | 0.650mm (25.59mil) | PTH | Round | Top Layer - Bottom Layer |
| | 2 | 0.850mm (33.47mil) | PTH | Round | Top Layer - Bottom Layer |
| | 16 | 0.889mm (35.00mil) | PTH | Round | Top Layer - Bottom Layer |
| | 6 | 0.900mm (35.43mil) | PTH | Round | Top Layer - Bottom Layer |
| | 2 | 1.150mm (45.28mil) | PTH | Round | Top Layer - Bottom Layer |
| | 2 | 2.700mm (106.30mil) | NPTH | Round | Top Layer - Bottom Layer |
| | 2 | 2.700mm (106.30mil) | PTH | Round | Top Layer - Bottom Layer |
| | 721 Total | | | | |

THIS PCB TO BE MANUFACTURED TO MEET ALL ACCEPTANCE LEVELS OF A CLASS 2 PCB PER ANSI/IPC-A-600G.

MATERIAL: FR-4 or Equivalent

- [X] MULTILAYER [4] LAYERS [X] CONTROLLED IMPEDANCE
- Cu EXTERNAL LAYERS [1.78 Mils] FINISHED
- Cu INTERNAL LAYERS [1.4 Mils] FINISHED
- FINISHED OVERALL THICKNESS [1.6] mm ± [10] %
- COPPER THIEVING ALLOWED [ ] YES [X] NO
- VIA TENTING ON BOTH SIDES [X] YES [ ] NO

FINISH:

- [ ] LEAD-FREE HOT AIR LEVELING
- [X] IMMERSION GOLD
- [ ] IMMERSION TIN
- [ ] SMOBC WITH SELECTIVE GOLD PLATING ON LANDS INDICATED. 1um GOLD OVER 5-10 um NICKEL

SOLDERMASK: DYNACHEM EPIC 200 LPI OR EQUIVALENT

SOLDERMASK COLOR: RED HIGH GLOSS

SILKSCREEN COLOR: WHITE

VIAS ARE TENTED IN BOTH SIDE.

ALL HOLES TO BE LOCATED BY THE COORDINATES FROM THE NC DRILL DATA PROVIDED.

USE ARTWORK SET NO. 05-11423 PCB REV 4.0

ALL UL LOGO, MANUFACTURER'S ID, AND DATE CODES SHALL BE PLACED ON THE BOTTOM SIDE UNLESS OTHERWISE INDICATED.

ANY ALTERNATIVES TO THE ABOVE SPECIFICATIONS MUST FIRST BE APPROVED.


MICROCHIP
Microchip Technology Inc.
2355 W. Chandler Blvd.
Chandler, AZ 85224


| | | | |
|---|---|---|---|
| TITLE: WBZ451 CURIOSITY BOARD | | | PART NUMBER: EV96B94A |
| PCB DESIGNER: BALAJI NARAYANA | GERBER FILE: Fab Drawing (Bottom,Top Layer) | | |
| ENGINEER: RINU CLEETUS | BOARD NUMBER: 04-11423 | DOCUMENT NUMBER: 04-11423-D | DATE: 1/17/2022 |
| PCB FILE NAME: WBZ451 Curiosity Board-R4.PcbDoc | LAYER NAME: FAB (M4) | REV: 4.0 | 10mm 400mil |