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Cromemco

ZPU

Z-80 Central Processing Unit

Instruction Manual

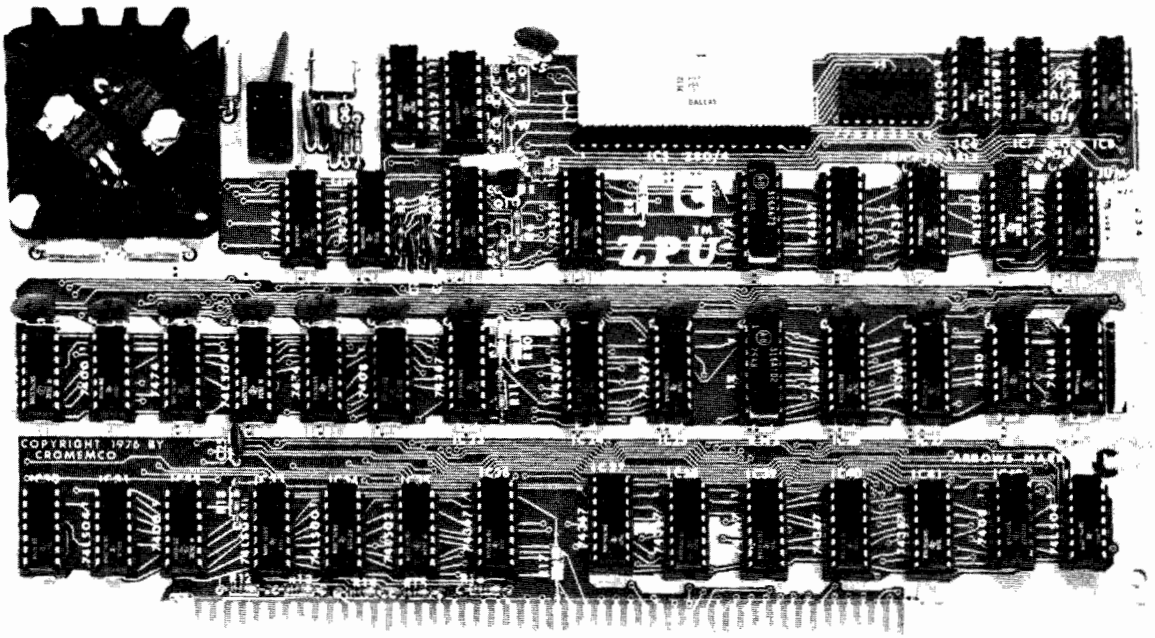
Marcus 6

1982

Cromemco

ZPU

Z-80 Central Processing Unit



Cromemco™
incorporated
Tomorrow's Computers Today
280 BERNARDO AVE MOUNTAIN VIEW, CA 94043

Part No. 023-0012

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Section 1

INTRODUCTION

This manual contains assembly and operating instructions for Cromemco's powerful 4 MHz S-100 bus compatible Z-80A CPU card (ZPU). The ZPU is designed to bring the power and speed of the Z-80A processor to systems using the 8080-oriented S-100 bus. Thus, the manual also includes an extensive section detailing S-100 bus features. Please read Section 2, OPERATING INSTRUCTIONS, before inserting the ZPU into your S-100 system bus.

TECHNICAL SPECIFICATIONS

PROCESSOR:	4 MHz version of the Z80
CLOCK RATE:	2 MHz or 4 MHz (switch selectable)
INSTRUCTION SET:	158 instructions including the 78 instructions of the 8080 processor
POWER-ON JUMP:	Jumper wire enabled
POWER-ON JUMP LOCATIONS:	16 switch selectable locations
WAIT STATE GENERATION:	0 - 4 jumper selectable wait states
M1 WAIT STATE:	Jumper wire selectable
BUS COMPATIBILITY:	S-100
POWER REQUIREMENTS:	+8 VDC @ 1.1 A
OPERATING ENVIRONMENT:	0 - 55 degrees Celsius

SECTION 2

OPERATING INSTRUCTIONS

The Cromemco ZPU is an S-100 bus compatible CPU (Central Processing Unit) which uses the powerful Z-80A microprocessor. The Cromemco ZPU has an exclusive set of features designed to increase your total system computing power. Most importantly, the ZPU operates reliably at a 4 MHz clock rate--twice the speed of most other microcomputer systems. The ZPU offers Power-On Jump capability, an on-board wait state generator, optional independent selection of M1 wait states, address mirroring circuitry, and several other features discussed in this section.

2.1 POWER-ON JUMP

The ZPU Power-On Jump circuitry allows the board to be used in an S-100 bus system without front panel controls (e.g., Cromemco's Z-2, Z-2D and SYSTEM THREE). When system power is turned ON, the ZPU hardware forces an automatic jump to one-of-sixteen memory location selected with the four position Jump Address select switch.

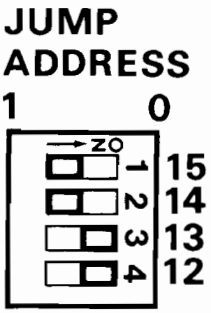
The automatic jump address corresponding to each switch setting is tabulated below:

SWITCH				POWER-ON
A15	A14	A13	A12	JUMP ADDRESS
Ø	Ø	Ø	Ø	ØØØØH
Ø	Ø	Ø	1	1ØØØH
Ø	Ø	1	Ø	2ØØØH
Ø	Ø	1	1	3ØØØH
Ø	1	Ø	Ø	4ØØØH
Ø	1	Ø	1	5ØØØH
Ø	1	1	Ø	6ØØØH
Ø	1	1	1	7ØØØH
1	Ø	Ø	Ø	8ØØØH
1	Ø	Ø	1	9ØØØH
1	Ø	1	Ø	AØØØH
1	Ø	1	1	BØØØH
1	1	Ø	Ø	CØØØH
1	1	Ø	1	DØØØH
1	1	1	Ø	EØØØH
1	1	1	1	FØØØH

Note the Jump Address switch determines the four highest order bits in the jump address, with all other address bits set to logic Ø.

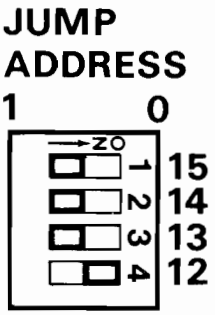
EXAMPLE 1

Suppose you have a Cromemco Z-2D System which comes standard with a 4FDC card and RDOS (Resident Disk Operating System) in PROM memory. This program, which resides at CØØØ-C3FFH, provides a convenient way to start-up a system. To effect an automatic jump to location CØØØH, the Jump Address switch should be set as shown below:



EXAMPLE 2

Suppose you have a Cromemco Z-2 System, and you want to force a jump to the Z-80 Monitor program after a system Power-On or RESET. The Z-80 Monitor spans addresses E000-E3FFH, so you would then set the Jump Address switch to E000H as shown below:



Your ZPU is factory shipped with the Power-On Jump feature enabled. To disable the function (resulting in an automatic jump to address 0000H only on a Power-On Clear or RESET), carefully cut the foil trace connecting two points on the board labeled "JUMP ENABLE".

If your computer system has RESET and EXAMINE front panel controls, the function of each of these switches is

altered when the automatic jump feature is enabled. Following a system RESET, the first instruction executed is not at address ØØØØH, but rather at one of the sixteen addresses specified with the Jump Address switch. Immediately after a RESET, the EXAMINE switch must be toggled twice in order to examine the automatic jump location: once to clear the automatic jump and a second time to perform the actual examine operation.

For computers with front panel switches and indicators, you can see how the Power-On Jump works by pressing the STOP switch, then raising the RESET switch. The number C3H should appear in the DATA display. This is the op code of the hardware jump instruction. Now press the EXAMINE NEXT switch; all Ø's will appear in the DATA display indicating the low order 8 bits of the jump address. Press the EXAMINE NEXT switch again; the high order 8 bits of the jump address will now appear in the DATA display. The lower four bits will all be Ø's, and the higher four bits will display the Jump Address switch bits.

2.2 Z-8ØA CLOCK FREQUENCY SELECTION

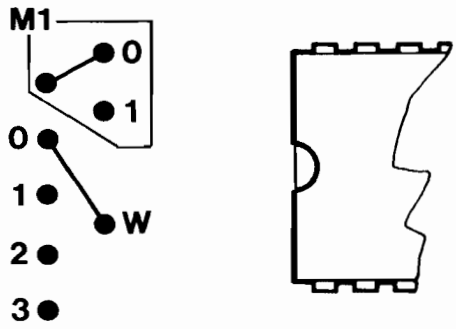
The Z-8ØA may be clocked at either 4 MHz (with a 25Ø nsec cycle time) or 2 MHz (with a 5ØØ nsec cycle time). The operating frequency is switch selectable with the toggle switch labeled "2" (2 MHz) and "4" (4 MHz).

The line previously labeled "STACK" on the S-100 bus is used by the ZPU as a 4 MHz indicator line. The Cromemco Z-1 System front panel indicator which monitors this line is labeled "4 MHz" (it may be labeled "STACK" on non-Cromemco products). The indicator will be ON for 4 MHz operation, and OFF for 2 MHz operation.

2.3 WAIT STATE SELECTION

The ZPU features an on-board WAIT STATE generator to match the Z-80A clock frequency to your system's memory access time. The ZPU allows two types of wait state insertion. The first inserts from 0 to 3 wait state cycles (1 cycle = 250 nsec at 4 MHz; 500 nsec at 2 MHz) during every machine cycle; the second type inserts either one or no additional wait states during an instruction fetch cycle only (referred to as an M1-cycle in the Zilog literature), where the timing requirements are the tightest.

If you are using Cromemco memory boards, leave your ZPU in its factory wired condition (no wait states); all wait state selection is done on the memory boards if required. Wait state selection to accomodate other boards is accomplished by re-configuring ZPU board jumpers M1 and W (just to the left of the Z-80A chip).



A jumper wire from "W" to points labeled Ø, 1, 2 and 3 selects Ø, 1, 2 or 3 wait states on every machine cycle. A jumper wire from "M1" to points labeled Ø and 1 selects either Ø or 1 additional wait states during an M1 cycle. When operating the ZPU at 4 MHz, a 25Ø nsec memory board requires no wait states to be compatible with the Z-8ØA CPU. Each additional W-wait state (from one to three) slows the required memory access time by 25Ø nsec, while an M1-wait state slows the required memory access time an additional 11Ø nsec (approx.). The corresponding figures for 2 MHz operation are; no wait states for 5ØØ nsec memory boards, 5ØØ nsec per W-wait state added, and an additional 235 nsec (approx.) for an M1-wait state. You may find these figures to be somewhat conservative in actual practice. To get the maximum performance from your memory, you may wish to experimentally find the fewest number of wait states required for reliable operation.

The ZPU comes factory pre-wired for no wait states. If a change is necessary, carefully cut the factory installed foil trace between points labeled "W" and "Ø", or between

"M1" and "Ø" as appropriate before installing new jumper wires.

2.4 ADDRESS MIRROR SELECTION

The 8Ø8Ø microprocessor repeats (or mirrors) the 8-bit address of an I/O port in both the high and low order 8 bits of the address bus. Although this characteristic is not inherent in the Z-8ØA CPU, the ZPU board is designed to mimic this behavior through address mirror circuitry assuring ZPU compatibility when updating older 8Ø8Ø systems.

The address mirror circuitry is enabled by the short run of foil between pads labeled "AM" and "ON" (between IC7 and IC8 on the board). If you wish to disable this circuitry, carefully cut the existing foil trace, and in its place, connect pads "AM" and "OFF" with a jumper wire.

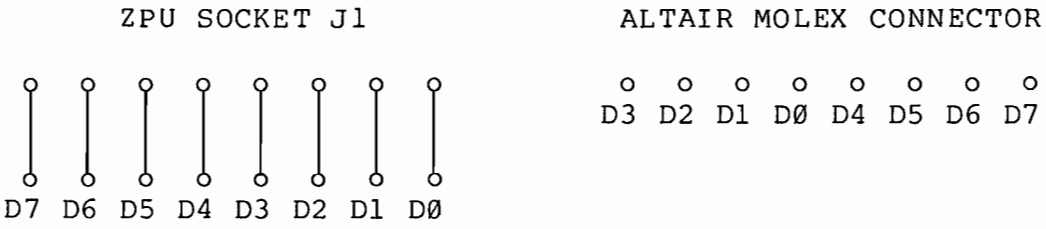
2.5 REFRESH ENABLE

Certain types of dynamic memory boards require that the refresh address supplied by the Z-8ØA be mirrored in the eight high order address lines. To enable this feature, install a jumper wire between the two pads labeled "RFSH ENAB". The ZPU is factory shipped with this connection broken as no Cromemco memory boards require address mirroring.

2.6 ALTAIR OR IMSAI INSTALLATION

If you are using an IMSAI 8080 computer, the cable from the front panel may be plugged directly into socket J1 on the ZPU board.

If you are using an ALTAIR 8800 or 8800A computer, a DIP plug must be installed in place of the Molex connector on the front panel cord. When wiring the connector, note that the data lines are not arranged sequentially on the ALTAIR connector as they are on the ZPU connector (refer to the figure below for wiring information).



Section 3

THE S-100 BUS

The Cromemco ZPU card is designed to interface the Z-80A microprocessor to the industry standard S-100 bus. The S-100 bus, in turn, is designed to interface a CPU module to as many as 20 additional memory, I/O interface, or other processor modules. This bus standard was originally known as the "Altair" bus appearing in the MITS Altair line of computers in 1975. The bus was quickly adopted by a host of microcomputer manufacturers and was named the "S-100" bus by Dr. Roger Melen of Cromemco Inc. in August of 1976. The S-100, or "Standard-100", bus is now widely regarded as the most-used busing standard ever developed in the computer industry.

Physically, the S-100 bus is realized as a set of 100-contact edge connectors mounted to a common mother board and wired in parallel. The modules that plug into the edge connectors of the S-100 bus are circuit cards that measure 5" by 10".

The S-100 bus was originally designed for use with a CPU module using the 8080 microprocessor, and consequently, the bus signal definitions closely follow those of an 8080 system. The Z-80A microprocessor signal lines differ quite

dramatically from the 8080 lines (e.g., the Z-80A is driven by a single phase clock, the 8080 by a two phase clock), but the ZPU board is designed to supply all "8080-like" S-100 bus functions (including the two phase clock). The signals of the S-100 bus can be grouped in four functional categories: 1) power supply, 2) address, 3) data, and 4) clock and control signals. A complete listing of the S-100 bus signals is shown below:

S-100 BUS

1.	+8 VOLTS	26.	pHLDA	51.	+8 VOLTS	76.	pSYNC
2.	+18 VOLTS	27.	pWAIT	52.	-18 VOLTS	77.	$\overline{\text{pWR}}$
3.	EXT. READY	28.	pINTE	53.	$\overline{\text{SSW DISABLE}}$	78.	pDBIN
4.	UNDEFINED	29.	A5	54.	$\overline{\text{EXT. CLEAR}}$	79.	A0
5.	"	30.	A4	55.	UNDEFINED	80.	A1
6.	"	31.	A3	56.	"	81.	A2
7.	"	32.	A15	57.	"	82.	A6
8.	"	33.	A12	58.	"	83.	A7
9.	"	34.	A9	59.	"	84.	A8
10.	"	35.	DO1	60.	"	85.	A13
11.	"	36.	DO0	61.	"	86.	A14
12.	$\overline{\text{NMI}}$	37.	A10	62.	"	87.	A11
13.	UNDEFINED	38.	DO4	63.	"	88.	DO2
14.	"	39.	DO5	64.	"	89.	DO3
15.	"	40.	DO6	65.	$\overline{\text{MEM. REQUEST}}$	90.	DO7
16.	"	41.	DI2	66.	$\overline{\text{REFRESH}}$	91.	DI4
17.	"	42.	DI3	67.	UNDEFINED	92.	DI5
18.	$\overline{\text{STATUS DISAB.}}$	43.	DI7	68.	$\overline{\text{MEM. WRITE}}$	93.	DI6
19.	$\overline{\text{CONTROL DISAB.}}$	44.	sM1	69.	$\overline{\text{PROTECT STAT.}}$	94.	DI1
20.	UNPROT. MEM.	45.	sOUT	70.	PROTECT MEM.	95.	DI0
21.	$\overline{\text{SINGLE STEP}}$	46.	sINP	71.	RUN	96.	sINTA
22.	$\overline{\text{ADDR. DISAB.}}$	47.	sMEMR	72.	pREADY	97.	$\overline{\text{sWO}}$
23.	$\overline{\text{DO DISABLE}}$	48.	sHLTA	73.	$\overline{\text{pINT}}$	98.	sSTACK/4 MHz
24.	ϕ2 CLOCK	49.	2 MHz CLK.	74.	$\overline{\text{pHOLD}}$	99.	$\overline{\text{PWR-ON CLEAR}}$
25.	ϕ1 CLOCK	50.	GROUND	75.	$\overline{\text{pRESET}}$	100.	GROUND

S-100 POWER SUPPLY

+8 Volts	Pins 1 and 51
+18 Volts	Pin 2
-18 Volts	Pin 52
Ground	Pins 50 and 100

Three unregulated D.C. power supply voltages appear on the S-100 bus: +8 volts, +18 volts and -18 volts. The main power supplies are unregulated, so power supply regulation must be performed on each individual circuit card, usually by three-terminal regulator IC's.

Distributed power supply regulation has several advantages over a single, centrally regulated supply:

-Each card is individually protected from voltage overload. Faulty regulation in one master supply cannot destroy the entire computer system.

-The heat produced by voltage regulation is thermally distributed through a larger physical volume.

-Voltage drops along the bus do not influence the voltage on the card circuitry itself.

-Initial cost of the computer mainframe is lower. Regulation circuitry is purchased only as additional cards are added to

the system.

An S-100 bus mainframe capable of accepting a full 21 cards (like the Cromemco Z-2, Z-2D and SYSTEM THREE) typically has a power supply current capacity of 30 amps at +8 volts and 15 amps at +18 and -18 volts.

S-100 ADDRESS SIGNALS

A0	PIN 79	A8	PIN 84
A1	PIN 80	A9	PIN 34
A2	PIN 81	A10	PIN 37
A3	PIN 31	A11	PIN 87
A4	PIN 30	A12	PIN 33
A5	PIN 29	A13	PIN 85
A6	PIN 82	A14	PIN 86
A7	PIN 83	A15	PIN 32

There are 16 address lines on the S-100 bus allowing the direct addressing of 65,536 words of memory space. Tri-state TTL drivers are used to drive the address bus. One S-100 bus control line ($\overline{\text{ADDRESS DISABLE}}$) can be used to disable the address drivers to allow DMA operations when other cards need to take control of the address bus.

S-100 DATA SIGNALS

DI0	PIN 95	DO0	PIN 36
DI1	PIN 94	DO1	PIN 35
DI2	PIN 41	DO2	PIN 88
DI3	PIN 42	DO3	PIN 89
DI4	PIN 91	DO4	PIN 38
DI5	PIN 92	DO5	PIN 39
DI6	PIN 93	DO6	PIN 40
DI7	PIN 43	DO7	PIN 90

Although the S-100 bus is based on the 8080 microprocessor which has an 8-bit bi-directional data bus, the S-100 has two directional data busses, each 8 bits wide. The data input bus is called the DI bus, and the data output bus is called the DO bus. The S-100 provides for one control line to disable the DO bus (DO DISABLE) for DMA operations.

S-100 CLOCK AND CONTROL SIGNALS

EXT READY	PIN 3	SSW DISABLE	PIN 53
NMI	PIN 12	EXT. CLEAR	PIN 54
STATUS DISAB.	PIN 18	MEM. REQ.	PIN 65
CONTROL DISAB.	PIN 19	REFRESH	PIN 66
UNPROTECT	PIN 20	MEM. WRITE	PIN 68
SINGLE STEP	PIN 21	PROTECT STATUS	PIN 69
ADDR. DISAB.	PIN 22	PROTECT	PIN 70
DO DISABLE	PIN 23	RUN	PIN 71
ϕ2	PIN 24	pREADY	PIN 72
ϕ1	PIN 25	pINT	PIN 73
pHLDA	PIN 26	pHOLD	PIN 74
pWAIT	PIN 27	pRESET	PIN 75
pINTE	PIN 28	pSYNC	PIN 76
sM1	PIN 44	pWR	PIN 77
sOUT	PIN 45	pDBIN	PIN 78
sINP	PIN 46	sINTA	PIN 96
sMEMR	PIN 47	sWO	PIN 97
sHLTA	PIN 48	sSTACK/4 Mhz	PIN 98
2 MHz CLOCK	PIN 49	PWR-ON CLEAR	PIN 99

There are three clock signals on the S-100 bus: ϕ1 (pin 25), ϕ2 (pin 24) and 2 MHz Clock (pin 49). The 2 MHz CLOCK line is always a 2 MHz signal regardless of the processor clock frequency. ϕ1 and ϕ2 provide a two phase non-overlapping clocks at the processor clock frequency. All clock and control signals on the S-100 bus are standard TTL levels.

Control signals on the S-100 bus which are functionally equivalent to control signals used with the 8080 microprocessor are prefixed with a lower case "p". Thus pHLDA, pWAIT, pINTE, pREADY, pHOLD, p$\overline{\text{INT}}$, p$\overline{\text{RESET}}$, pSYNC, p$\overline{\text{WR}}$ and pDBIN serve the same function as the corresponding control signals for the 8080 microprocessor. Similarly, S-100 bus signals prefixed with an "s" are functionally equivalent to the corresponding outputs of the 8080 status latch. These signals include sM1, sOUT, sINP, sMEMR, sHLTA, sINTA, s$\overline{\text{WO}}$ and sSTACK. The sSTACK line (pin 98) is used to indicate stack operations in 8080 systems; however in Cromemco Z-80A systems, this line is used instead to indicate 4 MHz operation (logic 1) or 2 MHz operation (logic 0).

Four of the S-100 control lines are dedicated to tri-stating bus drivers (e.g., during DMA operations). $\overline{\text{ADDRESS DISABLE}}$ is used to disable the address bus; $\overline{\text{DO DISABLE}}$ is

used to disable the Data Output bus; $\overline{\text{STATUS DISABLE}}$ is used to disable the status lines (those prefixed with an "s"); and $\overline{\text{CONTROL DISABLE}}$ is used to disable the clock and control signals.

Three of the S-100 control signals shown are used only with the Z-80A CPU. These are $\overline{\text{NMI}}$ (Non-Maskable Interrupt), $\overline{\text{MEMORY REQUEST}}$, and $\overline{\text{REFRESH}}$. The functions of these signals on the S-100 bus are the same as the corresponding lines of the Z-80A microprocessor.

The remaining ten defined lines are used primarily in S-100 systems with an operator's front panel. A front panel switch can be used to protect RAM or PROM memory from accidental memory write operations by issuing a PROTECT (pin 70) signal to the bus. The memory can be unprotected by the UNPROTECT (pin 20) signal, and the current PROTECTED or UNPROTECTED status of any memory can be determined from the PROTECT STATUS (pin 69) signal. MWRITE (pin 68) is used to indicate a memory write operation and is used in conjunction with front panel memory deposit. EXT. READY is an alternate to pREADY to avoid bus conflicts when both front panel circuitry and other circuitry need control of the processor READY line.

Front panel controls can be used to run or stop the processor or to single step through a program as indicated on

the RUN (pin 71) line and the SINGLE STEP (pin 21) line. When front panel sense switches are assigned to a specific input port, the SENSE SWITCH DISABLE ($\overline{\text{SSW DISABLE}}$, pin 53) is used to disable the DI bus during sense switch inputs. $\overline{\text{EXTERNAL CLEAR}}$ (pin 54) is activated by an auxillary front panel switch, but it is assigned to no specific function. Finally, there is the $\overline{\text{POWER-ON CLEAR}}$ signal that remains at logic Ø when power is first turned on, and then transitions to logic 1 approximately 1ØØ milliseconds later to indicate that power is on and the power supply voltages have stabilized.

ZPU PARTS LIST

Capacitors		Part No.
C1	10 uF	004-0032
C2	.001 uF	004-0022
C3	.005 uF	004-0025
C4	.005 uF	004-0025
C5	0.1 uF	004-0030
C6	10 uF	004-0032
C7	150 pF	004-0011
C8	56 pF	004-0006
C9	10 uF	004-0032
C10	10 uF	004-0032
C11-C24	0.1 uF	004-0030
C25	150 pF	004-0011
C26	10 uF	004-0032

Integrated Circuits		
IC1	LM340T-5	012-0001
IC2	LM340T-5	012-0001
IC3	74164	010-0007
IC4	74157	010-0009
IC5	Z-80A	011-0010
IC6	74LS04	010-0066
IC7	74LS10	010-0063
IC8	7400	010-0000
IC9	7474	010-0019
1C10	7404	010-0030
IC11	74367	010-0080
IC12	74367	010-0080
IC13	74367	010-0080
IC14	74367	010-0080
IC15	74LS04	010-0066
IC16	74157	010-0009
IC17	74LS10	010-0063
IC18	7400	010-0000
IC19	7474	010-0019
IC20	74LS04	010-0066
IC21	7474	010-0019
IC22	7408	010-0027
IC23	74367	010-0080
IC24	74367	010-0080
IC25	74367	010-0080
IC26	74367	010-0080
IC27	74367	010-0080
IC28	74S133	010-0089
IC29	74164	010-0007
IC30	7474	010-0019
IC31	74LS04	010-0066
IC32	7400	010-0000
IC33	74LS04	010-0066
IC34	74LS00	010-0069
IC35	74LS02	010-0068
IC36-41	74367	010-0080
IC42	7408	010-0027
IC43	74LS04	010-0066

Resistors		Part No.
R1	1K	001-0018
R2	1K	001-0018
R3	180	001-0009
R4	180	001-0009
R5	270	001-0011
R6	270	001-0011
R7	10K	001-0030
R8	390	001-0013
R9	330	001-0012
R10	330	001-0012
R11	1K	001-0018
R12	100	001-0007
R13	180	001-0009
R15	330	001-0012
R15	330	001-0012
R16	330	001-0012
R17	180	001-0009
R18	1K	001-0018
R19	180	001-0009

Resistor Networks		
RN1	4.7K DIP	003-0017
RN2	1K DIP	003-0016
RN3	1K SIP	003-0007
RN4	1K SIP	003-0007
RN5	330 SIP	003-0013

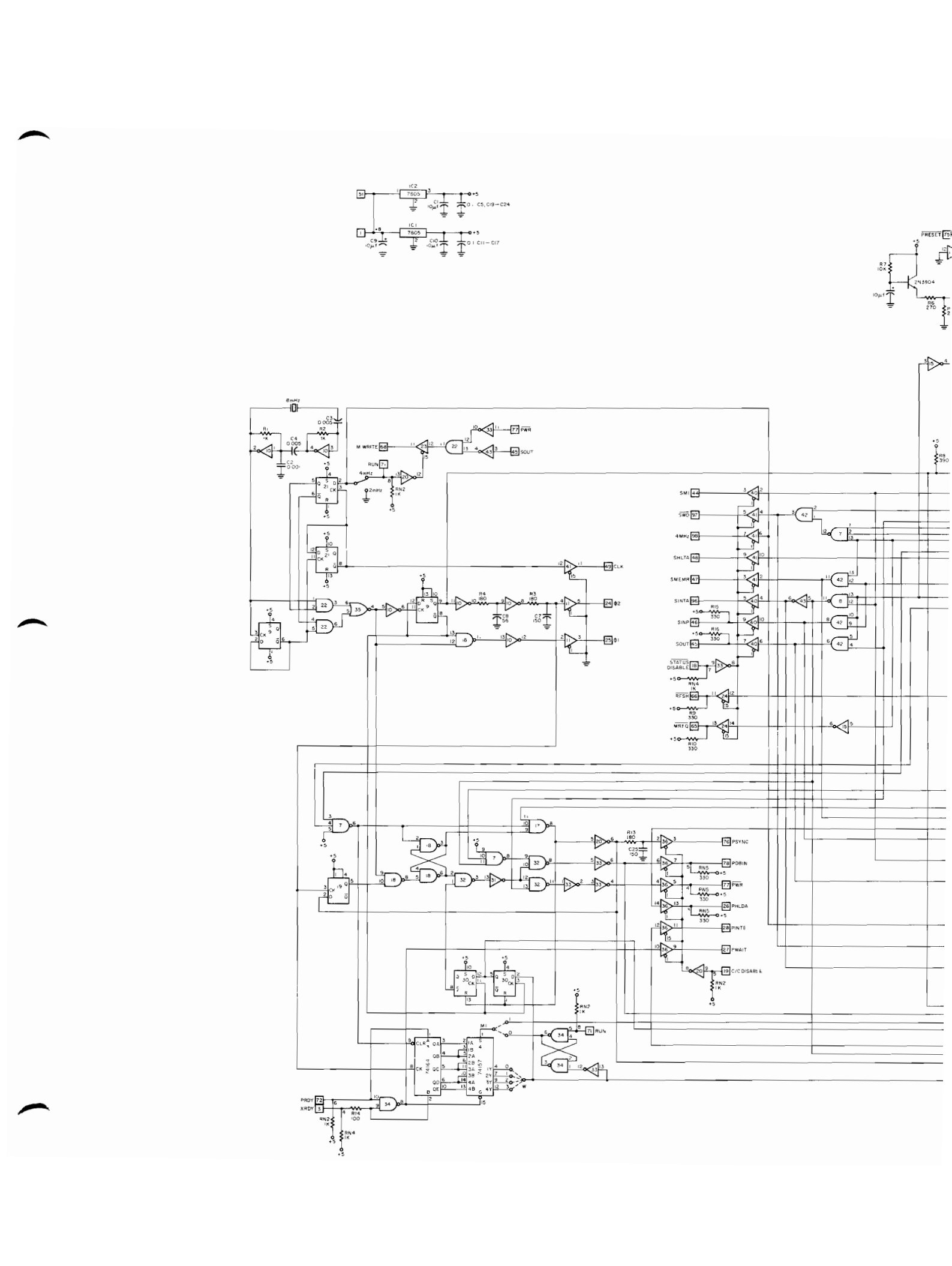
Miscellaneous

Q1 2N3404	009-0001
X1 8-MHZ XTAL	026-0001
SW1 SPDT SWITCH	013-0000
SW2 DIP SWITCH	013-0001
HEATSINK	021-0017
6-32 SCREWS (4)	015-0000
6-32 NUTS (4)	015-0013
#18 WIRE	019-0012
SOCKET 40 PIN	017-0006
22-SOCKETS, 14 PIN	017-0001
21-SOCKETS, 16 PIN	017-0002
ZPU PC BOARD	

LIMITED WARRANTY

Cromemco, Inc. warrants this ZPU processor board against defects in materials and workmanship for a period of Ninety (90) days from the date of delivery to the customer. Cromemco, Inc. will replace or repair at its option this product should it prove to be defective due to defects in materials or workmanship during the warranty period, provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. If this product fails after the above Ninety (90) day warranty period, it will be repaired for a fixed prepaid service fee provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. Cromemco, Inc. reserves the right to refuse to repair any product that in the discretion of Cromemco, Inc. has been subjected to electrical or mechanical abuse or not handled with reasonable care. The service fee is currently $70 and is subject to change without notice.

Cromemco, Inc. makes no further warranties either expressed or implied with respect to this product and its quality, performance, merchantability, or fitness for any particular use. In no event will Cromemco, Inc. be liable for direct, indirect, incidental or consequential damages resulting from any defect in this product even if Cromemco, Inc. has been advised of the possibility of such damages. Some states do not allow the exclusion or limitation of implied warranties or liability for incidental or consequential damages, so the above limitation may not apply to some customers.


IC2
7805
IC1
7805
C1
10µf
C9
10µf
C10
10µf
C5, C19–C24
C11–C17
PRESET
R7
10K
2N5904
R6
270
8mHz
C3
0.005
R1
1K
C4
0.005
R2
1K
C2
0.001
M WRITE
RUN
4mHz
2mHz
RN2
1K
PWR
SOUT
CLK
R4
180
R3
180
C8
56
C7
150
SMI
SWO
4MHz
SHLTA
SMEMR
SINTA
SINP
SOUT
STATUS DISABLE
RFSH
MRFQ
RN4
1K
R9
330
R10
330
R11
330
R15
330
R16
330
R99
390
C25
100
RN3
180
PSYNC
PDBIN
PWR
PHLDA
PINTE
PWAIT
C/C DISABLE
RN5
330
RN2
1K
M1
RUN
W
74164
74157
PRDY
XRDY
RN14
100
RN2
1K
RN4
1K

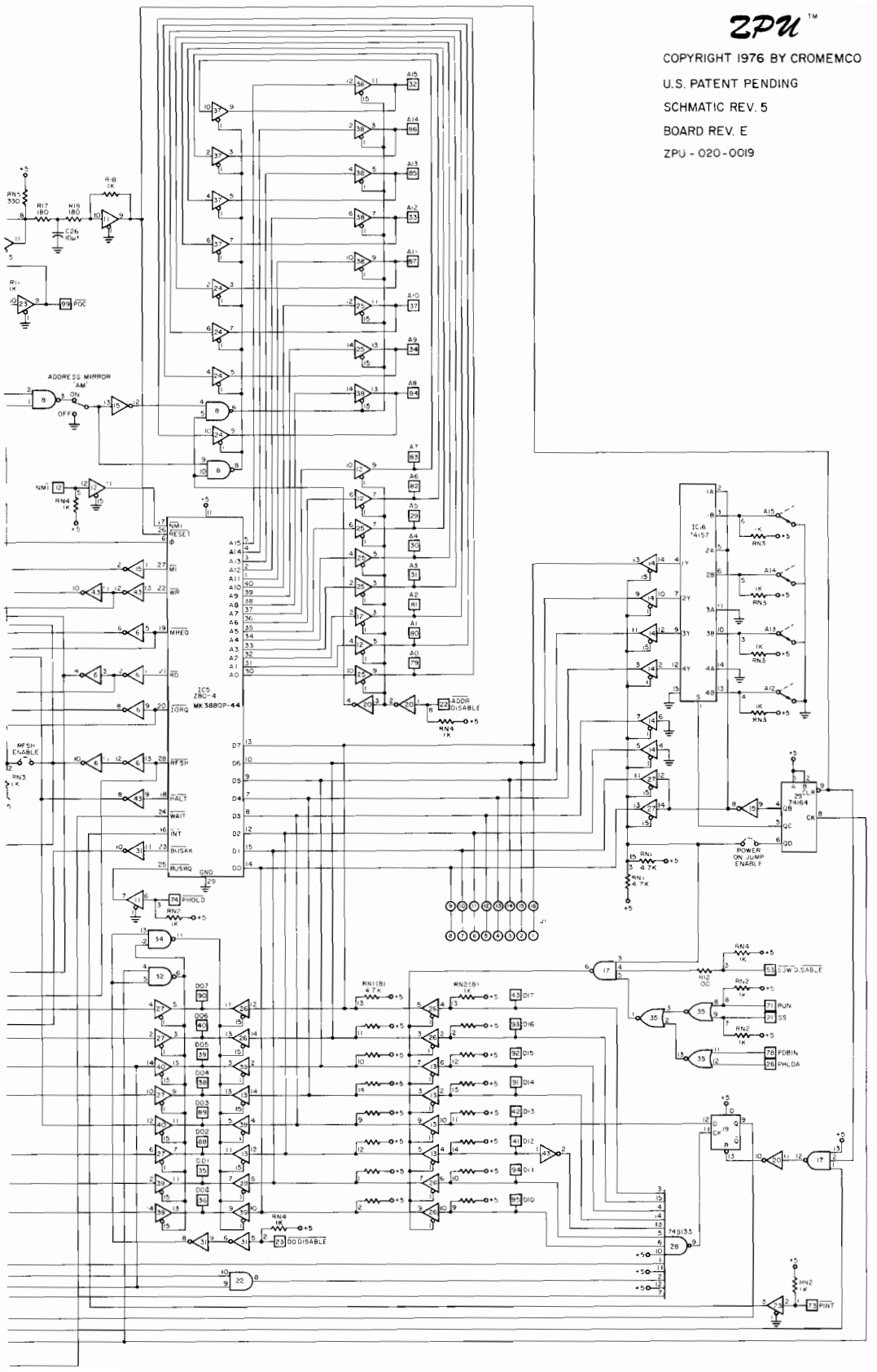
ZPU™

U.S. PATENT PENDING

SCHMATIC REV. 5

BOARD REV. E

ZPU - 020-0019



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