# <u>Lab 4 Parts A + B + C Reference Outputs (libg.mtr.gz)</u>

## Part A:

A.libq.res

CYCLES : 100000001

CORE\_0\_INST : 100000000 CORE\_0\_CYCLES : 1000 CORE\_0\_IPC : 1.000

: 100000000

MEMSYS\_IFETCH\_ACCESS : 100000000 MEMSYS\_LOAD\_ACCESS : 36353358 : 750076 : 0.000 MEMSYS\_LOAD\_ACCESS : 3635333
MEMSYS\_STORE\_ACCESS : 750076
MEMSYS\_IFETCH\_AVGDELAY : 0.000
MEMSYS\_LOAD\_AVGDELAY : 0.000
MEMSYS\_STORE\_AVGDELAY : 0.000 : 7500768

DCACHE\_READ\_ACCESS : 36353358
DCACHE\_WRITE\_ACCESS : 7500768
DCACHE\_READ\_MISS : 1191176
DCACHE\_WRITE\_MISS : 2321
DCACHE\_READ\_MISS\_PERC : 3.277

DCACHE\_WRITE\_MISS\_PERC : 0CACHE\_DIRTY\_EVICTS : 268702 0.031

#### Part B:

## B.S1MB.libq.res

CYCLES : 230595531

: 100000000

: 230595530

CORE\_0\_ING:
CORE\_0\_CYCLES : 0.434

MEMSYS\_IFETCH\_ACCESS : 100000000 MEMSYS\_LOAD\_ACCESS : 36353358 MEMSYS\_STORE\_ACCESS : 7500768 MEMSYS\_IFETCH\_AVGDELAY : 1.000 MEMSYS LOAD AVGDELAY 4.592 MEMSYS\_STORE\_AVGDELAY 1.003

ICACHE READ ACCESS : 100000000 ICACHE\_WRITE\_ACCESS 0 ICACHE\_READ\_MISS 17 ICACHE WRITE MISS 0

ICACHE\_READ\_MISS\_PERC 0.000 ICACHE\_WRITE\_MISS\_PERC 0.000

ICACHE\_DIRTY\_EVICTS 0

DCACHE DEAD DCACHE\_READ\_ACCESS : 36353358 : 7500768

DCACHE\_READ\_MISS : 1191176
DCACHE\_WRITE\_MISS : 2321
DCACHE\_READ\_MISS\_PERC : :

3.277 DCACHE\_WRITE\_MISS\_PERC 0.031

: 268702 DCACHE\_DIRTY\_EVICTS

L2CACHE\_READ\_ACCESS : 1193514 L2CACHE\_WRITE\_ACCESS 268702

L2CACHE READ MISS : 1186840 L2CACHE\_WRITE\_MISS 104

L2CACHE READ MISS PERC 99.441 L2CACHE\_WRITE\_MISS\_PERC 0.039 L2CACHE\_DIRTY\_EVICTS 263603

DRAM READ ACCESS : 1186840 DRAM\_WRITE\_ACCESS : 263603
DRAM\_READ\_DELAY\_AVG : 100.000 DRAM\_WRITE\_DELAY\_AVG : 100.000

#### Part C:

## C.S1MB.CP.libq.res

CYCLES : 230595531

CORE 0 INST : 100000000

CORE\_0\_CYCLES : 230595530

CORE\_0\_IPC : 0.434

MEMSYS\_IFETCH\_ACCESS : 100000000
MEMSYS\_LOAD\_ACCESS : 36353358
MEMSYS\_STORE\_ACCESS : 7500768
MEMSYS\_IFETCH\_AVGDELAY : 1.000
MEMSYS\_LOAD\_AVGDELAY : 4.592
MEMSYS\_STORE\_AVGDELAY : 1.003

ICACHE\_READ\_ACCESS : 100000000 ICACHE\_WRITE\_ACCESS : 0 ICACHE\_READ\_MISS : 17 ICACHE\_WRITE\_MISS : 0

ICACHE\_READ\_MISS\_PERC : 0.000
ICACHE\_WRITE\_MISS\_PERC : 0.000

ICACHE\_DIRTY\_EVICTS : 0

DCACHE\_READ\_ACCESS : 36353358 DCACHE\_WRITE\_ACCESS : 7500768

DCACHE\_READ\_MISS : 1191176 DCACHE WRITE MISS : 2321

DCACHE\_READ\_MISS\_PERC : 3.277
DCACHE\_WRITE\_MISS\_PERC : 0.031
DCACHE\_DIRTY\_EVICTS : 268702

L2CACHE\_READ\_ACCESS : 1193514 L2CACHE\_WRITE\_ACCESS : 268702

L2CACHE\_READ\_MISS : 1186840 L2CACHE\_WRITE\_MISS : 104

L2CACHE\_READ\_MISS\_PERC : 99.441 L2CACHE\_WRITE\_MISS\_PERC : 0.039 L2CACHE\_DIRTY\_EVICTS : 263603

DRAM\_READ\_ACCESS : 1186840 DRAM\_WRITE\_ACCESS : 263603 DRAM\_READ\_DELAY\_AVG : 100.000 DRAM\_WRITE\_DELAY\_AVG : 100.000

# C.S1MB.OP.libq.res

CYCLES : 206125791

CORE 0 INST : 100000000

CORE 0 CYCLES : 206125790

CORE\_0\_IPC : 0.485

MEMSYS\_IFETCH\_ACCESS : 100000000
MEMSYS\_LOAD\_ACCESS : 36353358
MEMSYS\_STORE\_ACCESS : 7500768
MEMSYS\_IFETCH\_AVGDELAY : 1.000
MEMSYS\_LOAD\_AVGDELAY : 3.919
MEMSYS\_STORE\_AVGDELAY : 1.003

ICACHE\_READ\_ACCESS : 100000000 ICACHE\_WRITE\_ACCESS : 0 ICACHE\_READ\_MISS : 17 ICACHE\_WRITE\_MISS : 0

ICACHE\_READ\_MISS\_PERC : 0.000 ICACHE\_WRITE\_MISS\_PERC : 0.000

ICACHE\_DIRTY\_EVICTS : 0

DCACHE\_READ\_ACCESS : 36353358 DCACHE\_WRITE\_ACCESS : 7500768

DCACHE\_READ\_MISS : 1191176 DCACHE WRITE MISS : 2321

DCACHE\_READ\_MISS\_PERC : 3.277 DCACHE\_WRITE\_MISS\_PERC : 0.031

DCACHE\_DIRTY\_EVICTS : 268702

L2CACHE\_READ\_ACCESS : 1193514 L2CACHE\_WRITE\_ACCESS : 268702

L2CACHE\_READ\_MISS : 1186840 L2CACHE\_WRITE\_MISS : 104

L2CACHE\_READ\_MISS\_PERC : 99.441 L2CACHE\_WRITE\_MISS\_PERC : 0.039 L2CACHE\_DIRTY\_EVICTS : 263603

DRAM\_READ\_ACCESS : 1186840 DRAM\_WRITE\_ACCESS : 263603 DRAM\_READ\_DELAY\_AVG : 79.383 DRAM\_WRITE\_DELAY\_AVG : 145.000