Software & Hardware Migration for Analog & Digital I/O in Rydberg-Assisted Quantum Engineering of Light Experiment

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JEIP Jeunes Equipes de l'Institut de Physique du Collège de France

- Quantum Photonics group
  - One principal investigator
  - One CNRS researcher
  - Two Doctoral students
  - Two Master 2 interns
  - One Master 1 intern

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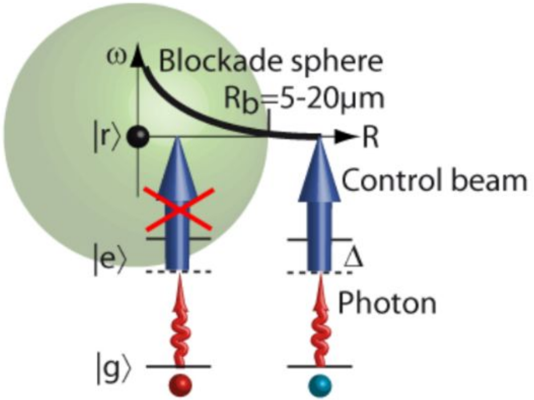
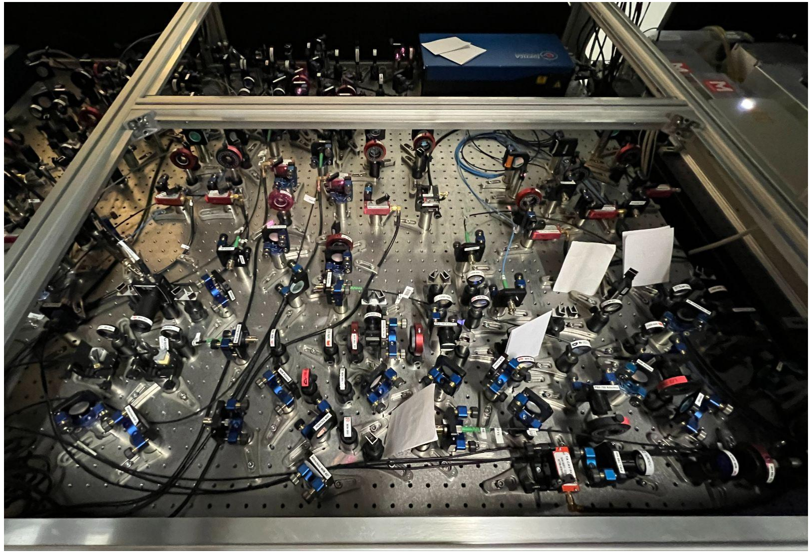
The Experiment

Theoretical Background

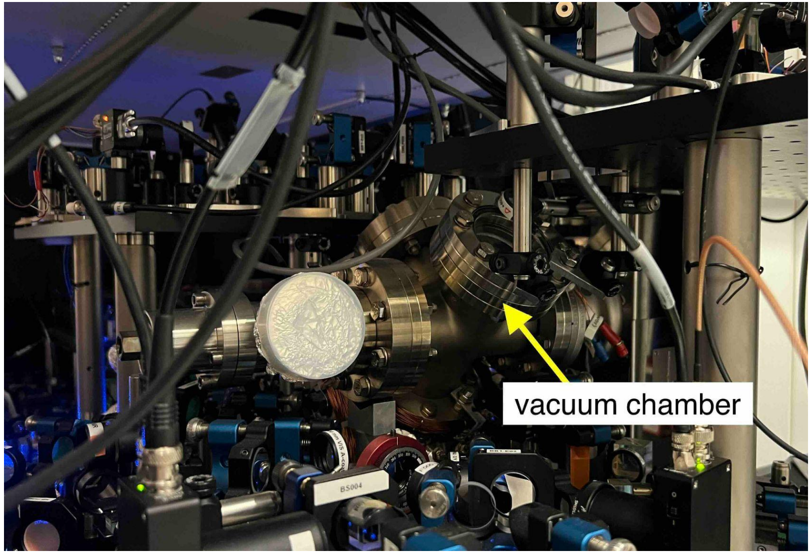
- Interactions b/w photons
  - Rb atoms & Rydberg states
  - Optical cavity
- Advantages
  - Better photon control
  - Minimize information loss
  - Experimental repeatability
- Probe & control beams



Experimental Setup

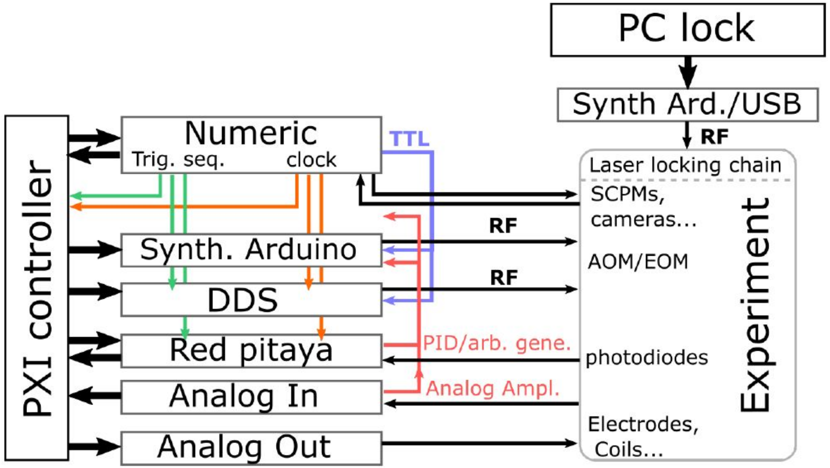


Controls & prepares lasers

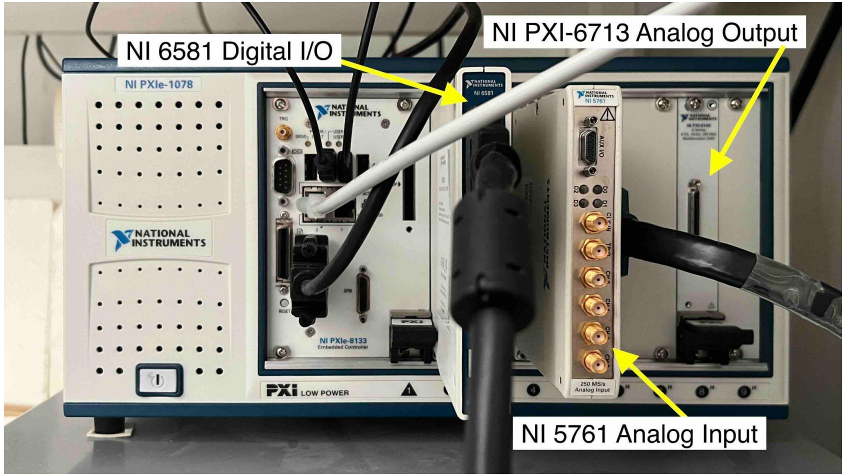


Hosts the optical cavity

Hardware



Experimental control system

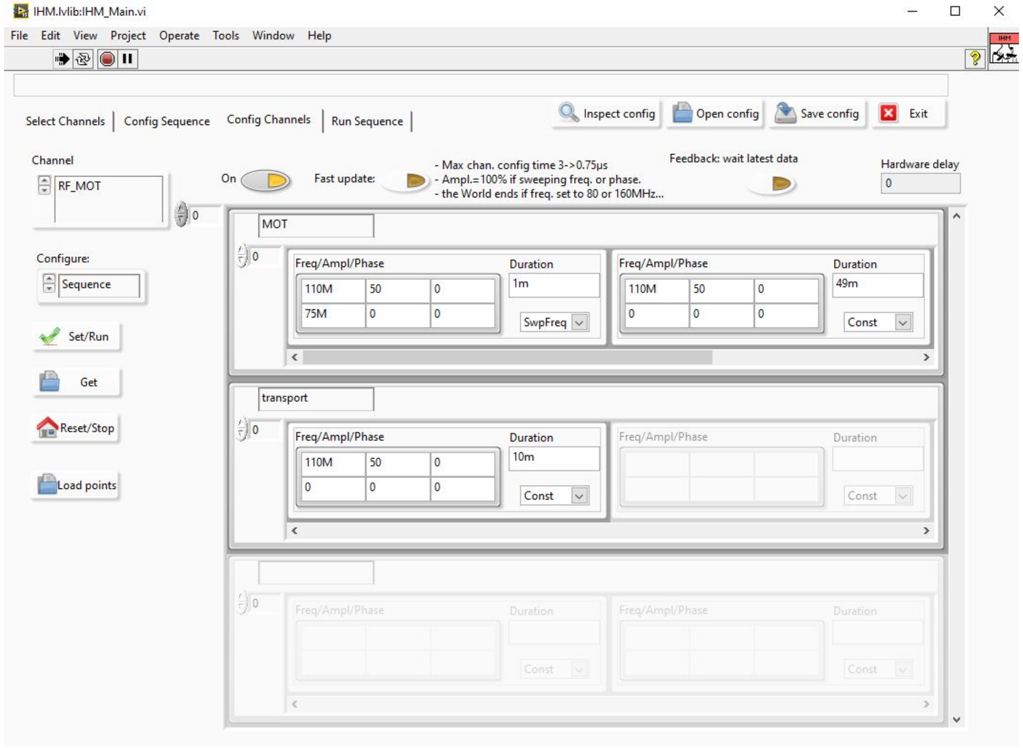


NI PXIe-1078 chassis

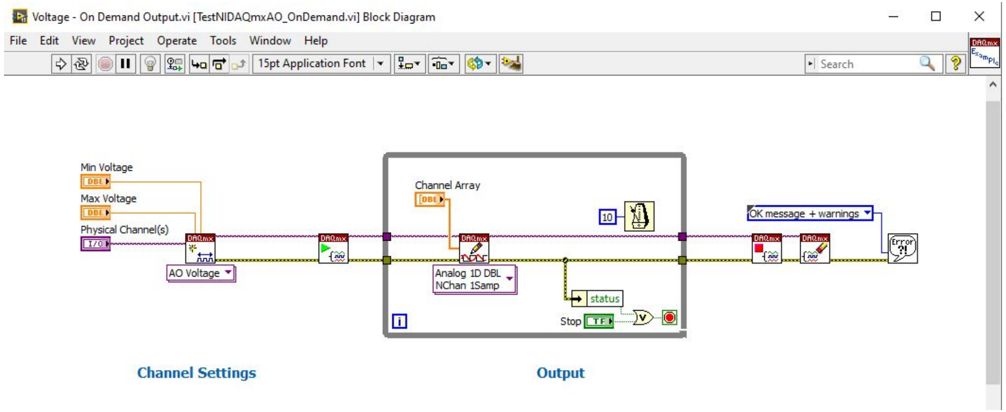
Software

VITO

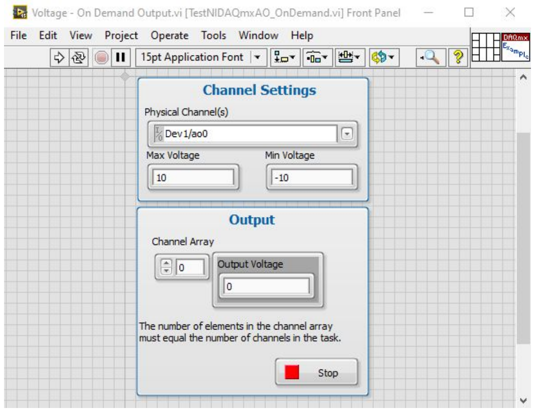
- Main control of the platform
- Home-made LabVIEW program



- **Lab**oratory **V**irtual **I**nstrument **E**ngineering **W**orkbench — 2015
- Design platform & development environment



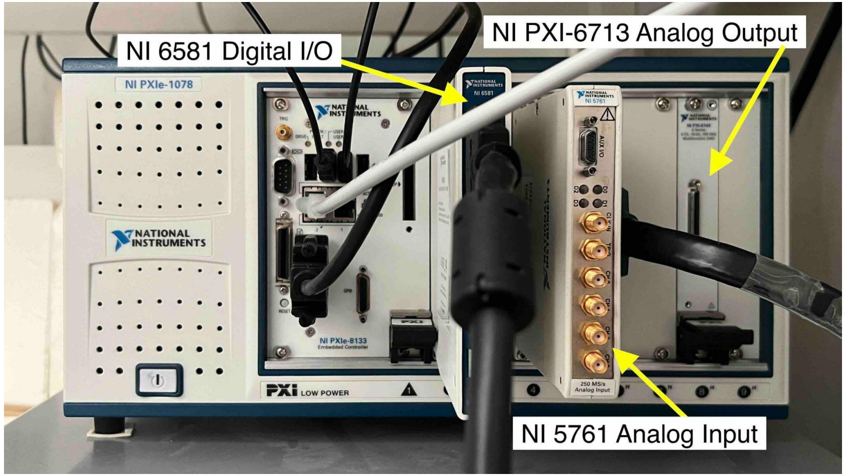
Block Diagram



Front Panel

NATIONAL INSTRUMENTS™ LabVIEW™

- Subscription starting in 2022
- Migration to open source alternatives
    - Cost reduction
    - Development efficiency
    - Experimental adaptability
- 3 Modules of interest



NI PXIe-1078 chassis

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NI PXI-6713 Analog Output

- NI-DAQmx instrument driver
- Translation from LabVIEW to Python & C
  - OnDemand, Finite
- Runtime tests :

OnDemand	Average Runtime (ms)	
	$V_{out} = 5$ V	$V_{out} = 7.5$ V
Python	2.085	2.130
C	1.904	1.800

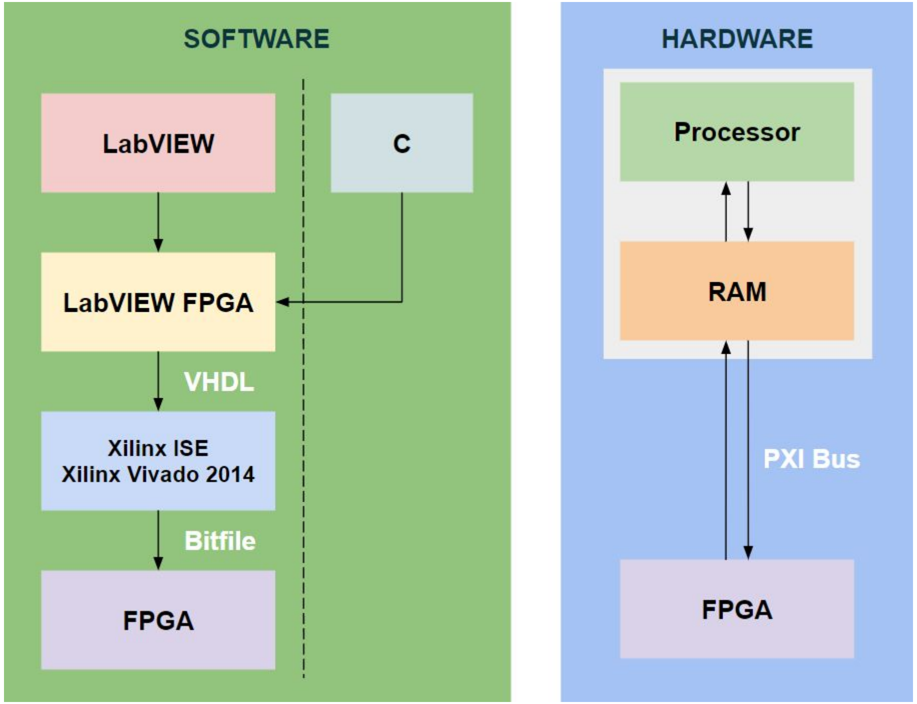
a. Average runtimes for the LabVIEW OnDemand program translated to Python and C. Each average runtime was calculated over 10 separate tests, with 10,000 runs per test. The constant, on-demand ouput analog voltage was set at 5 V and 7.5 V for different tests.

Finite	Average Runtime (ms)	
	$f = 0.1$ MHz	$f = 1$ MHz
Python	21.450	21.538
C	20.020	20.976

b. Average runtimes for the LabVIEW Finite program translated to Python and C. Each average runtime was calculated over 10 separate tests, with 1,000 runs per test. The sample time was fixed to 10 ms for all runs, while the sampling rate f was set to 0.1 MHz and the recommended maximum of 1 MHz for different tests.

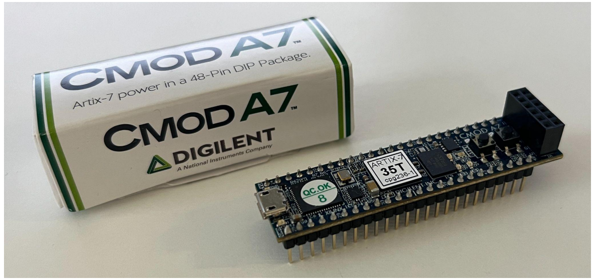
NI 6581 Digital I/O & NI 5761 Analog Input

- “Smart” modules with FPGAs
- Proprietary bottleneck
- Replace modules completely



Replacing NI FPGA Modules

Digilent Cmod A7-35T as Digital I/O



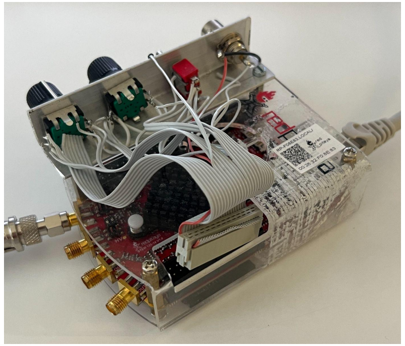
- 48 pins built around Xilinx Artix 7 FPGA
  - clock source, SRAM, basic I/O, etc
- Already used for some experimental control
- Can functionally replace a fraction of digital I/O
  - More effort is needed
- Intro to FPGAs & HDLs

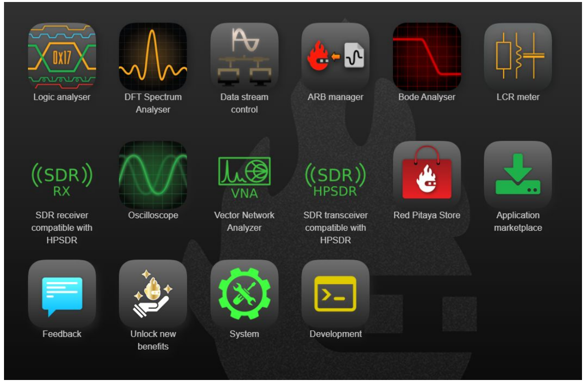
Key Specifications	Digilent Cmod A7-35T	NI 6581 Digital I/O
Number of I/O	44	54
Clock Frequency	> 100 MHz	100 MHz
Memory	512 KB SRAM	2 GB DRAM
Price	€ 92,50	€ 14.841,00

Table 2.1: Key specifications for the Digilent Cmod A7-35T and the NI 6581 Digital I/O modules.

Red Pitaya STEMlab 125-14 as Analog Input

- Single-board computer
  - Xilinx SoC (CPU, FPGA)
  - 125 MS/s I/O
  - 14-bit ADC & DAC
  - ethernet, etc
- Default applications
  - Alternative for lab equipments
- Data acquisition device
  - Sufficient memory
  - Noise limits
  - Discontinuous acquisition





Key Specifications	Red Pitaya STEMlab 125-14	NI 5761 Analog Input
Number of Inputs	2	4
ADC Sampling Rate	125 MHz	250 MHz
ADC Resolution	14-bit	14-bit
ADC Range	± 1 V (LV) and ± 20 V (HV)	± 1 V
Price	€ 465,60	€ 17.460,00

Table 2.2: Key specifications for the Red Pitaya STEMlab 125-14 and the NI 5761 Analog Input modules.

Experimental Data Acquisition

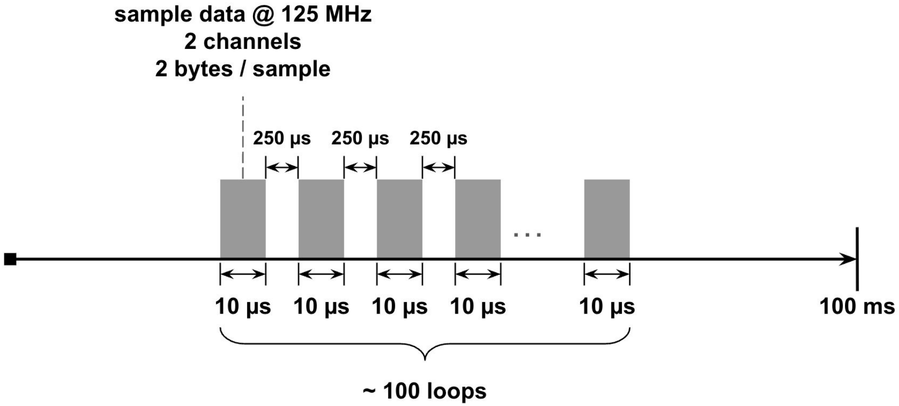
- NI 5761 Analog Input

  `4 channels · 250 MHz · 2 bytes/Sample · 10 µs/loop · 100 loops = 2 MB`

- Red Pitaya

  `2 channels · 120 MHz · 2 bytes/Sample · 10 µs/loop · 100 loops = 0.5 MB`

- Repeat every 130 ms



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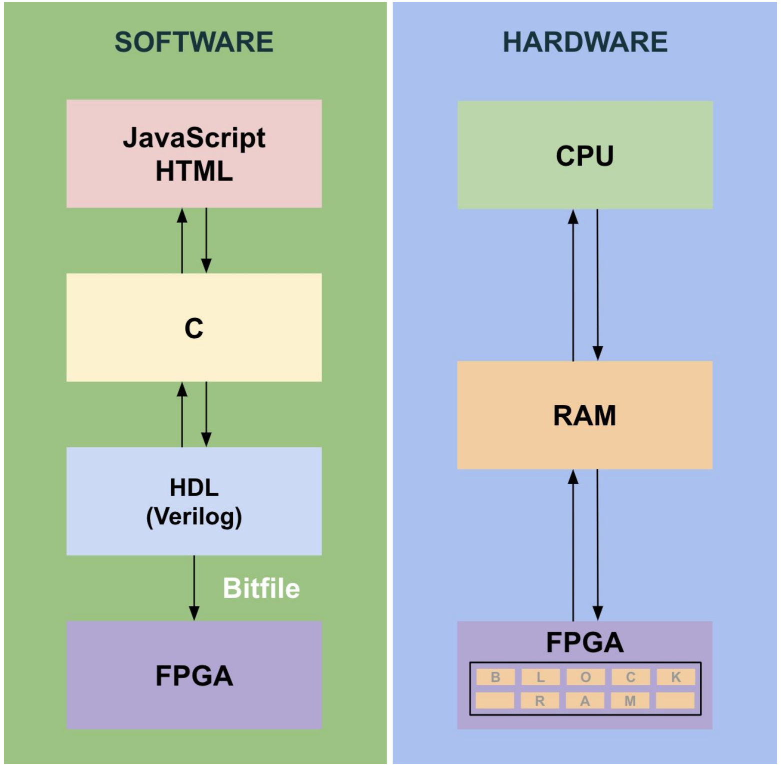
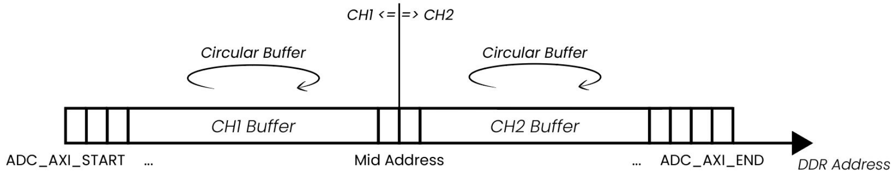
Red Pitaya: Input Data Memory Storage & Extension

- 512 MB on-board RAM
- Methods
  - Lock-in+PID with Oscilloscope
  - Data Streaming
  - Deep Memory Acquisition (DMA)

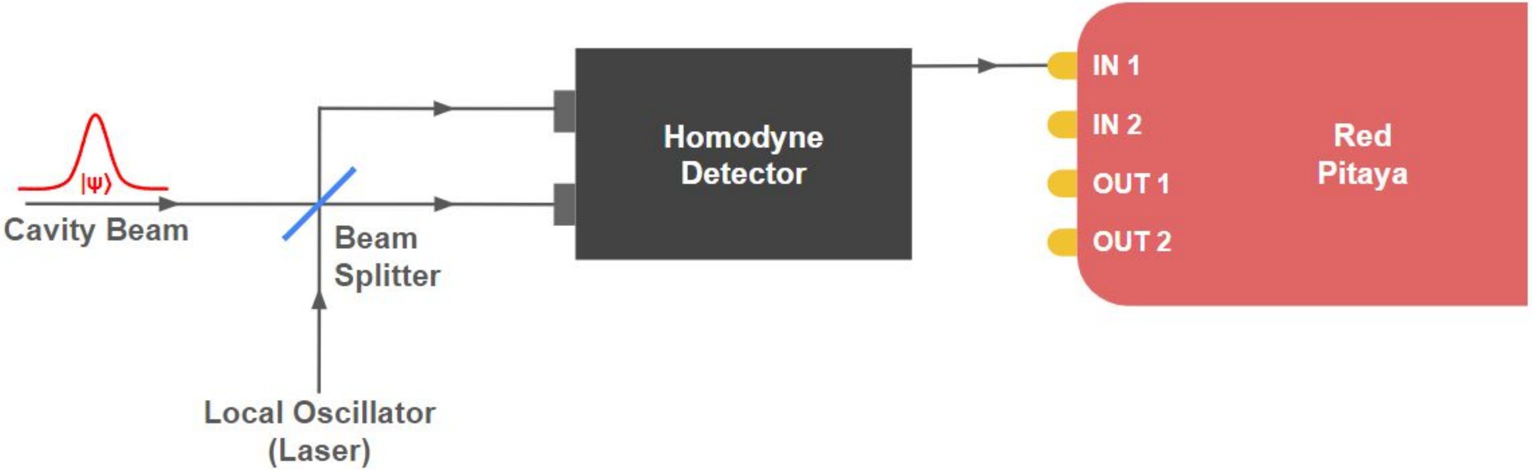


Deep Memory Acquisition (DMA)

- Variable ADC buffer RAM
  - Default : 2 MB
  - Max recommended : 412 MB
- 125 MS/s @ 32-bit resolution
- RAM reconfiguration & rebuild
  - 2 MB → 4 MB
- Remote ~ SCPI (Python / MATLAB)
- On-board ~ API (Python / C)
- Successful test acquisitions

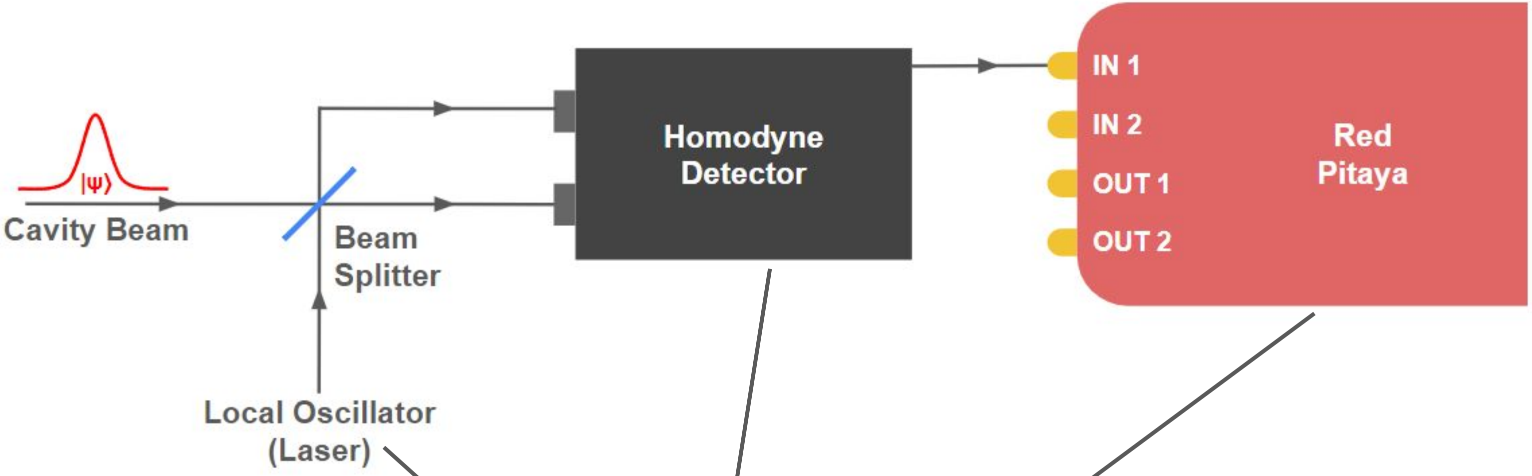


Homodyne Detection System with Red Pitaya



Homodyne Detection System with Red Pitaya

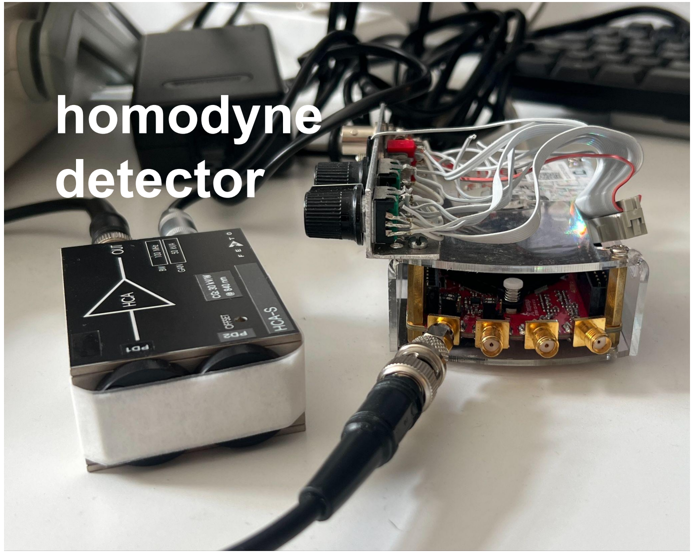
Noise

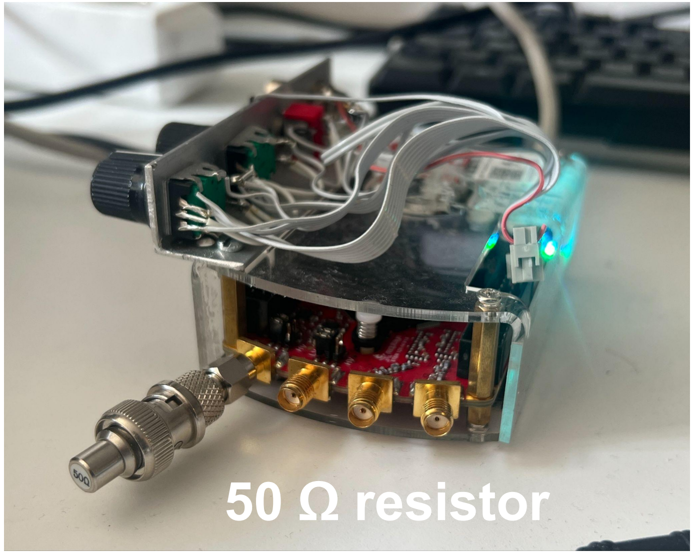


$$\boxed{\sigma^2_{\mathrm{SN}} \gg \sigma^2_{\mathrm{HDN}} + \sigma^2_{\mathrm{RPN}}}$$

Homodyne Detection System with Red Pitaya

Electronic Noise





$$\boxed{\sigma^2_{\mathrm{SN}} \gg \sigma^2_{\mathrm{HDN}} + \sigma^2_{\mathrm{RPN}}}$$

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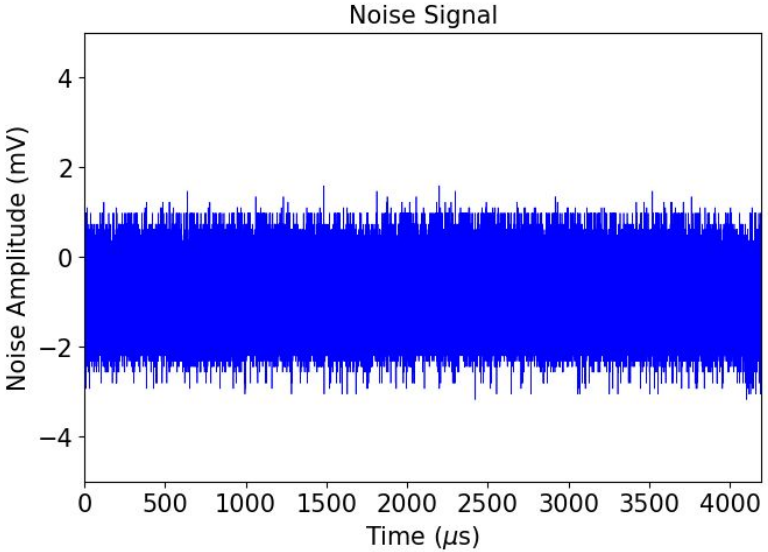
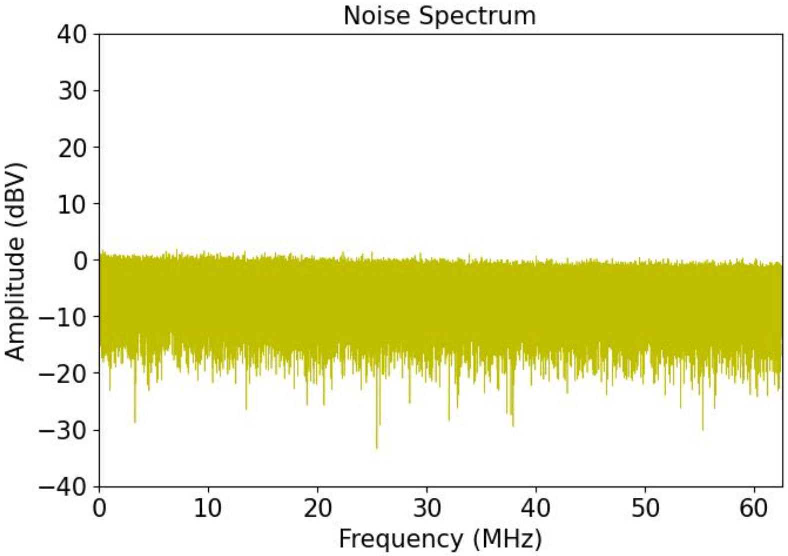
Red Pitaya: Intrinsic Electronic Noise

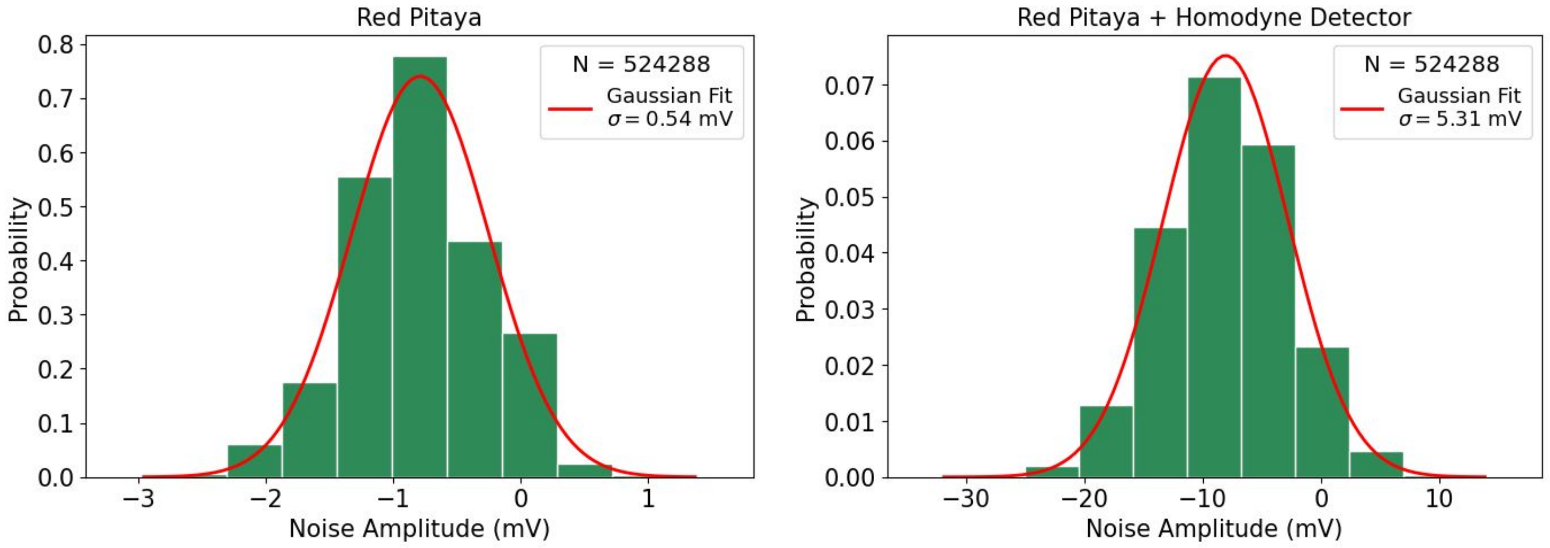
N = 524,288





Homodyne Detection System

Electronic Noise

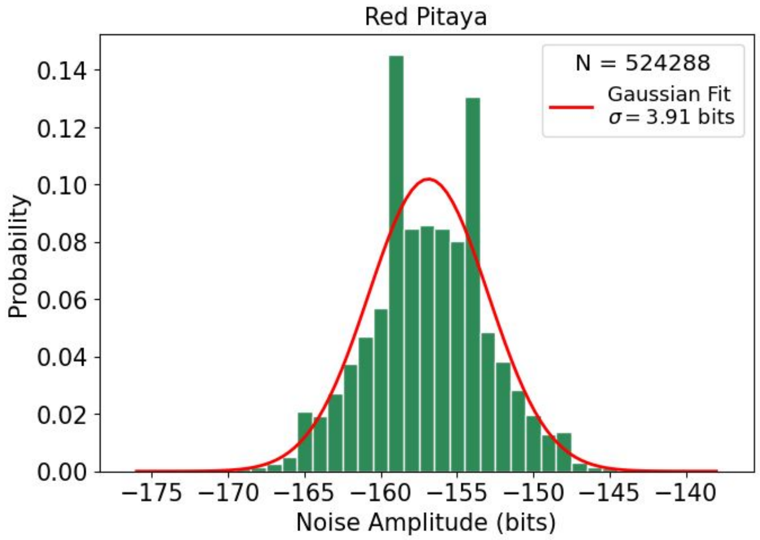


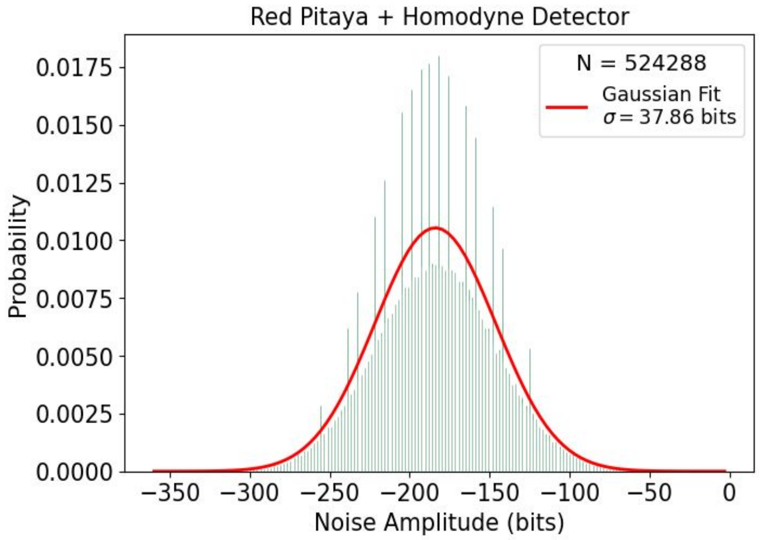
$$\sigma_{HDN}^{\ 2} + \sigma_{RPN}^{\ 2} = (5.31\ \text{mV})^2$$

$$\sigma_{HDN} = 27.88\ (\text{mV})^2 \quad >> \quad \sigma_{RPN}^{\ 2} = 0.29\ (\text{mV})^2$$

Homodyne Detection System

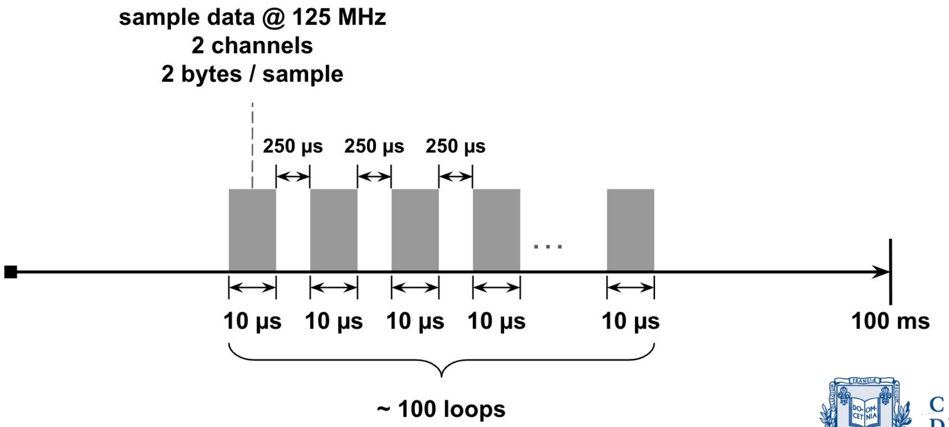
Electronic Noise: Bits





Conclusion

- Analog output w. Python / C
- Digital I/O w. Digilent Cmod A7-35T
- Analog input w. Red Pitaya
    - Noise distribution (bitwise resolution)
    - Discontinuous acquisition

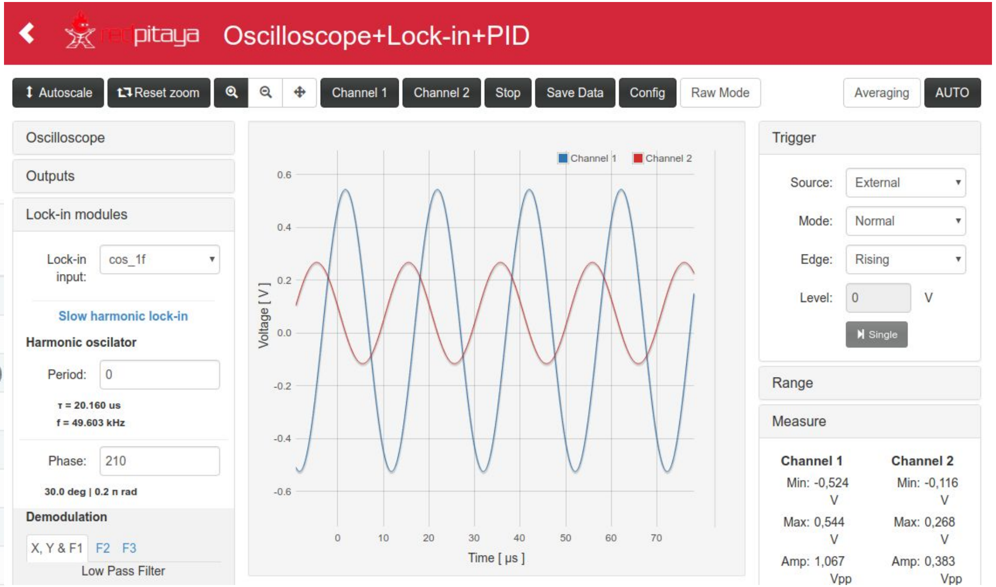


Annex

Lock-in+PID with Oscilloscope Application

- Maintains intensity of probe beam
- 1 IP core dedicated
  - 16^5 bytes ~ 1 MB
  - Channel A: `0x40110000`
  - Channel B: `0x40120000`

	Start	End	Module Name
CS[0]	0x40000000	0x400FFFFF	Housekeeping
CS[1]	0x40100000	0x401FFFFF	Oscilloscope
CS[2]	0x40200000	0x402FFFFF	Arbitrary signal generator (ASG)
CS[3]	0x40300000	0x403FFFFF	PID controller
CS[4]	0x40400000	0x404FFFFF	Analog mixed signals (AMS)
CS[5]	0x40500000	0x405FFFFF	Daisy chain
CS[6]	0x40600000	0x406FFFFF	FREE
CS[7]	0x40700000	0x407FFFFF	Power test



Methodology

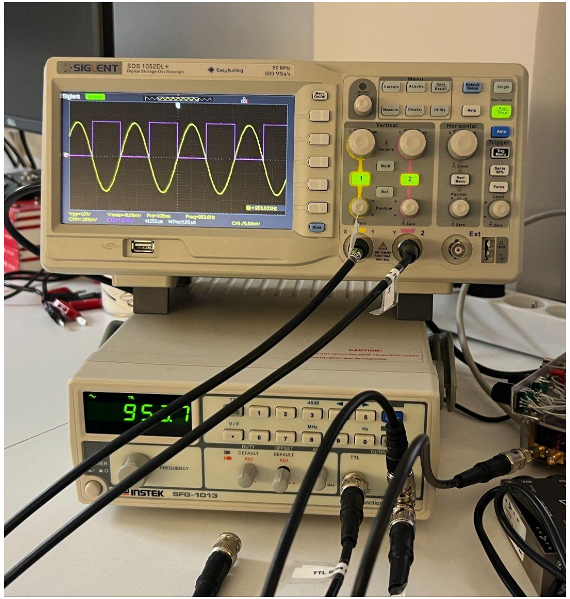
- Hardware modification
    - 4-byte single-channel → dual-channel storage
        - 4-byte → 2-byte per sample
        - 16,384 → 131,072 samples
    - Per channel (8x more samples)
        - `0x4012FFFF` → `0x4018FFFF`
        - $16^4 \rightarrow 8 * 16^4$ bytes
        - 65 KB → 0.25 MB !!!
- Software modification

Tests

- RAM monitor
- Sampling one waveform

$$f_{\text{full}} = \frac{\text{sampling rate}}{\text{max number of samples storable in memory at once}}$$

- Original
  - f_{full} = 7629 Hz, T_{full} = 131 μs
- Extended
  - f_{full} = 954 Hz, T_{full} = 1049 μs



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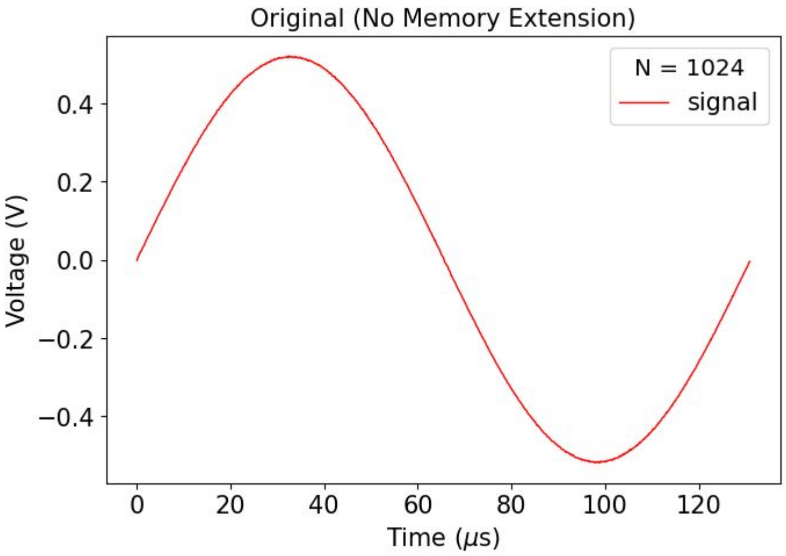
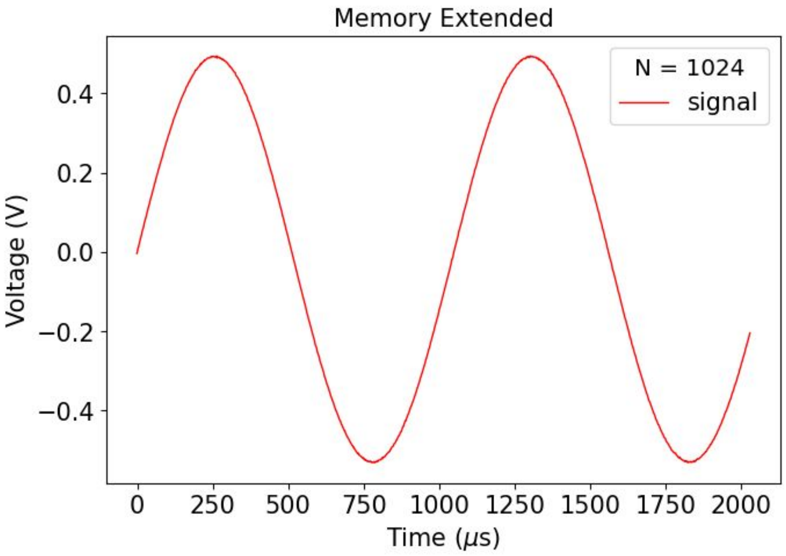
Results





$f_{\text{full}} = 7629$ Hz, $T_{\text{full}} = 131\ \mu s$

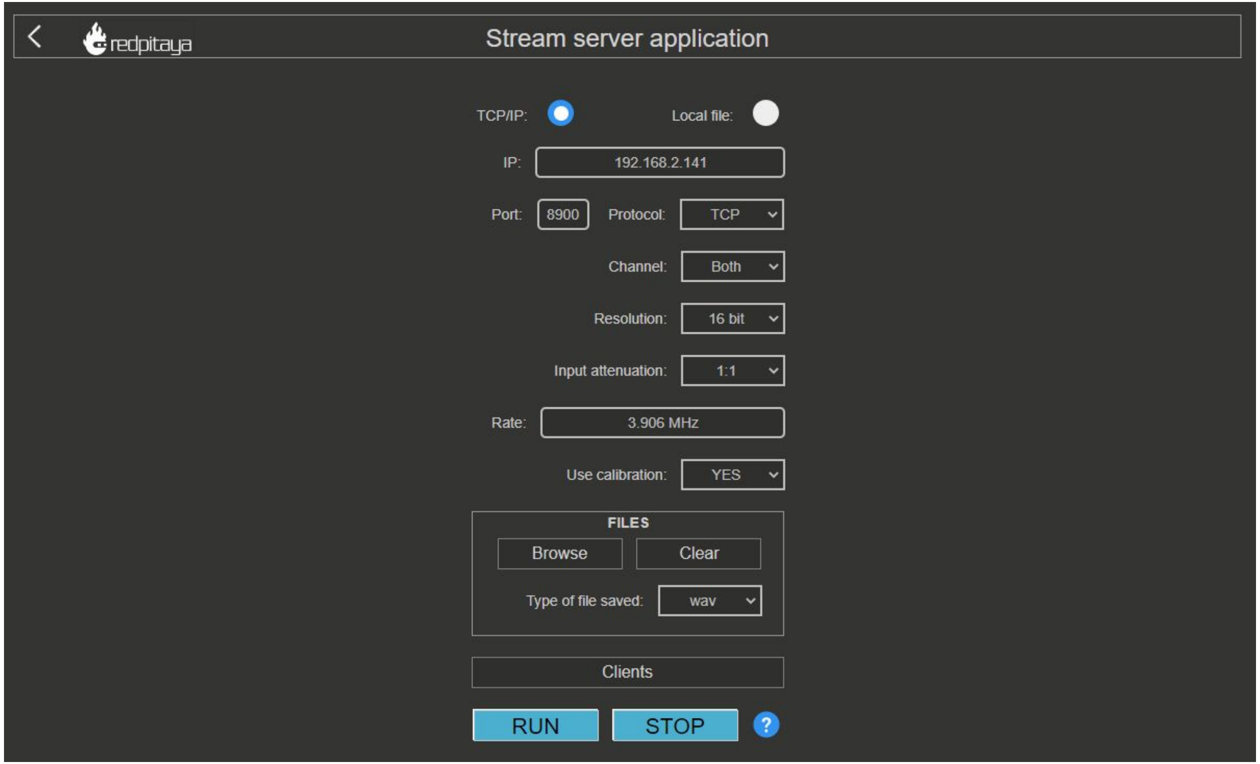
$f_{\text{full}} = 954$ Hz, $T_{\text{full}} = 1049\ \mu s$

Conclusion

- Buggy waveform behavior
- Front-end decimation
- Not practical for DAQ

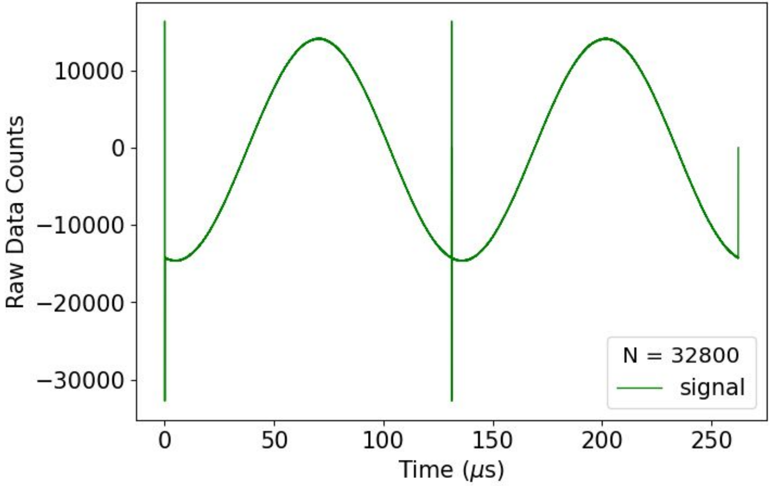
~~Lock-in+PID with Oscilloscope Application~~

Data Streaming Application



Tests & Results

- Assumption for default allocation
  - 16^4 bytes = 65 KB = 32,768 samples (16 bits / sample)
  - f_{full} = 3815 Hz
  - 125 MS/s



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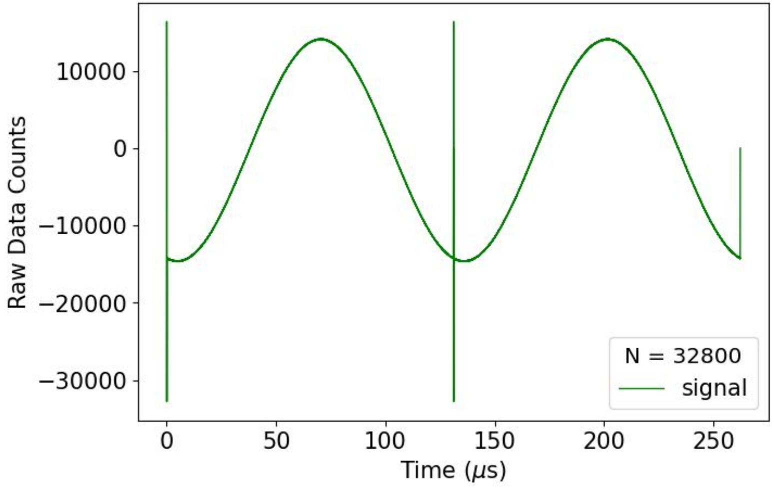
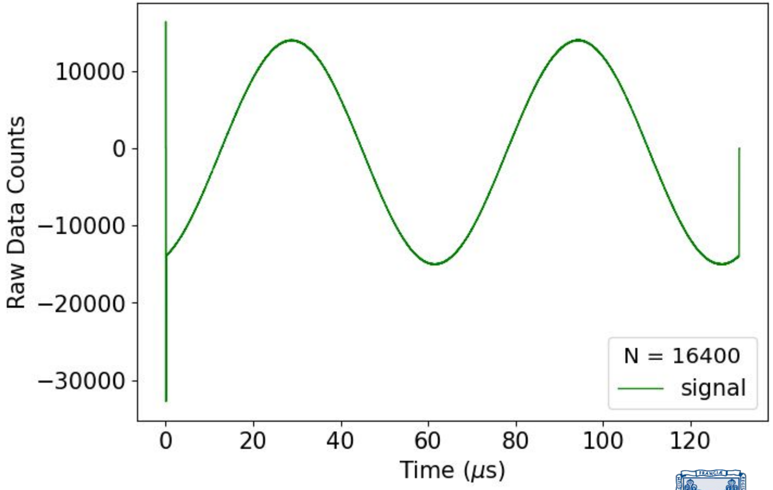
Tests & Results

$$f_{\mathrm{full}} = \frac{\text{sampling rate}}{\text{max number of samples storable in memory at once}}$$

- Assumption vs. verification
  - 16^4 bytes = 65 KB = 32,768 samples → $16^4/2$ bytes = 32 KB = 16,400 samples
  - f_{full} = 3815 Hz → f_{full} = 7629 Hz
  - 125 MS/s → 62.5 MS/s





Conclusion

- Sampling rate field is buggy
- Issues remain in newest ecosystem
- Also not a practical for DAQ

~~Data Streaming Application~~

DMA Code Structure

- Configure signal units, decimation, and trigger source and level
- Get reserved memory region address and size
- Set DMA buffer address and size for each input channel
- Continuously acquire data until buffer is full
- Read data from buffer
- Process and save data to external file

DMA Tests & Results

2 MB / channel

f_{full} = 238 Hz