Metal Oxide Semiconductor Capacitor

Problem - 1

An Al-gate n-channel MOS device is made on a p-type Si substrate with $N_A=10^{17}$ /cm^3. The SiO_2 thickness is 100 A^o in the gate region, and the effective interface charge Q_i is $5x10^{10}q$ C/cm^2.

(a) Find maximum depletion width, flat band voltage and threshold voltage.

(b) Sketch the C-V curve for this device and give important numbers for the scale.

Problem - 2

An Al-gate p-channel MOS device is made on an n-type Si substrate with $N_D=10^{17}$ /cm^3. The SiO_2 thickness is 100 A^o in the gate region, and the effective interface charge Q_i is $5x10^{10}q$ C/cm^2.

(a) Find maximum depletion width, flat band voltage and threshold voltage.

(b) Sketch the C-V curve for this device and give important numbers for the scale.

Problem - 3

Find the threshold voltage for a Si n-channel MOS transistor with $N_A=10^{17}$ /cm^3, Φ_{ms} = -0.95 V, $Q_i=10^{11}q$ C/cm^2, and an SiO_2 thickness d=200 A^o.

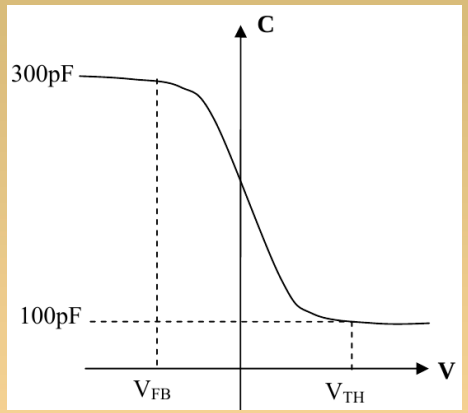
Problem - 4

(a) Find the voltage V_{FB} required to reduce to zero the negative charge induced at the semiconductor surface by a sheet of positive charge Q_{ox} located x' below the metal.

(b) In case of an arbitrary distribution of charge ρ(x') in the oxide, show that

$$V_{FB} = \frac{-1}{C_{ox}} \int_0^d \rho(x')\, dx'$$

Problem - 5



From the given C-V characteristics of a MOS capacitor, pick the correct statement below:

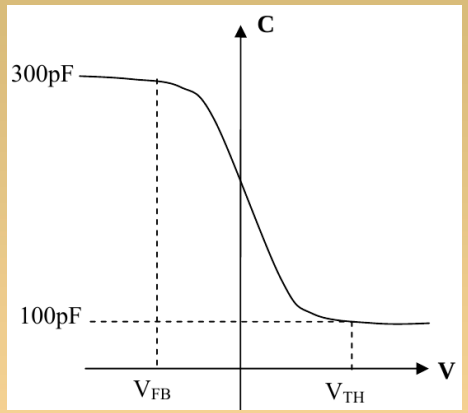
(A) The substrate is n-type and the measurement is done at low frequency.

(B) The substrate is p-type and the measurement is done at low frequency.

(C) The substrate is n-type and the measurement is done at high frequency.

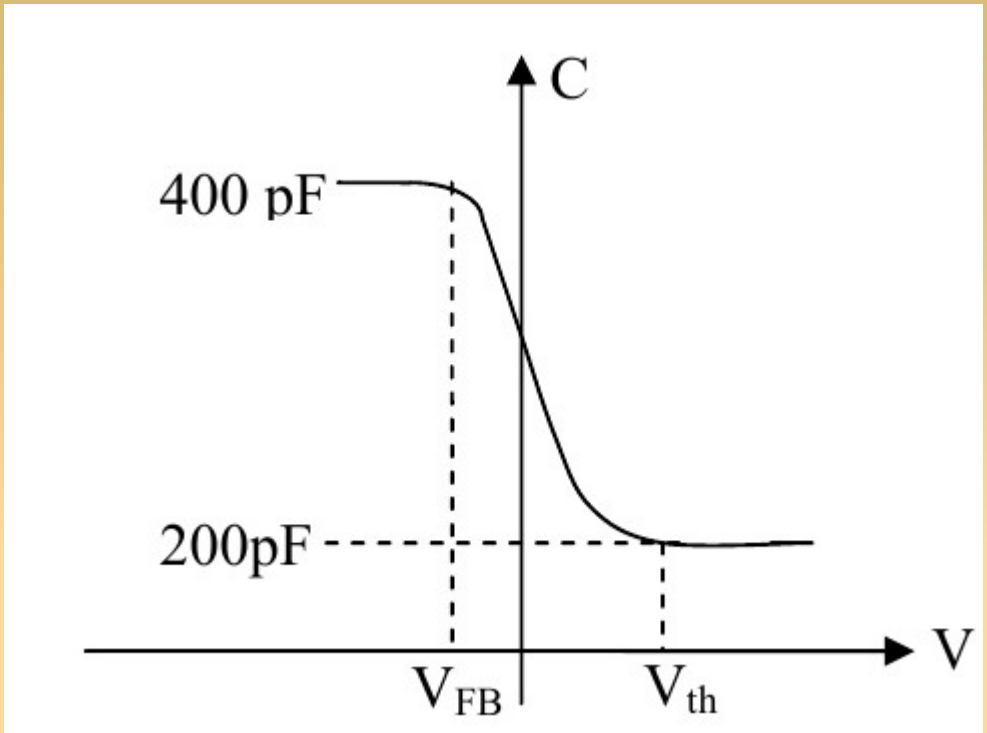
(D) The substrate is p-type and the measurement is done at high frequency

Problem - 6



For the given C-V characteristics of a MOS capacitor with an area of 1.5 mm^2. What is the maximum depletion layer width (W_{max}) in μm?

Problem - 7



In the given figure, if the area of the capacitor is 1 mm^2,

(a) what is the gate oxide thickness (t_{ox})?

(b) what is the maximum depletion layer width (W_{max})?

Problem - 8

If the area of a MOS capacitor is 1 mm^2 and the gate oxide thickness (t_{ox}) is 100nm,

(a) what is C_{max}?

(b) if $C_{min} = 0.5C_{max}$, what is the maximum depletion layer width (W_{max})?

Problem - 9

A MOS capacitor has an area of 2×10^{-3} cm^2. The substrate doping concentration is $10^{16}/cm^3$. If the maximum and minimum capacitances of the MOS capacitor are 350 pF and 200pF respectively, what is the maximum depletion width?

Problem - 10

In a metal/SiO_2/p-Si MOS capacitor, the SiO_2 layer thickness is t_{ox} and the doping concentration of the p-type substrate is N_A. The threshold voltage of the MOS capacitor will definitely increase if

(A) t_{ox} is decreased and N_A is increased

(B) t_{ox} is increased and N_A is decreased

(C) both t_{ox} and N_A are decreased

(D) both t_{ox} and N_A are increased.