MOS Transistor: Threshold voltage and drain current, small-signal model and short channel effect

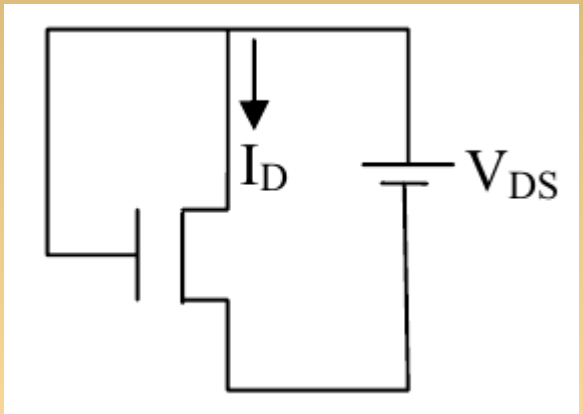
Problem - 1

Draw the drain current versus drain voltage characteristics of an n-type MOSFET for three different gate voltages. Clearly show the saturation and ohmic regions, and the relative spacing between the saturation segments of the curves assuming equal increments in gate voltage.

Problem - 2

The threshold voltage (V_{TH}) of an n-channel MOSFET is 1V. If the drain current (I_D) is 10μA when drain-to-source voltage (V_{DS}) is 3V and gate-to-source voltage (V_{GS}) is 2V, find out the value of I_D in μA when $V_{DS} = V_{GS} = 4V$.

Problem - 3



An n-channel MOSFET with threshold voltage (V_{th}) of 1 V has its gate shorted to drain as shown in the figure. If the drain current (I_D) = 2 mA when V_{DS} = 2 V, what is I_D when V_{DS} = 4 V?

Problem - 4

A MOSFET with threshold voltage (V_{TH}) of 1V has its gate and drain tied together and is used as a voltage variable resistor. A d.c resistance ($R = V_{DS}/I_D$) of 1 kΩ is seen between source and drain when $V_{DS} = V_{GS} = 10V$. What is the value of R when $V_{DS} = V_{GS} = 5V$.

Problem - 5

In an n-channel MOSFET having a threshold voltage (V_{th}) of 1 V, the drain current (I_D) is 2 mA when $V_{GS} = V_{DS} = 2V$, where V_{GS} and V_{DS} are the gate-to-source voltage and drain-to-source voltage, respectively. What is I_D when $V_{GS} = 4V$ and $V_{DS} = 2V$?

Problem - 6

An n-channel MOSFET has the following specifications: channel width W=5 μm, channel length L=1 μm, gate oxide thickness t_{ox} = 50 nm, surface electron mobility = 800 cm^2/V-s, threshold voltage V_{th}=1 V. Find the drain current (I_D) flowing through the device for the following conditions:

(a) V_{GS} = 2 V, V_{DS} = 0.5 V.

(b) V_{GS} = 2 V = V_{DS}.

Problem - 7

An n^+-poly gate n-channel MOSFET has a substrate doping concentration of 10^{16} /cm^3 and a gate oxide thickness of 100 nm. What will be the change in its threshold voltage if the source-to-substrate voltage is increased to 2 V from zero?

Problem – 8

Calculate the drain current, gd and gm of an n-channel MOSFET with W/L=10, V_{TH}=0.5 V, μ_n=500 cm^2/V-s, and oxide thickness of 0.12 μm with (a) V_{DS}=0.2 V, (b) 2 V and (c) in the saturation region. Assume V_{GS}=4 V in all the calculations.

If this MOSFET and a BJT are to be evaluated for use in a linear amplifier with a quiescent current of 2mA. Calculate the ratio of the transconductances of the two devices and answer which of the two devices will be more suitable for use in the amplifier.

Problem - 9

Derive the complete small-signal model for an nMOS transistor with I_D=100 μA, V_{SB}=1 V, V_{DS}=2V. Device parameters are ϕ_F=0.3 V, W=10 μm, L=1μm, body effect parameter γ=0.5 $V^{0.5}$, μC_{ox}=200 $\mu A/V^2$, λ=0.02 V^{-1}, t_{ox}= 100 angstroms, built-in potential for source-body and drain-body step p-n junctions is V_{bi}=0.6 V, C_{sb0}=C_{db0}=10 fF. Additional bias-independent overlap capacitance from gate-to-source and gate-to-drain is 1 fF, and C_{gb}=5 fF.

Problem - 10

A MOSFET is fabricated on p-type Si substrate having a doping concentration of $N_A=5x10^{15}$ /cm^3. The gate oxide thickness is 200 angstrom. As gate material, n^+ poly-Si is used and the device has a fixed oxide charge density $Q_f/q= 10^{11}$ /cm^2. The MOSFET is operated with V_{BS}=-2 V. The channel length and width of this device is given by L=1 μm and W=5 μm. Calculate $V_{D,sat}$ and $I_{D,sat}$ for V_{GS}=5 V.

Problem - 11

Calculate the values of the $V_{D,sat}$ and $I_{D,sat}$ when V_{GS}=2 V for n-channel MOSFET with V_{TH}=1 V considering field-dependent mobility. Assume L=1μm, W=5 μm, t_{ox}=20 nm, μ_n=500 cm^2/V-s, m=1.05 and E_c=5x10^4 V/cm.

What will be the values of $V_{D,sat}$ and $I_{D,sat}$ if is assumed that the current saturation occurs under pinch-off condition? Calculate the source resistance that can be used to model the velocity saturation effect under this simple pinch-off guided saturation model.

Problem - 12

Under the condition of VDS=VBS=0, it is commonly assumed that the surface potential ϕ_s is pinned at $2\phi_F$ once the inversion layer is formed. In fact ϕ_s still rises slightly as the gate voltage and inversion charge density increase. Show that a second order correction term yields

$$\phi_s = 2\phi_F + 2\frac{kT}{q}\ln\left(\frac{C_{ox}\left(V_G - V_{FB} - 2\phi_F\right)}{\sqrt{\left(2\epsilon_{si}kTN_a\right)}}\right)$$