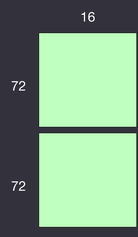
Given some Input Tensor w/ dims: 12x12x16

Dims [0, N-1] are always tightly packed physically in memory

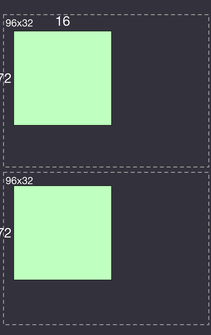
Regardless of RM or tiled,
shard shape is expressed as 2D logical shape that divides the above form. Here we have shard shape 72x16



Tile Shape is independently programmed, a [1, N] tile means row major. FPU and Noc have constraints that need to be enforced.

The physical shard shape is always the logical shard shape padded out to tile shape.

Here we've programmed a tile shape of 32x32 this implicitly bumps the physical shard shape to 96x32.



Let's consider a new case where we want dim=-2 padded to tile, we need to use explicit strides in order to achieve this.

Again, given some Input Tensor w/ dims: 12x12x16

By default the stride for this tensor would be:
192x16x1

To "pad" dim=-2 out to multiples of 32 we'd instead explicitly program:
512x16x1

Dims [0, N-1] are always tightly packed physically in memory

Again, logical shard shape divides the form above.
One possible shard shape 96x16

Again, physical shape gets padded to tile.
Again, here tile is 32x32