# W802 chip specification sheet

V1.1



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**Document modification record**

| Version revision time | Revision history | author | review |
|---|---|---|---|
| V1.0 | 2023/7/17 Create document | HMX | CYC,LGH |
| V1.1 | 2023/8/2 Add silk screen information | HMX | |
| | | | |

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## 1 Overview

The W802 chip is a secure IoT Wi-Fi/Bluetooth dual-mode SoC chip. The chip provides rich digital function interfaces. Support 2.4G IEEE802.11b/g/n Wi-Fi communication protocol; supports BT/BLE dual-mode working mode and BT/BLE4.2 protocol. Chip integrated 32-bit CPU processor, built-in UART, GPIO, SPI, I 2C, I 2S, 7816, SDIO, ADC, PSRAM, Touch Sensor and other digital interfaces port; supports TEE security engine, supports multiple hardware encryption and decryption algorithms, built-in DSP, floating point operation unit and security engine, supports code security rights Limit settings, support multiple security measures such as firmware encrypted storage, firmware signature, secure debugging, secure upgrade, etc. to ensure product security features. Applicable to It is used in a wide range of IoT fields such as smart home appliances, smart homes, smart toys, wireless audio and video, industrial control, and medical monitoring.

## 2 features

ÿ Chip appearance

ÿ QFN56 package, 6mm x 6mm

ÿMCU Features

ÿ Integrated 32-bit XT804 processor, operating frequency 240MHz, built-in DSP, floating point operation unit and security engine

ÿ Integrated PSRAM interface, supports up to 64M bit external PSRAM memory

ÿ Integrated high-speed QSPI interface, supports external Flash memory

ÿ Integrated 6-channel UART high-speed interface, supporting up to 2M bps

ÿ Integrated 4-channel 12-bit ADC, maximum sampling rate 1KHz

ÿ Integrated 1 high-speed slave SPI interface, supporting up to 50MHz

ÿ Integrated 1 master/slave SPI interface

ÿ Integrated 1 SDIO_HOST interface, supports SDIO2.0, SDHC, MMC4.2

ÿ Integrate 1 SDIO_DEVICE, support SDIO2.0, maximum operating frequency 200Mbps

ÿ Integrated 1 I 2C controller

ÿ Integrated GPIO controller, supports up to 37 GPIOs

ÿ Integrated 5-way PWM interface

ÿ Integrated 1-way Duplex I 2S controller

ÿ Integrated 1 7816 interface

ÿ Integrated 13 Touch Sensors

ÿ Integrated 1-way Wakeup interface

ÿ Security Features

ÿ The MCU has a built-in Tee security engine, and the code can distinguish between the secure world and the non-secure world.

ÿ Integrated SASC/TIPC, memory and internal modules/interfaces can be configured with security attributes to prevent non-security code access

ÿ Enable firmware signature mechanism to achieve safe boot/upgrade

ÿ Equipped with firmware encryption function to enhance code security

ÿ Firmware encryption keys are distributed using asymmetric algorithms to enhance key security

ÿ Hardware encryption module: RC4, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number generator

ÿ Wi-Fi Features

ÿ Support GB15629.11-2006, IEEE802.11 b/g/n

ÿ Support Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS

ÿ Support EDCA channel access method

ÿ Support 20/40M bandwidth working mode

ÿ Supports STBC, GreenField, Short-GI, and reverse transmission

ÿ Support AMPDU, AMSDU

ÿ Supports IEEE802.11n MCS 0~7 and MCS32 physical layer transmission rate levels, with the transmission rate up to 150Mbps

ÿ Supports Short Preamble when sending at 2/5.5/11Mbps rate

ÿ Supports HT-immediate Compressed Block Ack, Normal Ack, and No Ack response methods

ÿ Support CTS to self

ÿ Supports Station, Soft-AP, Soft-AP/Station functions

ÿ Bluetooth features

ÿ Integrated Bluetooth baseband processor/protocol processor, supports BT/BLE dual-mode working mode, and supports BT/BLE4.2 protocol

ÿ Low power consumption mode

ÿ 3.3V single power supply

ÿ Support Wi-Fi energy-saving mode power consumption management

ÿ Supports work, sleep, standby, and shutdown working modes

ÿ Standby power consumption is less than 10uA

## 3 chip structure

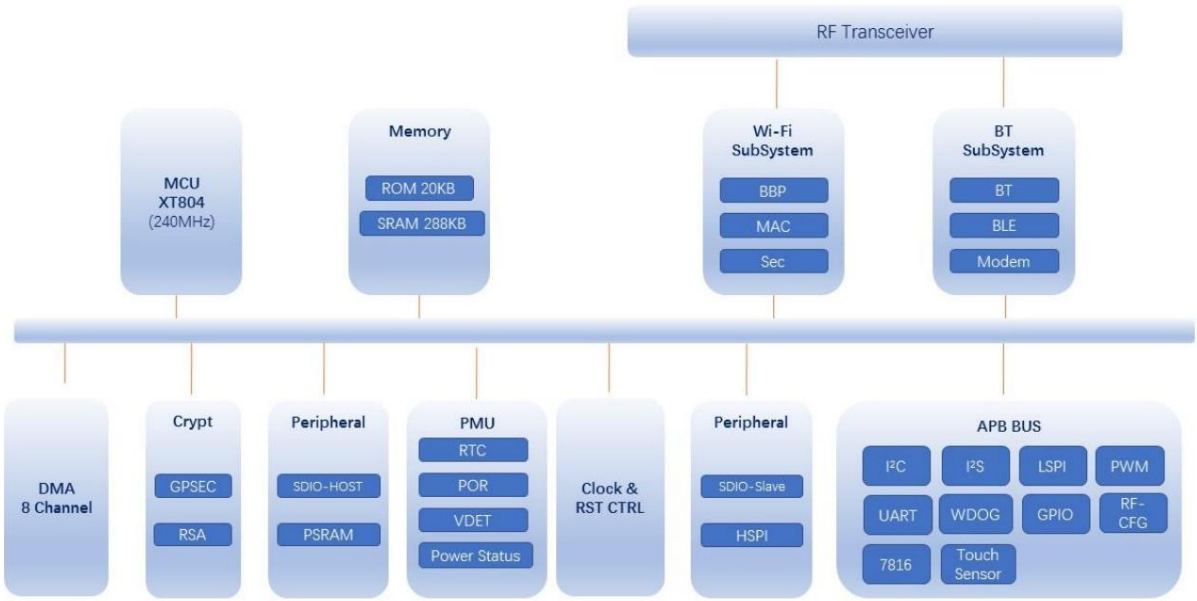


Figure 3-1 W802 chip structure diagram

## 4 Address space division

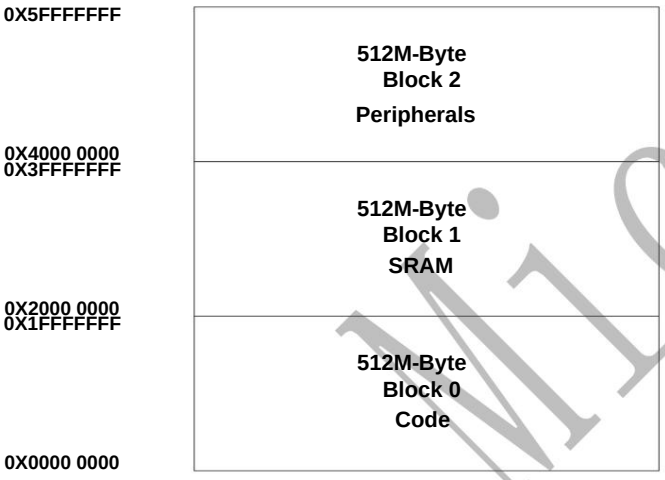



Figure 4-1 Address space mapping

Table 4-1 Detailed division of bus device address space

| bus slave | BootMode=0 | Address space segmentation | Remark |
|---|---|---|---|
| ROM | 0x0000 0000 ~ 0x0000 4FFF | | Store the solidified firmware code |
| FLASH | 0x0800 0000 ~ 0x0FFF FFFF | | As a dedicated instruction memory. |
| SRAM | 0x2000 0000 ~ 0x2002 7FFF | | Firmware Memory and Instruction Store |
| Mac RAM 0x2002 8000 ~ 0x2004 7FFF | | | SDIO/H-SPI/UART data cache |

| | | | |
|---|---|---|---|
| PSRAM | 0x3000 0000 ~ 0x3080 0000 | | Peripheral memory |
| CONFIG | 0x4000 0000 ~ 0x4000 2FFF | 0x4000 0000 ~ 0x4000 05FF | RSA configuration space |
| | | 0x4000 0600 ~ 0x4000 07FF | GPSEC configuration space |
| | | 0x4000 0800 ~ 0x4000 09FF | DMA configuration space |
| | | 0x4000 0A00 ~ 0x4000 0CFF | SDIO_HOST configuration space |
| | | 0x4000 0D00 ~ 0x4000 0DFF | PMU configuration space |
| | | 0x4000 0E00 ~ 0x4000 0EFF | Clock and Reset configuration space |
| | | 0x4000 0F00 ~ 0x4000 0FFF | MacPHY Router configuration space |
| | | 0x4000 1000 ~ 0x4000 13FF | BBP configuration space |
| | | 0x4000 1400 ~ 0x4000 17FF | MAC configuration space |
| | | 0x4000 1800 ~ 0x4000 1FFF | SEC configuration space |
| | | 0x4000 2000 ~ 0x4000 21FF | FLASH Controller configuration space |
| | | 0x4000 2200 ~ 0x4000 23FF | PSRAM_CTRL configuration space |
| | | 0x4000 2400 ~ 0x4000 25FF | SDIO Slave configuration space |
| | | 0x4000 2600 ~ 0x4000 27FF | H-SPI configuration space |
| | | 0x4000 2800 ~ 0x4000 29FF | SD Wrapper configuration space |
| | | 0x4000 2A00 ~ 0x4000 A9FF | BT Core configuration space |
| | | 0x4000 B000 ~ 0x4000 B0FF | SASC-B1 Level 1 bus memory security Configuration module |
| | | 0x4000 B100 ~ 0x4000 B1FF | SASC-Flash Flash security configuration |

| | | | |
|---|---|---|---|
| | | | module |
| | | 0x4000 B200 ~ 0x4000 B2FF SASC-B2 secondary bus memory security Configuration module | |
| APB | 0x4001 0000 ~ 0x4001 C000 | 0x4001 0000 ~ 0x4001 01FF I 2C master | |
| | | 0x4001 0200 ~ 0x4001 03FF Sigma ADC | |
| | | 0x4001 0400 ~ 0x4001 05FF SPI master | |
| | | 0x4001 0600 ~ 0x4001 07FF UART0 | |
| | | 0x4001 0800 ~ 0x4001 09FF UART1 | |
| | | 0x4001 0A00 ~ 0x4001 0BFF UART2 | |
| | | 0x4001 0C00 ~ 0x4001 0DFF UART3 | |
| | | 0x4001 0E00 ~ 0x4001 0FFF UART4 | |
| | | 0x4001 1000 ~ 0x4001 11FF | |
| | | 0x4001 1200 ~ 0x4001 13FF GPIO-A | |
| | | 0x4001 1400 ~ 0x4001 15FF GPIO-B | |
| | | 0x4001 1600 ~ 0x4001 17FF WatchDog | |
| | | 0x4001 1800 ~ 0x4001 19FF Timer | |
| | | 0x4001 1A00 ~ 0x4001 1BFF RF_Controller | |
| | | 0x4001 1C00 ~ 0x4001 1DFF | |
| | | 0x4001 1E00 ~ 0x4001 1FFF PWM | |
| | | 0x4001 2000 ~ 0x4001 21FF I²S | |
| | | 0x4001 2200 ~ 0x4001 23FF BT-modem | |
| | | 0x4001 2400 ~ 0x4001 25FF | |

| | | | |
|---|---|---|---|
| | | 0x4001 2600 ~ 0x4001 27FF TIPC | Interface security settings |
| | | 0x4001 4000 ~ 0x4001 BFFF RF_BIST DAC transmit memory | |
| | | 0x4001 C000 ~ 0x4003 BFFF RF_BIST ADC receiving memory | |
| | | 0x4003 C000 ~ 0x5FFF FFFF RSV | |

**5 Function description**

## 5.1 SDIO HOST controller

The SDIO HOST device controller provides a digital interface to access Secure Digital Input and Output Cards (SDIO) and MMC cards. were able

Access SDIO devices and SD card devices that are compatible with the SDIO 2.0 protocol. The main interfaces are CK, CMD and 4 data lines.

- ÿ Compatible with SD card specification 1.0/1.1/2.0 (SDHC)
- ÿ Compatible with SDIO memory card specification 1.1.0
- ÿ Compatible with MMC specification 2.0~4.2
- ÿ Configurable interface clock rate, supports host rate 0~50MHz
- ÿ Support standard MMC interface
- ÿ Supports Blocks up to 1024 bytes
- ÿ Support soft reset function
- ÿ Automatic Command/Response CRC generation/verification
- ÿ Automatic data CRC generation/verification
- ÿ Configurable timeout detection
- ÿ Supports SPI, 1-bit SD and 4-bit SD modes
- ÿ Support DMA data transfer

## 5.2 SDIO Device Controller

SDIO2.0 device-side interface completes the interaction with host data. Internally integrated 1024Byte asynchronous FIFO to complete the data between the host and the chip Interaction.

- ÿ Compatible with SDIO card specification 2.0
- ÿ Support host speed 0~50MHz
- ÿ Supports Blocks up to 1024 bytes
- ÿ Support soft reset function
- ÿ Supports SPI, 1-bit SD and 4-bit SD modes

### 5.3 High-speed SPI device controller

Compatible with the general SPI physical layer protocol, by agreeing on the data format for interaction with the host, the host can access the device at high speed, and the maximum supported operating frequency is 50Mbps.

- ÿ Compatible with universal SPI protocol
- ÿ Selectable level interrupt signal
- ÿ Supports up to 50Mbps rate
- ÿ Simple frame format, full hardware parsing and DMA

## 5.4 DMA controller

Supports up to 8 channels, 16 DMA request sources, and supports linked list structure and register control.

- ÿ Amba2.0 standard bus interface, 8 DMA channels
- ÿ Support DMA operation based on memory linked list structure
- ÿ Software configures 16 hardware request sources
- ÿ Support 1, 4-burst operation mode

ÿ Supports byte, half-word, word operations

ÿ The source and destination addresses remain unchanged or can be configured in sequential increments or operate cyclically within a predefined address range.

ÿ Synchronize DMA request and DMA response hardware interface timing

### 5.5 Clock and reset

Supports the control of chip clock and reset system. Clock control includes clock frequency conversion, clock shutdown and adaptive gate control; reset control includes system and

And soft reset control of sub-modules.

### 5.6 Memory Manager

Supports the configuration of the sending and receiving buffer size, as well as control information such as the base address of the MAC access buffer, the number of buffers, and the upper limit of frame aggregation.

### 5.7 Digital baseband

Supports IEEE802.11a/b/g/e/n (1T1R) transmitter and receiver algorithm implementation, main parameters:

ÿ Data rate: 1~54Mpbs (802.11a/b/g), 6.5~150Mbps (802.11n)

ÿ MCS format: MCS0~MCS7, MCS32 (40MHz HT Duplicate mode)

ÿ Support 40MHz bandwidth non-HT Duplicate mode, 6Mÿ54M

ÿ Signal bandwidth: 20MHz, 40MHz

ÿ Modulation method: DSSS (DBPSK, DQPSK, CCK) and OFDM (BPSK, QPSK, 16QAM, 64QAM)

ÿ Implement 1T1R MIMO-OFDM spatial multiplexing

ÿ Support Short GI mode

ÿ Supports legacy mode and Mixed mode

ÿ Supports transmission and reception of 20M upper and lower sideband signals under 40MHz bandwidth

ÿ Supports STBC reception of MCS0ÿ7, 32

ÿ Support Green Field mode

### 5.8 MAC Controller

Supports IEEE802.11a/b/g/e/n MAC sublayer protocol control. Specific specifications include:

- ÿ Support EDCA channel access method
- ÿ Support CSMA/CA, NAV and TXOP protection mechanisms
- ÿ Beacon, Mng, VO, VI, BE, BK five-way sending queue and QoS
- ÿ Support single and broadcast multicast frame reception and transmission
- ÿ Support RTS/CTS, CTS2SELF, Normal ACK, No ACK frame sequence
- ÿ Supports retransmission mechanism as well as retransmission rate and power control
- ÿ Supports MPDU hardware aggregation and deaggregation and Immediate BlockAck mode
- ÿ Support RIFS, SIFS, AIFS
- ÿ Support reverse transmission mechanism
- ÿ Supports TSF timing and is software configurable
- ÿ Support MIB statistics

### 5.9 Security system

Supports the security algorithm specified by the IEEE802.11a/b/g/e/n protocol, and cooperates to complete the encryption and decryption of sent and received data frames.

- ÿ Meet the encryption and decryption throughput rate greater than 150Mbps
- ÿ Amba2.0 standard bus interface
- ÿ Support WAPI security mode 2.0
- ÿSupports WEP security mode-64-bit encryption
- ÿSupports WEP security mode-128-bit encryption
- ÿ Support TKIP security mode
- ÿ Support CCMP security mode

### 5.10 FLASH controller

- ÿ Provide bus access to FLASH interface
- ÿ Support SPI, Quad SPI interface for external Flash
- ÿ External Flash supports up to 16MB
- ÿ Support hardware encryption module to encrypt Flash
- ÿ Provide system bus and data bus access arbitration
- ÿ Implement CACHE cache system to improve FLASH interface access speed
- ÿ Provide compatibility with different QFlash

### 5.11 RSA encryption module

RSA computing hardware coprocessor provides Montgomery (FIOS algorithm) modular multiplication computing function. Cooperate with the RSA software library to implement the RSA algorithm.

Supports 128-bit to 2048-bit modular multiplication.

#### 5.12 Universal hardware encryption module

The encryption module automatically completes the encryption of the source address space data of the specified length, and automatically writes the encrypted data back to the specified destination address space after completion;

Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG.

- ÿ Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG encryption algorithm
- ÿ DES/3DES supports ECB and CBC modes
- ÿ AES supports three modes: ECB, CBC and CTR
- ÿ CRC supports four modes: CRC8, CRC16_MODBUS, CRC16_CCITT and CRC32
- ÿ CRC supports input/output reverse
- ÿ SHA1/MD5/CRC supports continuous multi-packet encryption
- ÿ Built-in true random number generator, also supports seed to generate pseudo-random numbers

### 5.13 I2C controller

APB bus protocol standard interface, only supports main device controller, I²C working frequency supports configurable, 100K-400K.

### 5.14 Master/Slave SPI Controller

Supports synchronous SPI master-slave functionality. Its working clock is the system internal bus clock. Its characteristics are as follows:

- ÿ The transmit and receive paths each have 8 word depth FIFOs
- ÿ master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire timing
- ÿ slave supports 4 formats of Motorola SPI (CPOL, CPHA);
- ÿ Support full duplex and half duplex
- ÿ The main device supports bit transmission, with a maximum support of 65535bit transmission.
- ÿ The slave device supports transmission modes of various lengths of bytes
- ÿ The maximum clock frequency of SPI_Clk input from the slave device is 1/6 of the system clock

### 5.15 UART controller

- ÿ The device side complies with the APB bus interface protocol
- ÿ Support interrupt or polling working mode
- ÿ Supports DMA transfer mode, with 32-byte FIFO for sending and receiving.
- ÿ Programmable baud rate
- ÿ 5-8bit data length, and parity polarity configurable
- ÿ 1 or 2 stop bits configurable
- ÿ Support RTS/CTS flow control
- ÿ Support Break frame sending and receiving
- ÿ Overrun, parity error, frame error, rx break frame interrupt indication

ÿ Maximum 16-burst byte DMA operation

## 5.16 GPIO controller

Configurable GPIO, software-controlled input and output, hardware-controlled input and output, configurable interrupt mode.

The starting addresses of the GPIOA and GPIOB registers are different, but their functions are the same.

## 5.17 Timer

Microsecond and millisecond timing (the number of counts is configured according to the clock frequency), and six configurable 32-bit counters are implemented. When the count configured by the corresponding calculator is completed,

When completed, a corresponding interrupt is generated.

## 5.18 Watchdog Controller

Supports "watchdog" function. Observe correct software behavior and allow global reset after system crash. "Watchdog" generates a periodic

Interrupt, the system software must respond to this interrupt and clear the interrupt flag; if the interrupt flag is not cleared for a long time due to system crash, then

Generates a hard reset to globally reset the system.

## 5.19 RF Configurator

Implemented synchronous SPI master functionality. Its working clock is the system internal bus clock. Its characteristics are as follows:

ÿ The transmit and receive paths each have 1 word depth FIFO

## 5.20 RF transceiver

ÿ The RF transceiver part includes modules including power amplifier, transmit channel, receive channel, phase locked loop and SPI. By adjusting the control

Control ports SHDN, RXEN and TXEN to change the chip working status

ÿ The receiving path adopts a zero-IF structure to directly convert the radio frequency signal into two baseband I and Q outputs. The RF front-end works at 2.4GHz,

Contains low-noise amplifier and quadrature mixer; baseband consists of low-pass filter and variable gain amplifier to achieve channel filtering and gain control;

The driver amplifier provides different DC outputs for the ADC interface

ÿ The transmit path includes: programmable control filter, upconversion mixer, variable gain amplifier and power amplifier. The transmit path also uses direct

Frequency conversion structure. The output signal of the DAC passes through a low-pass filter to filter out the image frequency and out-of-band noise. The PA output is a differential output driver

Off-chip antenna

## 5.21 PWM controller

ÿ 5-channel PWM signal generation function

ÿ 2-channel input signal capture function (PWM0 and PWM4 two channels)

ÿ Output signal frequency range 3Hz~160KHz

ÿ Maximum accuracy of duty cycle: 1/256

ÿ Counter width inserted into dead zone: 8bit

## 5.22 I²S controller

ÿ Support AMBA APB bus interface, 32bit single read and write operations

ÿ Supports master and slave modes and can work in duplex

ÿ Supports 8/16/24/32 bit width, the maximum sampling frequency is 128KHz

ÿ Supports mono and stereo modes

ÿ Compatible with I²S and MSB justified data formats, compatible with PCM A/B format

ÿ Supports DMA request read and write operations. Only supports word-by-word operations

## 5.23 7816/UART controller

ÿ Compatible with UART and 7816 interface functions

ÿ The device side complies with the APB bus interface protocol

ÿ Support interrupt or polling working mode

ÿ Supports DMA transfer mode, with 32-byte FIFO for sending and receiving.

ÿ DMA can only operate on a byte basis, with a maximum of 16-burst byte DMA operations

Serial port function:

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity configurable

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt indication

7816 interface functions:

ÿ Compatible with ISO-7816-3 T=0.T=1 mode

ÿ Compatible with EVM2000 protocol

ÿ Configurable guard time (11 ETU-267 ETU)

ÿ Forward/reverse convention can be configured by software

ÿ Support send/receive parity check and retransmission function

ÿ Supports 0.5 and 1.5 stop bit configurations

## 5.24 PSRAM interface controller

The PSRAM controller with built-in SPI/QSPI interface supports external PSRAM device access and provides bus-based PSRAM read, write and erase operations.

The maximum read and write speed is 80MHz.

ÿ Supports read and write access to external PSRAM

ÿ Configurable for SPI and QSPI

ÿ SPI/QSPI clock frequency configurable

ÿ Support BURST INC mode access

ÿ Supports semi-sleep mode of PSRAM

## 5.25 ADC

The acquisition module based on Sigma-Delta ADC completes the acquisition of up to 4 analog signals. The sampling rate is controlled by the external input clock.

It collects input voltage and can also collect chip temperature, supporting input calibration and temperature compensation calibration.

## 5.26 Touch Sensor touch button controller

The basic functions of the module are as follows:

ÿ Supports up to 13 channels of Touch Sensor scanning

ÿ Record the scanning results of each Touch Sensor

ÿ Report scan results through interruption

## 6 pin definition

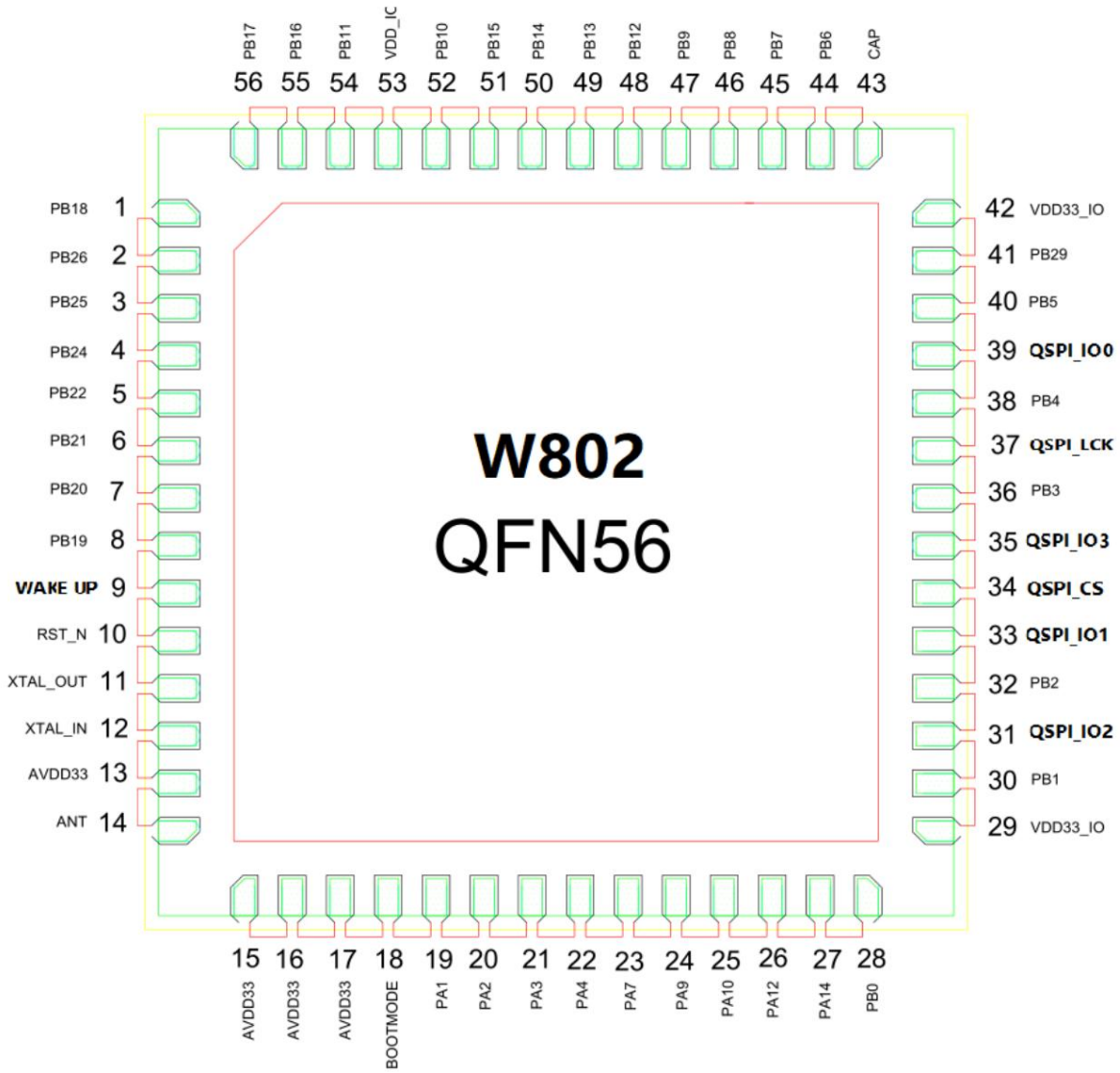



Figure 6-1 W802 pin layout diagram (QFN56)

Table 6-1W802 pin assignment definition (QFN56)

| No. | Name | Type | Pin function after reset | Reuse function | Maximum frequency | pull-down capability | driving capability |
|---|---|---|---|---|---|---|---|
| 1 | PB_18 | I/O | GPIO, input, high impedance | UART5_TX | 20MHz | UP/DOWN | 12mA |
| 2 | PB_26 | I/O | GPIO, input, high impedance | LSPI_MOSI/PWM4 | 20MHz | UP/DOWN | 12mA |
| 3 | PB_25 | I/O | GPIO, input, high impedance | LSPI_MISO/PWM3 | 20MHz | UP/DOWN | 12mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | PB_24 | I/O GPIO, input, high impedance | LSPI_CK/PWM2 | 20MHz | UP/DOWN | 12mA |
| 5 | PB_22 | I/O GPIO, input, high impedance | UART0_CTS/PCM_CK | 2MHz | UP/DOWN | 12mA |
| 6 | PB_21 | I/O GPIO, input, high impedance | UART0_RTS/PCM_SYNC | 2MHz | UP/DOWN | 12mA |
| 7 | PB_20 | I/O UART_RX | UART0_RX/PWM1/UART1_CTS/I2C_SCL | 2MHz | UP/DOWN | 12mA |
| 8 | PB_19 | I/O UART_TX | UART0_TX/PWM0/UART1_RTS/I2C_SDA | 2MHz | UP/DOWN | 12mA |
| 9 | WAKEUP | I external wake-up | | | | |
| 10 | RESET | I RESET reset | | | UP | |
| 11 XTAL_OUT O External crystal oscillator output | | | | | | |
| 12 XTAL_IN I External crystal oscillator input | | | | | | |
| 13AVDD33 | | P chip power supply, 3.3V | | | | |
| 4 | ANT | I/O RF antenna | | | | |
| 15AVDD33 | | P chip power supply, 3.3V | | | | |
| 16AVDD33 | | P chip power supply, 3.3V | | | | |
| 17 | AVDD33_AUX | P chip power supply, 3.3V | | | | |
| 18 BOOTMODE I/O BOOTMODE | | | I2S_MCLK/LSPI_CS/PWM2/I2S_DO | 30MHz | UP/DOWN | 12mA |
| 19 | PA_1 | I/O JTAG_CK | JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/ADC_0 | 20MHz | UP/DOWN | 12mA |
| 20 | PA_2 | I/O GPIO, input, high impedance | UART1_RTS/UART2_TX/PWM0/UART3_RTS/ADC_3 | 20MHz | UP/DOWN | 12mA |
| twenty one | PA_3 | I/O GPIO, input, high impedance | UART1_CTS/UART2_RX/PWM1/UART3_CTS/ADC_2 | 20MHz | UP/DOWN | 12mA |
| twenty two | PA_4 | I/O JTAG_SWO | JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/ADC_1 | 20MHz | UP/DOWN | 12mA |
| twenty three | PA_7 | I/O GPIO, input, high impedance | PWM4/LSPI_MOSI/I2S_MCK/I2S_DI | 25MHz | UP/DOWN | 12mA |
| twenty four | PA_9 | I/O GPIO, input, high impedance | MMC_CLK/UART4_RX/UART5_RX/I2S_LRCLK/Touch_1 | 50MHz | UP/DOWN | 12mA |
| 25 | PA_10 | I/O GPIO, input, high impedance | MMC_CMD/UART4_RTX/PWM0/I2S_DO/Touch_2 | 50MHz | UP/DOWN | 12mA |
| 26 | PA_12 | I/O GPIO, input, high impedance | MMC_DAT1/UART5_TX/PWM2 /Touch_Cap (CMOD) | 50MHz | UP/DOWN | 12mA |
| 27 | PA_14 | I/O GPIO, input, high impedance | MMC_DAT3/UART5_CTS/PWM4/Touch_Cap(CDC) | 50MHz | UP/DOWN | 12mA |
| 28 | PB_0 | I/O GPIO, input, high impedance | PWM0/LSPI_MISO/UART3_TX/PSRAM_CK /Touch_3 | 80MHz | UP/DOWN | 12mA |
| 29VDD33IO | | P IO power supply, 3.3V | | | | |
| 30 | PB_1 | I/O GPIO, input, high impedance | PWM1/LSPI_CK/UART3_RX/PSRAM_CS /Touch_4 | 80MHz | UP/DOWN | 12mA |
| 31 QSPI_IO2 I/O | | | QSPI_D2 | QSPI_D2 | 100MHz | UP/DOWN | 12mA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 32 | PB_2 | I/O GPIO, input, high impedance | | PWM2/LSPI_CK/UART2_TX/PSRAM_D0 /Touch_5 | 80MHz | UP | |
| 33 | QSPI_IO1 | I/O QSPI_D1 | | QSPI_D1 | 100MHz | UP/DOWN | 12mA |
| 34 | QSPI_CS | O | QSPI_CS | QSPI_CS | 100MHz | UP | |
| 35 | QSPI_IO3 | I/O QSPI_D3 | | QSPI_D3 | 100MHz | UP | |
| 36 | PB_3 | I/O GPIO, input, high impedance | | PWM3/LSPI_MISO/UART2_RX/PSRAM_D1 /Touch_6 | 80MHz | UP | |
| 37 | QSPI_CLK | O QSPI_CLK | | QSPI_CLK | 100MHz | UP/DOWN | 12mA |
| 38 | PB_4 | I/O GPIO, input, high impedance | | LSPI_CS/UART2_RTS/UART4_TX/PSRAM _D2 /Touch_7 | 80MHz | UP | |
| 39 | QSPI_IO0 | | QSPI_D0 | QSPI_D0 | 100MHz | UP/DOWN | 12mA |
| 40 | PB_5 | I/O GPIO, input, high impedance | | LSPI_MOSI/UART2_CTS/UART4_RX/PSA RM_D3 /Touch_8 | 80MHz | UP | |
| 41 | PB_29 | I/O GPIO, input, high impedance | | PSRAM_D1/UART0_RTS/Touch_15 | 80MHz | UP/DOWN | 12mA |
| 42 | VDD33IO | P | IO power supply, 3.3V | | | | |
| 43 | CAP | I | external capacitor, 4.7μF | | | - | |
| 44 | PB_6 | I/O GPIO, input, high impedance | | UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK /Touch_9 | 50MHz | UP/DOWN | 12mA |
| 45 | PB_7 | I/O GPIO, input, high impedance | | UART1_RX/MMC_CMD/HSPI_INT/SDIO_C MD /Touch_10 | 50MHz | UP/DOWN | 12mA |
| 46 | PB_8 | I/O GPIO, input, high impedance | | I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0 /Touch_11 | 50MHz | UP/DOWN | 12mA |
| 47 | PB_9 | I/O GPIO, input, high impedance | | I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1 /Touch_12 | 50MHz | UP/DOWN | 12mA |
| 48 | PB_12 | I/O GPIO, input, high impedance | | HSPI_CK/PWM0/UART5_CTS/I2S_BCLK | 50MHz | UP/DOWN | 12mA |
| 49 | PB_13 | I/O GPIO, input, high impedance | | HSPI_INT/PWM1/UART5_RTS/I2S_LRCL K | 50MHz | UP/DOWN | 12mA |
| 50 | PB_14 | I/O GPIO, input, high impedance | | HSPI_CS/PWM2/LSPI_CS/I2S_DO | 50MHz | UP/DOWN | 12mA |
| 51 | PB_15 | I/O GPIO, input, high impedance | | HSPI_DI/PWM3/LSPI_CK/I2S_DI | 50MHz | UP/DOWN | 12mA |
| 52 | PB_10 | I/O GPIO, input, high impedance | | I2S_DI/MMC_D2/HSPI_DI/SDIO_D2 | 50MHz | UP/DOWN | 12mA |
| 53 | VDD33IO | P | IO power supply, 3.3V | | | | |
| 54 | PB_11 | I/O GPIO, input, high impedance | | I2S_DO/MMC_D3/HSPI_DO/SDIO_D3 | 50MHz | UP/DOWN | 12mA |
| 55 | PB_16 | I/O GPIO, input, high impedance | | HSPI_DO/PWM4/LSPI_MISO/UART1_RX | 50MHz | UP/DOWN | 12mA |
| 56 | PB_17 | I/O GPIO, input, high impedance | | UART5_RX/PWM_BREAK/LSPI_MOSI/I2S _MCLK | 20MHz | UP/DOWN | 12mA |

Note: 1. I = input, O = output, P = power

## 7 Electrical Characteristics

### 7.1 Limit parameters

Table 7-1 Limit parameters

| parameter | name | minimum value | Typical value | maximum value | unit |
|---|---|---|---|---|---|
| Supply voltage | VDD | 3.0 | 3.3 | 3.6 | V |
| Input logic level is low | VIL | -0.3 | | 0.8 | V |
| Input logic level is high | VIH | 2.0 | | VDD+0.3 | V |
| Input pin capacitance | Cpad | | | 2 | pF |
| Output logic level is low | VOL | | | 0.4 | V |
| Output logic level is high | VOH | 2.4 | | | V |
| Output maximum drive capability | IMAX | | | twenty four | mA |
| Storage temperature range | TSTR | -40ÿ | | +125ÿ | ÿ |
| range of working temperature | TOPR | -40ÿ | | +85ÿ | ÿ |

### 7.2 RF power consumption parameters

Test conditions: 3.3V power supply, emission test at 50% duty cycle.

Table 7-2 RF power consumption parameters

| model | Typical value | unit |
|---|---|---|
| Transmit IEEE802.11b 1Mbps<br>POUT = +19.4dBm | 240 | mA |
| Transmit IEEE802.11b 11Mbps<br>POUT = +19.3dBm | 240 | mA |
| Transmit IEEE802.11g 54Mbps<br>POUT = +14.7 dBm | 180 | mA |
| Send IEEE802.11n MCS7<br>POUT = +12dBm | 175 | mA |
| Receive IEEE802.11b/g/n | 95 | mA |

**7.3 Wi-Fi radio frequency**

Table 7-3 Wi-Fi radio frequency parameters

| parameter | Typical value | unit |
|---|---|---|
| input frequency | 2.4~2.4835 | GHz |
| Transmit power | | |
| IEEE802.11b 11Mbps | 19±2 | dBm |
| IEEE802.11g 54Mbps | 16±2 | dBm |
| IEEE802.11nMCS7HT20 | 13±2 | dBm |
| Receive sensitivity | | |

| | | |
|---|---|---|
| IEEE802.11b 1Mbps | -96 | dBm |
| IEEE802.11b 11Mbps | -86 | dBm |
| IEEE802.11g 54Mbps | -73 | dBm |
| IEEE802.11gMCS7HT20 | -71 | dBm |
| adjacent channel suppression | | |
| IEEE802.11b 6Mbps | 32 | dB |
| IEEE802.11g 54Mbps | 16 | dB |
| IEEE802.11n HT20, MCS0 | 31 | dB |
| IEEE802.11n HT20, MCS7 | 12 | dB |

### 7.4 Bluetooth RF

#### 7.4.1 Traditional Bluetooth RF

Receiver-Base Rate (BR)

| parameter | condition | Minimum value | Typical value | Maximum value | Unit |
|---|---|---|---|---|---|
| Sensitivity@0.1% BER | | | -91 | | dBm |
| Maximum received signal @0.1% BER | | | 0 | | dBm |
| Common channel suppression ratio C/I | | | 9 | | dB |
| out-of-band blocking | 30 MHz ~ 2000 MHz | | -10 | | dBm |
| | 2000 MHz ~ 2400 MHz | | -27 | | dBm |

| | | | | | |
|---|---|---|---|---|---|
| | 2500 MHz ~ 3000 MHz | | -27 | | dBm |
| | 3000 MHz ~ 12.5 GHz | | -10 | | dBm |
| Intermodulation | | | -39 | | dB |

Transmitter - Base Rate (BR)

| parameter | condition | Minimum value | Typical value | Maximum value | Unit |
|---|---|---|---|---|---|
| RF transmit power | | | 6 | | dBm |
| Gain control step size | | | 3 | | db |
| RF power control range | | -10 | | 12 | dBm |
| 20 dB bandwidth | | 0.918 | 0.923 | | |
| ÿf1avg | | | 159.8 | | |
| ÿf2max | | | 142.8 | | |
| ÿ f2avg/ÿ f1avg | | | 0.89 | | |
| ICFT | | | 0 | | |
| drift rate | | -2.25 | -2.08 | 2.23 | kHz |
| Offset(DH1) | | -4 | | -1 | kHz |
| Offset(DH5) | | | 0 | twenty one | kHz |

Receiver - Enhanced Rate (EDR)

| parameter | condition | Minimum value | Typical value | Maximum value | Unit |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| ÿ/4 DQPSK | | | | | |
| Sensitivity@0.01% BER | | | -88 | | dBm |
| Maximum received signal@0.01% BER | | | 0 | | dBm |
| 8DPSK | | | | | |
| Sensitivity@0.01% BER | | | -81 | | dBm |
| Maximum received signal@0.01% BER | | | 0 | | dBm |

Transmitter - Enhanced Data Rate (EDR)

| parameter | condition | Minimum value | Typical value | Maximum value | Unit |
|---|---|---|---|---|---|
| RF transmit power | | | 0 | | dBm |
| Gain control step size | | | 3 | | db |
| RF power control range | | -10 | | 8 | dBm |
| ÿ/4 DQPSK max w0 | | -3.2 | | 2.6 | KHz |
| ÿ/4DQPSKmaxwi | | -5.3 | | -2.4 KHz | |
| ÿ/4 DQPSK max \|wi + w0\| | | -4.8 | | -3.9 KHz | |
| 8DPSK max w0 | | -1.4 | | 1.5 | KHz |
| 8DPSKmaxwi | | -4.1 | | -2.9 KHz | |
| 8DPSK max \|wi + w0\| | | -4.8 | | -4.1 | KHz |

| | | | | | |
|---|---|---|---|---|---|
| ÿ/4 DQPSK modulation accuracy | RMS DEVM | | 6.7 | | % |
| | 99%DEVM | | 100 | | % |
| | Peak DEVM | | 14.1 | | % |
| 8 DPSK modulation accuracy | RMS DEVM | | 6.8 | | % |
| | 99%DEVM | | 99.99 | | % |
| | Peak DEVM | | 15.3 | | % |
| EDR differential phase encoding | | | 100 | | % |

### 7.4.2 Bluetooth Low Energy RF

receiver

| parameter | condition | Minimum value | Typical value | Maximum value | Unit |
|---|---|---|---|---|---|
| Sensitivity@30.8% PER | | | -94 | | dBm |
| Maximum received signal@30.8% PER | | | | 0 | dBm |
| out-of-band blocking | 30MHz~2000MHz | | -30 | | dBm |
| | 2003MHz~2399MHz | | -35 | | dBm |
| | 2484MHz~3000MHz | | -35 | | dBm |
| | 3000MHz~12.5GHz | | -30 | | dBm |

| | | | | | |
|---|---|---|---|---|---|
| Intermodulation | | | -47 | | dBm |

launcher

| parameter | condition | Minimum value | Typical value | Maximum value | Unit |
|---|---|---|---|---|---|
| RF transmit power | | | 6 | | dBm |
| Gain control step size | | | 2 | | db |
| RF power control range | | -10 | | 12 | dBm |
| ÿf1avg | | 240.8 | 241.2 242 | | kHz |
| ÿf2max | | 175.7 | 182.7 183.9 kHz | | |
| drift rate | | | 1.5 | | kHz |
| offset | | | -4.3 | | kHz |

**8 Packaging information**

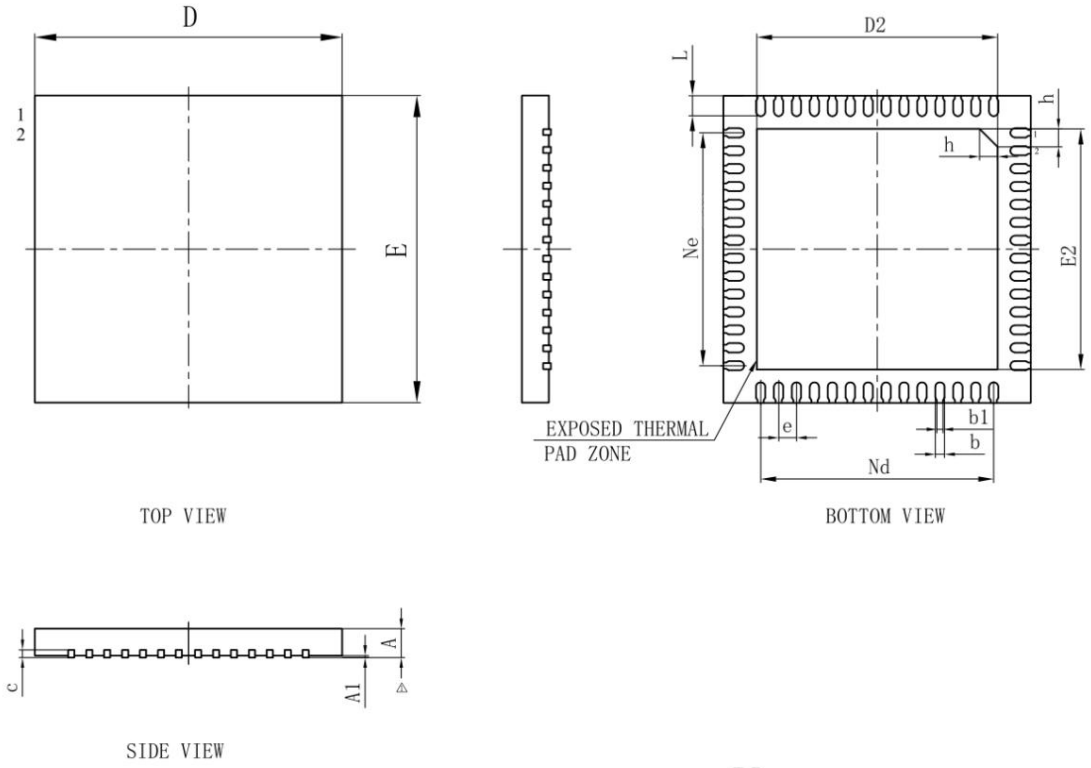


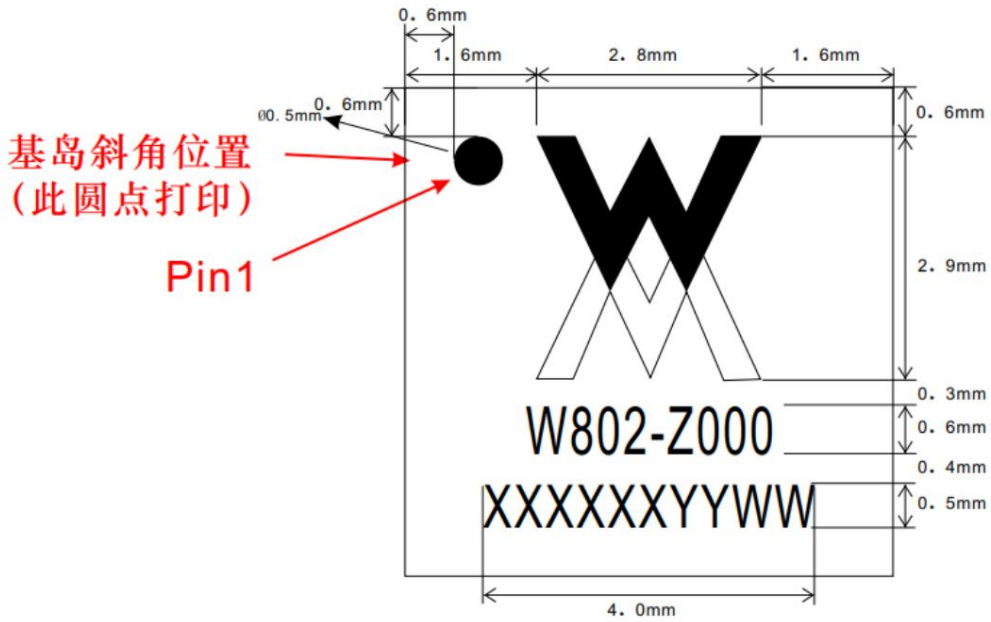

Figure 8-1 W802 packaging parameters

Table 8-1 W802 package parameter table

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.13 | 0.18 | 0.23 |
| b1 | 0.12REF | | |
| c | 0.18 | 0.20 | 0.25 |
| D | 5.90 | 6.00 | 6.10 |

| | | | |
|---|---|---|---|
| D2 | 4.60 | 4.70 | 4.80 |
| e | 0.35BSC | | |
| Ne | 4.55BSC | | |
| Nd | 4.55BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 4.60 | 4.70 | 4.70 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |
| L/F carrier size | 193x193 | | |

**9 silk screen information**




Note: Font: Arial;

The third line of the seal, XXXXXX, represents the first 6 digits of the batch number of the main core, and YYWW is the year and week number (if the year and week number is given in the order, the one given shall prevail, if not given,

Print the actual offline year and week number).