W806 MCU chip specification sheet

V3.0

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1 Overview

The W806 chip is a security MCU chip. The chip integrates a 32-bit CPU processor with built-in UART, GPIO, SPI, SDIO, I2C , I2S , PSRAM, 7816, ADC, LCD, TouchSensor and other digital interfaces; supports TEE security engine and supports multiple hardware encryption and decryption algorithms method, built-in DSP, floating point operation unit and security engine, supports code security permission settings, built-in 1MB Flash memory, supports firmware addition Numerous security measures such as password storage, firmware signature, secure debugging, and secure upgrades are implemented to ensure product security features. Suitable for small household appliances, toys, industry Control, medical monitoring and other fields.

2 features

ÿ Chip appearance

- ÿ QFN56 package, 6mm x 6mm

ÿMCU Features

- ÿ Integrated 32-bit XT804 processor, operating frequency 240MHz, built-in DSP, floating point operation unit and security engine
- ÿ Built-in 1MB Flash, 288KB RAM
- ÿ Integrated PSRAM interface, supports up to 64MB external PSRAM memory
- ÿ Integrated 6-way UART high-speed interface
- ÿ Integrated 4-channel 12-bit ADC, maximum sampling rate 1KHz
- ÿ Integrated 1 high-speed SPI interface (slave interface), supporting up to 50MHz
- ÿ Integrate a master/slave SPI interface
- ÿ Integrated 1 SDIO_HOST interface, supports SDIO2.0, SDHC, MMC4.2
- ÿ Integrate 1 SDIO_DEVICE, support SDIO2.0, maximum throughput 200Mbps
- ÿ Integrated 1 I 2C controller

ÿ Integrated GPIO controller, supports up to 44 GPIOs

ÿ Integrated 5-way PWM interface

ÿ Integrated 1-way Duplex I 2S controller

ÿ Integrated LCD controller, supports 4x32 interface

ÿ Integrated 1 7816 interface

ÿ Integrated 15 Touch Sensors

ÿ Security Features

ÿ The MCU has a built-in Tee security engine, and the code can distinguish between the secure world and the non-secure world.

ÿ Integrated SASC/TIPC, memory and internal modules/interfaces can be configured with security attributes to prevent non-security code access

ÿ Enable firmware signature mechanism to achieve safe boot/upgrade

ÿ Equipped with firmware encryption function to enhance code security

ÿ Firmware encryption keys are distributed using asymmetric algorithms to enhance key security

ÿ Hardware encryption module: RC4, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number generator

ÿ Low power consumption mode

ÿ 3.3V single power supply

ÿ Supports work, sleep, standby, and shutdown working modes

ÿ Standby power consumption is less than 10uA

3 chip structure

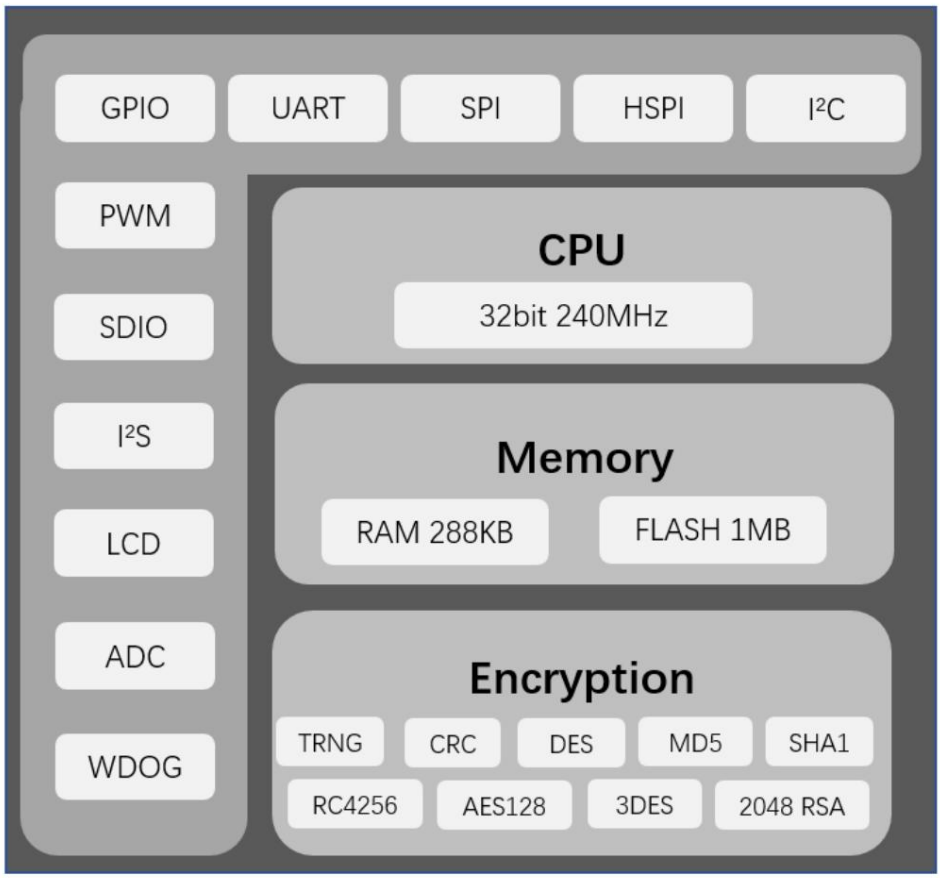

Figure 3-1 W806 chip block diagram

4 Function description

4.1 SDIO HOST controller

The SDIO HOST device controller provides a digital interface to access Secure Digital Input and Output Cards (SDIO) and MMC cards. were able

Access SDIO devices and SD card devices that are compatible with the SDIO 2.0 protocol. The main interfaces are CK, CMD and 4 data lines.

ÿ Compatible with SD card specification 1.0/1.1/2.0 (SDHC)

ÿ Compatible with SDIO memory card specification 1.1.0

ÿ Compatible with MMC specification 2.0~4.2

ÿ Configurable interface clock rate, supports host rate 0~50MHz

ÿ Support standard MMC interface

ÿ Supports Blocks up to 1024 bytes

ÿ Support soft reset function

ÿ Automatic Command/Response CRC generation/verification

ÿ Automatic data CRC generation/verification

ÿ Configurable timeout detection

ÿ Supports SPI, 1-bit SD and 4-bit SD modes

ÿ Support DMA data transfer

4.2 SDIO Device Controller

SDIO2.0 device-side interface completes the interaction with host data. Internally integrated 1024Byte asynchronous FIFO to complete the data between the host and the chip Interaction.

ÿ Compatible with SDIO card specification 2.0

ÿ Support host speed 0~50MHz

ÿ Supports Blocks up to 1024 bytes

ÿ Support soft reset function

ÿ Supports SPI, 1-bit SD and 4-bit SD modes

4.3 High-speed SPI device controller

Compatible with the general SPI physical layer protocol, by agreeing on the data format for interaction with the host, the host can access the device at high speed, and the maximum supported operating frequency is 50Mbps.

ÿ Compatible with universal SPI protocol

ÿ Selectable level interrupt signal

ÿ Supports up to 50Mbps rate

ÿ Simple frame format, full hardware parsing and DMA

4.4 DMA controller

Supports up to 8 channels, 16 DMA request sources, and supports linked list structure and register control.

ÿ Amba2.0 standard bus interface, 8 DMA channels

ÿ Support DMA operation based on memory linked list structure

ÿ Software configures 16 hardware request sources

ÿ Support 1, 4-burst operation mode

ÿ Supports byte, half-word, word operations

ÿ The source and destination addresses remain unchanged or can be configured in sequential increments or operate cyclically within a predefined address range.

ÿ Synchronize DMA request and DMA response hardware interface timing

4.5 Clock and reset

Supports the control of chip clock and reset system. Clock control includes clock frequency conversion, clock shutdown and adaptive gate control; reset control includes system and

And soft reset control of sub-modules.

4.6 Memory Manager

Supports the configuration of the sending and receiving buffer size, as well as control information such as the base address of the MAC access buffer, the number of buffers, and the upper limit of frame aggregation.

4.7 FLASH controller

ÿ Provide bus access to FLASH interface

ÿ Provide system bus and data bus access arbitration

ÿ Implement CACHE cache system to improve FLASH interface access speed

ÿ Provide compatibility with different QFlash

4.8 RSA encryption module

RSA computing hardware coprocessor provides Montgomery (FIOS algorithm) modular multiplication computing function. Cooperate with the RSA software library to implement the RSA algorithm.

Supports 128-bit to 2048-bit modular multiplication.

4.9 Universal hardware encryption module

The encryption module automatically completes the encryption of the source address space data of the specified length, and automatically writes the encrypted data back to the specified destination address space after completion;

Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG.

- ÿ Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG encryption algorithm
- ÿ DES/3DES supports ECB and CBC modes
- ÿ AES supports three modes: ECB, CBC and CTR
- ÿ CRC supports four modes: CRC8, CRC16_MODBUS, CRC16_CCITT and CRC32
- ÿ CRC supports input/output reverse
- ÿ SHA1/MD5/CRC supports continuous multi-packet encryption
- ÿ Built-in true random number generator, also supports seed to generate pseudo-random numbers

4.10 I2C controller

APB bus protocol standard interface, only supports main device controller, I²C working frequency supports configurable, 100K-400K.

4.11 Master/Slave SPI Controller

Supports synchronous SPI master-slave functionality. Its working clock is the system internal bus clock. Its characteristics are as follows:

- ÿ The transmit and receive paths each have 8 word depth FIFOs
- ÿ master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire timing
- ÿ slave supports 4 formats of Motorola SPI (CPOL, CPHA);

ÿ Support full duplex and half duplex

ÿ The main device supports bit transmission, with a maximum support of 65535bit transmission.

ÿ The slave device supports transmission modes of various lengths of bytes

ÿ The maximum clock frequency of SPI_Clk input from the slave device is 1/6 of the system clock

4.12 UART controller

ÿ The device side complies with the APB bus interface protocol

ÿ Support interrupt or polling working mode

ÿ Supports DMA transfer mode, with 32-byte FIFO for sending and receiving.

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity configurable

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt indication

ÿ Maximum 16-burst byte DMA operation

4.13 GPIO controller

Configurable GPIO, software-controlled input and output, hardware-controlled input and output, configurable interrupt mode.

The starting addresses of the GPIOA and GPIOB registers are different, but their functions are the same.

4.14 Timer

Microsecond and millisecond timing (the number of counts is configured according to the clock frequency), and six configurable 32-bit counters are implemented. When the count configured by the corresponding calculator is completed,

When completed, a corresponding interrupt is generated.

4.15 Watchdog Controller

Supports "watchdog" function. Observe the correctness of software behavior and allow a global reset after a system crash. "Watchdog" generates a periodic

Interrupt, the system software must respond to this interrupt and clear the interrupt flag; if the interrupt flag is not cleared for a long time due to system crash, then

Generates a hard reset to globally reset the system.

4.16 PWM controller

ÿ 5-channel PWM signal generation function

ÿ 2-channel input signal capture function (PWM0 and PWM4 two channels)

ÿ Frequency range: 3Hz~160KHz

ÿ Maximum accuracy of duty cycle: 1/256, counter width inserted into dead zone: 8bit

4.17 I²S controller

ÿ Support AMBA APB bus interface, 32bit single read and write operations

ÿ Supports master and slave modes and can work in duplex

ÿ Supports 8/16/24/32 bit width, the maximum sampling frequency is 128KHz

ÿ Supports mono and stereo modes

ÿ Compatible with I²S and MSB justified data formats, compatible with PCM A/B format

ÿ Supports DMA request read and write operations. Only supports word-by-word operations

4.18 7816/UART controller

ÿ The device side complies with the APB bus interface protocol

ÿ Support interrupt or polling working mode

ÿ Supports DMA transfer mode, with 32-byte FIFO for sending and receiving.

ÿ DMA can only operate on a byte basis, with a maximum of 16-burst byte DMA operations

Compatible with UART and 7816 interface functions:

Serial port function:

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity configurable

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt indication

7816 interface functions:

ÿ Compatible with ISO-7816-3 T=0.T=1 mode

ÿ Compatible with EVM2000 protocol

ÿ Configurable guard time (11 ETU-267 ETU)

ÿ Forward/reverse convention can be configured by software

ÿ Support send/receive parity check and retransmission function

ÿ Supports 0.5 and 1.5 stop bit configurations

4.19 PSRAM interface controller

W806 has a built-in PSRAM controller with SPI/QSPI interface, supports external PSRAM device access, and provides bus-based PSRAM read, write and erase operate. The maximum read and write speed is 80MHz.

ÿ Supports read and write access to external PSRAM

ÿ Configurable for SPI and QSPI

ÿ SPI/QSPI clock frequency configurable

ÿ Support BURST INC mode access

ÿ Supports semi-sleep mode of PSRAM

4.20 ADC

The acquisition module based on Sigma-Delta ADC completes the acquisition of up to 4 analog signals. The sampling rate is controlled by the external input clock.

It collects input voltage and can also collect chip temperature, supporting input calibration and temperature compensation calibration.

4.21 Touch button controller

The basic functions of the module are as follows:

ÿ Supports up to 15 Touch Sensor scans

ÿ Record the scanning results of each Touch Sensor

ÿ Report scan results through interruption

5 pin definition

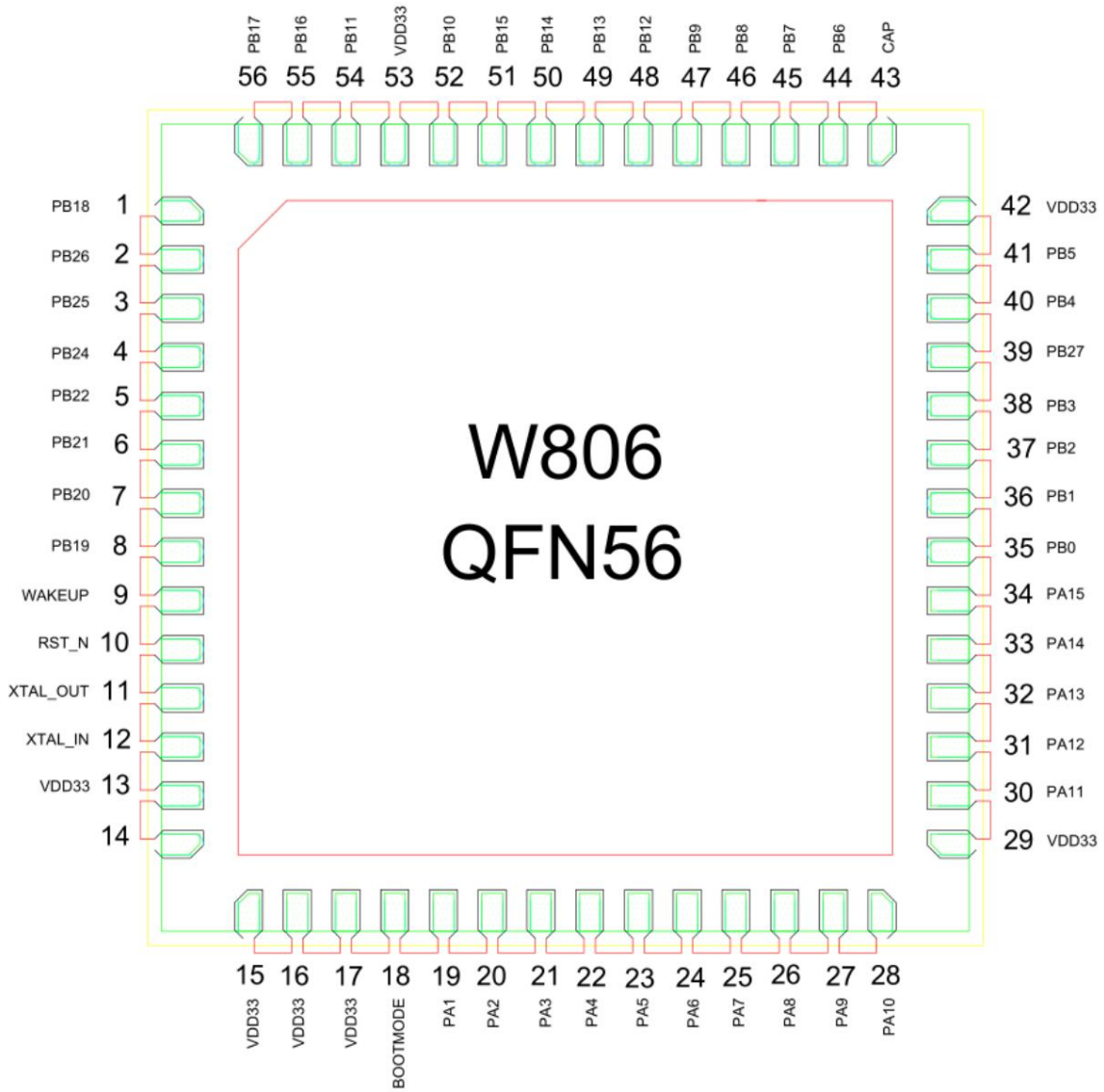

Figure 6-1 Pin layout (QFN56)

Table 6-1 Pin assignment definition (QFN56)

No.	Name	Type	Pin function after reset	Reuse function	Pull up and down ability
1	PB_18	I/O	GPIO, input, high impedance	UART5_TX/LCD_SEG30	UP/DOWN
2	PB_26	I/O	GPIO, input, high impedance	LSPI_MOSI/PWM4/LCD_SEG1	UP/DOWN
3	PB_25	I/O	GPIO, input, high impedance	LSPI_MISO/PWM3/LCD_COM0	UP/DOWN
4	PB_24	I/O	GPIO, input, high impedance	LSPI_CK/PWM2/LCD_SEG2	UP/DOWN
5	PB_22	I/O	GPIO, input, high impedance	UART0_CTS/PCM_CK/LCD_COM2	UP/DOWN
6	PB_21	I/O	GPIO, input, high impedance	UART0_RTS/PCM_SYNC/LCD_COM1	UP/DOWN
7	PB_20	I/O	UART_RX	UART0_RX/PWM1/UART1_CTS/I2C_SCL	UP/DOWN
8	PB_19	I/O	UART_TX	UART0_TX/PWM0/UART1_RTS/I2C_SDA	UP/DOWN
9	WAKEUP	I	WAKEUP wake-up function		DOWN
10	RESET	I	RESET reset		UP
11	XTAL_OUT	O	External crystal oscillator output		
12	XTAL_IN	I	External crystal oscillator input		
13	VDD33	P	chip power supply, 3.3V		
14	NC				
15	VDD33	P	chip power supply, 3.3V		
16	VDD33	P	chip power supply, 3.3V		
17	VDD33	P	chip power supply, 3.3V		
18	BOOTMODE	I/O	BOOTMODE	I2S_MCLK/LSPI_CS/PWM2/I2S_DO	UP/DOWN
19	PA_1	I/O	JTAG_CK	JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/ADC_1	UP/DOWN
20	PA_2	I/O	GPIO, input, high impedance	UART1_RTS/UART2_TX/PWM0/UART3_RTS/ADC_4	UP/DOWN
twenty one	PA_3	I/O	GPIO, input, high impedance	UART1_CTS/UART2_RX/PWM1/UART3_CTS/ADC_3	UP/DOWN
twenty two	PA_4	I/O	JTAG_SWO	JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/ADC_2	UP/DOWN
twenty three	PA_5	I/O	GPIO, input, high impedance	UART3_TX/UART2_RTS/PWM_BREAK/UART4_RTS	UP/DOWN
twenty four	PA_6	I/O	GPIO, input, high impedance	UART3_RX/UART2_CTS/NULL/UART4_CTS/LCD_SEG31	UP/DOWN
25	PA_7	I/O	GPIO, input, high impedance	PWM4/LSPI_MOSI/I2S_MCK/I2S_DI/LCD_SEG3/Touch_1	UP/DOWN
26	PA_8	I/O	GPIO, input, high impedance	PWM_BREAK/UART4_TX/UART5_TX/I2S_BCLK/LCD_SEG4	UP/DOWN
27	PA_9	I/O	GPIO, input, high impedance	MMC_CLK/UART4_RX/UART5_RX/I2S_LRCLK/LCD_SEG5/TOUCH_2	UP/DOWN
28	PA_10	I/O	GPIO, input, high impedance	MMC_CMD/UART4_RTS/PWM0/I2S_DO/LCD_SEG6/TOUCH_3	UP/DOWN
29	VDD33	P	chip power supply, 3.3V		
30	PA_11	I/O	GPIO, input, high impedance	MMC_DAT0/UART4_CTS/PWM1/I2S_DI/LCD_SEG7	UP/DOWN
31	PA_12	I/O	GPIO, input, high impedance	MMC_DAT1/UART5_TX/PWM2/LCD_SEG8/TOUCH_14	UP/DOWN
32	PA_13	I/O	GPIO, input, high impedance	MMC_DAT2/UART5_RX/PWM3/LCD_SEG9	UP/DOWN

33	PA_14	I/O GPIO, input, high impedance MMC_DAT3/UART5_CTS/PWM4/LCD_SEG10/TOUCH_15	UP/DOWN
34	PA_15	I/O GPIO, input, high impedance PSRAM_CK/UART5_RTS/PWM_BREAK/LCD_SEG11	UP/DOWN
35	PB_0	I/O GPIO, input, high impedance PWM0/LSPI_MISO/UART3_TX/PSRAM_CK/LCD_SEG12/Touch_4	UP/DOWN
36	PB_1	I/O GPIO, input, high impedance PWM1/LSPI_CK/UART3_RX/PSRAM_CS/LCD_SEG13/Touch_5	UP/DOWN
37	PB_2	I/O GPIO, input, high impedance PWM2/LSPI_CK/UART2_TX/PSRAM_D0/LCD_SEG14/Touch_6	UP/DOWN
38	PB_3	I/O GPIO, input, high-impedance PWM3/LSPI_MISO/UART2_RX/PSRAM_D1/LCD_SEG15/Touch_7	UP/DOWN
39	PB_27	I/O GPIO, input, high impedance PSRAM_CS/UART0_TX/LCD_COM3	UP/DOWN
40	PB_4	I/O GPIO, input, high impedance LSPI_CS/UART2_RTS/UART4_TX/PSRAM_D2/LCD_SEG16/Touch_8	UP/DOWN
41	PB_5	I/O GPIO, input, high impedance LSPI_MOSI/UART2_CTS/UART4_RX/PSARM_D3/LCD_SEG17/Touch_9	UP/DOWN
42	VDD33	P chip power supply, 3.3V	
43	CAP	I external capacitor, 4.7μF	
44	PB_6	I/O GPIO, input, high-impedance UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK/LCD_SEG18/Touch_10	UP/DOWN
45	PB_7	I/O GPIO, input, high-impedance UART1_RX/MMC_CMD/HSPI_INT/SDIO_CMD/LCD_SEG19/Touch_11	UP/DOWN
46	PB_8	I/O GPIO, input, high impedance I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0/LCD_SEG20/Touch_12	UP/DOWN
47	PB_9	I/O GPIO, input, high impedance I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/LCD_SEG21/Touch_13	UP/DOWN
48	PB_12	I/O GPIO, input, high-impedance HSPI_CK/PWM0/UART5_CTS/I2S_BCLK/LCD_SEG24	UP/DOWN
49	PB_13	I/O GPIO, input, high impedance HSPI_INT/PWM1/UART5_RTS/I2S_LRCLK/LCD_SEG25	UP/DOWN
50	PB_14	I/O GPIO, input, high impedance HSPI_CS/PWM2/LSPI_CS/I2S_DO/LCD_SEG26	UP/DOWN
51	PB_15	I/O GPIO, input, high impedance HSPI_DI/PWM3/LSPI_CK/I2S_DI/LCD_SEG27	UP/DOWN
52	PB_10	I/O GPIO, input, high impedance I2S_DI/MMC_D2/HSPI_DI/SDIO_D2/LCD_SEG22	UP/DOWN
53	VDD33	P chip power supply, 3.3V	
54	PB_11	I/O GPIO, input, high impedance I2S_DO/MMC_D3/HSPI_DO/SDIO_D3/LCD_SEG23	UP/DOWN
55	PB_16	I/O GPIO, input, high impedance HSPI_DO/PWM4/LSPI_MISO/UART1_RX/LCD_SEG28	UP/DOWN
56	PB_17	I/O GPIO, input, high-impedance UART5_RX/PWM_BREAK/LSPI_MOSI/I2S_MCLK/LCD_SEG29	UP/DOWN

Note: 1. I = input, O = output, P = power

6 Electrical Characteristics

6.1 Limit parameters

Table 7-1 Limit parameters

parameter	name	minimum value	Typical value	maximum value	unit
Supply voltage	VDD	3.0	3.3	3.6	V
Input logic level is low	VIL	-0.3		0.8	V
Input logic level is high	VIH	2.0		VDD+0.3	V
Input pin capacitance	Cpad			2	pF
Output logic level is low	VOL			0.4	V
Output logic level is high	VOH	2.4			V
Output maximum drive capacity	IMAX			twenty four	mA
Storage temperature range	TSTR	-40ÿ		+125ÿ	ÿ
range of working temperature	TOPR	-40ÿ		+85ÿ	ÿ

7 Packaging information

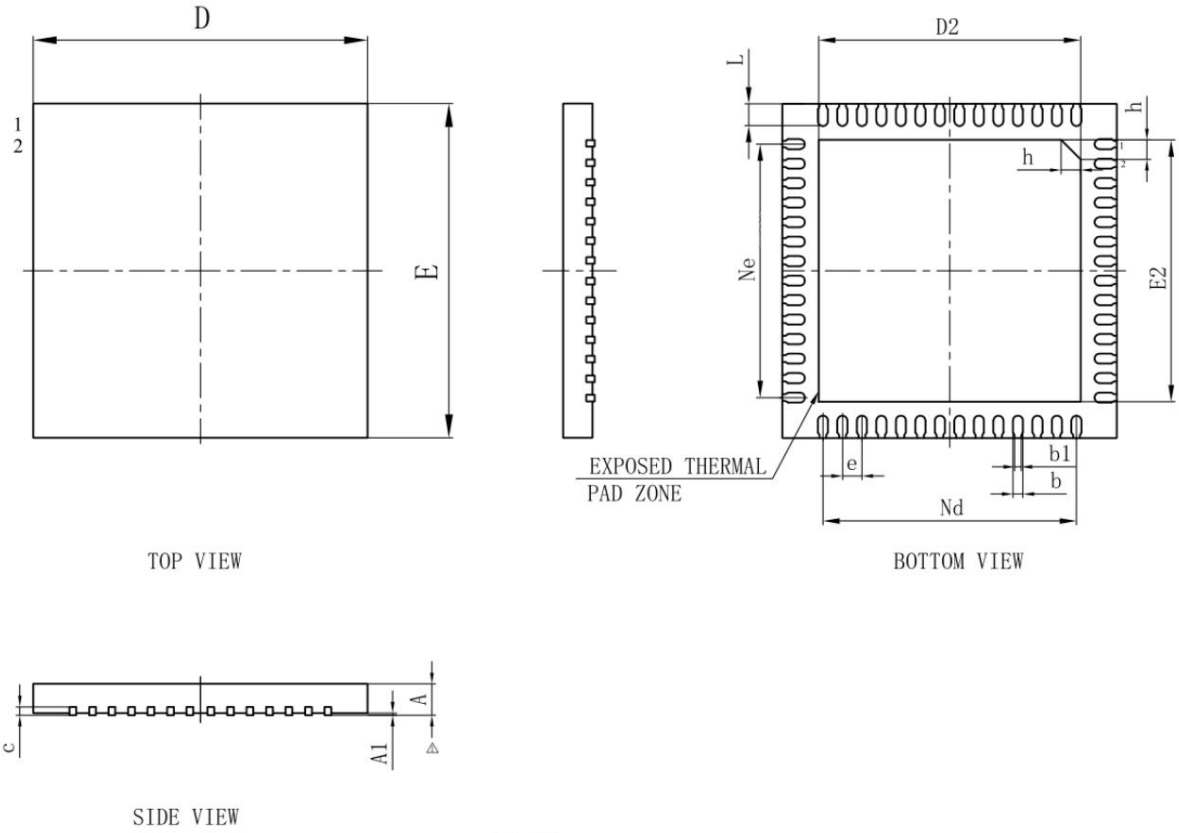

Figure 8-1 W806 packaging parameters

Table 8-1 W806 package parameter table

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		

c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.60	4.70	4.80
e	0.35BSC		
Ne	4.55BSC		
Nd	4.55BSC		
E	5.90	6.00	6.10
E2	4.60	4.70	4.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F carrier size	193x193		