

W861 chip specification

V2.0

Beijing Winner Microelectronics Co., Ltd. (Winner Micro)

Address: Floor 6, Yindu Building, No. 67 Fucheng Road, Haidian District, Beijing

Tel: +86-10-62161900

Website: www.winnermicro.com

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Winner Micro

1 Overview

The W861 chip is a secure IoT Wi-Fi/Bluetooth dual-mode SoC chip. The chip provides large-capacity RAM and Flash space, supports rich digital functional interface. Support 2.4G IEEE802.11b/g/n Wi-Fi communication protocol; support BLE4.2 protocol. Chip integrated 32-bit CPU

Processor, built-in UART, GPIO, SPI, I2C, I2S, 7816, SDIO, ADC, LCD, TouchSensor and other digital interfaces; built-in

2MFlash memory, 2MB memory; support TEE security engine, support multiple hardware encryption and decryption algorithms, built-in DSP, floating point unit

With the security engine, it supports code security permission setting, supports multiple security measures such as firmware encrypted storage, firmware signature, security debugging, security upgrade, etc.

Guaranteed product safety features. Suitable for a wide range of smart home appliances, smart homes, smart toys, wireless audio and video, industrial control, medical monitoring, etc.

IoT field.

2 features

• Chip Appearance

• QFN56 package, 6mm x 6mm

• MCU Features

• Integrated 32-bit XT804 processor, operating frequency 240MHz, built-in DSP, floating point unit and security engine

• Built-in 2MB Flash, 288KB RAM + 2MB PSRAM

• Integrated 6-way UART high-speed interface

• Integrated 4-channel 12-bit ADC, the highest sampling rate is 1KHz

• Integrates a high-speed SPI interface, supporting up to 50MHz

• Integrated 1 master/slave SPI interface

• Integrate 1 SDIO_HOST interface, support SDIO2.0, SDHC, MMC4.2

• Integrate 1 SDIO_DEVICE, support SDIO2.0, the highest throughput rate is 200Mbps

- Integrated 1 I 2C controller

- Integrated GPIO controller, supports up to 41 GPIOs

- Integrated 5-way PWM interface

- Integrated 1-way Duplex I 2S controller

- Integrated LCD controller, support 4x32 interface

- Integrate a 7816 interface

- Integrate 15 Touch Sensors

• Security Features

- MCU built-in Tee security engine, the code can distinguish safe world/non-safe world

- Integrated SASC/TIPC, memory and internal modules/interfaces can be configured with security attributes to prevent non-secure code access

- Enable firmware signature mechanism to achieve secure Boot/upgrade

- Equipped with firmware encryption function to enhance code security

- Firmware encryption keys are distributed using asymmetric algorithms to enhance key security

- Hardware encryption module: RC4, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number generator

• Wi-Fi Features

- Support GB15629.11-2006, IEEE802.11 b/g/n

- Support Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS

- Support EDCA channel access method

- Support 20/40M bandwidth working mode

- Support STBC, GreenField, Short-GI, support reverse transmission

- Support AMPDU, AMSDU

- Support IEEE802.11n MCS 0-7, MCS32 physical layer transmission rate stalls, the maximum transmission rate is 150Mbps

• Support Short Preamble when sending at 2/5.5/11Mbps

• Support HT-immediate Compressed Block Ack, Normal Ack, No Ack response mode

• Support CTS to self

• Support Station, Soft-AP, Soft-AP/Station functions

• Bluetooth Features

• Integrated Bluetooth baseband processor/protocol processor, supports BLE4.2 protocol

• Support Bluetooth Mesh

• Support Bluetooth network configuration

• Low Power Mode

• Single 3.3V power supply

• Support Wi-Fi power saving mode power management

• Support work, sleep, standby, shutdown working modes

3 chip structure

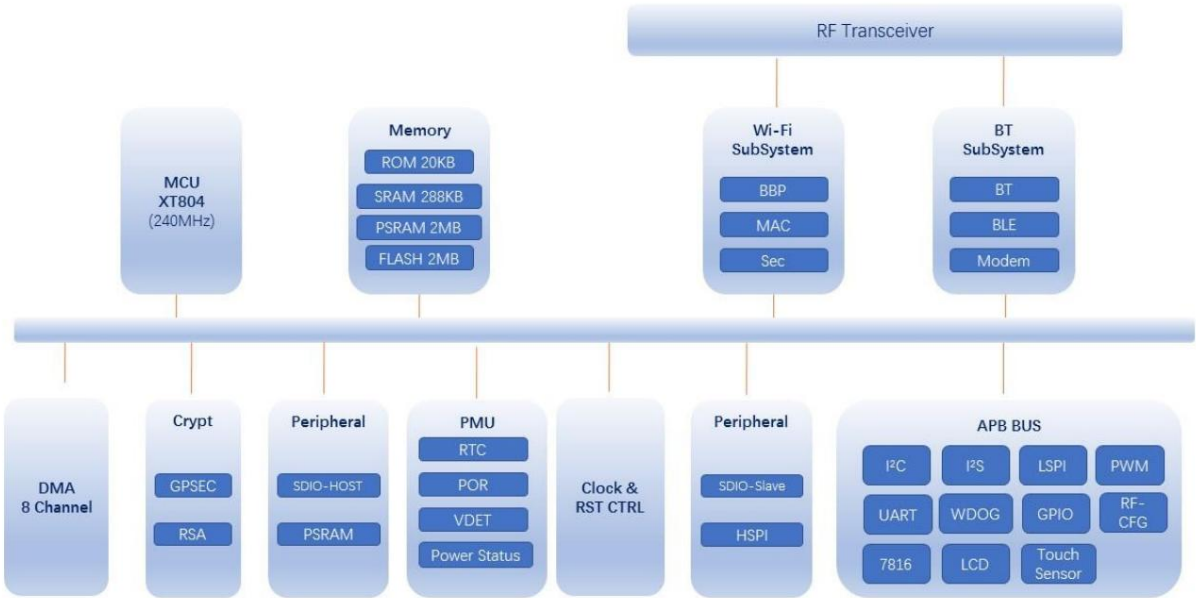


Figure 3-1 W861 chip structure diagram

4 Address space division

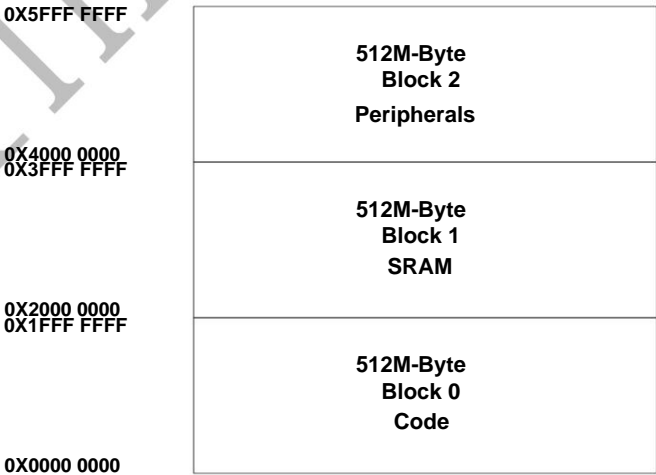


Figure 4-1 Address space mapping

Table 4-1 Detailed division of bus device address space

bus slave	BootMode=0	Address Space Subdivision	Remark
ROM	0x0000 0000 ~ 0x0004 FFFF		Store the solidified firmware code
FLASH	0x0800 0000 ~ 0x0FFF FFFF		as a dedicated instruction memory.
SRAM	0x2000 0000 ~ 0x2002 7FFF		Firmware memory and instruction store
Mac RAM	0x2002 8000 ~ 0x2004 7FFF		SDIO/H-SPI/UART data buffer
PSRAM	0x3000 0000 ~ 0x30800000		Memory
CONFIG	0x4000 0000 ~ 0x4000 2FFF	0x4000 0000 ~ 0x4000 05FF	RSA configuration space
		0x4000 0600 ~ 0x4000 07FF	GPSEC configuration space
		0x4000 0800 ~ 0x4000 09FF	DMA configuration space
		0x4000 0A00 ~ 0x4000 0CFF	SDIO_HOST configuration space
		0x4000 0D00 ~ 0x4000 0DFF	PMU configuration space
		0x4000 0E00 ~ 0x4000 0EFF	Clock and Reset configuration space
		0x4000 0F00 ~ 0x4000 0FFF	MacPHY Router configuration space
		0x4000 1000 ~ 0x4000 13FF	BBP configuration space

		0x4000 1400 ~ 0x4000 17FF MAC configuration space	
		0x4000 1800 ~ 0x4000 1FFF SEC configuration space	
		0x4000 2000 ~ 0x4000 21FF FLASH Controller configuration space	
		0x4000 2200 ~ 0x4000 23FF PSRAM_CTRL configuration space	
		0x4000 2400 ~ 0x4000 25FF SDIO Slave configuration space	
		0x4000 2600 ~ 0x4000 27FF H-SPI configuration space	
		0x4000 2800 ~ 0x4000 29FF SD Wrapper configuration space	
		0x4000 2A00 ~ 0x4000 A9FF BT Core configuration space	
		0x4000 B000 ~ 0x4000 B0FF SASC-B1 Level 1 bus memory security configuration module	
		0x4000 B100 ~ 0x4000 B1FF SASC-Flash Flash security configuration module	
		0x4000 B200 ~ 0x4000 B2FF SASC-B2 secondary bus memory security configuration module	
APB	0x4001 0000 ~ 0x4001 C000	0x4001 0000 ~ 0x4001 01FF I2C master	
		0x4001 0200 ~ 0x4001 03FF Sigma ADC	
		0x4001 0400 ~ 0x4001 07FF SPI master	
		0x4001 0600 ~ 0x4001 07FF UART0	
		0x4001 0800 ~ 0x4001 09FF UART1	
		0x4001 0A00 ~ 0x4001 0BFF UART2	
		0x4001 0C00 ~ 0x4001 0DFF UART3	
		0x4001 0E00 ~ 0x4001 0FFF UART4	

		0x4001 1000 ~ 0x4001 11FF UART5	
		0x4001 1200 ~ 0x4001 13FF GPIO-A	
		0x4001 1400 ~ 0x4001 15FF GPIO-B	
		0x4001 1600 ~ 0x4001 17FF WatchDog	
		0x4001 1800 ~ 0x4001 19FF Timer	
		0x4001 1A00 ~ 0x4001 1BFF RF_Controller	
		0x4001 1C00 ~ 0x4001 1DFF LCD	
		0x4001 1E00 ~ 0x4001 1FFF PWM	
		0x4001 2000 ~ 0x4001 22FF I²S	
		0x4001 2200 ~ 0x4001 23FF BT-modem	
		0x4001 2400 ~ 0x4001 25FF Touch Sensor	
		0x4001 2600 ~ 0x4001 25FF TIPC Interface security settings	
		0x4001 4000 ~ 0x4000 BFFF RF_BIST DAC transmit memory	
		0x4001 C000 ~ 0x4003 BFFF RF_BIST ADC receive memory	
		0x4001 3C00 ~ 0x5FFF FFFF RSV	

5 Functional description

5.1 SDIO HOST controller

The SDIO HOST device controller provides a digital interface capable of accessing Secure Digital Input Output (SDIO) and MMC cards. were able

Access SDIO devices and SD card devices compatible with SDIO 2.0 protocol. The main interfaces are CK, CMD and 4 data lines.

- Compatible with SD Card Specification 1.0/1.1/2.0(SDHC)
- Compatible with SDIO Memory Card Specification 1.1.0
- Compatible with MMC specification 2.0~4.2
- Configurable interface clock rate, support host rate 0~50MHz
- Support standard MMC interface
- Support up to 1024 bytes Block
- Support soft reset function
- Automatic Command/Response CRC generation/verification
- Automatic data CRC generation/checking
- Configurable timeout detection
- Support SPI, 1-bit SD and 4-bit SD modes
- Support DMA data transfer

5.2 SDIO Device Controller

SDIO2.0 device-side interface to complete the data interaction with the host. Internally integrates 1024Byte asynchronous FIFO to complete the data between the host and the chip interact.

- Compatible with SDIO Card Specification 2.0
- Support host rate 0~50MHz
- Support up to 1024 bytes Block
- Support soft reset function
- Support SPI, 1-bit SD and 4-bit SD modes

5.3 High Speed SPI Device Controller

Compatible with the general SPI physical layer protocol, by agreeing on the data format for interaction with the host, the host can access the device at a high speed, and the maximum supported operating frequency is

50Mbps.

- Compatible with general SPI protocol
- Selectable level interrupt signal
- Support up to 50Mbps rate
- Simple frame format, full hardware analysis and DMA

5.4 DMA Controller

Support up to 8 channels, 16 DMA request sources, support linked list structure and register control.

- Amba2.0 standard bus interface, 8 DMA channels
- Support DMA operation based on memory linked list structure
- Software configures 16 hardware request sources
- Support 1, 4-burst operation mode
- Support byte, half-word, word operations
- The source and destination addresses are unchanged or sequentially incremented, configurable or cyclically operate within a predefined address range
- Synchronous DMA request and DMA response hardware interface timing

5.5 Clock and Reset

Support chip clock and reset system control, clock control includes clock frequency conversion, clock shutdown and adaptive gating; reset control includes system and

And the soft reset control of the sub-module.

5.6 Memory Manager

Support the configuration of sending and receiving buffer size, as well as control information such as the base address of MAC access buffer, the number of buffers, and the upper limit of frame aggregation.

5.7 Digital baseband

Support IEEE802.11a/b/g/e/n (1T1R) transmitter and receiver algorithm implementation, the main parameters:

- Data rate: 1~54Mbps (802.11a/b/g), 6.5~150Mbps(802.11n)
- MCS format: MCS0~MCS7, MCS32 (40MHz HT Duplicate mode)
- Support 40MHz bandwidth non-HT Duplicate mode, 6M~54M
- Signal bandwidth: 20MHz, 40MHz
- Modulation: DSSS (DBPSK, DQPSK, CCK) and OFDM (BPSK, QPSK, 16QAM, 64QAM)
- Realize 1T1R MIMO-OFDM spatial multiplexing
- Support Short GI mode
- Support legacy mode and Mixed mode
- Support the transmission and reception of 20M upper and lower sideband signals under 40MHz bandwidth
- Support STBC reception of MCS0~7, 32
- Support Green Field mode

5.8 MAC Controller

Support IEEE802.11a/b/g/e/n MAC sublayer protocol control, specific specifications include:

- Support EDCA channel access mode
- Support CSMA/CA, NAV and TXOP protection mechanism
- Beacon, Mng, VO, VI, BE, BK five-way sending queue and QoS
- Support single and wide group wave frame receiving and sending
- Support RTS/CTS, CTS2SELF, Normal ACK, No ACK frame sequence
- Support retransmission mechanism and retransmission rate and power control
- Support MPDU hardware aggregation and de-aggregation and Immediate BlockAck mode

• Support RIFS, SIFS, AIFS

• Support reverse transfer mechanism

• Support TSF timing, and software configurable

• Support MIB statistics

5.9 Security system

Support the security algorithm stipulated in IEEE802.11a/b/g/e/n protocol, cooperate to complete the encryption and decryption of sending and receiving data frames.

• Satisfied that the encryption and decryption throughput rate is greater than 150Mbps

• Amba2.0 standard bus interface

• Support WAPI Security Mode 2.0

• Support WEP security mode - 64-bit encryption

• Support WEP security mode - 128-bit encryption

• Support TKIP security mode

• Support CCMP security mode

5.10 FLASH controller

• Provide bus access FLASH interface

• Provide system bus and data bus access arbitration

• Realize the CACHE cache system to improve the access speed of the FLASH interface

• Provide compatibility with different QFlash

5.11 RSA encryption module

RSA operation hardware coprocessor, providing Montgomery (FIO algorithm) modular multiplication operation function. Cooperate with RSA software library to realize RSA algorithm.

Supports 128-bit to 2048-bit modular multiplication.

5.12 General hardware encryption module

The encryption module automatically completes the encryption of the source address space data of the specified length, and automatically writes the encrypted data back to the specified destination address space after completion;

Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG.

- Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG encryption algorithm
- DES/3DES supports both ECB and CBC modes
- AES supports three modes: ECB, CBC and CTR
- CRC supports CRC8, CRC16_MODBUS, CRC16_CCITT and CRC32 four modes
- CRC supports input/output reverse
- SHA1/MD5/CRC supports continuous multi-packet encryption
- Built-in true random number generator, also supports seed seed to generate pseudo-random numbers

5.13 I2C Controller

APB bus protocol standard interface, only supports the main device controller, I²C working frequency support can be configured, 100K-400K.

5.14 Master/Slave SPI Controller

Supports synchronous SPI master-slave functionality. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

- 8-word-deep FIFOs for transmit and receive paths
- master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire timing
- slave supports 4 formats of Motorola SPI (CPOL, CPHA);
- Support full duplex and half duplex
- The master device supports bit transmission, up to 65535bit transmission
- The slave device supports transmission modes of various byte lengths
- The maximum clock frequency of SPI_Clk input from the device is 1/6 of the system clock

5.15 UART Controller

- The device side conforms to the APB bus interface protocol
- Support interrupt or polling mode
- Support DMA transfer mode, each send and receive has 32-byte FIFO
- Programmable baud rate
- 5-8bit data length, and parity polarity can be configured
- 1 or 2 stop bits configurable
- Support RTS/CTS flow control
- Support Break frame sending and receiving
- Overrun, parity error, frame error, rx break frame interrupt indication
- Maximum 16-burst byte DMA operation

5.16 GPIO Controller

Configurable GPIO, software-controlled input and output, hardware-controlled input and output, configurable interrupt mode.

The GPIOA and GPIOB registers have different starting addresses, but the functions are the same.

5.17 Timers

Microsecond and millisecond timing (the number of counts is configured according to the clock frequency), and six configurable 32-bit counters are realized. When the counting configured by the corresponding calculator is completed

When successful, a corresponding interrupt is generated.

5.18 Watchdog Controller

Support "watchdog" function. Observe the correctness of software behavior and allow a global reset after a system crash. "Watchdog" generates a periodic

The system software must respond to the interrupt and clear the interrupt flag; if the interrupt flag has not been cleared for a long time due to system crash, then

Generate a hard reset to perform a global reset of the system.

5.19 RF Configurator

A synchronous SPI master function is implemented. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

- 1-word-deep FIFOs for transmit and receive paths

5.20 RF Transceiver

- The radio frequency transceiver part includes modules including power amplifier, transmit path, receive path, phase-locked loop and SPI. By adjusting the control

Control ports SHDN, RXEN and TXEN to change the working state of the chip

- The receiving channel adopts a zero-IF structure, which directly converts the RF signal into two outputs of baseband I and Q. The RF front end works at 2.4GHz,

Contains a low noise amplifier and a quadrature mixer; the baseband is composed of a low-pass filter and a variable gain amplifier to achieve channel filtering and gain control;

Driver Amplifier Provides Different DC Outputs for ADC Interface

- The transmission path includes: programmable control filter, up-conversion mixer, variable gain amplifier and power amplifier, and the transmission path also uses direct

Frequency conversion structure. The output signal of the DAC passes through a low-pass filter to filter out the image frequency and out-of-band noise. PA outputs are differential output drivers

off-chip antenna

5.21 PWM Controller

- 5-channel PWM signal generation function

- 2-channel input signal capture function (PWM0 and PWM4 two channels)

- Frequency range: 3Hz~160KHz

- Maximum accuracy of duty cycle: 1/256, counter width for inserting dead zone: 8bit

5.22 I²S Controller

- Support AMBA APB bus interface, 32bit single read and write operations

- Support master and slave mode, can work duplex

- Support 8/16/24/32 bit width, the highest sampling frequency is 128KHz

• Support mono and stereo mode

• Compatible with I²S and MSB justified data format, compatible with PCM A/B format

• Support DMA request read and write operations. Only word-by-word operations are supported

5.23 7816/UART Controller

• The device side conforms to the APB bus interface protocol

• Support interrupt or polling mode

• Support DMA transfer mode, each send and receive has 32-byte FIFO

• DMA can only operate by byte, the maximum 16-burst byte DMA operation

Compatible with UART and 7816 interface functions:

Serial function:

• Programmable baud rate

• 5-8bit data length, and parity polarity can be configured

• 1 or 2 stop bits configurable

• Support RTS/CTS flow control

• Support Break frame sending and receiving

• Overrun, parity error, frame error, rx break frame interrupt indication

7816 interface function:

• Compatible with ISO-7816-3 T=0.T=1 mode

• Compatible with EVM2000 protocol

• Configurable guard time (11 ETU-267 ETU)

• Forward/reverse convention software configurable

• Support sending/receiving parity check and retransmission function

• Support 0.5 and 1.5 stop bit configuration

5.24 ADCs

The acquisition module based on Sigma-Delta ADC completes the acquisition of up to 4 channels of analog signals, and the sampling rate is controlled by an external input clock.

It can collect the input voltage and also collect the chip temperature, and supports input calibration and temperature compensation calibration.

5.25 Touch key controller

The basic functions of the module are as follows:

• Support up to 15 channels of Touch Sensor scanning

• Record the scanning results of each Touch Sensor

• Report scan results through interrupts

6 Pin definition

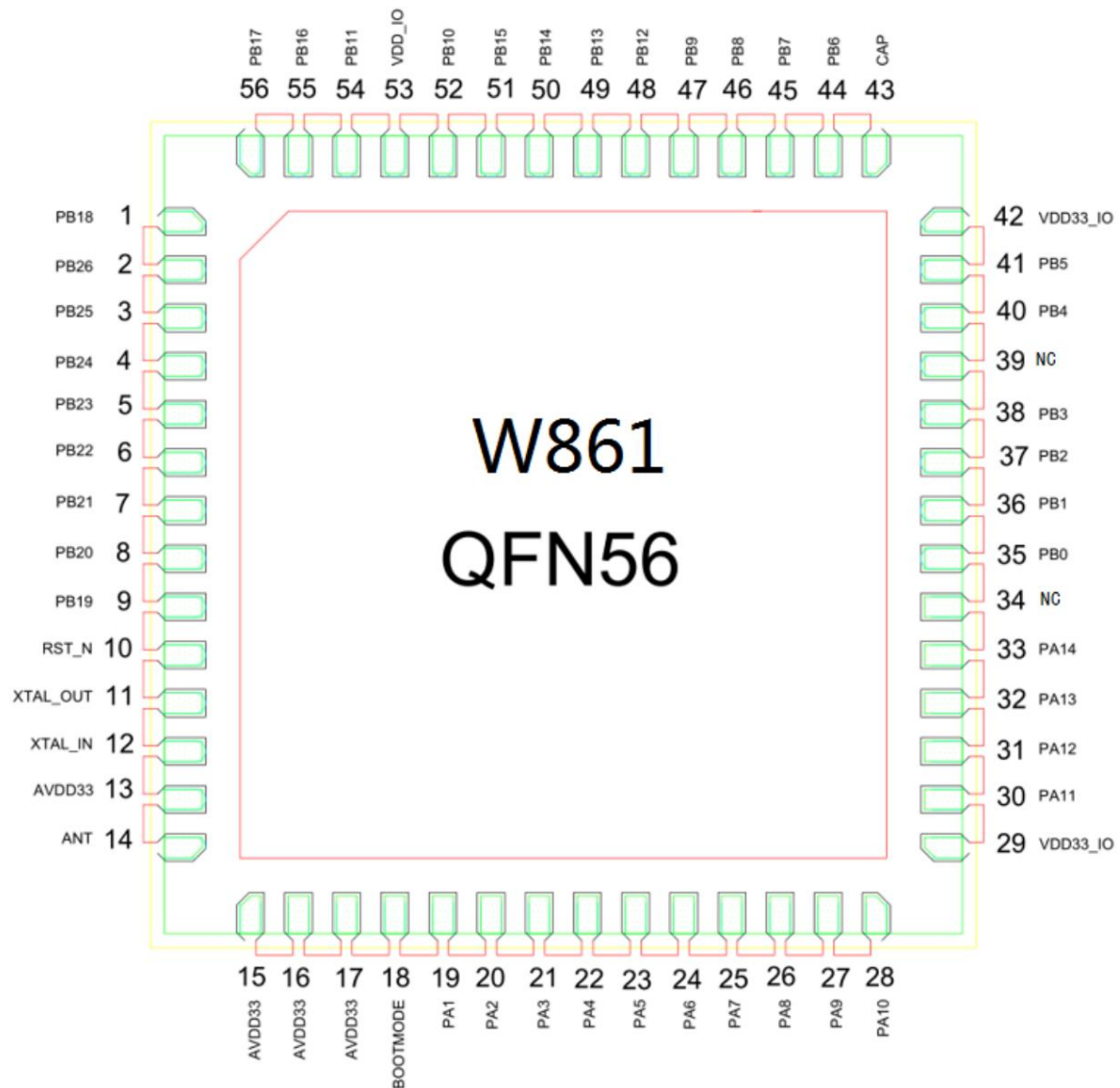


Figure 6-1 W861 pin layout (QFN56)

Table 6-1 W861 pin assignment definition (QFN56)

No.	Name	Type	Pin	Function	After Reset	multiplexing function	Highest frequency pull-up and pull-down capability	drive capability	
1	PB_18	I/O	GPIO	input, high impedance	UART5_TX/LCD_SEG30		10MHz	UP/DOWN	12mA
2	PB_26	I/O	GPIO	input, high impedance	LSPI_MOSI/PWM4/LCD_SEG1		20MHz	UP/DOWN	12mA
3	PB_25	I/O	GPIO	input, high impedance	LSPI_MISO/PWM3/LCD_COM0		20MHz	UP/DOWN	12mA
4	PB_24	I/O	GPIO	input, high impedance	LSPI_CK/PWM2/LCD_SEG2		20MHz	UP/DOWN	12mA
5	PB_23	I/O	GPIO	input, high impedance	LSPI_CS/PCM_DATA/LCD_SEG0		20MHz	UP/DOWN	12mA
6	PB_22	I/O	GPIO	input, high impedance	UART0_CTS/PCM_CK/LCD_COM2		10MHz	UP/DOWN	12mA
7	PB_21	I/O	GPIO	input, high impedance	UART0_RTS/PCM_SYNC/LCD_COM1		10MHz	UP/DOWN	12mA
8	PB_20	I/O	UART_RX		UART0_RX/PWM1/UART1_CTS/I2C_SCL		10MHz	UP/DOWN	12mA
9	PB_19	I/O	UART_TX		UART0_TX/PWM0/UART1_RTS/I2C_SDA		10MHz	UP/DOWN	12mA
10	RESET	I	RESET	Reset				UP	
11	XTAL_OUT	O		External crystal oscillator output					
12	XTAL_IN	I		External crystal oscillator input					
13	AVDD33	P		chip power supply, 3.3V					
14	ANT	I/O	RF	Antenna					
15	AVDD33	P		chip power supply, 3.3V					
16	AVDD33	P		chip power supply, 3.3V					
17	AVDD33_AUx	P		chip power supply, 3.3V					
18	BOOTMODE	I/O	BOOTMODE		I2S_MCLK/LSPI_CS/PWM2/I2S_DO		20MHz	UP/DOWN	12mA
19	PA_1	I/O	JTAG_CK		JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/ADC_1		20MHz	UP/DOWN	12mA
20	PA_2	I/O	GPIO	input, high impedance	UART1_RTS/UART2_TX/PWM0/UART3_RTS/ADC_4		20MHz	UP/DOWN	12mA
	PA_3	I/O	GPIO	input, high impedance	UART1_CTS/UART2_RX/PWM1/UART3_CTS/ADC_3		20MHz	UP/DOWN	12mA
	PA_4	I/O	JTAG_SWO		JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/ADC_2		20MHz	UP/DOWN	12mA
	PA_5	I/O	GPIO	input, high impedance	UART3_TX/UART2_RTS/PWM_BREAK/UART4_RTS/VRP_EXT		20MHz	UP/DOWN	12mA
	PA_6	I/O	GPIO	input, high impedance	UART3_RX/UART2_CTS/NULL/UART4_CTS/LCD_SEG31/VRP_EXT		20MHz	UP/DOWN	12mA
25	PA_7	I/O	GPIO	input, high impedance	PWM4/LSPI_MOSI/I2S_MCK/I2S_DI/LCD_SEG3/Touch_1		20MHz	UP/DOWN	12mA
26	PA_8	I/O	GPIO	input, high impedance	PWM_BREAK/UART4_TX/UART5_TX/I2S_BCLK/LCD_SEG4		20MHz	UP/DOWN	12mA

27	PA_9	I/O GPIO	O, input, high impedance	MMC_CLK/UART4_RX/UART5_RX/I2S_LR CLK/LCD_SEG5/TOUCH_2	50MHz	UP/DOWN	12mA
28	PA_10	I/O GPIO	O, input, high impedance	MMC_CMD/UART4_RTS/PWM0/I2S_DO/LC D_SEG6/TOUCH_3	50MHz	UP/DOWN	12mA
29	VDD33IO		PIO power supply, 3.3V				
30	PA_11	I/O GPIO	O, input, high impedance	MMC_DAT0/UART4_CTS/PWM1/I2S_DI/L CD_SEG7	50MHz	UP/DOWN	12mA
31	PA_12	I/O GPIO	O, input, high impedance	MMC_DAT1/UART5_TX/PWM2/LCD_SEG8/ TOUCH_14	50MHz	UP/DOWN	12mA
32	PA_13	I/O GPIO	O, input, high impedance	MMC_DAT2/UART5_RX/PWM3/LCD_SEG9	50MHz	UP/DOWN	12mA
33	PA_14	I/O GPIO	O, input, high impedance	MMC_DAT3/UART5_CTS/PWM4/LCD_SEG1 0/TOUCH_15	50MHz	UP/DOWN	12mA
34	NC						
35	PB_0	I/O GPIO	O, input, high impedance	PWM0/LSPI_MISO/UART3_TX/LCD_SEG1 2/Touch_4	80MHz	UP/DOWN	12mA
36	PB_1	I/O GPIO	O, input, high impedance	PWM1/LSPI_CK/UART3_RX/LCD_SEG13/ Touch_5	80MHz	UP/DOWN	12mA
37	PB_2	I/O GPIO	O, input, high impedance	PWM2/LSPI_CK/UART2_TX/LCD_SEG14/ Touch_6	80MHz	UP/DOWN	12mA
38	PB_3	I/O GPIO	O, input, high impedance	PWM3/LSPI_MISO/UART2_RX/LCD_SEG1 5/Touch_7	80MHz	UP/DOWN	12mA
39	NC						
40	PB_4	I/O GPIO	O, input, high impedance	LSPI_CS/UART2_RTS/UART4_TX/LCD_S EG16/Touch_8	80MHz	UP/DOWN	12mA
41	PB_5	I/O GPIO	O, input, high impedance	LSPI_MOSI/UART2_CTS/UART4_RX/LCD _SEG17/Touch_9	80MHz	UP/DOWN	12mA
42	VDD33IO		PIO power supply, 3.3V				
43	CAP		I External capacitor, 1μF				
44	PB_6	I/O GPIO	O, input, high impedance	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK /LCD_SEG18/Touch_10	50MHz	UP/DOWN	12mA
45	PB_7	I/O GPIO	O, input, high impedance	UART1_RX/MMC_CMD/HSPI_INT/SDIO_C MD/LCD_SEG19/Touch_11	50MHz	UP/DOWN	12mA
46	PB_8	I/O GPIO	O, input, high impedance	I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0 /LCD_SEG20/Touch_12	50MHz	UP/DOWN	12mA
47	PB_9	I/O GPIO	O, input, high impedance	I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/ LCD_SEG21/Touch_13	50MHz	UP/DOWN	12mA
48	PB_12	I/O GPIO	O, input, high impedance	HSPI_CK/PWM0/UART5_CTS/I2S_BCLK/ LCD_SEG24	50MHz	UP/DOWN	12mA
49	PB_13	I/O GPIO	O, input, high impedance	HSPI_INT/PWM1/UART5_RTS/I2S_LRCL K/LCD_SEG25	50MHz	UP/DOWN	12mA

50	PB_14	I/O GPIO, input, high impedance	HSPI_CS/PWM2/LSPI_CS/I2S_DO/LCD_SEG26	50MHz	UP/DOWN	12mA
51	PB_15	I/O GPIO, input, high impedance	HSPI_DI/PWM3/LSPI_CK/I2S_DI/LCD_SEG27	50MHz	UP/DOWN	12mA
52	PB_10	I/O GPIO, input, high impedance	I2S_DI/MMC_D2/HSPI_DI/SDIO_D2/LCD_SEG22	50MHz	UP/DOWN	12mA
53	VDD33IO	PIO power supply, 3.3V				
54	PB_11	I/O GPIO, input, high impedance	I2S_DO/MMC_D3/HSPI_DO/SDIO_D3/LCD_SEG23	50MHz	UP/DOWN	12mA
55	PB_16	I/O GPIO, input, high impedance	HSPI_DO/PWM4/LSPI_MISO/UART1_RX/LCD_SEG28	50MHz	UP/DOWN	12mA
56	PB_17	I/O GPIO, input, high impedance	UART5_RX/PWM_BREAK/LSPI_MOSI/I2S_MCLK/LCD_SEG29	20MHz	UP/DOWN	12mA

Note: 1. I = Input, O = Output, P = Power

7 Electrical Characteristics

7.1 Limit parameters

Table 7-1 Limit parameters

parameter	name	minimum value	typical value	maximum value	unit
supply voltage	VDD	3.0	3.3	3.6	V
Input Logic Level Low	VIL	-0.3		0.8	V
Input logic level high	VIH	2.0		VDD+0.3	V
Input Pin Capacitance	Cpad			2	pF
output logic level low	VOL			0.4	V
output logic level high	VOH	2.4			V
Output maximum drive capacity	IMAX			twenty four	mA
storage temperature range	TSTR	-40°C		+125°C	°C
range of working temperature	TOPR	-40°C		+85°C	°C

7.2 RF Power Consumption Parameters

Test conditions: 3.3V power supply, transmit according to 50% duty cycle test.

Table 7-2 RF power consumption parameters

model	typical value	unit
Transmit IEEE802.11b 1Mbps POUT = +19.4dBm	240	mA
Transmit IEEE802.11b 11Mbps	240	

POUT = +19.3dBm		
Transmit IEEE802.11g 54Mbps POUT = +14.7dBm	190	mA
Send IEEE802.11n MCS7 POUT = +12dBm	180	mA
Receive IEEE802.11b/g/n	95	mA

7.3 Wi-Fi Radio

Table 7-3 Wi-Fi radio parameters

parameter	typical value	unit
input frequency	2.4~2.4835	GHz
transmit power		
IEEE802.11b 11Mbps	19±2	dBm
IEEE802.11g 54Mbps	16±2	dBm
IEEE802.11n MCS7 HT20	13±2	dBm
Receiver sensitivity		
IEEE802.11b 1Mbps	-96	dBm
IEEE802.11b 11Mbps	-86	dBm
IEEE802.11g 54Mbps	-73	dBm
IEEE802.11g MCS7 HT20	-71	dBm

Adjacent channel inhibition		
IEEE802.11b 6Mbps	32	dB
IEEE802.11g 54Mbps	16	dB
IEEE802.11n HT20, MCS0	31	dB
IEEE802.11n HT20, MCS7	12	dB

7.4 Bluetooth RF

7.4.1 Traditional Bluetooth RF

Receiver - Base Data Rate (BR)

parameter	condition	Min	Typ	Max	Unit
Sensitivity@0.1% BER				-91	dBm
Maximum Received Signal@0.1% BER				0	dBm
Co-channel rejection ratio C/I				9	dB
out-of-band blocking	30 MHz ~ 2000 MHz			-10	dBm
	2000 MHz ~ 2400 MHz			-27	dBm
	2500 MHz ~ 3000 MHz			-27	dBm
	3000MHz ~ 12.5GHz			-10	dBm
Intermodulation				-39	dB

Emitter - Base Rate (BR)

parameter	condition	Min	Typ	Max	Unit
RF transmit power			6		dBm
Gain Control Step Size			3		db
RF power control range		-10		12	dBm
20dB bandwidth		0.918	0.923		
γ f1avg			159.8		
γ f2max			142.8		
γ f2avg/ γ f1avg			0.89		
ICFT			0		
Drift rate		-2.25	-2.08	2.23	kHz
Offset (DH1)		-4		-1	kHz
Offset (DH5)			0		kHz

Receiver - Enhanced Rate (EDR)

parameter	condition	Min	Typ	Max	Unit
$\gamma/4$ DQPSK					
Sensitivity@0.01% BER			-88		dBm
Maximum received signal@0.01% BER			0		dBm

8DPSK					
Sensitivity@0.01% BER			-81		dBm
Maximum received signal@0.01%			0		dBm
BER					

Transmitter - Enhanced Data Rate (EDR)

parameter	condition	Min	Typ	Max	Unit
RF transmit power				0	dBm
Gain Control Step Size				3	db
RF power control range		-10		8	dBm
π/4 DQPSK max w0		-3.2		2.6	KHz
π/4 DQPSK max wi		-5.3		-2.4	KHz
π/4 DQPSK max wi + w0		-4.8		-3.9	KHz
8DPSK max w0		-1.4		1.5	KHz
8DPSK max wi		-4.1		-2.9	KHz
8DPSK max wi + w0		-4.8		-4.1	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVM		6.7		%
	99% DEVM		100		%
	Peak DEVM		14.1		%
8 DPSK modulation accuracy	RMS DEVM		6.8		%

	99% DEVM		99.99		%
	Peak DEVM		15.3		%
EDR differential phase encoding			100		%

7.4.2 Bluetooth Low Energy Radio

receiver

parameter	condition	Min	Typ	Max	Unit
Sensitivity@30.8% PER				-94	dBm
Maximum received signal@30.8% PER				0	dBm
out-of-band blocking	30MHz~2000MHz			-30	dBm
	2003MHz~2399MHz			-35	dBm
	2484MHz~3000MHz			-35	dBm
	3000MHz~12.5GHz			-30	dBm
Intermodulation				-47	dBm

launcher

parameter	condition	Min	Typ	Max	Unit
RF transmit power				6	dBm
Gain Control Step Size				2	db
RF power control range		-10		12	dBm

Ƴ f1avg		240.8	241.2 242		kHz
Ƴ f2max		175.7	182.7 183.9 kHz		
Drift rate			1.5		kHz
offset			-4.3		kHz

Winner Micro

8 Package Information

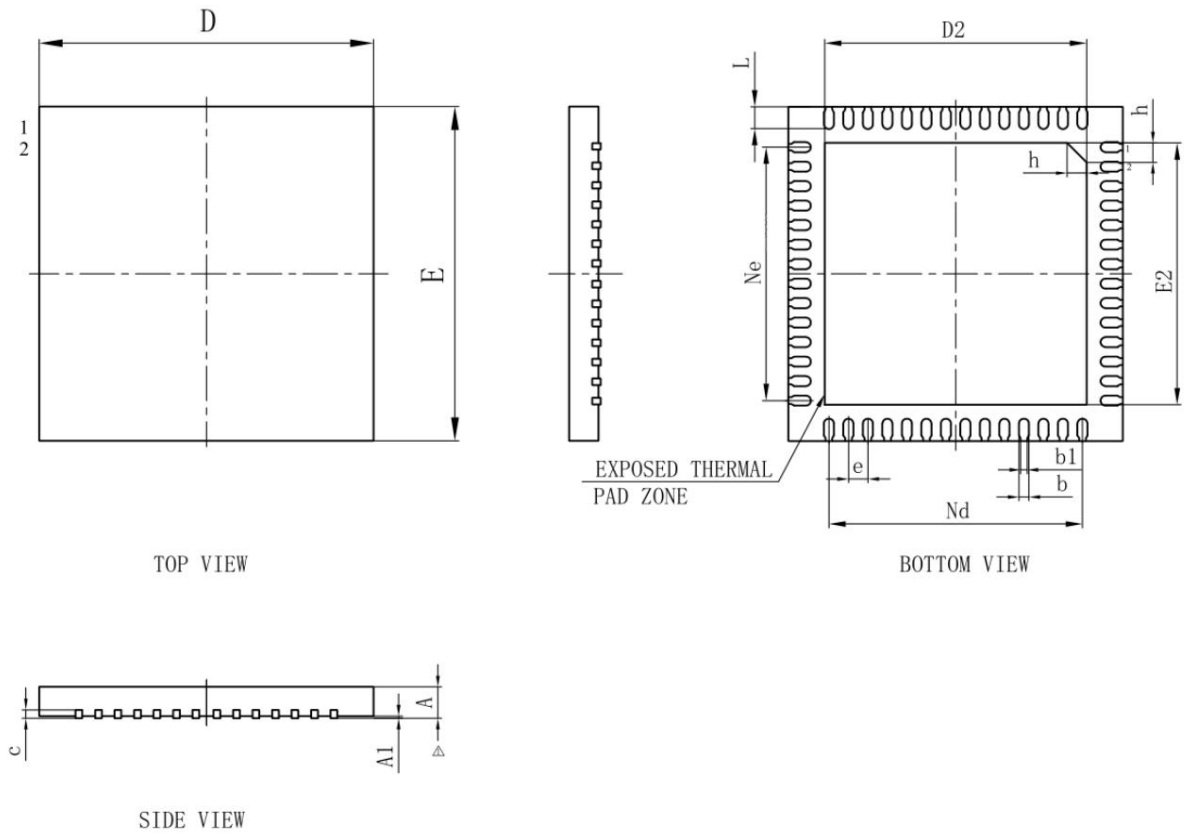


Figure 8-1 W861 package parameters

Table 8-1 W861 Package Parameters

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
b1	0.12 REF		

c	0.18	0.20	0.25
D.	5.90	6.00	6.10
D2	4.60	4.70	4.80
e	0.35BSC		
Ne	4.55BSC		
Nd	4.55BSC		
E.	5.90	6.00	6.10
E2	4.60	4.70	4.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F carrier size	193x193		