



Air103 core board design manual

Document name	Air103 core board design manual
author	wuzhuangzhuang
Modification date	2021.11.23
Version	1.2
Document status	internal

Table of contents

1. Product description.....3

2. Hardware resources.....4

3. Pin definition.....5

4. Function introduction.....8

5. Follow us.....10

Modification record:

Version number modification record	date	author
V1.0 new	2021-10-25	wuzhuangzhuang
V1.1 update pictures	2021-11-16	wuzhuangzhuang
V1.2 updates Pinout pin definition	2021-11-23	wuzhuangzhuang

1. Product description

Air103 core board is a development board designed based on Hezhou Air103 MCU, Size only

21mm*51mm, the edge of the board is designed with stamp holes to facilitate developers to use it in different scenarios. The core board supports UART,

GPIO, SPI, SDIO, I2C, PSRAM, ADC and other interfaces can be selected according to actual needs.

2. Hardware Resources

• Dimensions length and width 21mm*51mm

• 1 PSRAM interface, supports up to 64MB external PSRAM memory

• 6-way UART interface, UART0~UART5

• 4 channels of 16-bit ADC, maximum sampling rate 1KHz

• 1 low-speed SPI interface, supports master mode

• 1 channel SDIO_HOST interface, supports SDIO2.0, SDHC, MMC4.2

• 1 channel IIC controller

• 5-way PWM interface

• GPIO external pins 33 channels, reusable

3. Pin definition

Figure 3-1 is the function description;

Figure 3-2 is the definition of the 20 Pins on the left side;

Figure 3-3 is the definition of the 20 Pins on the right side;

Figure 3-4 is the middle position 8 Pin pin definition. Figure 3-1

供电	接地	特殊引脚	GPIO	UART	I2C	SPI	PWM	ADC	SDIO
----	----	------	------	------	-----	-----	-----	-----	------

Figure 3-2

PWM30	ADC3		GPIO2	PA_02	1	
PWM31	ADC2		GPIO3	PA_03	2	
				GND	3	
				5V	4	
				BOOT	5	
PWM04			GPIO07	PA_07	6	
	ADC1	I2C_SDA	GPIO04	PA_04	7	
	ADC0	I2C_SLK	GPIO01	PA_01	8	
				3.3V	9	
				GND	10	
PWM00		U3_TX	GPIO16	PB_00	11	
	SPI0_CS	U4_TX	GPIO20	PB_04	12	
PWM01		U3_RX	GPIO17	PB_01	13	
PWM03	SPI0_MISO	U2_RX	GPIO19	PB_03	14	
	SPI0_MOSI	U4_RX	GPIO21	PB_05	15	
PWM02	SPI0_CK	U2_TX	GPIO18	PB_02	16	
				3.3V	17	
				GND	18	
PWM13		U5_RX	GPIO13	PA_13	19	
			GPIO34	PB_18	20	



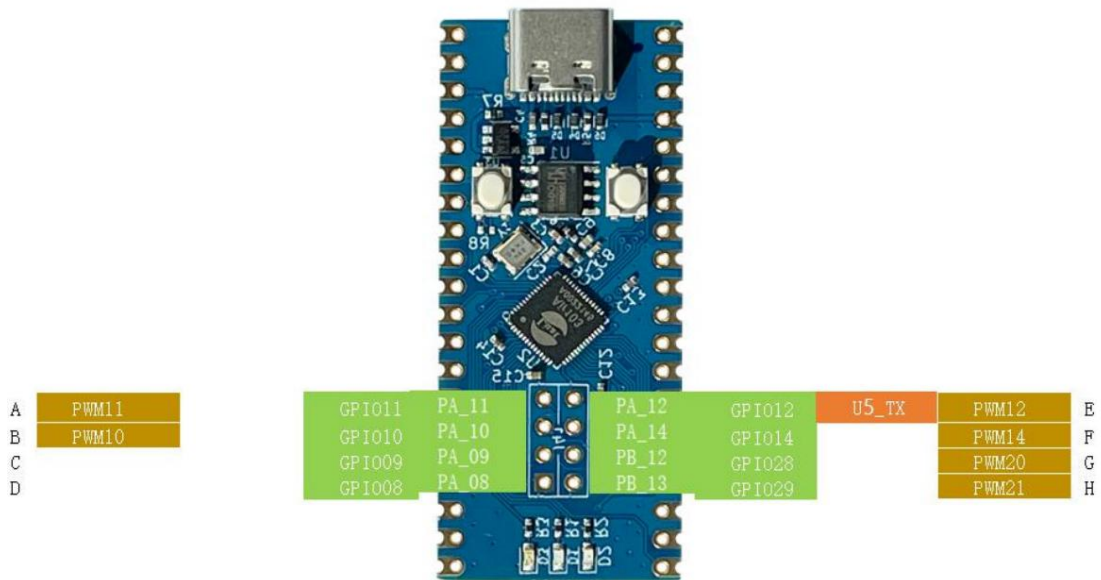


Figure 3-3



21	PB17	GPIO33		SPI1_MOSI	
22	PB16	GPIO32		SPI1_MISO	PWM24
23	5V				
24	PWB				
25	GND				
26	3.3V				
27	RESET				
28	WAKEUP				
29	PB_11	GPIO27		SDIO_D3	
30			U0_RX		
31			U0_TX		
32	GND				
33	PB_10	GPIO26		SDIO_D2	
34	PB_09	GPIO25		SDIO_D1	
35	PB_08	GPIO24		SDIO_D0	
36	PB_07	GPIO23	U1_RX	SDIO_CMD	
37	PB_06	GPIO22	U1_TX	SDIO_CK	
38	GND				
39	PB_15	GPIO31		SPI1_CK	PWM23
40	PB_14	GPIO30		SPI1_CS	PWM22

Figure 3-4



Note: SPI0 and SPI1 are the same SPI controller, and only one can be selected for use; the naming number of the PWM pin is divided into 2 digits:

XY, among which Y is the same PWM pin, only one can be selected and cannot be used at the same time, such as PWM01 and PWM11

They cannot take effect at the same time.

Detailed pin description

Pin serial number	name	Pin functions after multiplexing	Reuse function	Pull up and down ability
1	PA_2	GPIO02, input, high impedance	ADC_3/PWM30	UP/DOWN
2	PA_3	GPIO03, input, high impedance	ADC_2/PWM31	UP/DOWN
3	GND	grounded		
4	5V	5V power interface, and USB VBUS connected		
5	BOOT	BOOTMODE		UP/DOWN
6	PA_7	GPIO07, input, high resistance	PWM04	UP/DOWN
7	PA_4	GPIO04, input, high resistance	I2C_SDA/ADC_1	UP/DOWN
8	PA_1	GPIO01, input, high resistance	I2C_SCL/ADC_0 chip	UP/DOWN
9	3.3V	power supply, 3.3V		
10	GND	ground		
11	PB_0	GPIO16, input, high impedance	PWM00/UART3_TX	UP/DOWN
12	PB_4	GPIO20, input, high impedance	SPI0_CS/PSRAM_D2/UART4_ Tx	UP/DOWN
13	PB_1	GPIO17, input, high impedance	PWM01/UART3_RX	UP/DOWN
14	PB_3	GPIO19, input, high impedance	PWM03/SPI0_MISO/UART2_R X/PSRAM_D1	UP/DOWN
15	PB_5	GPIO21, input, high impedance	SPI0_MOSI/PSARM_D3/UART UP/DOWN	

			4_RX	
16PB_2		GPIO18, input, high impedance	PWM02/SPI0_CK/UART2_TX/ PSRAM_D0	UP/DOWN
17 3.3V		Chip power supply, 3.3V		
18GND		ground		
19PA_13		GPIO13, input, high impedance	UART5_RX/PWM3	UP/DOWN
20 PB_18		GPIO34, input, high impedance /		UP/DOWN
	PB_17	GPIO33, input, high impedance	SPI1_MOSI	UP/DOWN
22PB_16		GPIO32, input, high impedance	SPI1_MISO/PWM24	UP/DOWN
23 5V		5V power interface, with USB VBUS connected		
24 PWB		Chip 3.3V power supply control control, effective at high level, not can be left in the air		
25GND		ground		
26 3.3V		Chip power supply, 3.3V		
27 RESET		chip reset		
28 WAKEUP		wake function		
29	PB_11	GPIO27, input, high impedance	SDIO_D3	UP/DOWN
30 U0_RX		debug port		UP/DOWN
31	U0_TX	RX debug		UP/DOWN
32GND		port TX ground		
33 PB_10		GPIO26, input, high impedance	SDIO_D2	UP/DOWN
34PB_9		GPIO25, input, high impedance	SDIO_D1	UP/DOWN
35PB_8		GPIO24, input, high impedance	SDIO_D0	UP/DOWN
36PB_7		GPIO23, input, high impedance	UART1_RX/SDIO_CMD	UP/DOWN
37PB_6		GPIO22, input, high impedance	UART1_TX/SDIO_CK	UP/DOWN
38GND		Ground		
39PB_15		GPIO31,input, high-impedance	PWM23/SPI1_CK	UP/DOWN
40PB_14		GPIO30,input, high-impedance	PWM22/SPI1_CS	UP/DOWN
A	PA_11	GPIO11,input, high-impedance	PWM11	UP/DOWN
B	PA_10	GPIO10,input, high-impedance	PWM10	UP/DOWN
C	PA_9	GPIO09,input, high-impedance/		UP/DOWN
D	PA_8	GPIO08,input, high-impedance/		UP/DOWN
E	PA_12	GPIO12,input, High impedance	PWM12/UART5_TX	UP/DOWN
F	PA_14	GPIO14, input, high impedance	PWM14	UP/DOWN
G	PB_12	GPIO28, input, high impedance	PWM20	UP/DOWN
H	PB_13	GPIO29, input, high impedance	PWM21	UP/DOWN

4. Function introduction

1. LED control

The Air103 core board is equipped with 3 LEDs. Developers can refer to Table 4-1 to control the corresponding pins.

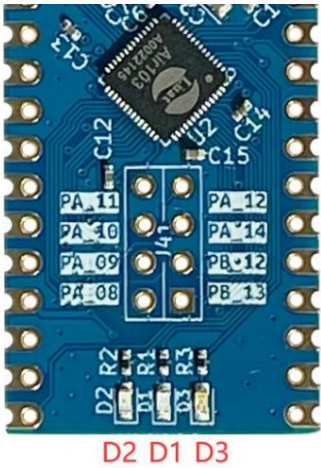


Table 4-1

LED number corresponds to GPIO		Pin function	describe
D1	PB_25	GPIO41 configuration	Active high level
D2	PB_26	GPIO42 configuration	Active high level
D3	PB_24	GPIO40 configuration	Active high level

2. Button introduction

The Air103 core board has two buttons onboard, among which K1 can realize the download function, and K2 can realize the reset function and pin control.

Refer to Table 4-2.

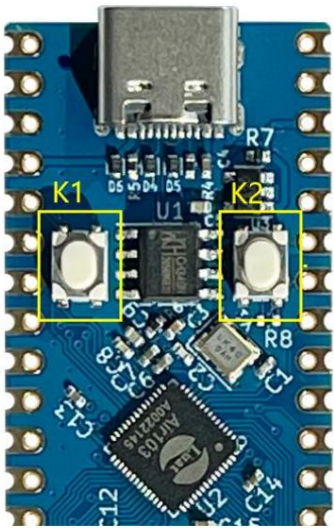


Table 4-2

Button number	When the pin	describe
K1	function button is pressed, the chip enters download mode.	Active low
K2	When the button is pressed, the chip resets.	Active low

3. PSRAM control

The Air103 core board does not have PSRAM by default. Developers can choose according to actual needs. For pin control, refer to Table 4-3.

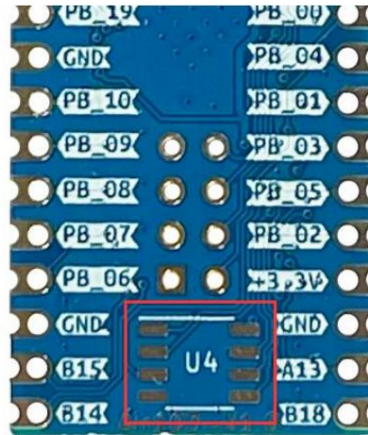


Table 4-3

PSRAM pin label	Corresponding to GPIO	Pin function	Pull up and down ability
CS	PB_27	GPIO43 configuration, PSRAM_CS, chip select	UP/DOWN
D1/SO	PB_03	GPIO19 configuration, PSRAM_D1, data Feet 1	UP/DOWN
WP	PB_04	GPIO20 configuration, PSRAM_D2, data feet 2	UP/DOWN
SI/IO0	PB_02	GPIO18 configuration, PSRAM_D0, data feet 0	UP/DOWN
SCLK	PA_15	GPIO15 configuration, PSRAM_CK, clock	UP/DOWN
HOLD	PB_05	GPIO21 configuration, PSRAM_D3, data feet 3	UP/DOWN

Note: PB_02, PB_03, PB_04, PB_05 are reused with the external pin header of the core board, and PSRAM is used with the external pin header at the same time.

Please pay attention to the configuration method.

5. Follow us

LUAT community: <https://doc.openluat.com>

Hezhou Mall : <http://mall.m.openluat.com>

Product information: <https://luatos.com/t/air103>

Official Taobao store 1: <https://openluat.taobao.com>

Official Taobao store 2: <https://luat.taobao.com>

Official technical support communication WeChat group:



For more updates, please scan the QR code to follow Hezhou's official public account. We look forward to your arrival.

