Air105 Core Board User Manual

Table of contents

1. Product description

The Air105 core board is a development board designed based on the Hezhou Air105 MCU. The size is only 21mm*51mm. The edge of the board is designed with stamp holes, which is convenient for developers to use in different scenarios. The core board supports UART, GPIO, SPI, I2C, PWM, ADC and other interfaces, which can be selected according to actual needs.

2. Hardware resources

ÿ Dimensions length and width 21mm*51mm

ÿ 4-way UART interface, UART0~UART3

ÿ 4-channel 12-bit ADC, the highest sampling rate is 857KHz

ÿ 1 channel DAC, 10-bit digital output, support DMA function

ÿ 4-way SPI interface, supports master mode, among which HSPI is high-speed mode, which are SPI0, SPI1, SPI2, HSPI, where SPI0 supports slave mode

ÿ 1 channel I2C controller

ÿ Support PWM interface in 5+1 mode, of which PWM5 can be used by the camera (LuatOS occupies PWM6 and PWM7)

ÿ Support full speed USB2.0, support device mode

ÿ Support camera

ÿ Support RTC function

ÿ GPIO has 39 external pins, which can be multiplexed; the maximum rate of flipping IO by software operation is 3MHz; PWM mode The output waveform under the mode, the maximum rate is 25.5M (LuatOS maximum 24M)

3. Power consumption

Limit parameters			
parameter		scope	unit
Iddpd	Description	-	nA
Tamb	Shutdown	-40~+85	°C
Tstg	current	-40~+125	°C
Ground	Operating	-0.3~0.3	V
Voh	temperature Storage	VDD -0.3 ~ VDD+0.3	V
Vol	temperature Digital	<0.4	V
Ioh	output high level Digital output low level	27(@3V)	mA
	Source current (PA2/3/4/5,	16(@3V)	mA
Iol	PC6/7/8/9) Source current (other IO) Sink	27(@0.5V)	mA
	current (PA2/3/ 4/5, PC6/7/8/9)	16(@0.5V)	mA
Vih	sink current (other IO) digital input	ÿ0.7×VDD	V
ViL	high level digital input low level	ÿ0.3×VDD	V

4. Pin Definition

ÿ: Figure 3-1 is the function description;

ÿ: Definition of 20 Pins on the left side of Figure 3-2;

ÿ: Definition of 20 Pins on the right side of Figure 3-3;

ÿ: Figure 3-4 is the definition of the 12 Pin pad in the middle position on the back.

Figure 3-1

Figure 3-2

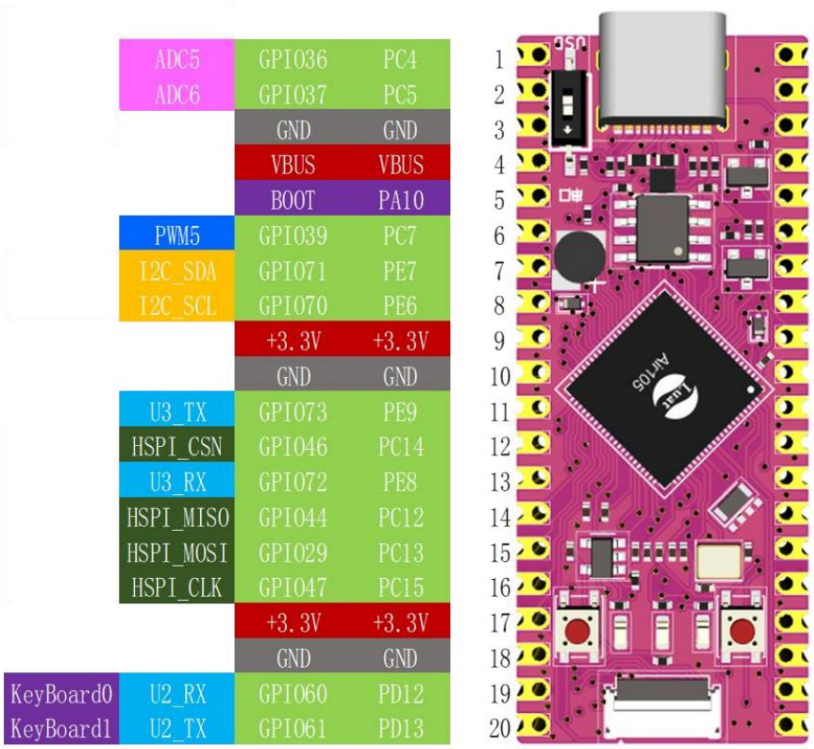


Figure 3-3

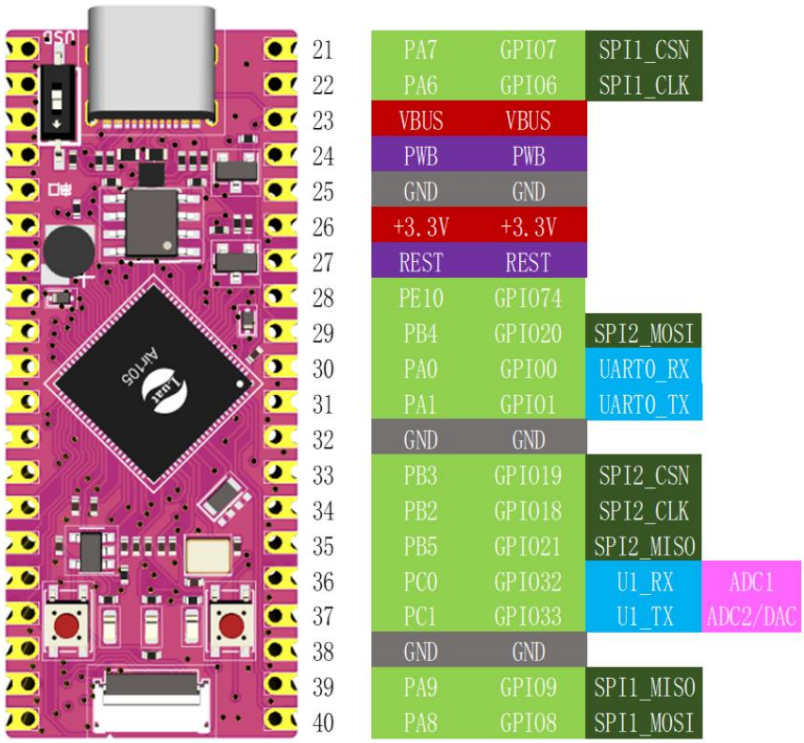
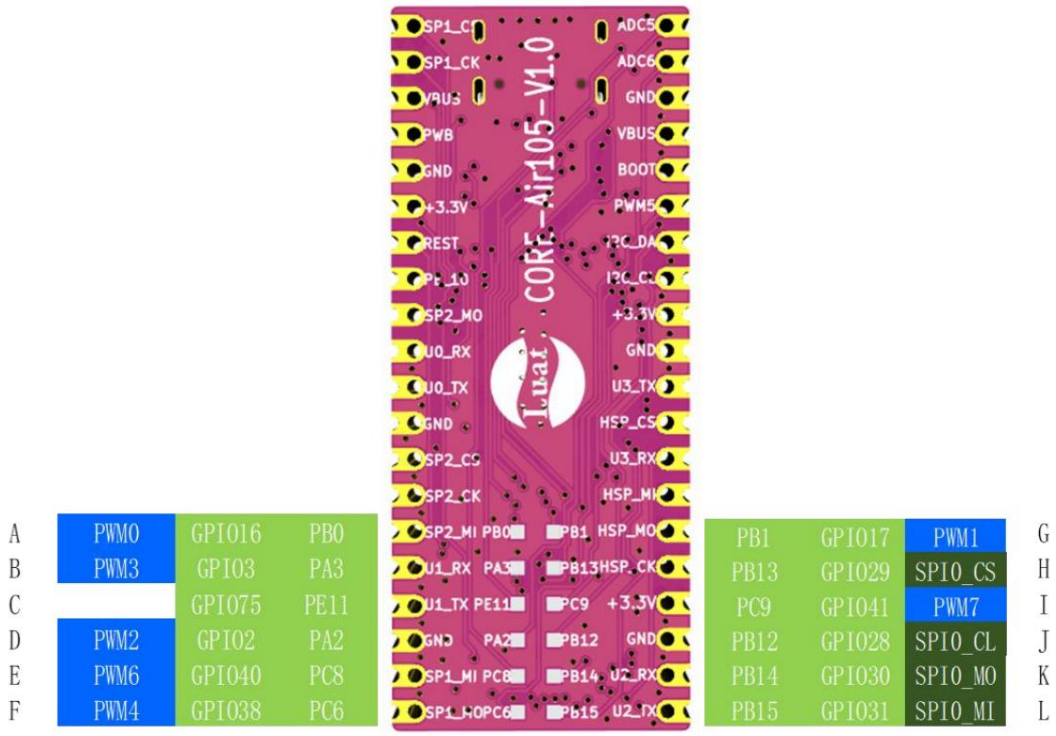


Figure 3-4



Detailed pin description

Pin Details					
All general-purpose I/Os default to pull-up after reset, and the resistance value is 51Kÿ					
Pin Number	Name	Type	Multiplexing function	Up and down ability	Remark
1	PC4	I/O	GPIO36/ADC5	UP/DOWN	
2	PC5	I/O	GPIO37/ADC6	UP/DOWN	
3	GND	GND			ground
4	VBUS	P			5V power interface, VBUS with USB connected
5	PA10	I/O	GPIO10	UP/DOWN	
6	PC7	I/O	GPIO39/PWM5	UP/DOWN	
7	PE7	I/O	GPIO71/I2C_SDA	UP/DOWN	
8	PE6	I/O	GPIO70/I2C_SCL	UP/DOWN	
9	+3.3V	P			chip output 3.3V voltage
10	GND	GND			ground
11	PE9	I/O	GPIO73/U3_TX	UP/DOWN	
12	PC14	I/O	GPIO46/HSPI_CSN	UP/DOWN	High-speed SPI
13	PE8	I/O	GPIO72/U3_RX	UP/DOWN	
14	PC12	I/O	GPIO44/HSPI_MISO	UP/DOWN	High-speed SPI

15	PC13	I/O	GPIO29/HSPI_MOSI	UP/DOWN	High-speed SPI
16	PC15	I/O	GPIO47/HSPI_CLK	UP/DOWN	High-speed SPI
17	+3.3V	P			chip output 3.3V voltage
18	GND	GND			ground
19	PD12	I/O	GPIO60/U2_RX/KeyBoard0	UP/DOWN	
20	PD13	I/O	GPIO61/U2_TX/KeyBoard1	UP/DOWN	
twenty one	PA7	I/O	GPIO7/SPI1_CSN	UP/DOWN	
twenty two	PA6	I/O	GPIO6/SPI1_CLK	UP/DOWN	
twenty three	VBUS	P			5V power interface, VBUS with USB connected
twenty four	PWB				Don't hang
25	GND	GND			ground
26	+3.3V	P			chip output 3.3V voltage
27	REST				chip reset
28	PE10	I/O	GPIO74	UP/DOWN	
29	PB4	I/O	GPIO20/SPI2_MOSI	UP/DOWN	
30	PA0	I/O	GPIO0/UART0_RX	UP/DOWN	download pin
31	PA1	I/O	GPIO1/UART0_TX	UP/DOWN	
32	GND	GND			ground
33	PB3	I/O	GPIO19/SPI2_CSN	UP/DOWN	
34	PB2	I/O	GPIO18/SPI2_CLK	UP/DOWN	
35	PB5	I/O	GPIO21/SPI2_MISO	UP/DOWN	
36	PC0	I/O	GPIO32/U1_RX/ADC1	UP/DOWN	
37	PC1	I/O	GPIO33/U1_TX/ADC2/DAC	UP/DOWN	
38	GND	GND			ground
39	PA9	I/O	GPIO9/SPI1_MISO	UP/DOWN	
40	PA8	I/O	GPIO8/SPI1_MOSI	UP/DOWN	
A	PB0	I/O	GPIO16/PWM0	UP/DOWN	
B	PA3	I/O	GPIO3/PWM3	UP/DOWN	
C	PE11	I/O	GPIO75	UP/DOWN	
D	PA2	I/O	GPIO2/PWM2	UP/DOWN	
E	PC8	I/O	GPIO40/PWM6	UP/DOWN	
F	PC6	I/O	GPIO38/PWM4	UP/DOWN	
G	PB1	I/O	GPIO17/PWM1	UP/DOWN	
H	PB13	I/O	GPIO29/SPI0_CS	UP/DOWN	
I	PC9	I/O	GPIO41/PWM7	UP/DOWN	
J	PB12	I/O	GPIO28/SPI0_CL	UP/DOWN	
K	PB14	I/O	GPIO30/SPI0_MO	UP/DOWN	
L	PB15	I/O	GPIO31/SPI0_MI	UP/DOWN	

Note: I, for input; O, for output; P, for power

5. Function introduction

LED control

The Air105 core board has 3 LEDs onboard. Developers can refer to Table 4-1 to control the corresponding pins.

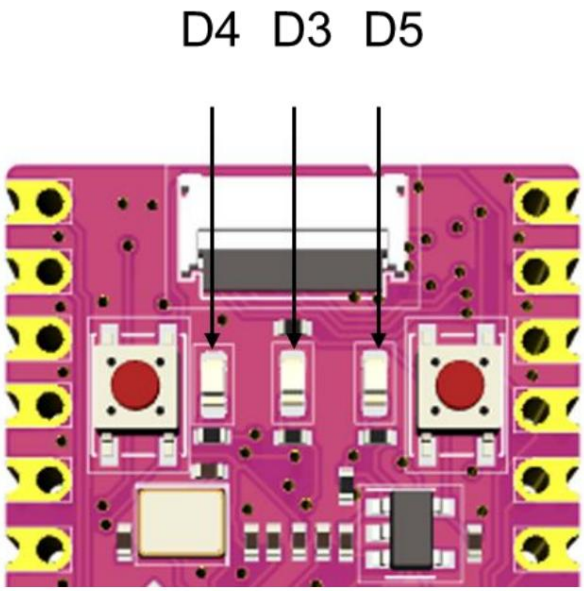
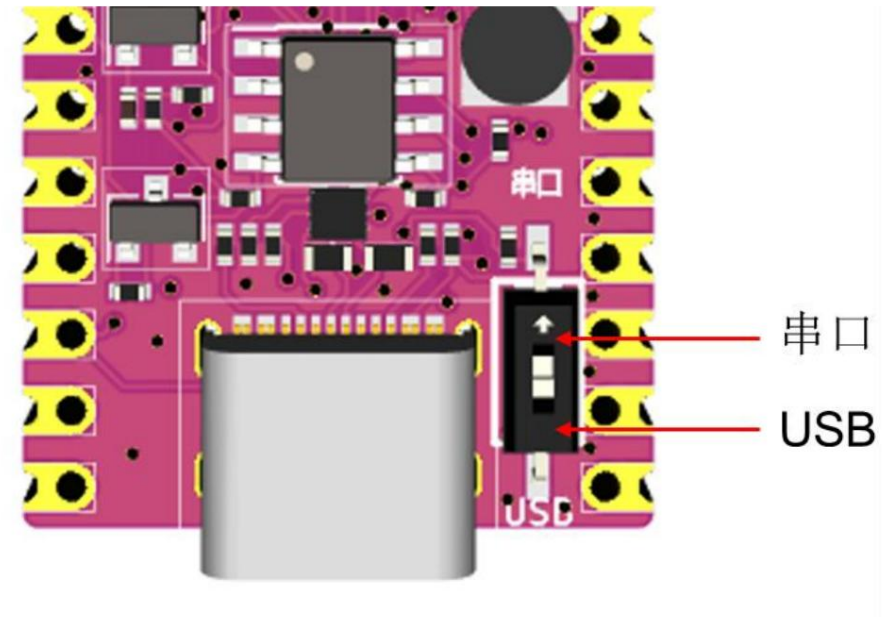


Table 4-1

LED number	Corresponding to GPIO	pin function	describe
D3	PD14	GPIO62 configuration	Active high
D4	PD15	GPIO63 configuration	Active high
D5	PC3	GPIO35 configuration	Active high

USB-serial switch

The Air105 core board supports serial/USB switching, and the two functions can be switched through the DIP switch.



The specific switching functions are:

switch position up	Function
and down	serial port
	USB

Button introduction

There are two buttons on the Air105 core board, among which K1 can realize the download function, K2 can realize the reset function, pin control

Refer to Table 4-2.

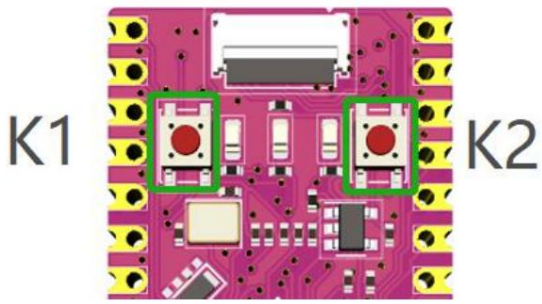


Table 4-2

key number	pin function	describe
When the K1 button is pressed, the chip reset is active at low level		

K2	When the button is pressed, the chip enters Download mode	Active low

Camera

Air105 core board can support up to 30W camera, the interface is 21PIN FPC pin, the PIN pin spacing is 0.3,

The connection with the FPC connector is in the down mode, it is recommended to use WSM-032A-RD63F-C83E, Sensor (GC032A), which can be Zhou Taobao store to buy.

6. PCB

PCB link address: 105-SE BOM (luatos.com)

7. Follow us

LUAT Community: https://doc.openluat.com

Openluat Mall : http://mall.m.openluat.com

Product information: https://luatos.com/t/air105

Official Taobao Store 1: https://openluat.taobao.com

Official Taobao Store 2: https://luat.taobao.com

Official technical support communication WeChat group:

For more information, please scan the QR code to follow the official account of Hezhou, and look forward to your arrival

document name	Air105 Core Board Design Manual
author	Wang Xuefeng
Modified date	2021.12.29
Version	1.1
Inside the document state	

Modification record:

Version number modification record	date	author
V1.0 New	2021-12-05	Wang Xuefeng
V1.1 modification	2021-12-29	Wang Xuefeng