

W806 chip design guide

V1.0

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Table of conten

Document modification record	5
1 Overview7	
2 Pin definition7	
3 Chip peripheral circuit design11	
3.1 RESET reset circuit design11	
3.2 Reference clock circuit design	
3.3 ADC circuit design12	
3.4 WAKEUP circuit design	
3.5 GPIO design13	
3.6 Touch Sensor Design13	
3.7 Download port14	
3.8 Power supply design	
4 Layout Design	



1 Overview

The W806 chip is a secure IoT MCU chip. The chip integrates a 32-bit CPU processor with built-in UART, GPIO, SPI, SDIO,

I 2C, I 2S, PSRAM, 7816, ADC, LCD, TouchSensor and other digital interfaces; supports TEE security engine and multiple hardware processing

Decryption algorithm, built-in DSP, floating point operation unit and security engine, supports code security permission settings, built-in 1MB Flash memory, supports

Firmware encrypted storage, firmware signature, secure debugging, secure upgrade and other security measures ensure product security features. Suitable for small household appliances, smart phones

It can be used in a wide range of IoT fields such as home furnishings, smart toys, industrial control, and medical monitoring

2 pin definition

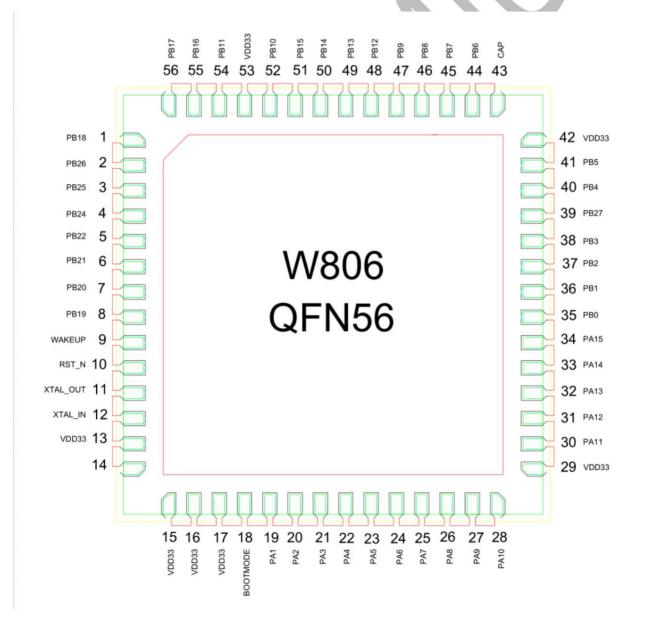




Figure 2-1 Pin layout diagram (QFN56)





Table 2-1 Pin assignment definition (QFN56)

No. Nam	ne Type Pin fund	ction after r	reset	Reuse function	Maximum frequency	pull-down capability	driving capability
1	PB_18	I/O GPI	O, input, high impedance UA	ART5_TX/LCD_SEG30	10MHz	UP/DOWN	12mA
2	PB_26	I/O GPI	O, input, high impedance LS	PI_MOSI/PWM4/LCD_SEG1	20MHz	UP/DOWN	12mA
3	PB_25	I/O GPI	O, input, high impedance LS	PI_MISO/PWM3/LCD_COM0	20MHz	UP/DOWN	12mA
4	PB_24	I/O GPI	O, input, high impedance LS	PI_CK/PWM2/LCD_SEG2	20MHz	UP/DOWN	12mA
5	PB_22	I/O GPI	O, input, high impedance UA	RT0_CTS/PCM_CK/LCD_COM2	10MHz	UP/DOWN	12mA
6	PB_21	I/O GPI	O, input, high impedance U	RT0_RTS/PCM_SYNC/LCD_COM1	10MHz	UP/DOWN	12mA
7	PB_20	I/O UAI	RT_RX	UARTO_RX/PWM1/UART1_CTS/I2C_SCL	10MHz	UP/DOWN	12mA
8	PB_19	I/O UAI	RT_TX	UART0_TX/PWM0/UART1_RTS/I2C_SDA	10MHz	UP/DOWN	12mA
9 WAI	KEUP I WAKEU	JP wake-up	function			DOWN	
10	RESET	IRES	ET reset			UP	
11 XT/	AL_OUT O Exte	rnal crysta	l oscillator output				
12 XT/	AL_IN I Externa	l crystal in	out				
13	VDD33	P chip	power supply, 3.3V				
14	NC						
15	VDD33	P chip	power supply, 3.3V				
16	VDD33	P chip	power supply, 3.3V				
17	VDD33	P chip	power supply, 3.3V				
18 BO	OTMODE I/O B	оотмор	E	I2S_MCLK/LSPI_CS/PWM2/I2S_DO	20MHz	UP/DOWN	12mA
19	PA_1	I/O JTA	G_CK	JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/AD	20MHz	UP/DOWN	12mA
20	PA_2	I/O GPI	O, input, high impedance	UART1_RTS/UART2_TX/PWM0/UART3_RT S/ADC_4	20MHz	UP/DOWN	12mA
lasty at	PA_3	I/O GPI	O, input, high impedance	UART1_CTS/UART2_RX/PWM1/UART3_CT S/ADC_3	20MHz	UP/DOWN	12mA
twelfy two	PA_4	I/O JTA	.g_swo	JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/AD C_2	20MHz	UP/DOWN	12mA
lacety Prize	PA_5	I/O GPI	O, input, high impedance	UART3_TX/UART2_RTS/PWM_BREAK/UAR T4_RTS/VRP_EXT	20MHz	UP/DOWN	12mA
twelly faur	PA_6	I/O GPI	O, input, high impedance	UART3_RX/UART2_CTS/NULL/UART4_CT S/LCD_SEG31/VRP_EXT	20MHz	UP/DOWN	12mA
25	PA_7	I/O GPI	O, input, high impedance	PWM4/LSPI_MOSI/I2S_MCK/I2S_DI/LC D_SEG3/Touch_1	20MHz	UP/DOWN	12mA
26	PA_8	I/O GPI	O, input, high impedance	PWM_BREAK/UART4_TX/UART5_TX/I2S_ BCLK/LCD_SEG4	20MHz	UP/DOWN	12mA



27	PA_9	I/O GPO, input, high impeda	MMC_CLK/UART4_RX/UART5_RX/I2S_LR CLK/LCD_SEG5/TOUCH_2	50MHz	UP/DOWN	12mA
28	PA_10	I/O GP O, input, high impeda	MMC_CMD/UART4_RTS/PWM0/I2S_DO/LC nce D_SEG6/TOUCH_3	50MHz	UP/DOWN	12mA
29	VDD33	P chip power supply, 3.3V	2_2268.166611_3			
30	PA_11	I/O GPIO, input, high impeda	MMC_DAT0/UART4_CTS/PWM1/I2S_DI/L CD_SEG7	50MHz	UP/DOWN	12mA
31	PA_12	I/O GPIO, input, high impeda	MMC_DAT1/UART5_TX/PWM2/LCD_SEG8/ TOUCH_14	50MHz	UP/DOWN	12mA
32	PA_13	I/O GPO, input, high impeda	nce MMC_DAT2/UART5_RX/PWM3/LCD_SEG9	50MHz	UP/DOWN	12mA
33	PA_14	I/O GPIO, input, high impeda	MMC_DAT3/UART5_CTS/PWM4/LCD_SEG1 0/TOUCH_15	50MHz	UP/DOWN	12mA
34	PA_15	I/O GPIO, input, high impeda	PSRAM_CK/UART5_RTS/PWM_BREAK/LCD _SEG11	50MHz	UP/DOWN	12mA
35	PB_0	I/O GPIO, input, high impeda	PWM0/LSPI_MISO/UART3_TX/PSRAM_CK /LCD_SEG12/Touch_4	80MHz	UP/DOWN	12mA
36	PB_1	I/O GPIO, input, high impeda	PWM1/LSPI_CK/UART3_RX/PSRAM_CS/L CD_SEG13/Touch_5	80MHz	UP/DOWN	12mA
37	PB_2	I/O GPIO, input, high impeda	PWM2/LSPI_CK/UART2_TX/PSRAM_D0/L CD_SEG14/Touch_6	80MHz	UP/DOWN	12mA
38	PB_3	I/O GPIO, input, high impeda	PWM3/LSPI_MISO/UART2_RX/PSRAM_D1 /LCD_SEG15/Touch_7	80MHz	UP/DOWN	12mA
39	PB_27	I/O GPIO, input, high impeda	nce P\$RAM_CS/UART0_TX/LCD_COM3	80MHz	UP/DOWN	12mA
40	PB_4	I/O GPIO, input, high impeda	LSPI_CS/UART2_RTS/UART4_TX/PSRAM _D2/LCD_SEG16/Touch_8	80MHz	UP/DOWN	12mA
41	PB_5	I/O GPIO, input, high impeda	LSPI_MOSI/UART2_CTS/UART4_RX/PSA RM_D3/LCD_SEG17/Touch_9	80MHz	UP/DOWN	12mA
42	VDD33	P chip power supply, 3.3V				
43	CAP	I external capacitor, 4.7μF				
44	PB_6	I/O GPIO, input, high impeda	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK /LCD_SEG18/Touch_10	50MHz	UP/DOWN	12mA
45	PB_7	I/O GPIO, input, high impeda	UART1_RX/MMC_CMD/HSPI_INT/SDIO_C MD/LCD_SEG19/Touch_11	50MHz	UP/DOWN	12mA
46	PB_8	I/O GPIO, input, high impeda	I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0 /LCD_SEG20/Touch_12	50MHz	UP/DOWN	12mA
47	PB_9	I/O GPIO, input, high impeda	I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/ LCD_SEG21/Touch_13	50MHz	UP/DOWN	12mA
48	PB_12	I/O GPIO, input, high impeda	HSPI_CK/PWM0/UART5_CTS/I2S_BCLK/ LCD_SEG24	50MHz	UP/DOWN	12mA
49	PB_13	I/O GPIO, input, high impeda	HSPI_INT/PWM1/UART5_RTS/I2S_LRCL K/LCD_SEG25	50MHz	UP/DOWN	12mA



50	PB_14	I/O GP	IO, input, high impedance	HSPI_CS/PWM2/LSPI_CS/I2S_DO/LCD_ SEG26	50MHz	UP/DOWN	12mA
51	PB_15	I/O GP	IO, input, high impedance	HSPI_DI/PWM3/LSPI_CK/I2S_DI/LCD_ SEG27	50MHz	UP/DOWN	12mA
52	PB_10	I/O GP	IO, input, high impedance	I2S_DI/MMC_D2/HSPI_DI/SDIO_D2/LC D_SEG22	50MHz	UP/DOWN	12mA
53	VDD33	P chip	power supply, 3.3V				
54	PB_11	I/O GP	IO, input, high impedance	I2S_DO/MMC_D3/HSPI_DO/SDIO_D3/LC D_SEG23	50MHz	UP/DOWN	12mA
55	PB_16	I/O GP	IO, input, high impedance	HSPI_DO/PWM4/LSPI_MISO/UART1_RX/ LCD_SEG28	50MHz	UP/DOWN	12mA
56	PB_17	I/O GP	IO, input, high impedance	UART5_RX/PWM_BREAK/LSPI_MOSI/I2S _MCLK/LCD_SEG29	20MHz	UP/DOWN	12mA
57 GN	ID P Chip botto	m ground	PAD				

Note: 1. I = input, O = output, P = power

3 Chip peripheral circuit design

3.1 RESET reset circuit design

The reset circuit is recommended to be designed as an RC circuit, with automatic reset after power-on, and W806 low-level reset. If using external control RESET tube

pin, when the level value is lower than 2.0v, the chip is in reset state. During reset, the low level needs to last for more than 100us, see Figure 3-1.

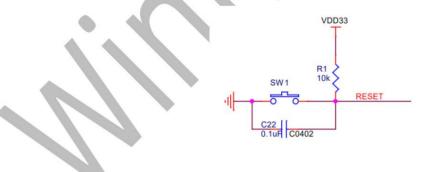


Figure 3-1 Reset circuit

3.2 Reference clock circuit design

The chip reference clock uses a frequency of 40MHz, and customers can choose different temperature levels, stability, and load capacitance values according to actual product requirements.

of crystals. The load capacitance connected at both ends of the crystal needs to be adjusted according to the crystal and frequency offset conditions of different manufacturers. See Figure 3-2 in the reference design.



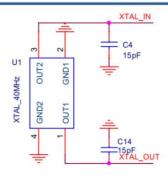


Figure 3-2 Crystal circuit

The crystal should be placed as close to the chip as possible, the traces should be as short as possible, and away from interference sources. There should be multiple ground holes around the clock for isolation. The layers below the clock are prohibited from

It is routed through to prevent interference with the clock source

3.3 ADC circuit design

Pins 19-21 of the chip can be used as an ordinary ADC, with an input voltage range of 0-2.4V. When it is higher than 2.4V, external voltage division processing is required before

Can enter the ADC interface. To improve accuracy, high-precision resistors are required for R1 and R2. Select the appropriate R1 and R2 according to the Sensor output voltage value

Resistor value divider. As shown in Figure 3-3.

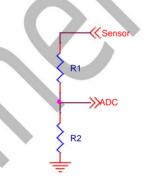


Figure 3-3 ADC voltage dividing circuit

3.4 WAKEUP circuit design

After the chip enters the sleep state, the WAKEUP function can be used to wake up the chip. The WAKEUP pin inputs a high level to wake up the chip in the sleep state.

chip. When the chip is in normal working condition, the WAKEUP pin is low level and can pull down the 10K resistor.

Note that if the WAKEUP function is not used, this pin can be left floating or pulled down, but cannot be pulled up.



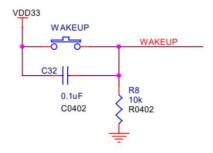


Figure 3-4 WAKEUP circuit

3.5 GPIO design

After the chip is powered on, pins 7 and 8 default to the UART0 port, which provides download and AT command ports and log output ports. Customer use

Be careful not to use this port as GPIO at will to prevent it from being occupied and unable to download and debug. After the system is up, the port can be restored

Used for other ports. If the port is occupied, you can follow Chapter 3.7.

Table 3-2 Chip UART0 pin description

7	PB20	I/O	UARTO_RX
8	PB19	1/0	UART0_TX

The multiplexing relationship and usage of the remaining pins are shown in Table 2-1. For all GPIOs, if the chip is internally configured as pull-up, the typical pull-up resistor value is 40K.

If configured as a pull-down, the typical pull-down resistor value is 49K.

3.6 Touch Sensor Design

W806 integrates 15 Touch Sensors internally. See Table 2-1 for detailed pin definitions. When designing, attention should be paid to the parasitic effects of wiring and external circuits.

The influence of capacitance, the size of parasitic capacitance directly affects the sensitivity of Touch Sensor.

Figure 3-6 is a schematic diagram of the touch capacitance distribution, where Cground is the capacitance between the touch circuit reference ground and the earth, and Ccomponet is

The parasitic capacitance inside the chip, the parasitic capacitance between the Ctrace trace and the circuit reference ground, the parasitic capacitance between the Celectrode touch electrode and the circuit reference ground.

The parasitic capacitance, Ctouch is the capacitance formed by the finger and the touch electrode relative to the ground.

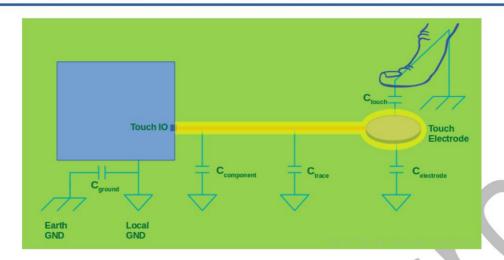


Figure 3-6 Schematic diagram of touch canacitance distribution

Parasitic capacitance Cp (that is, the capacitance when no touch action occurs) = Ccomponet + Ctrace + Celectrode. When a touch action occurs,

The change in the total capacitance of the system \bar{y} C=Ctouch, the common Ctouch is about 5pF~15pF. When the parasitic capacitance Cp is smaller and Ctouch is larger,

The easier the touch action is to be detected by the system, that is, the higher the sensitivity of the touch sensing system. When using this part of the function, you need to refer to

Related content of the "touch_sensor Software and Hardware Design Guide v1.0" document.

3.7 Download port

The W806 chip defaults to UART0 as the download port. When the chip does not have firmware for initial download, directly connect to the UART0 interface and use the relevant download software.

Download the firmware via the file. When there is firmware in the chip and you enter the download mode again, you can pull down BOOTMODE and then power on to enter the download mode.

load mode. After the download is completed, remove the BOOTMODE pull-down operation and need to restart before the firmware can run.

3.8 Power supply design

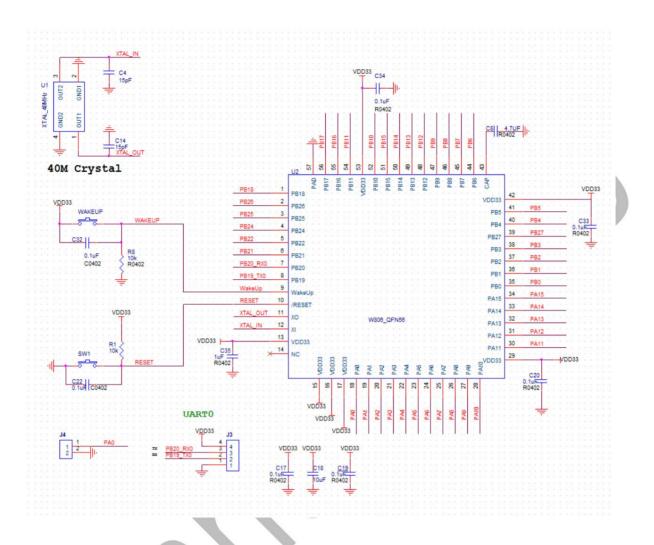
Chip power supply voltage: 3.3V, normal working power supply range: 3.0V-3.6V. Do not exceed this range. Exceeding 3.6V may cause damage to the chip.

Permanent damage, below 3.0V, the overall performance may be reduced, the total current is recommended to be above 500mA. Each power input pin of the chip should be placed accordingly

filter capacitor.



3.9 Reference design schematic diagram



4 Layout design

The middle PAD of the W806 chip is the heat dissipation pad, which needs to be grounded. At the same time, it needs to be drilled to have good contact with the ground for heat dissipation. The middle belly

Do not use window openings for vias. As shown in Figure 4-1.

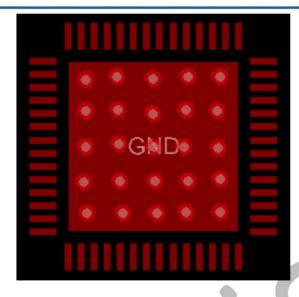


Figure 4-1 Ground pad processing