Air103 MCU Design Manual

Document name	Air103 MCU Design Manual
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Modification date	2021.11.23
Version	1.2
Document status	internal

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Modification record:

Version number modification record	date	author
V1.0 new	2021-10-25	wuzhuangzhuang
V1.1 corrects the pin location of uart4/uart5	2021-11-16	Wendal
V1.2 updates Pinout pin definition and pictures	2021-11-23	wuzhuangzhuang

I. Overview

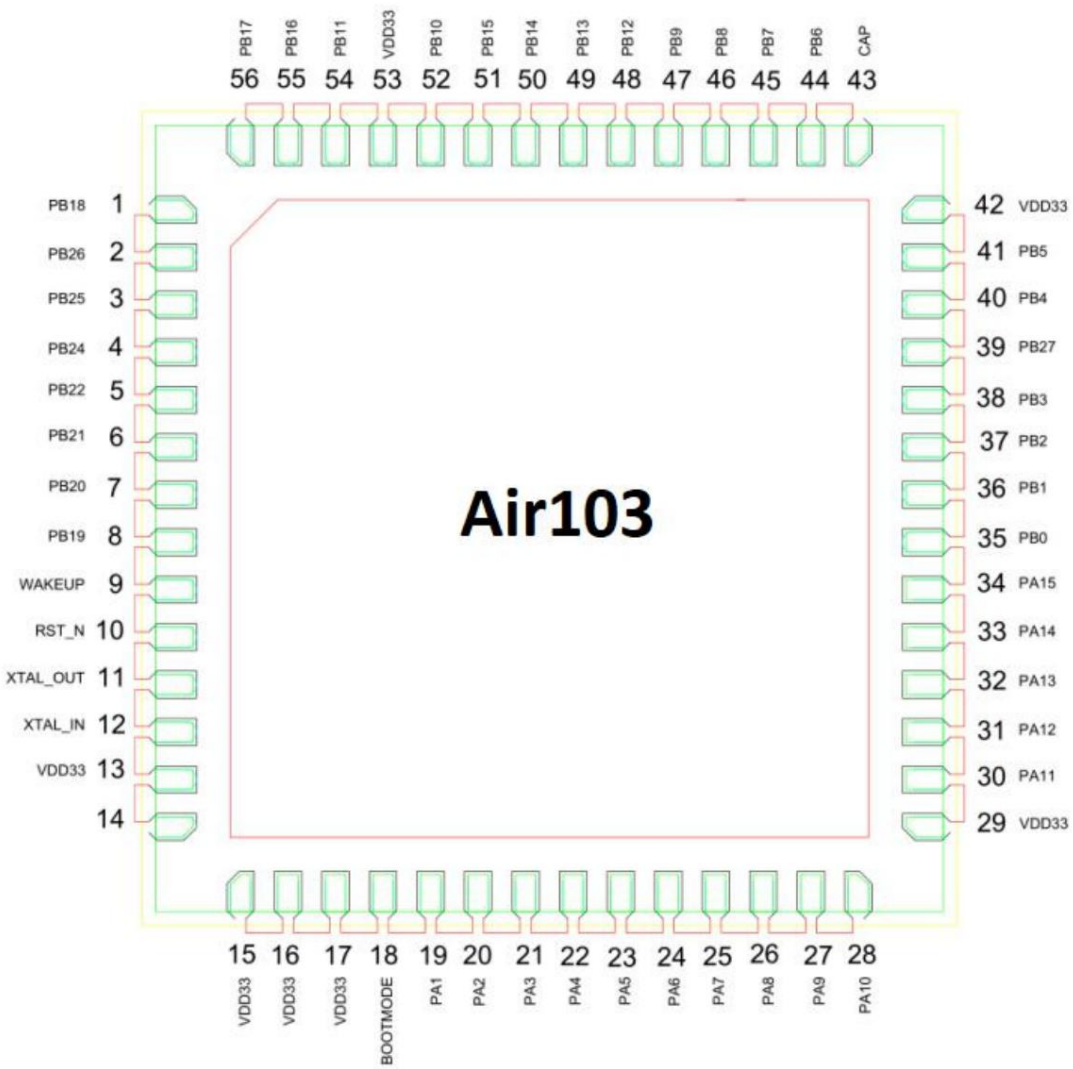
1.1 Product Overview

Air103 is an IOT MCU chip with an integrated 32-bit CPU processor and a QFN-56 package design.

Built-in UART, GPIO, SPI, SDIO, I2C, PSRAM, ADC and other digital interfaces, with 1MB Flash memory

storage. It is suitable for a wide range of IoT fields such as small household appliances, smart homes, smart toys, industrial control, and medical monitoring.

1.2 Pin definition



The following figure shows the pin definition of Air103. If all GPIOs are configured as pull-up inside the chip, the typical pull-up resistor value is 40K, if configured as pull-down, the typical value of the pull-down resistor is 49K.

Note: SPI0 and SPI1 are the same SPI controller, and only one can be selected for use; the naming number of the PWM pin is divided into 2 digits: XY, among which Y is the same PWM pin, only one can be selected and cannot be used at the same time, such as PWM01 and PWM11 They cannot take effect at the same time.

Pin assignment definition							
Pin name configuration mode I/O			Reset after	Highest reusability	frequency	Pull up and down ability	drive ability
1	PB_18	GPIO34	I/O GPIO, input	/	10MHz	UP/DOWN	12mA
			In, high resistance				
2	PB_26	GPIO42	I/O GPIO, input	PWM34	20MHz	UP/DOWN	12mA
			In, high resistance				
3	PB_25	GPIO41	I/O GPIO, input	PWM33	20MHz	UP/DOWN	12mA
			In, high resistance				
4	PB_24	GPIO40	I/O GPIO, input	PWM32	20MHz	UP/DOWN	12mA
			In, high resistance				
5	PB_22	GPIO38	I/O GPIO, input	/	10MHz	UP/DOWN	12mA
			In, high resistance				
6	PB_21	GPIO37	I/O GPIO, input	/	10MHz	UP/DOWN	12mA
			In, high resistance				
7	PB_20	/	I/O UART_RX	UART0_RX	10MHz	UP/DOWN	12mA
8	PB_19	/	I/O UART_TX	UART0_TX	10MHz	UP/DOWN	12mA
9	WAKEUP		I Wake-up function	/		DOWN	
10	RESET		I RESET complex Bit	/		UP	
11	XTAL_OUT		O External crystal oscillator output	/			
12	XTAL_IN		I external crystal oscillator enter	/			
13	VDD33		P chip power Source, 3.3V	/			
14	NC			/			
15	VDD33		P chip power Source, 3.3V	/			
16	VDD33		P chip power Source, 3.3V	/			
17	VDD33		P chip power Source, 3.3V	/			

18	BOOTMODE		I/O	BOOTMODE	/	20MHz UP/DOWN 12mA
19	PA_1	GPIO01	I/O	GPIO, input In, high resistance	I2C_SCL/ADC_0	20MHz UP/DOWN 12mA
20	PA_2	GPIO02	I/O	GPIO, input In, high resistance	ADC_3/PWM30	20MHz UP/DOWN 12mA
twenty one	PA_3	GPIO03	I/O	GPIO, input In, high resistance	ADC_2/PWM31	20MHz UP/DOWN 12mA
twenty two	PA_4	GPIO04	I/O	GPIO, input In, high resistance	I2C_SDA/ADC_1	20MHz UP/DOWN 12mA
twenty three	PA_5	GPIO05	I/O	GPIO, input In, high resistance	/	20MHz UP/DOWN 12mA
twenty four	PA_6	GPIO06	I/O	GPIO, input In, high resistance	/	20MHz UP/DOWN 12mA
25	PA_7	GPIO07	I/O	GPIO, input In, high resistance	PWM04	20MHz UP/DOWN 12mA
26	PA_8	GPIO08	I/O	GPIO, input In, high resistance	/	20MHz UP/DOWN 12mA
27	PA_9	GPIO09	I/O	GPIO, input In, high resistance	/	50MHz UP/DOWN 12mA
28	PA_10	GPIO10	I/O	GPIO, input In, high resistance	PWM10	50MHz UP/DOWN 12mA
29	VDD33		P	chip power Source, 3.3V		
30	PA_11	GPIO11	I/O	GPIO, input In, high resistance	PWM11	50MHz UP/DOWN 12mA
31	PA_12	GPIO12	I/O	GPIO, input In, high resistance	UART5_TX/PWM12	50MHz UP/DOWN 12mA
32	PA_13	GPIO13	I/O	GPIO, input In, high resistance	UART5_RX/PWM13	50MHz UP/DOWN 12mA
33	PA_14	GPIO14	I/O	GPIO, input In, high resistance	PWM14	50MHz UP/DOWN 12mA
34	PA_15	GPIO15	I/O	GPIO, input In, high resistance	PSRAM_CK	50MHz UP/DOWN 12mA
35	PB_0	GPIO16	I/O	GPIO, input In, high resistance	PWM00/UART3_TX	80MHz UP/DOWN 12mA
36	PB_1	GPIO17	I/O	GPIO, input In, high resistance	PWM01/UART3_RX	80MHz UP/DOWN 12mA
37	PB_2	GPIO18	I/O	GPIO, input In, high resistance	PWM02/SPI0_CK/ U2_TX/PSRAM_D0	80MHz UP/DOWN 12mA
38	PB_3	GPIO19	I/O	GPIO, input In, high resistance	PWM03/SPI0_MIS O/UART2_RX/PSR AM_D1	80MHz UP/DOWN 12mA
39	PB_27	GPIO43	I/O	GPIO, input	PSRAM_CS	80MHz UP/DOWN 12mA

			In, high resistance				
40	PB_4	GPIO20 I/O GPIO, input	In, high resistance	UART4_TX/SPI0_ CS/PSRAM_D2	80MHz UP/DOWN 12mA		
41	PB_5	GPIO21 I/O GPIO, input	In, high resistance	UART4_RX/SPI0_ MOSI/PSA RM_D3	80MHz UP/DOWN 12mA		
42	VDD33		P chip power Source, 3.3V	-			
43	CAP		I external power supply Capacitor, 4.7μF	-			
44	PB_6	GPIO22 I/O GPIO, input	In, high resistance	UART1_TX/SDIO_ CK	50MHz UP/DOWN 12mA		
45	PB_7	GPIO23 I/O GPIO, input	In, high resistance	UART1_RX/SDIO_ CMD	50MHz UP/DOWN 12mA		
46	PB_8	GPIO24 I/O GPIO, input	In, high resistance	SDIO_D0	50MHz UP/DOWN 12mA		
47	PB_9	GPIO25 I/O GPIO, input	In, high resistance	SDIO_D1	50MHz UP/DOWN 12mA		
48	PB_12	GPIO28 I/O GPIO, input	Input, high impedance	PWM20	50MHz UP/DOWN 12mA		
49	PB_13	GPIO29 I/O GPIO, input	In, high resistance	PWM21	50MHz UP/DOWN 12mA		
50	PB_14	GPIO30 I/O GPIO, input	In, high resistance	SPI1_CS/PWM22 50MHz UP/DOWN 12mA			
51	PB_15	GPIO31 I/O GPIO, input	In, high resistance	SPI1_CK/PWM23 50MHz UP/DOWN 12mA			
52	PB_10	GPIO26 I/O GPIO, input	In, high resistance	SDIO_D2	50MHz UP/DOWN 12mA		
53	VDD33		P chip power Source, 3.3V	/			
54	PB_11	GPIO27 I/O GPIO, input	In, high resistance	SDIO_D3	50MHz UP/DOWN 12mA		
55	PB_16	GPIO32 I/O GPIO, input	In, high resistance	PWM24/SPI1_MIS O	50MHz UP/DOWN 12mA		
56	PB_17	GPIO33 I/O GPIO, input	In, high resistance	SPI1_MOSI	20MHz UP/DOWN 12mA		
57	GND		P chip bottom Ground PAD	/			

合宙Air103芯片PinOut示意图

- V3.21112201 -

注意：
- SPI0与SPI1是同一个SPI控制器，仅能选一种使用；
- PWM脚的命名数字分2位：XY，其中Y相同的PWM脚，只能选取一个，不能同时使用，例如PWM01与PWM11不能同时生效。

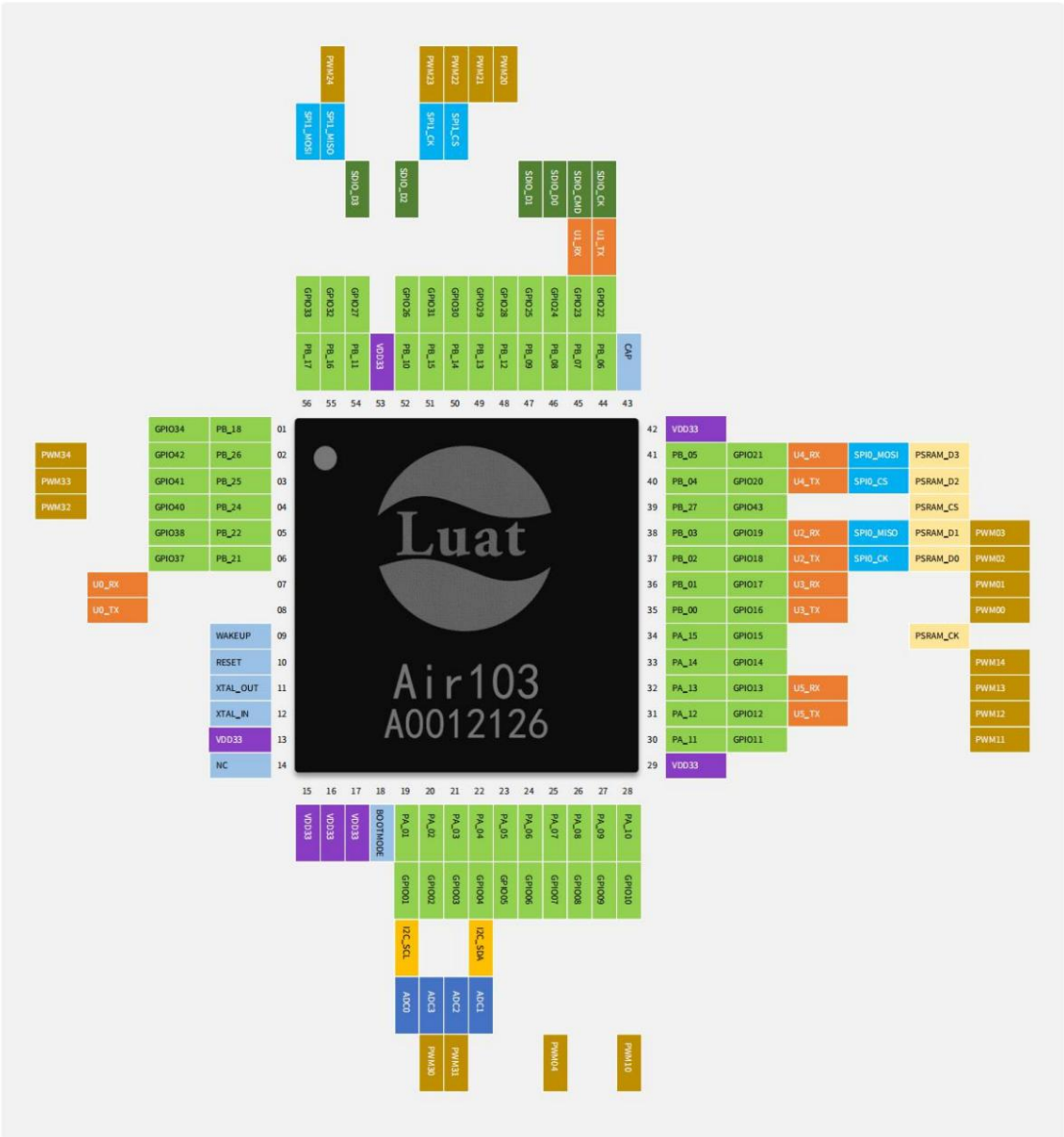


图 例 说 明

供电	特殊引脚	GPIO	UART	PSRAM
I2C	SPI	PWM	ADC	SDIO

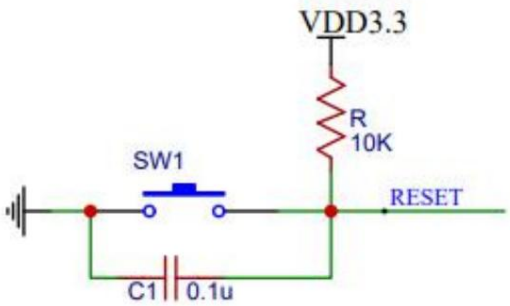
Powered by LuatOS

2. Peripheral circuit design

2.1Reset circuit

The reset circuit is recommended to be designed as an RC circuit, which automatically resets when powered on, and when the button is pressed at the same time, it is a low-level reset. When the level

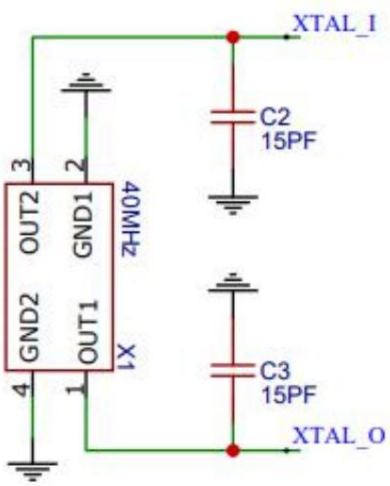
When the value is lower than 2.0v, the chip is in reset state. During reset, the low level needs to last for more than 100us.



2.2 Clock circuit

The reference clock uses a frequency of 40MHz, and different temperature levels, stability, and load currents are selected according to actual product requirements.

capacitance crystal. The load capacitance connected at both ends of the crystal needs to be adjusted according to the crystal and frequency offset conditions of different manufacturers.



The crystal should be placed as close to the chip as possible, the traces should be as short as possible, and away from interference sources. There should be multiple ground holes around the clock for isolation. under the clock

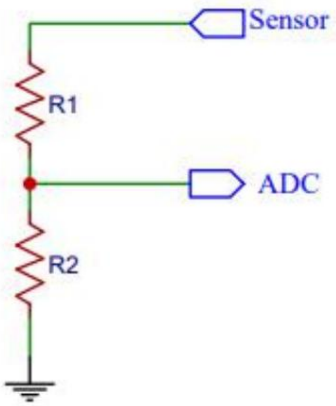
It is forbidden for other traces to pass through each layer of the surface to prevent interference with the clock source.

2.3 ADC circuit

Pins 19~21 of the Air103 chip can be used as an ordinary ADC, with an input voltage range of 0~2.4V. when higher than

At 2.4V, the external voltage needs to be divided before entering the ADC interface. To improve accuracy, R1 and R2 need to use high-precision

resistance. Select the appropriate resistance values of R1 and R2 according to the Sensor voltage.

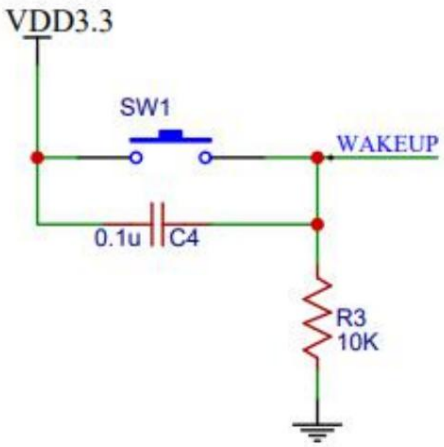


2.4 WAKEUP circuit

After the Air103 chip enters sleep state, you can use the WAKEUP function to wake up the chip. In normal working state,

The WAKEUP pin is low level, and this pin can wake up the chip by inputting a high level when the chip is in sleep mode.

Note that if the WAKEUP function is not used, this pin can be left floating or pulled down, but cannot be pulled up.



2.5 download port

After the Air103 chip is powered on, pins 7 and 8 are fixed as UART0 ports, which provide download and log output ports.

7	PB20	I/O	UART0_RX
8	PB19	I/O	UART0_TX

Chip UART0 pin description

Note: When there is no firmware inside the chip for the first download, directly connect to the UART0 interface to download the firmware.

When there is firmware inside, you can still flash the phone by starting the flash software and then resetting the module. You can also pull down BOOTMODE.

After powering on again, it is forced to enter the download mode. After reset, BOOTMODE can be released. There is no need to continue to pull it low during the download process.

BOOTMODE, the firmware can run only after restarting.

2.6 IIC circuit

Air103 chip supports 1-way IIC interface, which can realize interaction with IIC devices. The voltage domain is 3.3V. It is branded with Bosch

Taking the BMA250E acceleration sensor as an example, the pin control table is 2-1.

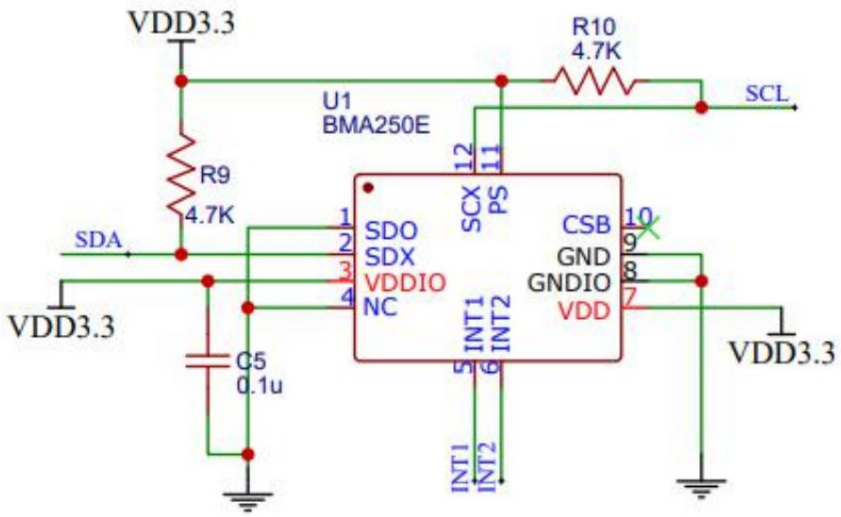


table 2-1

IIC pin number corresponds to GPIO configuration mode			Pin function	describe
SCL	PA_01	GPIO01	IIC device clock pin	3.3V voltage domain
SDA	PA_04	GPIO04	IIC device data pin	3.3V voltage domain

2.7 SPI circuit

The Air103 chip has 1 SPI interface, but supports mapping to different pin combinations. It should be noted that only

Configure one of the channels for communication. Voltage domain 3.3V, taking Winbond brand W25Q128 FIASH as an example, pin control table

2-2.

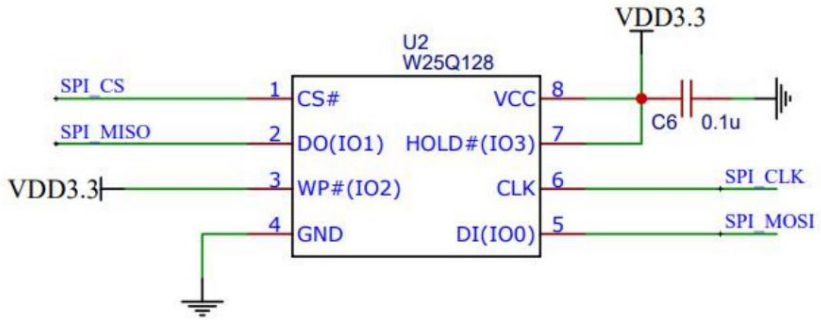


Table 2-2

SPI pin number corresponds to GPIO configuration mode			Pin function	describe
SPI0_CS	PB_04	GPIO20	SPI chip select pin	3.3V voltage domain
SPI0_CLK	PB_02	GPIO18	SPI clock pin	3.3V voltage domain
SPI0_MISO	PB_03	GPIO19	SPI data input	3.3V voltage domain
SPI0_MOSI	PB_05	GPIO21	SPI data output	3.3V voltage domain
SPI1_CS	PB_14	GPIO30	SPI chip select pin	3.3V voltage domain
SPI1_CLK	PB_15	GPIO31	SPI clock pin	3.3V voltage domain
SPI1_MISO	PB_16	GPIO32	SPI data input	3.3V voltage domain
SPI1_MOSI	PB_17	GPIO33	SPI data output	3.3V voltage domain

2.8 SDIO circuit

The Air103 chip supports 1 SDIO interface with a voltage domain of 3.3V. The connection method is as follows, and the pin control table is 2-3.

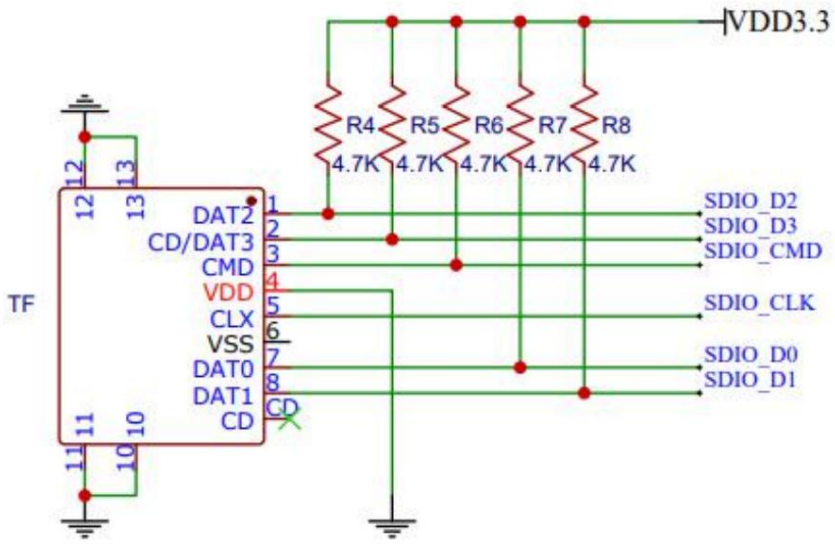


Table 2-3

SDIO pin serial number	Corresponding to GPIO configuration method		Pin function	describe
SDIO_CMD	PB_07	GPIO23	SDIO device chip select pin 3.3V voltage domain	
SDIO_CLK	PB_06	GPIO22	SDIO device clock pin 3.3V voltage domain	
SDIO_D0	PB_08	GPIO24	SDIO device data 0 3.3V voltage domain	
SDIO_D1	PB_09	GPIO25	SDIO device data 1 3.3V voltage domain	
SDIO_D2	PB_10	GPIO26	SDIO device data 2 3.3V voltage domain	
SDIO_D3	PB_11	GPIO27	SDIO device data 3 3.3V voltage domain	

2.9 PSRAM circuit

The Air103 chip supports 1 PSRAM interface with a voltage domain of 3.3V. Taking the LY68L6400SLIT model as an example, the tube

Foot control table 2-4.

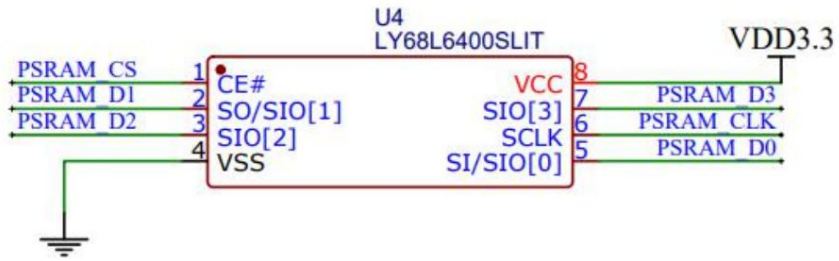


Table 2-4

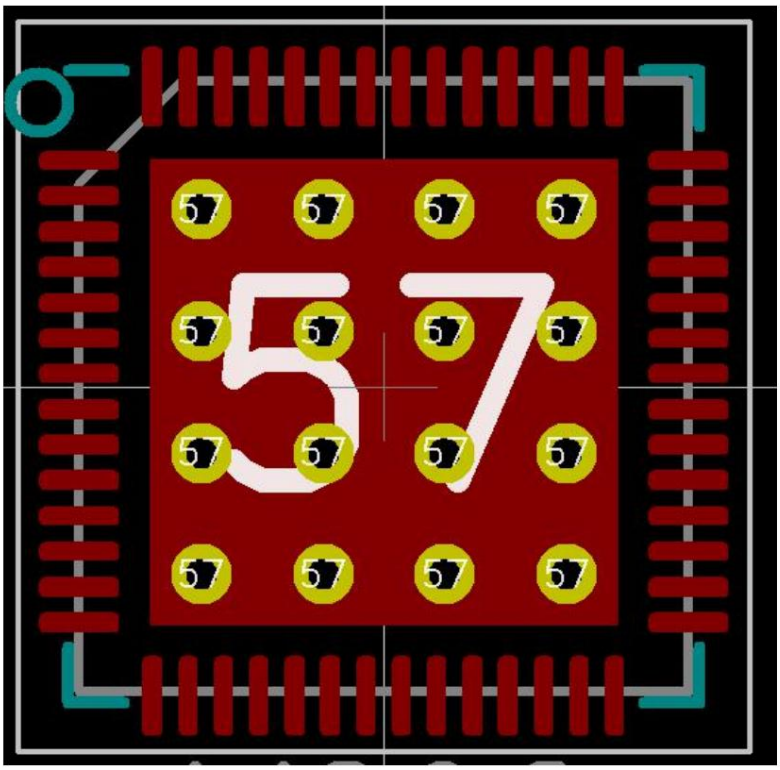
SDIO pin serial number	Corresponding to GPIO configuration method		Pin function	describe
PSRAM_CS	PB_27	GPIO43	PSRAM device chip select pin 3.3V voltage domain	

PSRAM_D0	PB_02	GPIO18	PSRAM device data 0	3.3V voltage domain
PSRAM_D1	PB_03	GPIO19	PSRAM device data 1	3.3V voltage domain
PSRAM_D2	PB_04	GPIO20	PSRAM device data 2	3.3V voltage domain
PSRAM_D3	PB_05	GPIO21	PSRAM device data 3	3.3V voltage domain
PSRAM_CLK	PA_15	GPIO15	PSRAM device clock pin 3.3V voltage domain	

2.10 Ground **PAD** design

The PAD in the middle of the Air103 chip is the heat dissipation pad, which needs to be grounded. At the same time, holes need to be drilled to maintain good grounding.

Do not use window openings for vias.

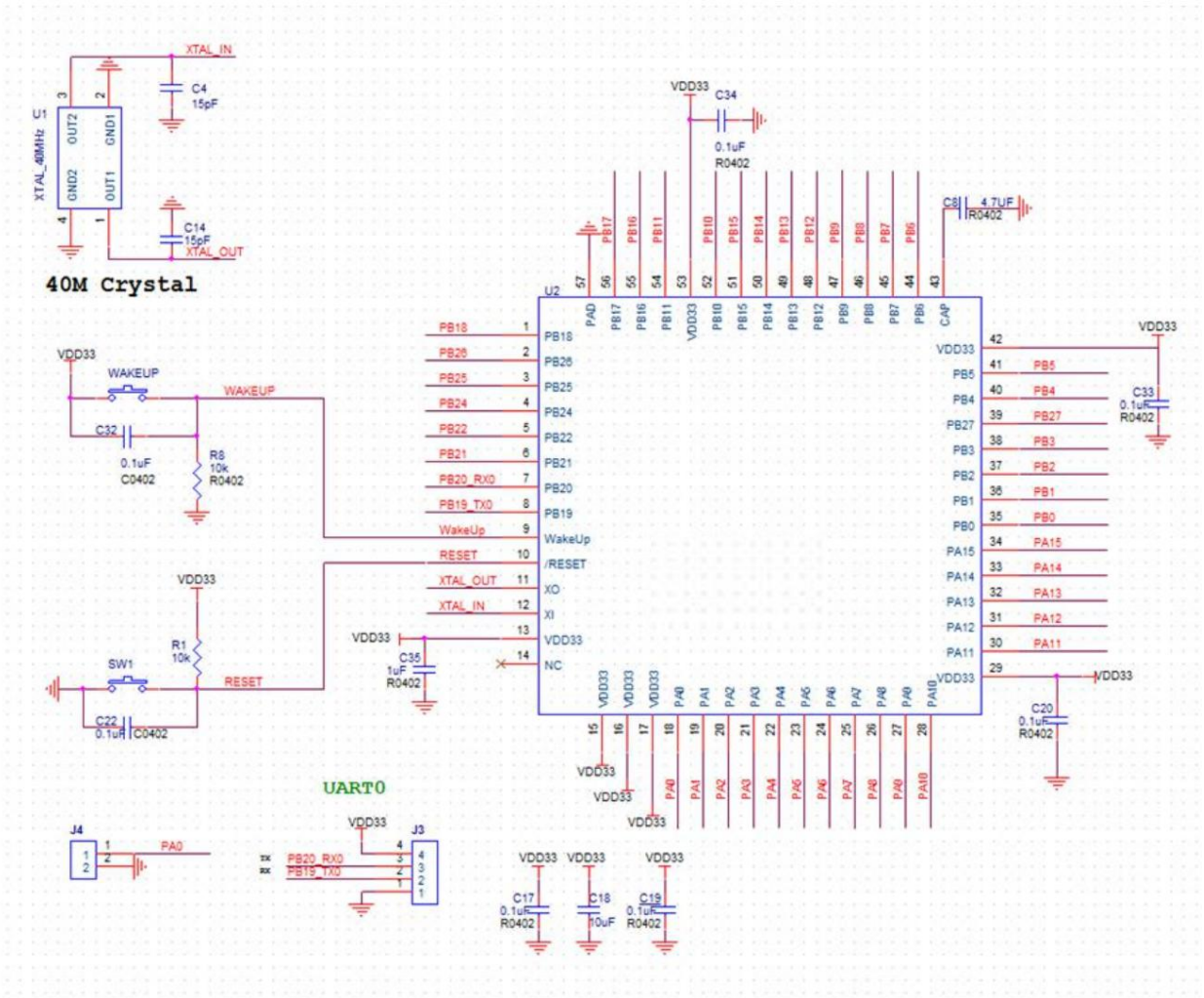


3. Reference circuit design

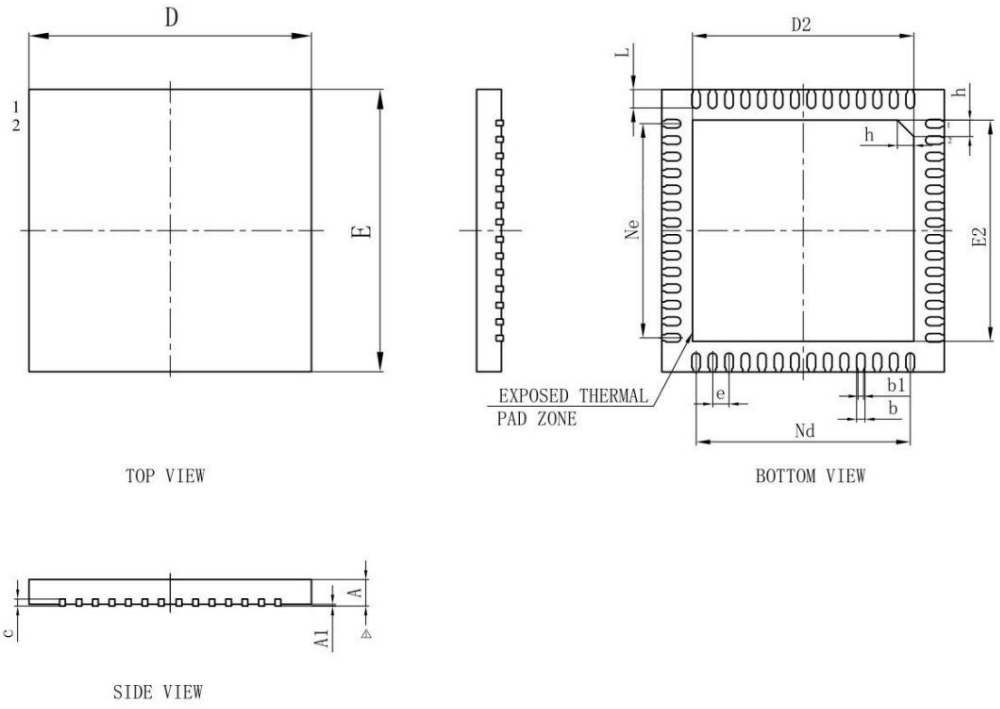
The power supply voltage of Air103 chip is 3.3V. The normal working power supply range is: 3.0V~3.6V. Please note that it may be lower than 3.0V.

The overall performance will decrease, and the total current is recommended to be above 500mA. Each power input pin of the chip (VDD33) except pin 13

In addition to the need to place corresponding filter capacitors, developers can select filter capacitors for other power input pins according to actual needs.



4. Package size



Parameter comparison table

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.60	4.70	4.80
e	0.35BSC		
Ne	4.55BSC		
Nd	4.55BSC		
E	5.90	6.00	6.10
E2	4.60	4.70	4.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F carrier size	193x193		

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