

Sequential Logic Design

Lecture 7

Beneath the Abstraction

Supply Voltage:

V_{DD} has dropped from 5 V to 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V

Logic Levels:

Mapping of a continuous variable onto a discrete binary variable

Noise Margin:

The amount of noise that could be added to a worst-case output such that the signal can still be interpreted as a valid input.

choose $V_{OL} < V_{IL}$ and $V_{OH} > V_{IH}$

Low and High Noise Margins

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

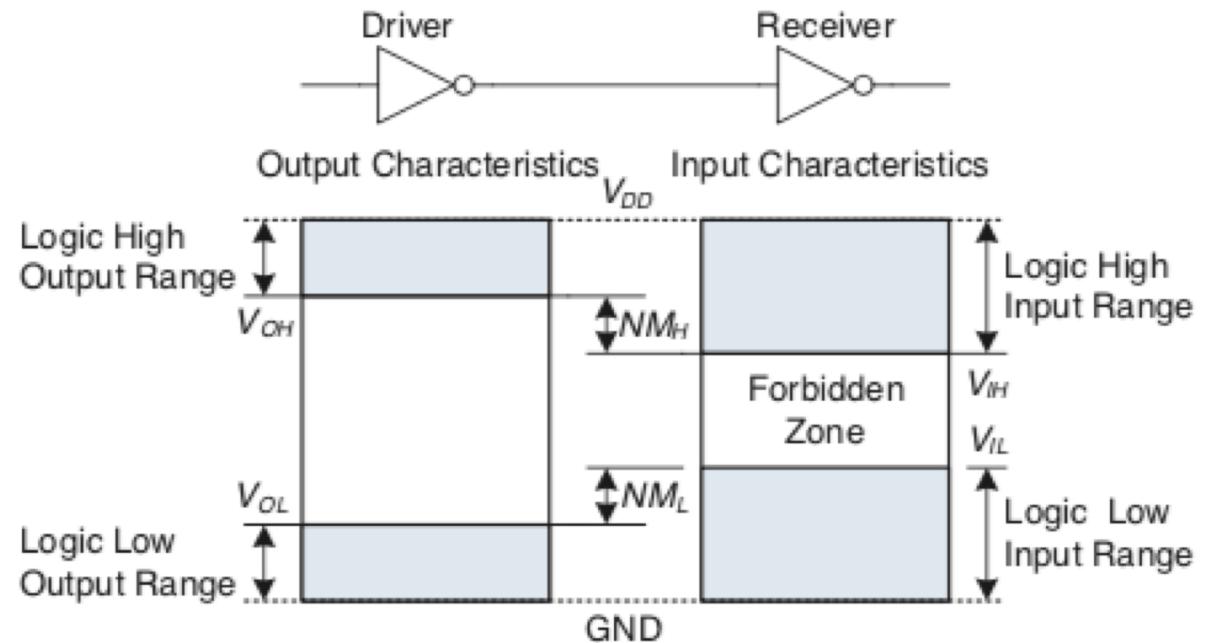
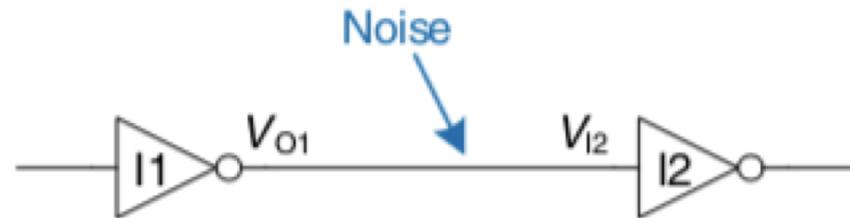


Figure 1.23 Logic levels and noise margins

Example

Consider the inverter circuit:



Both inverters have the following characteristics:

$V_{DD}=5V$, $V_{IL}=1.35V$, $V_{IH} =3.15V$, $V_{OL} =0.33V$, and $V_{OH} =3.84V$.

Can the circuit tolerate 1 V of noise between VO_1 and VI_2 ?

Example (Solution)

The inverter noise margins are:

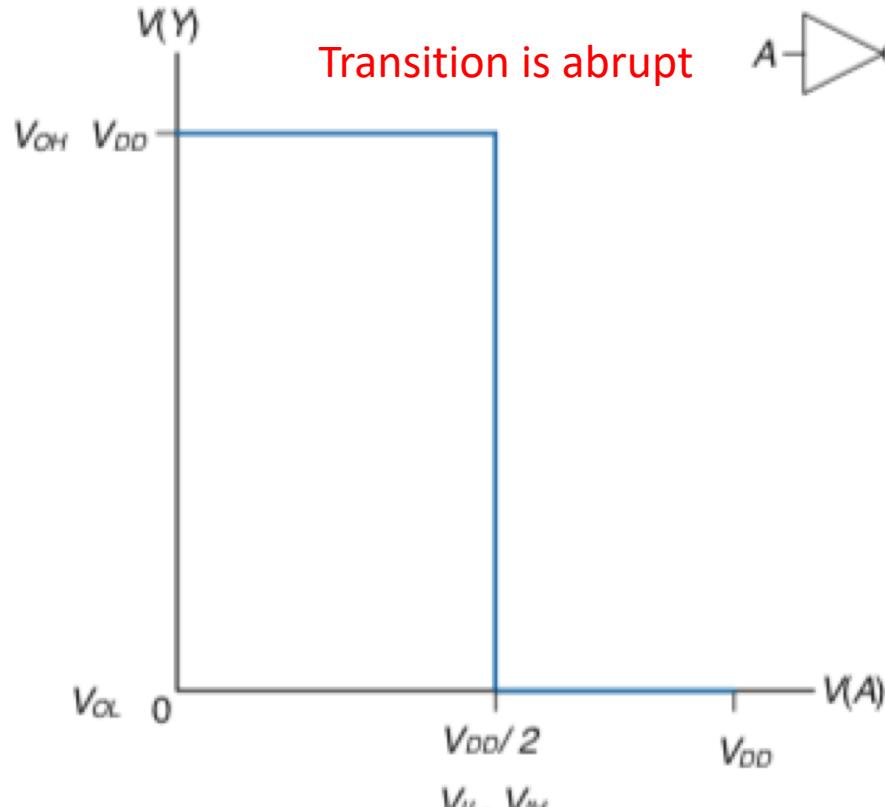
$$NM_L = V_{IL} - V_{OL} = (1.35 \text{ V} - 0.33 \text{ V}) = 1.02 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = (3.84 \text{ V} - 3.15 \text{ V}) = 0.69 \text{ V}.$$

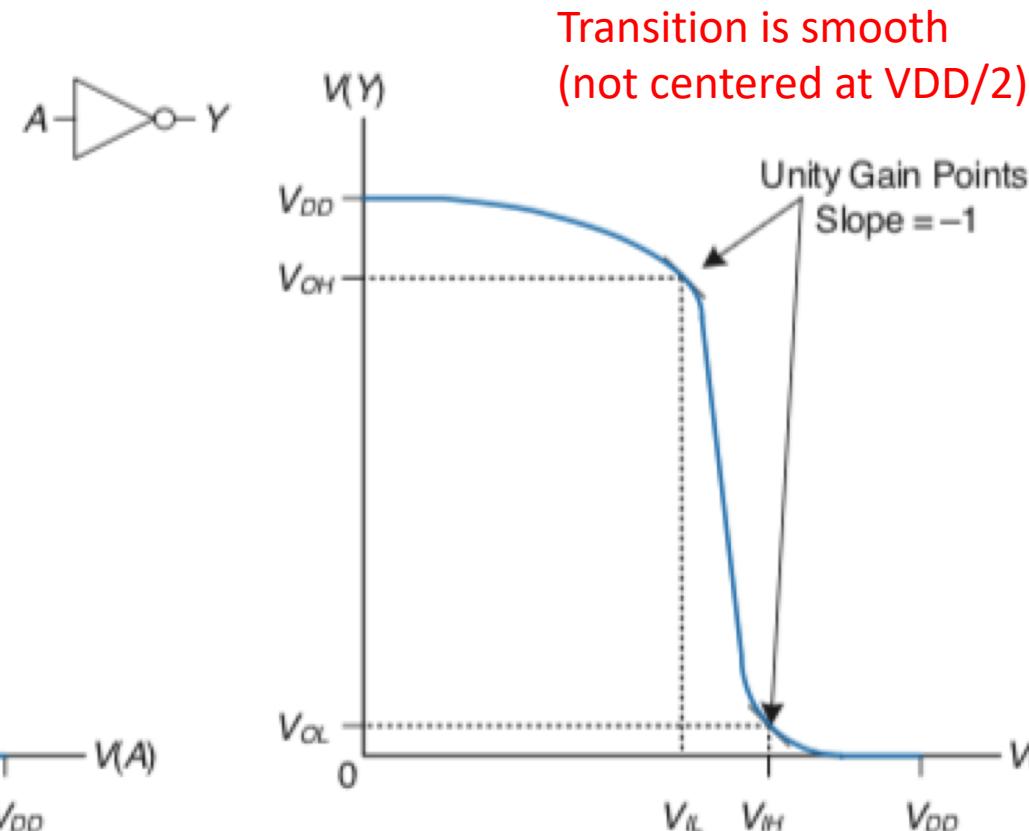
The circuit can tolerate 1 V of noise when the output is **LOW** but **not** when the output is **HIGH**.

DC Transfer Characteristics

Relationship Between Input and Output Voltages



(a) Ideal Inverter



(b) Real Inverter

Figure 1.25 DC transfer characteristics and logic levels

Choosing logic levels at the **unity gain points** usually maximizes the noise margins, that is where the slope of the transfer characteristic $dV(Y)/dV(A) = -1$

Static Discipline

To avoid inputs falling into the forbidden zone, digital logic gates are designed to conform to the **static discipline**, that is, given logically valid inputs, every circuit element will produce logically valid outputs.

Tradeoff

Simplicity and **robustness** at the expense of **freedom** of using arbitrary analog circuit elements.

All gates that communicate must have compatible logic levels.

Gates are grouped into four major **logic families**

Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75–5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5–6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3–3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3–3.6)	0.9	1.8	0.36	2.7

Table 1.5 Compatibility of logic families

		Receiver			
		TTL	CMOS	LVTTL	LVCMOS
Driver	TTL	OK	NO: $V_{OH} < V_{IH}$	MAYBE ^a	MAYBE ^a
	CMOS	OK	OK	MAYBE ^a	MAYBE ^a
	LVTTL	OK	NO: $V_{OH} < V_{IH}$	OK	OK
	LVCMOS	OK	NO: $V_{OH} < V_{IH}$	OK	OK

^a As long as a 5 V HIGH level does not damage the receiver input.

Timing

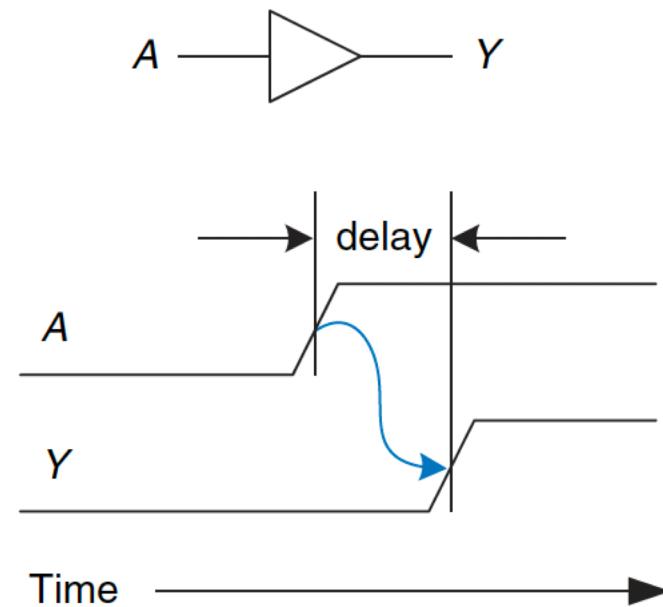
- Propagation and Contamination Delay
- Glitches

Delay

An output takes time to change in response to an input change.

- measured from the 50% point of the input signal, A , to the 50% point of the output signal, Y

Consider the timing diagram showing the transient response of a buffer



Propagation and Contamination

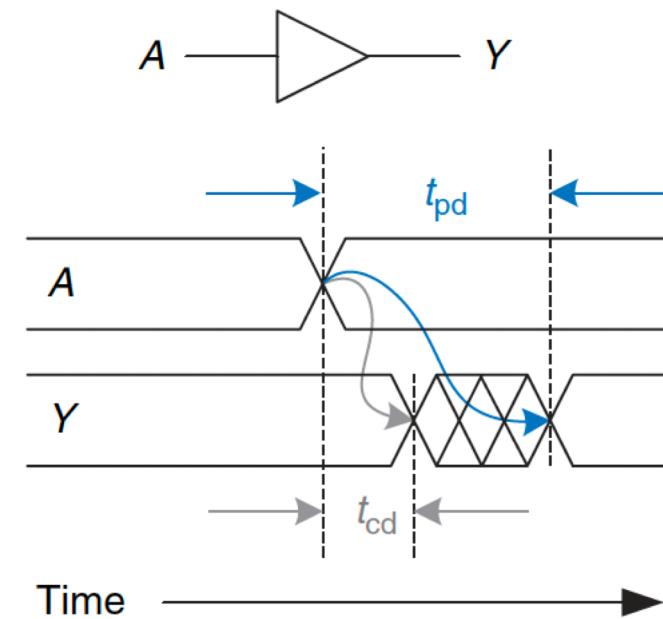
Combinational logic is characterized by:

Propagation delay (t_{pd})

The maximum time from when an input changes until the output or outputs reach their final value.

Contamination delay (t_{cd})

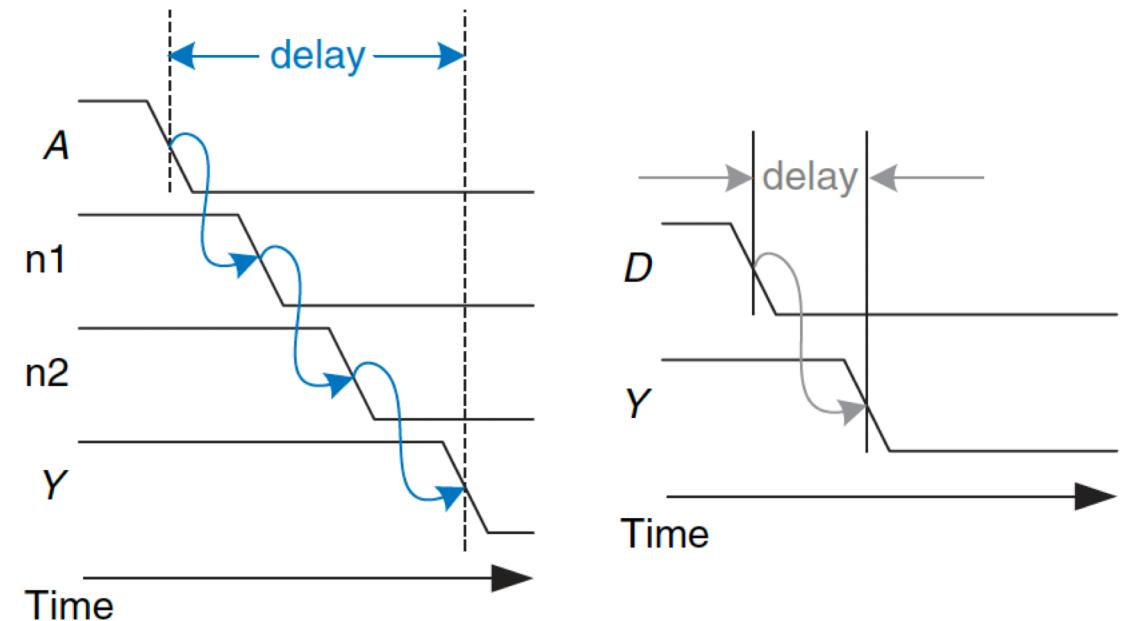
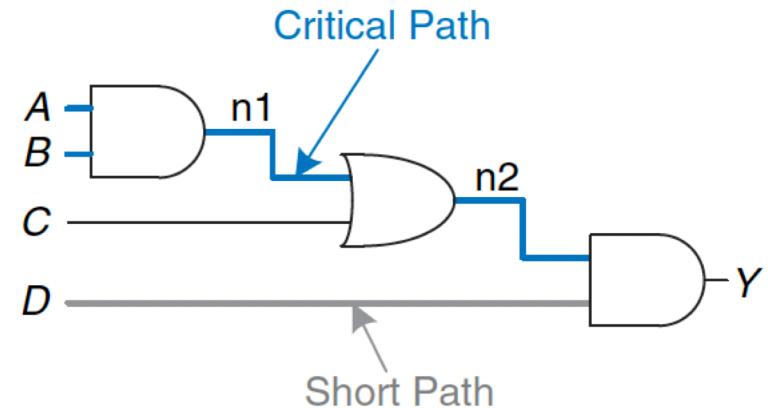
The minimum time from when an input changes until any output starts to change its value.



Delay Determination

Propagation and contamination delays are determined by the **path** a signal takes from input to output.

- The propagation delay of a combinational circuit is the **sum of the propagation delays** through each element on the **critical path**.
- The contamination delay is the **sum of the contamination delays** through each element on the **short path**.



$$t_{pd} = 2t_{pd_AND} + t_{pd_OR}$$

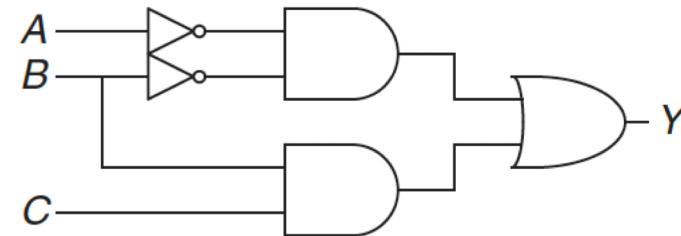
$$t_{cd} = t_{cd_AND}$$

Glitches

It is possible that a single input transition can cause multiple output transitions.

Example

When $A = 0$, $C = 1$, and
 B transitions from 1 to 0

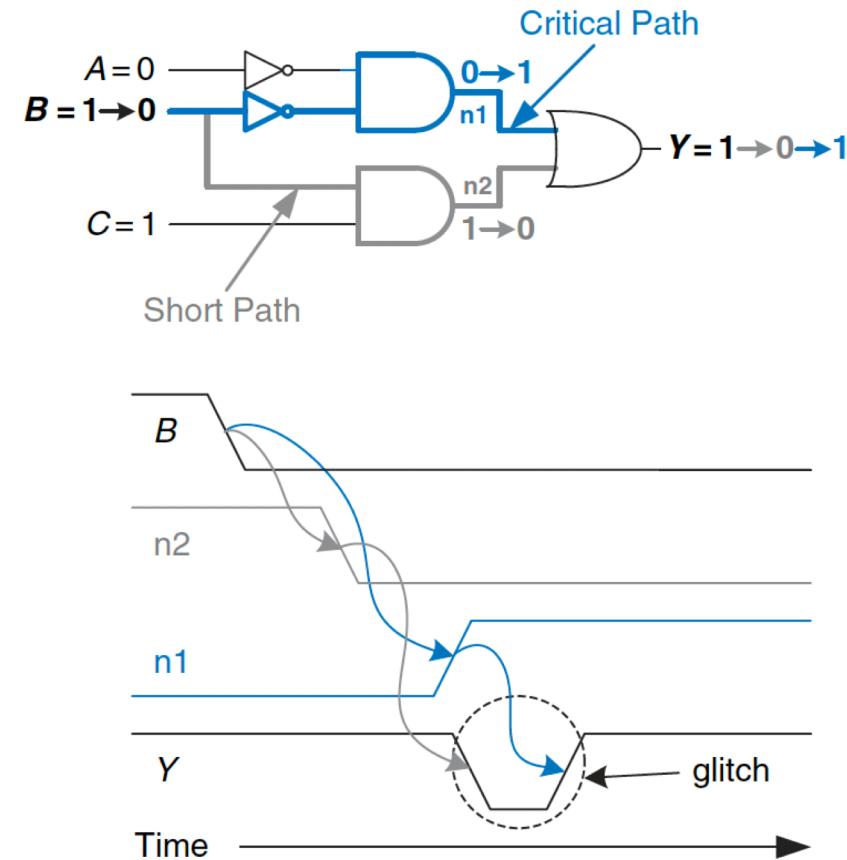


	AB	00	01	11	10
C	0	1	0	0	0
	1	1	1	1	0

$$Y = \overline{A}\overline{B} + BC$$

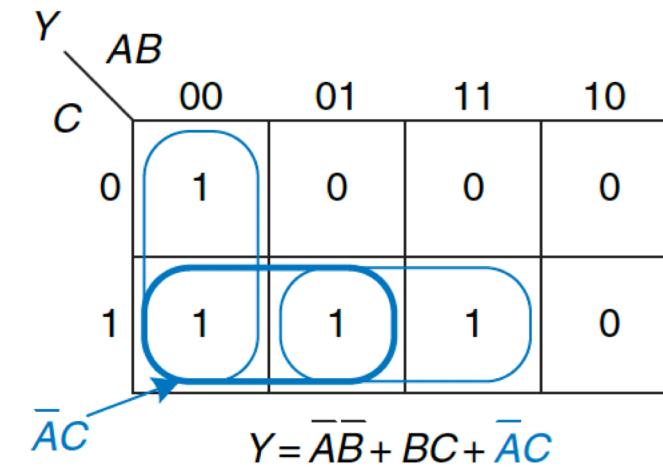
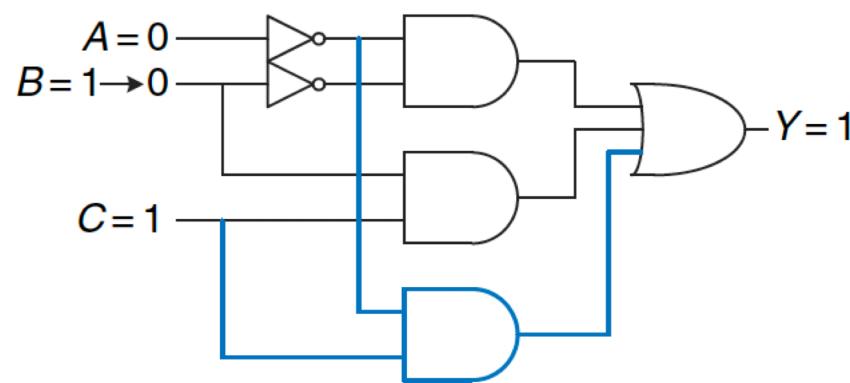
Figure 2.75 Circuit with a glitch

- As B transitions from 1 to 0, n_2 falls before n_1 can rise.
- Until n_1 rises, the two inputs to the OR gate are 0, and the output Y drops to 0
- When n_1 eventually rises, Y returns to 1



Y starts at 1 and ends at 1
but momentarily glitches to 0

Without a Glitch



Timing

- A sequential element has an **aperture** time around the clock edge, defined by a **setup time** and a **hold time**, before and after the clock edge, respectively. During which the input must be stable for the flip-flop to produce a well-defined output.
- Recall: **Static discipline** limited us to using logic levels outside the forbidden zone, the **dynamic discipline** limits us to using signals that change outside the aperture time.
- The **clock period** has to be long enough for all signals to settle. **The skew**, due to variation in arrival of the clock does to all flip-flops, further increases the clock period.
- Using **synchronizers** when interfacing with asynchronous inputs

Dynamic Discipline

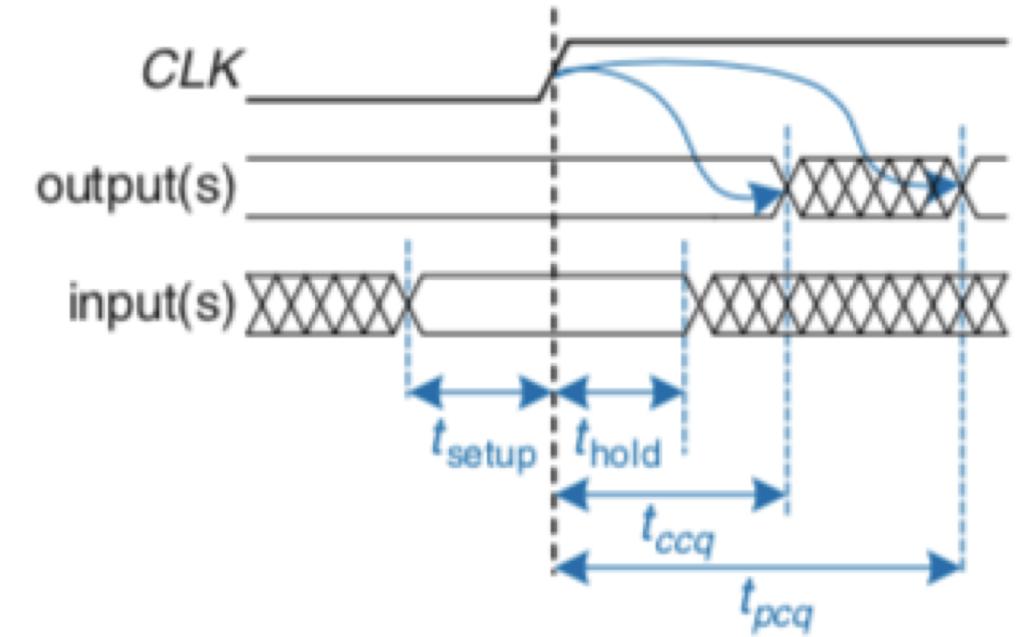
A synchronous sequential circuit, i.e. a flip-flop or FSM, has timing specifications:

After CLK rise, the **outputs**:

- Start to change after t_{ccq}
- Must settle within t_{pcq}

For correct input sampling, the **inputs**:

- Must have stabilized at least t_{setup} , before CLK rising
- Must remain stable for at least t_{hold} , after CLK rising



t_{ccq} - clock-to-Q contamination delay

t_{pcq} - clock-to-Q propagation delay

t_{setup} - setup time

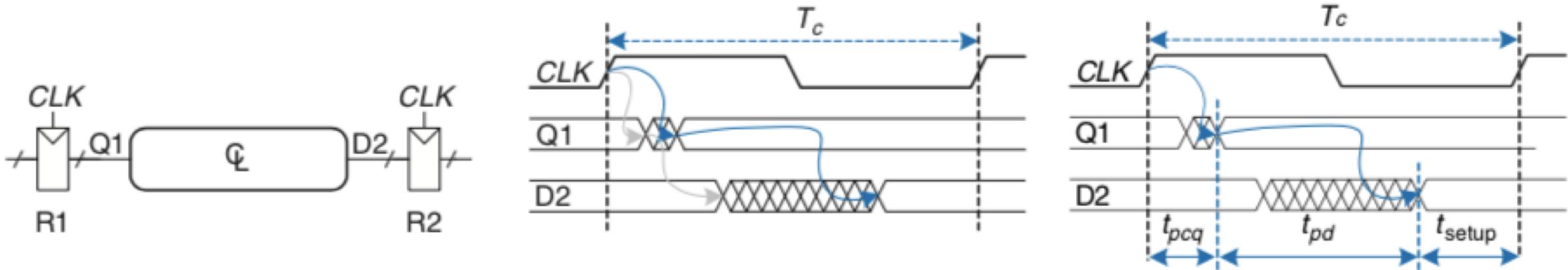
t_{hold} - hold time

Aperture Time = $t_{setup} + t_{hold}$

total time for which the input must remain stable.

Dynamic Discipline that the inputs of a synchronous sequential circuit must be stable during the setup and hold aperture time around the clock edge.

Setup Time Constraint



Minimum clock period:

$$T_c \geq t_{pcq} + t_{pd} + t_{setup}$$

Under the control
of the designer

specified by the manufacturer

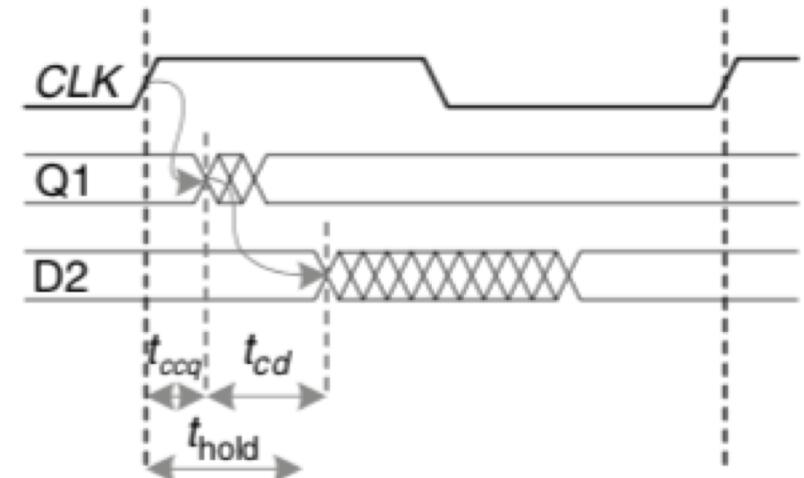
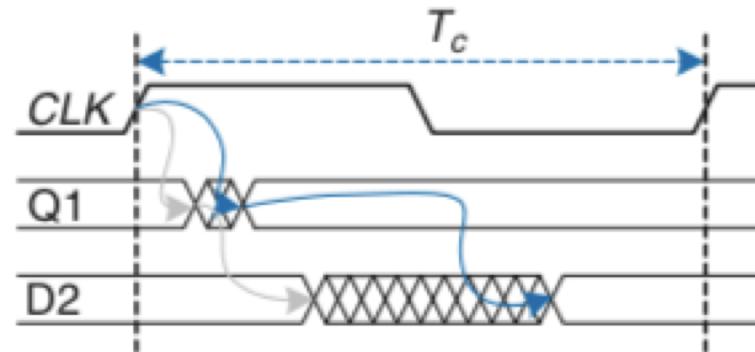
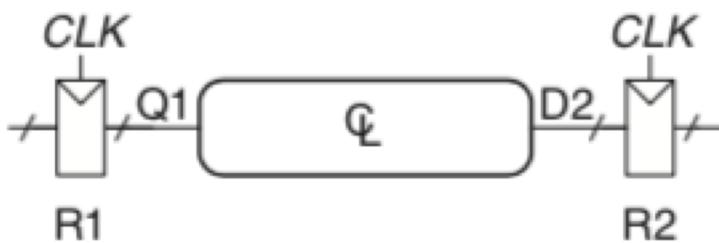
Setup time constraint or max-delay constraint :

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup})$$

sequencing overhead

Maximum propagation delay through the combinational logic

Hold Time Constraint



R₂ input, D₂, must not change until some time, t_{hold}, after the rising edge of the clock.

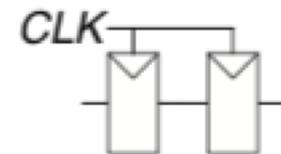
D₂ might change after $t_{ccq} + t_{cd} \geq t_{hold}$

Hold time constraint or min-delay constraint

$$t_{cd} \geq t_{hold} - t_{ccq}$$

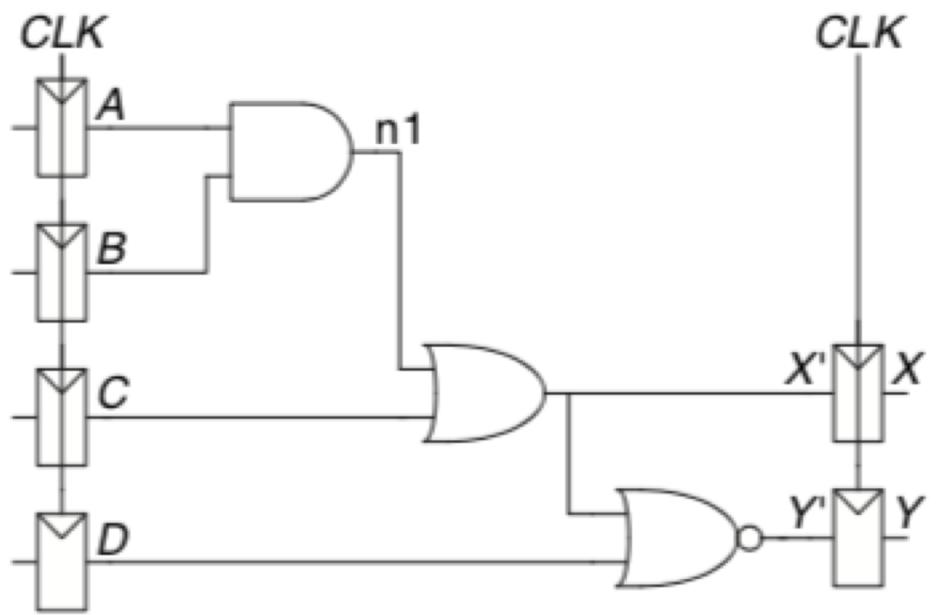
Minimum contamination delay through the combinational logic.

Consider Back-to-back flip-flops



$$t_{hold} \leq t_{ccq}$$

Example - Timing Analysis



Flip-flops have the following specifications:

$$t_{ccq} = 30 \text{ ps.}$$

$$t_{pcq} = 80 \text{ ps.}$$

$$t_{\text{setup}} = 50 \text{ ps.}$$

$$t_{\text{hold}} = 60 \text{ ps.}$$

Each logic gate has:

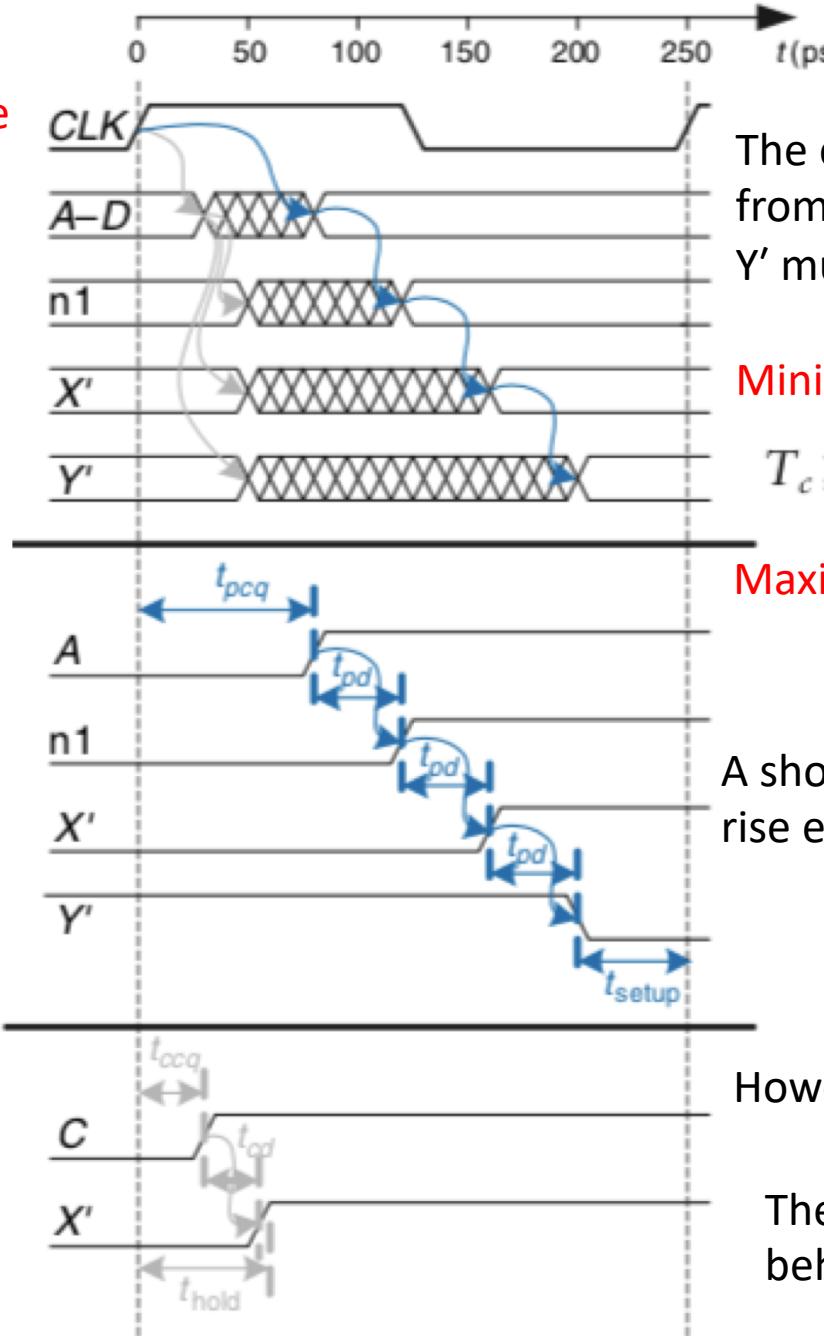
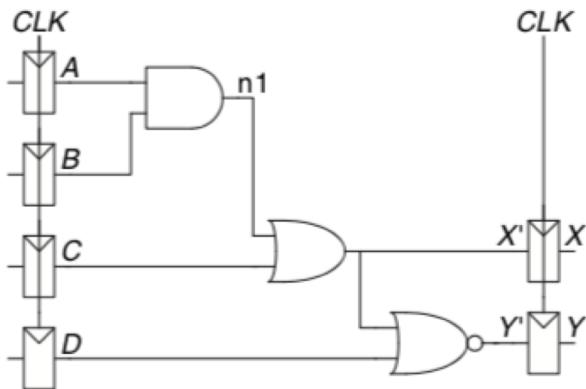
$$t_{pd} = 40 \text{ ps.}$$

$$\text{CLK } t_{cd} = 25 \text{ ps.}$$

Determine the maximum clock frequency and whether any hold time violations could occur.

Solution

General Case



The critical path occurs when B=1, C=0, D=0, and A rises from 0 to 1.

Y' must setup before the next rising edge of the CLK.

Minimum cycle time:

$$T_c \geq t_{pcq} + 3 t_{pd} + t_{setup} = 80 + 3 \times 40 + 50 = 250 \text{ ps}$$

Maximum clock frequency $f_c = 1/T_c = 4 \text{ GHz}$.

Critical Path (b)

Short Path (c)

A short path occurs when A = 0 and C rises, causing X' to rise each gate switches after only a contamination delay

$$t_{ccq} + t_{cd} = 30 + 25 = 55 \text{ ps}$$

However, the flip-flop has a hold time of 60 ps

The circuit has a **hold time violation** and may behave erratically at any clock frequency