

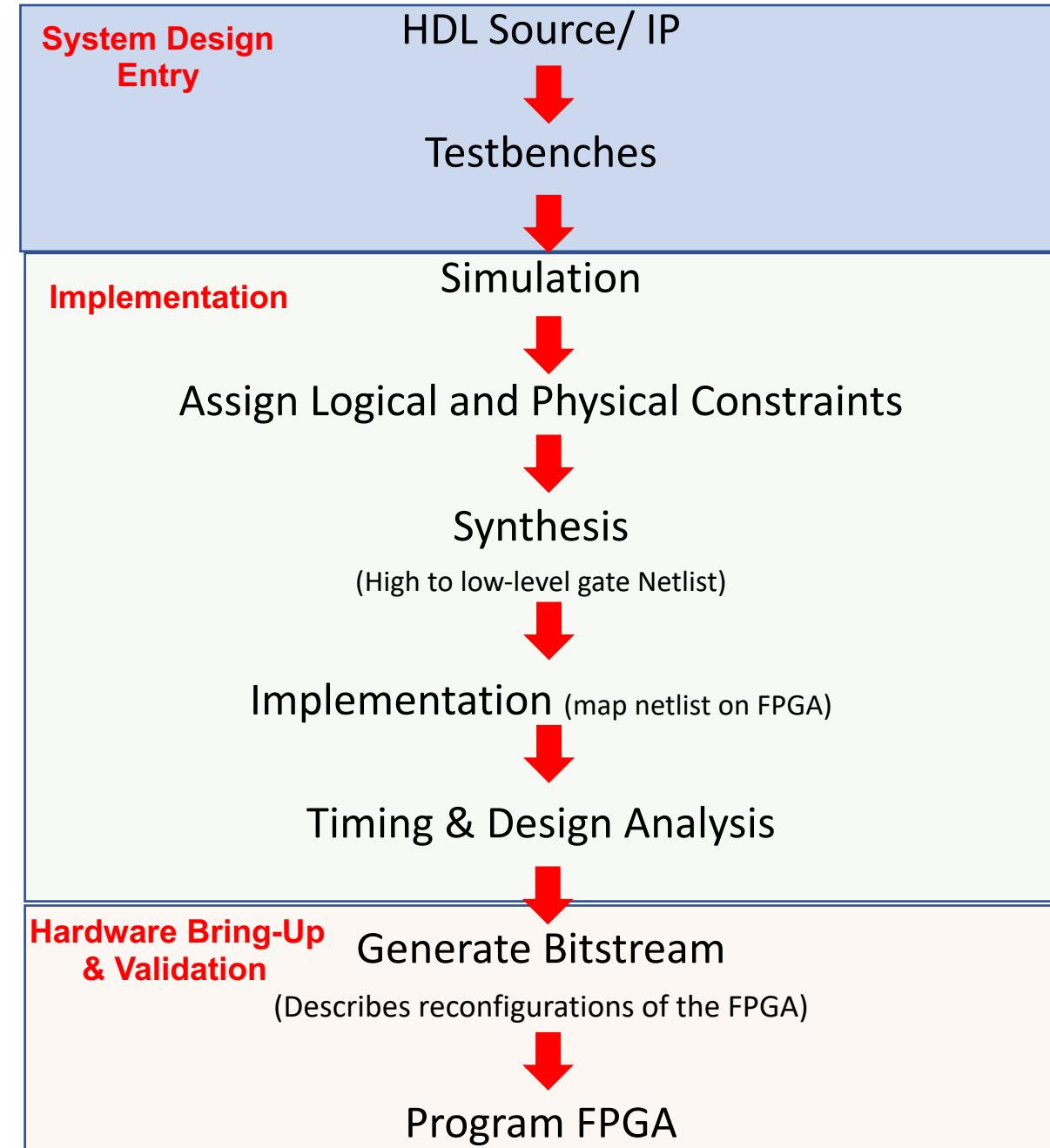
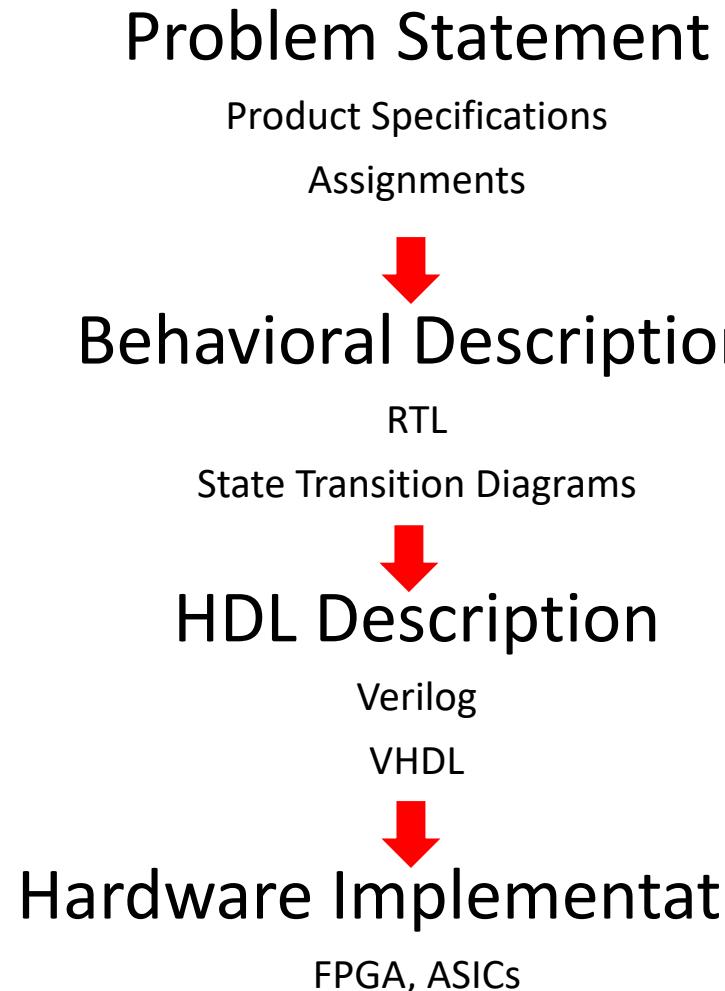
# Design Flow & Example

Lecture 3

# Outline

- Vivado Design Flow
- First Example – Schematics-based

# Design Flow



# Starting a New Project

## Create Project

1. Click **Next**

2. Project Name

- Enter **Project Name**
- Enter **Project Location**

3. Project Type

- Choose **RTL Project**
- Click **Next**

4. Add Sources

- Click **Next**

5. Add Constraints

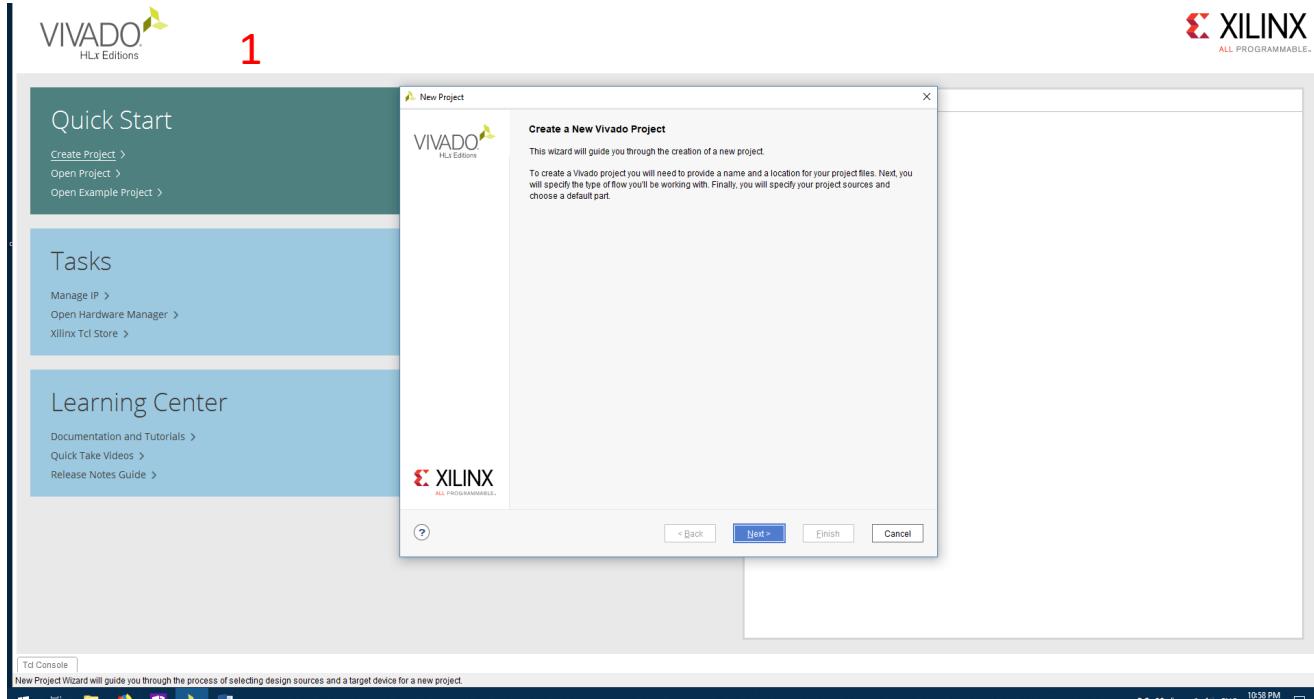
- Click **Next**

6. Default Part

- Click **Boards**
- Choose **ZedBoard**

7. New Project Summary

- Click **Finish**



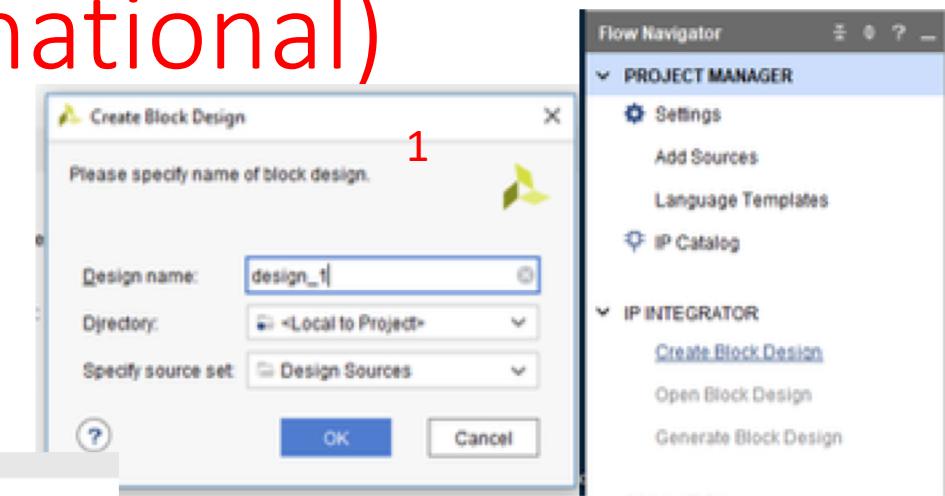
The image contains two side-by-side screenshots of the Vivado New Project Wizard. The left screenshot, labeled with a red '3', shows the 'Project Type' step. It lists several options: 'RTL Project' (selected), 'Post-synthesis Project', 'JTAG Planning Project', 'Imported Project', and 'Example Project'. The right screenshot, labeled with a red '6', shows the 'Default Part' step. It displays a grid of board options with columns for 'Display Name', 'Preview', 'Vendor', 'File Version', and 'Part'. The 'ZedBoard Zyng Evaluation and Development Kit' is highlighted in blue.

Display Name	Preview	Vendor	File Version	Part
ZedBoard Zyng Evaluation and Development Kit Add Daughter Card <a href="#">Connections</a>		em.avnet.com	1.4	xc7
ZYNQ-7 ZC702 Evaluation Board Add Daughter Card <a href="#">Connections</a>		xilinx.com	1.4	xc7

# Create a Block Design (Combinational)

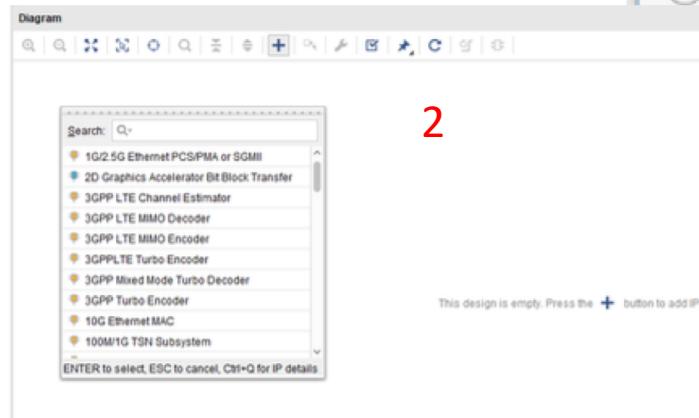
## 1. Flow Navigator

- IP Integrator
  - Click **Create Block Design**
  - Enter **Design Name**
  - Click **OK**



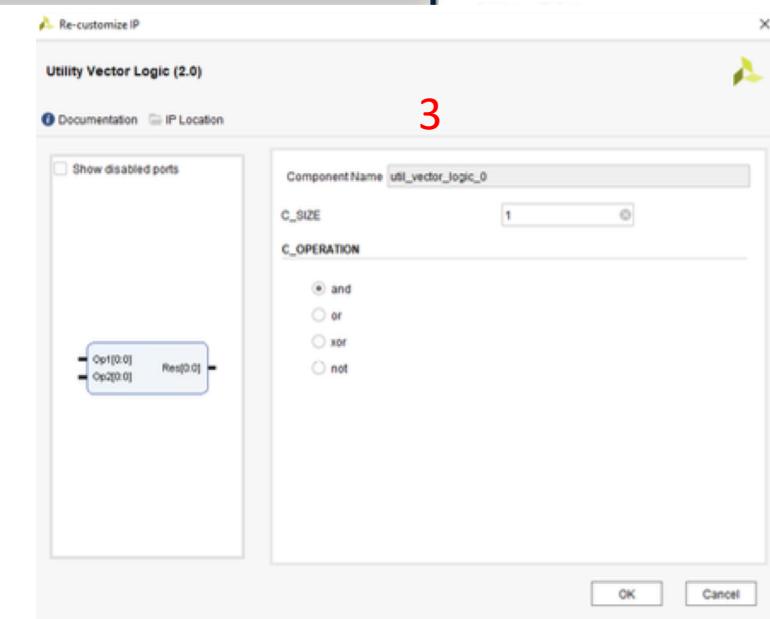
## 2. Under Diagram

- Click the + sign to **Add IP**
- Type **vector** in the search bar
- Choose **utility vector Logic**



## 3. Double click on the IP block

- Choose **size**
- Choose **Operation**



## 4. You may use the **Block Properties** window to set properties

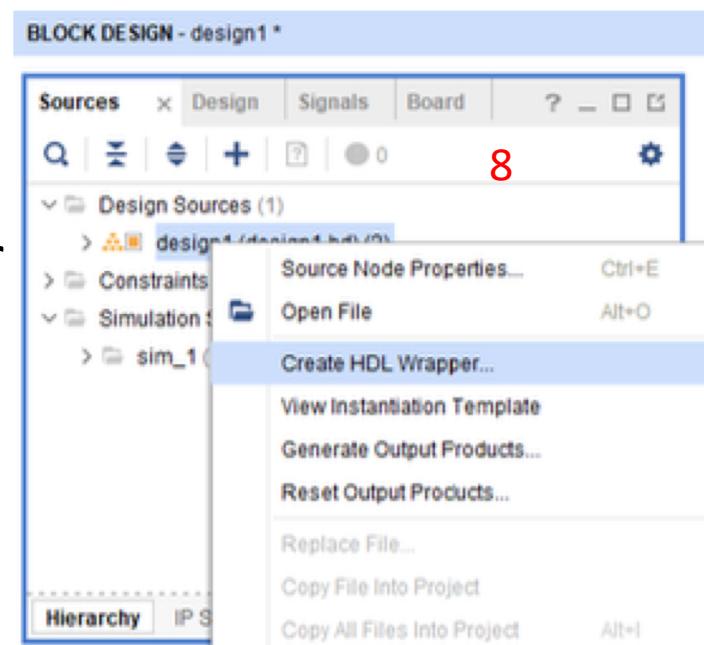
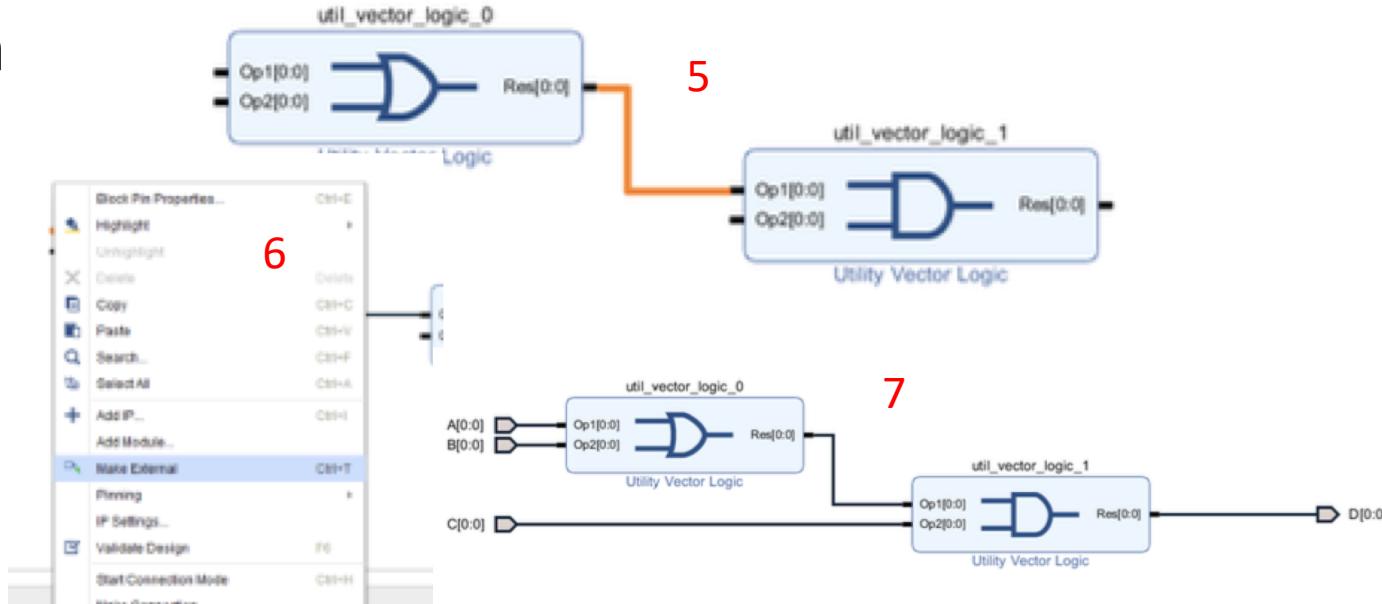
5. Make connections between the blocks (gates)

6. Add **external ports** at the outputs and inputs to drive the circuit as follows

- Right click on each I/O port
- Select **Make External**
- You may rename the external ports for convenience

7. Create HDL Code

- Right click on your design under **Design Sources**
- Click **Create Design Wrapper**
- Click **OK**



# Create Constraint File

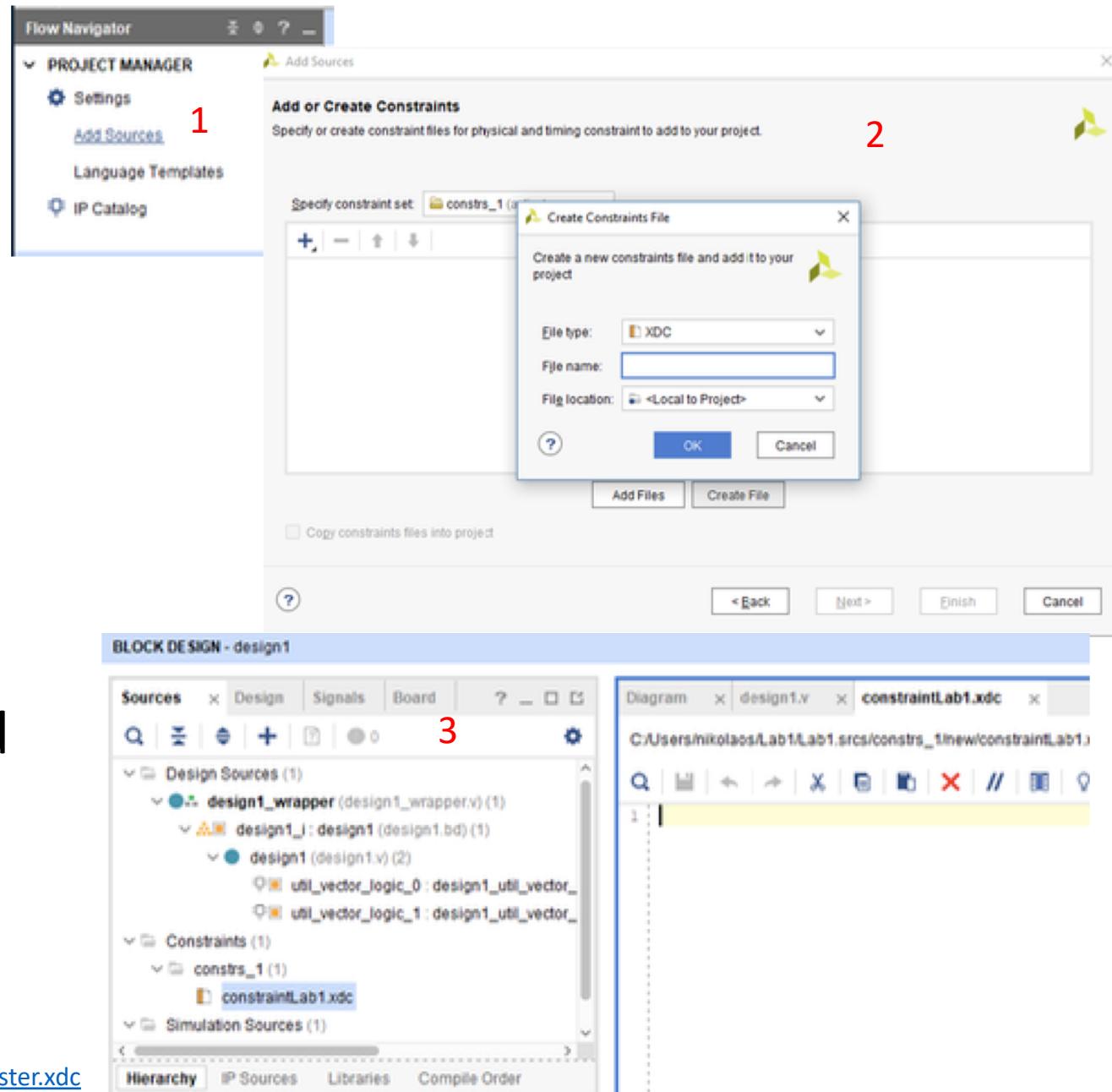
1. Click Add Sources under the Project Manager

2. Select Add or create constraints

- Name your file
- Click OK
- Click Finish

3. Double Click the newly created .xdc file

- Make I/O assignments and configure voltage levels



[https://www.xilinx.com/Attachment/valid\\_commands\\_for\\_xdc.txt](https://www.xilinx.com/Attachment/valid_commands_for_xdc.txt)

[https://github.com/Digilent/Zedboard/blob/master/Resources/XDC/zedboard\\_master.xdc](https://github.com/Digilent/Zedboard/blob/master/Resources/XDC/zedboard_master.xdc)

[http://zedboard.org/sites/default/files/documentations/ZedBoard\\_HW\\_UG\\_v2\\_2.pdf](http://zedboard.org/sites/default/files/documentations/ZedBoard_HW_UG_v2_2.pdf)

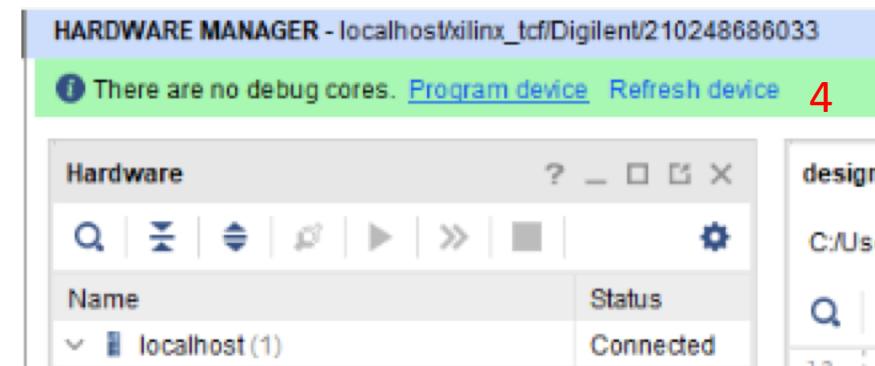
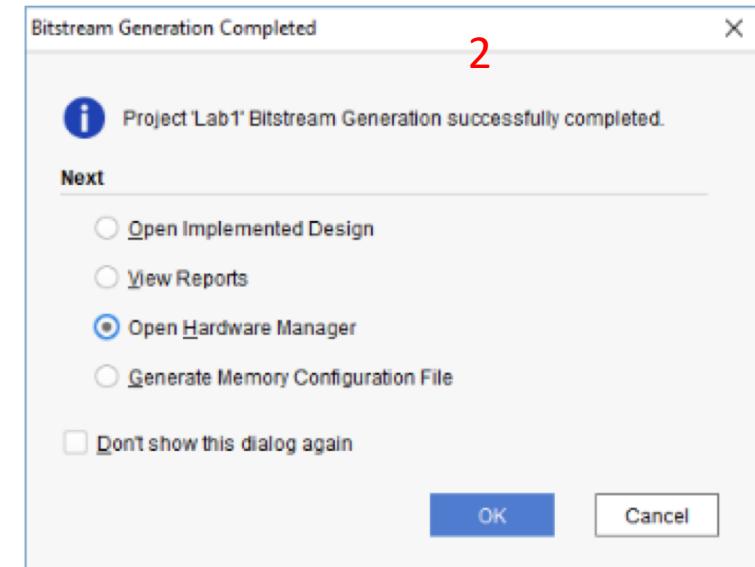
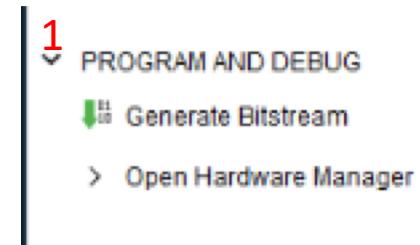
# .xdc File

```
# Assign inputs/outputs to actual pins on the FPGA
set_property PACKAGE_PIN M15 [get_ports A]
set_property PACKAGE_PIN H17 [get_ports B]
set_property PACKAGE_PIN H18 [get_ports C]
set_property PACKAGE_PIN W22 [get_ports D]

# Define voltage levels (3.3 for LEDs and 1.8 for Switches)
set_property IOSTANDARD LVCMOS18 [get_ports A]
set_property IOSTANDARD LVCMOS18 [get_ports B]
set_property IOSTANDARD LVCMOS18 [get_ports C]
set_property IOSTANDARD LVCMOS33 [get_ports D]
```

# Generate Bitstream & Program

1. Click Generate Bitstream under Program and Debug in the flow navigator
  - Click Yes
2. Choose Open Hardware Manager
3. Click Open target
  - Select Auto Connect
4. Click Program Device
  - Click Program
5. Test your program on the ZedBoard



IT WORKS!!