DATA SHEET

SUNPLUS

SPGT62C19B

Dual Full-Bridge Motor Driver

Preliminary

JUL. 30, 2003

Version 1.0

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DUAL FULL-BRIDGE MOTOR DRIVER

1. GENERAL DESCRIPTION

The SPGT62C19B motor driver is a CMOS monolithic integrated circuit able to drive both windings of a bipolar stepper motor or bi-directionally control two DC motors. The two output bridges can sustain 40 V and deliver up to 750 mA of continuous current each. The maximum output current, controlled by a PWM circuit, is determined by the user's selection of a reference voltage, a sensing resistor and two logic inputs. The outputs have been optimized for a low output saturation voltage drop.

Full, half and micro-stepping operations are possible.

The bridges are controlled by non-overlapping signals and have built-in clamp diodes for protection against transients. A thermal protection circuitry turns off all drivers when the junction temperature exceeds a safe operating limit. An under-voltage lockout circuitry prevents the chip from operating when the load supply is applied prior to the logic supply. Few external components are needed. Special power-up sequencing is not required.

The SPGT62C19B is available in 24-pin PowerDIP and SO packages.

2. FEATURES

- Pin-to-pin compatible with the ST L6219 and the ST or Allegro L6219DS circuits
- Able to drive both windings of a bipolar stepper motor
- Load voltage supply range: 10V to 40V
- Output current up to 750mA (each bridge)
- Internal fixed T_{off} time PWM current control
- Built-in protection diodes
- Internal thermal shutdown
- Under-voltage lockout
- LS-TTL compatible logic inputs with pull-up resistors
- Low Ron output resistance
- Low quiescent current
- -20°C to +85°C operating temperature range

3. BLOCK DIAGRAM

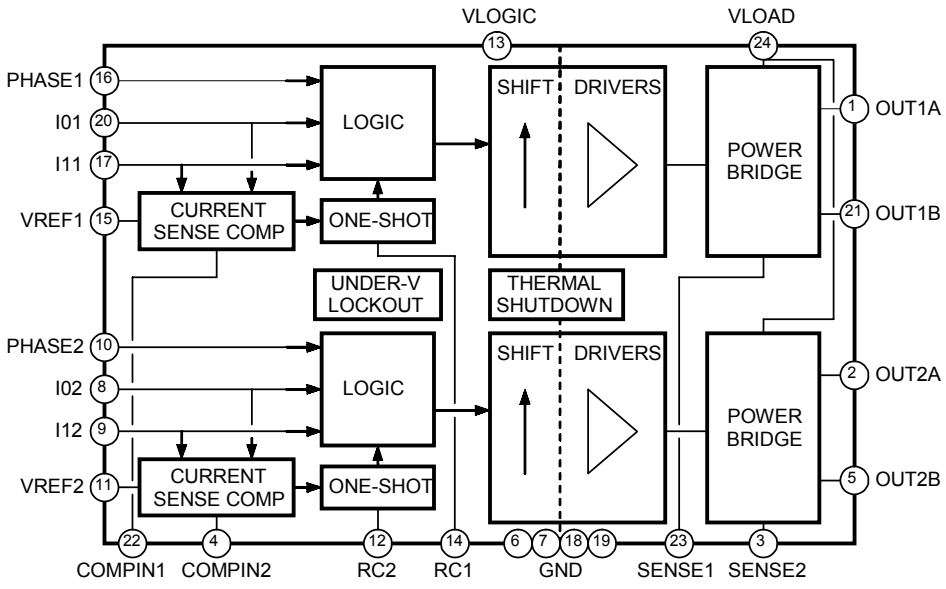


Figure 1: SPGT62C19B block diagram

4. SIGNAL DESCRIPTIONS

4.1. PIN Descriptions

Table 1: PIN description

PDIP & SO	Name	Function
1, 2	OUT1A, OUT2A	Output connection to "A" side of motor winding.
23, 3	SENSE1, SENSE2	Connection to lower sources of output stage for insertion of current sense resistor.
22, 4	COMPIN1, COMPIN2	Comparator input for current threshold detection. The voltage across the sense resistor is fed back to this input through the low pass filter RcCc (see Figure **7**). The power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by RtCt (toff = 1.1 RtCt) (see Figure 5).
21, 5	OUT1B, OUT2B	Output connection to "B" side of motor winding.
7, 18, 6, 19	GND1, GND2, GND3, GND4	Negative logic voltage supply (ground).
20, 8, 17, 9	I01, I02, I11, I12	Logic inputs to select level of current detection circuitry. Current also depends on sensing resistor and reference voltage. See FUNCTIONAL DESCRIPTION.
16, 10	PHASE1, PHASE2	Logic input to select direction of current flowing through load. 'H': load current from OUTxA to OUTxB; 'L': load current from OUTxB to OUTxA.
15, 11	VREF1, VREF2	Reference voltage for comparator. Determines the output current together with sensing resistor and logic inputs I0x, I1x. See FUNCTIONAL DESCRIPTION.
14, 12	RC1, RC2	A parallel RtCt network connected to this pin sets the OFF time of the power transistors. The pulse generator is a monostable triggered by the output of the comparators.
13	VLOGIC	Positive logic supply voltage.
24	VLOAD	Positive load supply voltage.

Note: Any logic input left unconnected will be treated as a high level.

4.2. PIN Assignments

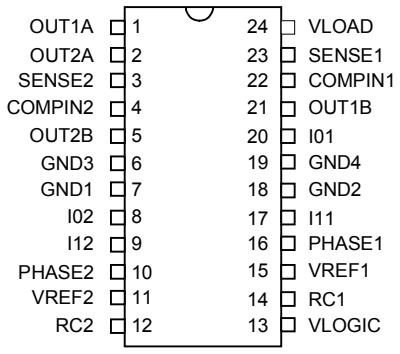


Figure 2: SPGT62C19B pin location (PDIP & SO packages)

4.3. Ordering Information

Product Number	Package Type
SPGT62C19B-PS10	Package form – SOP 24 (300mil)
SPGT62C19B-PD06	Package form - PDIP 24 (300mil)

5. FUNCTIONAL DESCRIPTIONS

The circuit is designed to drive the two windings of a bipolar stepper motor. Each motor winding is driven by an H-type bridge (see
Figure **3**) consisting of two N and two P transistors that allow the current to flow in both winding directions depending on the value of the PHASE signal.

Table 2: Current direction control

Phase	Output Current
L	Current flow from OUTB to OUTA
H	Current flow from OUTA to OUTB

Non-overlapping control logic is implemented to avoid shoot-through or crossover current through the bridge during transients when switching phases.

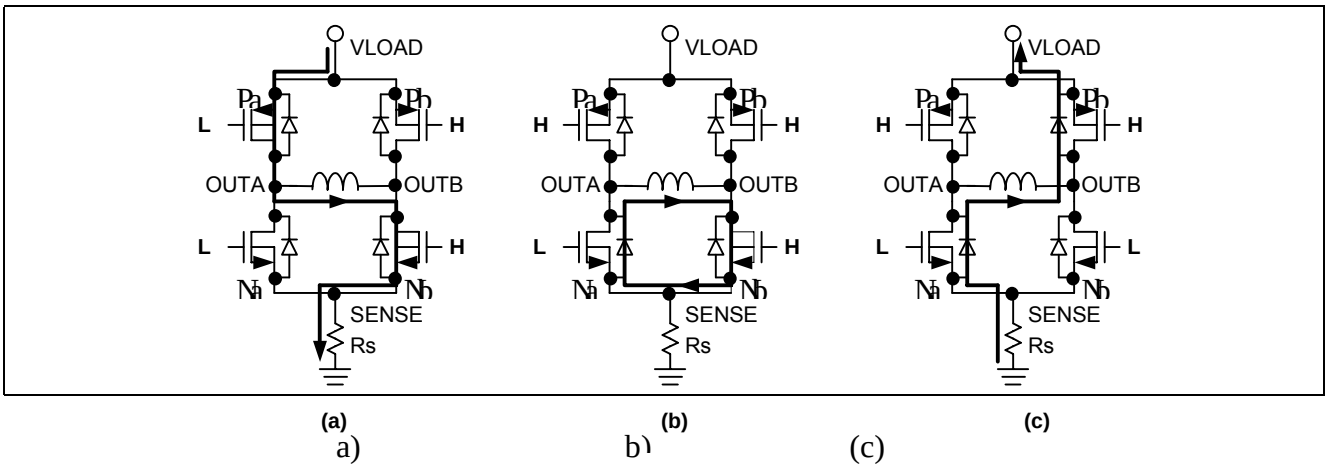


Figure 3: Power bridge control (PHASE = H / forward):
(a) bridge ON, (b) source OFF, and (c) all OFF / coasting
(for PHASE = L / reverse: invert A and B in drawings)

5.1. PWM Current Control

The current level in each motor winding is controlled by a PWM circuit with a fixed Toff time (see Figure **4**). The load current flowing in the winding is sensed through an external sensing resistor Rs connected between the power bridge's source pin SENSE (sources of transistors Na and Nb) and GND. The voltage across Rs is compared to a fraction of the reference voltage VREF, chosen with the logic input bits I0 and I1 (see **Table 3**). The maximum trip current for regulation, given for I0 I1 = 'LL', is:

$$I_{MAX} = \frac{V_{REF}}{10 * R_S}$$

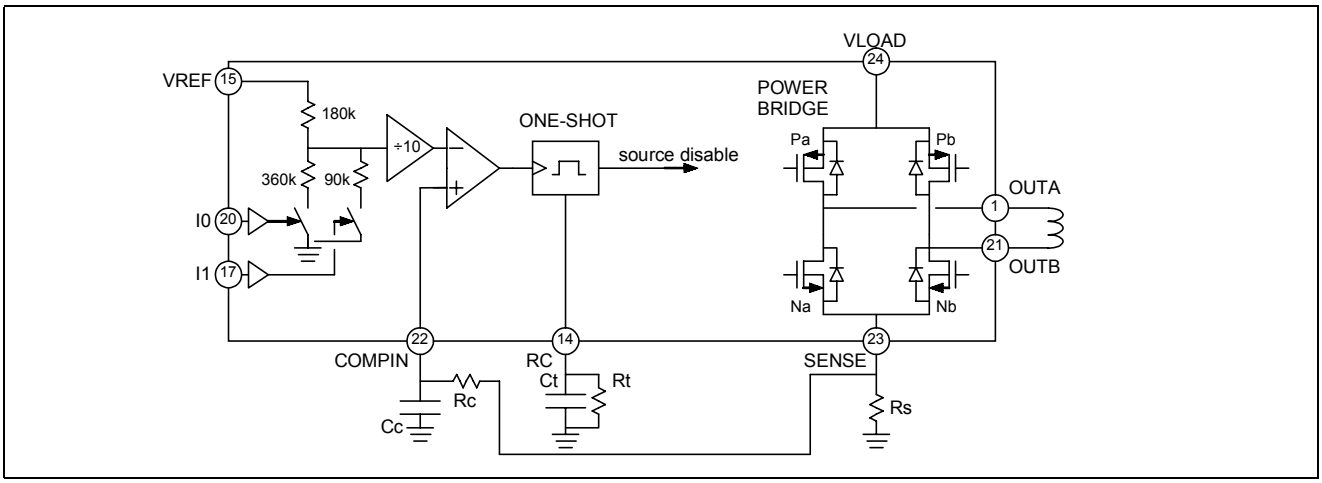


Figure 4: PWM current control circuit principle (channel 1 shown)

The power bridge and hence the load current can also be switched off completely when both logic inputs are High. Note that any logic input left unconnected will be treated as a high level.

Table 3: Current level control truth table

I0	I1	Output Current
L	L	$I_{MAX} = V_{REF}/10R_S$
H	L	$2/3*I_{MAX} = V_{REF}/15R_S$
L	H	$1/3*I_{MAX} = V_{REF}/30R_S$
H	H	0 (no current)

When the maximum allowed current is reached, the bridge source is turned off during a fixed period t_{off} (typically 50us) given by a non-retriggerable pulse generator and the external timing components Rt (20k-100kΩ range) and Ct (100pF-1000pF range):

$$t_{off} = 1.1 \cdot (Rt \cdot Ct)$$

During t_{off} the winding current decreases. When the driver is re-enabled, the winding current increases again until it reaches the threshold, and the cycle repeats itself maintaining the load current at the desired level.

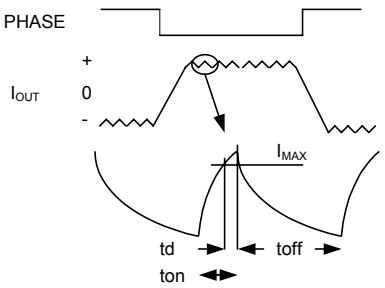


Figure 5: PWM output current waveform

5.2. Circuit Protection

A thermal protection circuitry turns off all drivers when the junction temperature exceeds a safe operating limit of 170°C (typ.). This protects the devices from failure due to excessive heating. Despite this thermal protection, output short circuits are not permitted. The output drivers are re-enabled once junction temperature has dropped below 145°C (typ.).

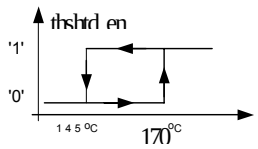


Figure 6: Thermal shutdown output vs. temperature showing hysteresis

An under-voltage lockout circuit protects the SPGT62C19B from potential shoot-through currents when the load supply voltage is applied prior to the logic supply voltage. The power bridge and all outputs are disabled if VLOGIC is smaller than 4V.

With this protection feature, the circuit will withstand any order of turn-on or turn-off of the supply voltages VLOGIC and VLOAD. Normal dV/dt values are assumed.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit	Comment
VLOAD	Load supply voltage	-	40	V	
Iout_peak	Output current (peak)	-	±1.0	A	
Iout_cont	Output current (continuous)	-	±0.75	A	
VLOGIC	Logic supply voltage	-	5.5	V	
Vin	Logic input voltage range	-0.3	5.5	V	
Vsense	Sense output voltage	-	1.5	V	
Tj	Junction temperature	-20	+150	°C	die temperature
Top	Operating temperature range	-20	+85	°C	
Tstg	Storage temperature range	-55	+150	°C	

Table 5: Thermal data

Symbol	Description	PDIP	SO	Unit
Rth_jc	Thermal resistance junction-case Max.	TBD	TBD	°C/W
Rth_ja	Thermal resistance junction-ambient Max.	TBD	76 (*)	°C/W

(*) With minimized copper area

6.2. Electrical characteristics

Table 6: SPGT62C19B target electrical characteristics. Unless otherwise specified: Ta = 25°C; VLOAD = 30V; VLOGIC = 4.75V to 5.25V; VREF = 5V. External components: Rs = 1Ω, Rc = 1kΩ, Cc = 820pF, Rt = 56kΩ, Ct = 820pF (see typical application circuit Figure **7**).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Comment
OUTPUT DRIVERS (OUTA or OUTB)						
VLOAD	Load/motor supply range	10	30	40	V	= VDDH
VLOGIC	Logic supply voltage	4.5	5	5.5	V	= VDD
Idsleak	Output leakage current					
	VOUT = VLOAD	-	<1	<50	μA	
	VOUT = 0	-	<-1	<-50	μA	
Vonn	Voltage OUTA/B-SENSE					sink driver
	Iout = +500mA	-	0.55	TBD	V	
	Iout = +750mA	-	0.9	TBD	V	
Vonp	Voltage VLOAD-OUTA/B					source driver
	Iout = +500mA	-	1.05	TBD	V	
	Iout = +750mA	-	1.85	TBD	V	
Ronn	Equivalent NMOS Ron					(1)
	Iout = +500mA	-	1.1	TBD	Ω	
	Iout = +750mA	-	1.2	TBD	Ω	
Ronp	Equivalent PMOS Ron					(1)
	Iout = +500mA	-	2.1	TBD	Ω	
	Iout = +750mA	-	2.5	TBD	Ω	
Vf_ndiode	Clamp diode forward voltage with I_F = 750mA	- -	0.95	TBD	V	(2)
Vf_pdiode	Clamp diode forward voltage with I_F = 750mA	-	1	TBD	V	(2)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Comment
Ivload_on	Driver supply current with both bridges ON, no load	-	0.55	1.0	mA	
Ivload_off	Driver supply current with both bridges OFF	-	0.55	1.0	mA	
CONTROL LOGIC						
Vin_h	High-level input voltage	2.4	-	-	V	all inputs (3)
Vin_l	Low-level input voltage	-	-	0.8	V	all inputs (3)
Iin_h	Input current (Vin = 2.4V)	-	-	-20	μA	(4)
Iin_l	Input current (Vin = 0.8V)	-	-	-40	μA	(4)
Vref	Reference voltage range	1.5	-	5.5	V	
Tjshutd	Thermal shutdown detection	-	170	-	°C	
Ivlogic	Total logic supply current					
	I0 = I1 = 0.8V	-	-	0.8	mA	
	I0 = I1 = 2.4V	-	-	0.8	mA	
Vref_Vsense	V_{REF}/V_{SENSE} current limit threshold					at trip point
	I0 = I1 = 0.8V	9.5	10	10.5	~ -	
	I0 = 2.4V; I1 = 0.8V	13.5	15	16.5	-	
	I0 = 0.8V; I1 = 2.4V	25.5	30	34.5	~ -	
toff	Cut-off time (one-shot pulse)	-	50	-	μs	
td	Turn-off delay	-	1-2	-	μs	

Notes: (1) Ronn and Ronp are defined as Vonn/Iout and Vonp/Iout respectively.

(2) Clamp/freewheel diode is the intrinsic body-drain diode of N/PMOS transistors.

(3) All digital inputs are LS-TTL compatible.

(4) Input current given by pull-up.

7. APPLICATION CIRCUITS

The SPGT62C19B circuit with external components for a typical application is shown in Figure **7**. Typical passive component values are: Rs = 1Ω, Rc = 1kΩ, Cc = 820pF, Rt = 56kΩ, Ct = 820pF.

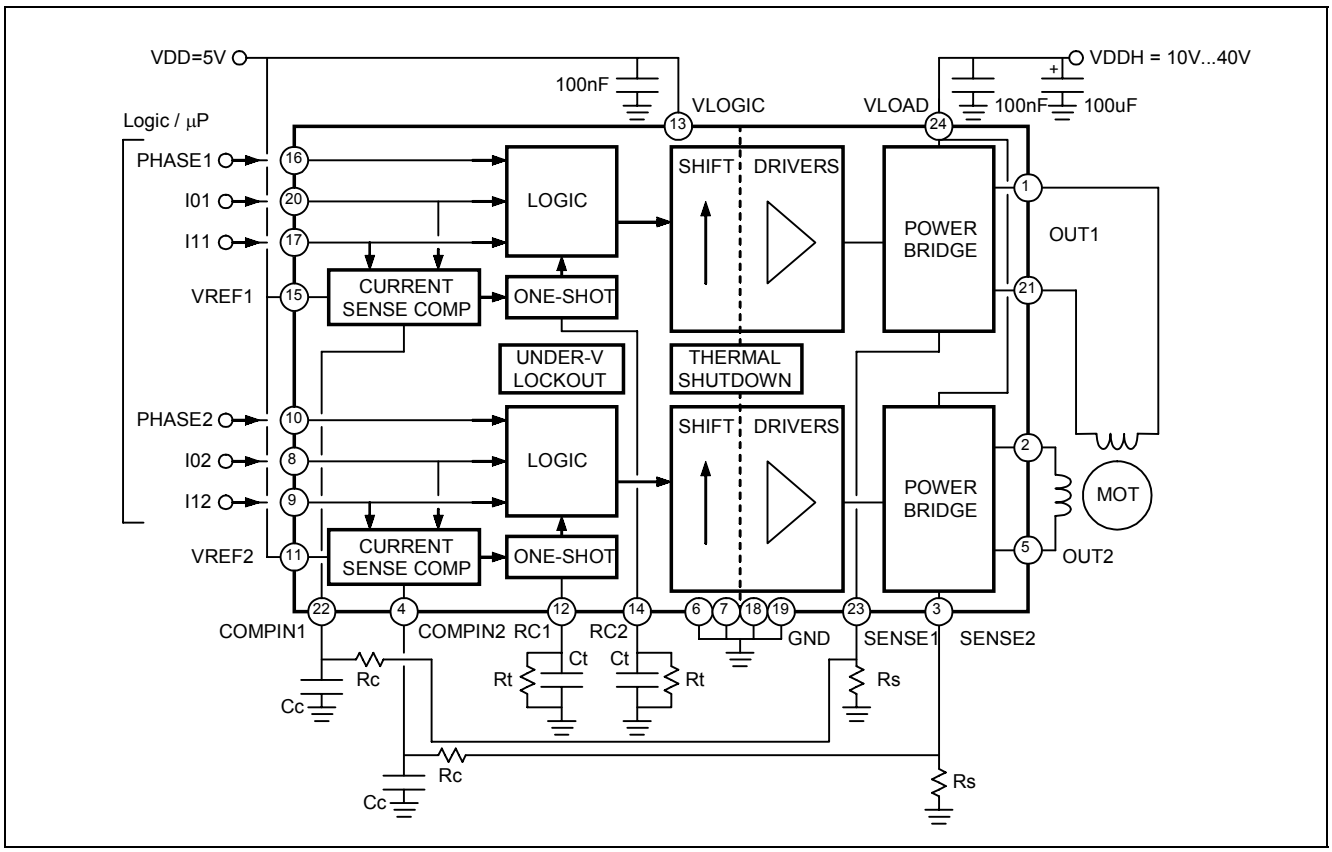


Figure 7: SPGT62C19B and typical application circuit

During PWM operation, when the output stage is turned-on, large voltage peaks might appear across Rs, which can wrongly trigger the input comparator. To avoid an unstable current control, an external RcCc filter should be used that delays the comparator action. Depending on load type many applications will not require this filter (SENSE connected to COMPIN).

7.1. Stepping Examples

The ASPMT62C19 allows commanding a motor in full-step, half-step, modified half-step and microstepping mode, as shown in the figure below.

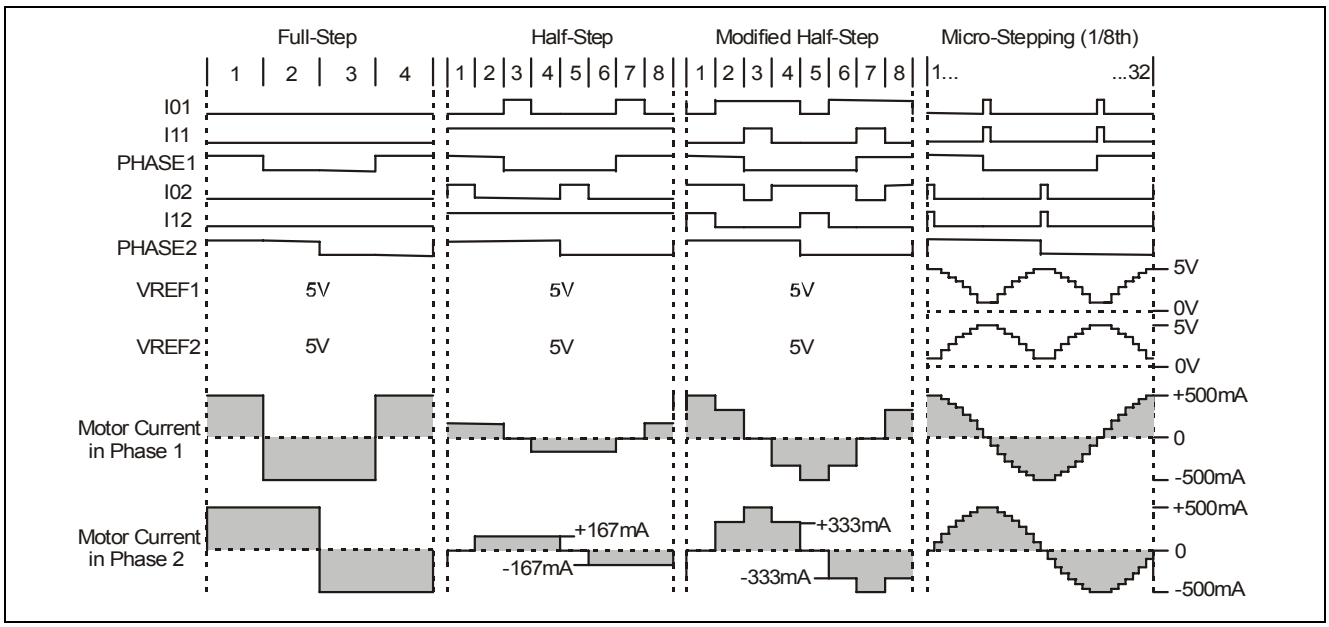


Figure 8: Examples of stepping modes achievable with typical application circuit

7.2. PCB Design Guidelines

Unused inputs should be connected to fixed voltage levels in order to get the highest noise immunity.

Typical PCB layout guidelines for power application should be followed. These include separate power ground planes, supply decoupling capacitors close to the IC, short connections and use of maximized copper areas to improve thermal dissipation.

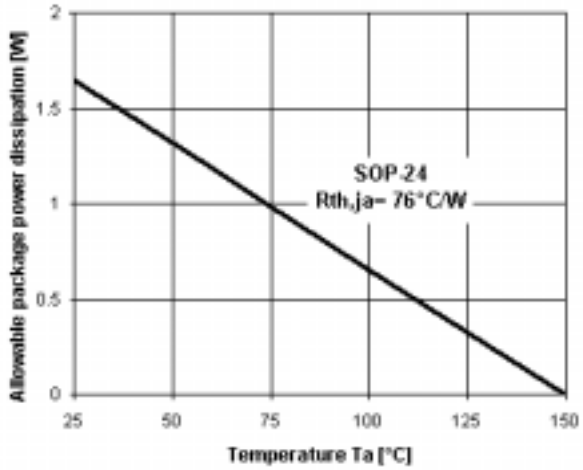
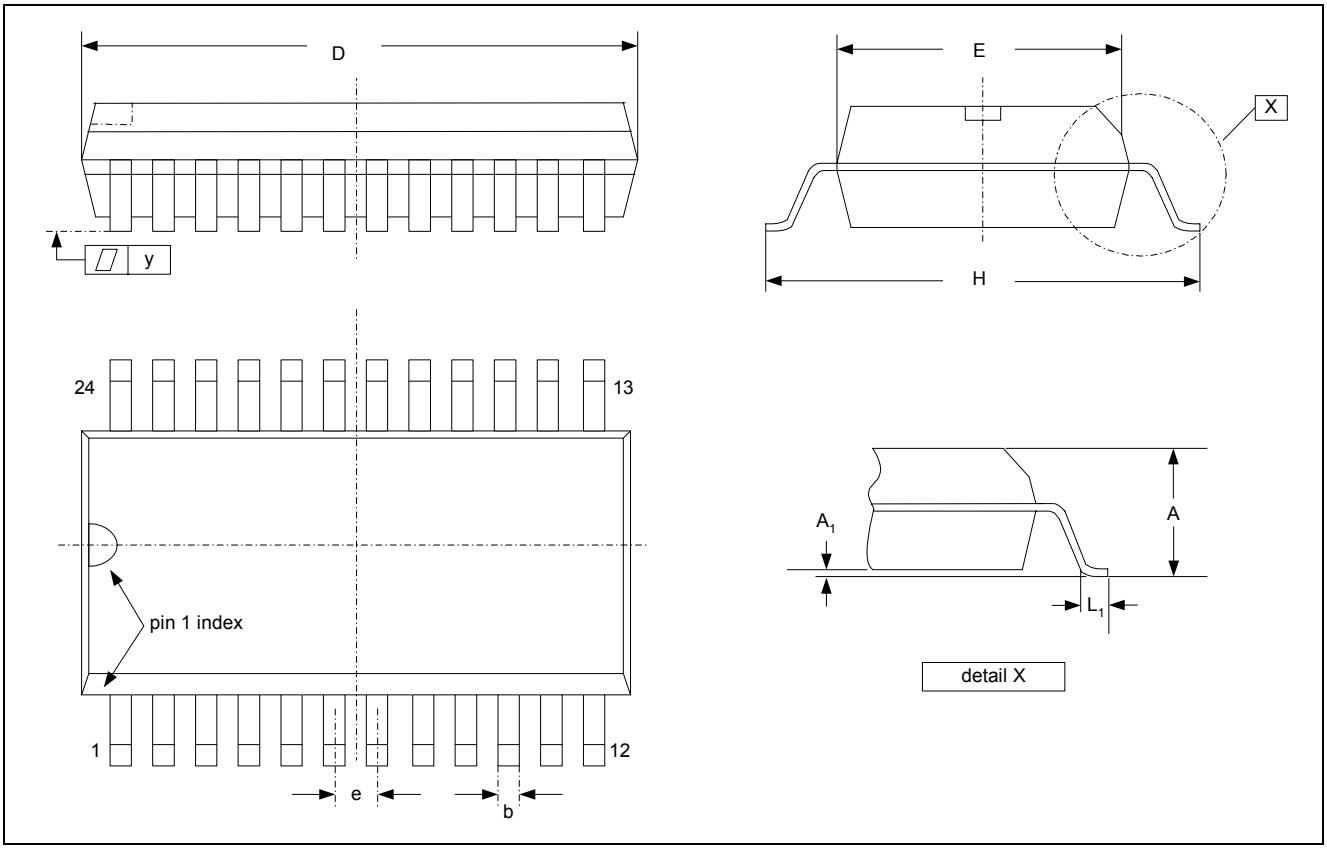


Figure 9: Maximum allowable package power dissipation vs. ambient temperature

8. PACKAGE/PAD LOCATIONS

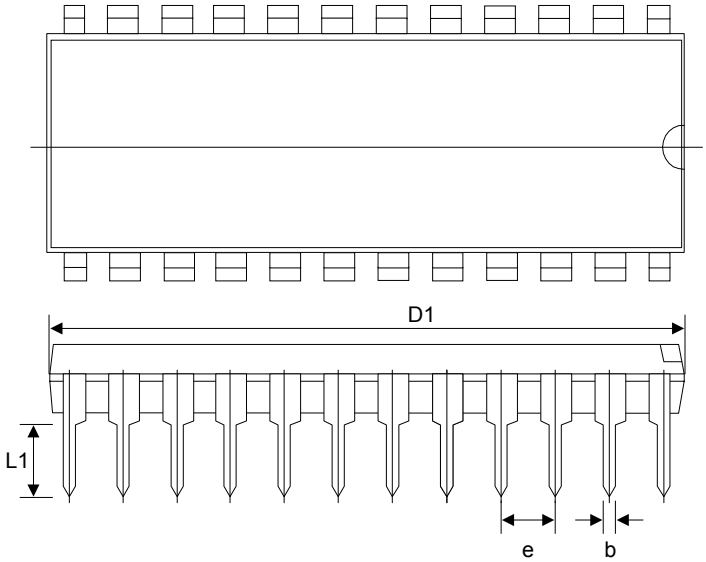
8.1. Package Information

8.1.1. SOP24 (300mil)



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.093	0.099	0.104
A1	0.004	-	0.012
b	-	0.016	-
D	0.599	0.600	0.614
E	0.291	0.295	0.299
e	-	0.050	-
H	0.394	0.406	0.419
L1	0.016	0.035	0.050
y	-	-	0.004

8.1.2. PDIP 24 (300mil)



Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1245 ±10	250 ±4	130 ±5	130 ±15	18 ±2	10Typ	100Typ

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-24-300

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10. REVISION HISTORY

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