深圳市亚晶达电子有限公司
SHENZHEN YAJINGDA ELECTRONICS CO.,LTD
电 话：0755-27668030 27668083　　传 真：0755-27668030-606

Specifications for Approval

Customer: _____

Model name: YJD12864C-1　　**VER:** V 1.0

ISSUE	QC DEPT	APPROVAL

Customer Approval

☐ **Accept**　　☐ **Reject**

Comment:

Approval by:

确认后请将此页回传

DATE: 2006-10-08

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YJD12864C-1 LCD Module

(Graphic Type)

1.0FEATURE

.Display mode: STN POSITIVE, TRANSFLECTIVE, YELLOW-GREEN COLOR(or BLUE,GRAY Negative Transmissive)
.Display format: 128*64 Dots
.Driving method: 1/32 Duty, 1/6 Bias
.Viewing direction: 6 o'clock(bottom view)
.Interface Input Data : 8-Bit ,4-Bit, Serial Bus
.Control IC: ST7920 ST7921
.Background color: Yellow (White)
.Glass to PCB: ZEBRA CONNECTO
.Operating temperature：-20~70°C
.Storage temperature：-30~80°C
. Dot Size : 0.48x 0.48 mm
. Dot Pitch : 0.52 x 0.52 mm

2.0 MAX STANDARD VALUE

ITEM	SYMBOL	MIN	TYPE	MAX	UNIT
OPERATING TEMPERATURE	Top	-20	25	70	℃
STORAGE TEMPERATURE	Tst	-30	25	80	℃
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	2.7	5.0	5.5	V

3.0 ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	V_{DD}-V_{SS}	Ta = 25 °C	4.5	5.0	5.5	V
INPUT HIGH VOL.	V_{IH}	Ta = 25 °C	V_{DD-1}	-	V_{DD}	V
INPUT LOW VOL.	V_{IL}	Ta = 25 °C	V_{SS}	-	1.0	V
OUTPUT HIGH VOL.	V_{OH}	Ta = 25 °C	0.8V_{DD}	-	V_{DD}	V
OUTPUT LOW VOL.	V_{OL}	Ta = 25 °C	-	-	0.1V_{DD}	V

4.0 MECHANICAL SPECIFICATIONS

ITEM	STANDARD VALUE	UNIT
PCB Dimension	93.0X70.0X1.60	mm
View Dimension	73.0X39.0	mm
Outline Dimension	93.0X70.0X13.0	mm

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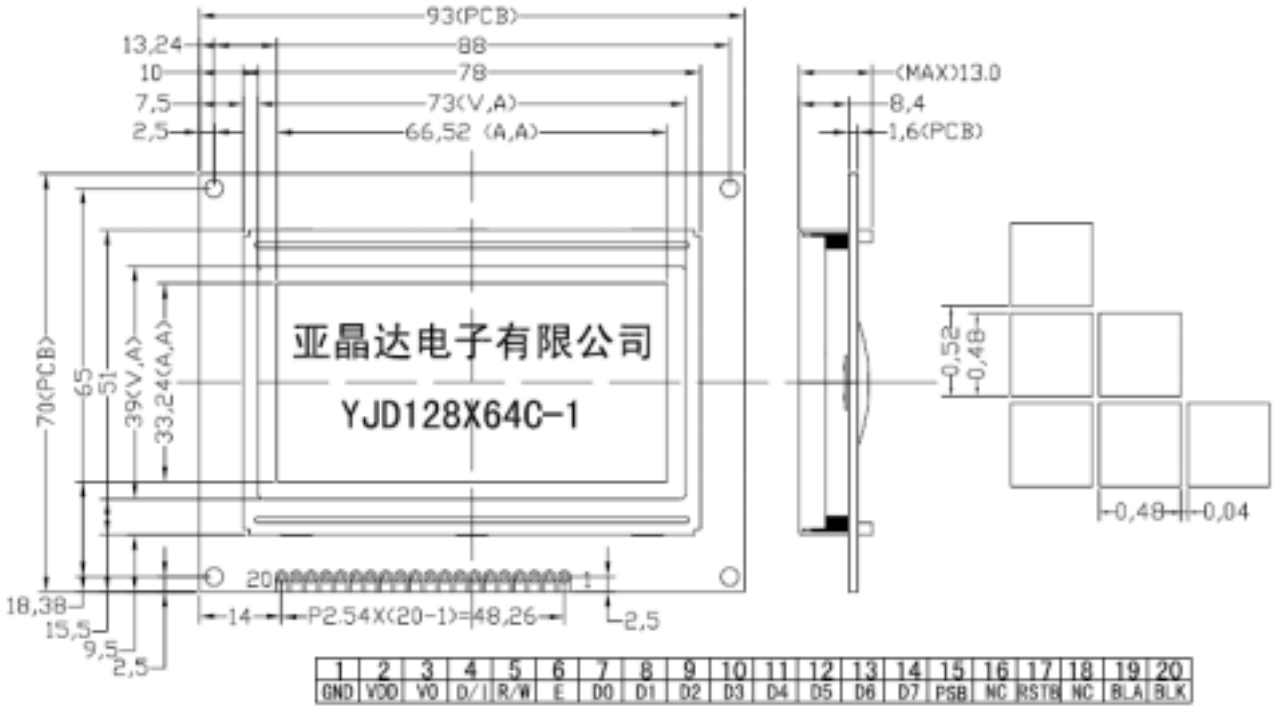
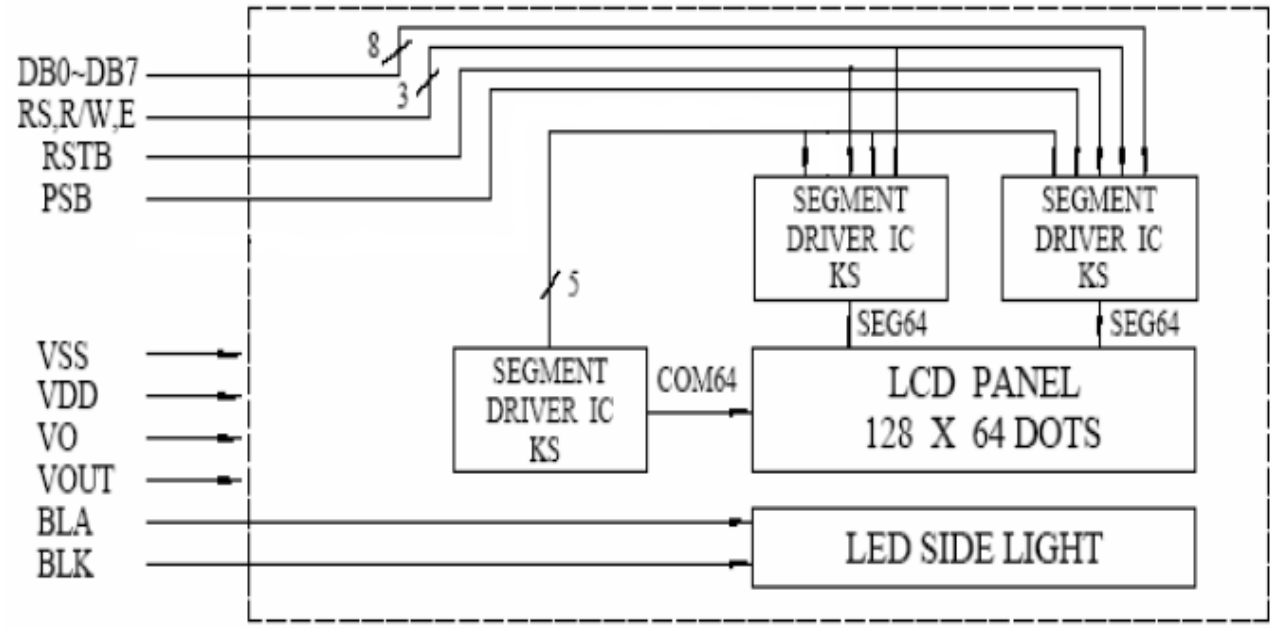
5.0 EXTERNAL DIMENSIONS



5.1 SYSTEM BLOCK DIAGRAM



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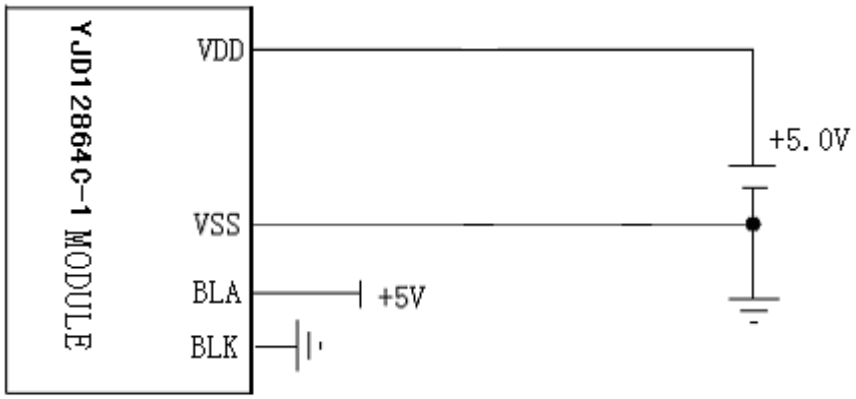
6.0 INTERFACE PIN FUNCTION DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	VSS	Ground(0V)
2	VDD	Power supply for logic circuit(5.0V)
3	VO	Operating voltage for LCD driving(Not connected)
4	D/I(CS*)	Register select 0: select instruction write, busy flag read, address counter read 1: select data write, read (Chip select) for serial mode 1: chip enable 0: chip disable
5	R/W(SID*)	Read write control 0: write 1: read (serial data input)
6	E(SCLK*)	Enable trigger (serial clock)
7-10	DB0 to DB3	Lower nibble data bus for 8 bit interface
11-14	DB4 to DB7	Higher nibble data bus for 8 bit interface and data bus for 4 bit interface
15	PSB	Interface selection: 0: serial mode 1: 8/4-bits parallel bus mode
16	NC	Not connected
17	RSTB	System reset low active
18	VEE	Not connected
19	BLA	Backlight (+5.0V)
20	BLK	Backlight (0V)

7.0 POWER SUPPLY BLOCK DIAGRAM



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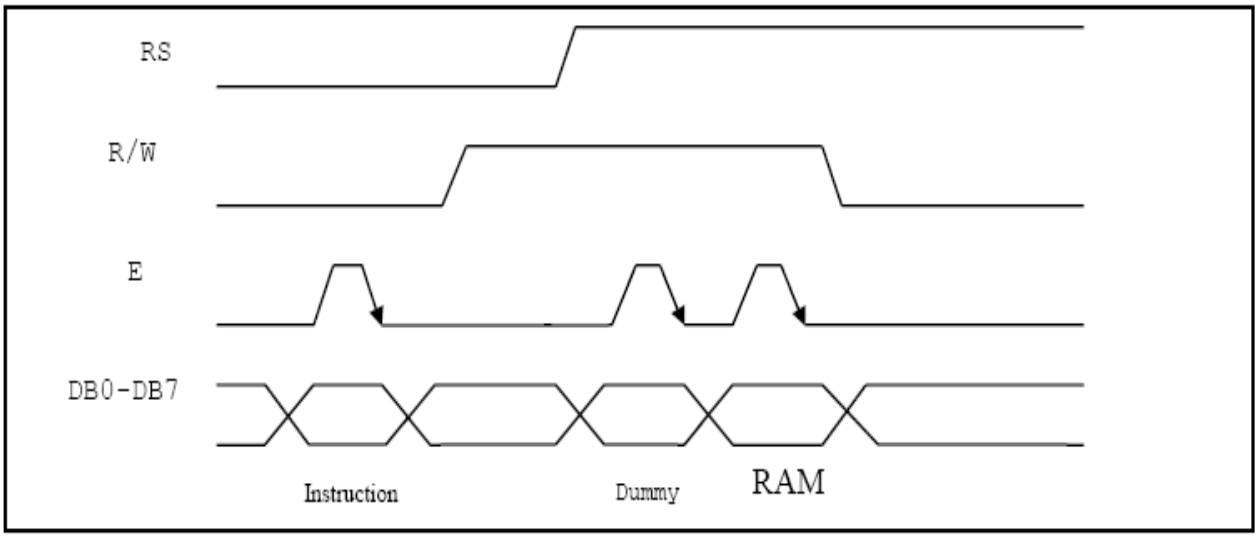
8.0 TIMING CHARACTERISTICS

Parallel interface :

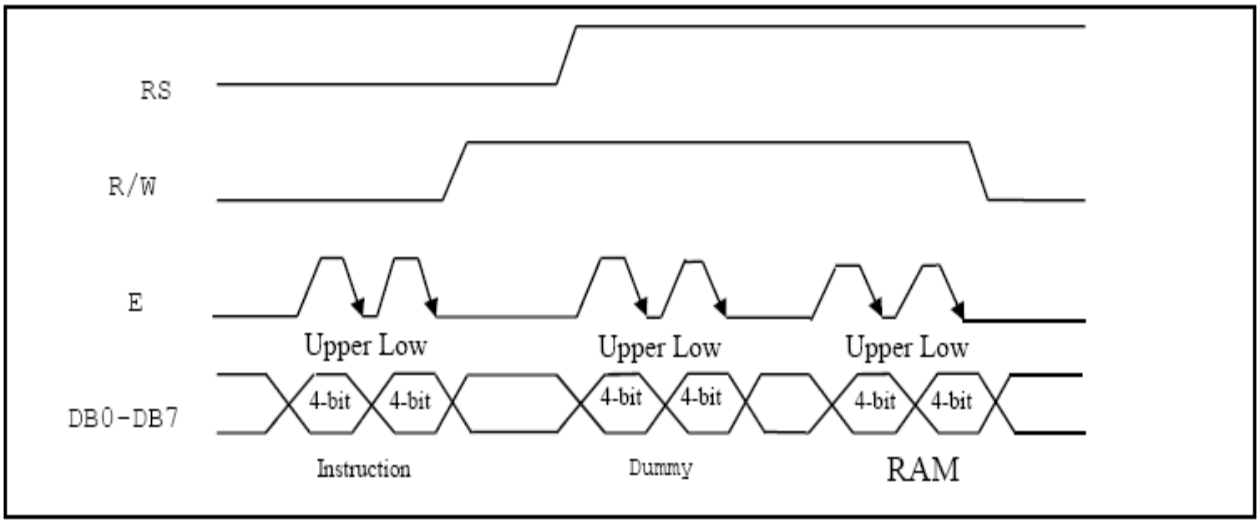
YJD12864C-1 is in parallel mode by pulling up PSB pin. And can select 8 bit or 4-bit bus interface by function set instruction DL control bit. MPU can control (RS , RW , E , and DB0..DB7) pins to complete the data transmission.

In 4-bit transfer mode, every 8 bits data or instruction is separated into 2 parts. Higher 4 bits (DB7~DB4) data will transfer

First and placed into data pins (DB7~DB4) . Lower 4 bits (DB3~DB0) data will transfer second and placed into data pins (DB7~DB4) . (DB3~DB0) data pins are not used.



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer



Timing Diagram of 4-bit Parallel Bus Mode Data Transfer

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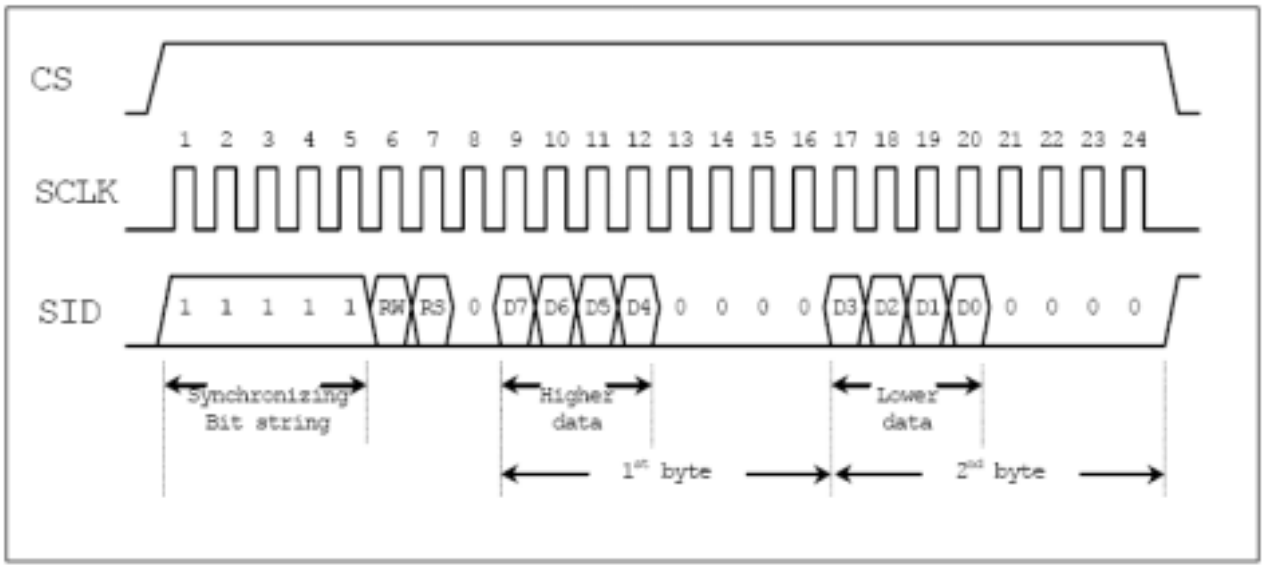
Serial interface :

YJD12864C-1 is in serial interface mode when pull down PSB pin. Two pins (SCLK and SID) are used to complete the data transfer. Only write data is available. When connecting several YJD12864C-1, chip select (CS) must be used. Only when (CS) is high the serial clock (SCLK) can be accepted. On the other hand, when chip select (CS) is low YJD12864C-1 serial counter and data will be reset. Transmission will be terminated and data will be cleared. Serial transfer counter is set to the first bit. For a minimal system with only one YJD12864C-1 and one MPU, only SCLK and SID pins are necessary. CS pin should pull to high.

YJD12864C-1's serial clock (SCLK) is asynchronous to the internal clock and is generated by MPU. When multiple instruction/data is transferred instruction execution time must be considered. Must wait for the previous instruction to finish before sending the next.

YJD12864C-1 has no internal instruction buffer area. When starting a transmission a start byte is required. It consists of 5 consecutive "1" (sync character). Serial transfer counter will be reset and synchronized. Following 2 bits for read/write (RW) and register/data select (RS). Last 4 bits is filled by "0". After receiving the sync character and RW and RS bits, every 8 bits instruction/data will be separated into 2 groups. Higher 4 bits (DB7~DB4) will be placed in first section followed by 4 "0". And lower 4 bits (DB3~DB0) will be placed in second section followed by 4 "0".



Timing Diagram of Serial Mode Data Transfer

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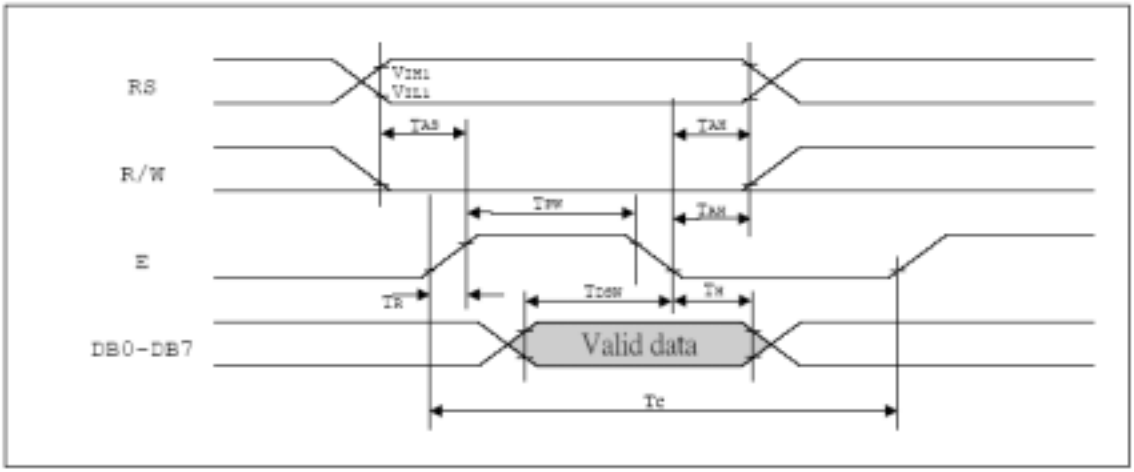
AC Characteristics (T_A = 25°C, V_{DD} = 4.5V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
		Internal Clock Operation				
f_{OSC}	OSC Frequency	R = 33KΩ	480	540	600	KHz
		External Clock Operation				
f_{EX}	External Frequency	-	480	540	600	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
		Write Mode (Writing data from MPU to ST7920)				
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
		Read Mode (Reading Data from ST7920 to MPU)				
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DDR}	Data Delay Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
		Interface Mode with LCD Driver(ST7921)				
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	-1000	-	1000	ns

8 bit interface timing diagram

MPU write data to YJD12864C-1



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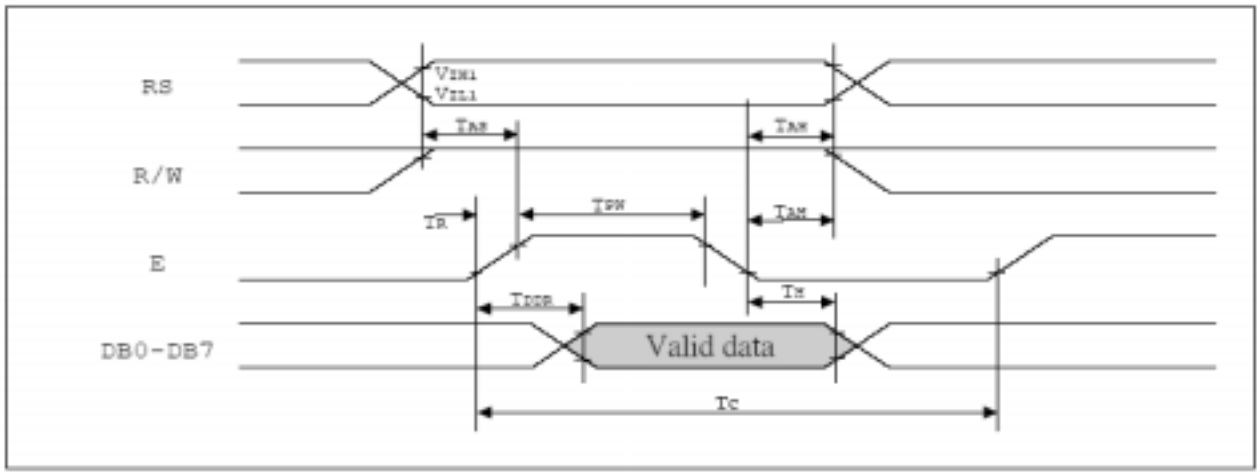
MPU read data from YJD12864C-1

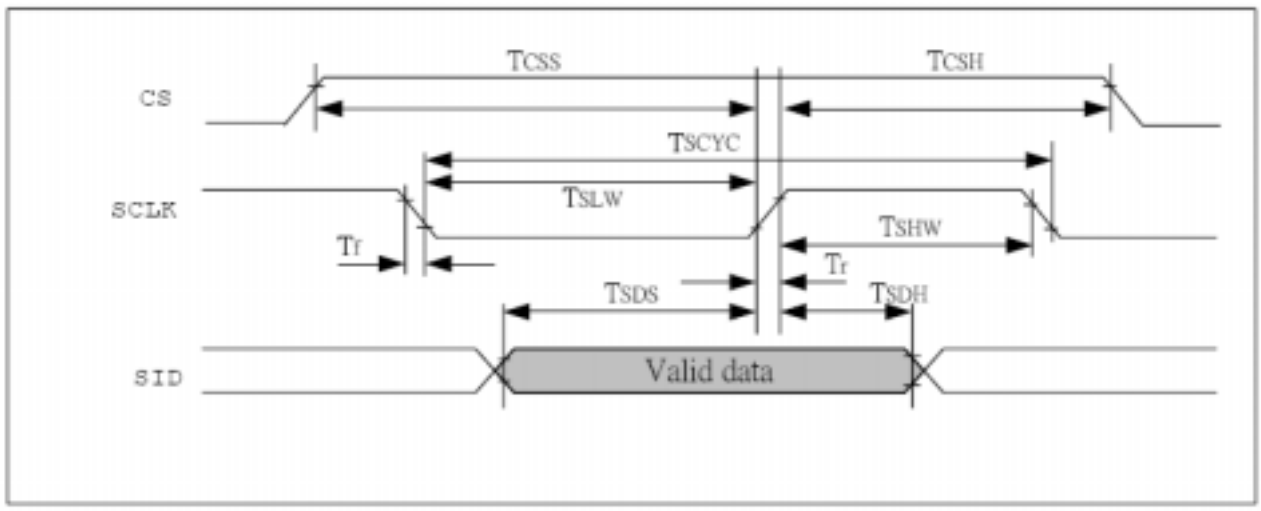


AC Characteristics (T_A = 25°C, V_{DD} = 4.5V) Serial Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
		Internal Clock Operation				
f_{OSC}	OSC Frequency	R = 33KΩ	470	530	590	KHz
		External Clock Operation				
f_{EX}	External Frequency	-	470	530	590	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
TSCYC	Serial clock cycle	Pin E	400	-	-	ns
TSHW	SCLK high pulse width	Pin E	200	-	-	ns
TSLW	SCLK low pulse width	Pin E	200	-	-	ns
TSDS	SID data setup time	Pins RW	40	-	-	ns
TSDH	SID data hold time	Pins RW	40	-	-	ns
TCSS	CS setup time	Pins RS	60	-	-	ns
TCSH	CS hold time	Pins RS	60	-	-	ns

Serial interface timing diagram

MPU write data to ST7920



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9.0 Display control instruction

Instruction set 1: (RE=0: basic instruction)

Ins	code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CLEAR	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H", and set DDRAM address counter (AC) to "00H"	1.6 ms
HOME	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin : the content of DDRAM are not changed	72us
ENTRY MODE	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation	72us
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1: display ON C=1: cursor ON B=1: blink ON	72 us
CURSOR DISPLAY CONTROL	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control : the content of DDRAM are not changed	72 us
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1: extended instruction** **RE=0: basic instruction**	72 us
SET CGRAM ADDR.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter (AC) **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
SET DDRAM ADDR.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter (AC) AC6 is fixed to 0	72 us
READ BUSY FLAG (BF) & ADDR.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) for completion of internal operation, also Read out the value of address counter (AC)	0 us
WRITE RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/GDRAM)	72 us
READ RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/GDRAM)	72 us

Instruction set 2: (RE=1: extended instruction)

Inst.	code										description	Exec. time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
STAND BY	0	0	0	0	0	0	0	0	0	1	Enter stand by mode, any other instruction can terminate (Com1..32 halted)	72 us
SCROLL or RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	SR=1: enable vertical scroll position SR=0: enable CGRAM address(**basic instruction**)	72 us
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction **R1,R0 initial value is 00**	72 us
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1: extended instruction set** **RE=0: basic instruction set** G=1 graphic display ON G=0 graphic display OFF	72 us
SET IRAM or SCROLL ADDR	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5~AC0 the address of vertical scroll	72 us
SET GRAPHIC RAM ADDR.	0	0	1	0 0	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set GDRAM address to address counter (AC) First set vertical address and the horizontal address by consecutive writing Vertical address range AC5...AC0 Horizontal address range AC3...AC0	72 us

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9.1 Command Description

CLEAR

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Fill DDRAM with "20H"(space code). And set DDRAM address counter (AC) to"00H". Set entry mode I/D bit to be "1". Cursor moves right and AC adds 1 after write or read operation.

HOME

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

Set DDRAM address counter (AC) to "00H". Cursor moves to origin. Then content of DDRAM is not changed.

ENTRY MODE SET

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the cursor movement and display shift direction when doing write or read operation.
I/D :address counter increase / decrease
When I/D = "1", cursor moves right, DRAM address counter (AC) add by 1.
When I/D = "0", cursor moves left, DRAM address counter (AC) subtract by 1.
S: Display shift

S	I/D	DESCRIPTION
H	H	Entire display shift left by 1
H	L	Entire display shift right by 1

DISPLAY STATUS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Controls display, cursor and blink ON/OFF.
D : Display ON/OFF control bit
When D = "1", display ON
When D = "0",display OFF , the content of DDRAM is not changed
C : Cursor ON/OFF control bit
When C = "1", cursor ON.
When C = "0", cursor OFF.
B : Blink ON/OFF control bit
When B = "1", cursor position blink ON. Then display data in cursor position will blink.
When B = "0", cursor position blink OFF

CURSOR AND DISPLAY SHIFT CONTROL

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	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	x	x

Instruction to move the cursor or shift the entire display. The content of DDRAM is not changed.

S/C	R/L	Description	AC Value
L	L	Cursor moves left by 1	AC=AC-1
L	H	Cursor moves right by 1	AC=AC+1
H	L	Display shift left by 1, cursor also follows to shift.	AC=AC
H	H	Display shift right by 1, cursor also follows to shift.	AC=AC

FUNCTION SET

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	X	RE	x	x

DL : 4/8 BIT interface control bit
When DL = "1", 8 BIT MPU bus interface
When DL = "0", 4 BIT MPU bus interface
RE : extended instruction set control bit
When RE = "1", extended instruction set
When RE = "0", basic instruction set
In same instruction cannot alter DL and RE at once. Make sure that change DL first then RE.

SET CGRAM ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to address counter (AC)
AC range is 00H..3FH
Make sure that in extended instruction SR=0 (scroll address or RAM address select)

SET DDRAM ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to address counter (AC) .
First line AC range is 80H..8FH
Second line AC range is 90H..9FH
Third line AC range is A0H..AFH
Fourth line AC range is B0H..BFH
Please note that only 2 lines can be display at a time.

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READ BUSY FLAG（BF）AND ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read busy flag (BF) can check whether internal operation is finished. At the same time the value of address counter
(AC) is also read. When BF = "1" new instruction will not be accepted. Must wait for BF = "0" for new instruction.

WRITE DATA TO RAM

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write data to internal RAM and alter the (AC) by 1
Each RAM address (CGRAM,DDRAM,IRAM…..) must write 2 consecutive bytes for 16 bit data. After the second
byte the address counter will add or subtract by 1 according to the entry mode set control bit.

READ RAM DATA

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read data from internal RAM and alter the (AC) by 1
After address set to read (CGRAM,DDRAM,IRAM…..)a DUMMY READ is required.
There is no need to DUMMY READ for the following bytes unless a new address set instruction is issued.

Description of extended instruction set

STAND BY

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Instruction to enter stand by mode. Any other instruction follows this instruction can terminate stand by.
The content of DDRAM remain the same.

VERTICAL SCROLL OR RAM ADDRESS SELECT

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	SR

When SR = "1", the vertical scroll address set is enabled.
When SR = "0", the IRAM address set (extended instruction) and CGRAM address set(basic instruction) is enabled.

REVERSE

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	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	R1	R0

Select 1 out of 4 lines to reverse the display and to toggle the reverse condition by repeating this instruction.
R1,R0 initial vale is 00. When set the first time the display is reversed and set the second time the display become normal.

R1	R0	Description
L	L	First line normal or reverse
L	H	Second line normal or reverse
H	L	Third line normal or reverse
H	H	Fourth line normal or reverse

Please note that only 2 lines out of 4 line display data can be displayed.

EXTENED FUNCTION SET

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	x	RE	G	x

DL : 4/8 BIT interface control bit
When DL = "1", 8 BIT MPU interface
When DL = "0", 4 BIT MPU interface
RE : extended instruction set control bit
When RE = "1", extended instruction set
When RE = "0", basic instruction set
G : Graphic display control bit
When G = "1", graphic display ON
When G = "0", Graphic display OFF
In same instruction cannot alter DL, RE and G at once. Make sure that change DL or G first and then RE.

SET SCROLL ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

SR=1: AC5~AC0 is vertical scroll displacement address

SET GRAPHIC RAM ADDRESS

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0

Set GDRAM address to address counter (AC) .
First set vertical address and then horizontal address(write 2 consecutive bytes to complete vertical and horizontal address set)
Vertical address range is AC5...AC0
Horizontal address range is AC3…AC0
The address counter (AC) of graphic RAM(GRAM) only increment after write for horizontal address. After horizontal address =0FH it will automatically back to 00H. However, the vertical address will not increase as the result of the same action.

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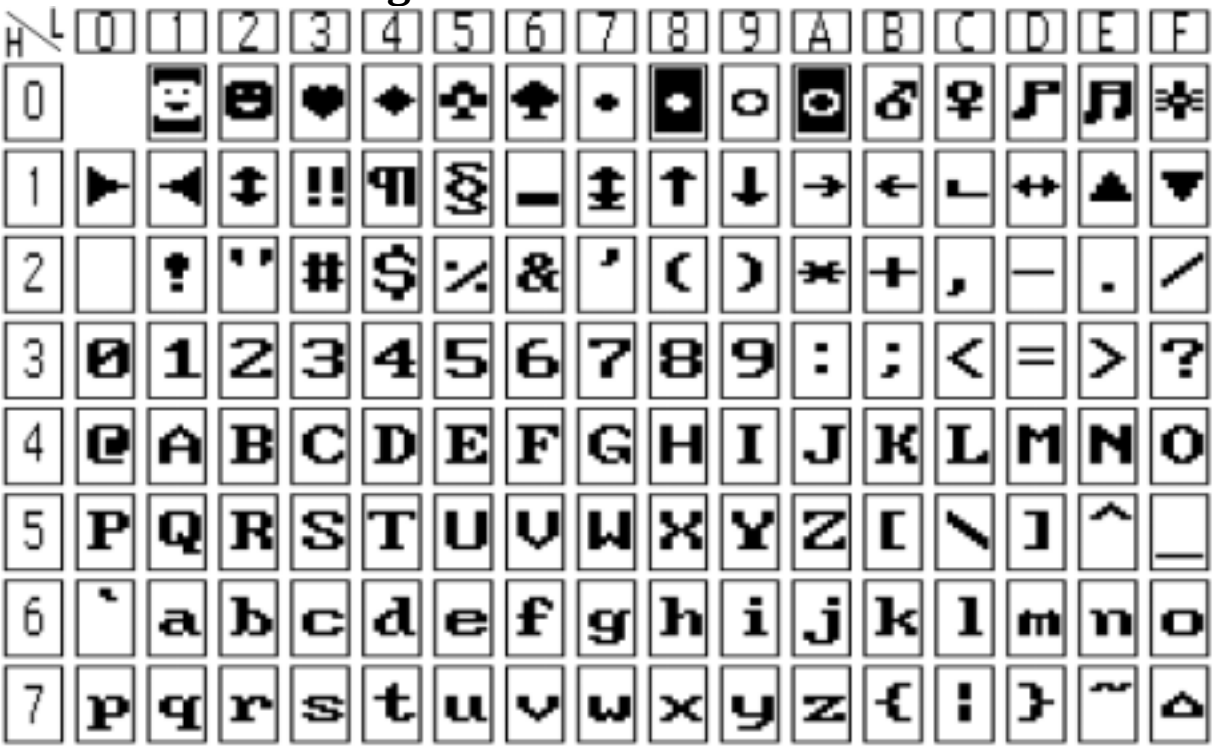
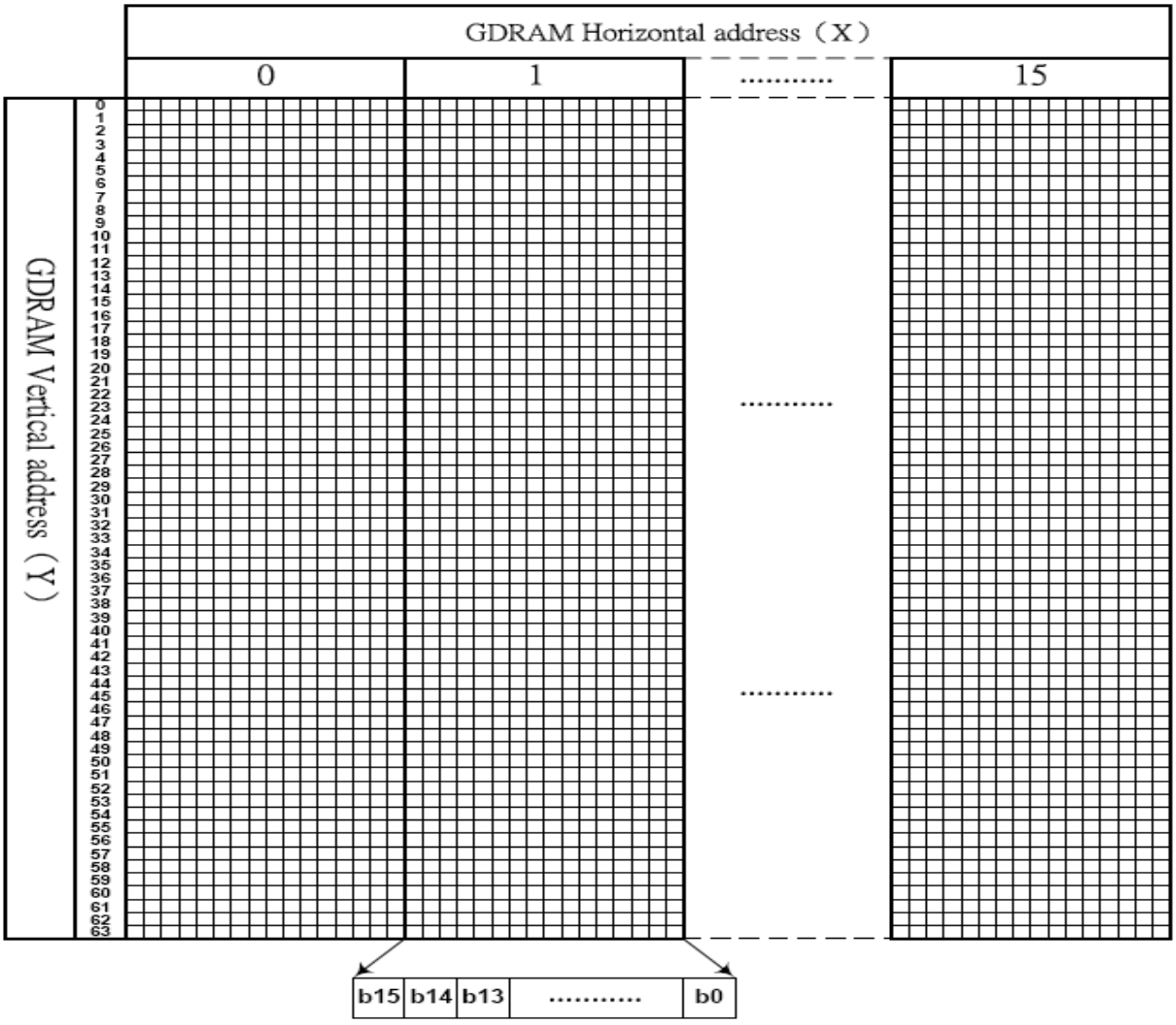
10.0 16x8 half-height characters



11.0 GDRAM display coordinates and corresponding address



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12.0 16x16 character generation ROM (CGROM) and 8x16 half height ROM（HCGROM）

ST7920 provides character generation ROM supporting 8192 16 x 16 character fonts and 126 8 x 16 alphanumeric characters. It is easy to support multi languages application such as Chinese and English. Two consecutive bytes are used to specify one 16x16 character or two 8x16 half-height characters. Character codes are written into DDRAM and the corresponding fonts are mapped from CGROM or HCGROM to the display drivers.

12.1 Character generation RAM (CGRAM)

ST7920 provides RAM to support user-defined fonts. Four sets of 16x16 bit map area are available. These user-defined fonts are displayed the same ways as CGROM fonts through writing character cod data to DDRAM.

12.2 Display data RAM（DDRAM）

There are 64x2 bytes for display data RAM area. Can store display data for 16 characters(16x16) by 4 lines or 32 characters(8x16) by 4 lines. However, only 2 lines can be displayed at a time. Character codes stored in DDRAM point to the fonts specified by CGROM, HCGROM and CGRAM. ST7920 display half height HCGROM fonts, user-defined CGRAM fonts and full 16x16 CGROM fonts. Data codes 0000H～0006H are for CGRAM user-defined fonts. Data codes 02H～7FH are for half height alpha numeric fonts. Data codes (A140～D75F) are for BIG5 code and (A1A0～F7FF) are for GB code.

1. display HCGROM fonts：Write 2 bytes data to DDRAM to display two 8x16 fonts. Each byte represents 1 character font. The data of each byte is 02H～7FH.
2. display CGRAM fonts：Write 2 bytes data to DDRAM to display one 16x16 font. Only 0000H, 0002H, 0004H, 0006H are allowed.
3. display CGROM fonts：Write 2 bytes data to DDRAM to display one 16x16 font. A140H～D75FH are for (BIG5) code, A1A0H～F7FFH are for (GB) code. Higher byte (D15～D8) are written first and then lower byte (D7～D0) .

12.3 Graphic RAM（GDRAM）

Graphic display RAM supports 64x256 bits bit-mapped memory space. GDRAM address is set by writing 2 consecutive bytes for vertical address and horizontal address. Two-bytes data write to GDRAM for one address. Address counter will automatically increase by one for the next two-byte data. The procedure is as followings.

1. Set vertical address (Y) for GDRAM
2. Set horizontal address (X) for GDRAM
3. Write D15～D8 to GDRAM (first byte)
4. Write D7～D0 to GDRAM (second byte)

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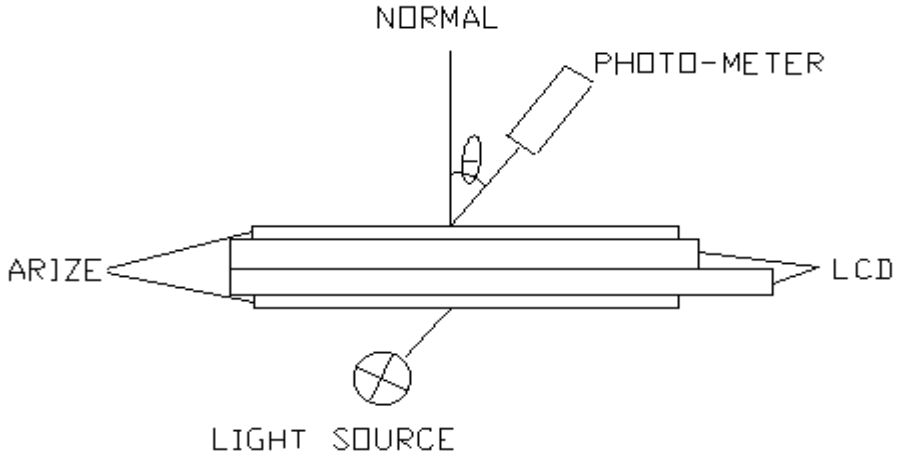
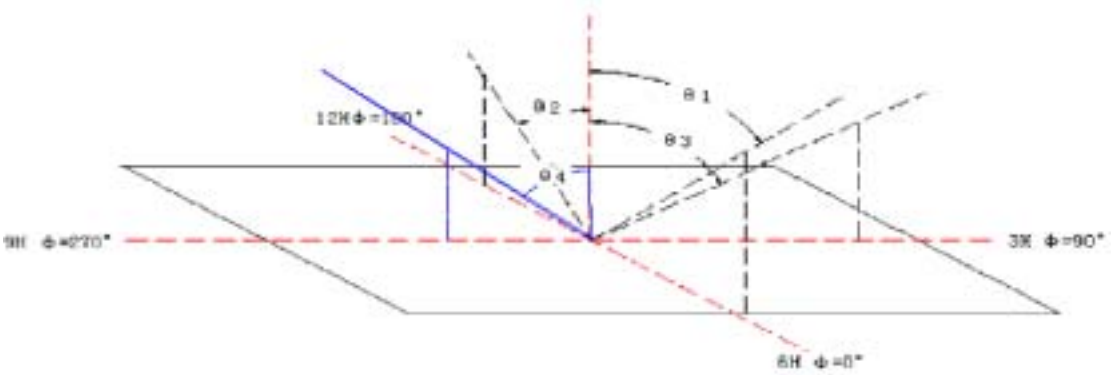
13.1 OPTICAL MEASUREMENT SYSTEM



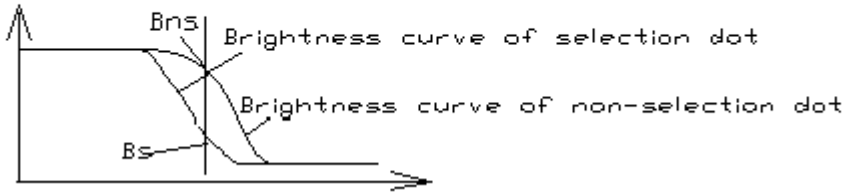
.DEFINITION OF θ AND Φ



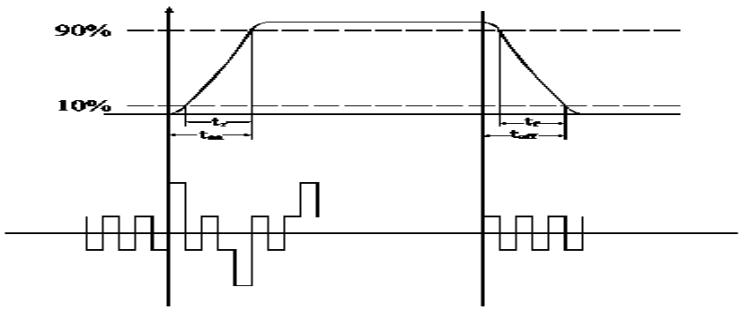
.DEFINITION OF CONTRAST RATIO Cr

DEFINITION:

$$Cr = \frac{\text{Brightness of non-selection dot (bns)}}{\text{Brightness of selection dot (bs)}}$$



.DEFINITION OF OPTICAL RESPONSE TIME



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