DATA SHEET

SUNPLUS

SPR1024A

128K x 8 Bits Bus Flash

OCT. 01, 2003

Version 1.2

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128Kx8 BITS BUS FLASH

1. GENERAL DESCRIPTION

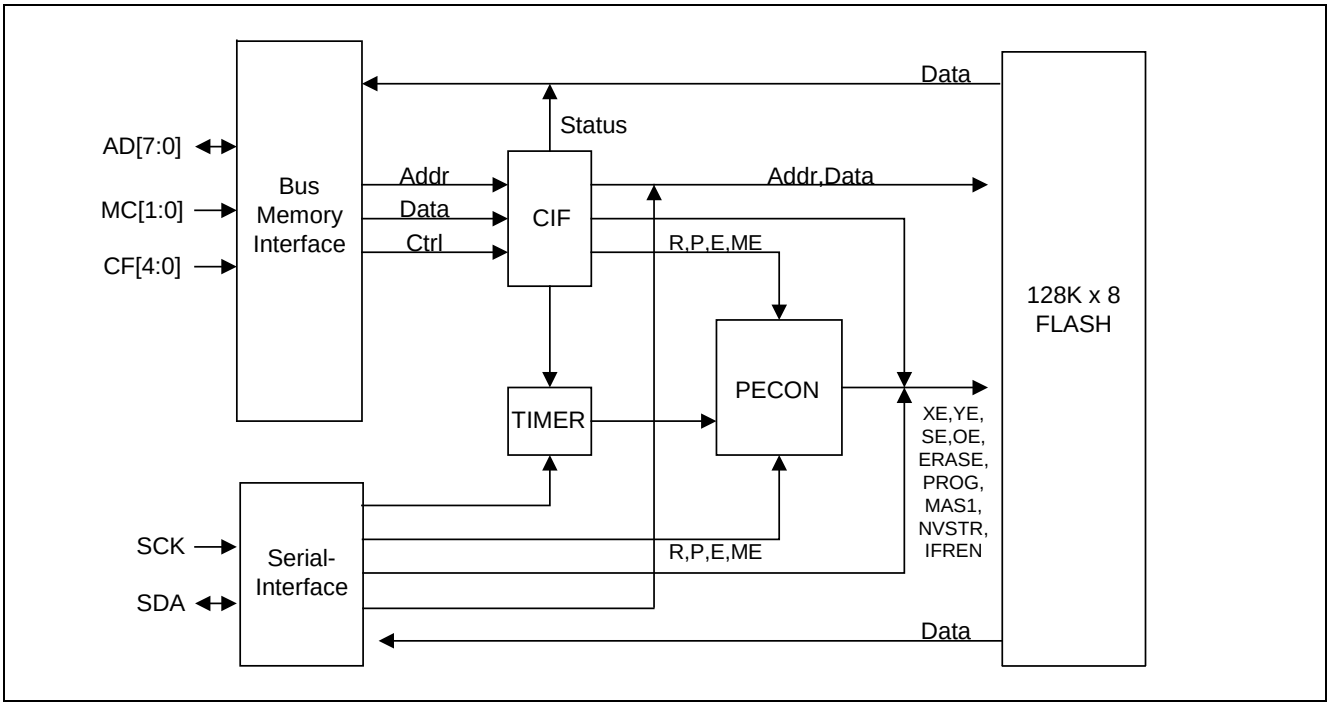
SPR1024A, a high-performance 1M-bit bus FLASH organized as 128K-byte, embeds a Bus Memory Interface (BMI) and a serial interface (SIF). SPR1024A allows SPL13X & SPLB3X MCU to access its FLASH memory via BUS memory or 1-bit serial interface. In 2.7V to 3.6V power, SPR1024A is able to operate up to 5.0MHz. Maximum current of read operation is 1.0mA and maximum current of program/erase is 4.0mA..

2. FEATURES

- 1M-bit (128K x 8 bits).
- Endurance: 20,000 Cycles (min)
- Data Retention: 10 years under Room Temperature
- 128 separate sectors for erase operation and 1K-byte per sector
- Working voltage: 2.7V - 3.6V
- Operating frequency: 5.0MHz
- Operating current: 1.0mA(max.) for read and 4.0mA (max.) for program/erase
- Standby current: 1.0μA (max.)
- TTL-compatible I/O
- Bus memory interface or serial interface
- DIP8 package

3. BLOCK DIAGRAM

This device contains six components - Bus Memory Interface (BMI), Serial Interface (SIF), Command Interface (CIF), timer, program & erase controller (PECON), and a 1M-bit FLASH. The CF[4:0] and SEL determine the device configuration. When BMI is selected, MC0 and MC1 behave as the Read/Write control signal and AD[7:0] are the bi-directional Address/Data bus. BMI executes these signals and generates chip enable ($\overline{CE}$), output enable ($\overline{OE}$), write enable ($\overline{WE}$), and FLASH memory address in READ mode. In WRITE mode, BMI also generates FLASH data. CIF interprets signals generated by BMI. If CIF receives READ command, it will perform read operation from FLASH directly. If CIF receives PROGRAM, ERASE or MASS ERASE, it forwards these commands to PECON to execute these commands. When SIF is chosen, SCK acts as serial clock and SDA as 1-bit serial I/O. If READ command is received, SIF will also read from flash memory directly. If PROGRAM, ERASE or MASS ERASE is received, SIF also forwards these commands to EPCON. When EPCON is active, it needs a 200 KHz clock, provided by the TIMER block shown in block diagram.



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
CF1 - 4 CF0	13 - 16 19	I	Configuration bonding option
AD0 - 7	2 – 9	I/O	Bus Interface Address/Data I/O
MC0 - 1	20 - 21	I	Bus Interface write/read control signal
SEL	23	I	Bus Interface/Serial Interface selection
$\overline{\text{RESET}}$	22	I	Reset (low active)
SDA	10	I/O	Serial Interface data I/O
SCK	18	I	Serial Interface Clock
VDD	1, 17	I	Power Supply (2.7V ~ 3.6V)
VSS	11	I	Ground
NC	0, 12	I	No connection

4.1. Ordering Information

Product Number	Package Type
SPR1024A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

5. FUNCTIONAL DESCRIPTIONS

5.1. Bus Memory Interface (BMI)

5.1.1. BMI description

In the use of Bus Memory Interface, pins are connected as table below:

Name	Description
CF0 - CF4	Configuration bonding option
AD0 - AD7	Bus Interface address/data I/O
MC0 - MC1	Bus Interface write/read control signal
SEL	Connected to GND
$\overline{\text{RESET}}$	Reset (low active)
SCK	Connected to GND
SDA	Connected to GND
VDD	Power supply (2.7V ~ 3.6V)
VSS	GND

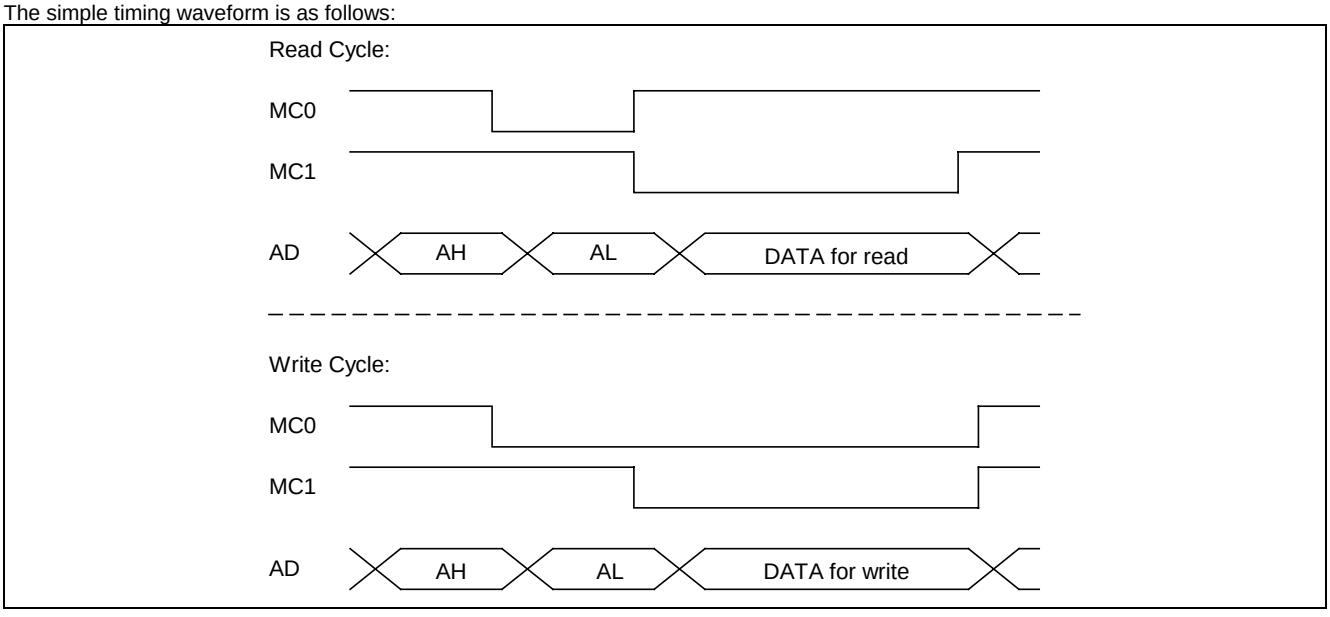
BMI, an interface between SPR1024A and SPL13X or SPLB3X MCU, is intended to provide flexible and efficient memory management. BMI contains an 8-bit bi-directional Address/Data bus, AD bus, which is multiplexed by two control signals - MC0 and MC1. MC0 determines operation mode (Read or Write), and MC1 decides AD bus to be address or data bus. See the following table for MC0 and MC1 configuration.

MC1	MC0	AD BUS
L	L	Data for Write
L	H	Data for Read
H	L	AL
H	H	AH

AH: high byte address

AL: low byte address.

The simple timing waveform is as follows:



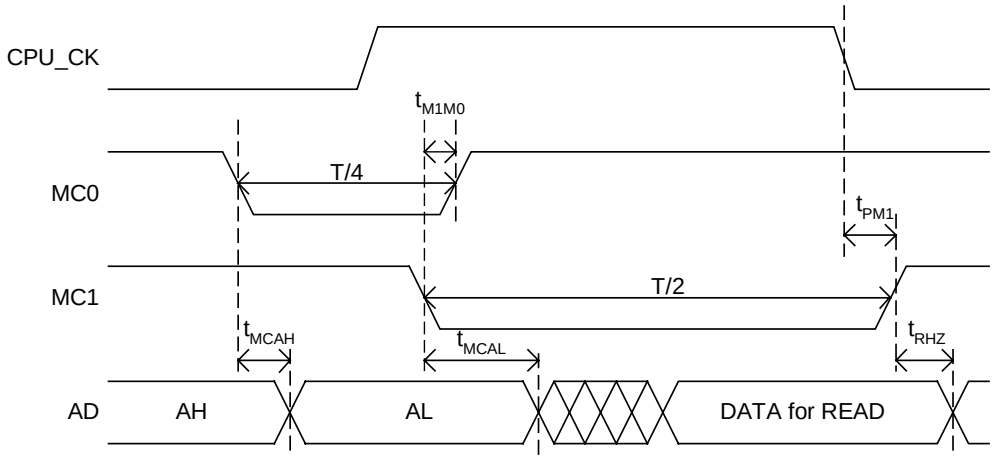
MC0 falling edge => latch AH.

MC1 falling edge => (1) latch AL. (2) if MC0=1→ READ; if MC0=0 → WRITE.

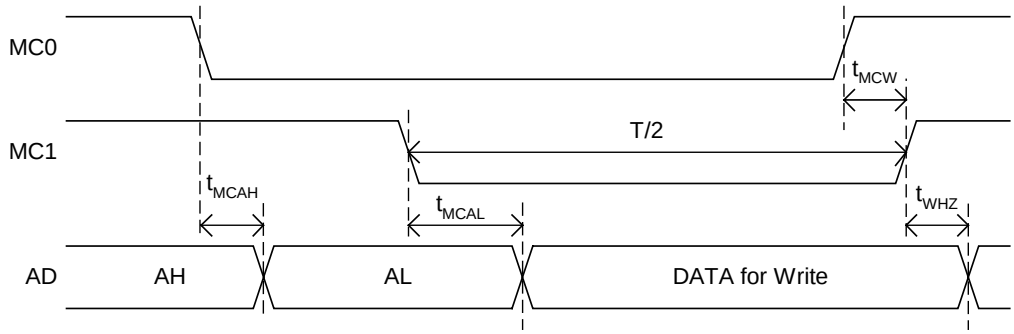
MC1 rising edge => if READ, set AD bus to Hi. If WRITE, latch DATA for WRITE.

5.1.2. BMI AC characteristics

Read Cycle



Write Cycle



5.1.3. AC characteristics (VDD = 2.7V - 3.6V, T_A = 0 - 70℃)

Characteristic	Symbol	Min.	Max.	Unit
Read cycle				
Read cycle period	T	250	-	ns
MC0 falling to AH end	t_{MCAH}	15	-	ns
MC1 falling to MC0 rising	t_{M1M0}	-20	10	ns
MC1 falling to AL end	t_{MCAL}	-	35	ns
Data latch to MC1 falling	t_{PM1}	20	35	ns
MC1 rising to AD Hi-Z	t_{RHZ}	-	5.0	ns
Write Cycle				
MC0 rising to MC1 rising	t_{MCW}	15	20	ns
MC1 rising to AD Hi-Z	t_{RHZ}	15	-	ns

5.1.4. BMI configuration setting

The Bus Memory Interface (BMI) has four modes - A, C, E, and G. The configuration settings are illustrated in the CF[2:0], where CF indicates the physical pin, see Table 1. For the physical pins, simply apply logic high (1) or low (0) to the pins to participate the settings. Moreover, the CF[4:3] determines the bank control register ($00) configuration, see the Table 2 for detailed setups. Note that the change of bank is accomplished by given the corresponding value to the $00. For example, to access the Bank0, a value of “00h” must be given to $00 in addition to a logic value of “00” should be given to the external pins, CF[4:3].

Table 1: CF[2:0], configuration of BMI mode

BMI Type	CF2	CF1	CF0	Volume ID $0D[1:0]
A	0	0	0	00
C	0	1	0	01
E	1	0	0	xx
G	1	1	0	01

Table 2: CF[4:3], configuration of bank setting. “b” is for extender memory bank select.

Type	CF4	CF3	Bank switch
A, C, E	0	0	00XXXXbb
	0	1	01XXXXbb
	1	0	10XXXXbb
	1	1	11XXXXbb
G	1	0	10XXXXbb
	1	1	11XXXXbb

5.1.5. BMI register description

The BMI uses MCU address from 4000h to FFFFh and duplicates some registers of SPL13X and SPLB3X into SPR1024A as bank switch. The register usage and mapping table is as below:

1). Memory Bank Switch ($00, BSW)

b7	b6	b5	b4	b3	b2	b1	b0
*	*	-	-	-	-	BSW1	BSW0

* $00[7:6] must be set the same value as the logic setting of CF[4:3].

2). Volume ID ($0D, VOL)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	VOL1	VOL0

3). External Memory Mapping ($0B.1, EXC)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	EXC	-

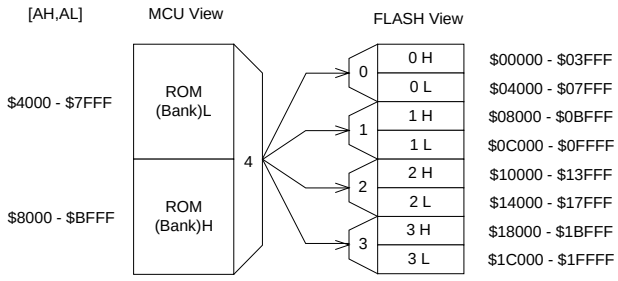
MCU address mapping of $C000 - $FFFF

b1: EXC = 0: Map to internal ROM

= 1: Map to external Bus Flash

Note: SUNPLUS recommends always keep this bit to “0” when bus flash is applied.

5.1.6. BMI memory mapping



5.1.7. BMI command sequence

5.1.7.1. Bus memory interface command sequence

Command sequence	Bus cycle											
	1st		2nd		3rd		4th		5th		6th	
	addr	data	addr	data	addr	data	addr	data			addr	data
Read device ID	5555h	AAh	AAAAh	55h	5555h	90h	8000h/ 8001h	ID (read)				
Read status	5555h	AAh	AAAAh	55h	5555h	70h	Any addr.	Status(1)				
Return to normal mode (RESET)	XXXX	F0h										
Read	RA	RD (read)										
Byte program	5555h	AAh	AAAAh	55h	5555h	A0h	PA(2)	PD(3)				
Sector Erase	5555h	AAh	AAAAh	55h	5555h	80h	5555h	AAh	AAAAh	55h	EA(4)	30h
Mass erase	5555h	AAh	AAAAh	55h	5555h	88h	5555h	AAh	AAAAh	55h	5555h	10h

Note1: Status: b7 for 0/1: busy/ready, b3 for 0/1: fail/success

Note2: PA: program byte address

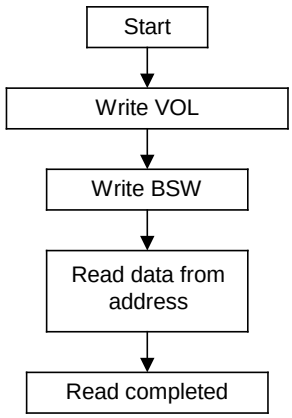
Note3: PD: program data

Note4: EA: sector erase address (gray bits in next table)

5.1.7.2. Read device ID command output

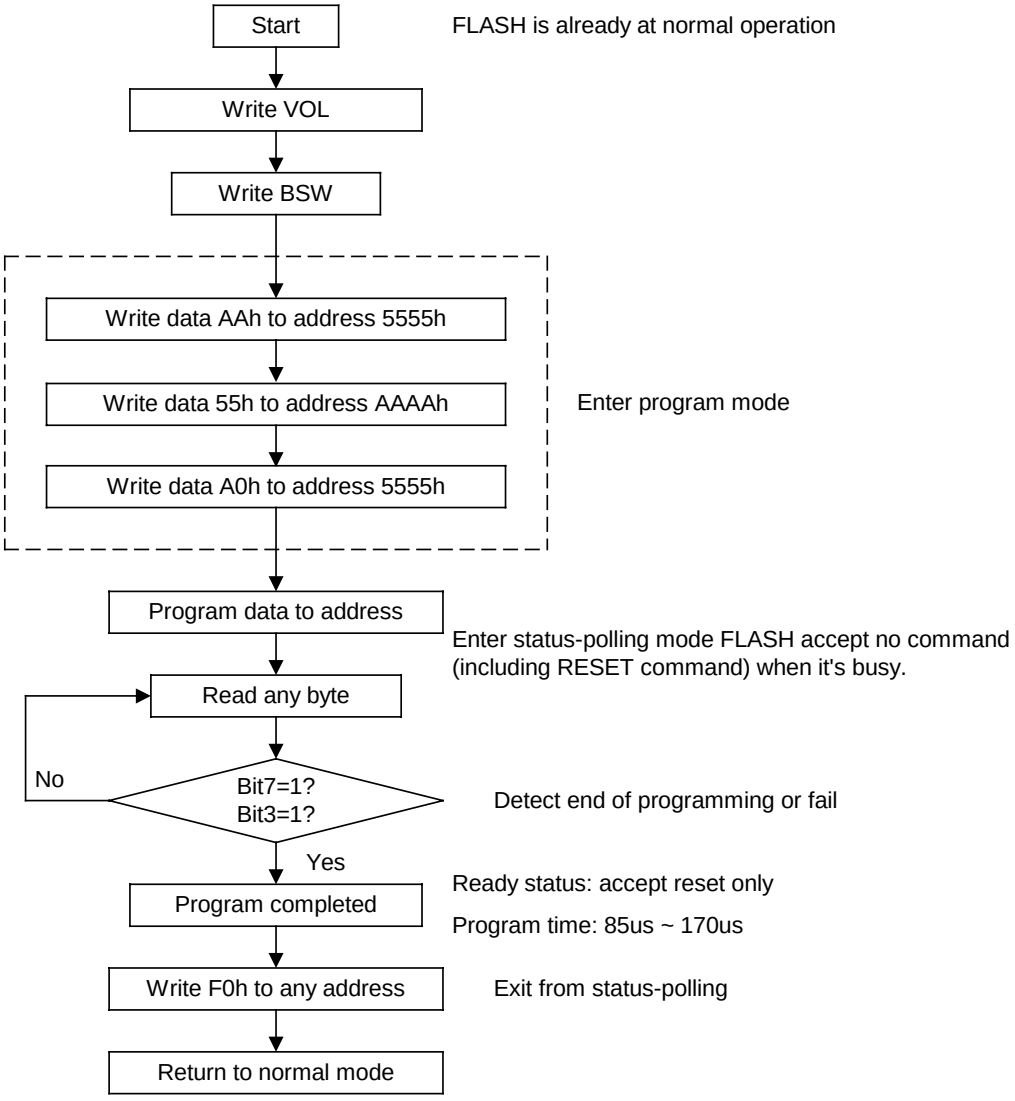
	Address	Data
Manufacture code	00000h	C7h
Device code	00001h	D5h

5.1.7.3. BMI read command sequence

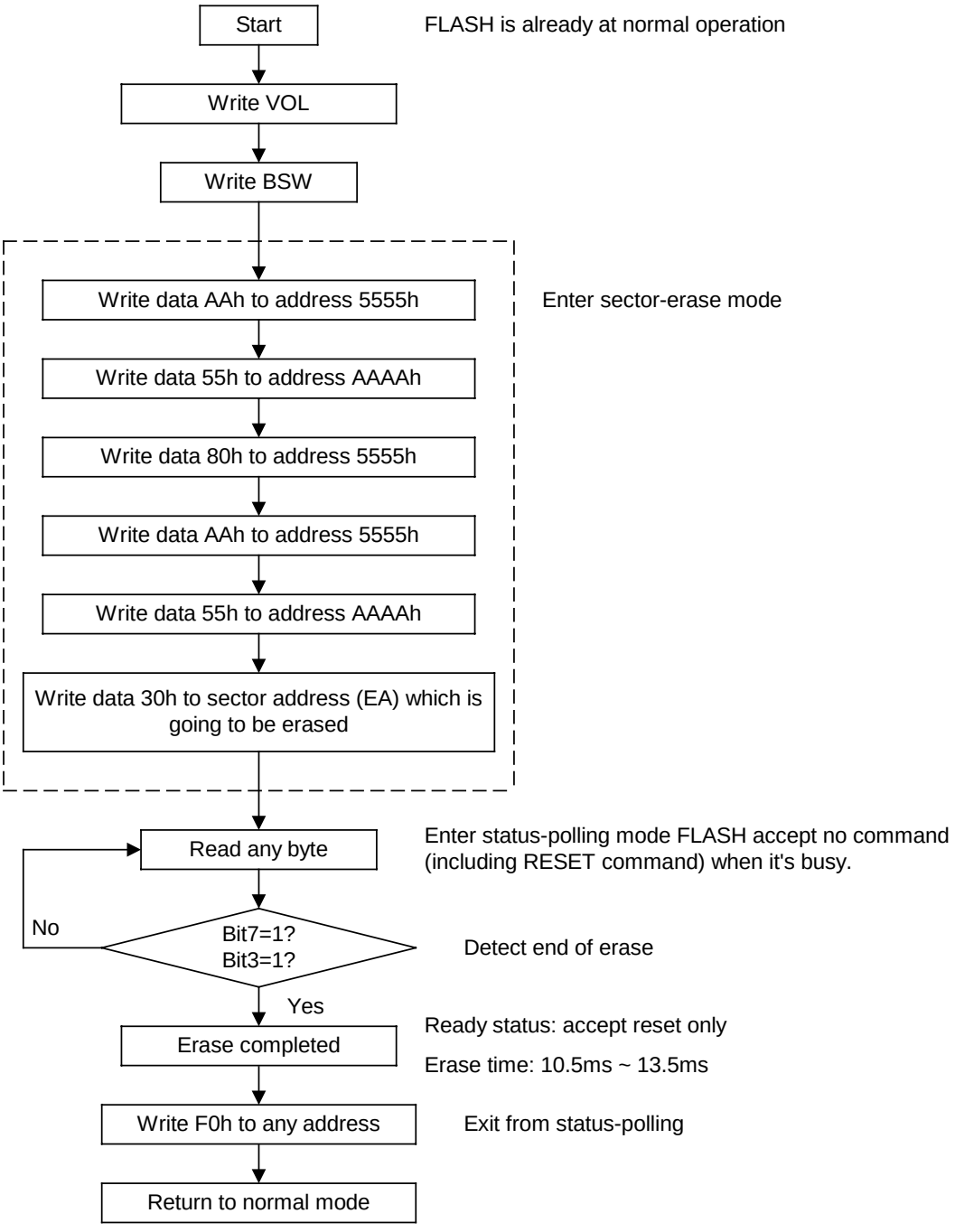


FLASH is already at normal operation

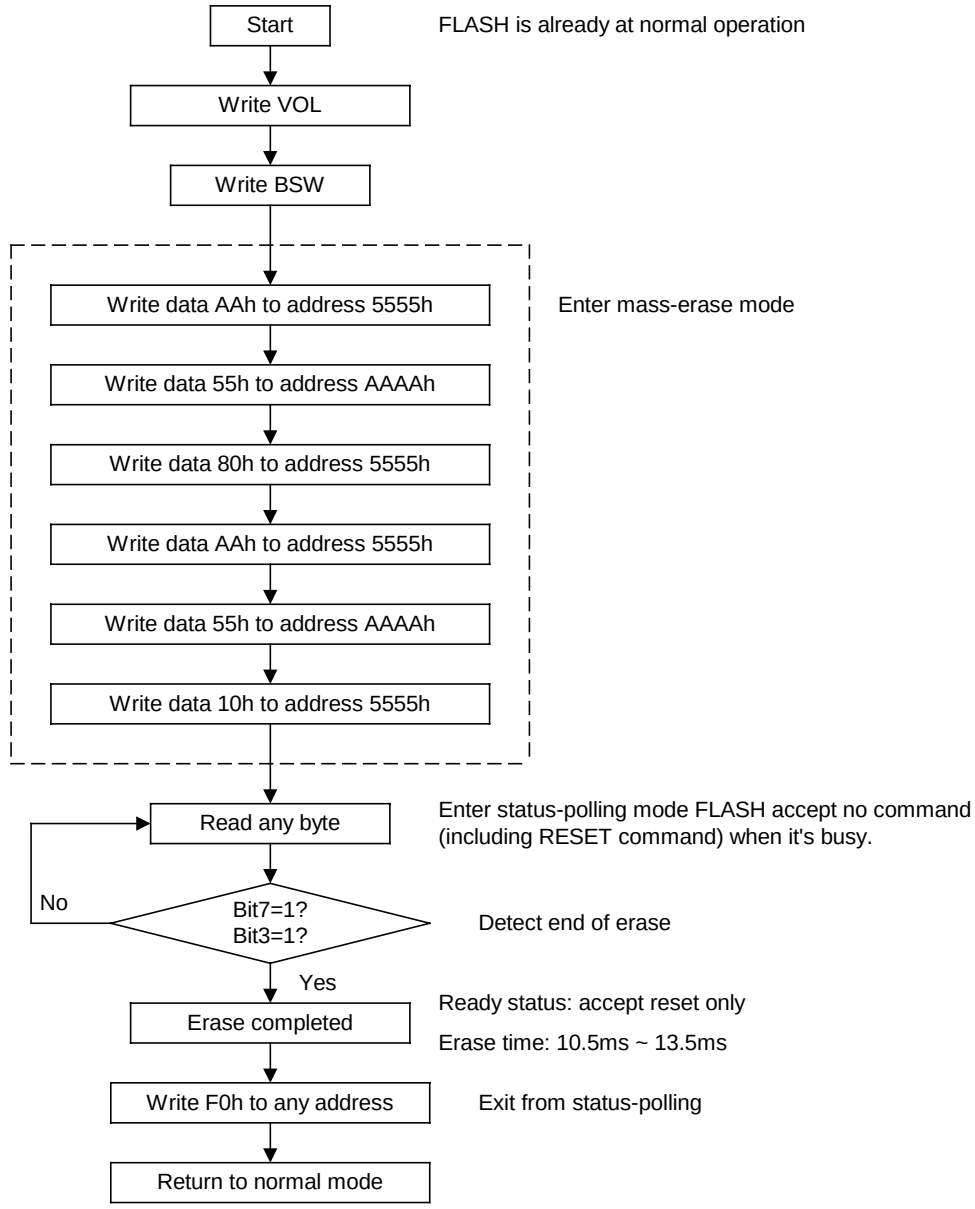
5.1.7.4. BMI byte program command sequence



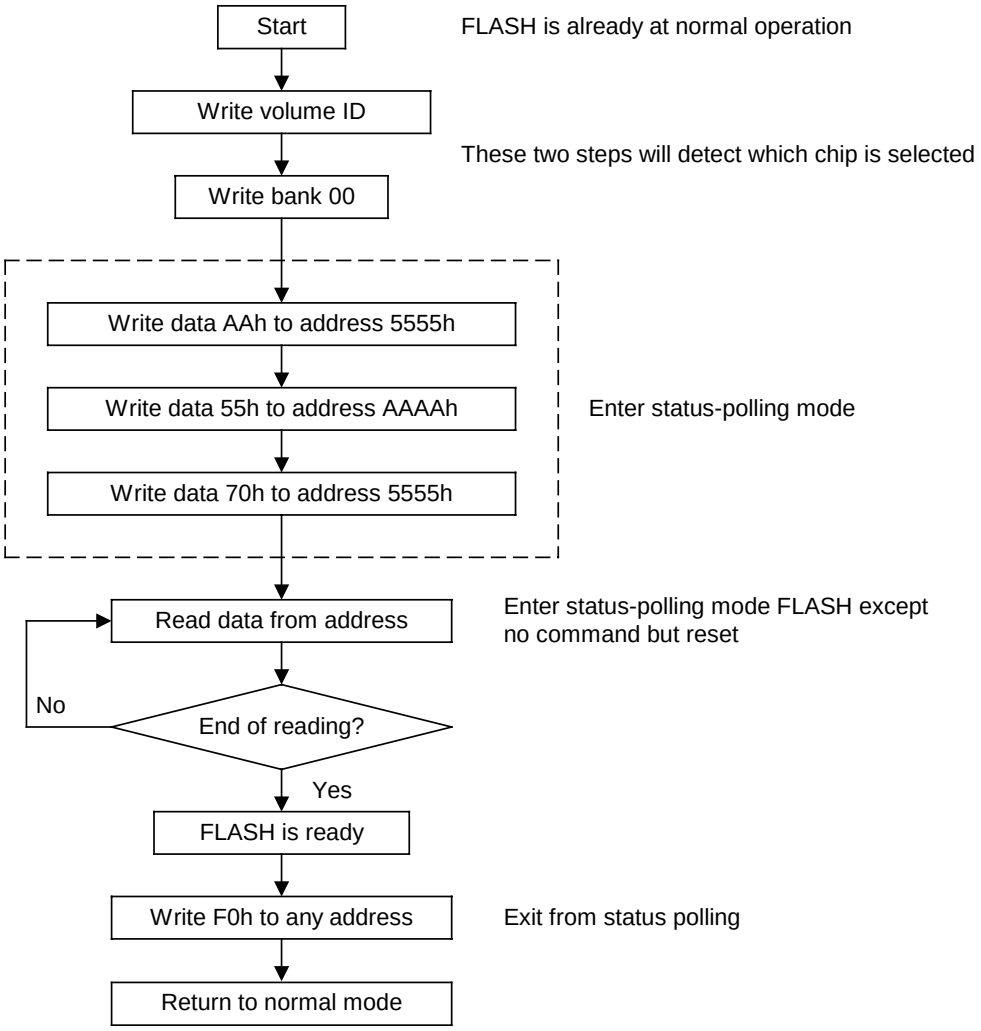
5.1.7.5. BMI sector erase (1K byte) command sequence



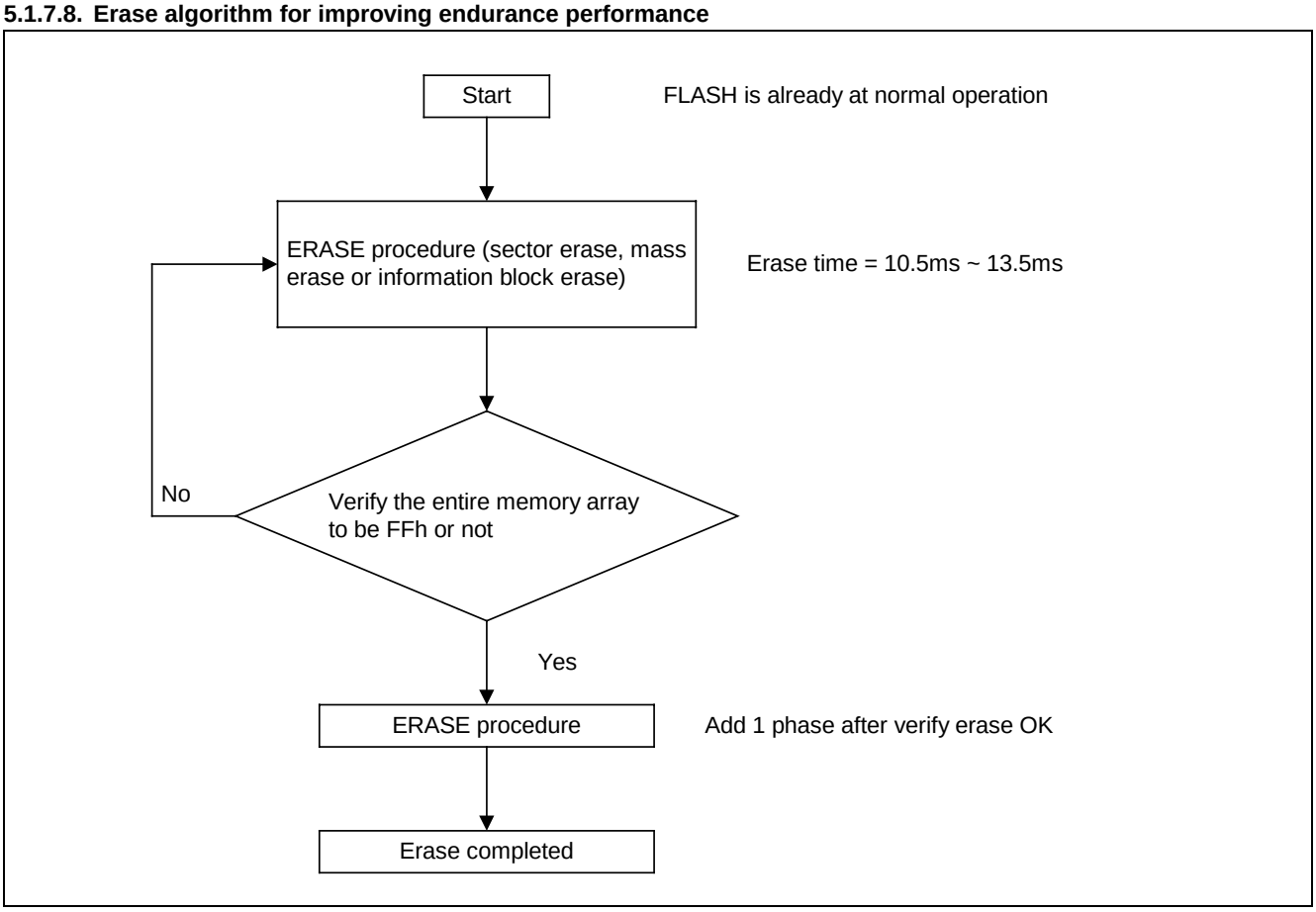
5.1.7.6. BMI mass erase command sequence



5.1.7.7. Enter status-polling mode from normal mode



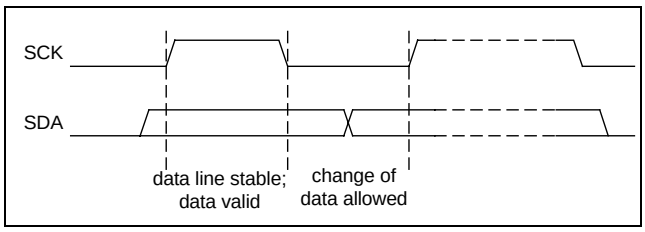
5.1.7.8. Erase algorithm for improving endurance performance



5.2. Serial Interface (SIF)

When using serial Interface, pins are connected as table below:

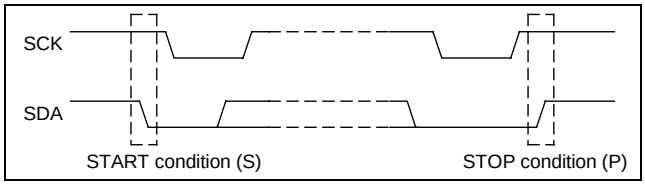
Name	Description
CF0 - CF4	NC
AD0 - AD7	NC
MC0 - MC1	NC
SEL	Connected to VDD
$\overline{\text{RESET}}$	Reset (low active)
SCK	Serial clock
SDA	Serial data I/O
VDD	Power supply (2.7V ~ 3.6V)
VSS	GND



Within the procedure of the SUNPLUS Serial Interface, unique situation arises for START (S) and STOP (P) conditions. A HIGH to LOW transition on SDA line while SCK is HIGH indicates a START condition. A LOW to HIGH transition on SDA line while SCK is HIGH means STOP condition.

5.2.1. Bit transfer

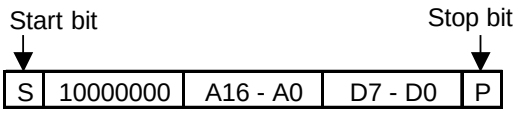
One clock pulse is generated for each data bit transmission. The data on SDA line must be stable during the HIGH clock period. The HIGH or LOW on the data line can only be changed when the clock signal on the SCK line is LOW.



5.2.2. Instruction set

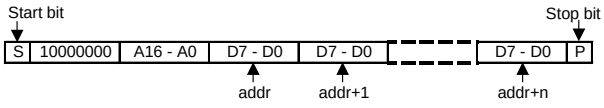
1). READ with random address access:

READ command is a start bit followed by an 8-bit opcode (A[24:17]=10000000) and a 17-bit address (A[16:0]). After receiving READ command, the SDA line should be set to the high-impedance state. SPR1024A will begin shifting out the data address (MSB first) at the falling edge of the SCK clock and the output data bit will be stable after certain time delay (t_{ACC}). After 8 data bits are shifted out, a stop bit is needed to terminate the command.



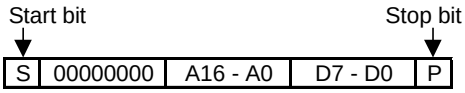
2). READ with auto-address-count:

READ with auto-address-count command is the same as READ except that after first 8 data bits are shifted out, no stop bit is inserted before the next SCK falling edge. SPR1024A will automatically increase the address by 1 and its data content will be shifted out, preceded by the clock cycle. The procedure will continue until a stop bit is received.



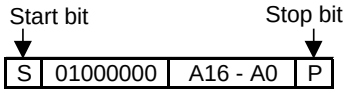
3). Byte program:

BYTE PROGRAM command is a start bit followed by an 8-bit opcode (A[24:17]=00000000), a 17-bit address (A[16:0]) and an 8-bit data (D[7:0]). After receiving BYTE PROGRAM command, a specified interval (t_{PGM}) is needed to program data into FLASH. After all, a stop bit terminates the command.



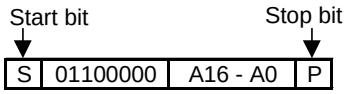
4). Sector erase:

SECTOR ERASE command is a start bit followed by an 8-bit opcode (A[24:17]=01000000) and a 17-bit address (A[16:0]). A16 to A10 are used to identify which sector to be erased. A9 to A0 are DON'T CARE. After receiving SECTOR ERASE command, a specified interval (t_{ERASE}) is needed to erase the selected sector in the FLASH. Finally, a stop bit terminates the command.



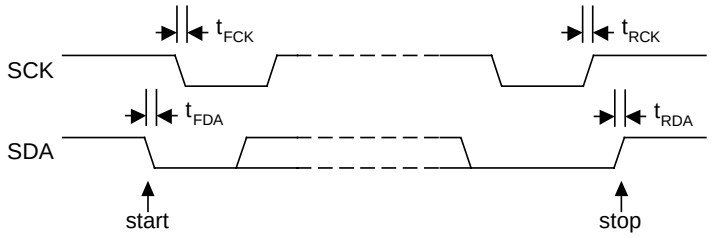
5). Mass erase:

MASS ERASE command is a start bit followed by an 8-bit opcode (A[24:17]=01100000) and a 17-bit address (A[16:0]). A16 to A0 are DON'T CARE. After receiving MASS ERASE command, a specified interval (t_{ERASE}) is needed to erase the main block in the FLASH. Then, a stop bit terminates the command.

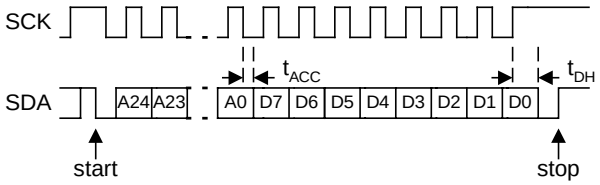


5.2.3. AC characteristics (VDD = 2.7 - 3.6V, T_A = 0 - 70℃)

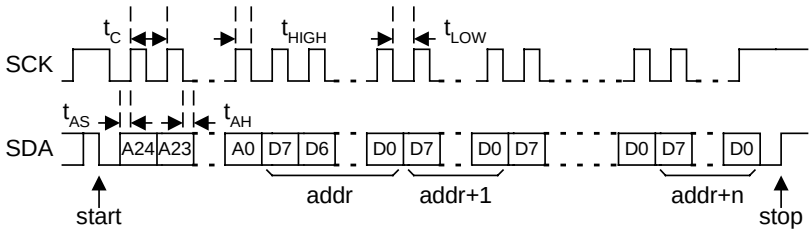
Characteristic	Symbol	Max.	Min.	Unit
Period of SCK	t_C	-	400	ns
Low period of SCK clock	t_{LOW}	-	170	ns
High period of SCK clock	t_{HIGH}	-	170	ns
Address setup time	t_{AS}	-	100	ns
Address hold time	t_{AH}	-	20	ns
READ access time	t_{ACC}	100	-	ns
READ data hold time	t_{DH}	-	20	ns
PROGRAM data setup time	t_{PDS}	-	100	ns
PROGRAM data hold time	t_{PDH}	-	20	ns
PROGRAM time	t_{PGM}	-	125	us
ERASE time	t_{ERASE}	-	13.5	ms
Rise time of SCK	t_{RCK}	15	-	ns
Fall time of SCK	t_{FCK}	15	-	ns
Rise time of SDA	t_{RDA}	15	-	ns
Fall time of SDA	t_{FDA}	15	-	ns



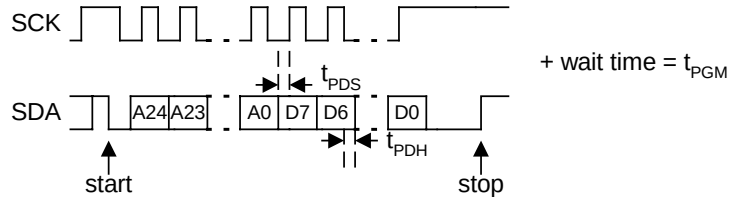
1). Read command



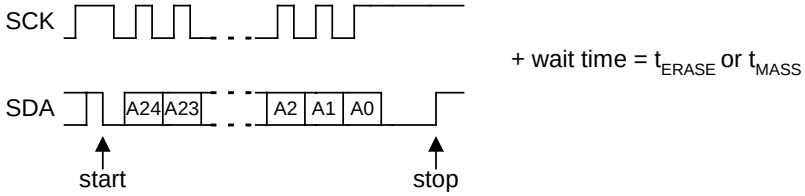
2). Read command with auto-address-count



3). Program command



4). Sector erase and mass erase command



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings*

Characteristics	Symbol	Ratings
Supply Voltage to Ground Potential	VDD	-0.5V ~ 4.5V
Ambient Operating Temperature	T_A	-10℃ ~ 80℃
Storage Temperature	T_{STG}	-65℃ ~ 150℃
Output Voltage	V_{OUT}	-0.5V ~ VDD+0.5V
Input Voltage	V_{IN}	-0.5V ~ VDD+0.5V

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

6.2. Recommended DC Operating Conditions (VDD =2.7V - 3.6V, T_A = 0 - 70℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Supply Voltage	VDD	2.7	3.0	3.6	V
Supply Voltage	VSS	-	0	-	V
Input High Voltage	V_{IH}	2.2	-	VDD+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.4	V

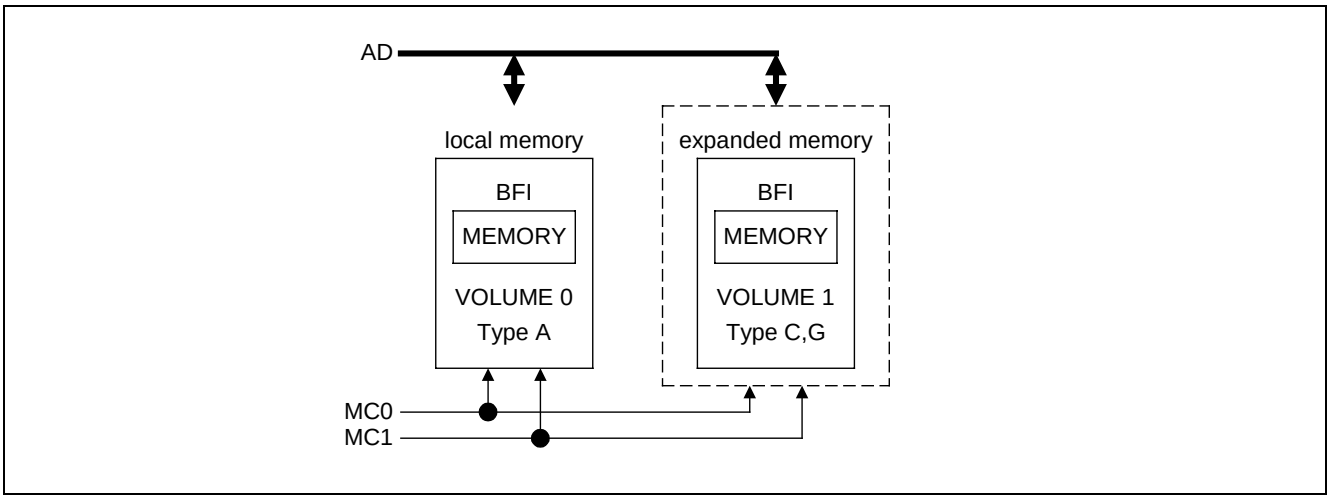
6.3. DC Characteristics (VDD = 2.7V - 3.6V, T_A = 0 - 70℃)

Characteristic	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	2.3	-	-	V	I_{OH} = -1.0mA
Output Low Voltage	V_{OL}	-	-	0.3	V	I_{OL} = 1.0mA
Input Leakage Current	$I_{I(L)}$	-	-	1.0	A	
Output Leakage Current	$I_{O(L)}$	-	-	1.0	A	
Operating Supply Current (f = 4.0MHz), C_L = 80pF	I_{CC}	-	-	4.0	mA	
Standby Current (CMOS)	I_{SB}	-	-	1.0	uA	MC0 = MC1 = VDD AD[0:7] = VSS

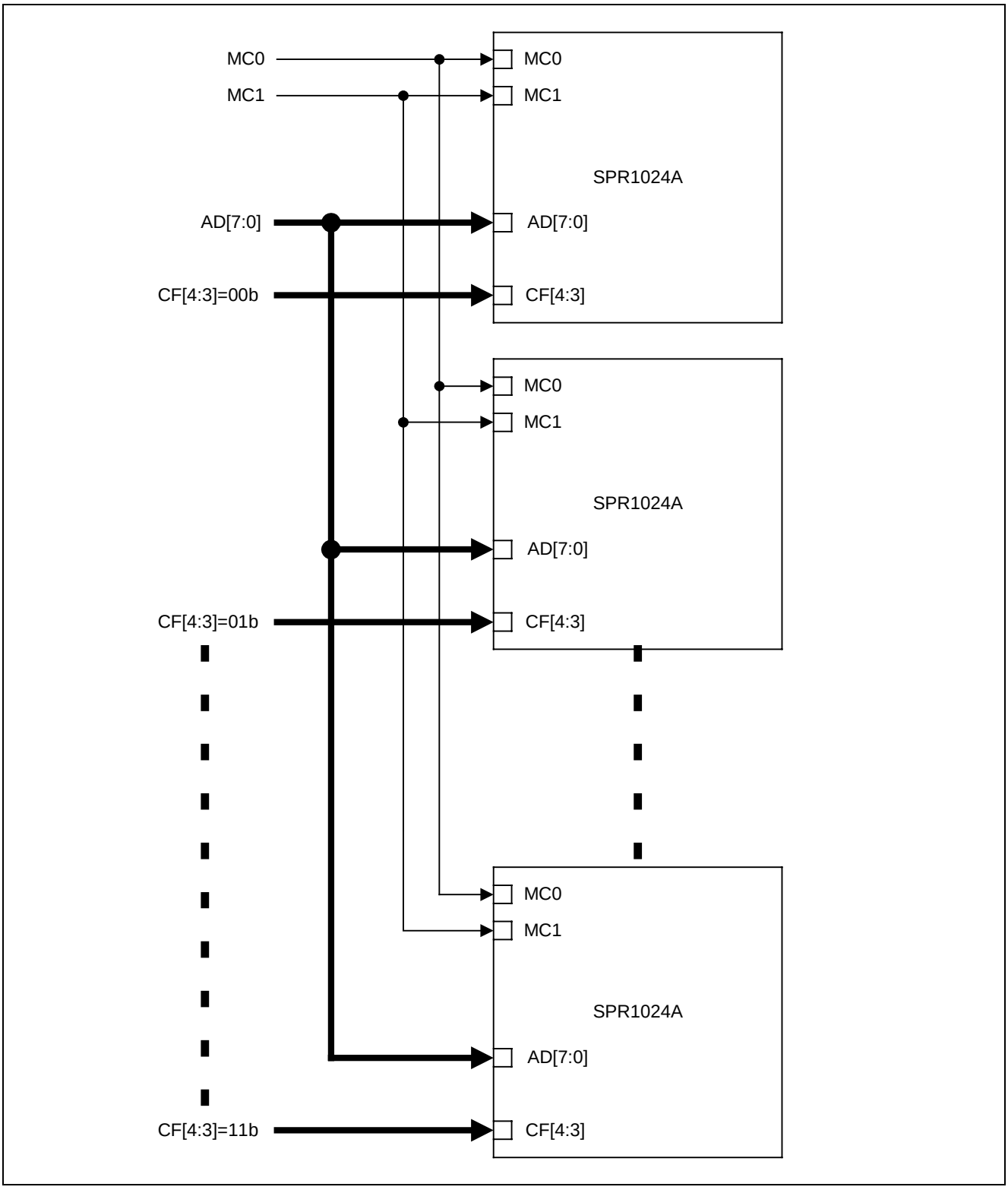
7. APPLICATION CIRCUITS

7.1. BMI Cascade Access Mode

To expand memory in SPR1024A, a cascade access mode is designed to identify local memory and expanded memory. It is defined by the configuration control signal, mentioned in the previous section. For old version of SPL series, it is recommended to expand only to volume 1 (The built-in volume ID is fixed to 1 for Type C and Type G).



7.2. Bus Interface



8. PACKAGE/PAD LOCATIONS

8.1 DIP8

PIN No.	PAD Name
1	NC
2	VDD
3	SDA
4	VSS
5	VDD
6	SCK
7	$\overline{\text{RESET}}$
8	SEL

Please contact Sunplus sales representatives for more information.

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 01, 2003	1.2	Add two items: “Endurance: 20,000 Cycles (min)” and “Data Retention: 10 years under Room Temperature” in “*2. FEATURES*”	3
MAR. 12, 2003	1.1	Delete “*8. PACKAGE/PAD LOCATIONS*”	20 - 21
DEC. 20, 2002	1.0	To enhance BMI memory mapping description and remove some confusing tables.	23
AUG. 2, 2000	0.1	Original	30