DATA SHEET

SUNPLUS

SPL10A2

7KB LCD Controller/Driver

JAN. 12, 2004

Version 1.5

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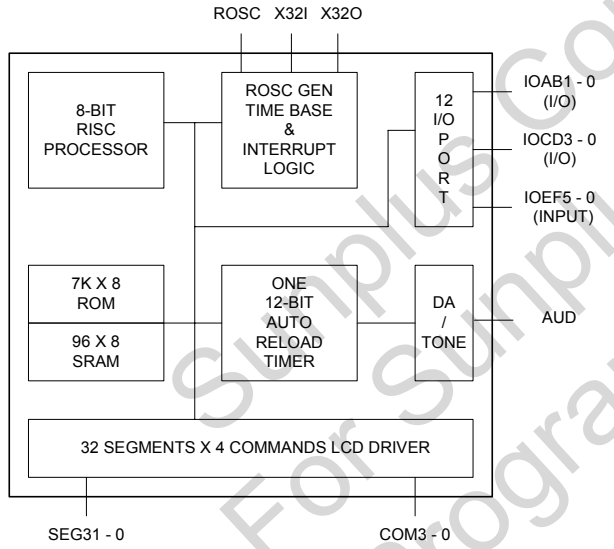
7KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPL10A2 is a CMOS 8-bit single chip micro-controller which contains LCD drivers, ROM, SRAM, I/O, timer/counter and audio output on a single chip. The SPL10A2 is designed to drive LCD directly and performs efficient controller function as well as arithmetic function. With the on chip crystal oscillator, the real time clock is easily realized. For power saving, a software controllable standby switch is also built-in. The SPL10A2 is widely used in electronic products requiring very low power consumption, for example, multi-function watch, calendar, calculator, thermometer or LCD game with audio output.

2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit CPU
- Operating voltage: 2.4V to 5.5V
- Max. CPU clock: 2.0MHz @ 3.0V
- ROM capacity: 7K x 8 bits
- RAM capacity: 96 x 8 bits
- Direct Driver for LCD: 4 Commons X 32 Segments (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
- Input Port: 6 input pins with key wakeup function with 4 different configurations (mask option)
- I/O Port: 2 general purpose I/O pins and 4 special purpose I/O pins that can implement thermometer
- Timer/Counter: one 12-bit timer/counter
- 6 Interrupt sources:
  . External Interrupt
  . Timer Interrupt
  . 2 KHz Interrupt
  . LCD Service Interrupt (in LCD share mode)
  . 128Hz Interrupt
  . 2Hz Interrupt
- Dual Clock System: One built-in RC oscillator (only one resistor is needed) for CPU and one built-in crystal oscillator or RC oscillator (mask option) for LCD scanning.
- Audio or Tone Output: One 7-bit current DA for playing melody/ speech or Tone output for playing melody
- System Reset: External Reset, Watch Dog Reset and Low Voltage Reset are built-in
- Low Operating Current:
  Typical current < 3μA @ 3.0V for timepiece products

Note: Patent Circuit Included.
Taiwan Patent No. 68824.

4. SIGNAL DESCRIPTIONS

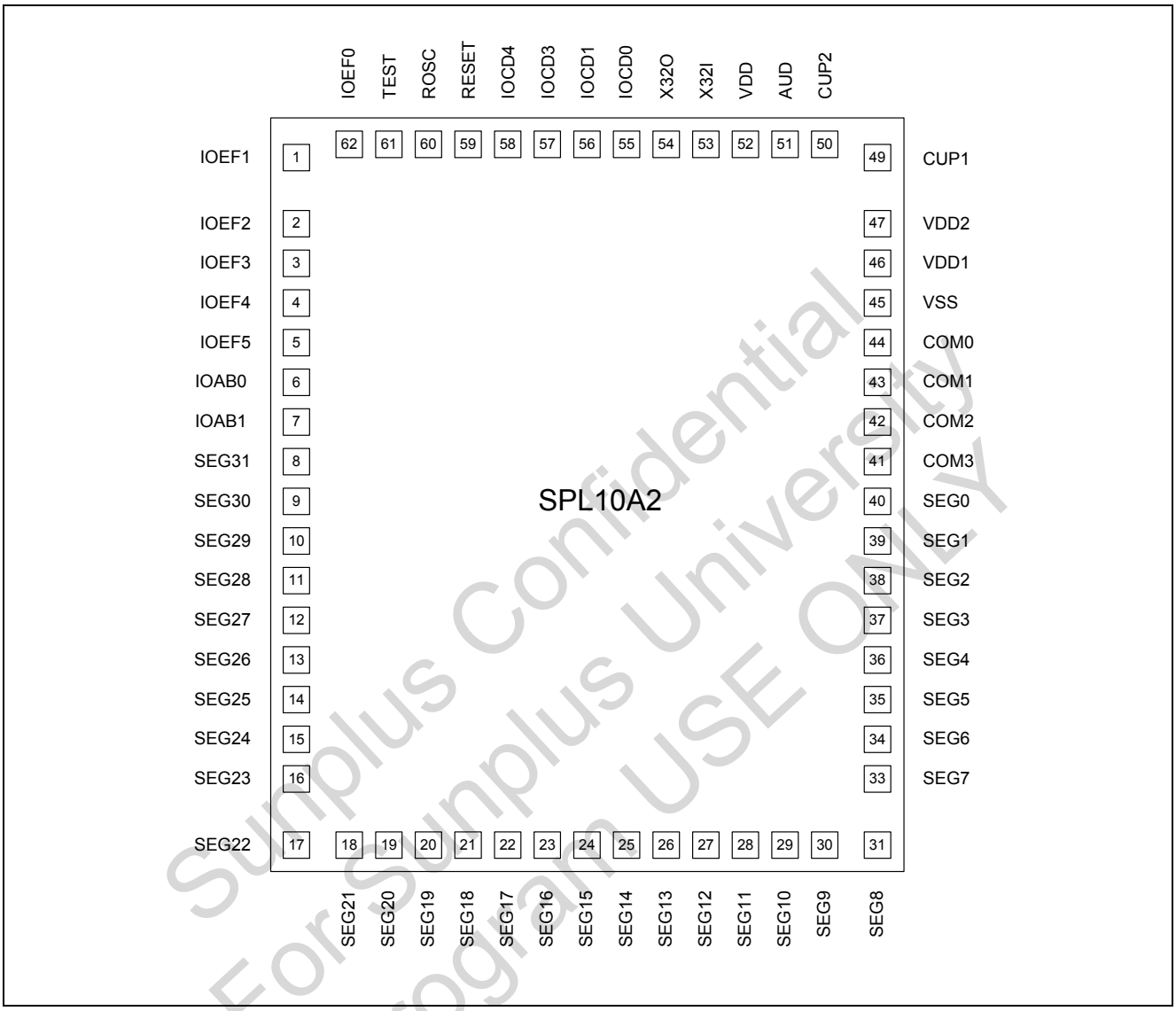
Mnemonic	PIN No.	Type	Description
SEG31 - 0	8 - 39	O	LCD driver segment output
COM3 - 0	40 - 43	O	LCD driver common output
IOAB1 - 0	7 - 6	I/O	I/O port
IOEF5 - 1 IOEF0	5 - 1 60	I	INPUT port (also for key wake-up input)
IOCD3 - 0	56 - 53	I/O	I/O port
ROSC	58	I	R-osc input, connect to VDD through a resistor
RESET	57	I	External reset input
AUD	49	O	Current DA output /Tone output
X32I	51	I	32.768KHz crystal input/R oscillator input
X32O	52	O	32.768KHz crystal output
TEST	59	I	Test input
VDD	50	I	Power input
VSS	44	I	Ground input
VDD1	45	I	Inputs for setting LCD bias
VDD2	46	I	Inputs for setting LCD bias
CUP1	47	I	Input for maintaining 1/3 Bias LCD
CUP2	48	I	Input for maintaining 1/3 Bias LCD

4.1. Ordering Information

Product Number	Package Type
SPL10A2-NnnV-C	Chip form
SPL10A2-NnnV-PL02	Package form - LQFP 64

Note1: Code number is assigned for customer.
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

4.2. PIN Map



64 pin LQFP package

5. FUNCTION DESCRIPTIONS

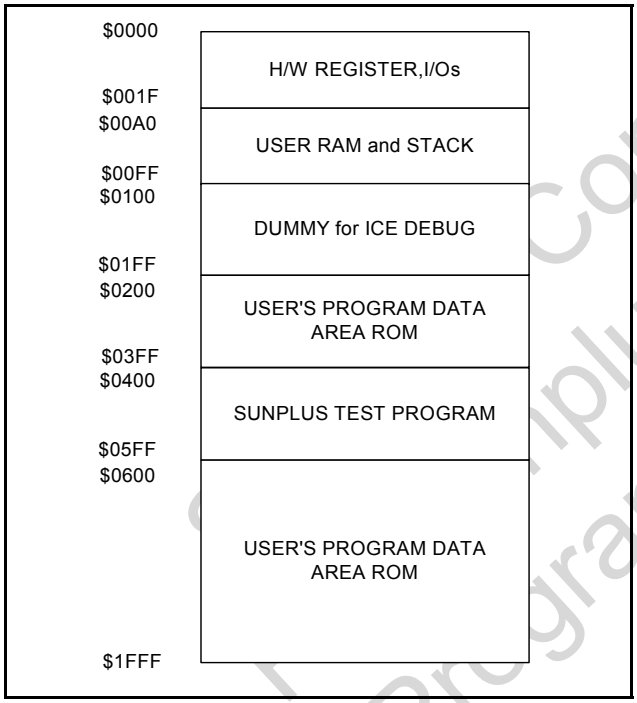
5.1. ROM

The SPL10A2 provides 7.5K bytes ROM size. The users have 7K bytes for program and data. The other 0.5K bytes are for SUPLUS internal test use. The ROM address is from $0200 to $1FFF.

5.2. RAM

The SPL10A2 provides 96 bytes RAM. The RAM is for both stack and data storage. The RAM address is from $00A0 to $00FF.

5.3. Memory and I/O Map

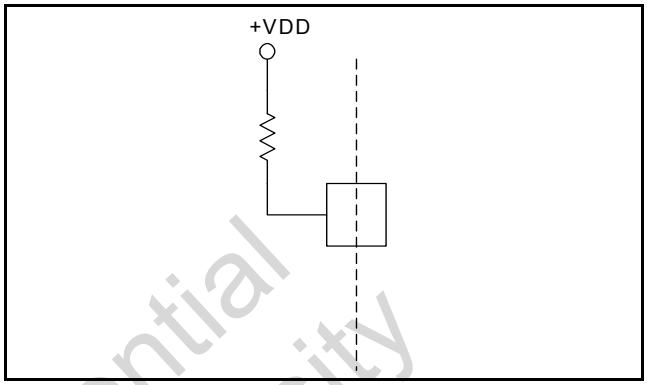


5.4. Oscillators

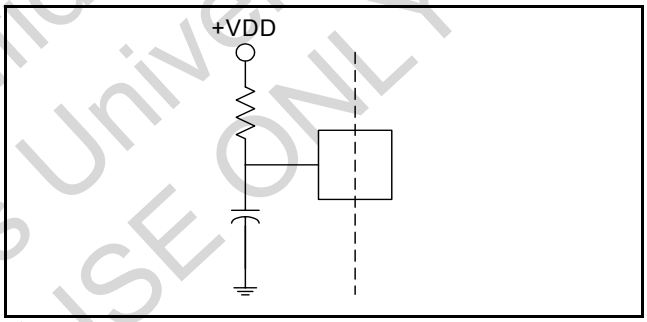
The SPL10A2 is a dual clock system. One clock is for the CPU and system and the other is for the LCD scanning and interrupt sources.

5.4.1. R oscillator for the CPU and system clock

5.4.1.1. Normal case

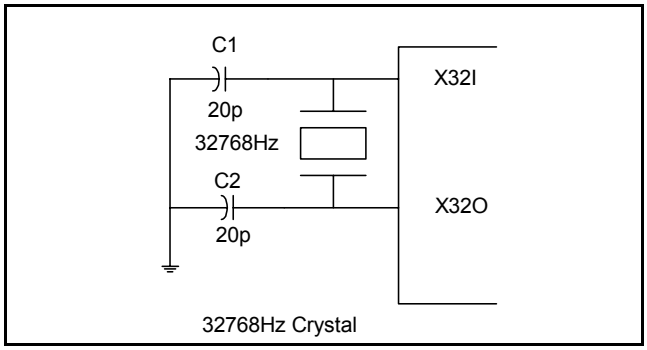


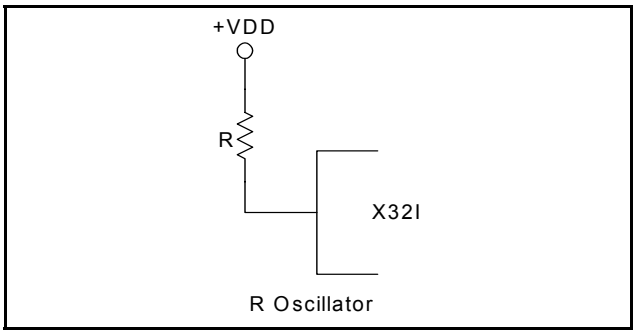
5.4.1.2. Noise environment



Note: Length of the wiring for ROSC pin should be minimized because the oscillator frequency varies due to coupling from other signal lines.

32768Hz crystal oscillator or R oscillator (mask option) for LCD scanning and interrupt sources (2KHz, LCDL for LCD service, 128Hz, 2Hz). It is suggested to enable 32768Hz crystal in strong mode for a few seconds and then switch to weak mode when reset occurs.





Note: Length of the wiring for X32I and X32O should be as short as possible.

5.5. Stop Clock Mode

The SPL10A2 supports the power saving mode for those applications needing very low standby current. The user can simply enable the wake-up sources then stop the CPU clock by writing the STOP CLOCK register ($09). The CPU will go to stand-by and the RAM and I/O remain their previous states until wake-up. There are three sources of wake-up in this chip, PORT IOEF wake-up, TIMER 0 wake-up and 2 Hz wake-up. After the chip being waken up, the internal CPU will go to the next instruction and the RAM and I/O are not affected by the wake-up reset. The standby current of timepiece product typically is less than 3 μA @ 3.0V by using this mode and 32768Hz clock source in weak mode.

For non-timepiece products, 32768Hz crystal driver or R oscillator (mask option) that generates the 32768Hz clock source also can be turned off to stop the chip operation. The standby current of the SPL10A2 is less than 1 μA @ 3.0V. In this mode, IOEF port can be used to wake up the chip.

5.6. Timer/Counter

The SPL10A2 contains one 12-bit timer/counter, TM0. In timer mode, TM0 is reloadable up-counter. When timer overflows from 0FFF to 0000, the carry signal will generate the INTERRUPT signal if the corresponding bit is enabled in INT ENABLE register ($0D), and the timer will be auto reloaded to the user's setup value and upcount again. If TM0 being specified as a counter, the user may reset the counter by loading 0 into register $14 and $1C. After the counter being activated, the count value can also be read from above registers on-the-fly, the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter are selectable as the following:

Timer/Counter		Addr.	Clock source
TM0	12 BIT TIMER	$0014 $001C	CPU CLOCK (T) or T/4
	12 BIT COUNTER	$0014 $001C	T/128, T/256, T/2048 or EXT CLK
MODE SELECT REGISTER		$000B	Select TM0 timer or counter
TIMER CLOCK SELECTOR		$001C	Select T or T/4

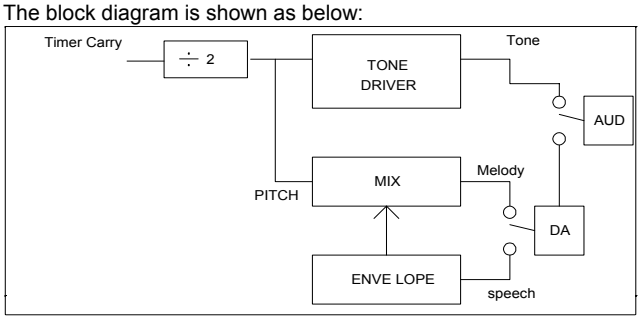
5.7. Interrupts

The SPL10A2 has six interrupt sources. They are INT0 (interrupt fromTIMER 0), 2 KHz INT, LCDL INT (LCD service in share mode, due to LCD registers is shared with the TIMER/COUNTER), 128 Hz INT, EXT INT (external INTERRUPT from IOCD1), 2 Hz INT. The 2KHz INT, LCDL INT (256 Hz in 1/3, 1/4 bias; 128 Hz in 128 Hz), 128 Hz INT, 2Hz INT, all are divided from 32768 Hz Crystal Oscillator.

5.8. Audio (Melody/Speech) / Tone Output

The SPL10A2 provides both speech and single tone melody output in current DA type that can drive SPEAKER through transistor. Also, the SPL10A2 provides TONE output that can directly drive BUZZER. The two modes, current DA and tone, share the same AUD pin. In current DA mode, it should smoothly switch current DA output current to zero by using speech mode to reduce noise to turn off current DA. The current DA should be turned off when not used due to the current consumption. The TONE output is a full-swing (VDD and VSS) signal and its frequency source is the frequency of TIMER Carry divided by 2.

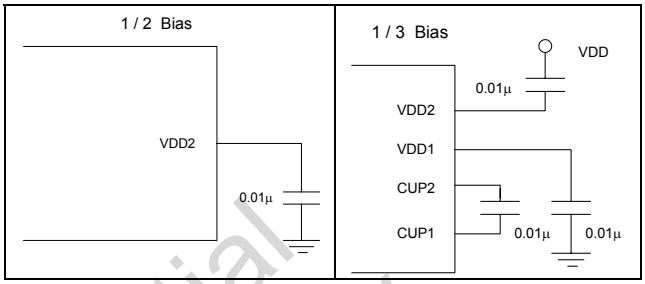
The block diagram is shown as below:



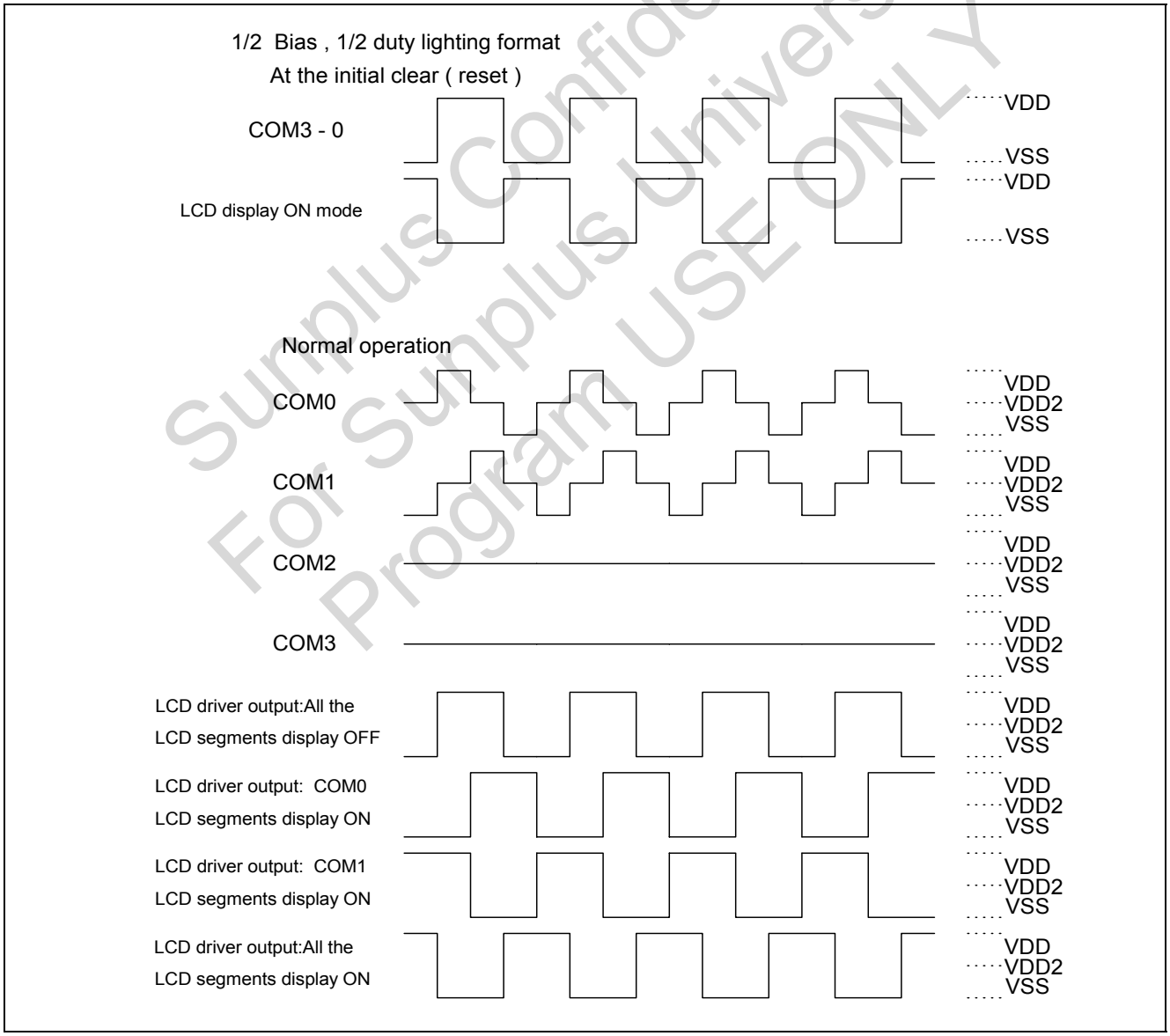
5.9. Liquid Crystal Display

The SPL10A2 can directly drive the liquid crystal display (LCD) panel of 1/2 duty, 1/3 duty, and 1/4 duty with 1/2 bias or 1/3 bias. It has 4 commons and 32 segments signal pins. In share mode (Timer/Counter is used), the LCD is refreshed by LCDL interrupt. The INT routine will read the number of common which is under serving, and send the next common's pattern to LCD port ($10 - $13) from RAM buffer. If the Timer/the Counter is not used, hardware mechanism will auto refresh the LCD after writing OPTION register ($1F).

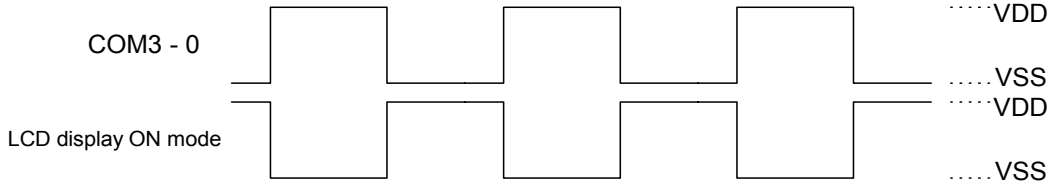
The power connections for LCD (1/2 bias, 1/3bias) are shown as below:



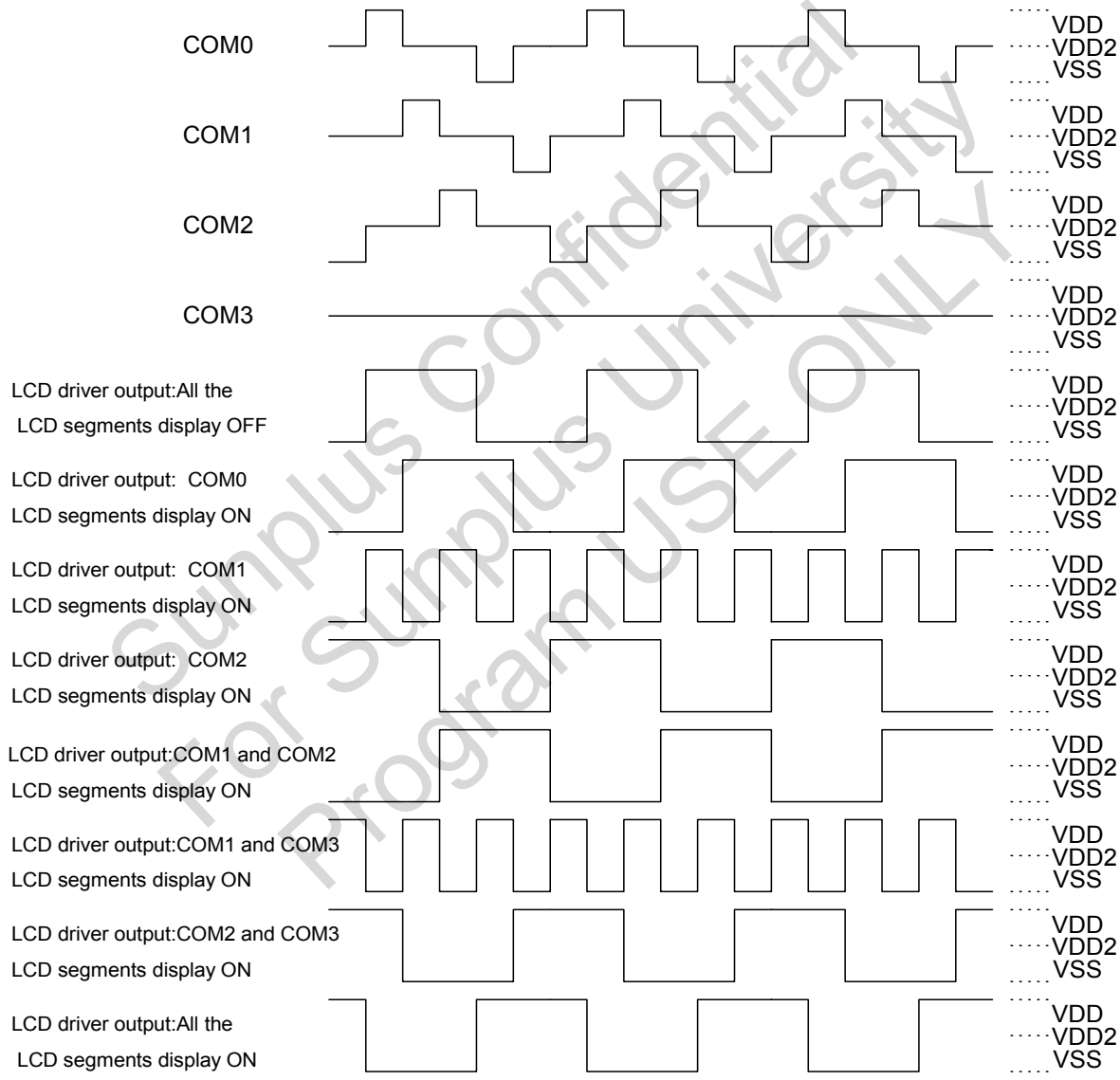
5.10. Output Waveform of the LCD Driver



1/2 Bias , 1/3 duty lighting format
At the initial clear (reset)

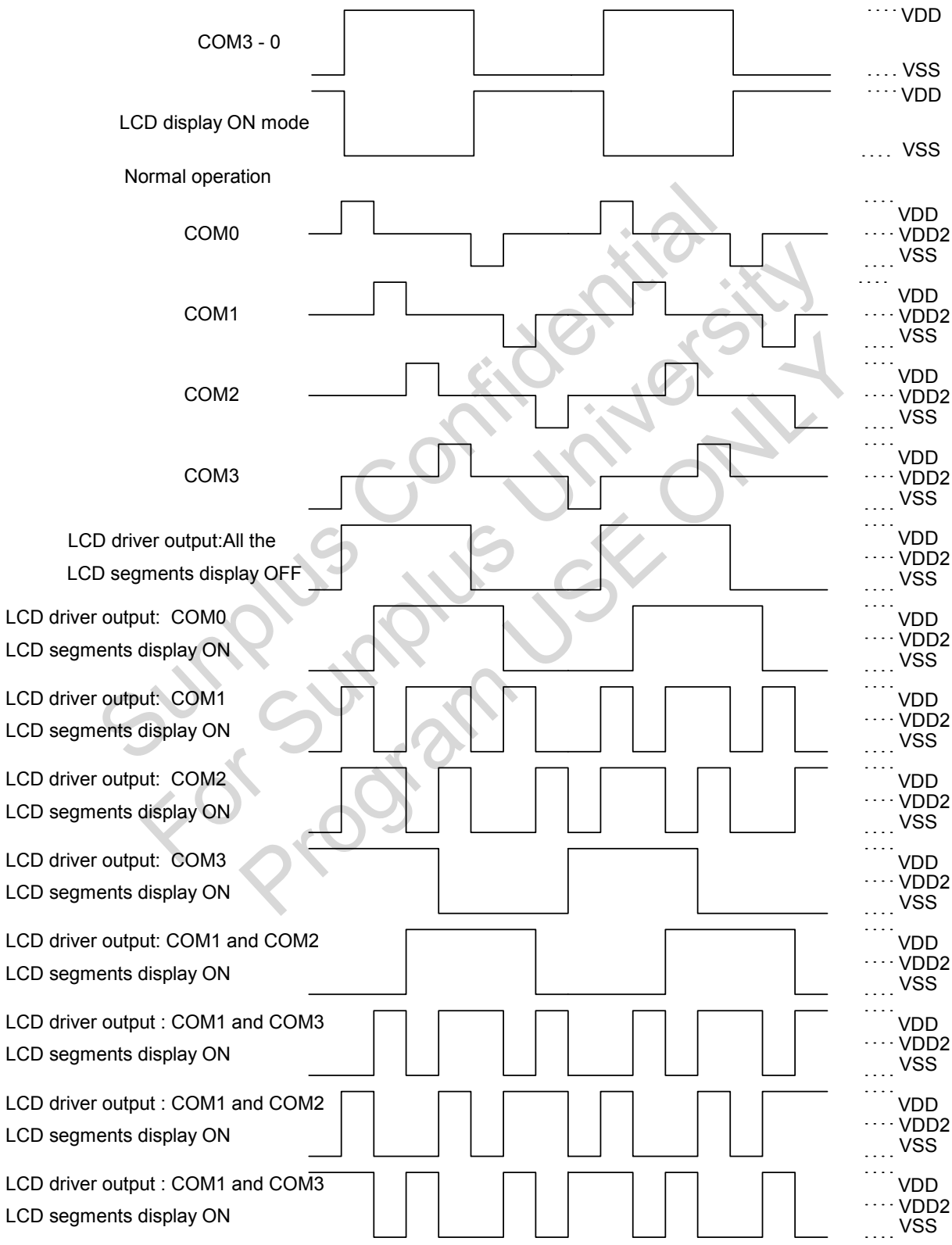


Normal operation



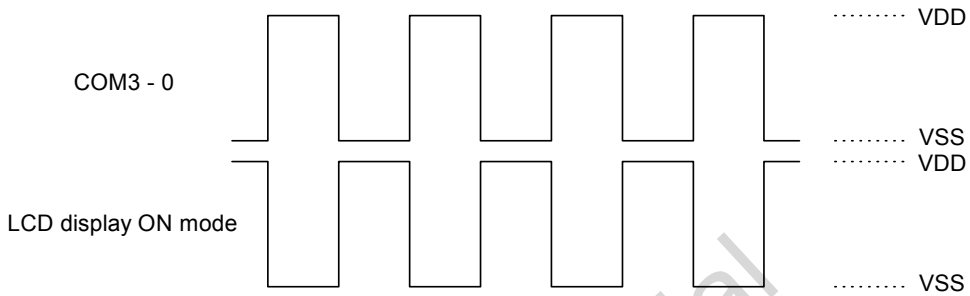
1/2 Bias , 1/4 duty lighting format

At the initial clear (reset)

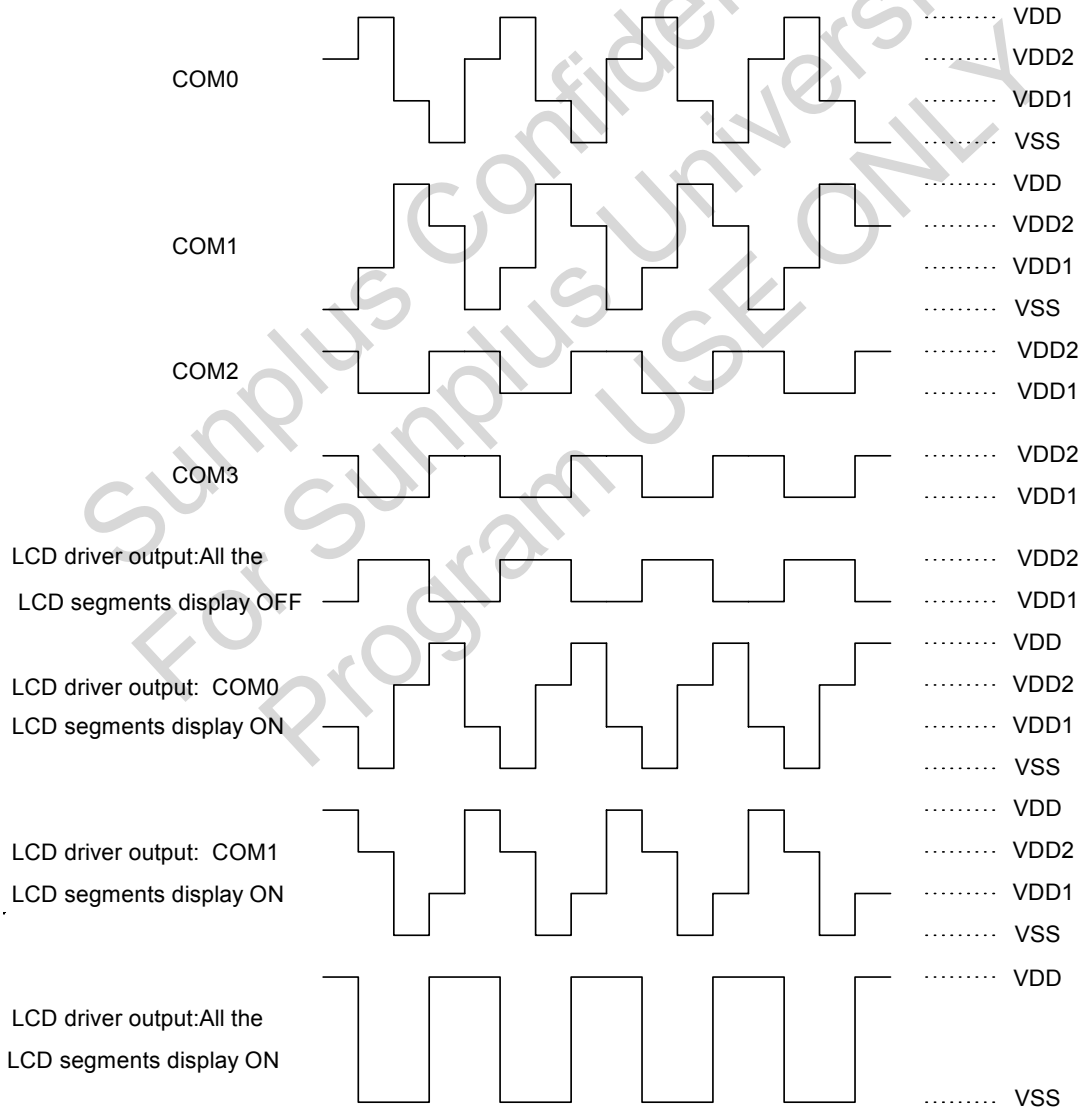


1/3 Bias , 1/2 duty lighting format

At the initial clear (reset)

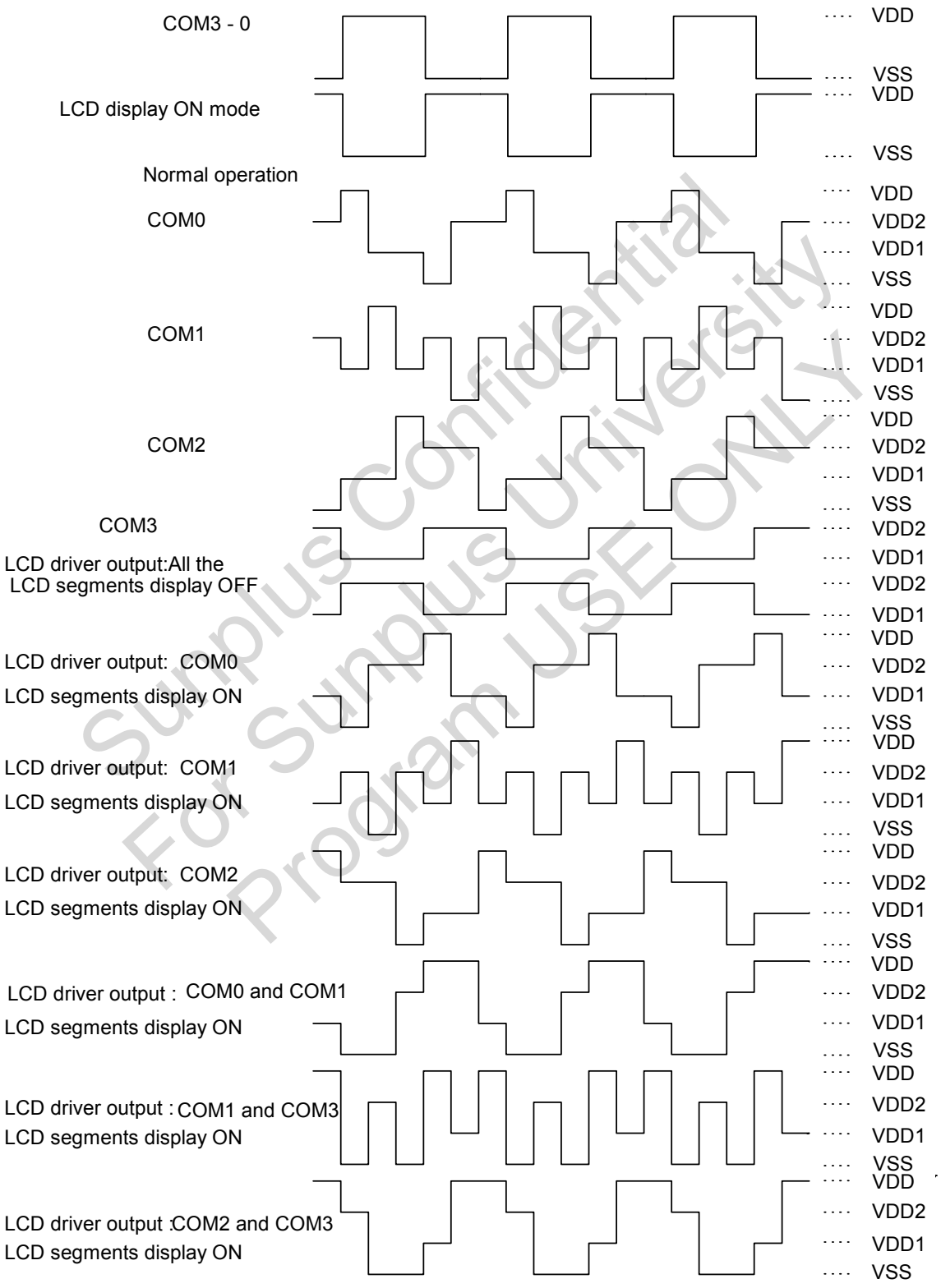


Normal operation



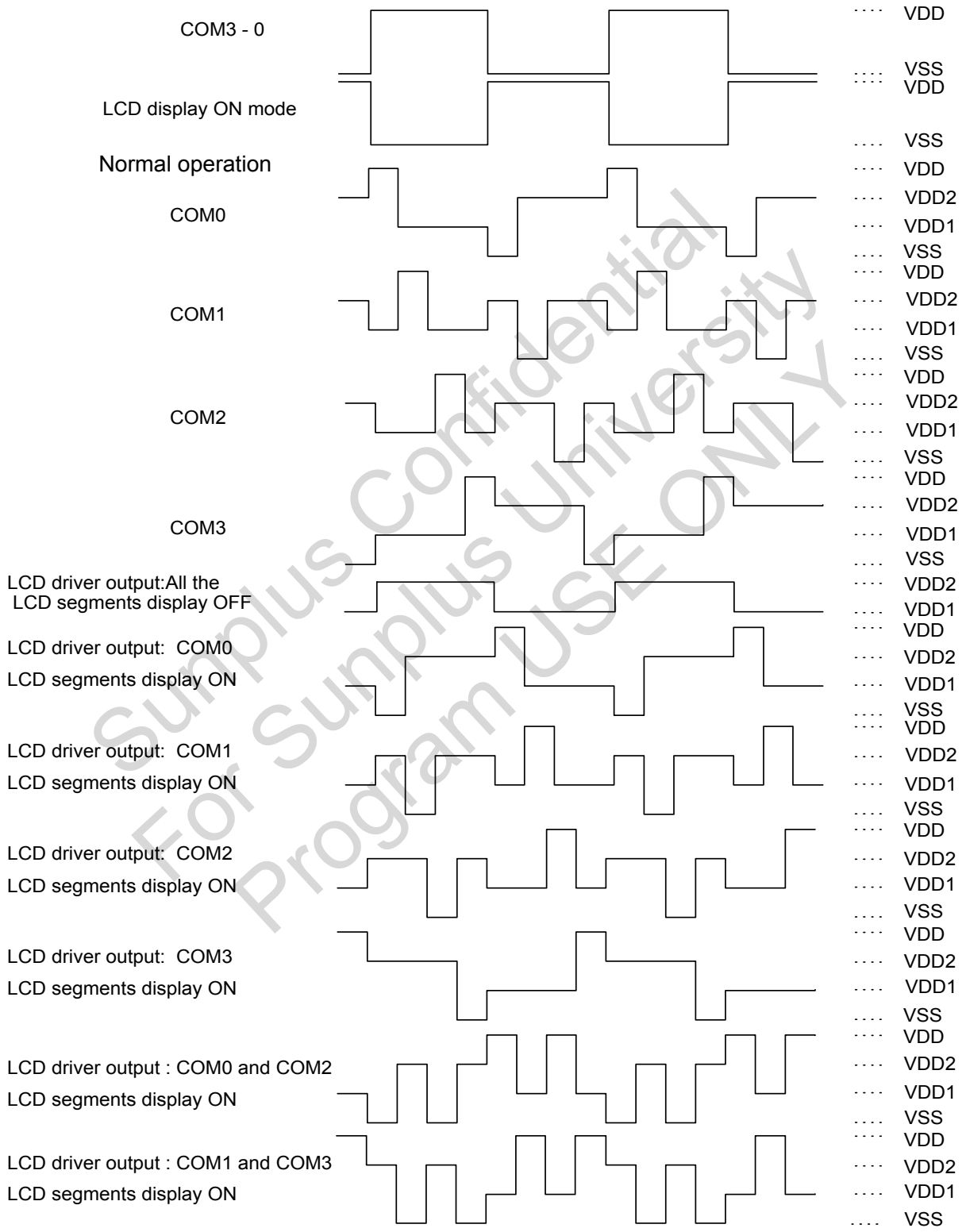
1/3 Bias , 1/3 duty lighting format

At the initial clear (reset)



1/3 Bias , 1/4 duty lighting format

At the initial clear (reset)



5.11. Reset Function

The SPL10A2 can be reset by setting the RESET pin to ground voltage and its operation starts when this pin is set to power voltage. Also an automatic reset function (internal reset function) operates when power is turned on.

5.12. Watch Dog Function

The SPL10A2 provides a watchdog timer. The watchdog timer must be reset when 2Hz wake-up by writing $0F, otherwise it will reset the system.

5.13. Mask Option

The following type mask option is available.

IOEF0 to IOEF5 ..... Select one of A, B, C, D (Refer to INPUT/OUTPUT)

1). Without Fixed Pull Low Resistor 200KΩ, with Feedback MOS
2). With Fixed Pull Low Resistor 200KΩ, without Feedback MOS
3). With Fixed Pull Low Resistor 200KΩ, with Feedback MOS
4). Without Fixed Pull Low Resistor 200KΩ, without Feedback MOS

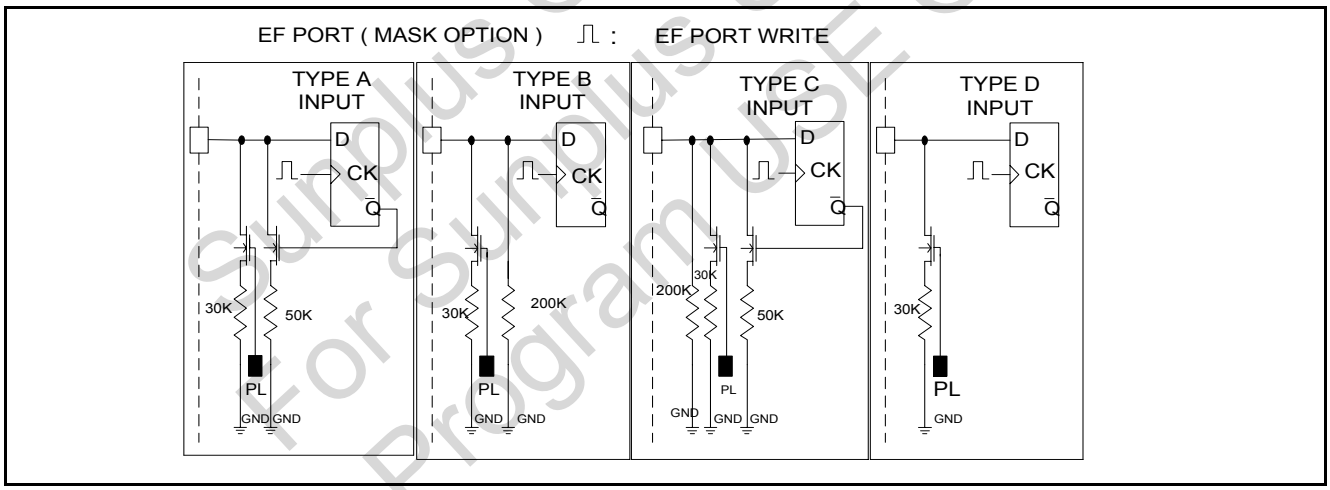
32768 Hz clock source ..... Select one of A, B (Refer to R oscillator)

1). 32768 Crystal Oscillator
2). R Oscillator

5.14. I/O Port Configuration

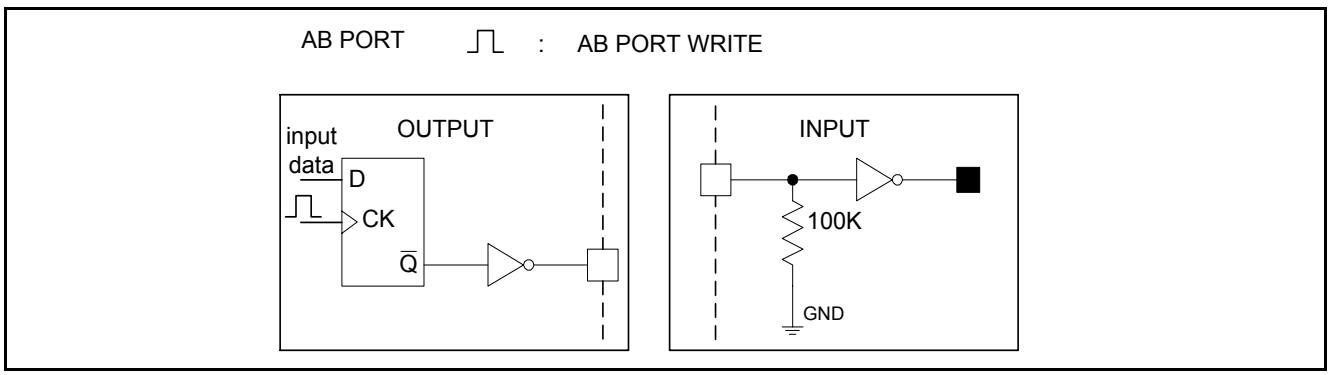
5.14.1. Input IOEF port: IOEF0 to IOEF5

There are 4 different configurations in IOEF port. They are shown as following:



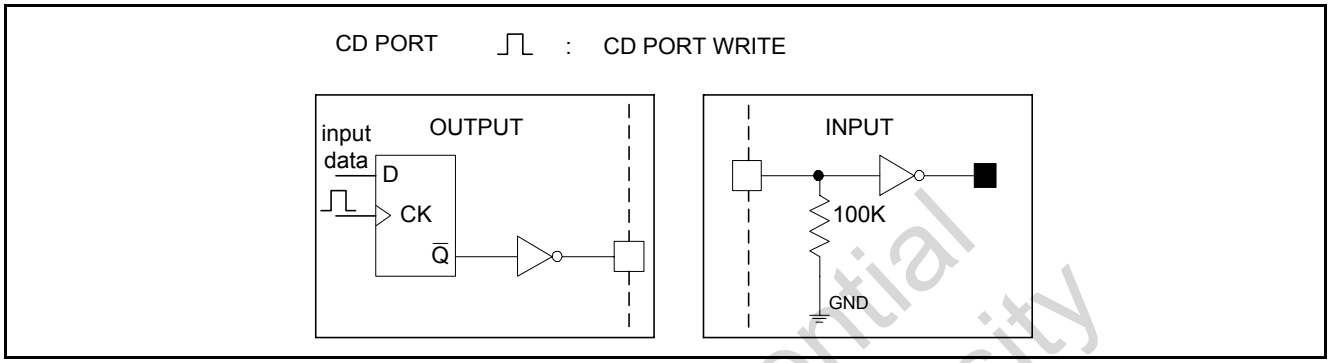
5.14.2. Input/Output IOAB port: IOAB0 and IOAB1

These two ports can be programmed to be INPUT or OUTPUT pins. The configurations are shown as below:

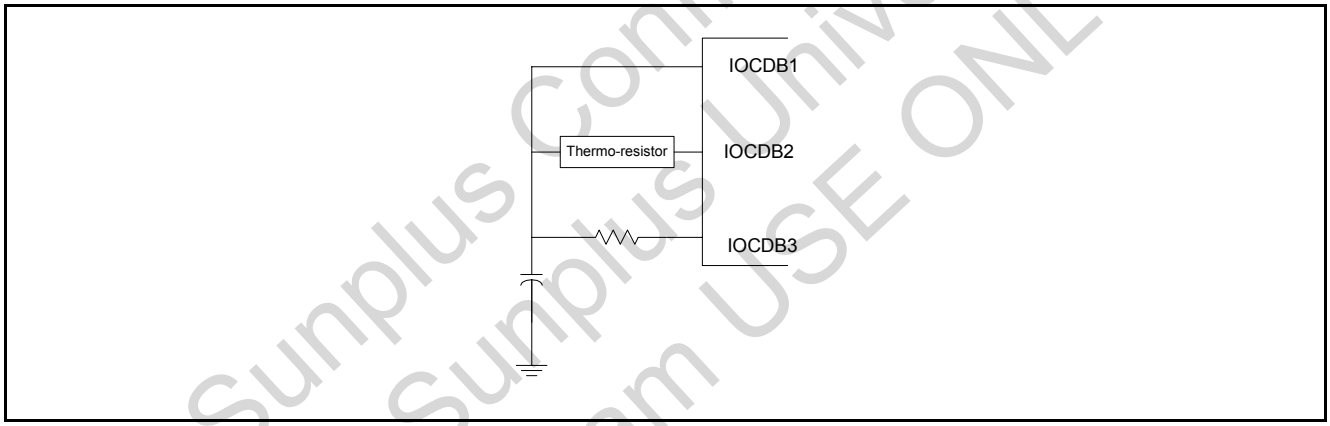


5.14.3. Input/Output IOCD port: IOCD0 to IOCD3

These four IOCD ports can be programmed to be INPUT or OUTPUT pins independently. These pins also can be used to implement a thermometer by sense mode. Their configurations are shown as belows:



The application circuit for sense mode:



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

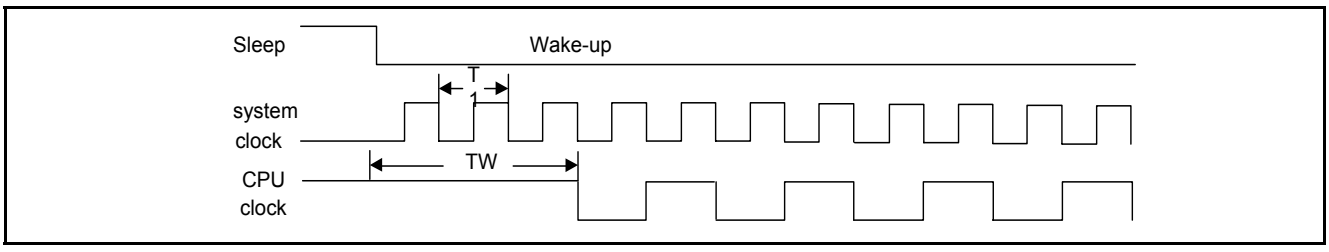
6.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.0	V	
Operating Current	I_{OP}	-	350	-	μA	F_{CPU} = 600KHz @ 3.0V
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V, 32768 Hz OFF
Current DA output	I_{OH}	-	-1.0	-	mA	VDD = 3.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I (I/O)	I_{OH}	-300	-	-	μA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink I (I/O)	I_{OL}	600	-	-	μA	VDD = 3.0V, V_{OL} = 0.8V
LCD Display Voltage	V_{LCD}	-	-	VDD	V	
LCD Drive	VDD	2.8	-	3.0	V	V_{LCD} = 3.0V, I_O = -6μA
Output Voltage	VDD2	1.8	-	2.2	V	V_{LCD} = 3.0V, I_O = ±3.5μA
	VDD1	0.8	-	1.2	V	V_{LCD} = 3.0V, I_O = ±3.5μA
	VSS	0	-	0.2	V	V_{LCD} = 3.0V, I_O = +6μA

6.3. AC Characteristics

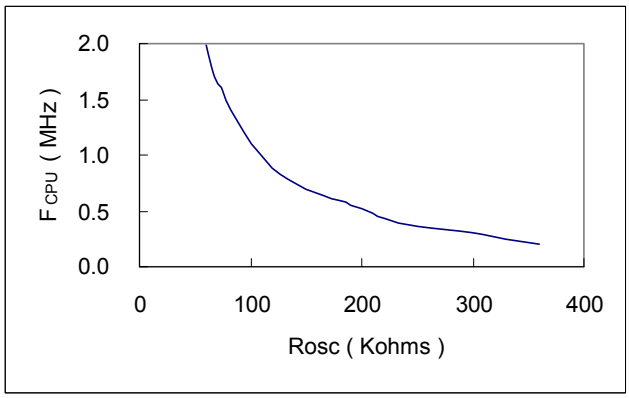
Characteristics	Symbol	Limits			Unit	Test condition
		Min.	Typ.	Max.		
OSC frequency	F_{OSC}	-	-	4.0	MHz	VDD = 3.0V
CPU clock	F_{CPU}	0.01	-	2.0	MHz	F_{CPU} = F_{OSC} /2 @ 3.0V
Frame frequency of the LCD drive	F_{FM1}	-	64	-	Hz	1/2 duty
		-	85	-	Hz	1/3 duty
		-	64	-	Hz	1/4 duty
Wake-up time	T_W	6T1	-	-	Sec.	

T1 = 1/(F_{OSC}), Tw = 3 x T1, F_{CPU} = F_{OSC}/2

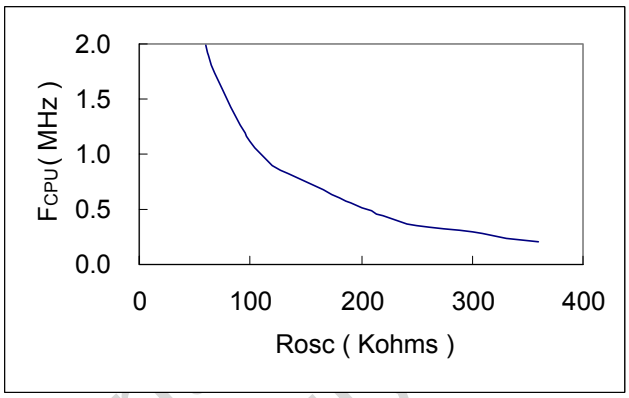


6.4. The Relationship between the R_{OSC} and the F_{CPU}

6.4.1. VDD = 3.0V, T_A = 25℃

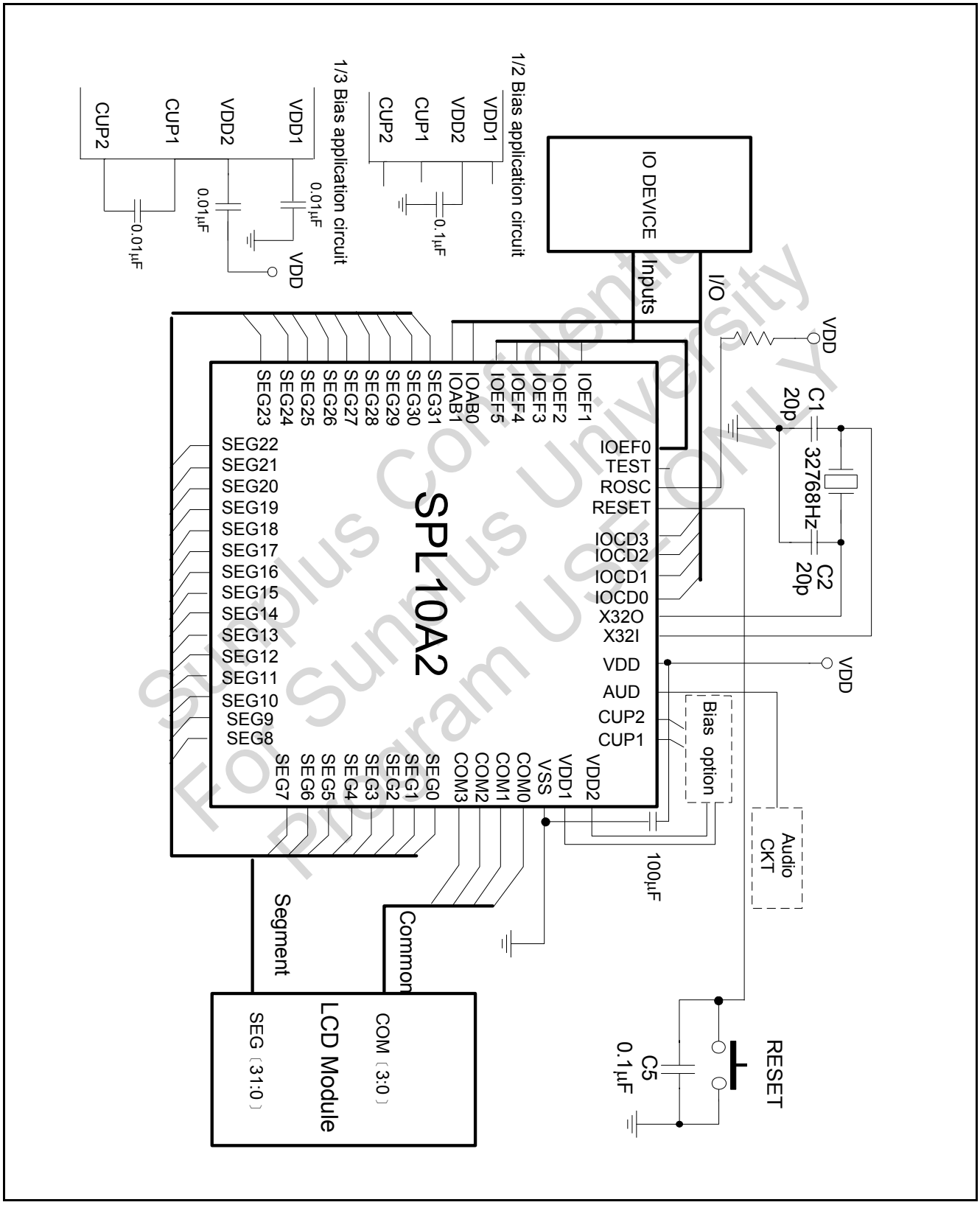


6.4.2. VDD = 4.5V, T_A = 25℃

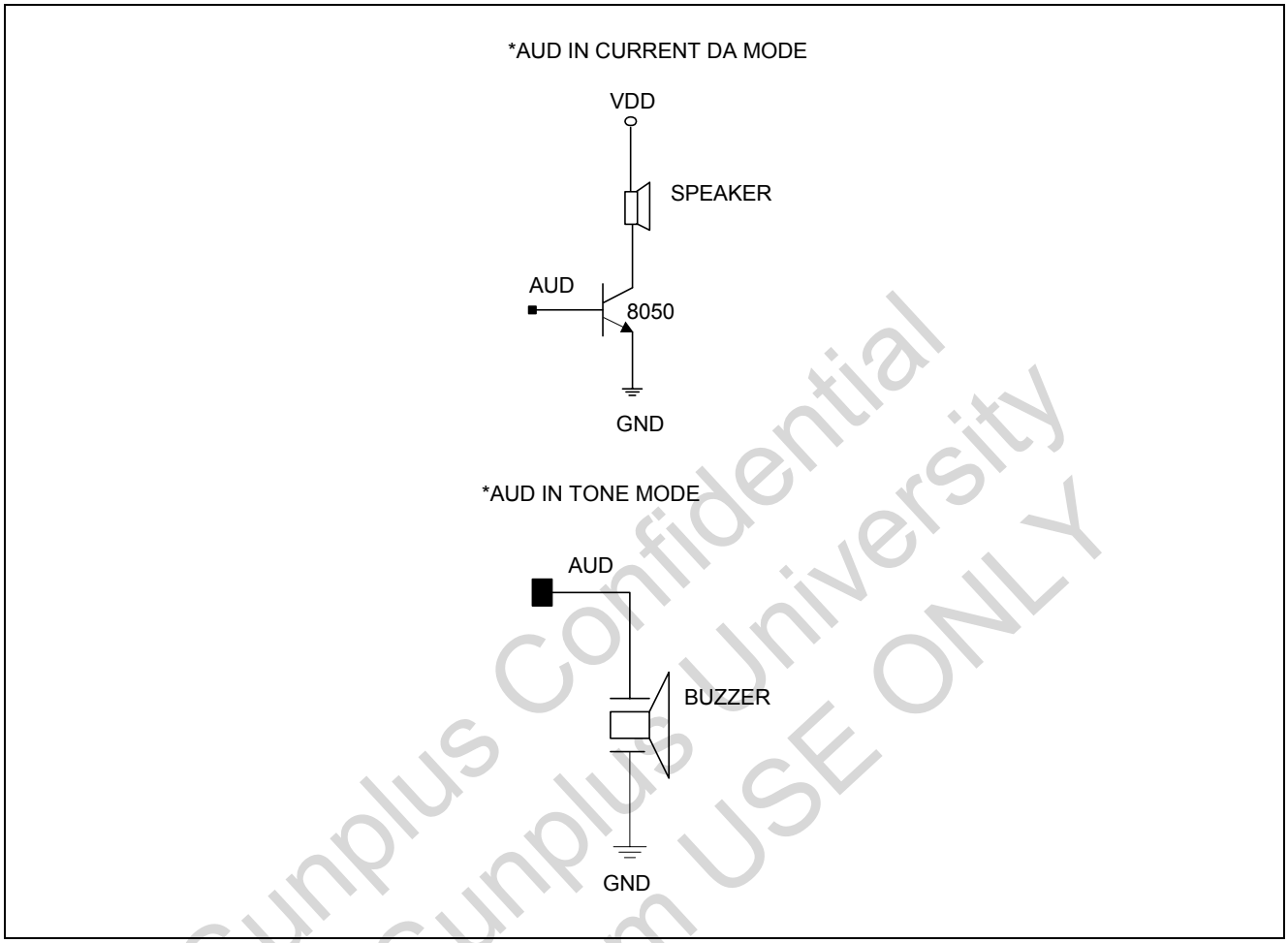


7. APPLICATION CIRCUITS

7.1. Application Circuit



7.2. Audio Driver/Amplifier for DA Mode

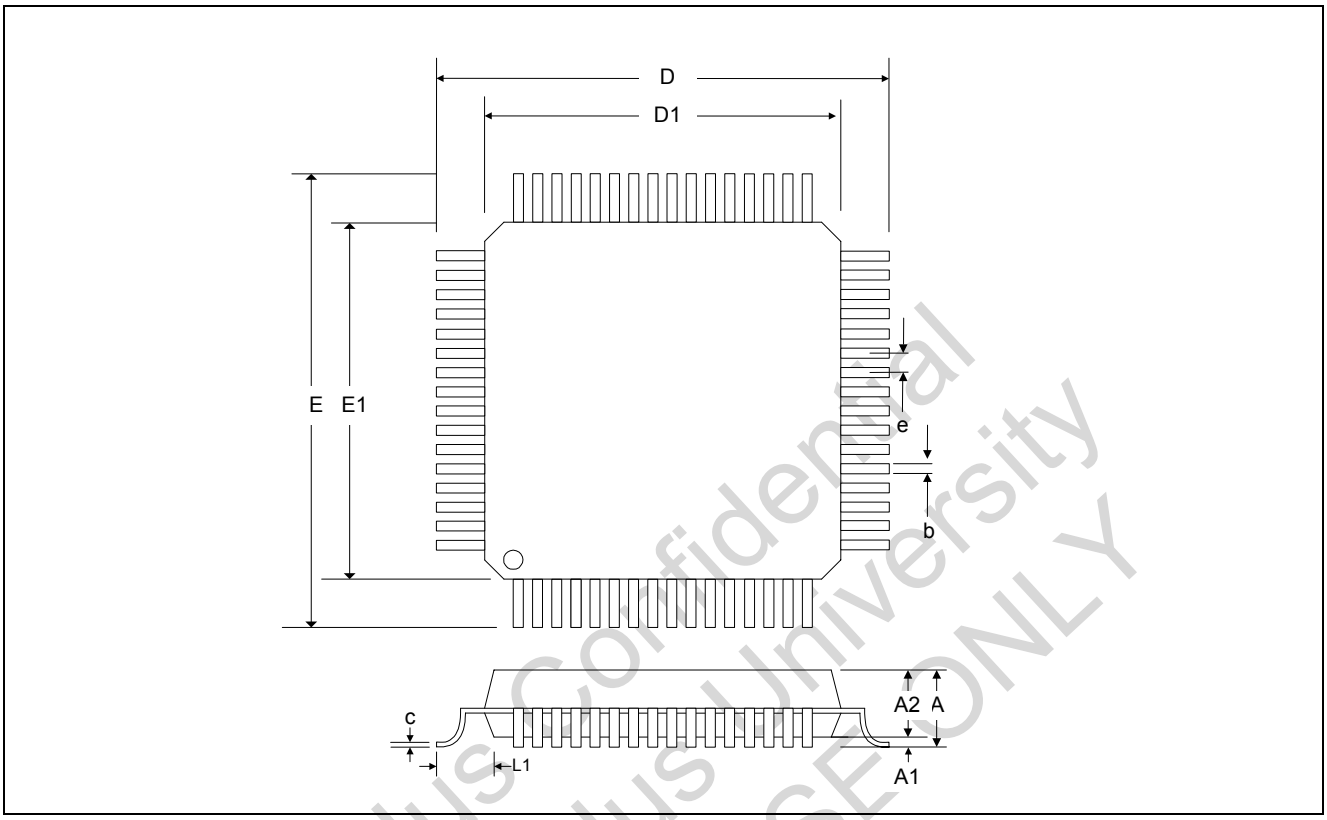


8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

8.2. Package Information



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
D		12.00 BSC.		Millimeter
D1		10.00 BSC.		Millimeter
E		12.00 BSC.		Millimeter
E1		10.00 BSC.		Millimeter
e		0.50 BSC.		Millimeter
b	0.17	0.20	0.27	Millimeter
c	0.90	-	0.20	Millimeter
L1		1.00 REF		Millimeter

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10. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 12, 2004	1.5	Add LQFP 64 pin package information	4 - 5, 21
AUG. 28, 2003	1.4	1. Modify RESET state to next instruction in "*5.5. Stop Clock Mode*" 2. Remove "*8. PACKAGE/PAD LOCATIONS*"	6
MAR. 18, 2002	1.3	1. Modify X32I description 2. Delete item "OSC Resistor" in the "*6.2 DC Characteristics*" 3. Add "*6.4 The Relationship between the R_{OSC} and the F_{CPU}*" 4. Renew to a new document format	4 15 16
MAR. 23, 2001	1.2	1. Add "Note: Patent Circuitry Included. Taiwan Patent No. 68824" 2. Add "Note2: The 0.1μF capacitor between VDD and VSS…" 3. Add "*REVISION HISTORY*" 4. Renew to a new document format	1 17 20
NOV. 19, 2000	1.1	Change ROM Size 7.5 -> 7 (test program uses 0.5K)	
DEC. 06, 1999	1.0	Delete "*Preliminary*"	
MAY. 03, 1999	0.1	Original	