DATA SHEET

SUNPLUS

SPR4096A

512K x 8 Bits Bus Flash

OCT. 01, 2003

Version 1.2

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512K X 8 BITS BUS FLASH

1. GENERAL DESCRIPTION

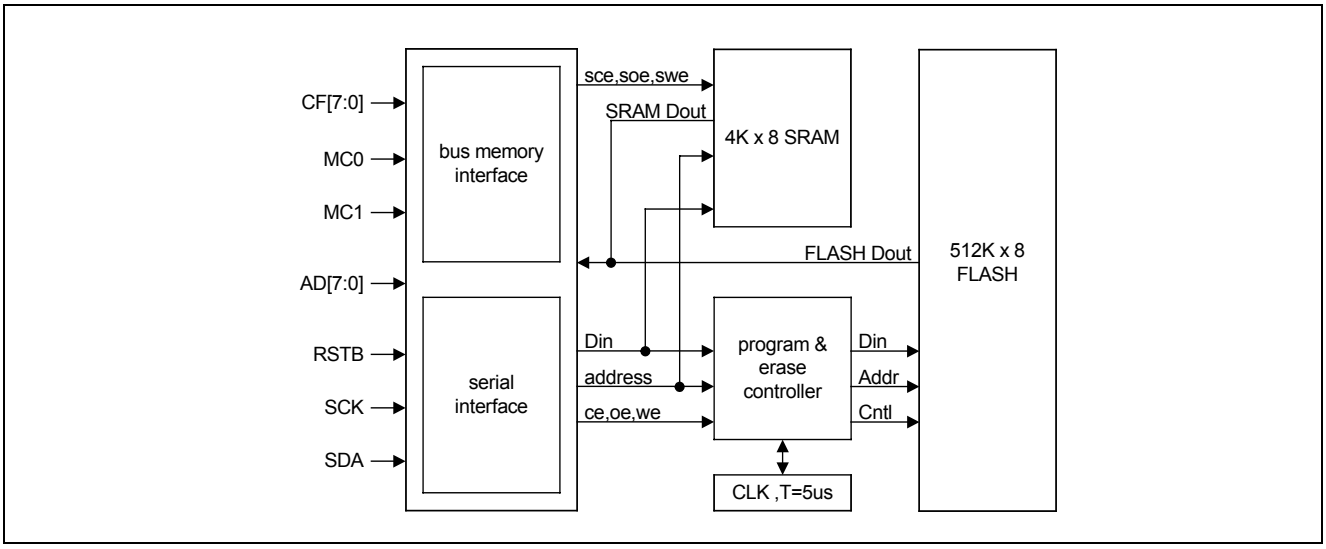
SPR4096A embeds 512K x 8-bit high performance bus flash memory and 4K x 8-bit SRAM. In the embedded Bus Memory Interface (BMI) and a Serial Interface, SPR4096A allows SPL13X & SPLB3X MCU to access FLASH/SRAM memory via BMI or 1-bit serial mode. In SPR4096A, two power types are offered - VDDI and VDDQ. The VDDI, ranged between 2.25V to 2.75V, is the power supply for internal FLASH memory and logical control components. The VDDQ, ranged from 2.25V to 3.6V, is the power supply to I/O only. SPR4096A is able to operate up to 5.0MHz. Its maximum read current is 2mA and maximum program/erase current is 6.0mA.

2. FEATURES

- 512K x 8 bits FLASH, 256 sectors and 2K bytes per sector.
- Endurance: 20,000 Cycles (min)
- Data Retention: 10 years under Room Temperature
- 4K x 8 bits SRAM.
- Supply voltage: VDDQ: 2.25V ~ 3.6V, VDDI: 2.25V ~ 2.75V.
- Maximum operating frequency: Bus Interface and serial interface at 5.0MHz.
- Operating current: 6.0mA (max).
- Standby current: 4.0μA (max).
- Concurrent SRAM write/read while erasing/programming FLASH.
- Fast page programming mode (16 bytes).
- Cascade application is available for both Bus and Serial Interface.

3. BLOCK DIAGRAM

The SPR4096A contains six components: Bus Memory Interface (BMI), Serial Interface (SIF), timer, 32K-bit SRAM, program & erase controller (PECON), and a 4M-bit FLASH memory. The CF0 - CF7 define the memory configuration. When BMI is selected, MC0 and MC1 act as write/read control signal, and AD[7:0] is bi-direction address/data bus. BMI processes these signals and generates control signals and address/data for FLASH or SRAM write/read. If BMI receives PROGRAM, ERASE or MASS ERASE command for FLASH, it forwards these commands to PECON for command execution. When SIF is selected, SCK behaves as serial clock and SDA as 1-bit serial I/O. If FLASH read or SRAM write/read command is received, SIF is capable of writing to/reading from the embedded memory directly. However, if PROGRAM, ERASE or MASS ERASE for FLASH is received, SIF also forwards these commands to PECON. When EPCON is active, it needs a 200KHz clock (provided by the CLK block shown in block diagram).


CF[7:0]
MC0
MC1
AD[7:0]
RSTB
SCK
SDA
bus memory interface
serial interface
sce,soe,swe
SRAM Dout
4K x 8 SRAM
FLASH Dout
512K x 8 FLASH
Din
address
ce,oe,we
program & erase controller
Din
Addr
Cntl
CLK ,T=5us

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Description
CF0 - CF7	30 - 23	Configuration bonding option.
AD0 - AD7	12 - 19	Bus Interface address/data I/O.
MC0 - MC1	7 - 8	Bus Interface write/read control signal.
$\overline{\text{RESET}}$	3	Reset (low active).
SCK	4	Serial Interface clock.
SDA	10	Serial Interface data I/O.
VDDQ	20	Power supply for 3.3V device.
VDDI	9	Power supply for 2.5V device.
VSS VSSQ	1, 6 11	Ground

4.1. Ordering Information

Product Number	Package Type
SPR4096A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

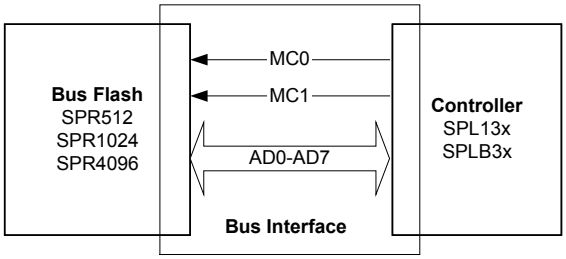
5. FUNCTIONAL DESCRIPTIONS

5.1. BUS Memory Interface (BMI)

5.1.1. BMI description

When Bus Memory Interface is used, the pins should be connected as follows:

Name	Description
CF0 - CF7	Configuration bonding option
AD0 - AD7	Bus Interface address/data I/O
MC0 - MC1	Bus Interface write/read control signal
$\overline{\text{RESET}}$	Reset (low active)
SCK	Not connected
SDA	Not connected
VDDQ	Power supply for 3.3V device.
VDDI	Power supply for 2.5V device.
VSS, VSSQ	Ground



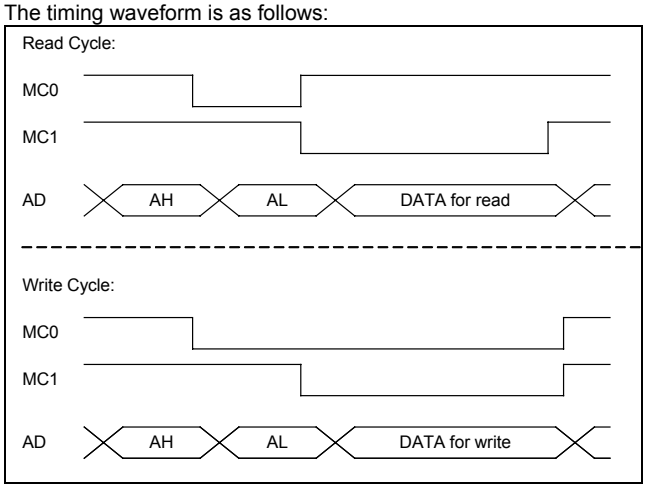
Block diagram of bus flash and BMI controller

BMI is an interface between SPR4096A and SPL13X or SPLB3X MCU. It provides flexible and efficient memory management. BMI contains an 8-bit bi-directional Address/Data bus, ADbus, which is multiplexed by two control signals - MC0 and MC1. The relationship of Bus flash and BMI controller is shown above. MC0 configures the operation mode (Read or Write), and MC1 determines whether the ADbus is an address or a data bus. The MC0 and MC1 decoded table is depicted as follows:

MC1	MC0	AD BUS
L	L	Data for Write
L	H	Data for Read
H	L	AL
H	H	AH

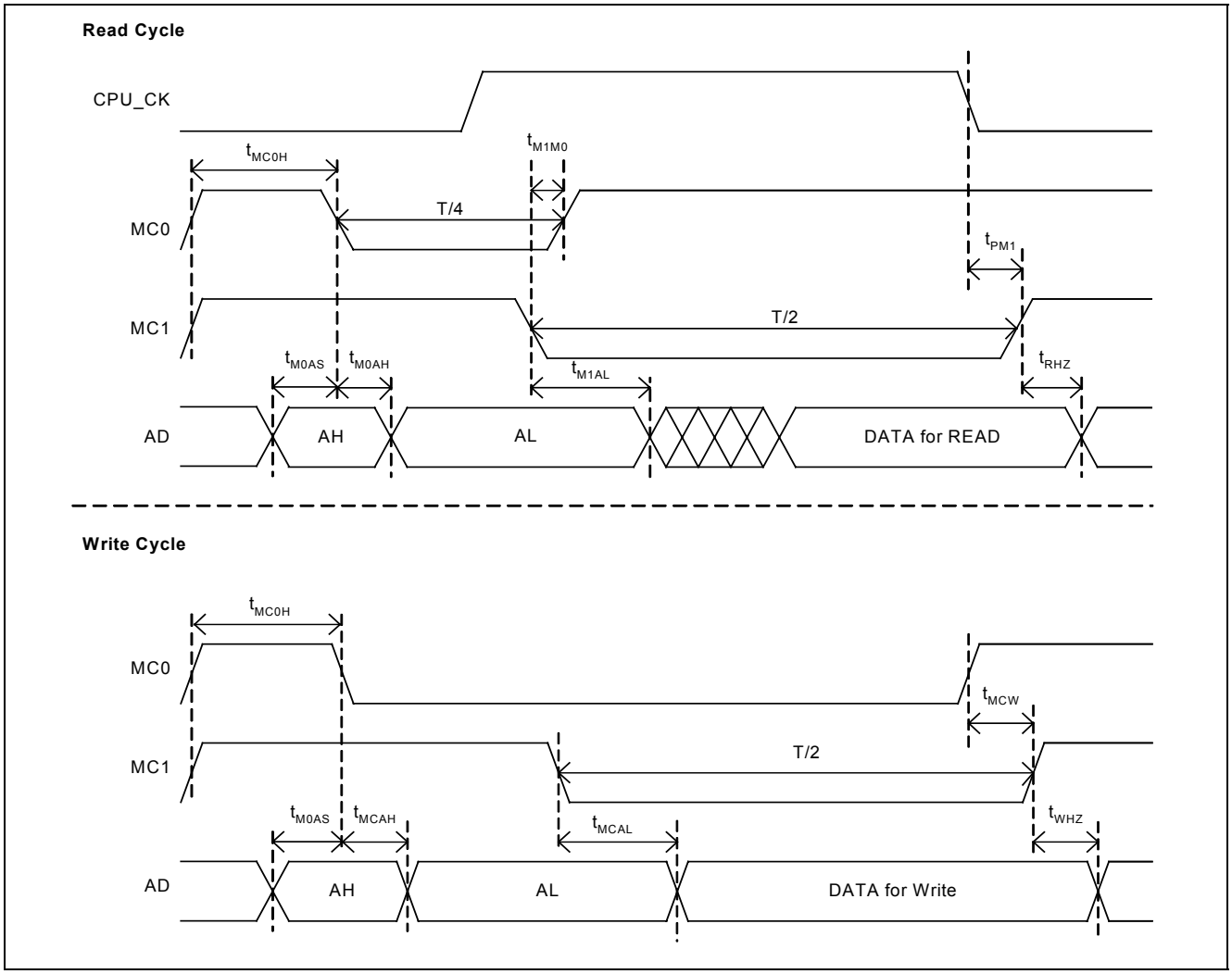
AH: high byte address
AL: low byte address.

The timing waveform is as follows:



MC0 falling edge => latch AH.
MC1 falling edge => (1) latch AL.
(2) if MC0 = 1 then READ, if MC0 = 0 then WRITE.
MC1 rising edge => if READ then set ADbus to HiZ. if WRITE then latch DATA for WRITE.

5.1.2. BMI AC characteristics



5.1.2.1. AC characteristics (VDD = 2.85V - 3.15V , T_A = 0 - 70℃)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
MC1 period	T	200	-	-	ns
High period of MC0	T_{MC0H}	20	-	-	ns
AH setup time	T_{M0AS}	10	-	-	ns
MC0 falling to AH end	T_{M0AH}	10	-	-	ns
MC1 rising to MC0 falling	T_{M1M0}	-	-	15	ns
MC1 falling to AL end	T_{M1AL}	10	-	35	ns
MC1 rising to AD Hi-Z (W)	T_{WHZ}	10	-	-	ns
MC1 rising to AD Hi-Z (R)	T_{RHZ}	-	-	5.0	ns
Data latch to MC1 rising	T_{PM1}	-	25	-	ns
MC0 rising to MC1 rising	T_{MCW}	-	15	-	ns

5.1.3. BMI configuration setting

The Bus Memory Interface (BMI) has four modes, A, C, E, and G in which volume IDs are “00”, “01”, “xx”, and “01” respectively, where “xx” represents “don’t care”. The configuration settings are illustrated in the CF[2:0], where CF indicates the physical pins, see Table 1. For the physical pins, simply apply logic high (1) or low (0) to the pins to participate the settings. Moreover, the CF[7:3] determines the bank control register ($00) configuration and SRAM allocation area, see the Table 2 for detailed setups. Note that the change of bank is accomplished by given the corresponding value to the $00. For example, to access the Bank0, a value of “00h” must be given to $00 in addition to a logic value of “10000” should be given to the external pins, CF[7:3].

Table 1: CF[2:0], configuration of BMI mode.

BMI Type	CF2	CF1	CF0	Volume ID $0D[1:0]
A	0	0	0	00
C	0	1	0	01
E	1	0	0	xx
G	1	1	0	01

Table 2: CF[7:3], configuration of bank setting and SRAM allocation. “b” is for extender memory bank select.

BMI Type	CF7	CF6	CF5	CF4	CF3	Flash Bank Switch	SRAM allocation
A, C, E	1	0	0	0	0	0000bbbb	$2000~2FFF
	1	0	0	0	1	0001bbbb	$3000~3FFF
	1	0	0	1	0	0010bbbb	$2000~2FFF
	1	0	0	1	1	0011bbbb	$3000~3FFF
	1	0	1	0	0	0100bbbb	$2000~2FFF
	1	0	1	0	1	0101bbbb	$3000~3FFF
	1	0	1	1	0	0110bbbb	$2000~2FFF
	1	0	1	1	1	0111bbbb	$3000~3FFF
	1	1	0	0	0	1000bbbb	$2000~2FFF
	1	1	0	0	1	1001bbbb	$3000~3FFF
	1	1	0	1	0	1010bbbb	$2000~2FFF
	1	1	0	1	1	1011bbbb	$3000~3FFF
	1	1	1	0	0	1100bbbb	$2000~2FFF
	1	1	1	0	1	1101bbbb	$3000~3FFF
	1	1	1	1	0	1110bbbb	$2000~2FFF
	1	1	1	1	1	1111bbbb	$3000~3FFF
G	X	X	0	0	0	1000bbbb	N/A
	X	X	0	0	1	1001bbbb	N/A
	X	X	0	1	0	1010bbbb	N/A
	X	X	0	1	1	1011bbbb	N/A
	X	X	1	0	0	1100bbbb	N/A
	X	X	1	0	1	1101bbbb	N/A
	X	X	1	1	0	1110bbbb	N/A
	X	X	1	1	1	1111bbbb	N/A

5.1.4. BMI register description

The BMI uses MCU address from 4000h to FFFFh and duplicates some registers of SPL13X and SPLB3X into SPR4096A as bank switch. The register usage and mapping table is as below.

5.1.4.1. Memory bank switch ($00, BSW)

b7	b6	b5	b4	b3	b2	b1	b0
*	*	*	*	BSW3	BSW2	BSW1	BSW0

* $00[7:4] must be set the same value as the physical logic setting of CF[6:3]

5.1.4.2. Volume ID ($0D , VOL)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	1	VOL1	VOL0

5.1.4.3. External memory mapping ($0B.1 , EXC)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	EXC	-

CPU address mapping of $C000 - $FFFF.

b1 : EXC = 0: Map to internal ROM

= 1: Map to external Bus Flash

Note: SUNPLUS recommend “always” keep this bit to “0” when bus flash is applied.

5.1.4.4. Flash writing protection ($18.2 , PT)

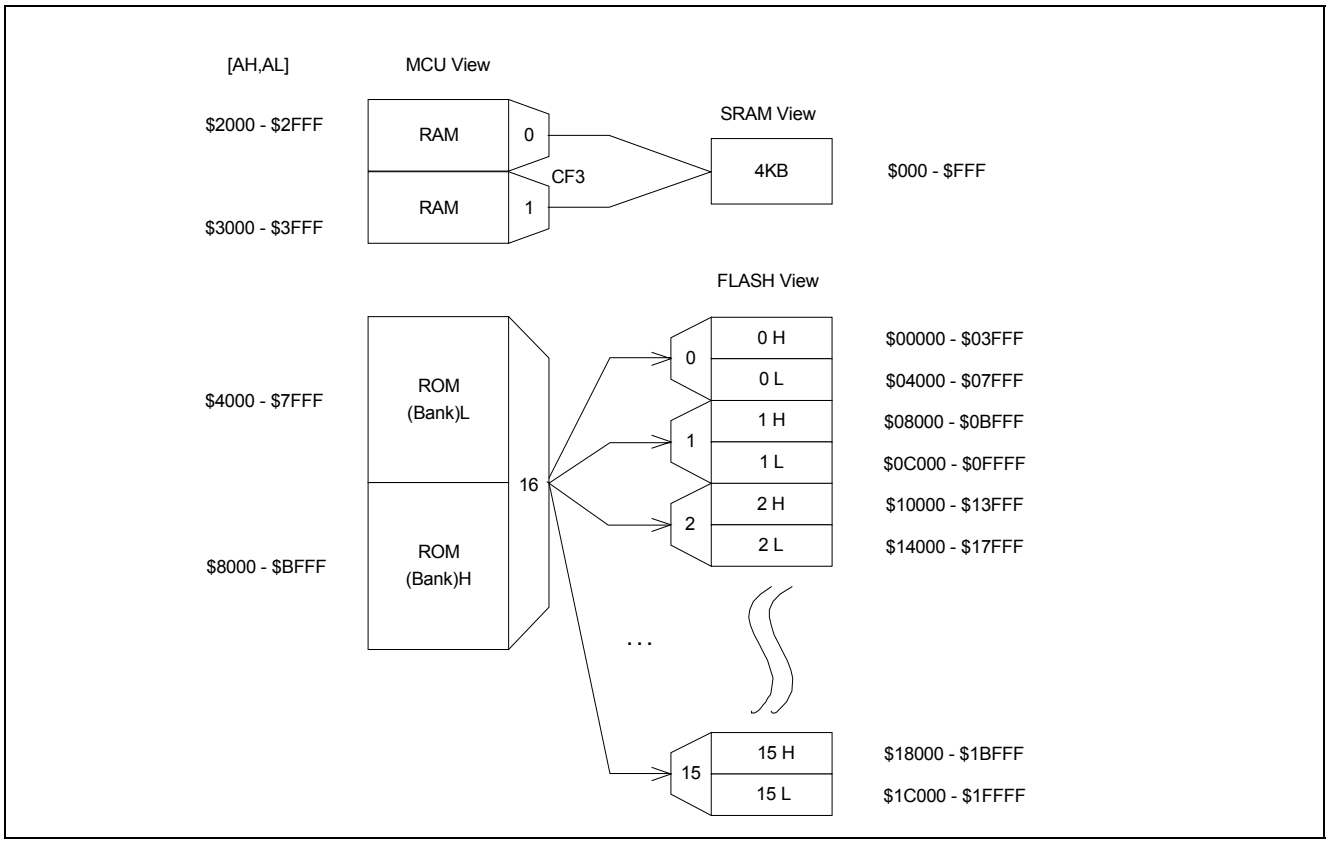
b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	PT	-	-

Write-protect for the beginning 1M bit Flash when using Bus Interface. (Serial Interface don’t support write protect function)

b1: PT = 0: enabled (default)

= 1: disabled

5.1.5. BMI memory mapping



5.1.6. BMI command sequence

5.1.6.1. Bus memory interface command sequence

Command sequence	Bus cycle											
	1nd		2rd		3th		4th		5th		6th	
	Addr	Data	addr	Data	addr	Data	addr	Data			addr	Data
Read device ID	5555h	AAh	AAAAh	55h	5555h	90h	8000h/ 8001h	ID (read)				
Read status	5555h	AAh	AAAAh	55h	5555h	70h	Any addr.	Status(1)				
Return to normal mode (RESET)	XXXX	F0h										
Read	RA	RD (read)										
Byte program	5555h	AAh	AAAAh	55h	5555h	A0h	PA(2)	PD(3)				
Page program	5555h	AAh	AAAAh	55h	5555h	B0h	PA0	PD0	---	---	PAn	PDn
Sector Erase	5555h	AAh	AAAAh	55h	5555h	80h	5555h	AAh	AAAAh	55h	EA(4)	30h
Mass erase	5555h	AAh	AAAAh	55h	5555h	88h	5555h	AAh	AAAAh	55h	5555h	10h

Note1: Status: b7 for 0/1: busy/ready, b0 for 0/1: write enable/write protect.

Note2: PA: program byte address

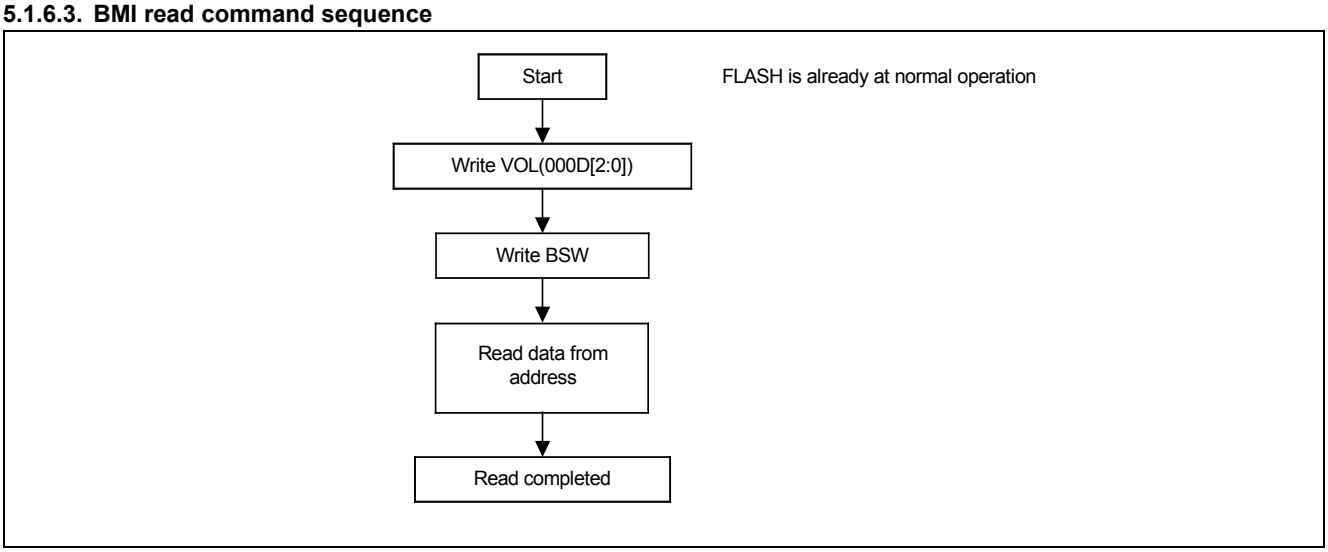
Note3: PD: program data

Note4: EA: sector erase address

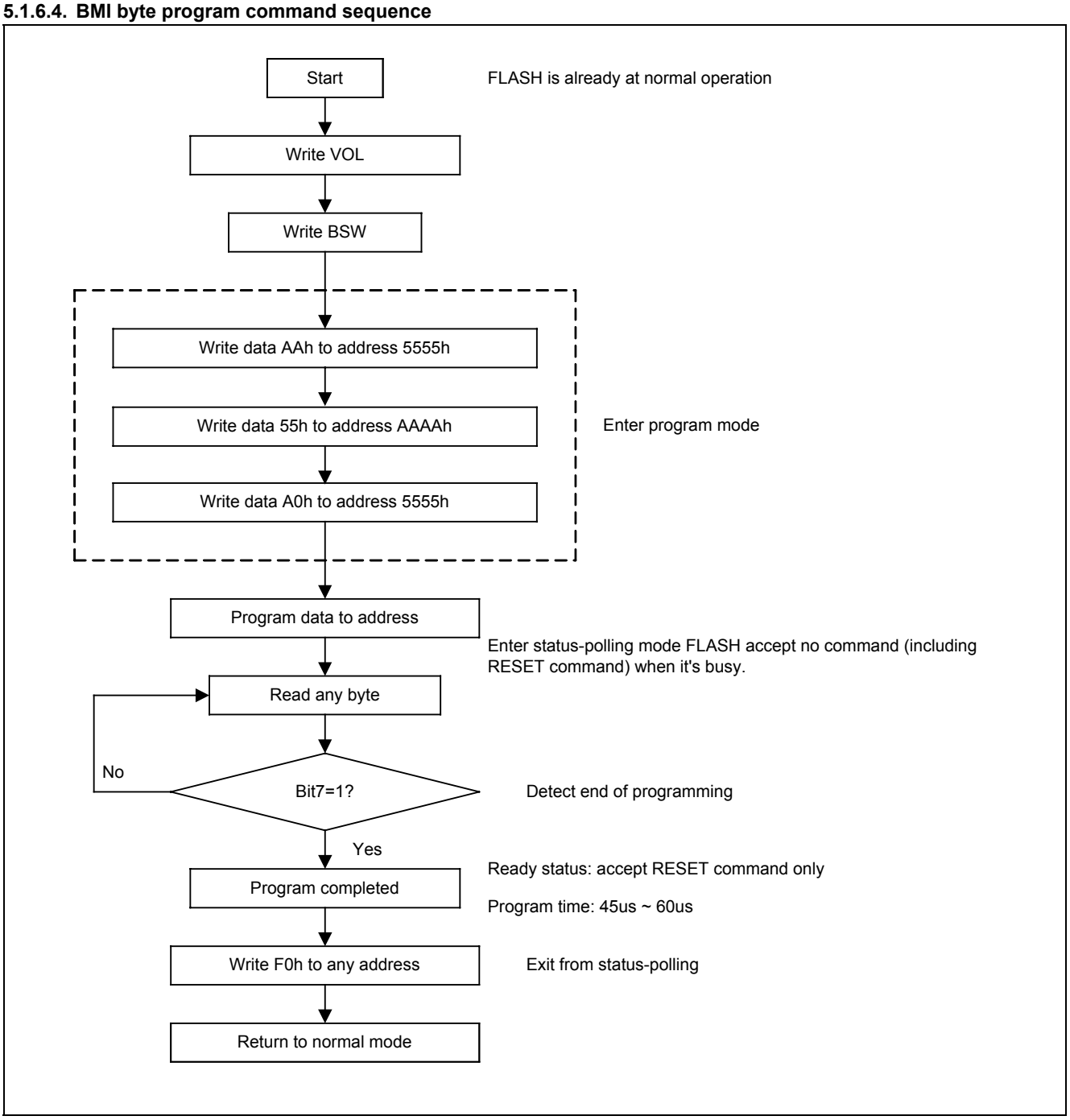
5.1.6.2. Read device ID command output

	Address	Data
Manufacture's code	00000h	C7h
Device code	00001h	D7h

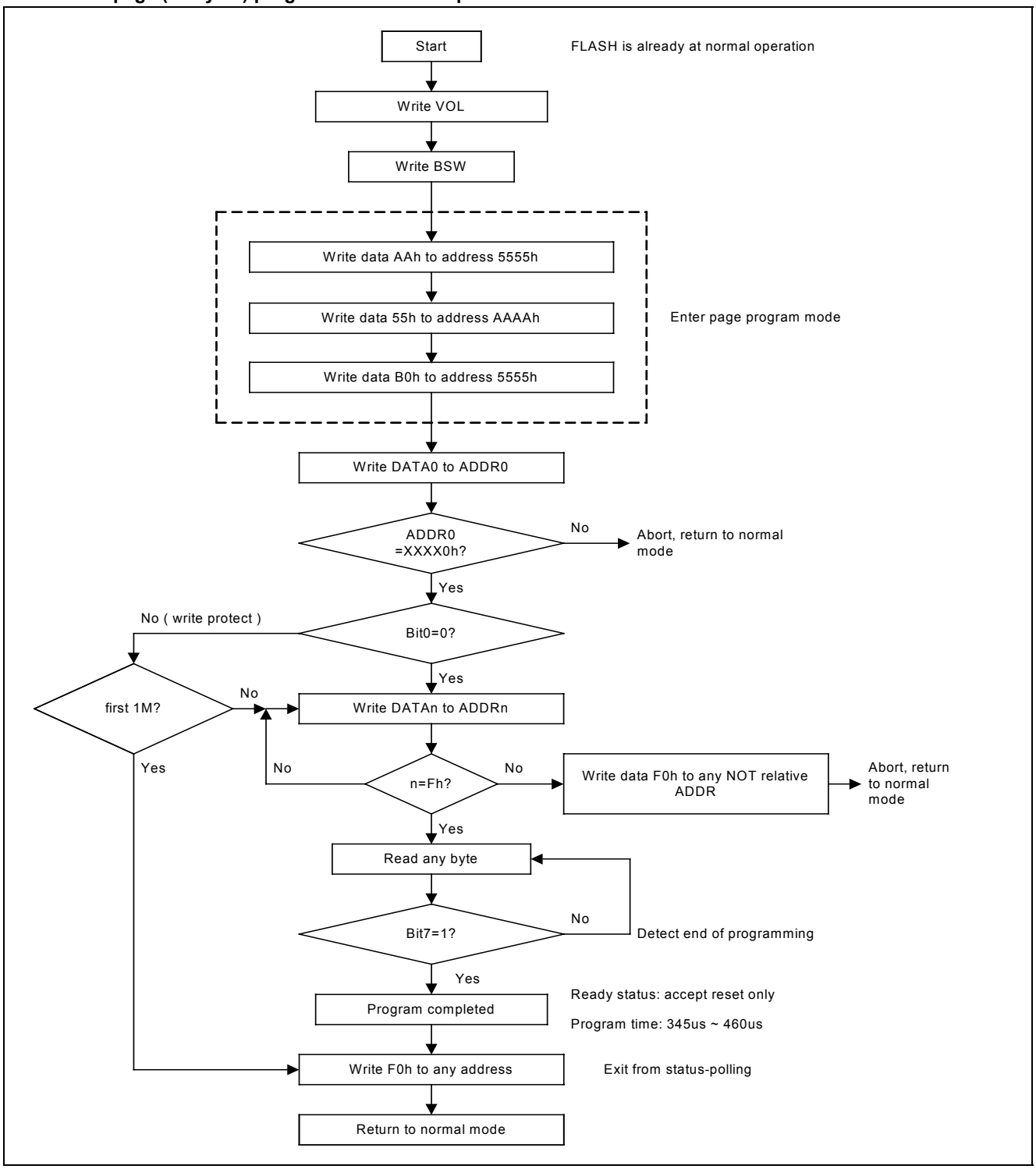
5.1.6.3. BMI read command sequence



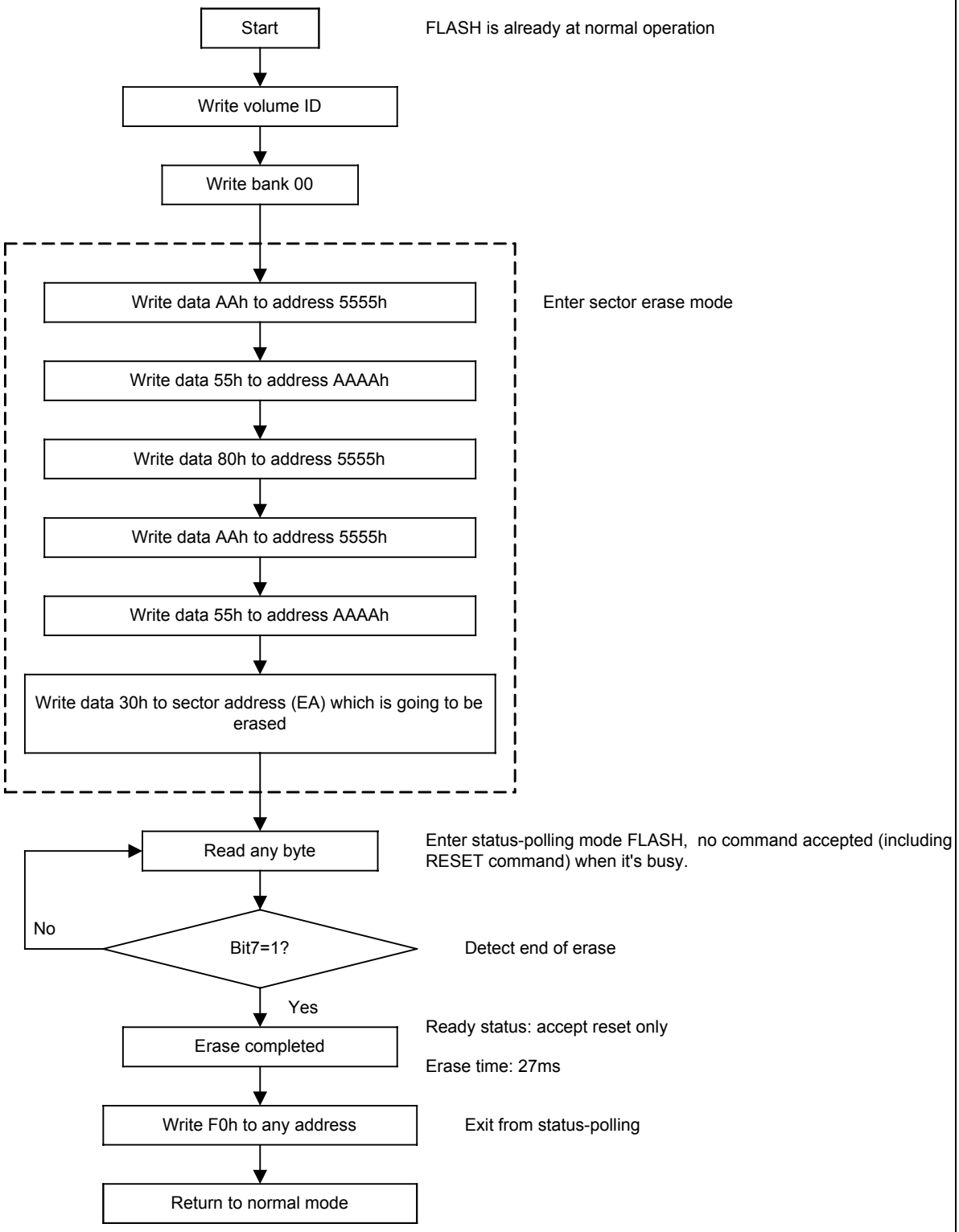
5.1.6.4. BMI byte program command sequence



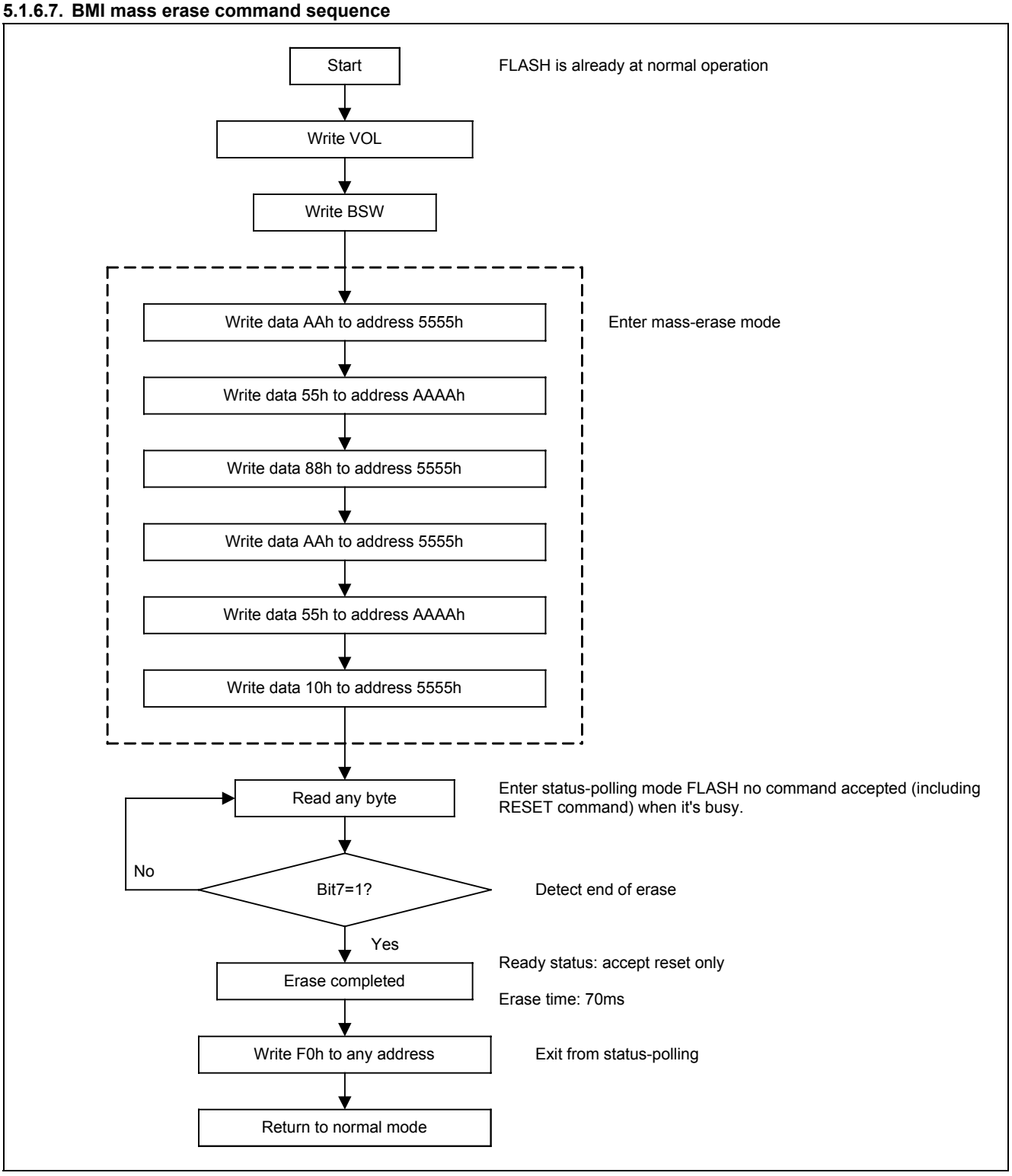
5.1.6.5. BMI page (16 bytes) program command sequence



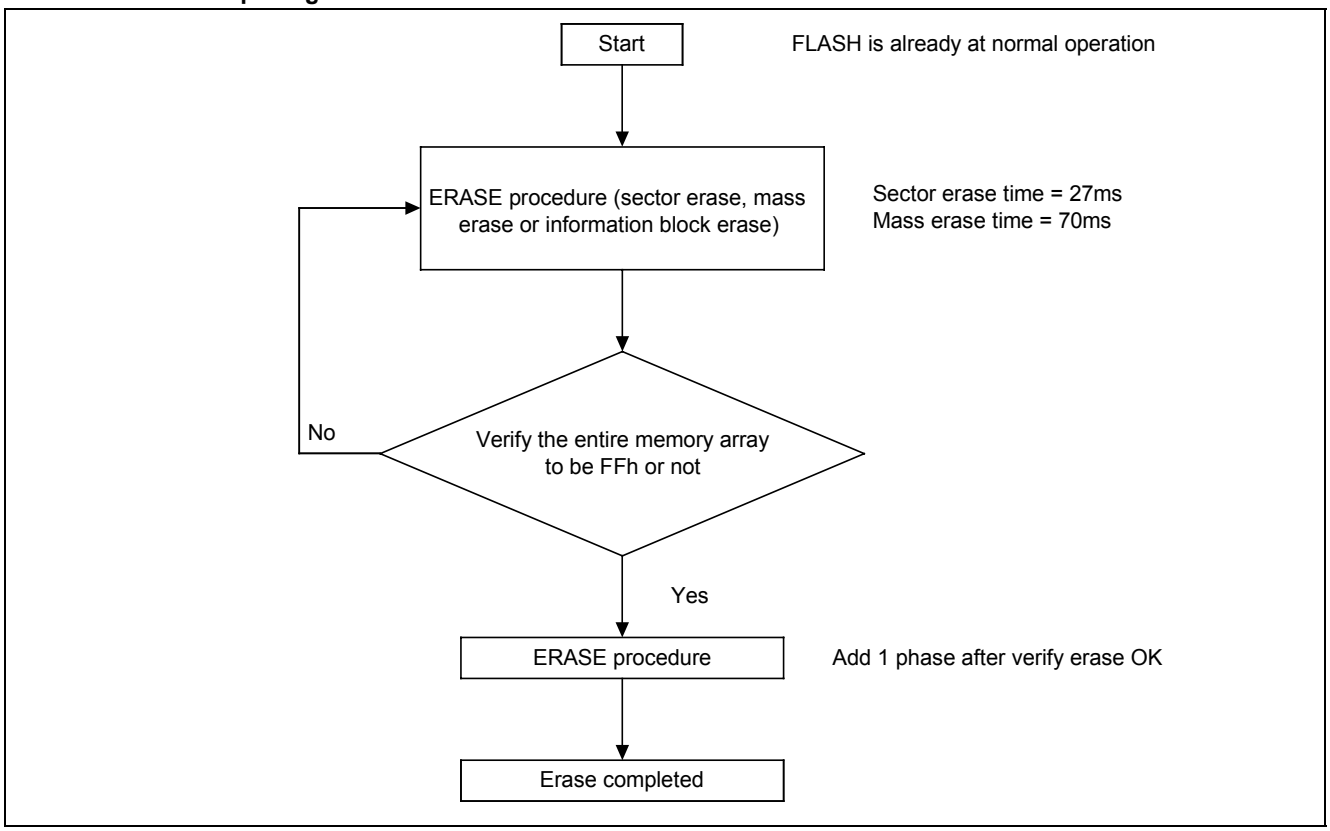
5.1.6.6. BMI sector (2K bytes) erase command sequence



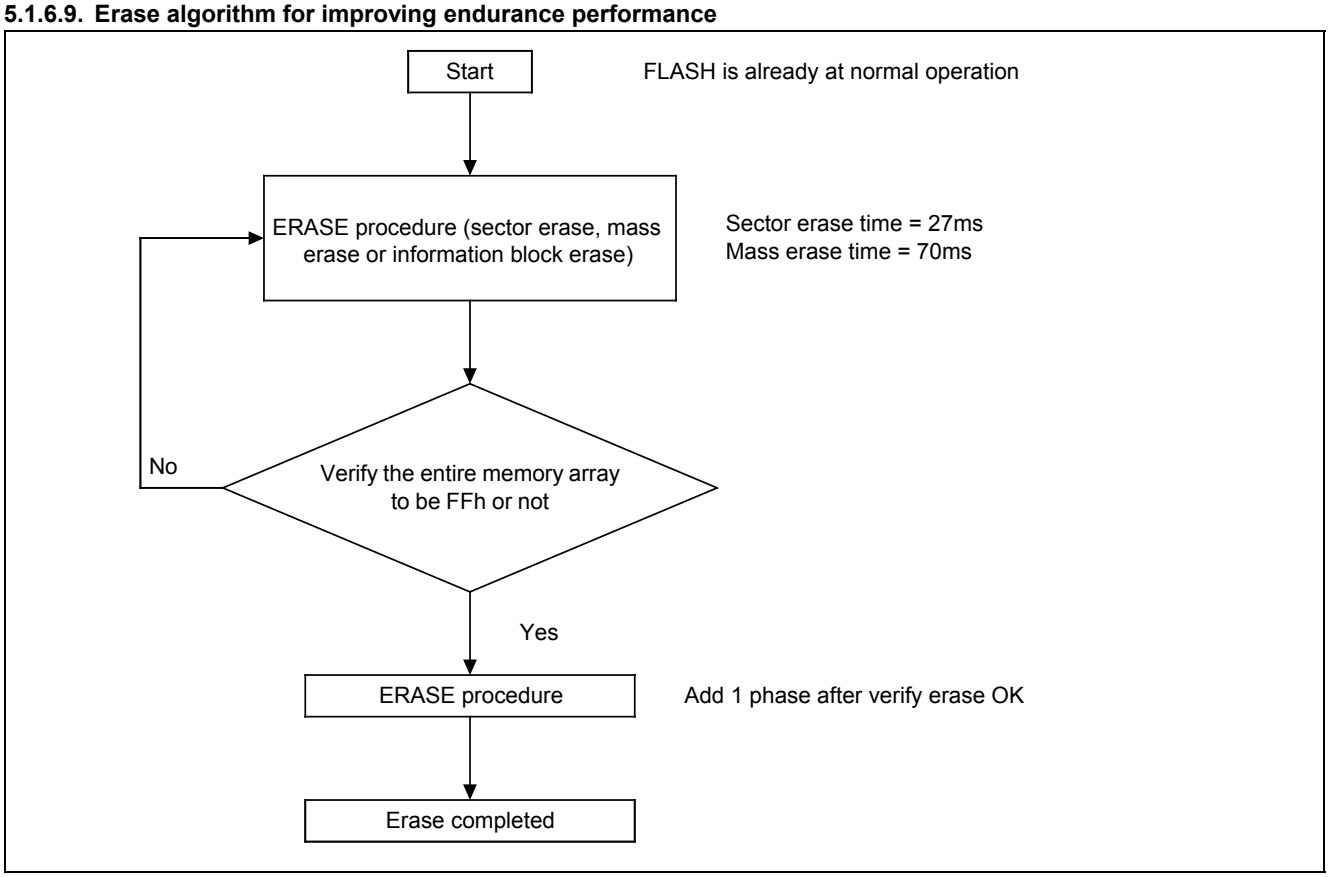
5.1.6.7. BMI mass erase command sequence



5.1.6.8. Enter status-polling mode from normal mode



5.1.6.9. Erase algorithm for improving endurance performance



5.2. Serial Interface (SIF)

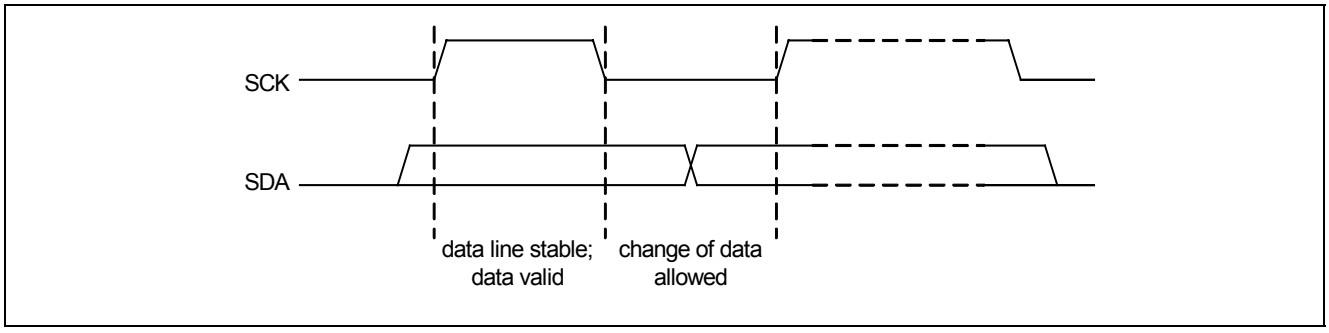
Using serial interface, PINs should be configured as follows:

Name	Description
CF0 - CF2	Set CF[2:0] = 111 to select SIF
CF3 - CF4	Cascade SIF configuration
CF7	FLASH/SRAM selector (0:FLASH, 1:SRAM)
AD0 - AD7	Not connected
MC0 - MC1	Not connected
$\overline{\text{RESET}}$	Reset (low active)
SCK	Serial clock
SDA	Serial data I/O
VDDQ	Power supply for 3.3V device.
VDDI	Power supply for 2.5V device.
VSS, VSSQ	Ground

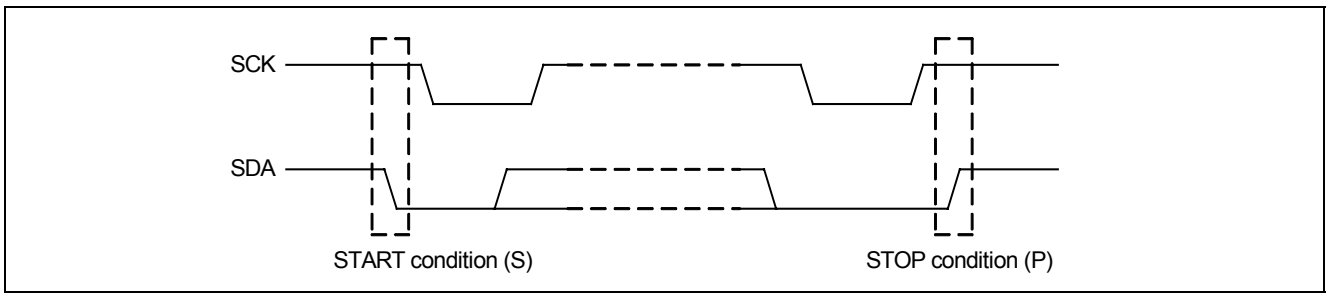
Note: PIN CF3 and CF4 are internal pull-low.

5.2.1. BIT transfer

One clock pulse is generated for each data bit transferring. The data on SDA line must be stabilized during the clock HIGH period. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCK line is LOW.



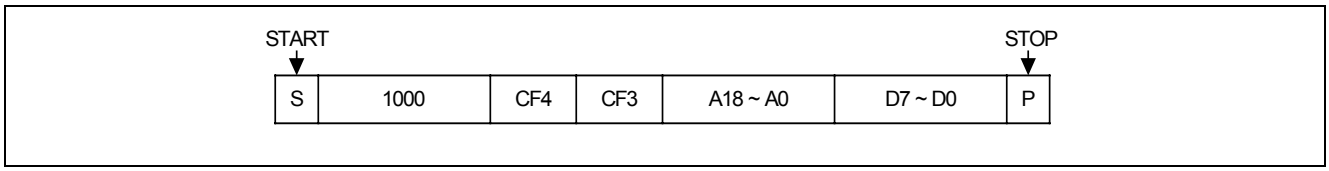
Within the procedure of the SUNPLUS Serial Interface, unique conditions (defined as START (S) and STOP (P)) arise. A HIGH to LOW transition on SDA line while SCK is HIGH indicates a START condition. A LOW to HIGH transition on SDA line while SCK is HIGH defines a STOP condition.



5.2.2. Instruction set

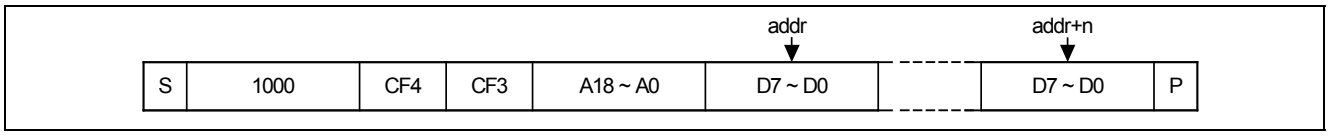
5.2.2.1. READ with random address access (CF7 = 0: FLASH, CF7 = 1: SRAM)

FLASH READ command composes of a start bit followed by: a 4-bit opcode (A[24:21] = 1000), a 2-bit memory selection, and a 19-bit address (A[18:0]) location. After receiving FLASH READ command, the SDA line should be set to high-impedance. SPR4096A will begin shifting out the data addressed (MSB first) on the falling edge of the SCK clock and the output data bit will be stable after the specified time delay (t_{ACC}). After 8 data bits are shifted out, a stop bit is required to terminate the command. SRAM READ command is the same as FLASH READ except CF7 = 1.



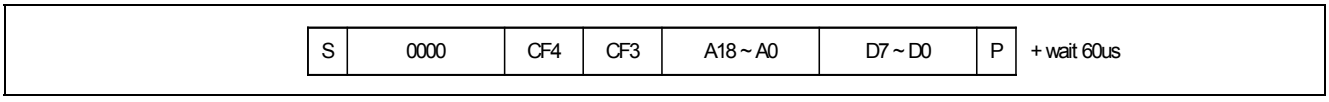
5.2.2.2. READ with auto-address-count (CF7 = 0: FLASH, CF7 = 1: SRAM)

FLASH READ with auto-address-count command is the same as FLASH READ except no stop bit is inserted before the next SCK falling edge, after the first 8 data bits are shifted out. SPR4096A will automatically increment the address by 1 and its data content will be shifted out proceeded by the clock cycle. The procedure continues until a stop bit is received. SRAM READ with auto-address-count command is the same as FLASH READ with auto-address-count except CF7 = 1.



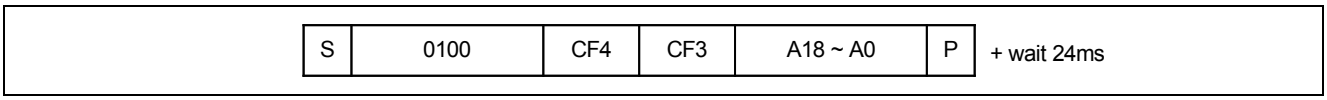
5.2.2.3. BYTE program (CF7 = 0: FLASH, CF7 = 1: SRAM)

FLASH BYTE PROGRAM command is a start bit followed by: a 4-bit opcode (A[24:21] = 0000), a 2-bit memory selection, a 19-bit address location (A[18:0]), and an 8-bit data (D[7:0]). After receiving FLASH BYTE PROGRAM command, a specified interval (t_{PGM}) is necessary to program data into FLASH. After all, a stop bit terminates the command. SRAM WRITE command is the same as FLASH BYTE PROGRAM except CF7 = 1 and no wait time is necessary.



5.2.2.4. Flash sector erase

FLASH SECTOR ERASE command is a start bit followed by: a 4-bit opcode (A[24:21] = 0100), a 2-bit memory selection, and a 19-bit address location (A[18:0]). The A18 to A11 determines which sector to be erased. The A10 to A0 are “DON’T CARE”. After receiving FLASH SECTOR ERASE command, a specified interval (t_{ERASE}) is needed to erase the selected sector of the FLASH. After that, a stop bit terminates the command.



5.2.2.5. Flash mass erase

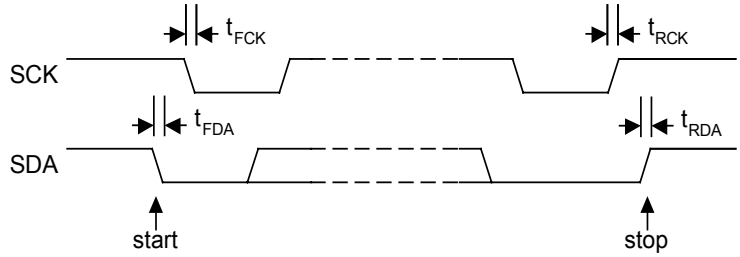
FLASH MASS ERASE command is a start bit followed by: a 4-bit opcode (A[24:21] = 0110), a 2-bit memory selection and a 19-bit address location (A[18:0]). The A18 to A0 are “DON’T CARE”. After receiving main block MASS ERASE command, a specified interval (t_{MASS}) is needed to erase the information block and/or main block of the FLASH. Finally, a stop bit terminates the command.

S	0110	CF4	CF3	A18 ~ A0	P	+ wait 70ms

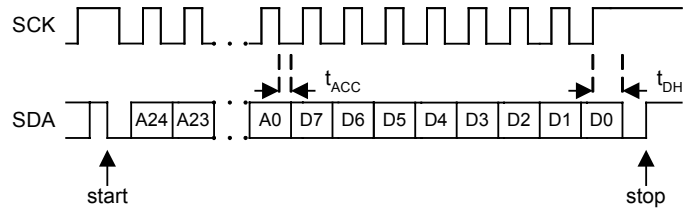
5.2.3. SIF AC characteristics

5.2.3.1. AC characteristics (VDD = 2.85V - 3.15V, T_A = 0 - 70℃)

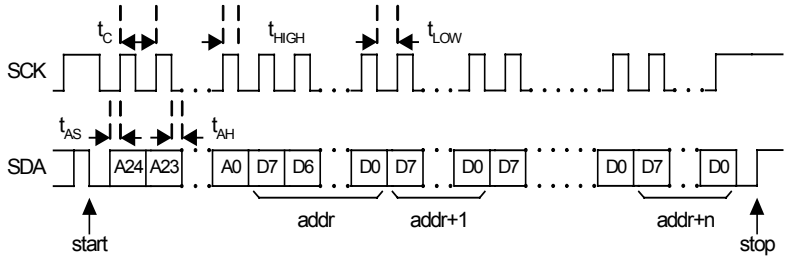
Characteristic	Symbol	Max.	Min.	Unit
Period of SCK	t_C	-	200	ns
Low period of SCK clock	t_{LOW}	-	85	ns
High period of SCK clock	t_{HIGH}	-	85	ns
Address setup time	t_{AS}	-	15	ns
Address hold time	t_{AH}	-	15	ns
READ access time	t_{ACC}	35	15	ns
READ data hold time	t_{DH}	-	15	ns
PROGRAM data setup time	t_{PDS}	-	15	ns
PROGRAM data hold time	t_{PDH}	-	15	ns
PROGRAM time	t_{PGM}	-	60	μs
ERASE time	t_{ERASE}	-	24	ms
MASS ERASE time	t_{MASS}	-	70	ms
Rise time of SCK	t_{RCK}	15	-	ns
Fall time of SCK	t_{FCK}	15	-	ns
Rise time of SDA	t_{RDA}	15	-	ns
Fall time of SDA	t_{FDA}	15	-	ns



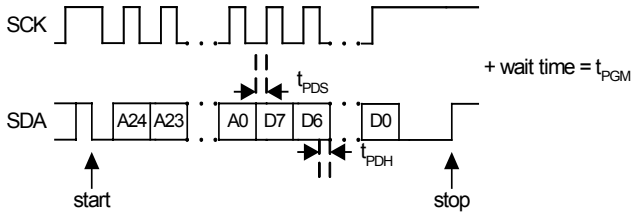
1). Read Command



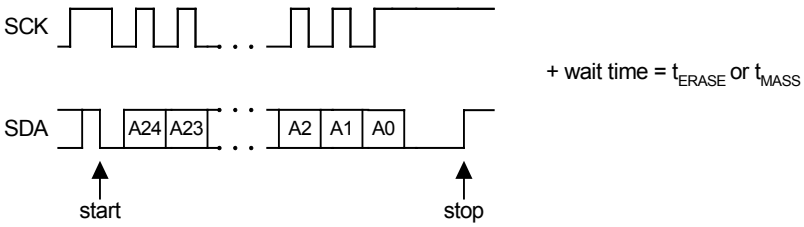
2). Read Command with Auto-Address-Count



3). Program Command



4). Sector Erase and Mass Erase Command



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Ambient Operating Temperature	T_A	-10℃ ~ 80℃
Storage Temperature	T_{STG}	-65℃ ~ 150℃
Supply Voltage to Ground Potential	VDD	-0.4V ~ 4.0V
Output Voltage	V_{OUT}	-0.4V ~ VDD + 0.4V
Input Voltage	V_{IN}	-0.4V ~ VDD + 0.4V

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. Recommended DC Operating Conditions (V_{DDQ} = 2.25V - 3.6V, V_{DDI} = 2.25V - 2.75V, T_A = 0 - 70℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
External Supply Voltage	V_{DDQ}	2.25	3.0	3.6	V
Internal Supply Voltage	V_{DDI}	2.25	2.5	2.75	V
Supply Voltage	VSS	-	0.0	-	V
Input High Voltage	V_{IH}	2.2	-	VDD + 0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.4	V

6.3. DC Electrical Characteristics (V_{DDQ} = 2.25V - 3.6V, V_{DDI} = 2.25V - 2.75V, T_A = 0 - 70℃)

Characteristic	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	2.3	-	-	V	I_{OH} = -1.0mA
Output Low Voltage	V_{OL}	-	-	0.3	V	I_{OL} = 1.0mA
Input Leakage Current	$I_{I(L)}$	-	-	1.0	μA	
Output Leakage Current	$I_{O(L)}$	-	-	1.0	μA	
Operating Supply Current (f = 5.0MHz), C_L = 80pF	I_{CC}	-	-	6.0	mA	
Standby Current (CMOS)	I_{SB}	-	-	4.0	μA	MC0 = MC1 = V_{DDQ}, AD[0:7] = VSS

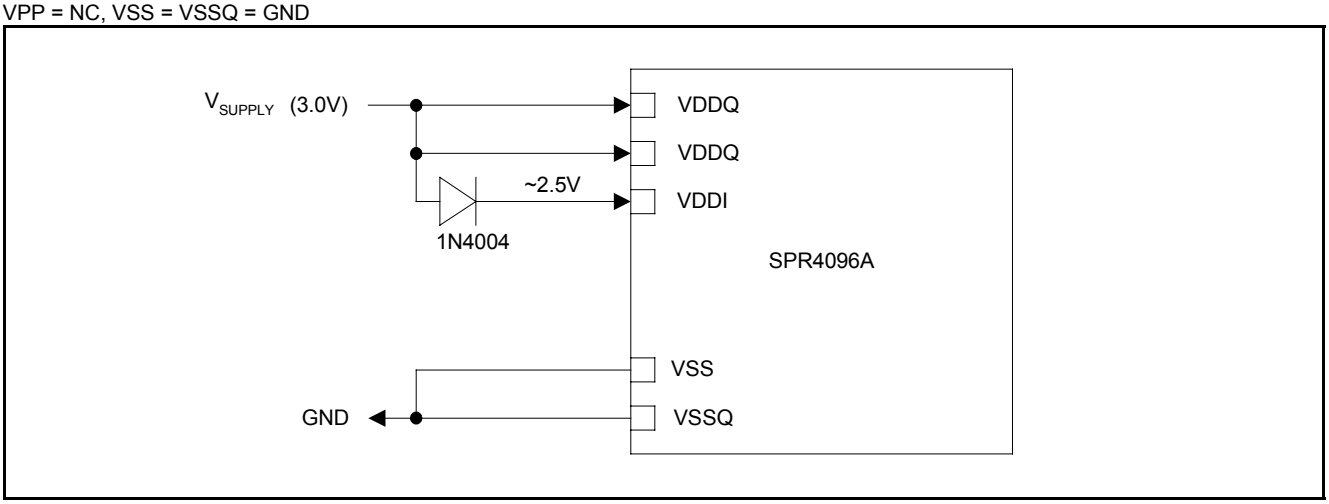
7. APPLICATION CIRCUITS

7.1. Power Supply Voltage

V_{SUPPLY} (working voltage) > 2.75V

VDDQ = V_{SUPPLY}, VDDI = Voltage dropped by diode

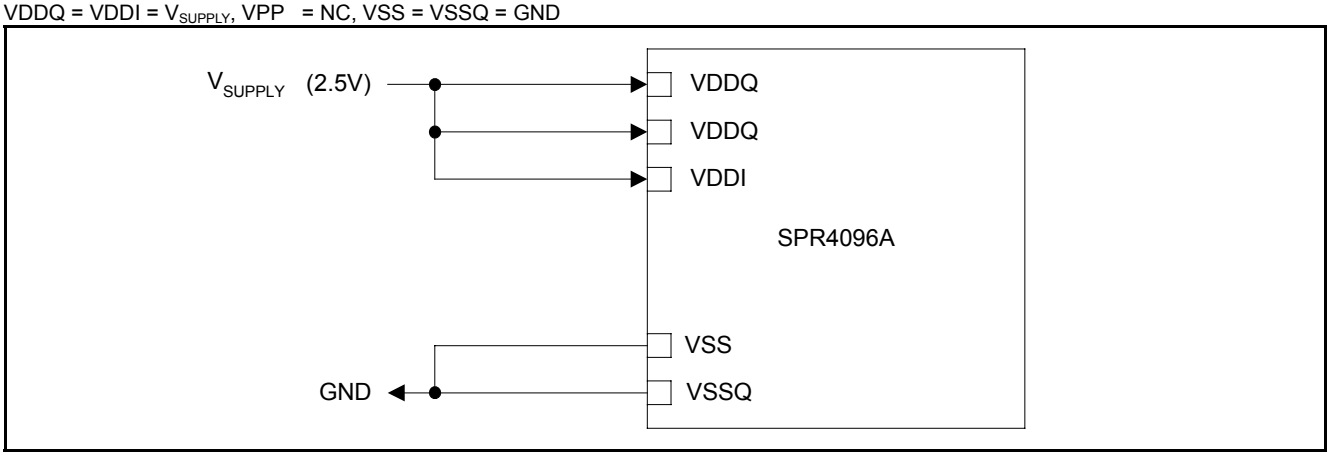
VPP = NC, VSS = VSSQ = GND



Note: The VDDI PIN must work at 2.25V - 2.75V for reliability consideration.

V_{SUPPLY} (working voltage) < 2.75V

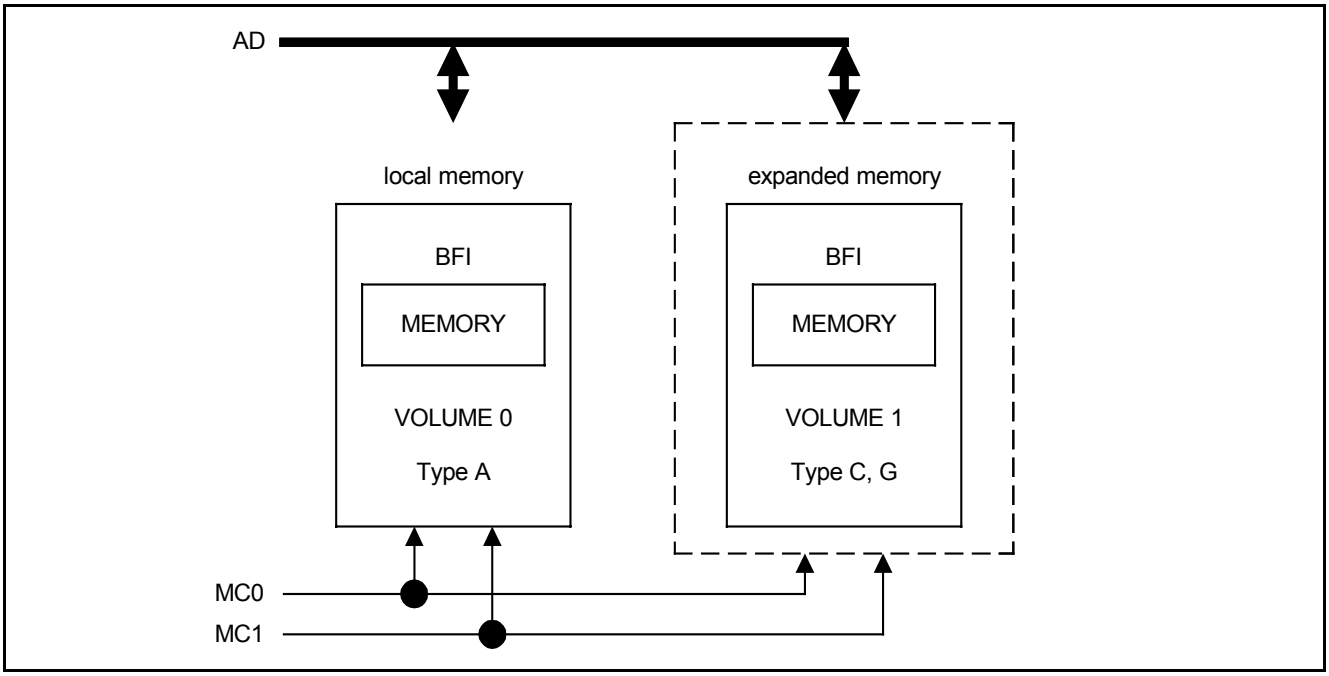
VDDQ = VDDI = V_{SUPPLY}, VPP = NC, VSS = VSSQ = GND



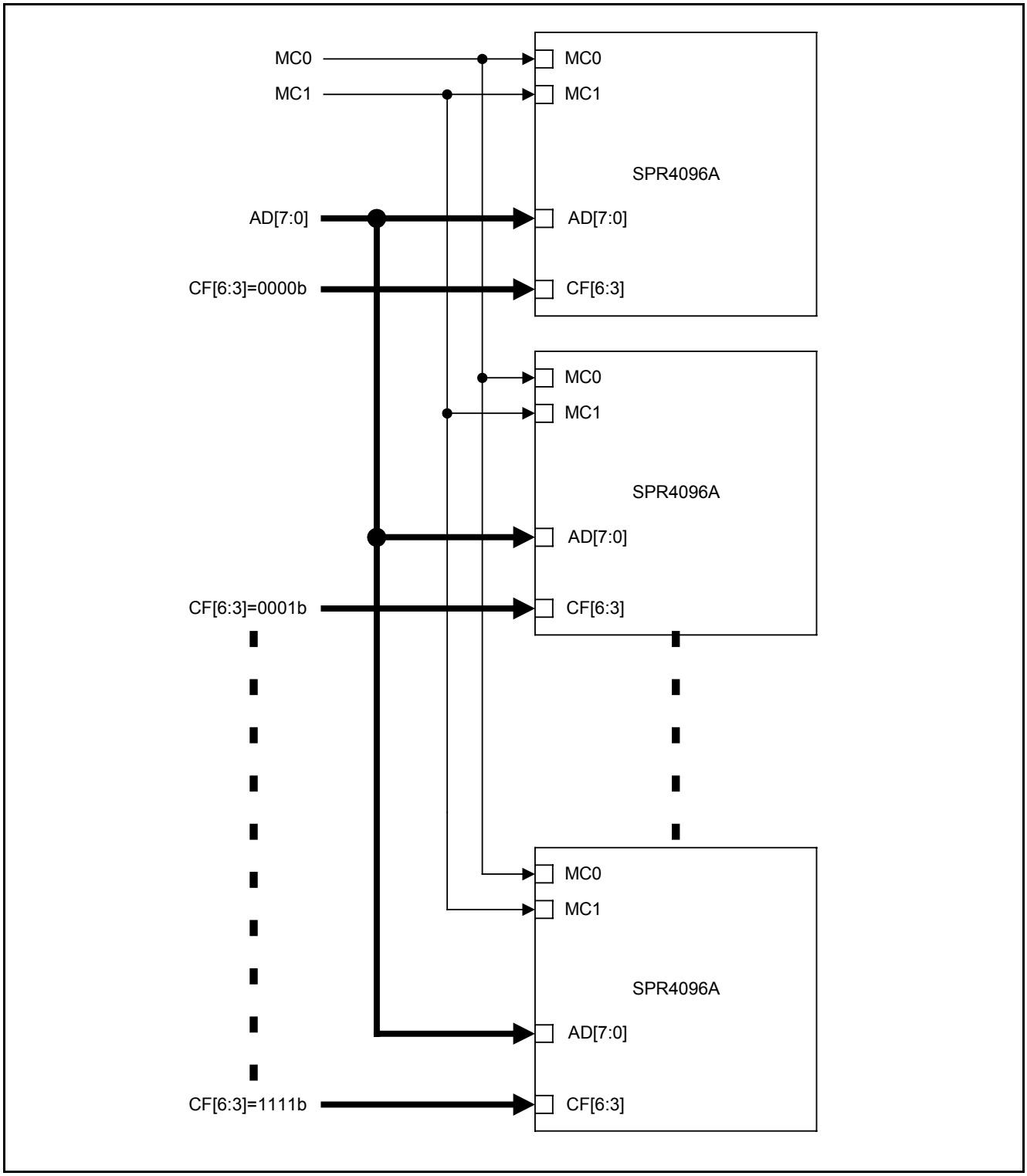
7.2. Bus Interface

7.2.1. Cascade access mode (type A, C, G)

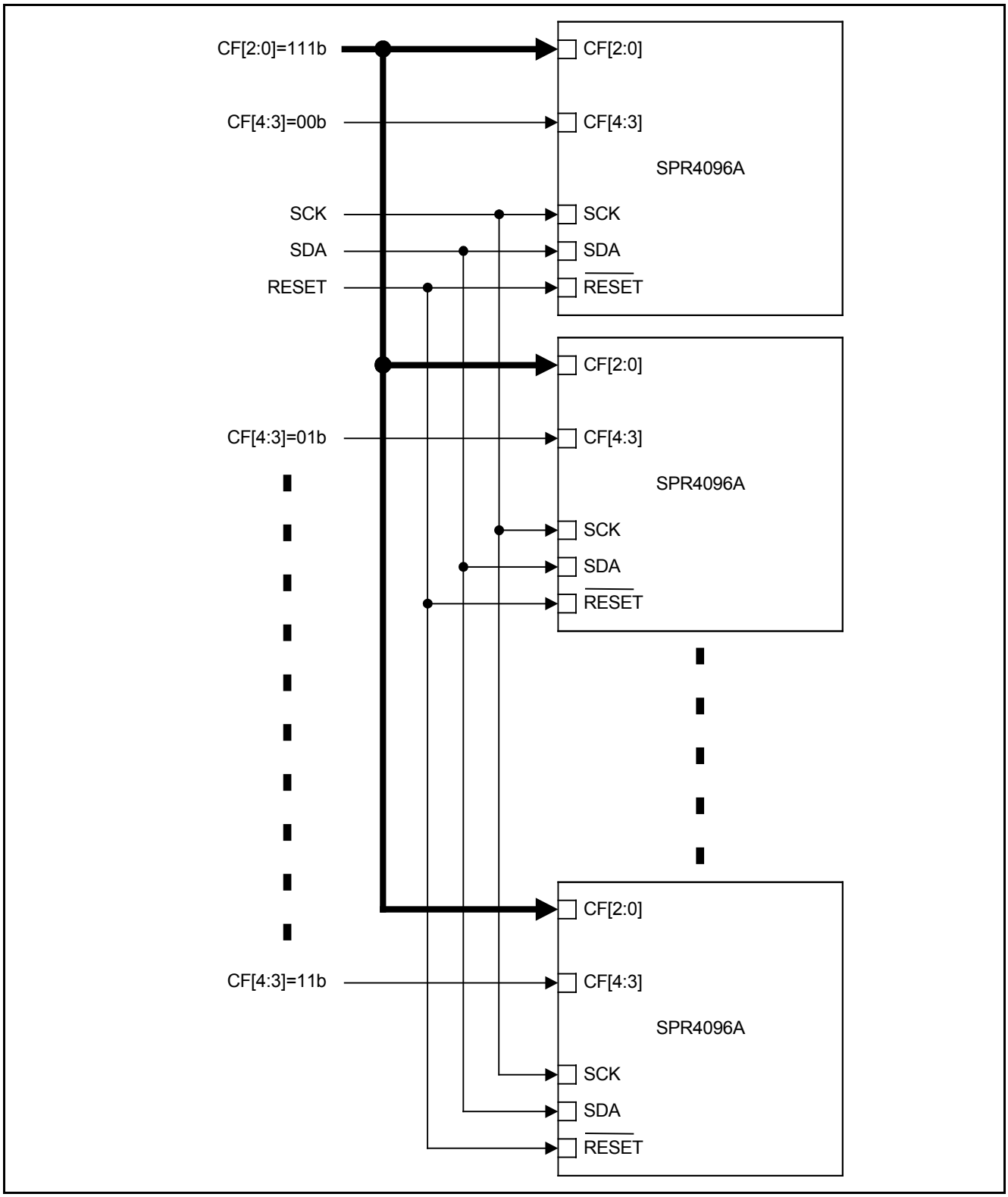
To expand memory in SPR4096A, a cascade access mode is designed to identify local memory and expanded memory. It is defined by the configuration control signal, mentioned in the previous section. For old version of SPL series, it is recommended to expand only to volume 1 (The built-in volume ID is fixed to 1 for Type C and Type G).



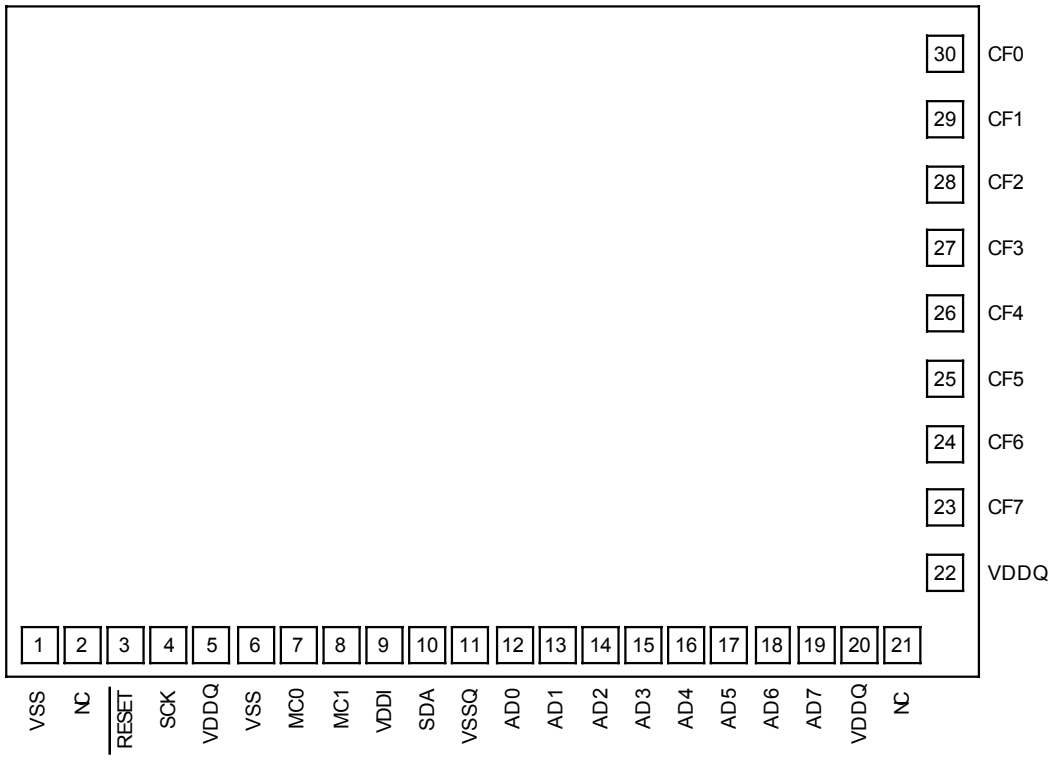
7.2.2. Bus Interface



7.3. Serial Interface



8. PACKAGE / PAD LOCATIONS



Chip Size : 2790μm × 3330μm

This IC substrate should be connected to VSS

Please contact Sunplus sales representatives for more information.

PAD No.	PAD Name	X	Y
1	VSS	113.50	
2	NC	233.50	
3	$\overline{\text{RESET}}$	353.50	
4	SCK	473.50	
5	VDDQ	593.48	
6	VSS	713.48	
7	MC0	833.48	
8	MC1	953.48	
9	VDDI	1073.48	
10	SDA	1198.48	
11	VSSQ	1318.48	110.00
12	AD0	1438.48	
13	AD1	1558.48	
14	AD2	1678.48	
15	AD3	1798.48	
16	AD4	1918.48	
17	AD5	2038.48	
18	AD6	2158.48	
19	AD7	2278.48	
20	VDDQ	2398.48	
21	NC	2574.00	120.00

22	VDDQ	2576.50	677.77
23	CF7		945.73
24	CF6		1208.57
25	CF5		1476.53
26	CF4		1739.37
27	CF3		2007.33
28	CF2		2270.17
29	CF1		2538.13
30	CF0		2800.97

8.1 DIP24

PAD Name	PIN No.	PAD Name	PIN No.
VDDI	1	NC	13
SDA	2	NC	14
VSSQ	3	NC	15
VDDQ	4	NC	16
CF7	5	NC	17
CF4	6	NC	18
CF3	7	NC	19
CF2~0	8	VSS	20
NC	9	$\overline{\text{RESET}}$	21
NC	10	SCK	22
NC	11	VDDQ	23
NC	12	VSS	24

8.2 PLCC84

PAD Name	PIN No.	PAD Name	PIN No.
VSS	12	AD4	27
NC	13	AD5	28
$\overline{\text{RESET}}$	14	AD6	29
SCK	15	AD7	30
VDDQ	16	VDDQ	31
VSS	17	NC	32
MC0	18	VDDQ	33
MC1	19	CF7	34
VDDI	20	CF6	35
SDA	21	CF5	36
VSSQ	22	CF4	37
AD0	23	CF3	38
AD1	24	CF2	39

AD2	25	CF1	40
AD3	26	CF0	41

其他沒寫的腳位是 NC. 不接即可.

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9. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 01, 2003	1.2	Add two items: “Endurance: 20,000 Cycles (min)” and “Data Retention: 100 years under Room Temperature” in “*2. FEATURES*”	3
MAR. 12, 2003	1.1	Delete “*8. PACKAGE/PAD LOCATIONS*”	24 - 25
NOV. 29, 2002	1.0	Document Release	
JAN. 29, 2002	0.1	Original	