

CD4002M/CD4002C Dual 4-Input NOR Gate CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

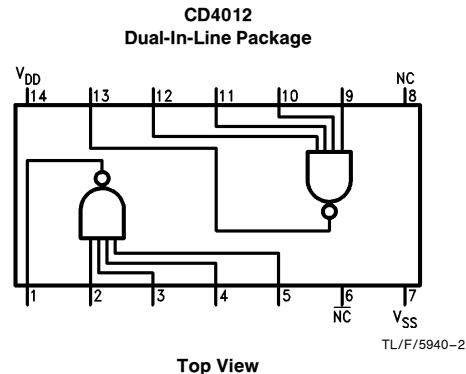
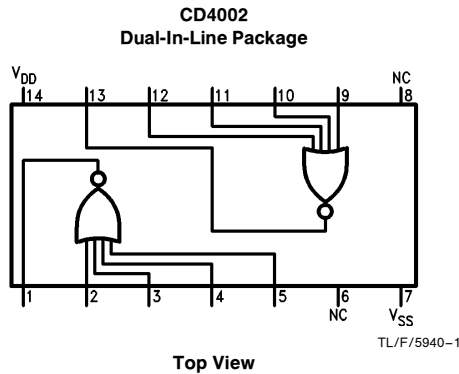
- Wide supply voltage range
- Low power
- High noise immunity

3.0V to 15V
10 nW (typ.)
0.45 V_{DD} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams



Order Number CD4002 or CD4012

CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$

Operating Temperature Range

CD4002M, CD4012M

CD4002C, CD4012C

$-55^{\circ}C$ to $+125^{\circ}C$

$-40^{\circ}C$ to $+85^{\circ}C$

Storage Temperature Range (T_S)

$-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)

Dual-In-Line

700 mW

Small Outline

500 mW

Operating Range (V_{DD})

$V_{SS} + 3.0V$ to $V_{SS} + 15V$

Lead Temperature (T_L)

(Soldering, 10 seconds)

$260^{\circ}C$

DC Electrical Characteristics CD4002M, CD4012M

Symbol	Parameter	Conditions	Limits							Units
			−55°C		+25°C			+125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5.0V V _{DD} = 10V		0.05 0.1		0.001 0.001	0.05 0.1		3.0 6	μA μA
P _D	Quiescent Device Dissipation/Package	V _{DD} = 5.0V V _{DD} = 10V		0.25 1.0		0.005 0.01	0.25 1.0		15 60	μW μW
V _{OL}	Output Voltage Low Level	V _{DD} = 5.0V, V _I = V _{DD} , I _O = 0A V _{DD} = 10V, V _I = V _{DD} , I _O = 0A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V _{OH}	Output Voltage High Level	V _{DD} = 5.0V, V _I = V _{SS} , I _O = 0A V _{DD} = 10V, V _I = V _{SS} , I _O = 0A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V _{NL}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O = 3.6V, I _O = 0A V _{DD} = 10V, V _O = 7.2V, I _O = 0A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V _{NH}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O = 0.95V, I _O = 0A V _{DD} = 10V, V _O = 2.9V, I _O = 0A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I _{DN}	Output Drive Current N-Channel (4002) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.5 1.1		0.40 0.9	1.0 2.5		0.28 0.65		mA mA
I _{DP}	Output Drive Current P-Channel (4002) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.62 −0.62		−0.5 −0.5	−2.0 −1.0		−0.35 −0.35		mA mA
I _{DN}	Output Drive Current N-Channel (4012) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.31 0.63		0.25 0.5	0.5 0.6		0.175 0.35		mA mA
I _{DP}	Output Drive Current P-Channel (4012) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.31 −0.75		−0.25 −0.6	−0.5 −1.2		−0.175 −0.4		mA mA
I _I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_{DN} and I_{DP} are tested one output at a time.

DC Electrical Characteristics CD4002C, CD4012C

Symbol	Parameter	Conditions	Limits							Units
			− 55°C		+ 25°C			+ 85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5.0V V _{DD} = 10V		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P _D	Quiescent Device Dissipation/Package	V _{DD} = 5.0V V _{DD} = 10V		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V _{OL}	Output Voltage Low Level	V _{DD} = 5.0V, V _I = V _{DD} , I _O = 0A V _{DD} = 10V, V _I = V _{DD} , I _O = 0A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V _{OH}	Output Voltage High Level	V _{DD} = 5.0V, V _I = V _{SS} , I _O = 0A V _{DD} = 10V, V _I = V _{SS} , I _O = 0A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V _{NL}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O ≥ 3.6V, I _O = 0A V _{DD} = 10V, V _O ≥ 7.2V, I _O = 0A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V _{NH}	Noise Immunity (All Inputs)	V _{DD} = 5.0V, V _O ≤ 0.95V, I _O = 0A V _{DD} = 10V, V _O ≤ 2.9V, I _O = 0A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I _{DN}	Output Drive Current N-Channel (4002) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I _{DN}	Output Drive Current N-Channel (4012) (Note 2)	V _{DD} = 5.0V, V _O = 0.4V, V _I = V _{DD} V _{DD} = 10V, V _O = 0.5V, V _I = V _{DD}	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I _{DP}	Output Drive Current P-Channel (4002) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I _{DP}	Output Drive Current P-Channel (4012) (Note 2)	V _{DD} = 5.0V, V _O = 2.5V, V _I = V _{SS} V _{DD} = 10V, V _O = 9.5V, V _I = V _{SS}	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I _I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_{DN} and I_{DP} are tested one output at a time.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4002M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		35	50	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		35	50	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		65	175	ns
		$V_{DD} = 10\text{V}$		35	75	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		65	125	ns
		$V_{DD} = 10\text{V}$		35	70	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4002C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		35	120	ns
		$V_{DD} = 10\text{V}$		25	65	ns
T_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		35	80	ns
		$V_{DD} = 10\text{V}$		25	55	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		65	300	ns
		$V_{DD} = 10\text{V}$		35	125	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		65	200	ns
		$V_{DD} = 10\text{V}$		35	115	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4012M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		50	75	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		50	75	ns
		$V_{DD} = 10\text{V}$		25	40	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		75	125	ns
		$V_{DD} = 10\text{V}$		50	75	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		75	100	ns
		$V_{DD} = 10\text{V}$		40	60	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4012C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0\text{V}$		50	100	ns
		$V_{DD} = 10\text{V}$		25	50	ns
T_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0\text{V}$		50	100	ns
		$V_{DD} = 10\text{V}$		25	50	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0\text{V}$		75	150	ns
		$V_{DD} = 10\text{V}$		50	100	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0\text{V}$		75	125	ns
		$V_{DD} = 10\text{V}$		40	75	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

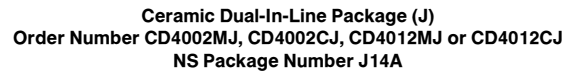
Physical Dimensions inches (millimeters)

The diagram shows the physical dimensions of the J14A Ceramic Dual-In-Line Package (J) in inches and millimeters. The package is a rectangular ceramic body with 14 pins (pins 1-7 on the bottom, pins 8-14 on the top) and a glass sealant on top. The dimensions are as follows:

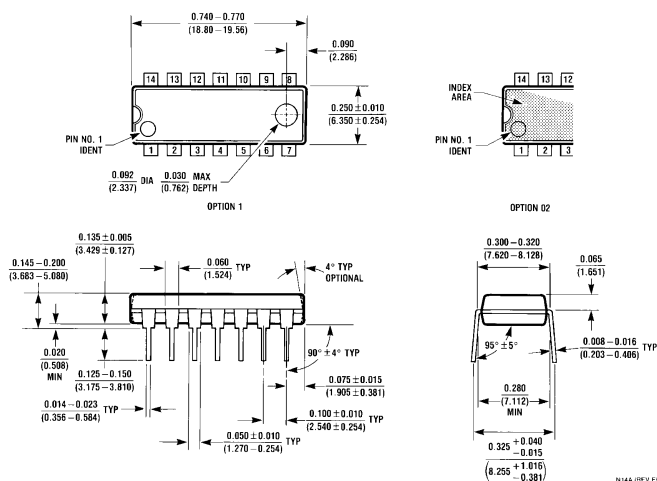
- Overall width: 0.785 (19.939) MAX
- Overall height: 0.220-0.310 (5.588-7.874)
- Pin pitch (center-to-center): 0.060 ± 0.005 (1.524 ± 0.127)
- Pin diameter: 0.018 ± 0.003 (0.457 ± 0.076)
- Pin length: 0.100 ± 0.010 (2.540 ± 0.254)
- Pin angle: 86°-94° TYP
- Pin spacing (from package edge): 0.008-0.012 (0.203-0.305)
- Pin spacing (from package edge): 0.098 (2.489)
- Pin spacing (from package edge): 0.125-0.200 (3.175-5.080)
- Pin spacing (from package edge): 0.150 (3.81) MIN
- Pin spacing (from package edge): 0.200 (5.080) MAX
- Pin spacing (from package edge): 0.020-0.060 (0.508-1.524)
- Pin spacing (from package edge): 0.025 (0.635) RAD
- Pin spacing (from package edge): 0.180 (4.572) MAX
- Pin spacing (from package edge): 0.290-0.320 (7.366-8.128)
- Pin spacing (from package edge): 0.310-0.410 (7.874-10.41)
- Pin spacing (from package edge): 10° MAX
- Pin spacing (from package edge): 95° ± 5°
- Pin spacing (from package edge): 0.005 (0.127) MIN
- Pin spacing (from package edge): 0.008-0.012 (0.203-0.305)
- Pin spacing (from package edge): 0.098 (2.489)
- Pin spacing (from package edge): 0.125-0.200 (3.175-5.080)
- Pin spacing (from package edge): 0.150 (3.81) MIN
- Pin spacing (from package edge): 0.200 (5.080) MAX
- Pin spacing (from package edge): 0.020-0.060 (0.508-1.524)
- Pin spacing (from package edge): 0.025 (0.635) RAD
- Pin spacing (from package edge): 0.180 (4.572) MAX
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- Pin spacing (from package edge): 0.310-0.410 (7.874-10.41)
- Pin spacing (from package edge): 10° MAX
- Pin spacing (from package edge): 95° ± 5°
- Pin spacing (from package edge): 0.005 (0.127) MIN
- Pin spacing (from package edge): 0.008-0.012 (0.203-0.305)
- Pin spacing (from package edge): 0.098 (2.489)
- Pin spacing (from package edge): 0.125-0.200 (3.175-5.080)
- Pin spacing (from package edge): 0.150 (3.81) MIN
- Pin spacing (from package edge): 0.200 (5.080) MAX
- Pin spacing (from package edge): 0.020-0.060 (0.508-1.524)

Ceramic Dual-In-Line Package (J)
Order Number CD4002MJ, CD4002CJ, CD4012MJ or CD4012CJ
NS Package Number J14A

J14A (REV G)



Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4002MN, CD4002CN, CD4012MN or CD4012CN
NS Package Number N14A

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