

CD4517BMS

CMOS Dual 64-Stage Static Shift Register

December 1992

Features

- High-Voltage Types (20-Volt Rating)
- Low Quiescent Current 10nA/pkg (Typ.) at VDD = 5V
- Clock Frequency 12MHz (Typ.) at VDD = 10V
- Schmitt Trigger Clock Inputs Allow Operation with Very Slow Clock Rise and Fall Times
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load, or Two HTL Loads
- 3-State Outputs
- 100% Tested for Quiescent Current at 20V
- · Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

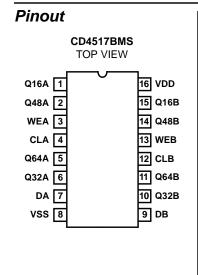
- · Time-delay Circuits
- · Scratch-pad Memories
- General-purpose Serial Shift-register Applications

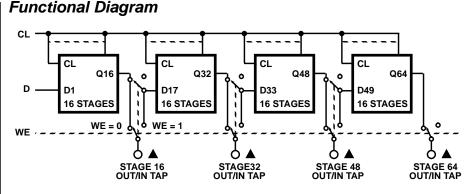
Description

CD4517BMS dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32rd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the opeation of the CD4517BMS. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

The CD4517BMS is supplied in these 16 lead outline packages:

Braze Seal DIP H4X
Frit Seal DIP H1F
Ceramic Flatpack H6P





Reliability Information Absolute Maximum Ratings Thermal Resistance Ceramic DIP and FRIT Package θ_{ja} Clathack Package DC Supply Voltage Range, (VDD) -0.5V to +20V (Voltage Referenced to VSS Terminals) Flatpack Package 70°C/W Input Voltage Range, All Inputs -0.5V to VDD +0.5V 20°C/W Maximum Package Power Dissipation (PD) at +125°C DC Input Current, Any One Input±10mA For $T_A = -55^{\circ}C$ to $+100^{\circ}C$ (Package Type D, F, K) 500mW Operating Temperature Range.....-55°C to +125°C For $T_A = +100^{\circ}C$ to $+125^{\circ}C$ (Package Type D, F, K). Derate Package Types D, F, K, H Storage Temperature Range (TSTG) -65°C to +150°C Linearity at 12mW/°C to 200mW Lead Temperature (During Soldering) +265°C Device Dissipation per Output Transistor 100mW For T_A = Full Package Temperature Range (All Package Types) At Distance 1/16 \pm 1/32 Inch (1.59mm \pm 0.79mm) from case for 10s Maximum

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

				GROUP A		LIN	IITS	
PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VD	D or GND	1	+25°C	-	10	μΑ
				2	+125°C	-	1000	μΑ
		VDD = 18V, VIN = VD	D or GND	3	-55°C	-	10	μΑ
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load	(Note 3)	1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.	4V	1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0).5V	1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1	1.5V	1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.	6V	1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.	5V	1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10	μΑ	1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μΑ	4	1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND VDD = 20V, VIN = VDD or GND		7	+25°C	VOH> V	VOL <	V
				7	+25°C	VDD/2	VDD/2	
		VDD = 18V, VIN = VD	D or GND	8A	+125°C	İ		
		VDD = 3V, VIN = VDD or GND		8B	-55°C	1		
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5	V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5	V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13 VOL < 1.5V	3.5V,	1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13 VOL < 1.5V	3.5V,	1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output	IOZL	VIN = VDD or GND	VDD = 20V	1	+25°C	-0.4	-	μΑ
Leakage		VOUT = 0V		2	+125°C	-12	-	μΑ
			VDD = 18V	3	-55°C	-0.4	-	μΑ
Tri-State Output	IOZH	VIN = VDD or GND	VDD = 20V	1	+25°C	-	0.4	μΑ
Leakage		VOUT = VDD		2	+125°C	-	12	μΑ
			VDD = 18V	3	-55°C	-	0.4	μΑ
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NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.

3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

2. Go/No Go test with limits applied to inputs.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

			GROUP A		LIM	IITS	
PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	SUBGROUPS	TEMPERATURE	MIN	MAX	UNITS
Propagation Delay TPH		VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
Clock to 16	TPLH		10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
	TTLH		10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
Frequency			10, 11	+125°C, -55°C	2.22	-	MHz

NOTES:

- 1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
- 2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

					LIMITS		
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μΑ
				+125°C	-	150	μΑ
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μА
				+125°C	-	300	μА
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μА
				+125°C	-	600	μА
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	٧

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

					LIN	IITS	
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
Propagation Delay	TPHL	VDD = 10V	1, 2, 3	+25°C	-	220	ns
Clock to Q16	TPLH	VDD = 15V	1, 2, 3	+25°C	-	180	ns
Propagation Delay	TPHZ, ZH	VDD = 5V	1, 2, 5	+25°C	-	150	ns
3-State WE to Q16	TPLZ, ZL	VDD = 10V	1, 2, 4	+25°C	-	80	ns
		VDD = 15V	1, 2, 4	+25°C	=	60	ns
Transition Time	TTHL	VDD = 10V	1, 2, 3	+25°C	=	100	ns
	TTLH	VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input	FCL	VDD = 10V	1, 2	+25°C	6	-	MHz
Frequency		VDD = 15V	1, 2	+25°C	8	-	MHz
Minimum Data to Clock	TS	VDD = 5V	1, 2, 3	+25°C	-	20	ns
Setup Time		VDD = 10V	1, 2, 3	+25°C	-	10	ns
		VDD = 15V	1, 2, 3	+25°C	-	10	ns
Minimum Data to Clock	TH	VDD = 5V	1, 2, 3	+25°C	-	200	ns
Hold Time		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Clock Pulse	TW	VDD = 5V	1, 2, 3	+25°C	-	180	ns
Width		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Write Enable -	TR	VDD = 5V	1, 2, 3	+25°C	-	100	ns
to-Clock Release Time		VDD = 10V	1, 2, 3	+25°C	-	50	ns
		VDD = 15V	1, 2, 3	+25°C	-	40	ns
Write Enable-to-Clock	TS	VDD = 5V	1, 2, 3	+25°C	0	-	ns
Setup Time		VDD = 10V	1, 2, 3	+25°C	0	-	ns
		VDD = 15V	1, 2, 3	+25°C	0	-	ns
Maximum Clock Input	TRCL	VDD = 5V	1, 2, 3, 5	+25°C	-	15	μs
Rise and Fall Time	TFCL	VDD = 10V	1, 2, 3, 5	+25°C	-	5	μs
		VDD = 15V	1, 2, 3, 5	+25°C	-	5	μs
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

- 1. All voltages referenced to device GND.
- 2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
- 3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
- 4. Measured at the point of 10% change in output with an output load 50pF, RL = $1K\Omega$ to VDD for TPZL and TPLZ and RL = $1K\Omega$ to VSS for TPZH and TPHZ
- 5. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

					LIM	LIMITS	
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μΑ
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	+25°C	=	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

					LIMITS		
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
P Threshold Voltage Delta	ΔVΤΡ	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND VDD = 3V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.

3. See Table 2 for +25°C limit.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFO	RMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test	1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note	: 1)	100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1.5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

	MIL-STD-883	MIL-STD-883		READ AND RECORD	
CONFORMANCE GROUPS	METHOD	PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

					OSCILLATOR	
FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	50kHz	25kHz
Static Burn-In 1 (Note 1)	1, 2, 5, 6, 10, 11, 14, 15	3, 4, 7-9, 12, 13	16			
Static Burn-In 2 (Note 1)	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16			
Dynamic Burn- In (Note 1)	-	3, 8, 13	16	1, 2, 5, 6, 10, 11, 14, 15	4, 12	7, 9

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS (Continued)

					OSCILLATOR	
FUNCTION	OPEN	GROUND	VDD	9V \pm -0.5V	50kHz	25kHz
Irradiation (Note 2)	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16			

NOTES:

- 1. Each pin except VDD and GND will have a series resistor of 10K \pm 5%, VDD = 18V \pm 0.5V
- 2. Each pin except VDD and GND will have a series resistor of 47K ±5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagram

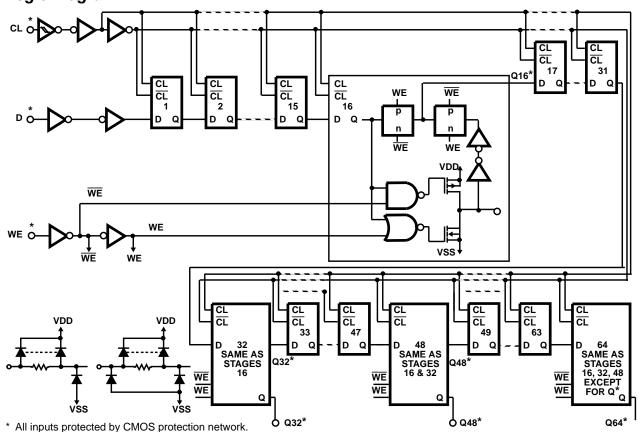


FIGURE 1. LOGIC BLOCK DIAGRAM
TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	STAGE 16 TAP	STAGE 32 TAP	STAGE 48 TAP	STAGE 64 TAP
0	0	Х	Q16	Q32	Q48	Q64
0	1	Х	Z	Z	Z	Z
1	0	Х	Q16	Q32	Q48	Q64
1	1	Х	Z	Z	Z	Z
	0	DI In	Q16	Q32	Q48	Q64
	1	DI In	D17 In	D33 In	D49 In	Z
	0	Х	Q16	Q32	Q48	Q64
	1	Х	Z	Z	Z	Z

1 = HIGH LEVEL

X = DON'T CARE

0 = LOW LEVEL

Z = HIGH IMPEDANCE

Typical Performance Characteristics

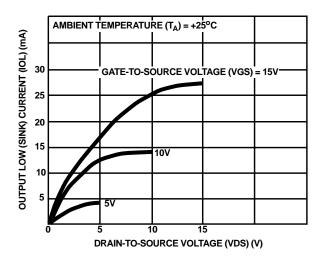


FIGURE 2. TYPICAL N-CHANNEL OUTPUT LOW (SINK)
CURRENT CHARACTERISTICS

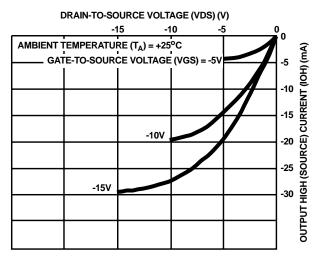


FIGURE 4. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE)
CURRENT CHARACTERISTICS

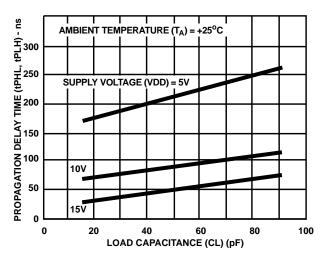


FIGURE 6. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

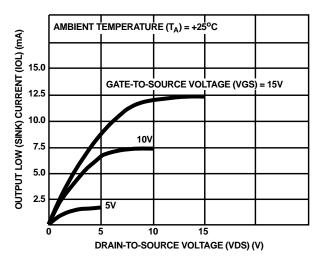


FIGURE 3. MINIMUM N-CHANNEL OUTPUT LOW (SINK)
CURRENT CHARACTERISTICS

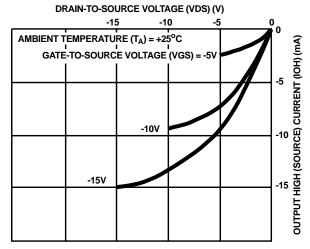


FIGURE 5. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE)
CURRENT CHARACTERISTICS

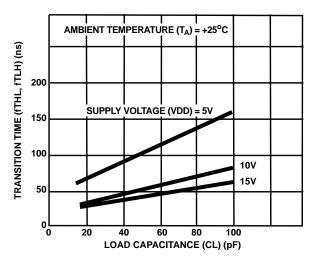


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

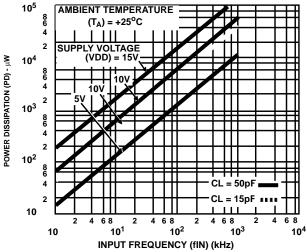
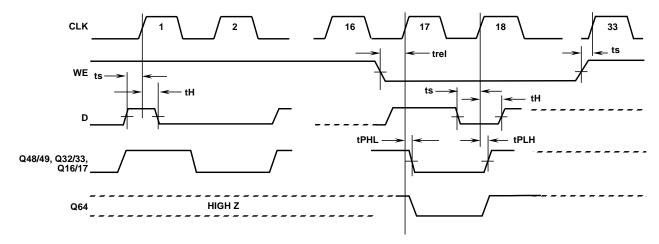


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Waveforms and Test Circuits



FIIGURE 9. DYNAMIC TEST WAVEFORMS

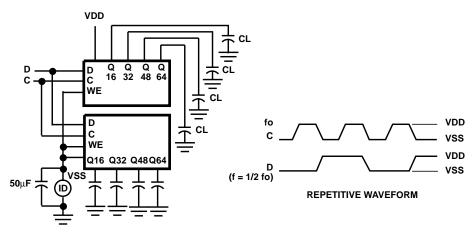
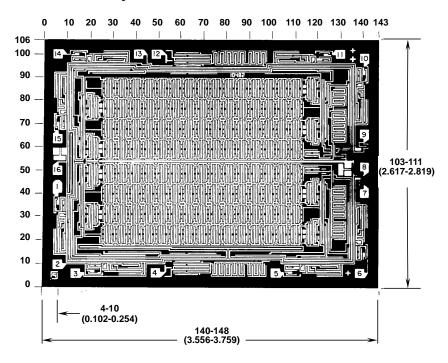


FIGURE 10. DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in milimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch.)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN **DIE THICKNESS:** 0.0198 inches - 0.0218 inches

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Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
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TEL: (321) 724-7000 FAX: (321) 724-7240

EUROPE

Intersil SA Mercure Center 100, Rue de la Fusee 1130 Brussels, Belgium TEL: (32) 2.724.2111 FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310

FAX: (886) 2 2715 3029