CD4033BMS

December 1992

CMOS Decade Counter/Divider

Features

- **High Voltage Types (20V Rating)**
- **Decoded 7 Segment Display Outputs and Ripple Blanking**
- **Counter and 7 Segment Decoding in One Package**
- **Easily Interfaced with 7 Segment Display Types**
- **Fully Static Counter Operation DC to 6MHz (typ.) at VDD = 10V**
- **Ideal for Low-Power Displays**
- **"Ripple Blanking" and Lamp Test**
- **100% Tested for Quiescent Current at 20V**
- **Standardized Symmetrical Output Characteristics**
- **5V, 10V and 15V Parametric Ratings**
- **Schmitt-Triggered Clock Inputs**
- **Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's**

Applications

- **Decade Counting 7 Segment Decimal Display**
- **Frequency Division 7 Segment Decimal Displays**
- **Clocks, Watches, Timers (e.g. ÷ 60, ÷ 60, ÷12 Counter/ Display**
- **Counter/Display Driver For Meter Applications**

Description

CD4033BMS consists of a 5 stage Johnson decade counter and an output decoder which converts the Johnson code to a 7 segment decoded output for driving one stage in a numerical display.

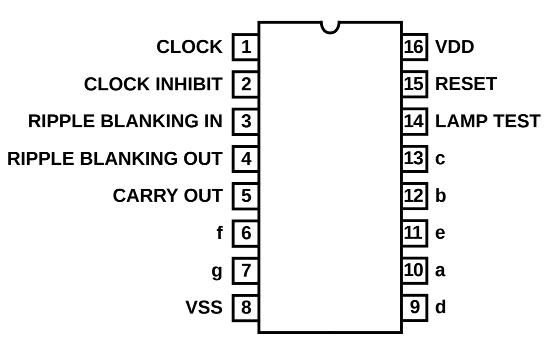
This device is particularly advantageous in display applications where low power dissipation and/or low package count is important.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (Cout) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

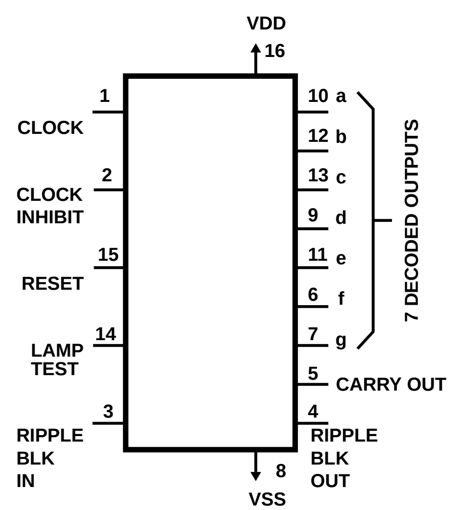
The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7 segment outputs go high on selection.

Pinout

CD4033BMS
TOP VIEW



Functional Diagram



The CD4033BMS has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033BMS associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033BMS in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033BMS on the interger side of the display.

On the fraction side of the display the RBI of the CD4033BMS associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033BMS is connected to the RBI terminal of the CD4033BMS in the next more-significant-bit position. Again, this procedure is continued for all CD4033BMS's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033BMS associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033BMS has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4033BMS are supplied in these 16 lead outline packages:

Braze Seal DIP	H4W
Frit Seal DIP	H2R
Ceramic Flatpack	H6W

Logic Diagram

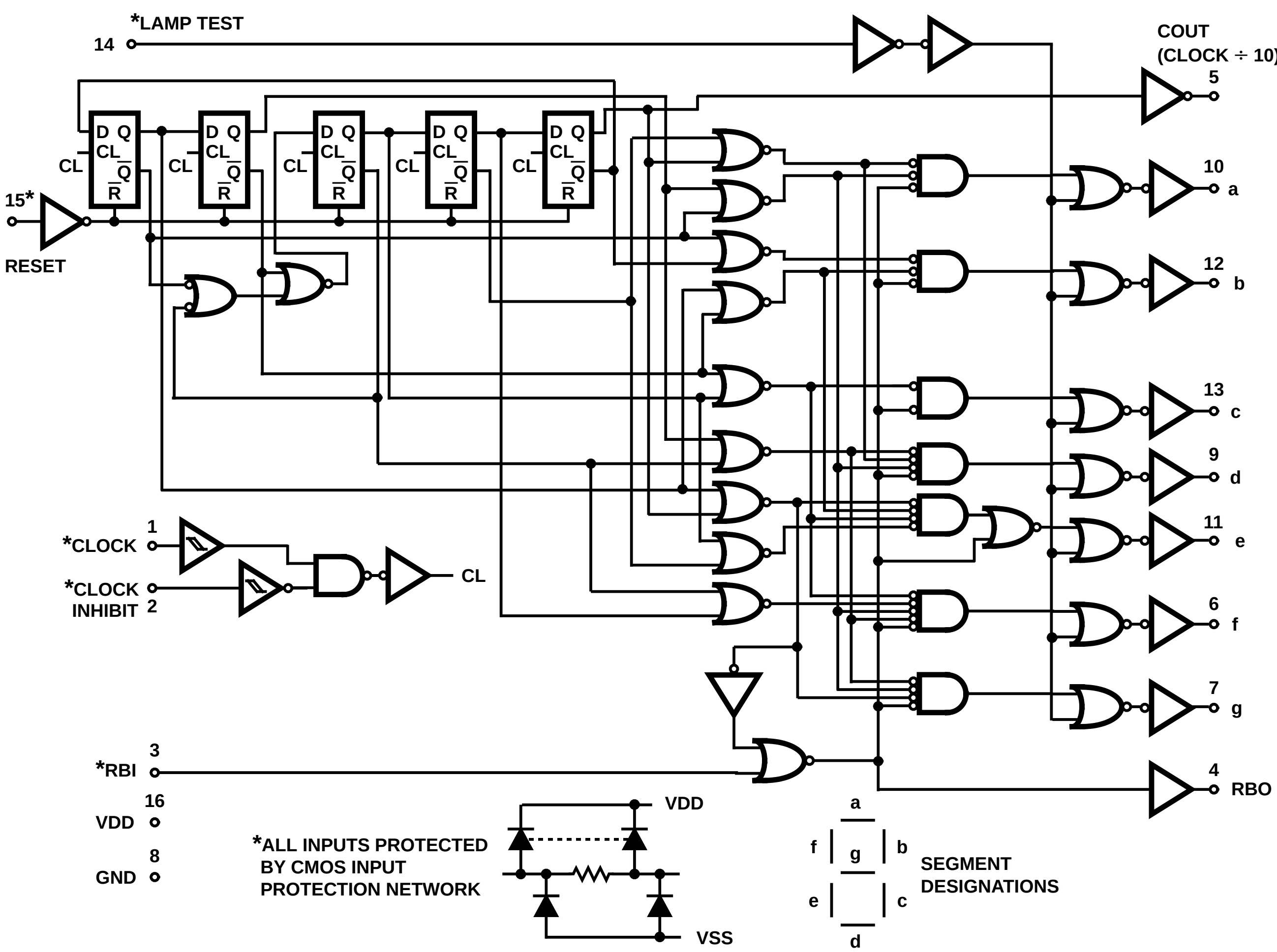


FIGURE 1. CD4033BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . .±10mA
Operating Temperature Range . . . . -55^oC to $+125^oC$
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering) . . . . $+265^oC$
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	$80^oC/W$	$20^oC/W$
Flatpack Package	$70^oC/W$	$20^oC/W$

Maximum Package Power Dissipation (PD) at $+125^oC$
For TA = -55^oC to $+100^oC$ (Package Type D, F, K) 500mW
For TA = $+100^oC$ to $+125^oC$ (Package Type D, F, K) . . . . . Derate Linearity at $12mW/^oC$ to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . $+175^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^oC$	-	10	µA
				2	$+125^oC$	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55^oC	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-100	-	nA
				2	$+125^oC$	-1000	-	nA
			VDD = 18V	3	-55^oC	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-	100	nA
				2	$+125^oC$	-	1000	nA
			VDD = 18V	3	-55^oC	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^oC$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^oC$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^oC$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^oC$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^oC$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^oC$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^oC$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	$+25^oC$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	$+25^oC$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^oC$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^oC$			
		VDD = 3V, VIN = VDD or GND		8B	-55^oC			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock To Carry Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	500	ns
			10, 11	+125^{o}C, -55^{o}C	-	675	ns
Propagation Delay Clock To Decode Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	700	ns
			10, 11	+125^{o}C, -55^{o}C	-	945	ns
Propagation Delay Reset To Carry Out	TPLH3	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	550	ns
			10, 11	+125^{o}C, -55^{o}C	-	743	ns
Propagation Delay Reset To Decode Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	600	ns
			10, 11	+125^{o}C, -55^{o}C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	-	200	ns
			10, 11	+125^{o}C, -55^{o}C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25^{o}C	2.5	-	MHz
			10, 11	+125^{o}C, -55^{o}C	1.85	-	MHz

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55^{o}C and +125^{o}C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55^{o}C, +25^{o}C	-	5	µA
				+125^{o}C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55^{o}C, +25^{o}C	-	10	µA
				+125^{o}C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55^{o}C, +25^{o}C	-	10	µA
				+125^{o}C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25^{o}C, +125^{o}C, -55^{o}C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125^{o}C	0.36	-	mA
				-55^{o}C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125^{o}C	0.9	-	mA
				-55^{o}C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125^{o}C	2.4	-	mA
				-55^{o}C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125^{o}C	-	-0.36	mA
				-55^{o}C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125^{o}C	-	-1.15	mA
				-55^{o}C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125^{o}C	-	-0.9	mA
				-55^{o}C	-	-2.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	$+125^oC$	-	-2.4	mA
				-55^oC	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	$+25^oC$, $+125^oC$, -55^oC	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	$+25^oC$, $+125^oC$, -55^oC	+7	-	V
Propagation Delay Clock To Carry Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	$+25^oC$	-	200	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	150	ns
Propagation Delay Clock To Decode Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	$+25^oC$	-	250	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	180	ns
Propagation Delay Reset To Carry Out	TPLH3	VDD = 10V	1, 2, 3	$+25^oC$	-	240	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	160	ns
Propagation Delay Reset To Decode Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	$+25^oC$	-	250	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	180	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	$+25^oC$	-	100	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	50	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	$+25^oC$	5.5	-	MHz
		VDD = 15V	1, 2, 3	$+25^oC$	8	-	MHz
Minimum Reset Pulse Width	TW	VDD = 5V	1, 2, 3	$+25^oC$	-	120	ns
		VDD = 10V	1, 2, 3	$+25^oC$	-	100	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	50	ns
Minimum Reset Removal Time	TREM	VDD = 5V	1, 2, 3	$+25^oC$	-	30	ns
		VDD = 10V	1, 2, 3	$+25^oC$	-	15	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	10	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1, 2, 3	$+25^oC$	-	220	ns
		VDD = 10V	1, 2, 3	$+25^oC$	-	100	ns
		VDD = 15V	1, 2, 3	$+25^oC$	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	$+25^oC$	-	7	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	$+25^oC$	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	$+25^oC$	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1, 4	$+25^oC$	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1, 4	$+25^oC$	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1, 4	$+25^oC$	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	$+25^oC$	-	1.35 x $+25^oC$ Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for $+25^oC$ limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS $+25^oC$

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9(	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER						
Static Burn-In 1 (Note 1)	4 - 7, 9 - 14	1 - 3, 8, 15	16			
Static Burn-In 2 (Note 1)	1, 2, 14, 15	3 - 6, 8, 10 - 13	7, 9, 16			
Dynamic Burn-In (Note 1)	-	2, 8, 15	3, 16	4 - 7, 9 - 13	1	
Irradiation (Note 2)	4 - 7, 9 - 14	8	1 - 3, 15, 16			
PART NUMBER CD4033BMS						

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	4 - 7, 9 - 13	1 - 3, 8, 14, 15	16			
Static Burn-In 2 Note 1	4 - 7, 9 - 13	8	1 - 3, 14 - 16			
Dynamic Burn-In Note 1	-	2, 3, 8, 14, 15	16	4 - 7, 9 - 13	1	
Irradiation Note 2	4 - 7, 9 - 13	8	1 - 3, 14 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Timing Diagram

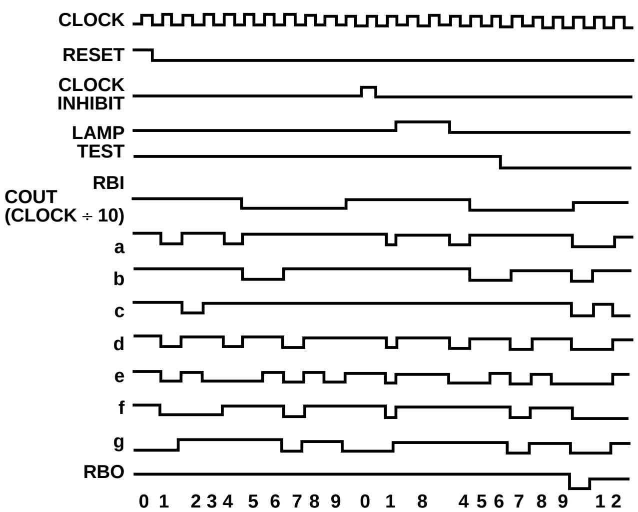


FIGURE 2. CD4033BMS TIMING DIAGRAM

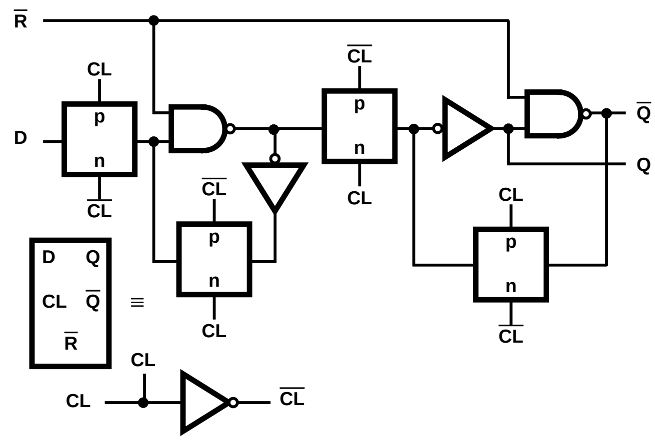


FIGURE 3. DETAIL OF TYPICAL FLIP-FLOP STAGE

Typical Performance Characteristics

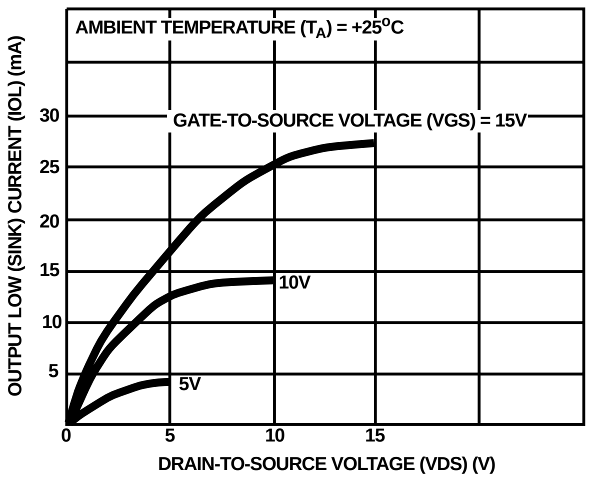


FIGURE 4. TYPICAL N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

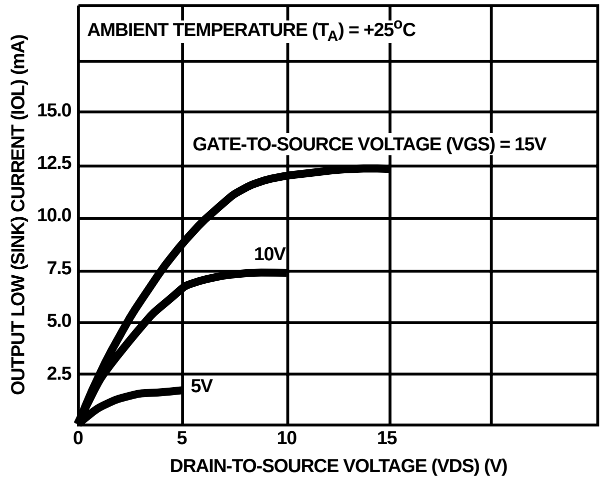


FIGURE 5. MINIMUM N-CHANNEL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

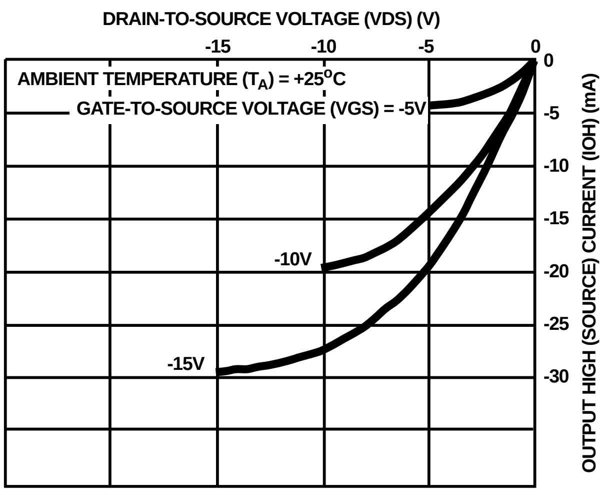


FIGURE 6. TYPICAL P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

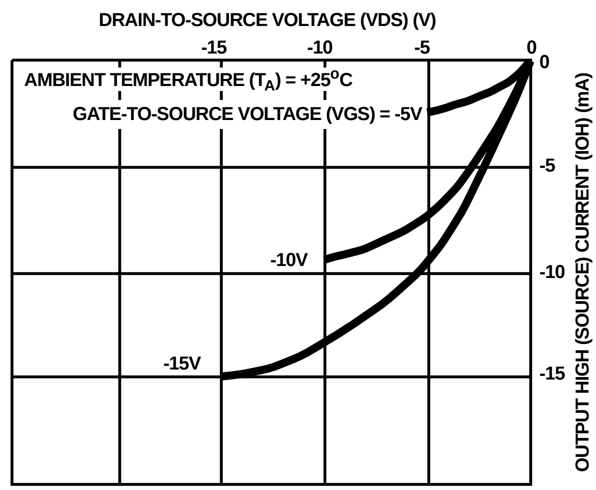


FIGURE 7. MINIMUM P-CHANNEL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

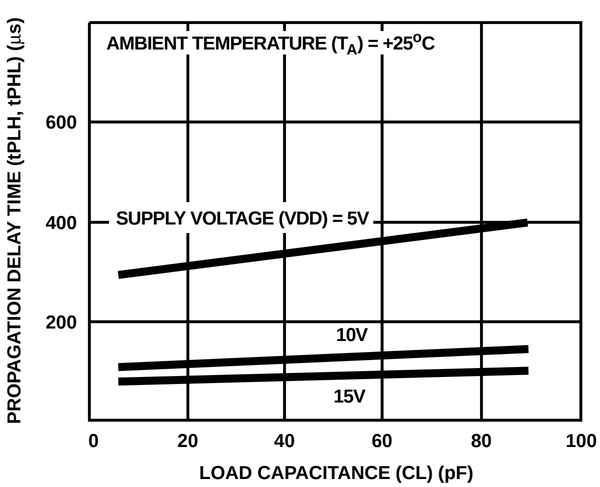


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE FOR DECODED OUTPUTS

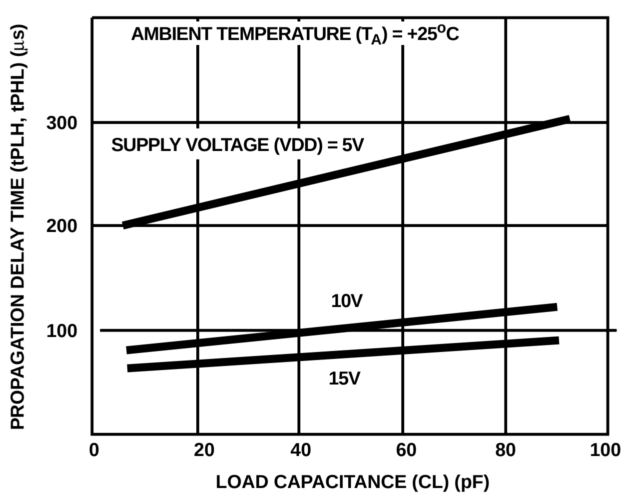


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE FOR CARRY-OUT OUTPUTS

Typical Performance Characteristics (Continued)

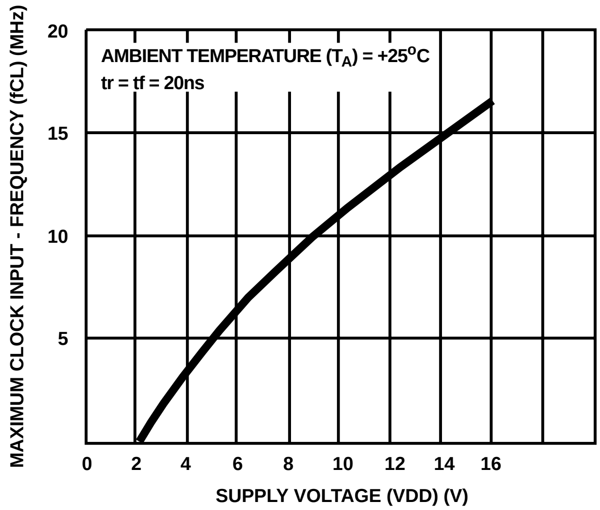


FIGURE 10. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

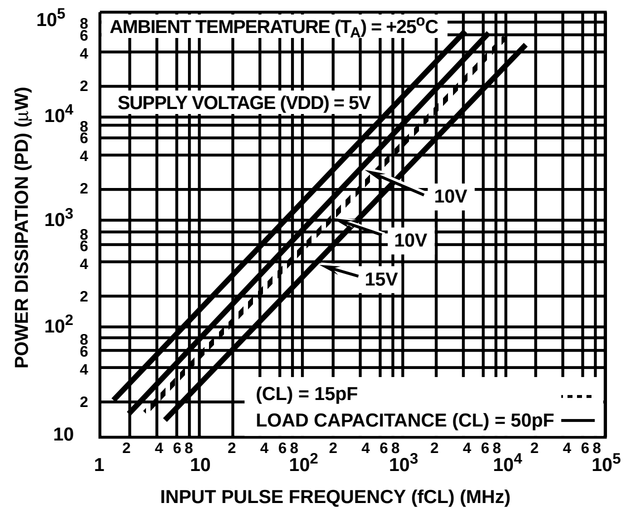


FIGURE 11. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK INPUT FREQUENCY

Light Emitting Diode Displays

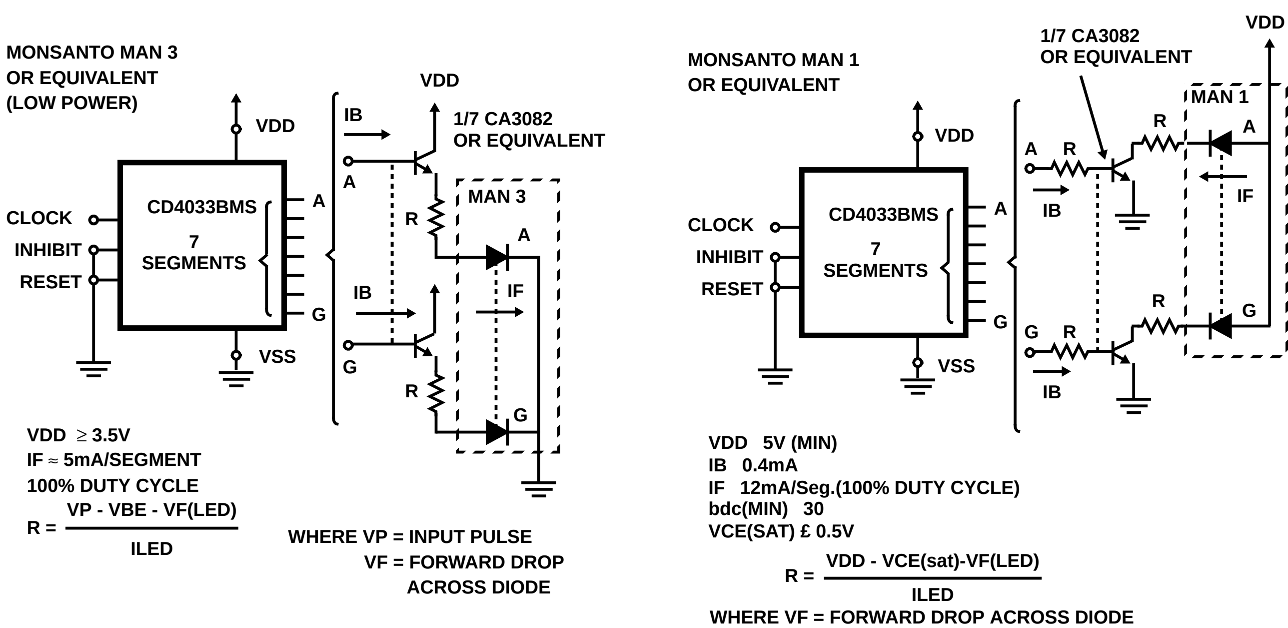
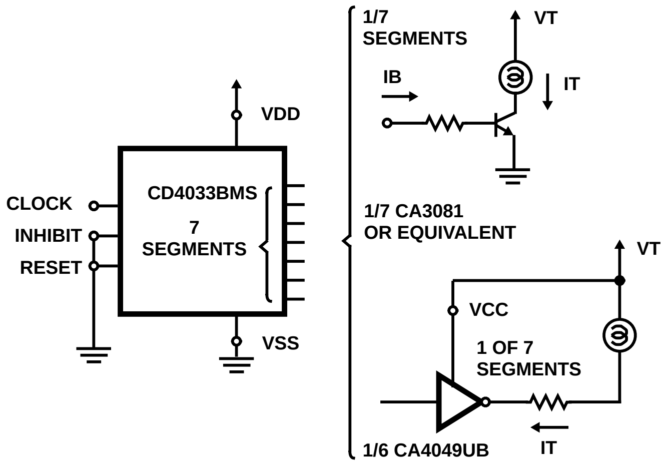


FIGURE 12. INTERFACING THE CD4033BMS WITH COMMERCIALLY AVAILABLE LIGHT EMITTING DIODE DISPLAYS

7-Segment Display Devices



INCANDESCENT READOUTS
Numitron DR2000 Series
TUBE REQUIREMENTS
VT = 3.5 - 5V
IT = 24mA Segment

ASSUMED TRANSISTOR CHARACTERISTICS	CD4049UB
βdc (min) ≥ 25	at VCC = 10V (min)
VCE (sat) ≤ 0.5V	Vo “0” ≤ 2V
VDD = 8V (min)	IT = 8mA (min)
IB = 1mA (min)	VT ≈ 3.5V to 6V
IT = 24mA (min)	

CD4049UB

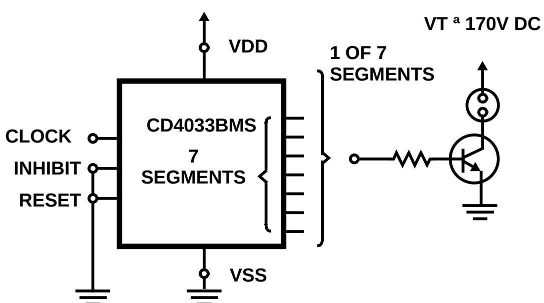
at VCC = 10V (min)
Vo “0” ≤ 0.6V
IT = 8mA (min)

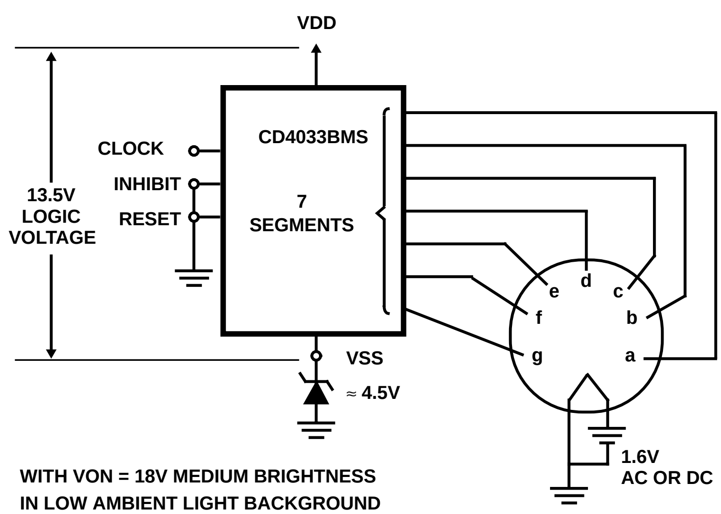
at VCC = 6V (min)
Vo “0” ≤ 1V
IT = 5mA (min)
VT ≈ 1.5V to 3.5V

LOW-POWER INCANDESCENT READOUTS
PINLITES INC-Series O and R

TUBE REQUIREMENTS	VT(V)	mA/Segment	**ASSUMED TRANSISTOR CHARACTERISTICS**
0-03-15	1.5	8	βdc (min) ≥ 30
0-04-30	3	8	VCE (sat) ≤ 0.5V
0-06-30	3	8	VCC ≥ 3.5V (min)
R-R3-20	2	4.3	IB ≥ 0.25mA (min)
R-R4-30	3	4.3	IT ≤ 7.5mA (min)

*The interfacing buffers shown, while a necessity with the CD4033A, are not required when using the “B” devices; the “B” outputs (≈ 10 times the “A” outputs) can drive most display devices directly especially at voltages above 10V.





WITH VON = 18V MEDIUM BRIGHTNESS IN LOW AMBIENT LIGHT BACKGROUND WILL RESULT. THE POINT OF NO NOTICEABLE GLOW IS VOFF ≈ 4.5V

NEON READOUT (NIXIE TUBE)**
1. Alco Electronics - MG19
2. Burroughs - B5971, B7971, B8971

TUBE REQUIREMENTS	VT(Vdc)	mA/Segment
Alco MG19	180	0.5
Burroughs B5971	170	3
Burroughs B7971, B8971	170	6

**(Trademark) Burroughs Corp.
TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff - 0.05mA

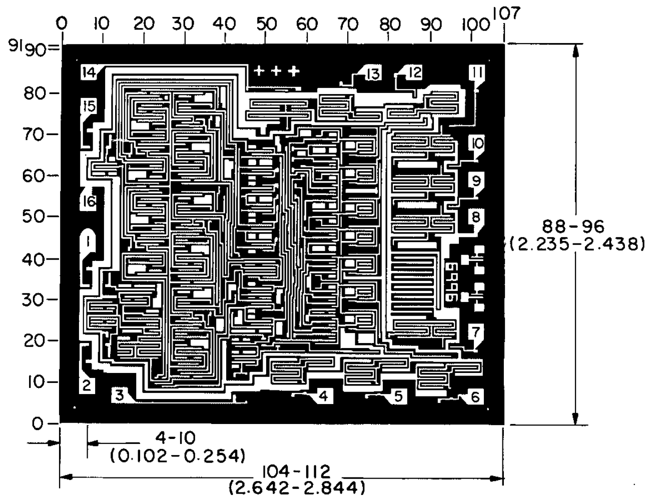
V(BR)CER >VT
βdc (min) ≥ 30

LOW VOLTAGE VACUUM FLORESCENT READOUTS
1. Tung-Sol DIGIVAC S/G ‡ Type DT1704A or DT1705C
2. Nippon Electric (NEC): Type DG12E or LD915
   TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12V to 25V depending on required brightness Filament requirement 45mA at 1.6V, ac or dc.

‡ (Trademark) Wagner Electric Co.

FIGURE 13. INTERFACING THE CD4033BMS WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES*

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches