DATA SHEET

SUNPLUS

SPMC701FM0A

16-bit Micro Controller with 32K x 16 Flash Memory

Preliminary

NOV. 10, 2003

Version 0.2

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16-BIT MICRO CONTROLLER WITH 32K X 16 FLASH MEMORY

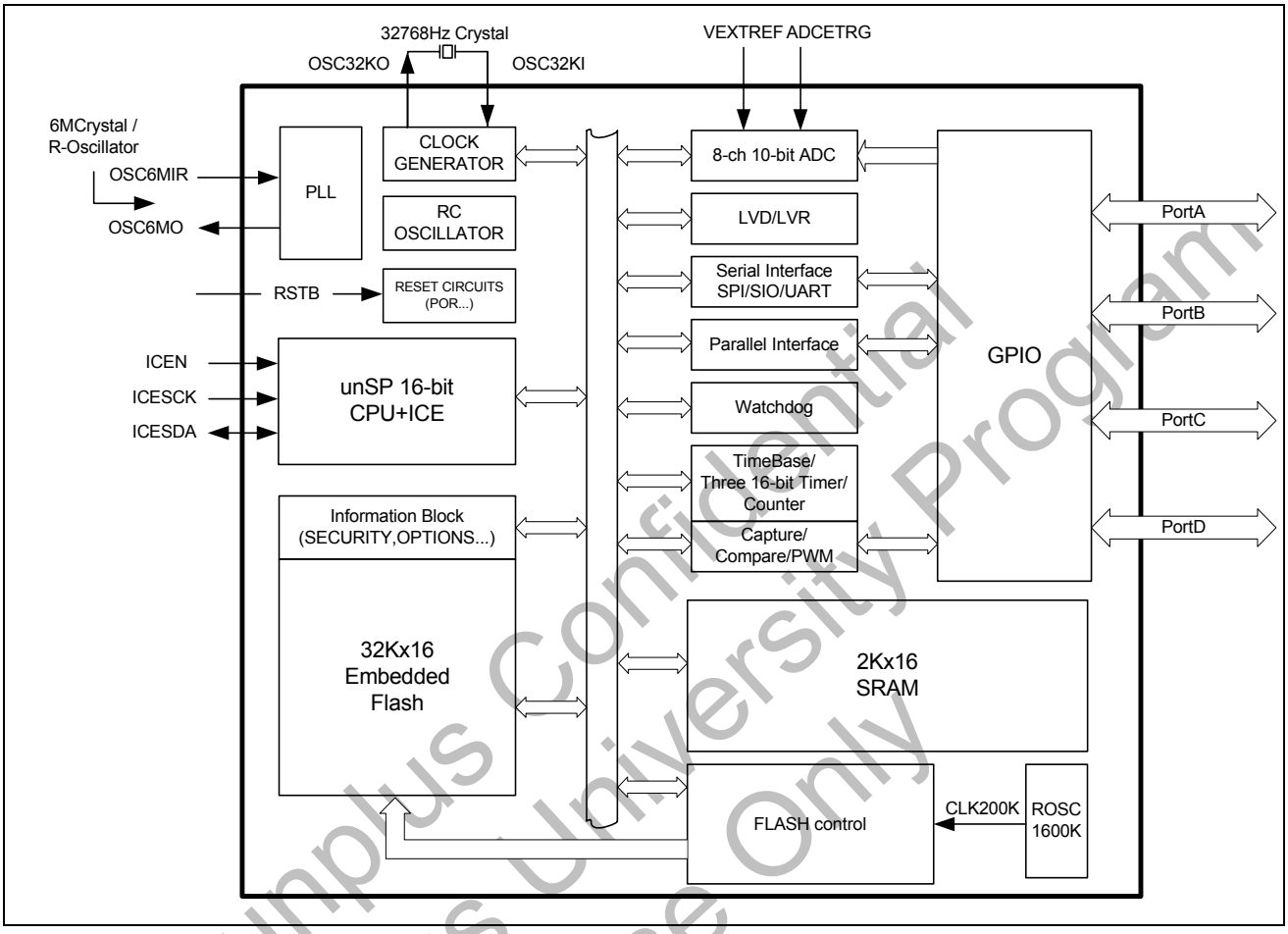
1. GENERIAL DESCRIPTION

The SPMC701FM0A, a 16-bit architecture product, carries the newest 16-bit microprocessor, *μ'nSP*™ (pronounced as *micro-n*-SP), developed by SUNPLUS Technology. The high processing speed assures the *μ'nSP*™ is capable of handling complex digital signal processes easily and rapidly. The SPMC701FM0A is applicable to areas of controlling peripherals through the serial and parallel interfaces. The operation voltage of 3.0V through 3.6V and speed of 6MHz through 48MHz yield the SPMC701FM0A to be easily used in varieties of applications. The memory capacity includes 32K-word flash memory plus a 2K-word working SRAM. Other features include dual clock, 64 programmable multi-functional I/Os, UART, SPI, Synchronous Serial IO, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight 10-bit ADC input and many others.

2. FEATURES

- 16 bit *μ'nSP*™ microprocessor
- Programmable CPU clock: 6MHz, 12MHz, 24MHz, 48MHz
- Operating voltage: 3.0V ~ 3.6V @ 48MHz ~ 6MHz
- Operating voltage for Flash programming: 3.0V ~ 3.6V
- IO PA, PB, PC, PD operating voltage: 3.0V ~ 5.0V
- Operating temperature 0°C to +70°C
- ICE interface built-in
- 32K-word Flash ROM embedded
  - Programmable by CPU in free run mode
  - Endurance: > 20,000 write cycles
  - Retention: 100 years under room temperature
- Programmable code-option (security, low-voltage detect, low-voltage reset, watchdog timer, clock selection)
- 2K-word working RAM built-in
- Power-on-reset and Power-up-timer (PWRT)
- Low voltage reset/detect (LVR/LVD), programmable LVD level 2.6V, 2.8V, 3.0V and 3.2V.
- Watchdog timer
- Power saving mode
- PLL, RC or crystal optional
- Interrupt controller
- Three 16-bit Timer/Counters
- 10-bit, 8-channel, Analog-to-Digital converter
- Capture/Compare/PWM functions
- Universal Asynchronous Receiver/Transmitter (UART)
- Serial interface including Standard Peripheral Interface (SPI) and Synchronous Serial IO (SIO)
- Parallel communication port
- 64 GPIOs, 5.0V tolerant I/O
- 100 pins LQFP package

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
RSTB	18	I (PH)	External reset
OSC6MIR	23	I	External 6MHz crystal input or R-oscillator resistor input according to the code option for crystal or R-oscillator, which is stored in embedded flash information block.
OSC6MO	24	O	External 6MHz crystal output
ECLKEN	27	I (PL)	External clock enable,
ICEN	28	I (PL)	ICE enable 1 = ICE enable 0 = Normal mode (ICE disable)
ICECLK	67	I	ICE serial clock input
ICESDA	68	I/O	ICE serial address/data input/output
OSC32KI	20	I	32768Hz crystal input
OSC32KO	21	O	32768Hz crystal output
VDDA	17	I	3V/5V power for PA[15:0]
PA15/SCL/$\overline{SS}$	16	I/O	PA[15], SIO serial clock or the $\overline{SS}$ input of SPI
PA14/SDA	15	I/O	PA[14] or SIO serial address/data
PA13/TXD	14	I/O	PA[13] or UART transmission data output
PA12/RXD	13	I/O	PA[12] or UART receive data input
PA11/PRDB	12	I/O	PA[11] or Parallel Communication Interface PRDB
PA10/PWEB /OUTRST	11	I/O	PA[10] or Parallel Communication Interface PWEB Or system reset output
PA9/PCIA0	10	I/O	PA[9] or Parallel Communication Interface PCIA0
PA8/PCSB	9	I/O	PA[8] or Parallel Communication Interface PCSB
PA7/PCID7	8	I/O	PA[7] or Parallel Communication Interface data bit 7
PA6/PCID6	7	I/O	PA[6] or Parallel Communication Interface data bit 6
PA5/PCID5	6	I/O	PA[5] or Parallel Communication Interface data bit 5
PA4/PCID4	5	I/O	PA[4] or Parallel Communication Interface data bit 4
PA3/PCID3	4	I/O	PA[3] or Parallel Communication Interface data bit 3
PA2/PCID2	3	I/O	PA[2] or Parallel Communication Interface data bit 2
PA1/PCID1	2	I/O	PA[1] or Parallel Communication Interface data bit 1
PA0/PCID0	1	I/O	PA[0] or Parallel Communication Interface data bit 0
VDDB	64	I	3V/5V power for PB[15:8]
PB15/SCK	79	I/O	PB[15] or SPI serial clock
PB14/SDI	78	I/O	PB[14] or SPI serial data input
PB13/SDO	75	I/O	PB[13] or SPI data output
PB12/CCP1	74	I/O	PB[12] or Timer1 Capture/Compare/PWM input/output
PB11/CCP0	73	I/O	PB[11] or Timer0 Capture/Compare/PWM input/output
PB10/EXT2	72	I/O	PB[10] or External input 2
PB9/EXT1	71	I/O	PB[9] or External input 1
PB8/ADTRIG	70	I/O	PB[8] or ADC external trigger
PB7/AD7	63	I/O	PB[7] or ADC channel 7 analog input
PB6/AD6	62	I/O	PB[6] or ADC channel 6 analog input
PB5/AD5	61	I/O	PB[5] or ADC channel 5 analog input
PB4/AD4	60	I/O	PB[4] or ADC channel 4 analog input
PB3/AD3	59	I/O	PB[3] or ADC channel 3 analog input

Mnemonic	PIN No.	Type	Description
PB2/AD2	58	I/O	PB[2] or ADC channel 2 analog input
PB1/AD1	57	I/O	PB[1] or ADC channel 1 analog input
PB0/AD0	56	I/O	PB[0] or ADC channel 0 analog input
VDDC	88	I	3V/5V power for PC[15:0]
PC15	96	I/O	PC[15]
PC14	95	I/O	PC[14]
PC13	94	I/O	PC[13]
PC12	93	I/O	PC[12]
PC11	92	I/O	PC[11]
PC10	91	I/O	PC[10]
PC9	90	I/O	PC[9]
PC8	89	I/O	PC[8]
PC7	87	I/O	PC[7]
PC6	86	I/O	PC[6]
PC5	85	I/O	PC[5]
PC4	84	I/O	PC[4]
PC3	83	I/O	PC[3]
PC2	82	I/O	PC[2]
PC1	81	I/O	PC[1]
PC0	80	I/O	PC[0]
VDDD	38	I	3V/5V power for PD[15:0]
PD15	30	I/O	PD[15]
PD14	31	I/O	PD[14]
PD13	32	I/O	PD[13]
PD12	33	I/O	PD[12]
PD11	34	I/O	PD[11]
PD10	35	I/O	PD[10]
PD9	36	I/O	PD[9]
PD8	37	I/O	PD[8]
PD7	39	I/O	PD[7]
PD6	40	I/O	PD[6]
PD5	41	I/O	PD[5]
PD4	42	I/O	PD[4]
PD3	43	I/O	PD[3]
PD2	44	I/O	PD[2]
PD1	45	I/O	PD[1]
PD0	46	I/O	PD[0]
TEST	69	I (PL)	Test mode control 0 = Normal mode 1 = Test mode
VPP	100	I	High voltage pin used in flash test mode and operating in 0 ~ 15V.
AVDD	52	I	Analog power
AVSS	54	I	Analog ground
VDD1	19	I	Digital power 1

Mnemonic	PIN No.	Type	Description
VSS1	22	I	Digital ground 1
VDD2	66	I	Digital power 2
VSS2	55	I	Digital ground 2
VEXTREF	51	I	ADC top voltage reference
VCMP	53	I	Common mode voltage of ADC, basically define as AVDD/2
VREF2V	48	O	2.0V reference output voltage, which can be connected to VEXTREF as a reference voltage

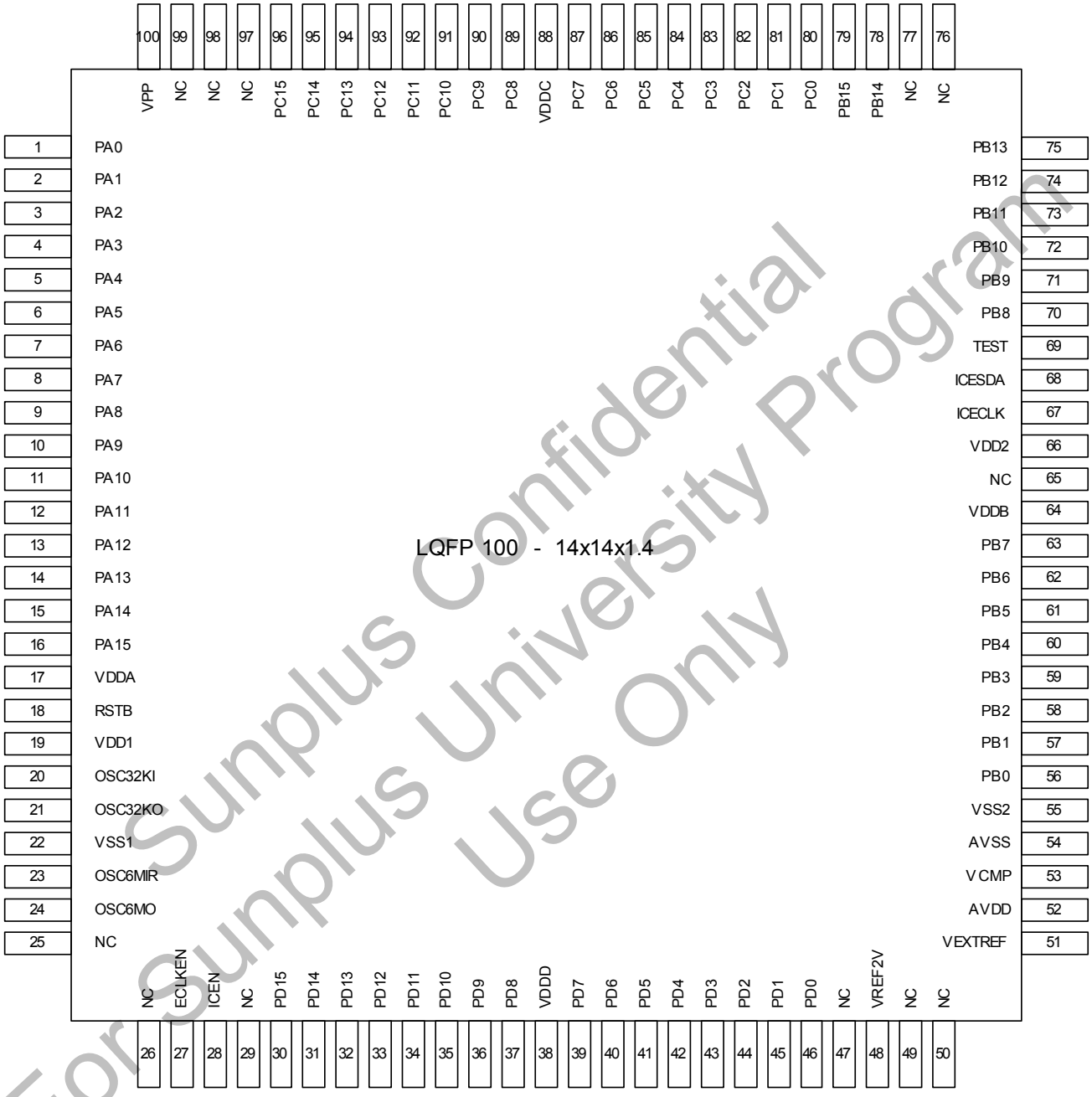
PH: pull high, PL: pull low

4.1. Ordering Information

Product Number	Package Type
SPMC701FM0A - C	Chip form
SPMC701FM0A - PL08	Package form - LQFP 100

Note: If needs code programming service please contact with Sunplus sales representatives for more information.

4.2. PIN Map



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

The SPMC701FM0A is equipped with a 16-bit *μ'nSP™*, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. 13 registers are involved in *μ'nSP™:* 5 General registers (R1 – R5), 4 secondary registers (SR1-SR4), 3 system registers (SP, SR, PC), 1 inner register (FR). The interrupts include 1 FIQ (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. Moreover, a high performance hardware multiplier is also built in to reduce the software multiplication loading.

5.2. Memory

5.2.1. SRAM

The amount of SRAM is 2K-word (including Stack), ranged from $0000 through $07FF with access speed of two CPU clock cycles.

5.2.2. Flash memory

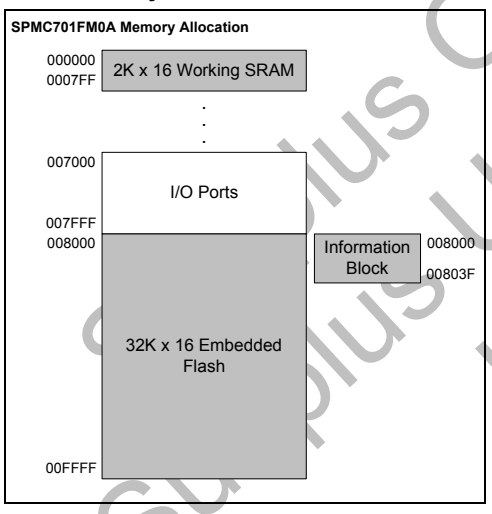


Figure 5-1

The 32K words embedded flash is partitioned into 16 regions of 2K words. Except the 00F800 - 00FFFF bank is read-only in free run mode. The rest 15 2K-word banks can be programmed to be read-only or read-write for CPU in free run mode independently. All 32K words can be programmed or erased in ICE mode.

5.2.3. Information block and security

There are 64 words in the information block of the embedded flash. They can be used to store the important information defined by users. The system option bits are stored in the embedded flash information block first word (address = 0x8000).

When power is turned on or external reset occurs, system reset is activated until the power-on-timer counts 16384 times of 200kHz clock cycle then reset signal is deactivated.

Table 5-1

B15 - B5	B4	B3	B2	B1	B0
Verification Pattern 01010101010	Security 1: Disable 0: Enable	LVD 1: Disable 0: Enable	LVR 1: Enable 0: Disable	Watch dog 1: Enable 0: Disable	Clock Selection 1: crystal 0: R-oscillator

In case of security option in information block is enabled, SPMC701FM0A is protected from reading data through ICE. In addition, SRAM cannot be accessed (read/write) in ICE enable mode. The "mass erase" command that users can perform exclusively is to completely erase flash data and clear security bit. The above limitations don't exist in free run mode. In normal operation (ICEN = 0), CPU can access the flash data and the working SRAM. The ICE cannot program the flash memory when the ice mode is activated and Security is turn on.

5.2.4. PLL and clock sources

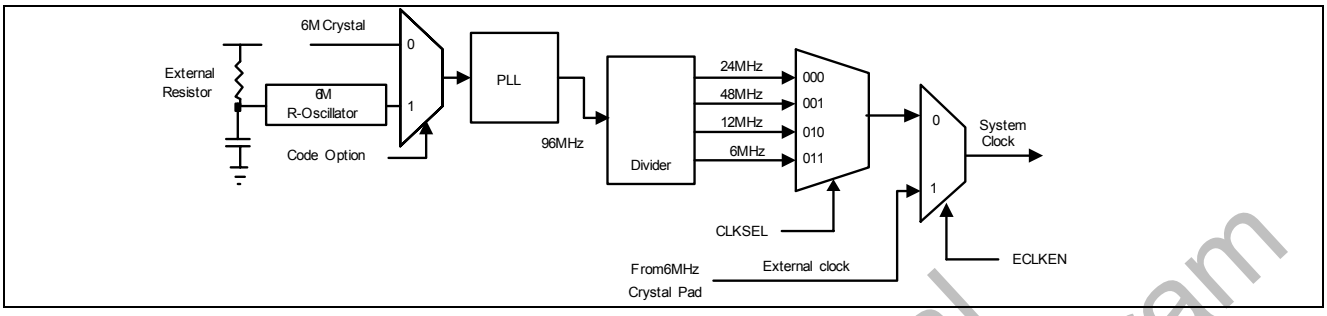


Figure 5-2

5.2.5. Phase-lock loop (PLL)

Either the 6MHz crystal or R-oscillator can be as PLL reference clock source optionally to produce the system clock. The code option is stored in the information block of embedded flash. In the reset stage, the option word is read and loaded into option registers.

5.2.6. Clock sources

The circuits needed to provide clock sources are listed as follows:

- 1600KHz R-oscillator (produce 200KHz clock by divider)
- Phase-Lock Loop (Pumps the 6MHz crystal or 6MHz R-oscillator to 96MHz)
- 6MHz crystal pads
- 32768Hz crystal pads

The default system clock is 24MHz and can be programmed as 48MHz, 24MHz, 12MHz, and 6MHz. The 1600KHz R-oscillator provides a 200 KHz clock for flash controller to generate the required control signals for meeting the timing specifications of flash erasing and programming. It can be disabled in Standby mode for power saving. Besides, 200 KHz clock is also used for Power-up-timer (PWRT) and Wakeup-timer. For real-time counter (RTC), another 32768Hz crystal is needed to provide precise clock source. A 2Hz-RTC (1/2 second) is provided.

5.3. Power Saving Modes and Wakeup

There are two modes for power saving:

1.) Halt mode: Only CPU off

2.) Standby mode: all clock sources are off

Table 5-2

Clock Source and Modules	Halt	Standby
32768Hz crystal	ON	OFF
PLL	ON	OFF
6M R-oscillator or crystal	ON	OFF
CPU	OFF	OFF
LVD/LVR	Reserved	OFF
ADC	Reserved	OFF
Working SRAM	ON	OFF
Flash	ON	OFF
1.6MHz R-oscillator	ON	OFF

If there is no wake-up source enabled, the power saving command is not acceptable by hardware protection circuit. According to two power saving mode, one of wake-up sources is necessary at lease to be activated is as follows:

Table 5-3

Wake-up source	HALT mode	STDBY mode
Keychange of PA	√	√
Keychange of PB	√	√
Keychange of PC	√	√
Keychange of PD	√	√
UART interrupt	√	-
SPI interrupt	√	-
SIO interrupt	√	-
PCI interrupt	√	-
TMR2 interrupt	√	-
TMR1 interrupt	√	-
TMR0 interrupt	√	-
TMB2 interrupt	√	-
TMB1 interrupt	√	-
4HZ interrupt	√	-
2HZ interrupt	√	-

5.4. Interrupt

The SPMC701FM0A has 16 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ0~IRQ7 (Interrupt request). Besides, the SPMC701FM0A also implements a software interrupt, BREAK. The priority of BREAK, FIQ, IRQ is as follows: BREAK > FIQ > IRQ 0 > IRQ 1 > IRQ 2 > IRQ 3 > IRQ 4 > IRQ 6 > IRQ 7.

Table 5-4

Interrupt Source	Interrupt Name	IRQ NO.	Set as FIQ
ADC	ADCINT	IRQ0	Yes
EXT2	EXT2INT	IRQ1	Yes
EXT1	EXT1INT	IRQ1	Yes
UART	UARTINT	IRQ3	Yes
SPI	SPIINT	IRQ3	Yes
SIO	SIOINT	IRQ3	Yes
PCI	PCIINT	IRQ2	Yes
Timer2	TMR2INT	IRQ4	Yes
Timer1	TMR1INT	IRQ4	Yes
Timer0	TMR0INT	IRQ4	Yes
LVD	LVDINT	IRQ5	Yes
Keychange	KEYCINT	IRQ5	Yes
Timebase2	TMB2INT	IRQ6	No
TimeBase1	TMB1INT	IRQ6	No
4HZ	4HZINT	IRQ7	No
2HZ	2HZINT	IRQ7	No

5.5. Low Voltage Detection and Low Voltage Reset

5.5.1. Low voltage detection (LVD)

The low voltage detection reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0V and 3.2V. When the operating voltage drops below LVD level, the interrupt will be issued. In such situation, the programs can be designed to react to this condition. This module can output stable 2 volts voltage, which can be as ADC top voltage reference input.

5.5.2. Low voltage reset (LVR)

With the low voltage reset function, a reset signal is generated to reset system when the operation voltage drops below 2.6V for over 3 consecutive 3MHz clock cycles. In case of voltage rising back to above 2.6, the reset duration will be added with an 80us extension time. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below 2.6V. The LVR will reset all functions to the initial states.

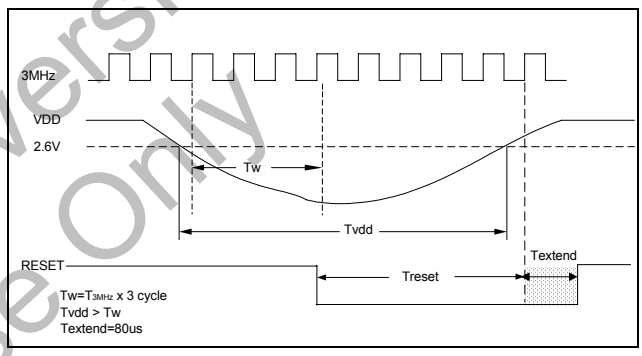


Figure 5-3

5.6. General purpose input/output (GPIO) ports

The purpose of GPIOs is to communicate with other devices. Four I/O ports are available in SPMC701FM0A, PA, PB, PC, and PD. PC, PD are ordinary I/O and PA, PB contains some special functions in certain pins. PA, PB, PC, and PD are software programmable for wake up capability. The GPIOs are capable of 5V tolerance.

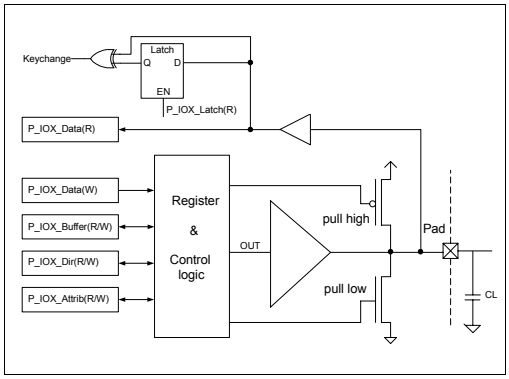


Figure 5-4

Although data can be written into the same register through either of the P_IOX_Data(W, X=A,B,C,D) and P_IOX_Buffer(W), they can be read from different places, P_IOX_Data(R) and P_IOX_Buffer(R). The GPIOs have keychange wakeup function. To activate key wakeup function, latch data on P_IOX_Latch(R) and enable the key wakeup control option. Wakeup is triggered when the GPIOs state is different from the state at the time latched. In addition to an ordinary I/O port, PA and PB carry some special functions. A summary of PA and PB special functions is listed as follows:

Table 5-5

Port Name	SFR Pin	Type	PHB	PL	Description
PA15	SCL ($\overline{SS}$)	I/O (I)	1	0	SIO serial clock input/output (SPI $\overline{SS}$ input)
PA14	SDA	I/O	1	0	SIO serial data Input/output
PA13	TXD	O	1	0	UART transmission data output
PA12	RXD	I	1	0	UART receive data input
PA11	PRDB	I/O	1	0	PCI RDB input/output
PA10	PWEB (OUTRST)	I/O (O)	1	0	PCI WEB input/output (System reset output)
PA9	PCIA0	I/O	1	0	PCI A0 input/output
PA8	PCSB	I/O	1	0	PCI CSB input/
PA7	PCID7	I/O	1	0	PCI data bit 7
PA6	PCID6	I/O	1	0	PCI data bit 6
PA5	PCID5	I/O	1	0	PCI data bit 5
PA4	PCID4	I/O	1	0	PCI data bit 4
PA3	PCID3	I/O	1	0	PCI data bit 3
PA2	PCID2	I/O	1	0	PCI data bit 2
PA1	PCID1	I/O	1	0	PCI data bit 1
PA0	PCID0	I/O	1	0	PCI data bit 0
PB15	SCK	I/O	1	0	SPI clock input/
PB14	SDI	I	1	0	SPI data input
PB13	SDO	O	1	0	SPI data output
PB12	CCP1	I/O	1	0	Input for timer1 in Capture mode Output for timer1 in Compare mode Output for timer1 in PWM mode
PB11	CCP0	I/O	1	0	Input for timer0 in Capture mode Output for timer0 in Compare mode Output for timer0 in PWM mode
PB10	EXT2	I	User	User	External clock input
PB9	EXT1	I	User	User	External clock input
PB8	ADCETRG	I	User	User	Analog-to-digital converter external trigger to start a sample conversion
PB7	ADCCH7	I	User	User	Analog input of ADC channel 7
PB6	ADCCH6	I	User	User	Analog input of ADC channel 6
PB5	ADCCH5	I	User	User	Analog input of ADC channel 5
PB4	ADCCH4	I	User	User	Analog input of ADC channel 4
PB3	ADCCH3	I	User	User	Analog input of ADC channel 3
PB2	ADCCH2	I	User	User	Analog input of ADC channel 2
PB1	ADCCH1	I	User	User	Analog input of ADC channel 1
PB0	ADCCH0	I	User	User	Analog input of ADC channel 0

PHB: Pull high (low active) PL: Pull low OEB: Output enable (low active) User: According to user configuration

5.7. Timer/Counters with Capture/Compare/PWM Functions

SPMC701FM0A provides three 16-bit timer/counters (Timer0, Timer1, and Timer2). Timer0 and Timer1 cooperate with another two 16-bit registers (P_Timerx_CCPR and P_Timerx_CCPR2, x=0,1) and support Capture/Compare/PWM functions. The 16-bit timer/counter itself is an up counter (Timerx, x=0,1,2). The initial value of the up counter is stored in the pre-load register (P_Timerx_Preload, x=0,1,2). When the counter is enabled or overflow occurs, the initial value is loaded into counter on the next increment clock edge (synchronous load). So, if the initial value is FFFC, the counter will count by the sequence FFFC, FFFD, FFFE, FFFF, FFFC, FFFD, FFFE, FFFF, FFFC, FFFD, …, and so on. The Timerx interrupt flag is set when Timerx overflows.

The clock sources of Timerx can be generated by the internal clock sources (timer mode) or from external pin (counter mode).

1.) In timer mode, the clock source of Timerx is programmable by selecting the internal clock sources.
2.) In counter mode, the clock source of Timerx is generated by external clock source pin (EXTx, x=1,2). Additionally, EXTx can be divided by 1, 4, 16 pre-scaler divider and capable of selecting clock edge.

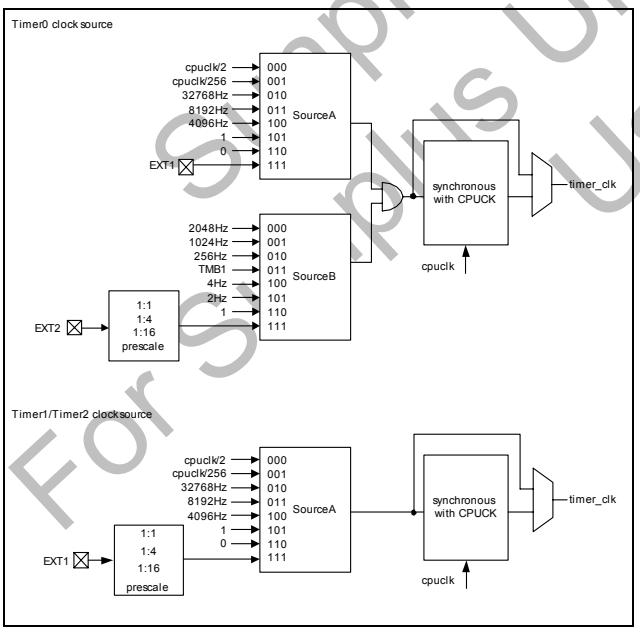


Figure 5-5

The clock source of Timer0 comes from the combination of clock source A and clock source B. In Timer1 and Timer2, the clock source is given from source A. The clock source A is a high frequency source and clock source B is a low frequency source. The combination of clock source A and B provides a variety of speeds to Timer0. A “1” represents pass signal and not gating. In contrast, “0” indicates deactivating timer. In addition, The Timer0 and Timer1 can support Capture, Compare and PWM functions. In capture mode, the value of Timerx (x=0,1) is latched and stored in Capture/Compare/PWM registers (P_Timerx_CCPR, x=0,1) at the selected edge of pin CCPx (x=0,1). The corresponding GPIO pin for CCPx is configured as input pin automatically when Timerx is set as capture mode. The value of Timerx can be latched to P_Timerx_CCPR for every 1, 4 or 16 rising or falling edges of CCPx. Timerx have an auxiliary register P_Timerx_CCPR2 (x=0,1) for capture mode. In case of every rising/ falling edge capture mode selected for P_Timerx_CCPR, the value of Timerx can be latched to P_Timerx_CCPR2 at every falling/rising edge. That is, P_Timerx_CCPR2 is loaded in opposite edge to P_Timerx_CCPR selected edge. When a value is captured into P_Timerx_CCPR, the interrupt flag is set. In this way, the pulse width of CCPx can be measured in capture mode. For example, the high pulse width can be measured by setting falling edge capture mode. The value of Timerx can be latched to P_Timerx_CCPR at every falling edge of CCPx and the value of Timerx can be latched to P_Timerx_CCPR2 at every rising edge. Therefore, the high pulse width can be acquired by subtracting the value of P_Timerx_CCPR to the value of P_Timerx_CCPR2.

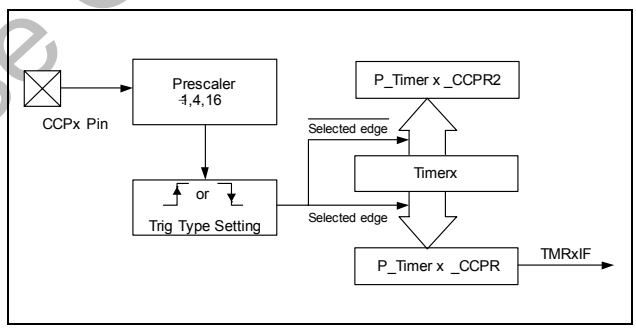


Figure 5-6

In compare mode, the value to be compared with Timerx is stored in P_Timerx_CCPR. When a match occurs, the Timerx will reload the value in P_Timerx_Preload (x=0,1). The corresponding CCPx pin is configured as an output pin automatically when compare mode is set. When a match occurs, the CCPx pin can be as set output or clear output according to configuration. In compare mode, the overflow of Timerx will not reload P_Timerx_Preload value to Timerx, and interrupt flag is set when a match occurs.

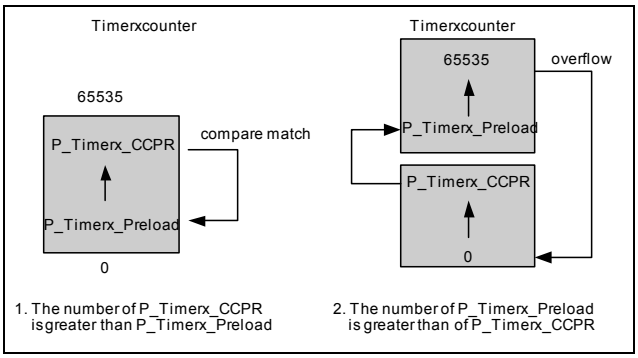


Figure 5-7

When Timerx is set as PWM mode, the CCPx pin is configured as output pin. When the Timerx is enabled, it acquires the initial value from P_Timerx_Preload. , The PWM output will go high/low at the rising edge of selected clock initially and then goes low/high when the value of Timerx matches with P_Timerx_CCPR, which depend on the control option. When overflow occurs, Timerx will reload the value of P_Timerx_Preload. Figure 5-8 is shown for the PWM output of Timer0 as an example.

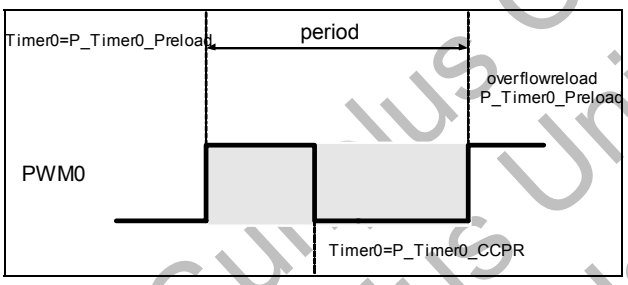


Figure 5-8

In addition, the PWM mode can generate return to one (RTO) or return to zero (RTZ) output. In this case, the counter acquires the initial value from P_Timerx_Preload in one another Timerx. The two transition edge of PWM output depends on it's own P_Timerx_Preload and P_Timerx_CCPR. For example (Figure 5-9), Timer1 acquires the initial value from P_Timer0_Preload. The transition edge of PWM1 output depends on it's own P_Timer1_Preload and P_Timer1_CCPR. When overflow occurs, Timer1 will reload the value of P_Timer0_Preload. At the same time, the interrupt flag is set.

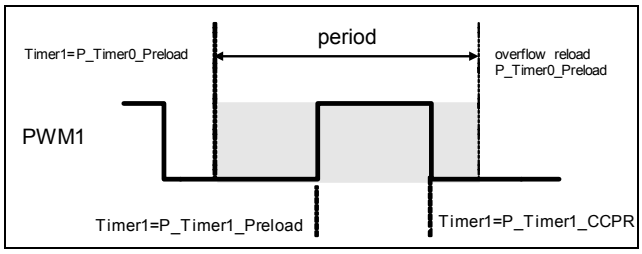


Figure 5-9

5.8. Timebase

Timebase, generated by 32768Hz, is a combination of frequency selections. The outputs of timebase block are named to TMB1 and TMB2. The TMB1 and TMB2 are the sources for Interrupt (IRQ6). Furthermore, the timebase block generates additional 2Hz and 4Hz clock as interrupt sources (IRQ7) for Real-Time-Clock (RTC).

Table 5-6

TMB2	TMB1
128Hz	8Hz
256Hz	16Hz
512Hz	32Hz
1024Hz	64Hz
Default: 128Hz	Default: 8Hz

5.9. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If watchdog is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. The watchdog function can be disabled by the option in information block. The clear period can be configured. If watchdog is cleared within period, the system will not be reset. The watchdog function is disabled during power saving mode.

5.10. Analog to Digital Converter (ADC)

SPMC701FM0A is embedded with a 10-bit 8-channel ADC. It is used for many applications like touch panel, battery power detection, etc. For speech record, an external AGC is needed. The channel inputs of ADC are shared with PB bit7-bit0. When an ADC channel is enabled, the digital function (pull high, pull down, output enable, etc.) of the corresponding pin is necessarily disabled to avoid disturbing ADC analog input signal.

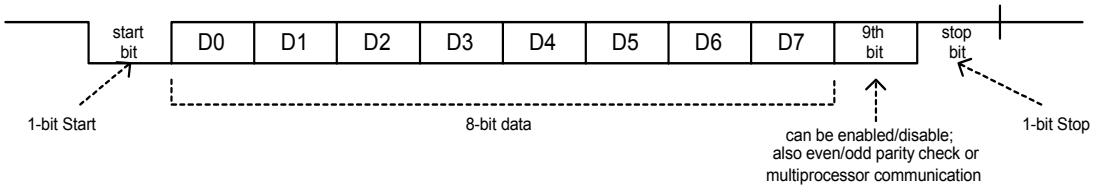


Figure 5-10

5.11. Universal Asynchronous Receiver/Transmitter (UART)

UART block provides a full-duplex standard interface that is able to communicate with other devices. With this interface, SPMC701FM0A can transmit and receive simultaneously. The baud-rate can be programmed from 1200 bps up to 115200bps. The Tx and Rx of UART are shared with PA13 and PA12, respectively. The UART transmits data on the *txd* pin in the following order: start bit, 8 data bits (LSB first), 9th bit (11-bit mode only), stop bit.

Reception begins at the falling edge of a start bit received on *rxd* pin when UART function is enabled. For this purpose, *rxd* is sampled 16 times per bit for any baud rate. For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. If the falling edge on *rxd* is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on *rxd*. Moreover, UART is capable of the parity check and multiprocessor communication feature in 11-bit mode. A typical usage of the multiprocessor communication feature is the situation when a master wants to send a block of data to one of several slaves.

5.12. Standard Peripheral Interface (SPI)

SPI supports full-duplex synchronous transfer between a Master device and a Slave device. As in master mode, the shift clock (SCK) is generated by the SPI. There are two register bits (SPIPHA and SPIPOL) to control the clock phase and polarity. The transmission starts from an I/O write to the P_SPI_TxBuf register (write port). If the user just wants to receive the data from the slave device, the firmware still needs to do a dummy write to the P_SPI_TxBuf to initiate the transfer.

After the firmware writes one byte to P_SPI_TxBuf, there are two situation as follows: If the shift register is not shifting data currently, the data will be loaded from P_SPI_TxBuf to the shift register at the first SCK phase and start transmitting. If the shift register is busy shifting data, SPITBF flag in P_SPI_Statue register will be set. The new data will be loaded from P_SPI_TxBuf to shift register when the transmission has finished. When the transmission session is in progress, the data from the slave device is also shifted in through the SDI pin. The data from SDI pin can be sampled according to SPISMPS bit. The received data is then latched to the P_SPI_RxBuf(read port) for the firmware reading. When each 8-bit transfer has completed, the SPIIF flag bit of the P_SPI_Status register will be set and an interrupt will be generated if the SPIIEN bit is set.

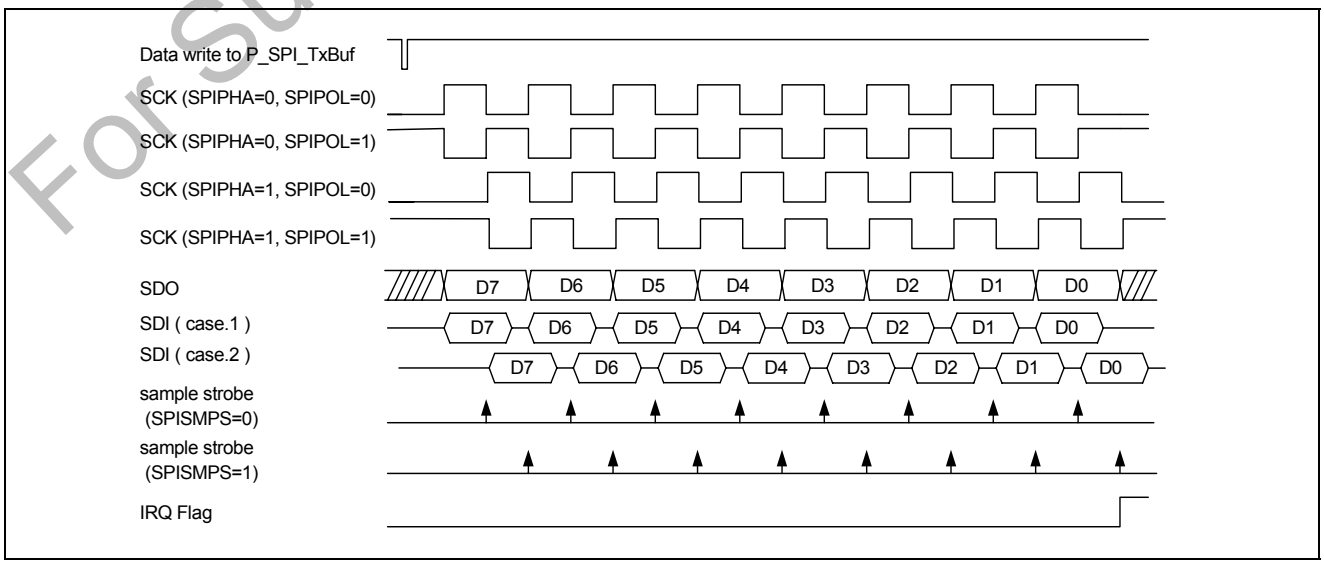


Figure 5-11 SPI Master Mode Timing

If SPICSEN of P_SPI_Ctrl is clear, the SPI module working in slave mode depends on SPIMS of P_SPI_Ctrl. In case of SPIMS is set, the SPI module is in slave mode. The shift clock (SCK) comes from external SPI master, so the transmission starts from the first SCK event. To transmit, the firmware should write the data to the P_SPI_TxBuf register before the first SCK from the master. Both of the master and of slave device must be programmed to same SCK polarity to send and receive the data at the same time. If the clock phase bit "SPIPHA" is set to 1, the 1st data bit being shifted out starts right after the I/O write to P_SPI_TxBuf register.

If the clock phase bit SPIPHA is set to 0, the 1st data bit being shifted out starts after first SCK edge. In case of SPICSEN of P_SPI_Ctrl is set, the SPI mode working in slave mode depends on SPIMS of P_SPI_Ctrl and low active input $\overline{SS}$. If SPIMS of P_SPI_Ctrl is set and $\overline{SS}$=0, the SPI module works in slave mode. In this way, SPI is capable of multi-slave communication by using the slave selection pin $\overline{SS}$. The GPIO pin PA15 is shared with $\overline{SS}$ of SPI module and SCL of SIO module. In multi-slave communication mode, SPI slave mode and SIO cannot be enable at the same time.

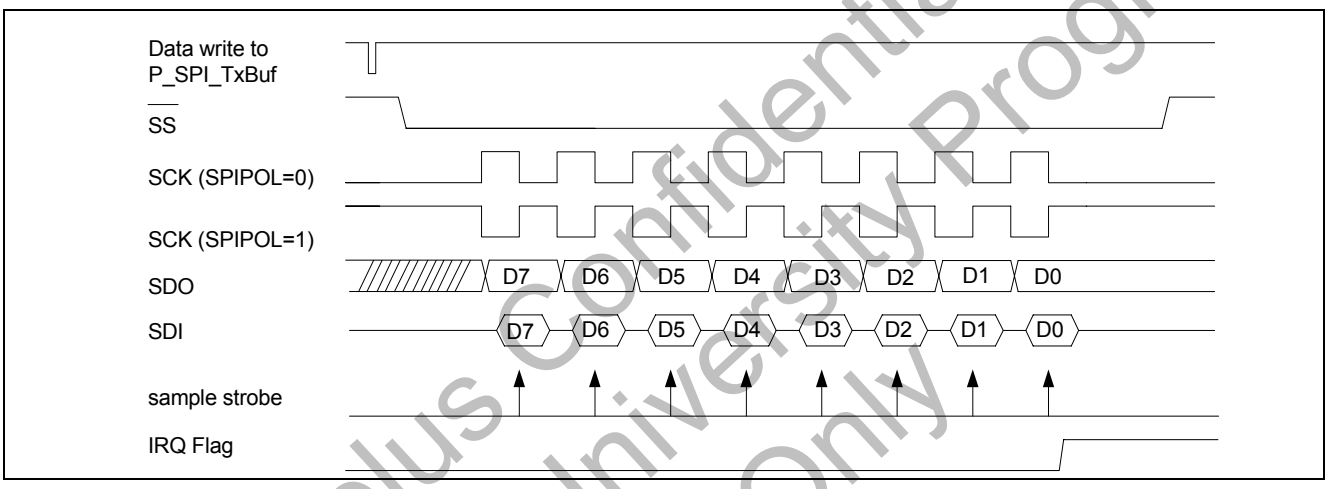


Figure 5-12 SPI Slave Mode Timing (SPIPHA=0)

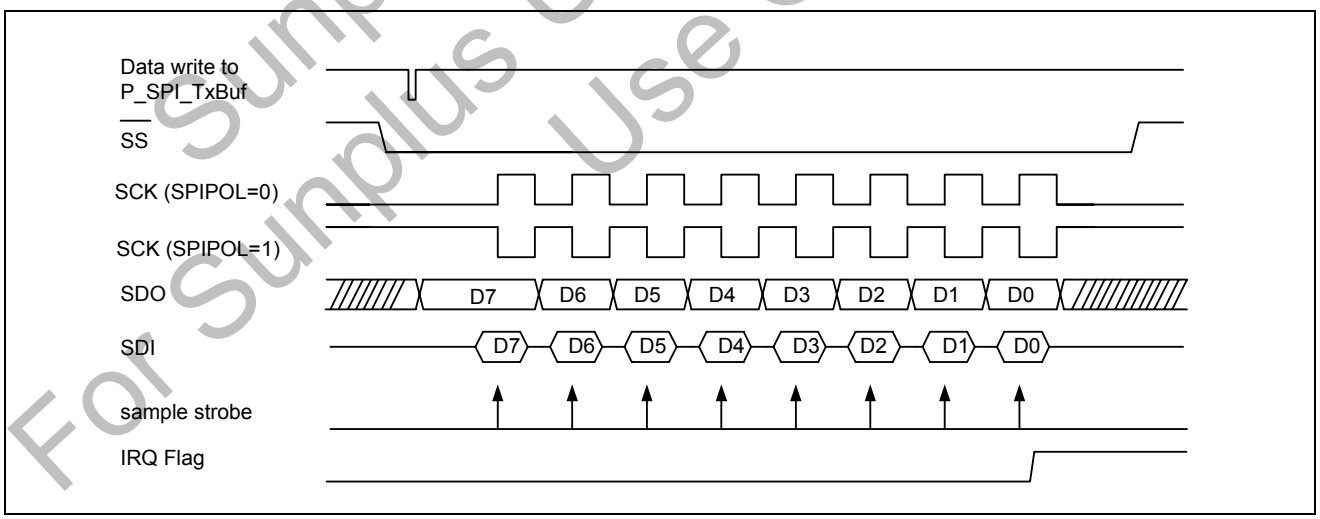


Figure 5-13 SPI Slave Mode Timing (SPIPHA=1)

Consecutive bytes transfer is available in both master and slave modes. For transmission, the firmware could send the data consecutively as long as the SPITBF flag is not set. For reception, the firmware should check for overrun error to monitor if there are any missing data due to the polling rate is too low.

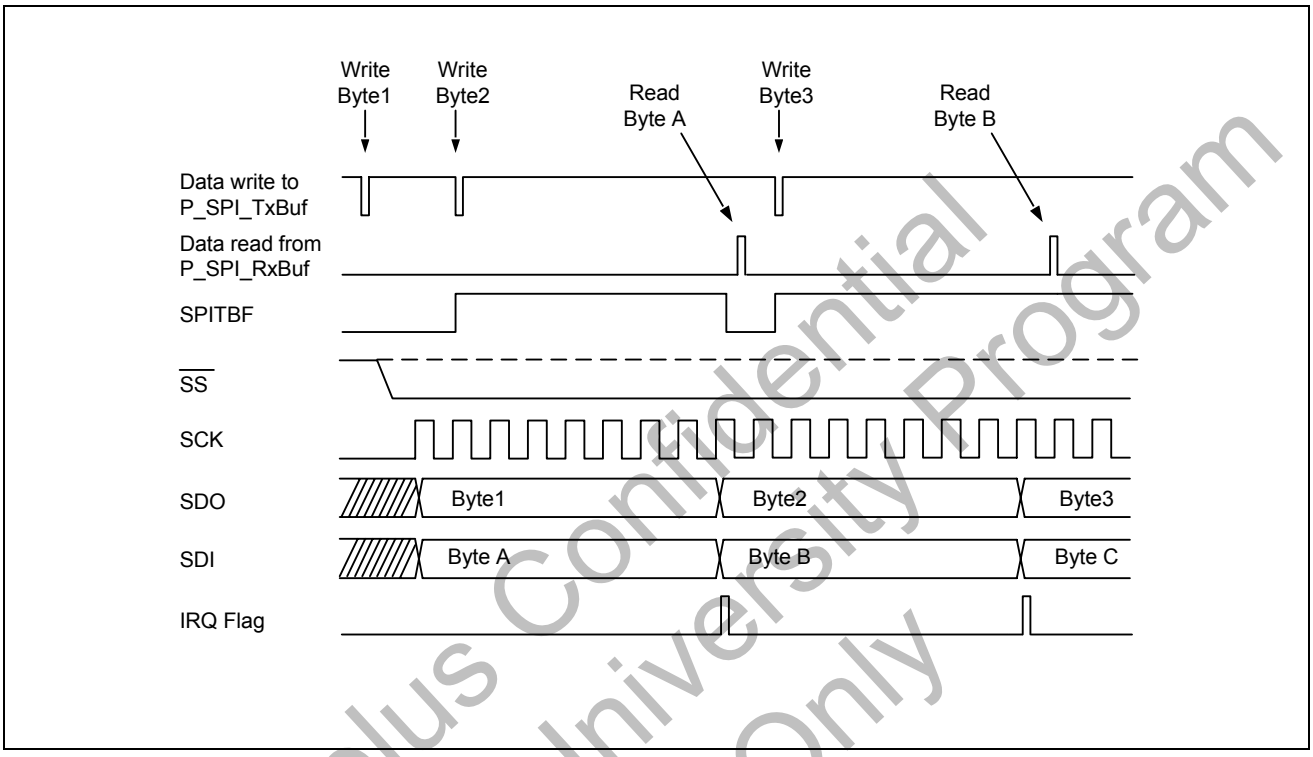


Figure 5-14 Consecutive bytes receiving timing (Master or slave mode SPIPOL=0;SPIPHA=0)

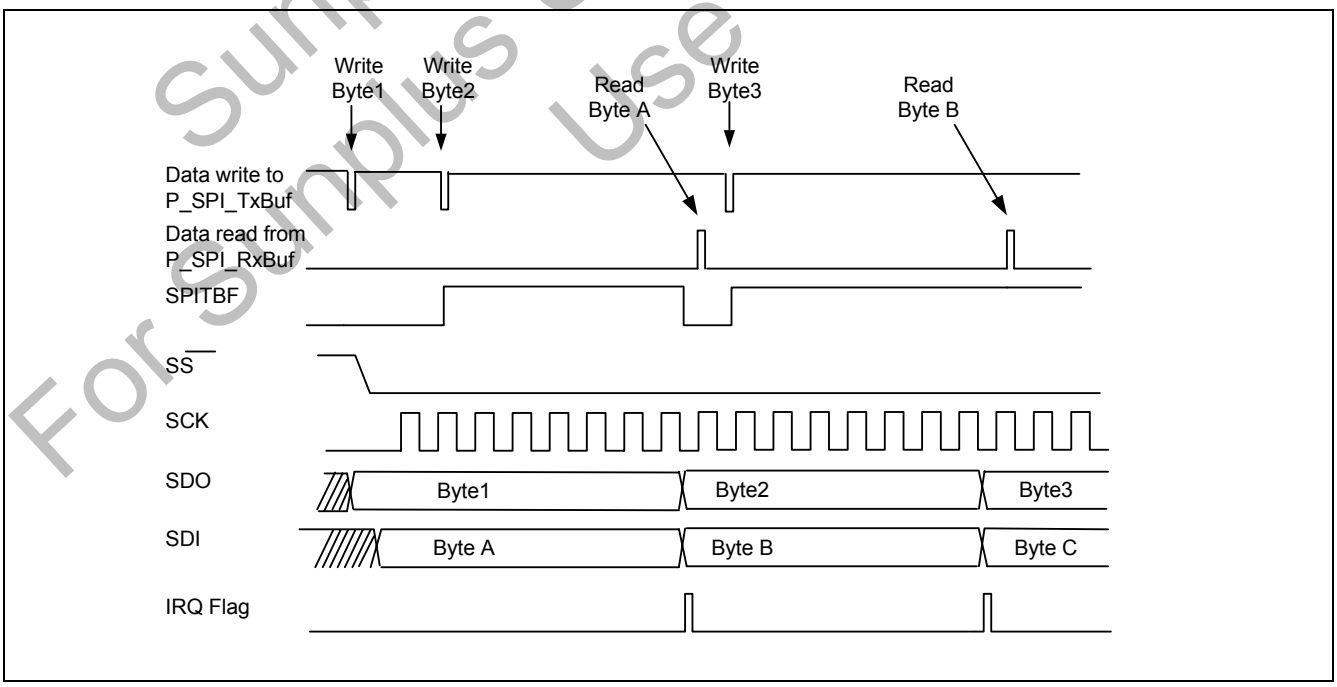


Figure 5-15 Consecutive bytes receiving timing (Slave mode, SPIPOL=0;SPIPHA=1)

5.13. Synchronous Serial IO (SIO)

The Synchronous Serial IO (SIO) supports half-duplex synchronous serial transfer between a Master device and a Slave device. The SIO module of SPMC701FM0A fully implements all slave functions, except general call support. To facilitate firmware implementations of the master functions, the interrupts on start and stop bits are asserted by hardware. Two pins are used for data transfer. These are the SCL pin that is the clock, and the SDA pin, which is the data. The SCL and SDA pins shared with GPIO PA[11:10] respectively and the two pins are configured as the required attributes (open drain, input/output) automatically when SIO is enabled. (Note: When the slave selection $\overline{SS}$ is used, SPI slave mode and SIO mode cannot be activated at the same time.)

The Master functions are implemented by firmware. In order to support Master functions, interrupts on Start (SIOSTRT) bit and Stop (SIOSTOP) bit are generated by hardware, which are only cleared by a system reset or when SIO is disabled. The Start (SIOSTRT) and Stop (SIOSTOP) status bits will toggle based on the START and STOP conditions. Control of the SIO may be taken when the SIOSTOP bit is set, or the bus is idle and both the SIOSTRT and SIOSTOP bits are clear. In master mode, the SCL and SDA lines are manipulated by clearing the corresponding SIOSCKOLB and SIOSDAOLB. In case of no master controlling bus lines, SCL and SDA keep high. First, master issues a START conditions, then data transfer by controlling the SCL states (write port to pull-low SCL and release SCL to generate the required clock pulses). Before generating clock pulses, the address or data has to be written into P_SIO_Buf first. At the same time, the address or data is also written into transmit shift register. The address/data is shifted out at the falling edge of SCL to keep data valid when SCL is high. The data shifted out is also received in receive shift register. If transmit has been finished, the interrupt will be issued and the data in receive shift register be loaded in P_SIO_Buf. The firmware can compare the data in P_SIO_Buf with the data that is just transmitted. By this way, CPU can identify if arbitration condition has occurred and terminate the transmit session. The Acknowledge bit state is detected to make sure that the addressed Slave receives the previous data octet. If Not-Acknowledge is detected, Not-Acknowledge bit will be set. The firmware can monitor Not-Acknowledge bit to identify not-acknowledge condition and issues a STOP condition.

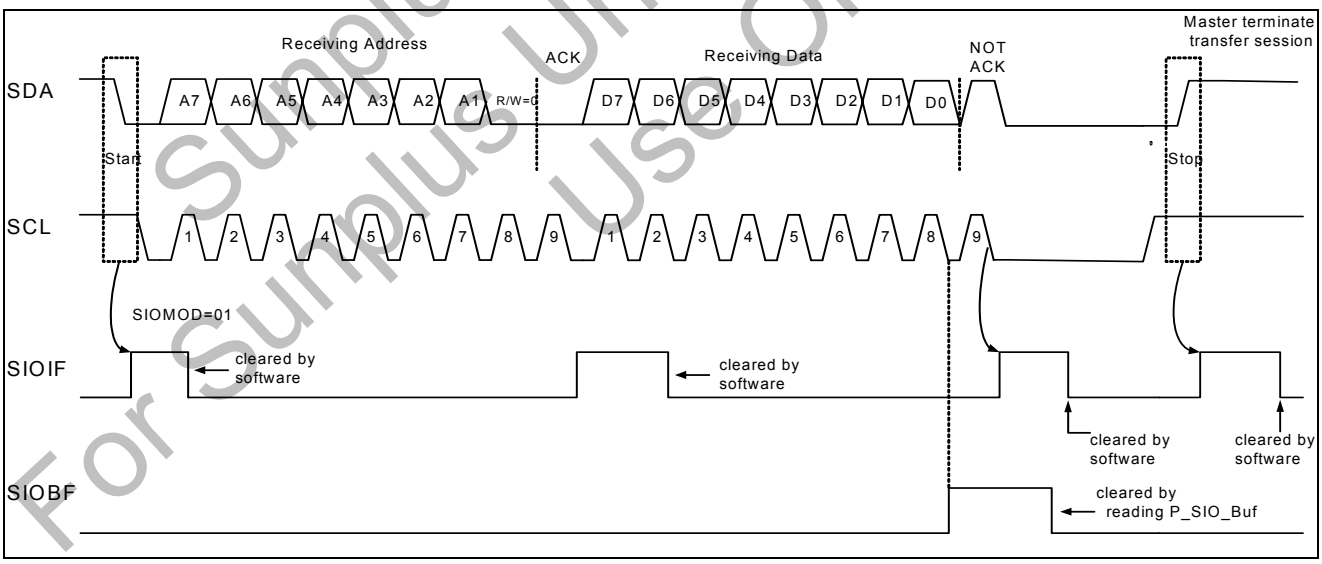


Figure 5-16 SIO waveforms reception for Slave mode (7-bit Address)

Slave-receiver receives the address, compares the address and response an Acknowledge bit on SDA line, records the 8th bit (read/write) status, and asserts an interrupt to CPU. In case of received address mismatched with P_SIO_Addr, an interrupt will not be issued. In 10-bit address mode, two address bytes need to be received by the slave. The first five bits of the first address byte specify if this is a 10-bit address. The R/W bit must specify a write so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the first two bits of the address. After the first address byte is received, the SIOUA bit in status register and SCL pin is held low until CPU write the second address byte to address register. CPU on Slave can responses the interrupt from SIO module and read the status register and P_SIO_Buf. When the R/W bit of the incoming address byte is set and an address match occurs, the SIODIRT bit in SIO_Status is set. Slave operates as a

transmitter. The ACK will be sent on the ninth bit, and the SCL pin is held low. The transmitted data must be loaded into the P_SIO_Buf register, then SCL pin is released by slave. The master should monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the SCL clock.

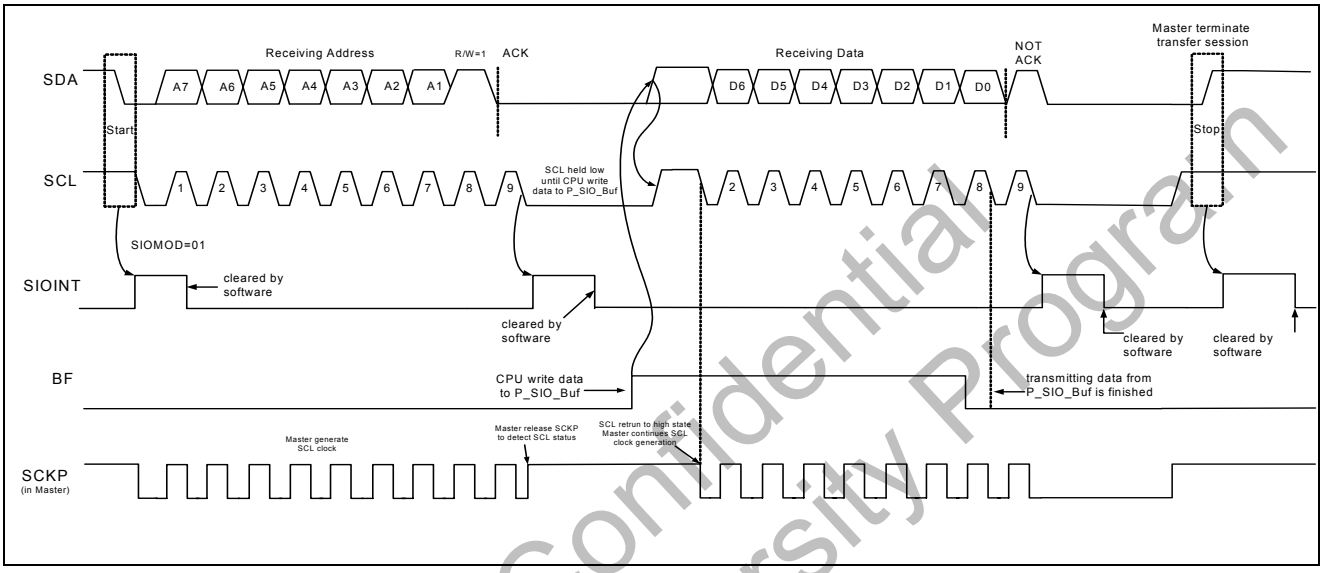


Figure 5-17 SIO waveforms transmission for Slave mode (7-bit Address)

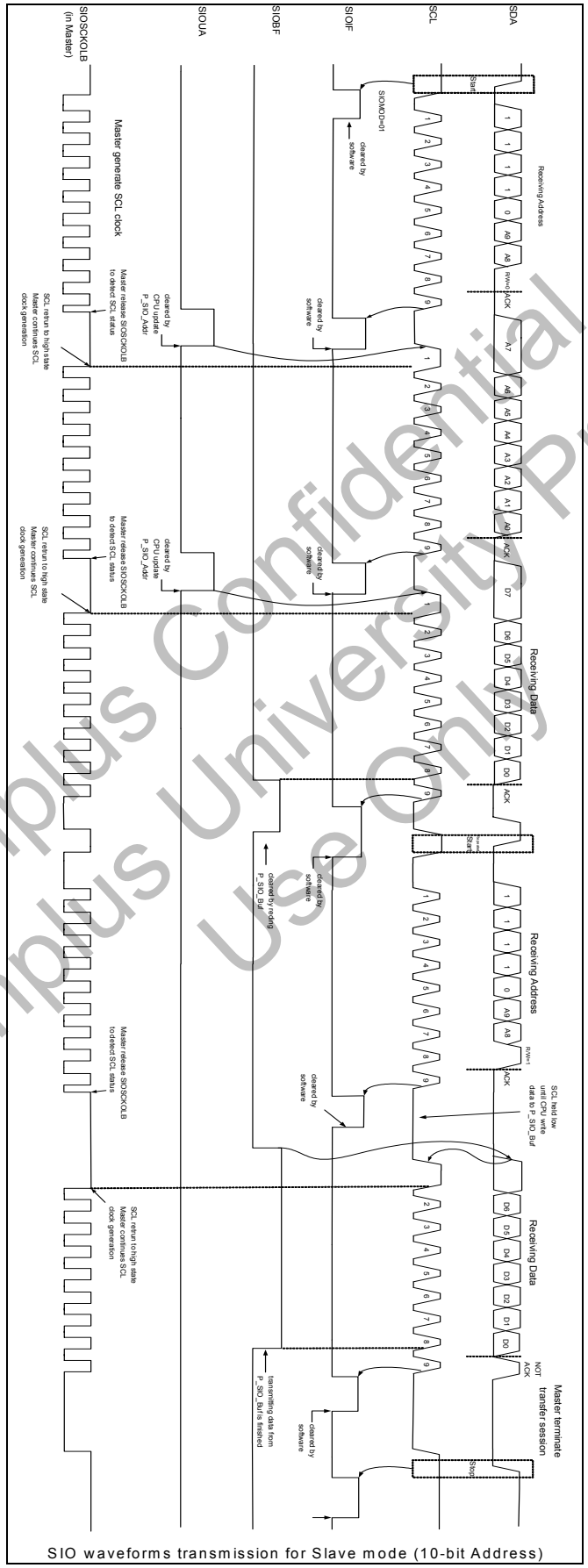


Figure 5-18

5.14. Parallel Communication Interface (PCI)

The Parallel Communication Interface (PCI) provides half-duplex asynchro-nous parallel communication between a Master device and a Slave device. The PCI module of SPMC701FM0A supports both of the Master mode and Slave mode.

To be as a Master, the hardware generates the required interface signals to Slave. The communication cases between a Master and a Slave include:

1.) Master reads Slave's status of Slave to Master's input buffer
2.) Master reads Slave's output buffer of Slave to Master's input buffer
3.) Master sends command to Slave
4.) Master sends data to Slave

Parallel Interface Signals is described as follows:

1.) PCID7 – PCID0: parallel data bus (I/O).
2.) PCSB: chip select (Input for Slave and Output for Master), low active.
3.) PRDB: read control signal (Input for Slave and Output for Master), low Active.
4.) PWEB: write control signal (Input for Slave and Output for Master), low active. In case of RSTEN = 1, this pin is configured as system reset output.
5.) PCIA0: indicate that command/data which master write to slave, or status/data which master read from slave (Input for Slave and Output for Master).

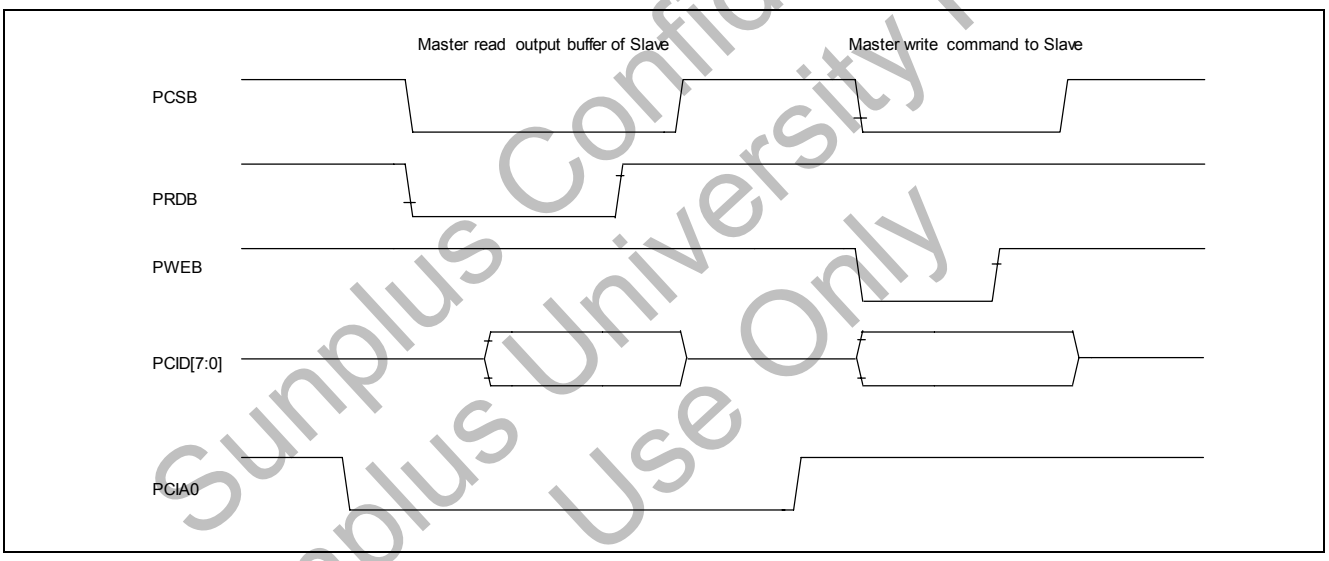


Figure 5-19 Parallel communication interface read/write operation timing

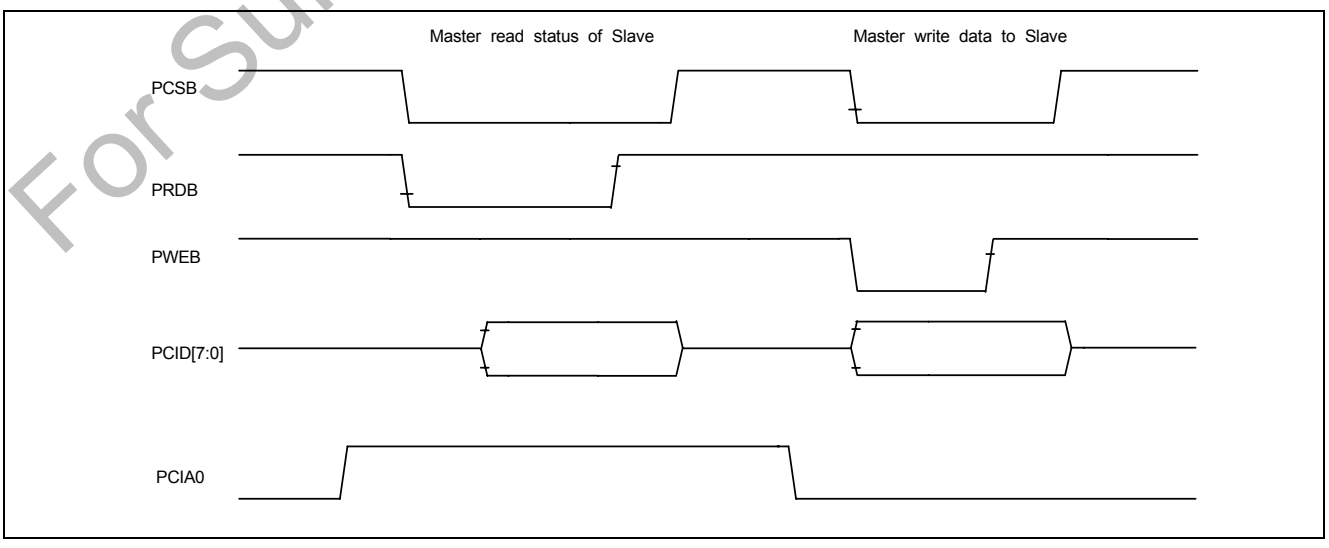


Figure 5-20 Parallel communication interface read/write operation timing

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
PA/PB/PC/PD Pad Supply Voltage	V_{IO}	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions, see DC Electrical Characteristics.

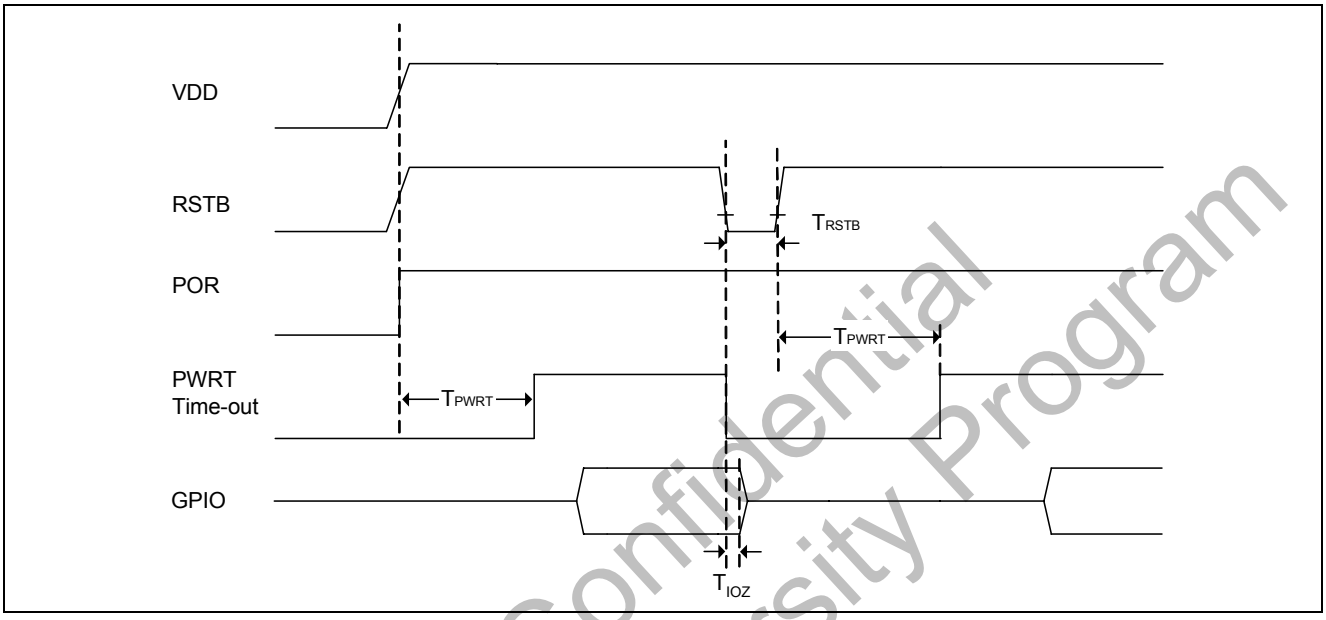
6.2. DC Characteristics (VDD = 3.3V, VDD_{IO} = 3.3V ~ 5.0V (PA, PB, PC, PD), T_A = 0 ~ 70°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.0	3.3	3.6	V	
LVR voltage	V_{LVR}	2.4	2.6	2.8	V	
Reference voltage	V_{REF2V}	1.8	2.0	2.2	V	
Operating Current	I_{OPT}		-	35	mA	VDD_{IO} = 3.3V
			-	40		VDD_{IO} = 5.0V
Halt Current	I_{HLT}	-	-	25	mA	Halt mode, CPU off
Standby Current	I_{STB}	-	1.0	5.0	μA	Standby mode, all clock off
Input High Level	V_{IH}	0.7VDDIO	-	-	V	
Input Low Level	V_{IL}	-	-	0.3VDDIO	V	
Output High Current	I_{OH1}	1.6	-	-	mA	VDD_{IO} = 3.3V, V_{OH} = 2.4V
		1.7	-	-		VDD_{IO} = 5.0V, V_{OH} = 4.5V
	I_{OH2}	6.0	-	-	mA	VDD_{IO} = 3.3V, V_{OH} = 2.4V (PB[13:10] only)
		6.0	-	-		VDD_{IO} = 5.0V, V_{OH} = 4.5V (PB[13:10] only)
Output Low Current	I_{OL1}	2.0	-	-	mA	VDD_{IO} = 3.3V, V_{OL} = 0.5V
		3.0	-	-		VDD_{IO} = 5.0V, V_{OL} = 0.5V
	I_{OL2}	8.0	-	-	mA	VDD_{IO} = 3.3V, V_{OL} = 0.5V (PB[13:10] only)
		11	-	-		VDD_{IO} = 5.0V, V_{OL} = 0.5V (PB[13:10] only)
Input Pull-Low Resister	R_{PL}	-	185	-	KΩ	VDD_{IO} = 3.3V, V_O = VDDIO
		-	110	-		VDD_{IO} = 5.0V, V_O = VDDIO
Input Pull-High Resister	R_{PH}	-	270	-	KΩ	VDD_{IO} = 3.3V, V_O = VSS
		-	160	-		VDD_{IO} = 5.0V, V_O = VSS

Note: Data in "Typ" column is at 25°C unless otherwise stated.

6.3. AC Characteristics

6.3.1. External reset, Power-On Reset, Power-Up Timer Timing

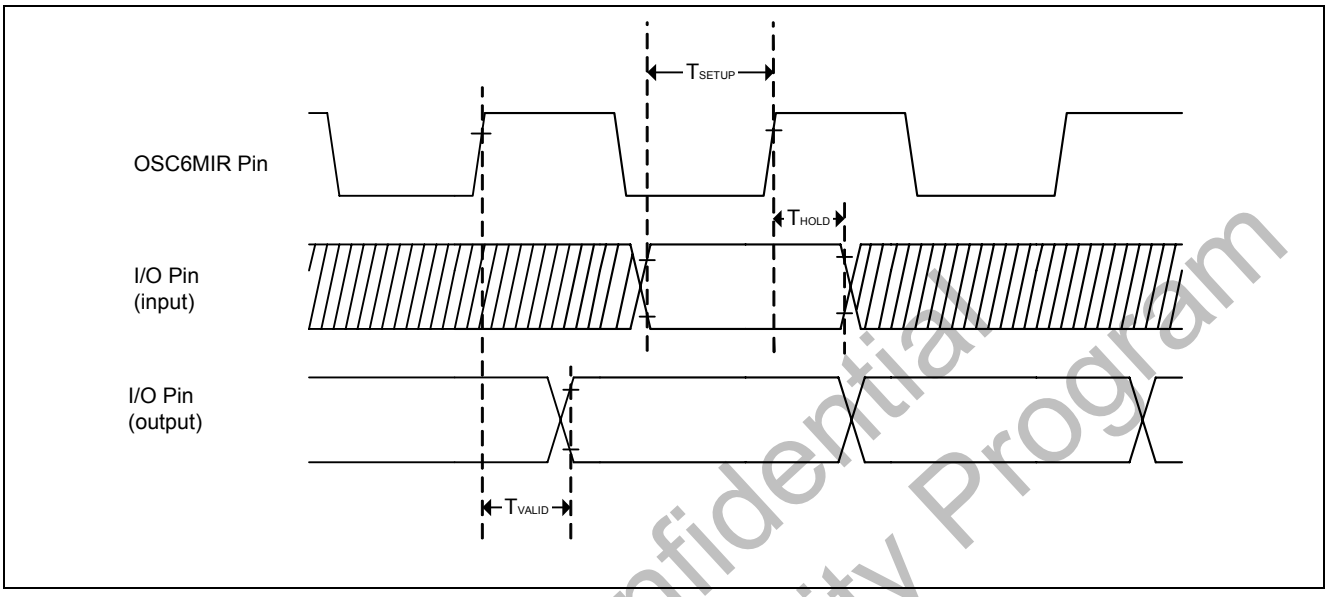


(VDD = 3.3V, VDDIO = 3.3V ~ 5.0V, T_A = 0 ~ 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
VDD Rise Rate to ensure Power-On Reset	S_{VDD}	0.5	-	-	V/μs	
Power-up Timer time out	T_{PWRT}	-	82	-	ms	
External reset pulse width	T_{RSTB}	2.0	-	-	μs	
External reset pulse width	T_{RSTB}	40	-	-	μs	
GPIO Hi-impedance from RSTB low	T_{IOZ}	-	10	-	ns	

Note: Data in "Typ" column is at 25°C unless otherwise stated.

6.3.2. GPIO output timing

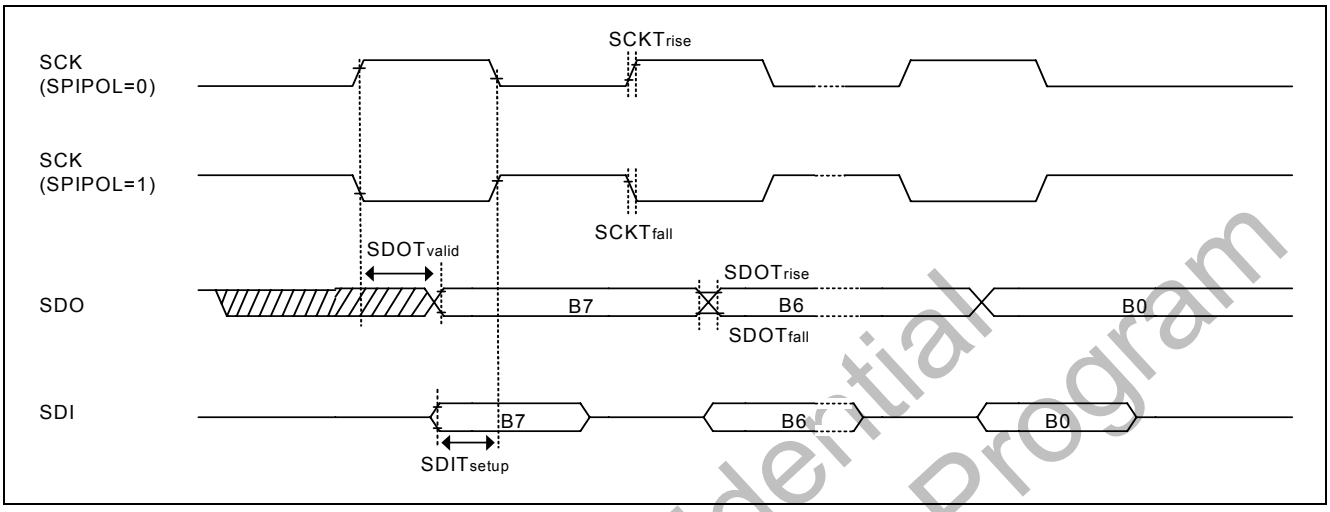


(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 ~ 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
GPIO port input to OSC6MIR ↑ setup time	T_{SETUP}	2.0	-	-	ns	
GPIO port input to OSC6MIR ↑ hold time	T_{HOLD}	2.0	-	-	ns	
OSC6MIR ↑ to GPIO port output valid	T_{VALID}	-	50	-	ns	VDDIO = 3.3V
		-	45	-		VDDIO = 5.0V
		-	30	-		VDDIO = 3.3V - 5.0V PB[13:10] only
Output rise time	T_{RISE}	-	40	-	ns	VDDIO = 3.3V
		-	30	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V ~ 5.0V PB[13:10] only
Output fall time	T_{FALL}	-	25	-	ns	VDDIO = 3.3V
		-	15	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V ~ 5.0V PB[13:10] only,

Note: Data in "Typ" column is at 25°C unless otherwise stated.

6.3.3. SPI Mode timing requirements (Master Mode, SPIPHA = 0)

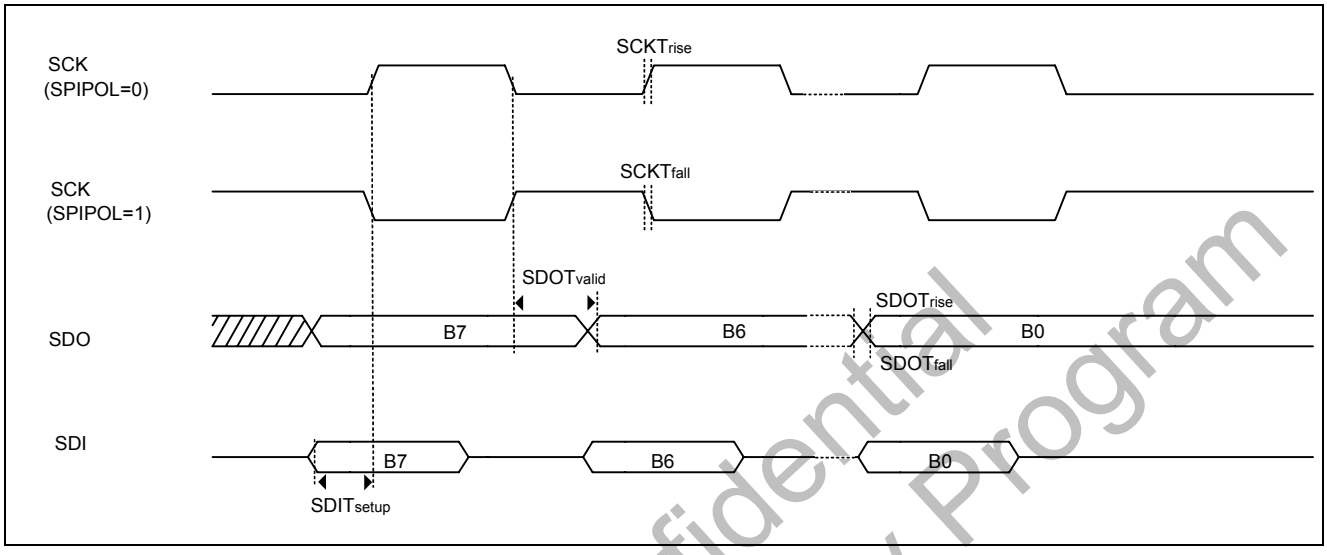


(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 ~ 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Setup time of SDI data to SCK edge	$SDIT_{setup}$	10	-	-	ns	
SDO data output valid after SCK edge	$SDOT_{valid}$	-	-	-	ns	
SCK and SDO output rise time	$SCKT_{rise}$	-	40	-	ns	VDDIO = 3.3V
		-	30	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only
SCK and SDO output fall time	$SCKT_{fall}$	-	25	-	ns	VDDIO = 3.3V
		-	15	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only

Note: Data in "Typ" column is at 25°C unless otherwise stated.

6.3.4. SPI mode timing requirements (Master Mode, SPIPHA=1)

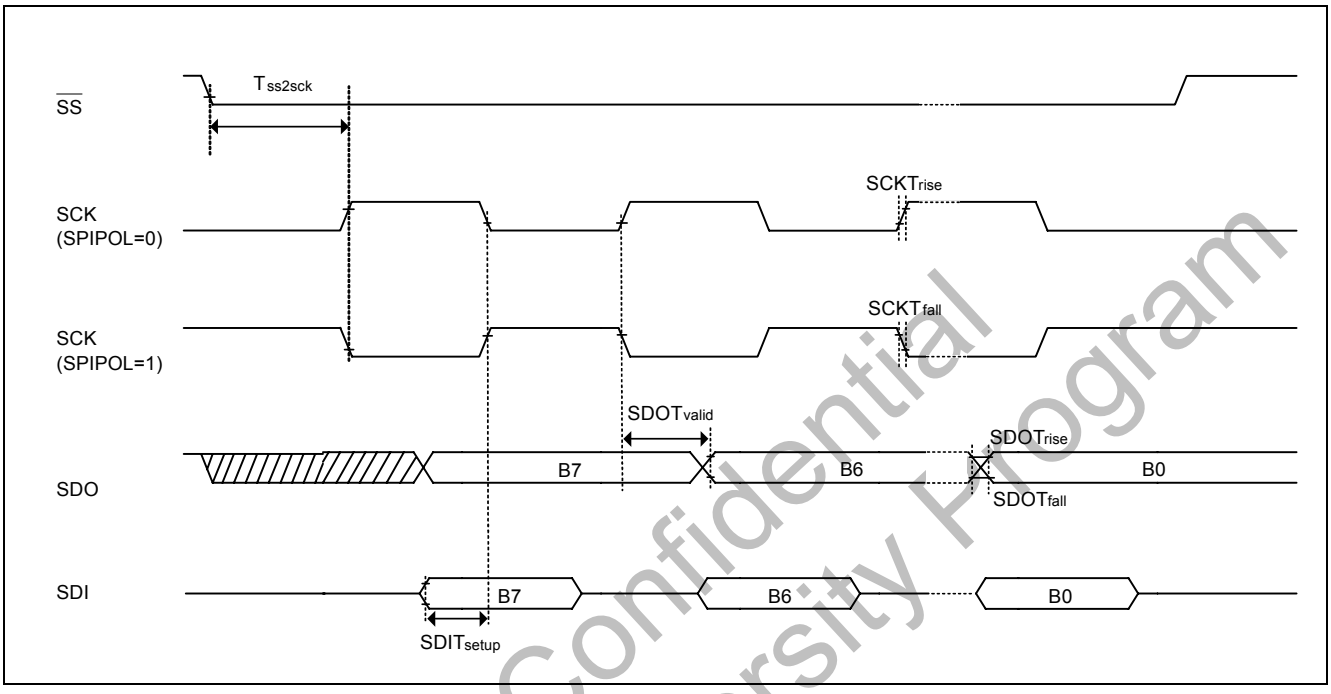


(VDD= 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 ~ 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Setup time of SDI data to SCK edge	$SDIT_{setup}$	10	-	-	ns	
SDO data output valid after SCK edge	$SDOT_{valid}$	-	-	-	ns	
SCK and SDO output rise time	$SCKT_{rise}$	-	40	-	ns	VDDIO = 3.3V
		-	30	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5V PB[13:10] only
SCK and SDO output fall time	$SCKT_{fall}$	-	25	-	ns	VDDIO = 3.3V
		-	15	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only

Note: Data in "Typ" column is at 25°C unless otherwise stated.

6.3.5. SPI mode timing requirements (Slave Mode, SPIPHA=0)

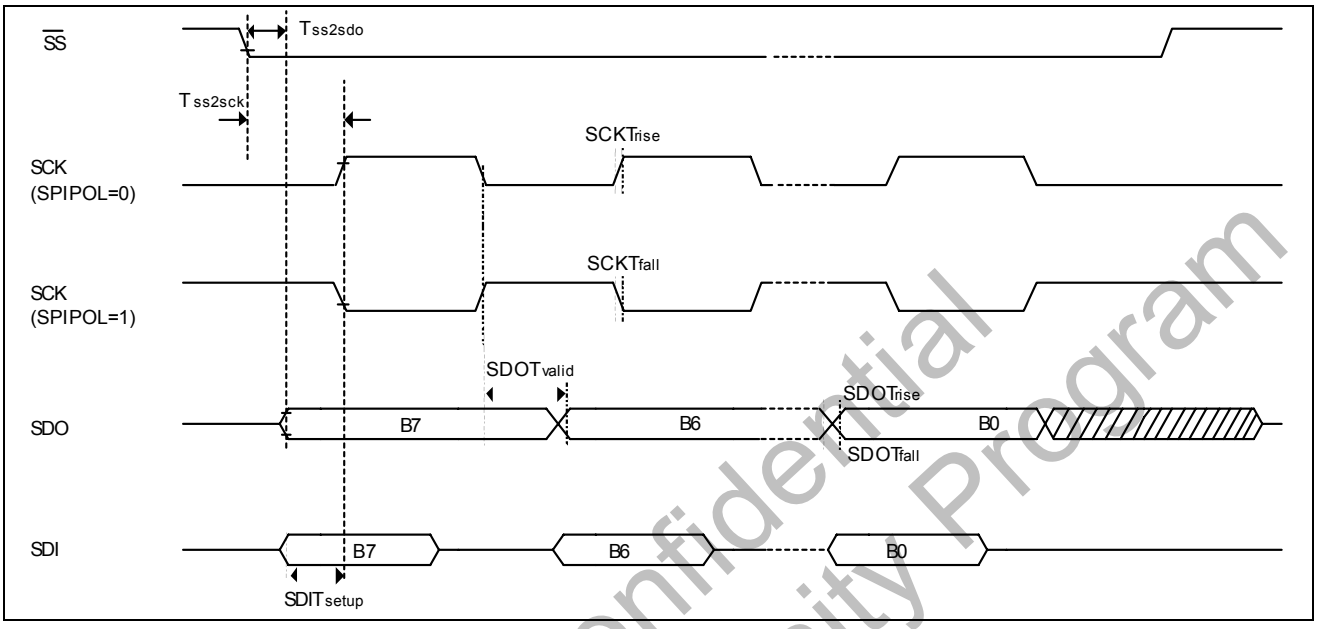


(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 - 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
The time of $\overline{SS}\downarrow$ to SCK	T_{ss2sck}	10	-	-	ns	
Setup time of SDI data to SCK edge	$SDIT_{setup}$	10	-	-	ns	
SDO data output valid after SCK edge	$SDOT_{valid}$	-	25	-	ns	
SCK and SDO output rise time	$SCKT_{rise}$	-	40	-	ns	VDDIO = 3.3V
		-	30	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only
SCK and SDO output fall time	$SCKT_{fall}$	-	25	-	ns	VDDIO = 3.3V
		-	15	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only

Note: Data in "Typ" column is at 25°C unless otherwise stated.

6.3.6. SPI mode timing requirements (Slave Mode, SPIPHA = 1)

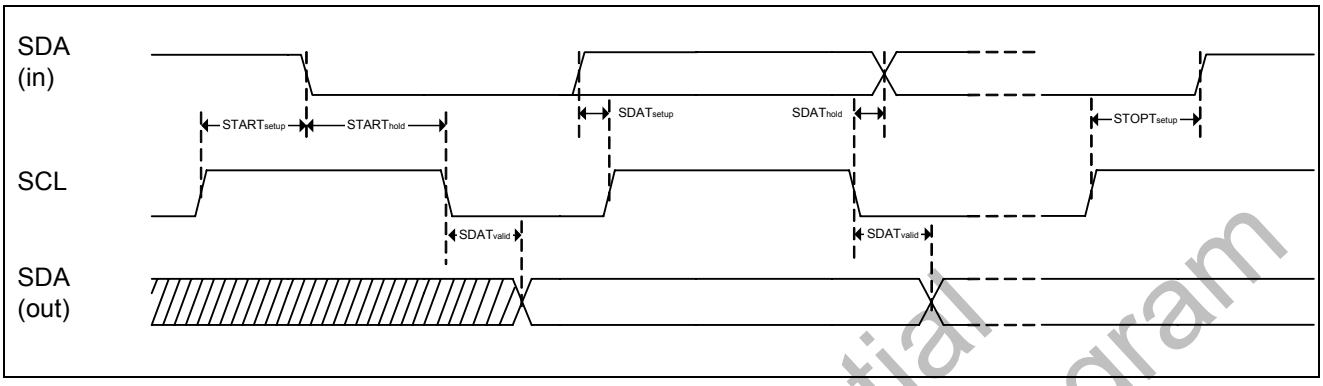


(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 - 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
The time of $\overline{SS}\downarrow$ to SCK	T_{ss2sck}	10	-	-	ns	
SDO data output valid after $\overline{SS}\downarrow$ edge	T_{ss2sdo}	-	15	-	ns	
Setup time of SDI data to SCK edge	$SDIT_{setup}$	10	-	-	ns	
SDO data output valid after SCK edge	$SDOT_{valid}$	-	25	-	ns	
SCK output rise time	$SCKT_{rise}$	-	40	-	ns	VDDIO = 3.3V
		-	30	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only
SCK output fall time	$SCKT_{fall}$	-	25	-	ns	VDDIO = 3.3V
		-	15	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only

Note: Data in "Typ" column is at 25°C unless otherwise stated

6.3.7. SIO timing requirements

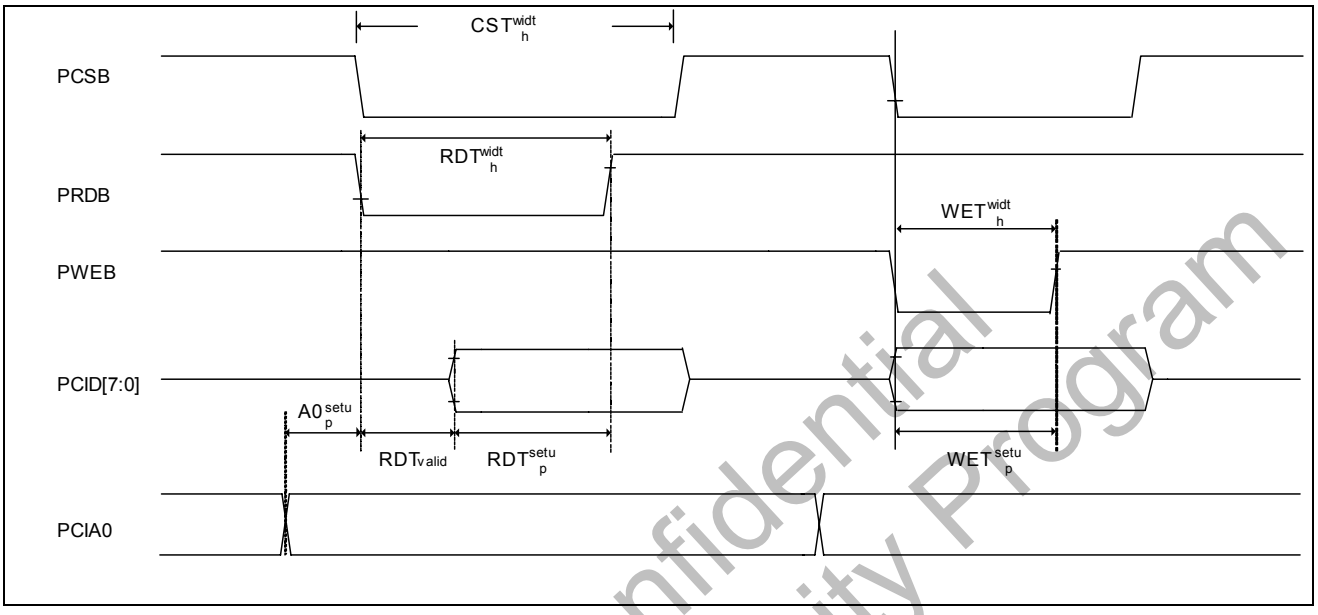


(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 - 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Setup time of START condition	START$_{setup}$	100	-	-	ns	
Hold time of START condition	START$_{hold}$	100	-	-	ns	
Setup time of STOP condition	STOP$_{setup}$	100	-	-	ns	
SDA output Setup time	SDA$_{setup}$	50	-	-	ns	
SDA output Hold time	SDA$_{hold}$	50	-	-	ns	
SDO data output valid after SCK edge	SDOT$_{valid}$	-	25	-	ns	
SCK output rise time	SCKT$_{rise}$	-	40	-	ns	VDDIO = 3.3V
		-	30	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only
SCK output fall time	SCKT$_{fall}$	-	25	-	ns	VDDIO = 3.3V
		-	15	-		VDDIO = 5.0V
		-	15	-		VDDIO = 3.3V - 5.0V PB[13:10] only

Note: Data in "Typ" column is at 25°C unless otherwise stated

6.3.8. Parallel communication interface timing requirements (12-pin mode)



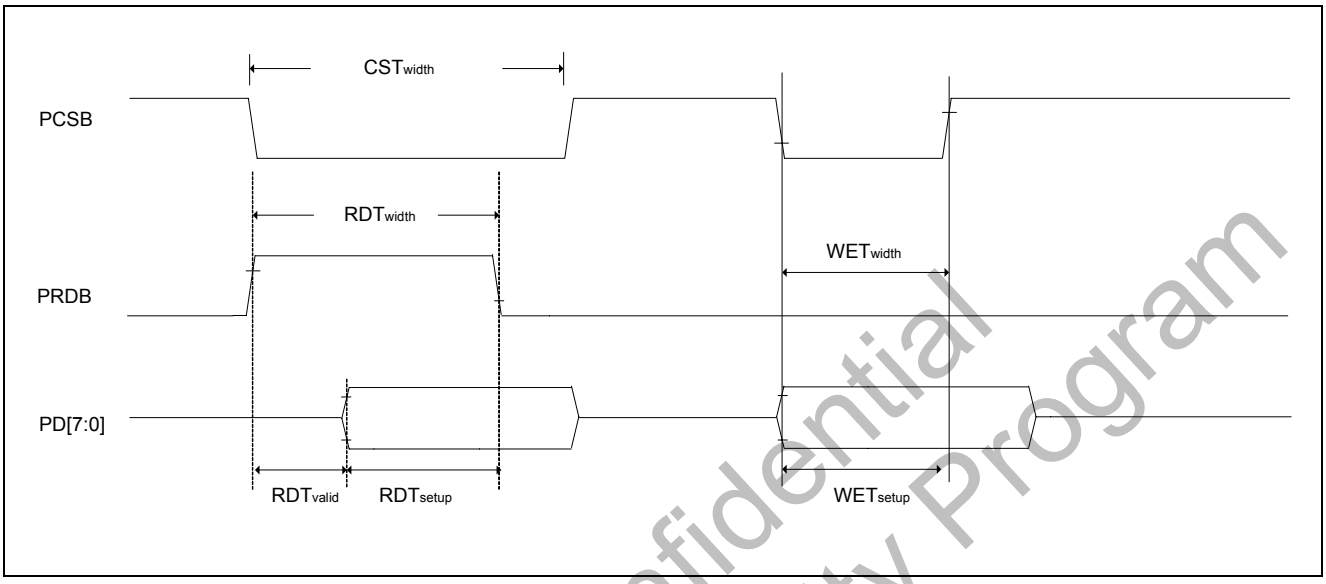
(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 ~ 70°C, C_{Load} = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
PCSB low time	CSTwidth	-	4Tosc	-	ns	Read operation, Note2
		-	3Tosc	-	ns	Write operation, Note2
PRDB low time	RDTwidth	-	3Tosc	-	ns	Note2
PWEB low time	WETwidth	-	2Tosc	-	ns	
CSB ↓ and PRDB ↓ to data out valid	RDTvalid	-	50	-	ns	VDDIO = 3.3V
		-	40	-		VDDIO = 5.0V
Setup time of data input to PRDB edge (for master)	RDTsetup	7	-	-	ns	
Setup time of data input to PWEB edge (for slave)	WETsetup	10	-	-	ns	

Note1: Data in "Typ" column is at 25°C unless otherwise stated

Note2: Tosc is one system clock period

6.3.9. Parallel communication interface timing requirements (11-pin mode)



(VDD = 3.3V, VDDIO = 3.3V - 5.0V, T_A = 0 - 70°C, CL = 50pF)

Characteristics	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
PCSB low time	CSTwidth	-	4Tosc	-	ns	Read operation, Note2
		-	2Tosc	-	ns	Write operation, Note2
PRDB high time	RDTwidth	-	3Tosc	-	ns	Note2
PWEB low time	WET_{width}	-	2Tosc	-	ns	Note2
PCIA0 setup time	$A0_{setup}$	-	1Tosc	-	ns	Note2
CSB ↓ and PRDB ↓ to data out valid	RDT_{valid}	-	50	-	ns	VDDIO = 3.3V
		-	40	-		VDDIO = 5.0V
Setup time of data input to PRDB edge (For master)	RDT_{setup}	7.0	-	-	ns	
Setup time of data input to PWEB edge (For slave)	WET_{setup}	10	-	-	ns	

Note1: Data in "Typ" column is at 25°C unless otherwise stated

Note2: Tosc is one system clock period

6.3.10. ADC characteristics (AVDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
ADC Line_In Input Voltage Range from PB[7:0]	VINL (Note 1)	AVSS-0.3	-	AVDD+0.3	V
External ADC Top Voltage	VEXTREF (Note 2)	2.0	-	AVDD+0.3	V
Resolution of ADC	RESO	-	-	10	bits
Effective Number of Bit	ENOB (Note 4)	8.0	9.0	-	bits
Integral Non-Linearity of ADC	INL	-	±4.0	-	LSB (Note 3)
Differential Non-Linearity of ADC	DNL (Note 5)	-	±0.5	-	LSB
AD Conversion Rate	F_{SH}	-	-	100K	Hz

Note1: Internal protection diodes clamp the analog input to VDD and VSS. These diodes allow the analog input to swing from (VSS-0.3V) to (VDD+0.3V) without causing damage to the devices.

Note2: The ADC performance is limited by the system's noise level, so the SPMC701FM0A just guarantee with the 8-bit accuracy when VEXTREF is 2.0V.

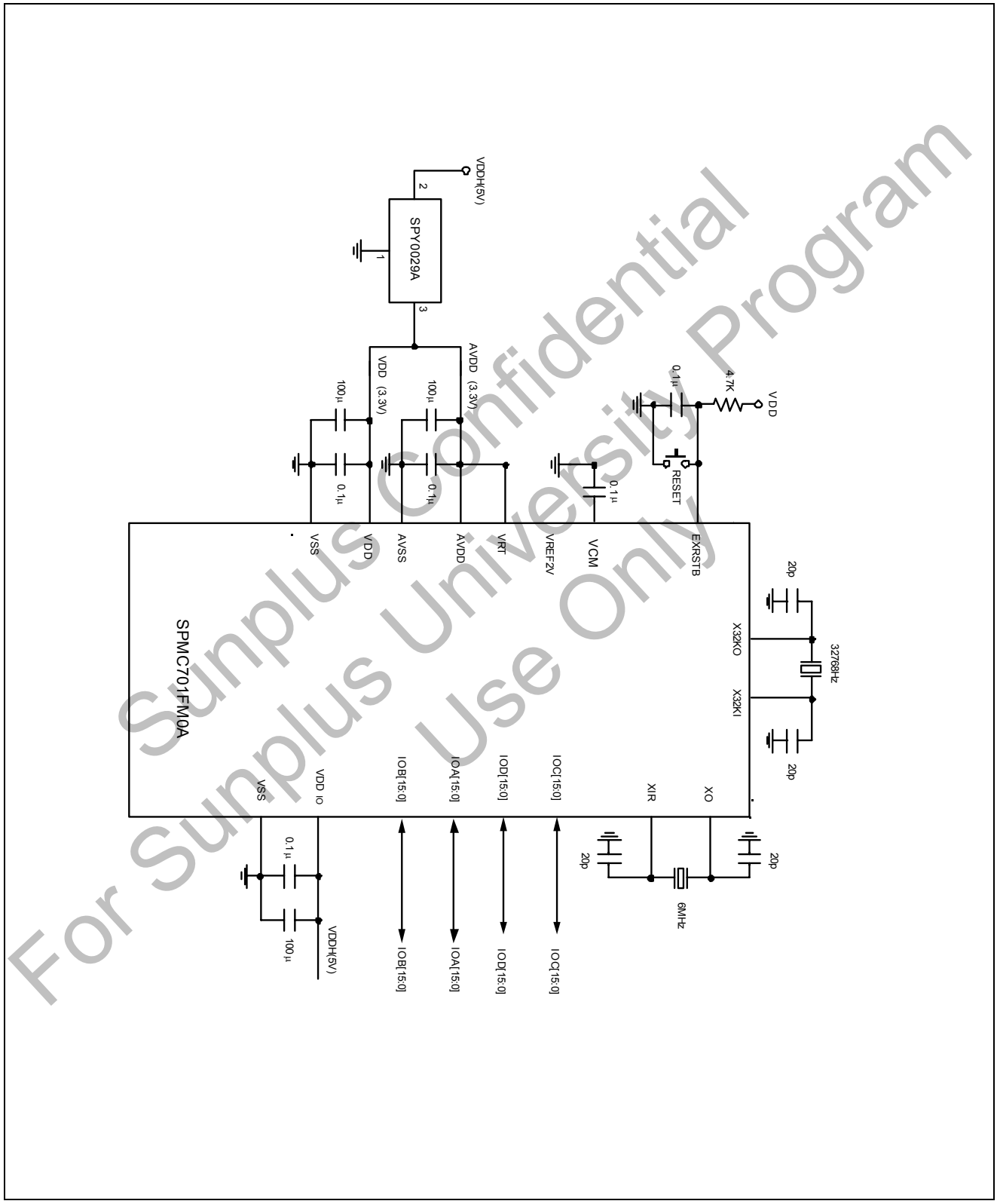
Note3: LSB means Least Significant Bit. With VINL=2.0V, 1LSB=2.0V/2^10= 1.953 mV.

Note4: ENOB=(SINAD-1.76)/6.02.

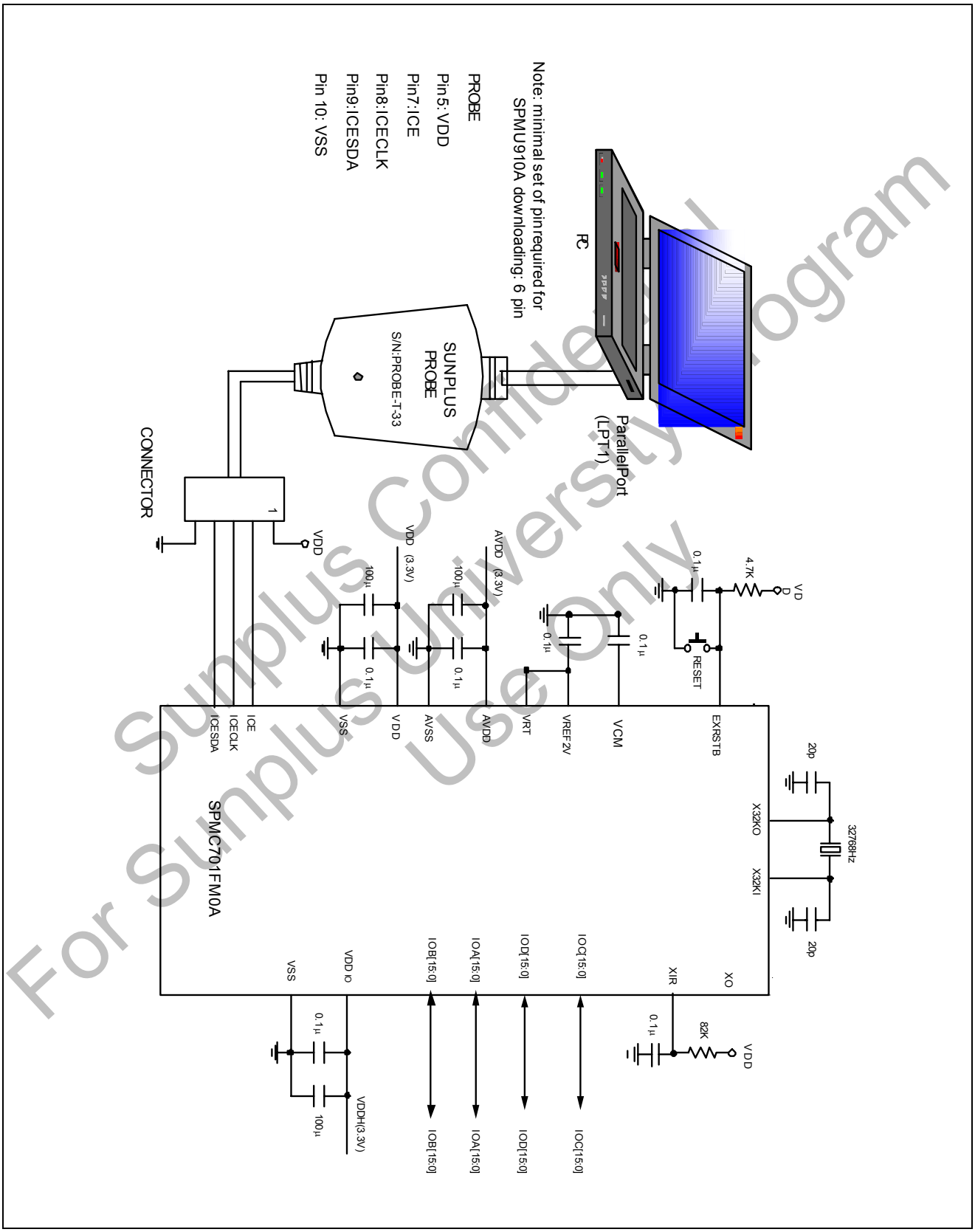
Note5: The ADC of SPMC701FM0A can guarantee no missing code.

7. APPLICATION CIRCUITS

7.1. Application Circuit - (1)



7.2. Application Circuit - (2)



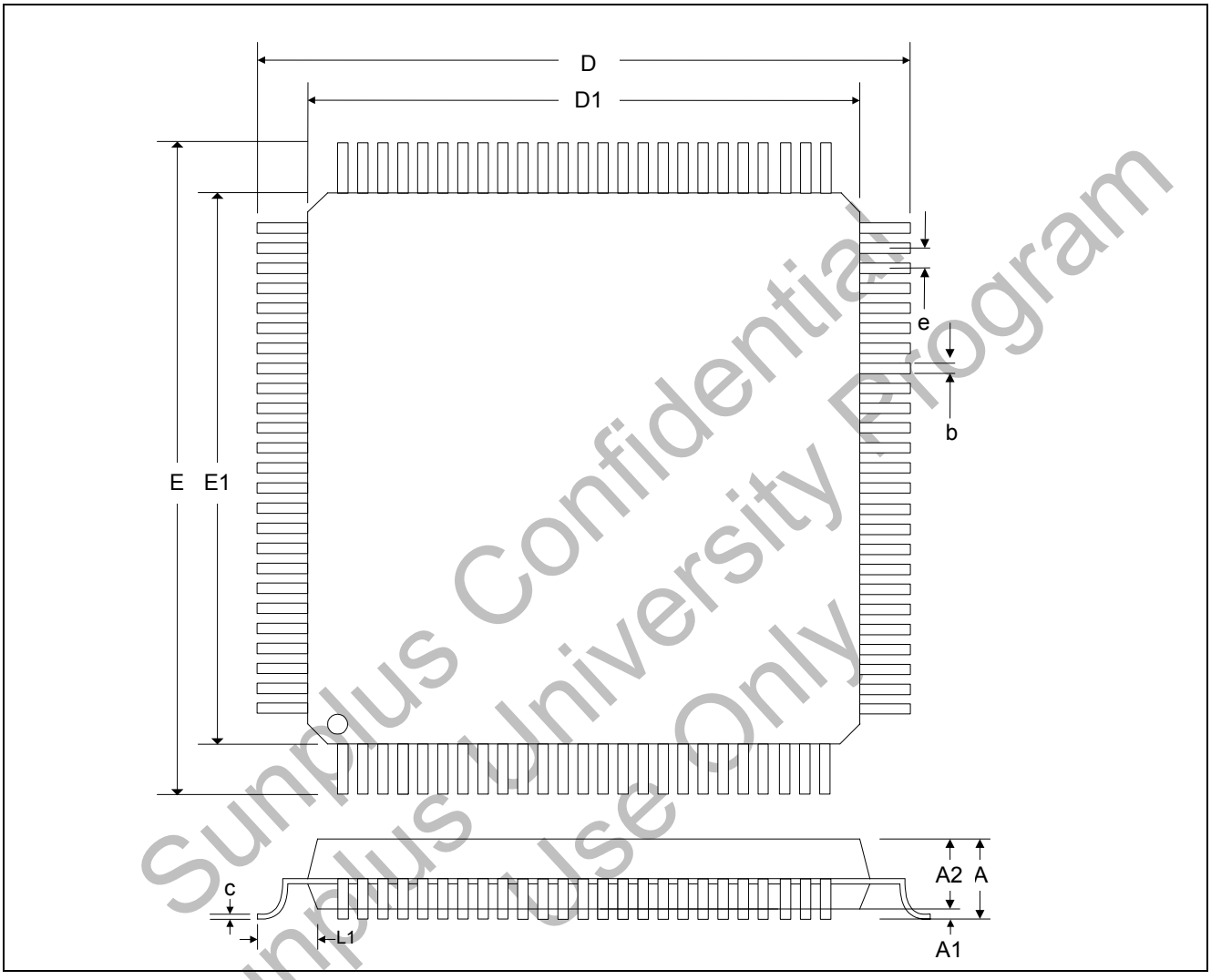
8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

8.2. Package Information

8.2.1. LQFP 100



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	0.063
A1	0.002	-	0.006
A2	0.053	0.055	0.057
b	0.007	0.008	0.011
c	0.004	-	0.008
D	0.630 BSC.		
D1	0.551 BSC.		
E	0.630 BSC.		
E1	0.551 BSC.		
e	0.020 BSC.		
L1	0.039 REF		

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 10, 2003	0.2	1.Modify “Programmable dual CPU clock: 32768Hz, 750KHz, 1.5MHz, 3MHz, 6MHz, 12MHz, 24MHz, 48MHz” to “Programmable CPU clock: 6MHz, 12MHz, 24MHz, 48MHz”	3
		2.Modify “Operating voltage: 3.0V ~ 3.6V @ 48MHz” to “Operating voltage: 3.0V ~ 3.6V”, remove “2.7V ~ 3.6V @ 24MHz ~ 32768Hz”	
		3.Modify “Operating voltage for Flash programming: 2.7V ~ 3.6V” to “Operating voltage for Flash programming: 3.0V ~ 3.6V”	
		4.Modify “IO PA, PB, PC, PD operating voltage: 2.7V ~ 5.0V” to “IO PA, PB, PC, PD operating voltage: 3.0V ~ 5.0V”	
		5. Remove the detailed description of verification pattern in the information block.	9-11
		6. Remove the description of clock filter, modify Figure 5-2	
		7. Remove sleep mode in power saving, modify Table 5-2, 5-3	
		8. Add interrupt priority	
		9. Modify GPIO diagram Figure 5-4	
		10. Rewrite “Timer/Counters with Capture/Compare/PWM Functions”	13-14
		11. Modify the last sentence in section 5.11(ADC)	
		12. Rewrite section 5.13(SPI)	15-16
		13. Remove “Sleep Current”, modify “Operating Voltage”	22
		14. Rename “SPMU910A” to “SPMC701FM0A”	
		15. Modify “PA0” to “PCIA0”	4
		16. Correct package information	5, 12,
		17. Rewrite document	21, 30
AUG. 04, 2003	0.1	Original	