# **4-Bit Arithmetic Logic Unit**

The MC14581B is a CMOS 4-bit ALU capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 14-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate  $(\overline{P})$  and carry generate  $(\overline{G})$  outputs are provided to allow a full look—ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input  $(C_n)$  and a ripple carry output  $(C_{n+4})$  are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4–bit words present at the  $\overline{A}$  and  $\overline{B}$  inputs is provided using the A = B output. It assumes a high–level state when indicating equality. Also, when the ALU is in the subtract mode the  $C_{n+4}$  output can be used to indicate relative magnitude as shown in this table:

Data Level	Cn	C <sub>n+4</sub>	Magnitude
Active High	HLHL	HLL	A ≤ B A < B A > B A ≥ B
Active Low	L H L H	L H H	A ≤ B A < B A > B A ≥ B

- Functional and Pinout Equivalent to 74181.
- · Diode Protection on All Inputs
- · All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	– 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

# MC14581B



L SUFFIX CERAMIC CASE 623



P SUFFIX PLASTIC CASE 709



SOIC CASE 751E

#### ORDERING INFORMATION

MC14XXXBCP Plastic MC14XXXBCL Ceramic MC14XXXBDW SOIC

 $T_A = -55^{\circ}$  to  $125^{\circ}$ C for all packages.

#### **PIN ASSIGNMENT** 24 D VDD 23 🛮 Ā1 Ā0 ☐ 2 3 S3 [ 21 🛮 🗚 S2 [ S1 🛮 5 20 | B2 S0 [ 6 19 **□** Ā3 $c_n$ 18 MC **∏** 8 ΠG 17 F0 [ 9 16 C<sub>n+4</sub> 15 | P 0 F2 [ 11 14 🛮 A = B V<sub>SS</sub> [] 12 13 🛮 F3



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

			V <sub>DD</sub>	- 5	5°C		25°C		125	i°C	
Characteristic		Symbol	Vdc	Min	Max	Min	Тур #	Max	Min	Max	Unit
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	VOL	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level	VOH	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0 10 15	_ _ _	1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	VIH	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	ЮН	5.0 5.0 10 15	- 1.2 - 0.64 - 1.6 - 4.2		- 1.0 - 0.51 - 1.3 - 3.4	- 1.7 - 0.88 - 2.25 - 8.8		- 0.7 - 0.36 - 0.9 - 2.4		mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	l <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Capacitance (V <sub>in</sub> = 0)		C <sub>in</sub>	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		I <sub>DD</sub>	5.0 10 15	_ _ _	5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiesce Per Package) (C <sub>L</sub> = 50 pF on all outp buffers switching)		lΤ	5.0 10 15			$I_T = (3$	.8 μΑ/kHz) f ε.7 μΑ/kHz) f ε.5 μΑ/kHz) f	+ I <sub>DD</sub>			μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.008.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25  $^{\circ}\text{C}.$ 

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

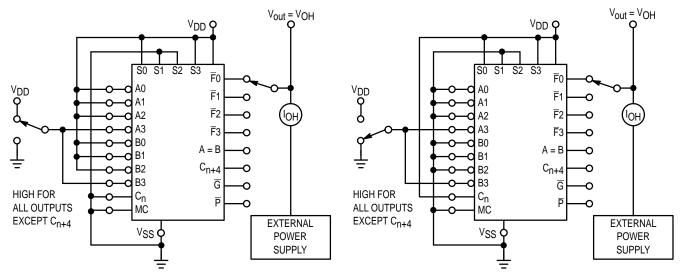
# **SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}C$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns $t_{TLH}$ , $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns $t_{TLH}$ , $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns	tTLH, tTHL	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Propagation Delay Time Sum in to Sum Out  tpLH, tpHL = (1.7 ns/pF) CL + 620 ns  tpLH, tpHL = (0.66 ns/pF) CL + 217 ns  tpLH, tpHL = (0.5 ns/pF) CL + 155 ns	tPLH, tPHL	5.0 10 15	_ _ _	705 250 180	1410 500 360	ns
Sum in to Sum Out (Logic Mode) $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 182 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$	tPLH, tPHL	5.0 10 15	_ _ _	605 215 180	1210 430 360	ns
Sum in to A = B $tp_{LH}$ , $tp_{HL} = (1.7 \text{ ns/pF}) C_L + 870 \text{ ns}$ $tp_{LH}$ , $tp_{HL} = (0.66 \text{ ns/pF}) C_L + 297 \text{ ns}$ $tp_{LH}$ , $tp_{HL} = (0.5 \text{ ns/pF}) C_L + 220 \text{ ns}$	tPLH, tPHL	5.0 10 15	_ _ _	955 330 245	1910 660 490	ns
Sum in to P or G $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 400 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$	tPLH, tPHL	5.0 10 15	_ _ _	485 180 130	970 360 260	ns
Sum in to $C_{n+4}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 530 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 187 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$	<sup>†</sup> PLH	5.0 10 15	_ _ _	615 220 160	1230 440 360	ns
Carry in to Sum Out  tpLH, tpHL = (1.7 ns/pF) CL + 295 ns  tpLH, tpHL = (0.66 ns/pF) CL + 112 ns  tpLH, tpHL = (0.5 ns/pF) CL + 80 ns	tPLH, tPHL	5.0 10 15	_ _ _	380 145 105	760 290 210	ns
Carry in to $C_{n+4}$ $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$	tPLH, tPHL	5.0 10 15		305 120 85	610 240 170	ns

## AC TEST SETUP REFERENCE TABLE

AO 1201 OETOT REFERENCE TABLE						
	AC P	aths	DC Data	a Inputs		Fig. 3
Test	Inputs	Outputs	To V <sub>SS</sub>	To V <sub>DD</sub>	Mode	Waveform
Sum <sub>in</sub> to Sum <sub>out</sub> Delay Time	Ā0	Any F	Remaining $\overline{A}$ 's $C_n$	All B's	Add	#1
Sum <sub>in</sub> to P Delay Time	Ā0	P	Remaining A's C <sub>n</sub>	All B's	Add	#1
Sum <sub>in</sub> to <del>G</del> Delay Time	B <sub>0</sub>	G	All Ā's C <sub>n</sub>	Remaining B's	Add	#1
Sum <sub>in</sub> to C <sub>n+4</sub> Delay Time	B <sub>0</sub>	C <sub>n+y</sub>	All Ā's C <sub>n</sub>	Remaining B's	Add	#2
C <sub>n</sub> to Sum <sub>out</sub> Delay Time	C <sub>n</sub>	Any F	All Ā's	All B's	Add	#1
C <sub>n</sub> to C <sub>n+4</sub> Delay Time	C <sub>n</sub>	C <sub>n+4</sub>	All Ā's	All B's	Add	#1
Sum <sub>in</sub> to A = B Delay Time	Ā0	A = B	All B's Remaining A's	C <sub>n</sub>	Sub	#2
Sum <sub>in</sub> to Sum <sub>out</sub> Delay Time (Logic Mode)	B̄ <sub>0</sub>	Any F	All A's	М	Exclusive OR	#2

<sup>\*</sup> The formulas given are for the typical characteristics only at 25°C. #Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



**Figure 1. Typical Source Current Test Circuit** 

Figure 2. Typical Sink Current Test Circuit

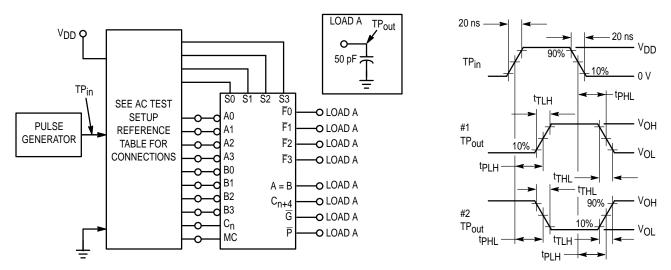


Figure 3. Switching Time Test Circuit and Waveforms

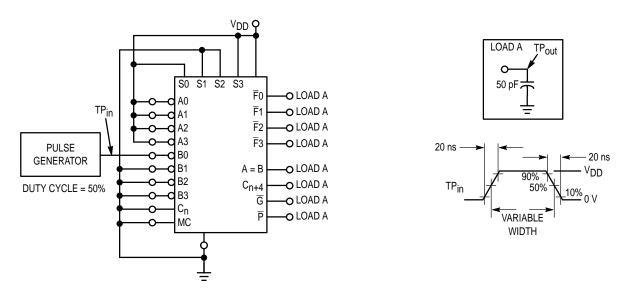


Figure 4. Dynamic Power Dissipation Test Circuit and Waveform

#### **BLOCK DIAGRAM BLOCK DIAGRAM** (ACTIVE LOW) (ACTIVE HIGH) 3 **o**-**FUNCTION SELECT INPUTS** V<sub>DD</sub> = PIN 24 V<sub>SS</sub> = PIN 12 S0 S1 S2 S3 S0 S1 S2 S3 F<sub>0</sub> F0 **-0** 9 **•** 9 Α1 23 **o**-WORD $\overline{A}$ F<sub>1</sub> OUTPUT F1 **-0** 10 A2 A2 21 **o**-**FUNCTION** F<sub>2</sub> F2 **o** 11 АЗ АЗ 19 **o**-F3 F3 **-o** 13 B0 B0 10-В1 22 **o**-WORD $\overline{\mathsf{B}}$ • 14 COMPARISON OUTPUT A = BB2 20 **o**-B2 • 16 RIPPLE CARRY OUTPUT $\overline{C}_{n+4}$ **-o** 16 ВЗ 18 **o**-ВЗ ) LOOK AHEAD **o** 17 $C_n$ $C_{\mathsf{n}}$ CARRY IN 7 O-7 **o**o 15 ∫ CARRY OUTPUTS Р **-o** 15 MODE CONTROL 8 o MC MC

#### **TRUTH TABLE**

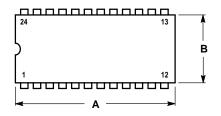
F	Function Select			Inputs/O	utputs Active Low	Inputs/Outputs Active High	
<b>S</b> 3	S2	S1	S0	Logic Function (MC = H)	Arithmetic* Function (MC = L, C <sub>n</sub> = L)	Logic Function (MC = H)	Arithmetic* Function (MC = L, $\overline{C}_n$ = H)
L	٦	L	L	Ā	A minus 1	Ā	Α
L	L	L	Н	ĀB	AB minus 1	A + B	A + B
L	L	Н	L	A + B	AB minus 1	ĀB	A + B
L	L	Н	Н	Logic "1"	minus 1	Logic "0"	minus 1
L	Н	L	L	A + B	A plus $(A + \overline{B})$	ĀB	A plus AB
L	Н	L	Н	B	AB plus $(A + \overline{B})$	В	(A + B) plus AB
L	Н	Н	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	Н	Н	Н	A + B	A + B	AB	AB minus 1
Н	L	L	L	ĀB	A plus (A + B)	Ā+B	A plus AB
Н	L	L	Н	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
Н	L	Н	L	В	AB plus (A + B)	В	(A + B) plus AB
Н	L	Н	Н	A + B	A + B	AB	AB minus 1
Н	Н	L	L	Logic "0"	A plus A	Logic "1"	A plus A
Н	Н	L	Н	AΒ	AB plus A	$A + \overline{B}$	(A + B) plus A
Н	Н	Н	L	AB	AB plus A	A + B	(A + B) plus A
Н	Н	Н	Н	Α	Α	Α	A minus 1

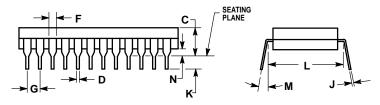
<sup>\*</sup> Expressed as two's complements. For arithmetic function with C<sub>n</sub> in the opposite state, the resulting function is as shown plus 1.

### **OUTLINE DIMENSIONS**

### **L SUFFIX**

CERAMIC DIP PACKAGE CASE 623-05 ISSUE M





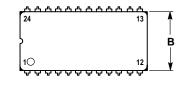
- NOTES:

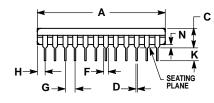
  1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED DAS ALL EL) PARALLEL).

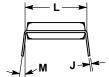
.,					
	MILLIN	METERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	31.24	32.77	1.230	1.290	
В	12.70	15.49	0.500	0.610	
С	4.06	5.59	0.160	0.220	
D	0.41	0.51	0.016	0.020	
F	1.27	1.52	0.050	0.060	
G	2.54	BSC	0.100	BSC	
J	0.20	0.30	0.008	0.012	
K	3.18	4.06	0.125	0.160	
L	15.24 BSC		0.600	BSC	
М	0 °	15°	0 °	15°	
N	0.51	1 27	0.020	0.050	

#### **P SUFFIX**

PLASTIC DIP PACKAGE CASE 709-02 **ISSUE C** 





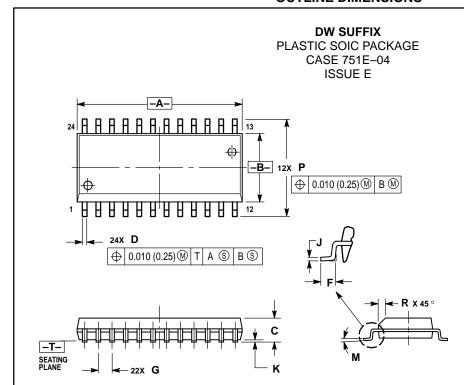


- OTES:

  1. POSITIONAL TOLERANCE OF LEADS (D),
  SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM
  MATERIAL CONDITION, IN RELATION TO
  SEATING PLANE AND EACH OTHER.
  2. DIMENSION L TO CENTER OF LEADS WHEN
  FORMED PARALLEL.
- 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	31.37	32.13	1.235	1.265
В	13.72	14.22	0.540	0.560
С	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
Н	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24	BSC	0.600	BSC
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

#### **OUTLINE DIMENSIONS**



#### NOTES

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS A AND B DO NOT INCLUDE
- MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION: ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN
  EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	15.25	15.54	0.601	0.612
В	7.40	7.60	0.292	0.299
С	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27	BSC	0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
М	0°	8°	0°	8°
Р	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Marare registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609 INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



