MC14099B
MC14599B

8-Bit Addressable Latches

The MC14099B and MC14599B are 8–bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/Read line controls this port in the MC14599B.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
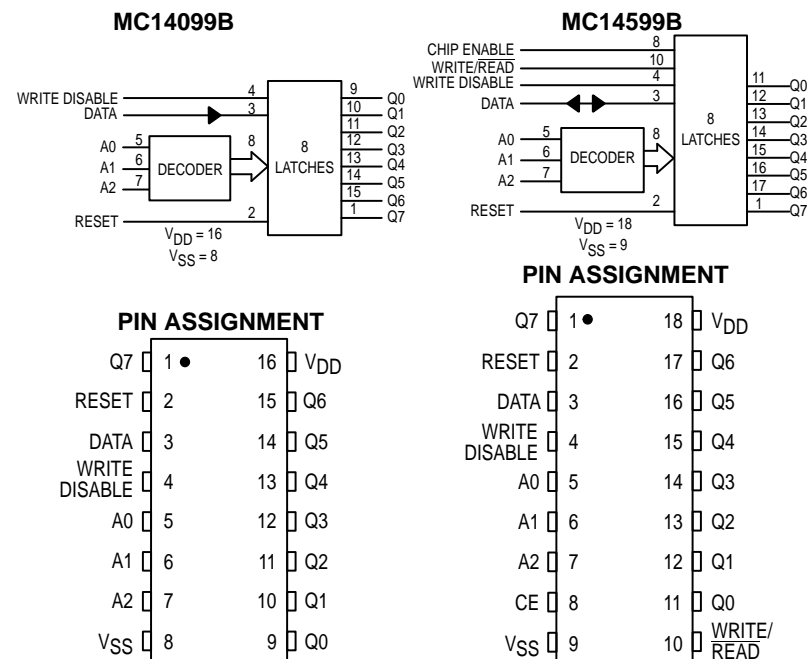
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

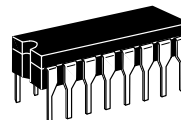* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
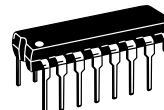   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
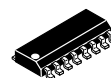   Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

MC14099B

MC14599B

PIN ASSIGNMENT

MC14099B:

Q7	1 ●	16	V_{DD}
RESET	2	15	Q6
DATA	3	14	Q5
WRITE DISABLE	4	13	Q4
A0	5	12	Q3
A1	6	11	Q2
A2	7	10	Q1
V_{SS}	8	9	Q0

PIN ASSIGNMENT

MC14599B:

Q7	1 ●	18	V_{DD}
RESET	2	17	Q6
DATA	3	16	Q5
WRITE DISABLE	4	15	Q4
A0	5	14	Q3
A1	6	13	Q2
A2	7	12	Q1
CE	8	11	Q0
V_{SS}	9	10	WRITE/READ

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14099BCP	Plastic
MC14099BCL	Ceramic
MC14099BDW	SOIC

T_A = − 55° to 125°C for all packages.
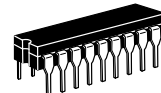
L SUFFIX
CERAMIC
CASE 726
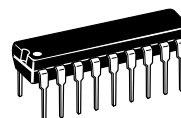
P SUFFIX
PLASTIC
CASE 707

ORDERING INFORMATION

MC14599BCP	Plastic
MC14599BCL	Ceramic

T_A = − 55° to 125°C for all packages.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, pre-cautions must be taken to avoid applications of any voltage higher than maximum rated volt-ages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

REV 0
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MOTOROLA

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0	− 3.0	—	− 2.4	− 4.2	—	− 1.7	—	mAdc
		5.0	− 0.64	—	− 0.51	− 0.88	—	− 0.36	—	
		10	− 1.6	—	− 1.3	− 2.25	—	− 0.9	—	
		15	− 4.2	—	− 3.4	− 8.8	—	− 2.4	—	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Input Capacitance MC14599B — Data (pin 3) (V_{in} = 0)	C_{in}	—	—	—	—	15	22.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0			I_T = (1.5 µA/kHz) f + I_{DD}					µAdc
		10			I_T = (3.0 µA/kHz) f + I_{DD}					
		15			I_T = (4.5 µA/kHz) f + I_{DD}					

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Data to Output Q	t_{PHL}, t_{PLH}	5.0 10 15	— — —	200 75 50	400 150 100	ns
Write Disable to Output Q		5.0 10 15	— — —	200 80 60	400 160 120	ns
Reset to Output Q		5.0 10 15	— — —	175 80 65	350 160 130	ns
CE to Output Q (MC14599B only)		5.0 10 15	— — —	225 100 75	450 200 150	ns
Propagation Delay Time, MC14599B only Chip Enable, Write/$\overline{\text{Read}}$ to Data	t_{PHL}, t_{PLH}	5.0 10 15	— — —	200 80 65	400 160 130	ns
Address to Data		5.0 10 15	— — —	200 90 75	400 180 150	ns
Pulse Widths Reset	$t_{w(H)}$ $t_{w(L)}$	5.0 10 15	150 75 50	75 40 25	— — —	ns
Write Disable		5.0 10 15	320 160 120	160 80 60	— — —	ns
Set Up Time Data to Write Disable	t_{su}	5.0 10 15	100 50 35	50 25 20	— — —	ns
Hold Time Write Disable to Data	t_h	5.0 10 15	150 75 50	75 40 25	— — —	ns
Set Up Time Address to Write Disable	t_{su}	5.0 10 15	100 80 40	45 30 10	— — —	ns
Removal Time Write Disable to Address	t_{rem}	5.0 10 15	0 0 0	– 80 – 40 – 40	— — —	ns

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
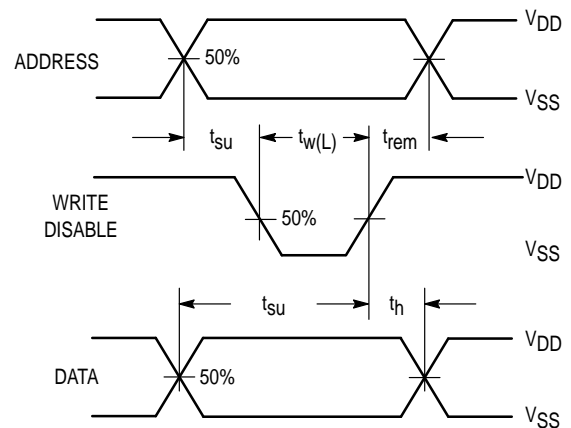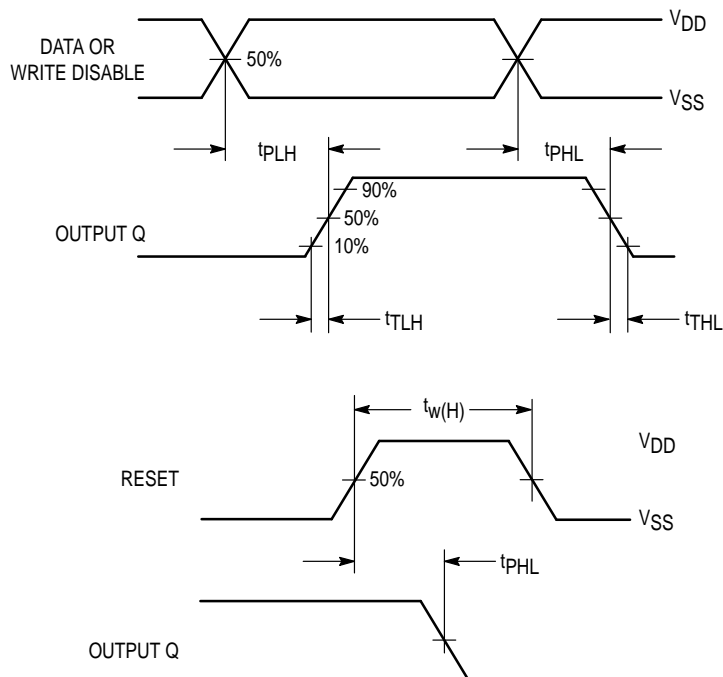
MC14099B
FUNCTION DIAGRAM
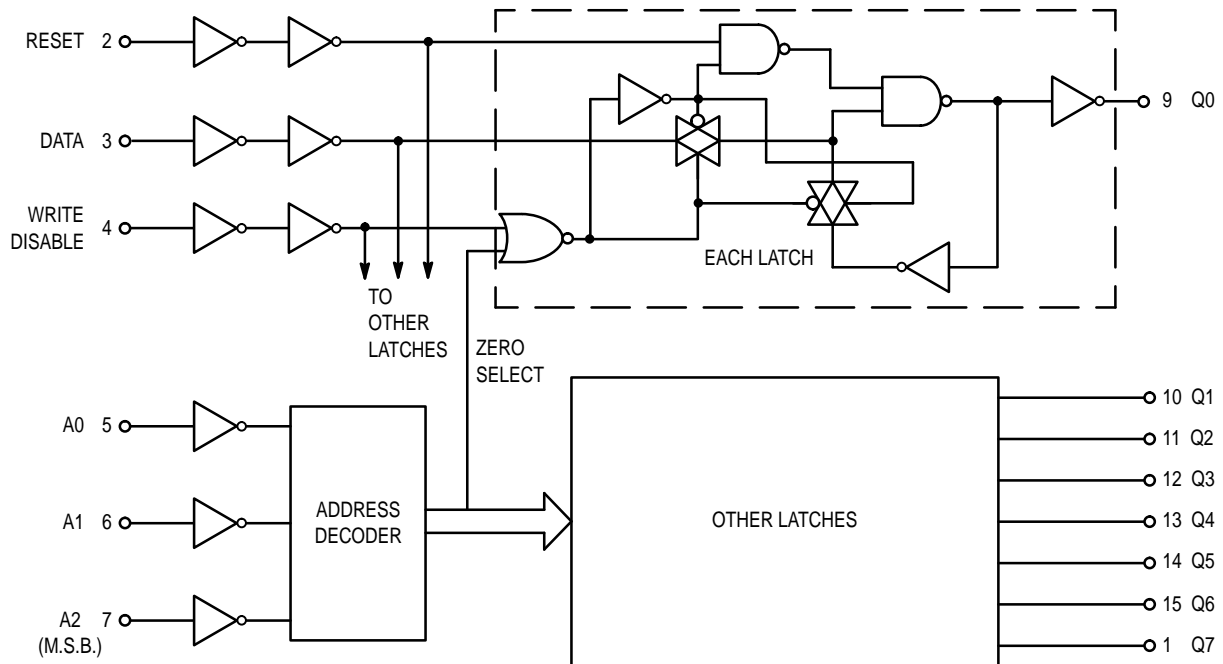
TRUTH TABLE

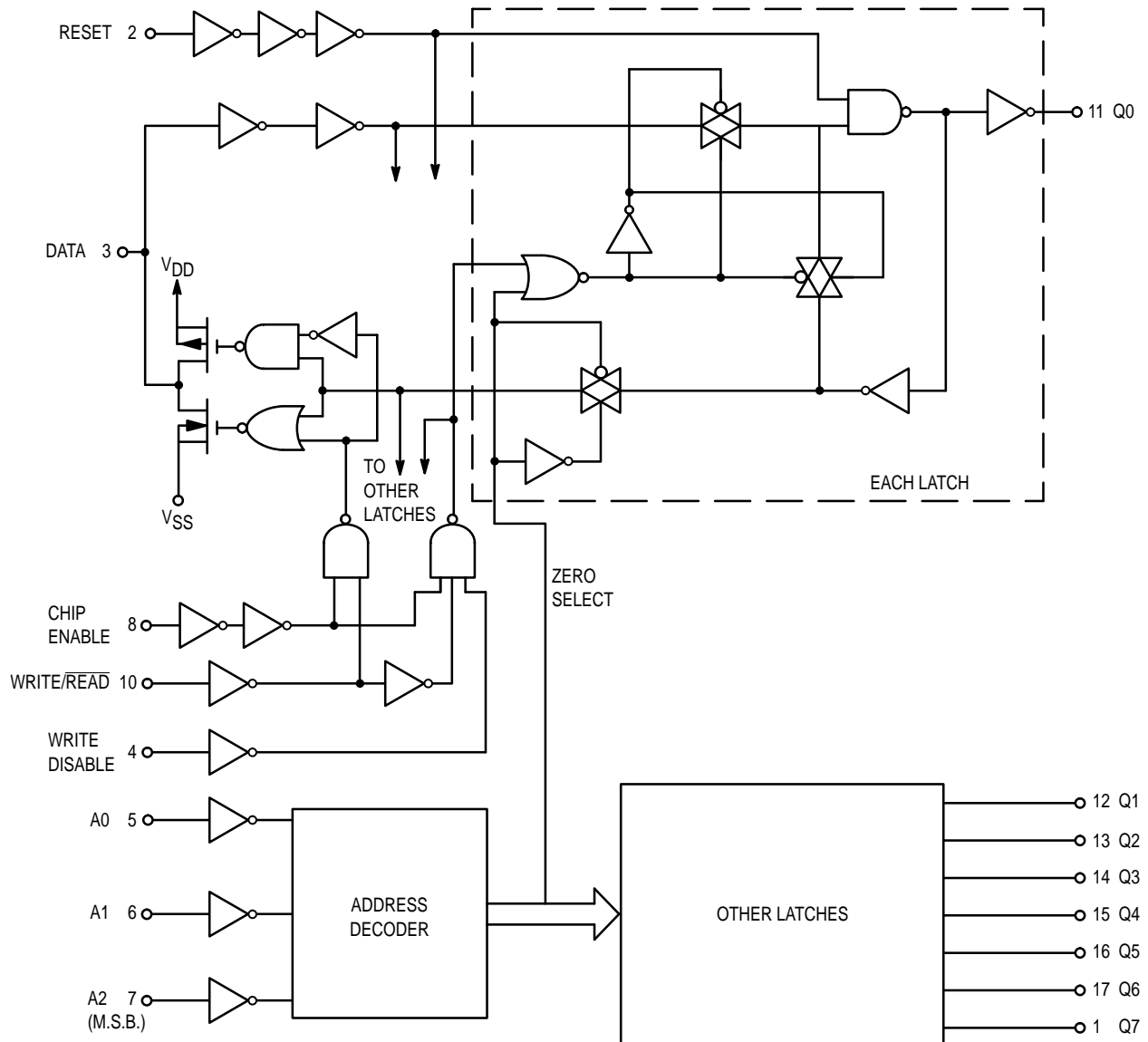| Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q_n*
0	1	Data	Reset†
1	0	Q_n*	Q_n*
1	1	Reset	Reset

* Q_n is previous state of latch.
†Reset to zero state.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

SWITCHING WAVEFORMS

MC14599B
FUNCTION DIAGRAM

RESET 2

Q0 11

DATA 3

V_{DD}

V_{SS}

TO OTHER LATCHES

EACH LATCH

ZERO SELECT

CHIP ENABLE 8

WRITE/$\overline{READ}$ 10

WRITE DISABLE 4

A0 5

A1 6

A2 7 (M.S.B.)

ADDRESS DECODER

OTHER LATCHES

12 Q1
13 Q2
14 Q3
15 Q4
16 Q5
17 Q6
1 Q7

TRUTH TABLE

Chip Enable	Write/$\overline{Read}$	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	X	X	0	*	*	Z
1	1	0	0	Data	*	Input
1	1	1	0	*	*	Z
1	0	X	0	*	*	Q_n
X	X	X	1	0	0	Z/0

X = Don't care.
* = No change in state of latch.
Z = High impedance.
Q_n = State of addressed latch.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

MC14599B
SWITCHING WAVEFORMS

DATA WRITE
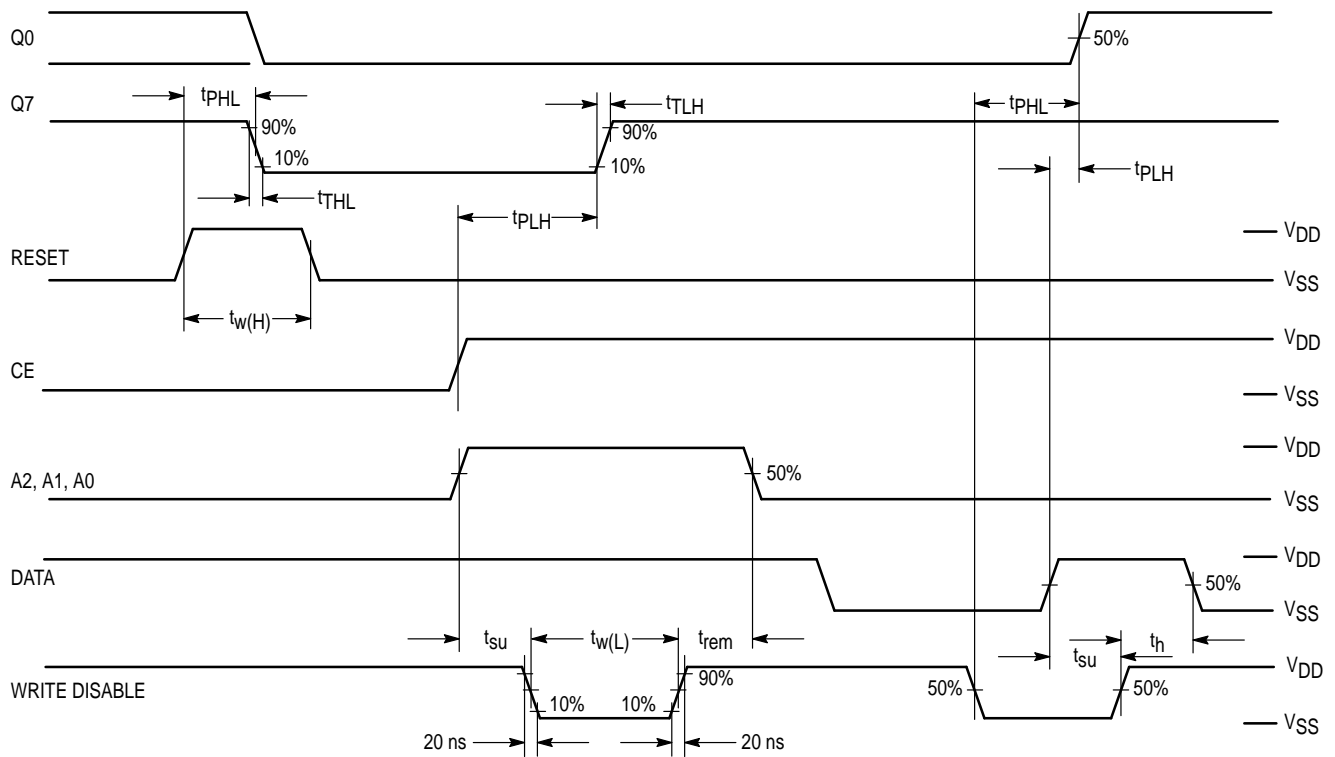
DATA READ
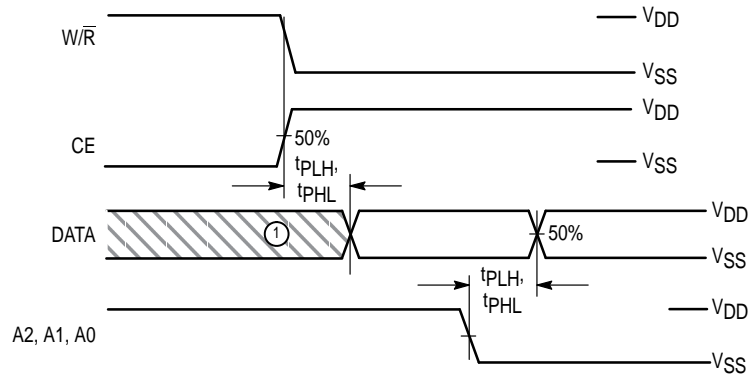
NOTE: 1. Invalid Data Output
2. Reset in LOW State

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V
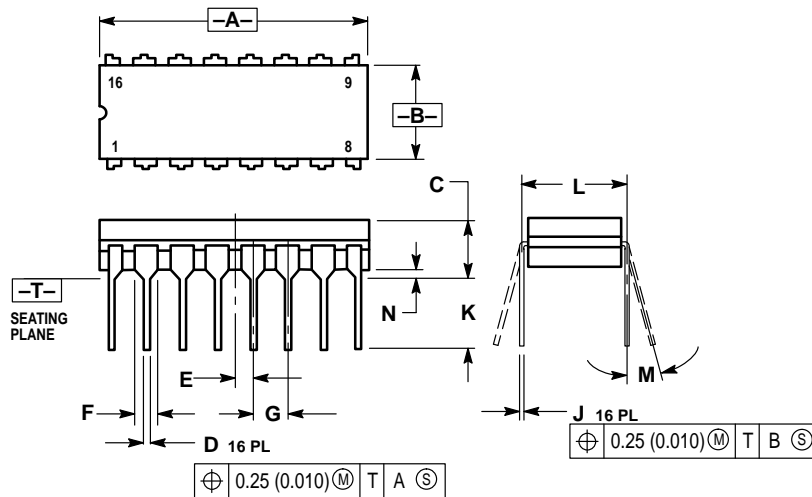
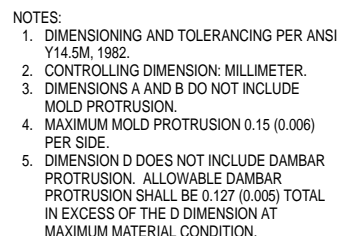NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

⊕ 0.25 (0.010) Ⓜ T B Ⓢ

⊕ 0.25 (0.010) Ⓜ T A Ⓢ

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R
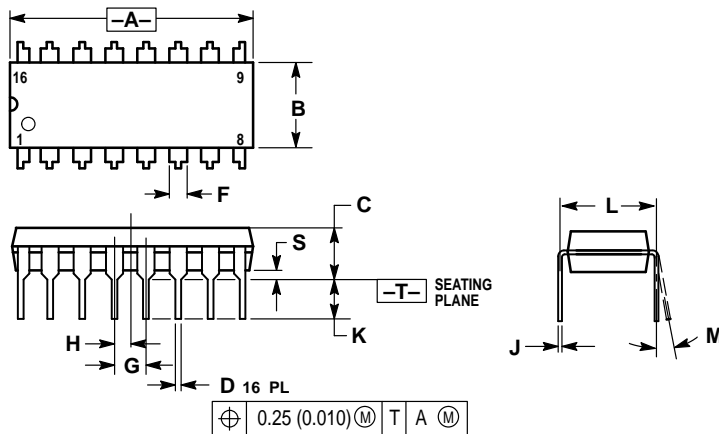
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

⊕ 0.25 (0.010) Ⓜ T A Ⓜ

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

L SUFFIX
CERAMIC DIP PACKAGE
CASE 726–04
ISSUE G

OPTIONAL LEAD
CONFIGURATION (1, 9, 10, 18)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

P SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C
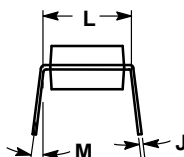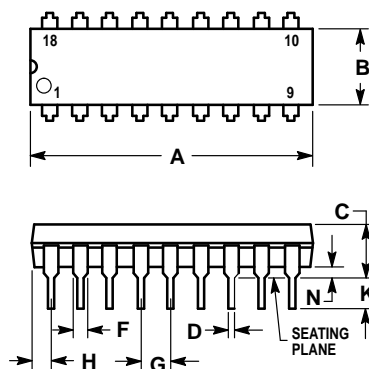
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0 °	15°	0 °	15°
N	0.51	1.02	0.020	0.040

MOTOROLA

◊

MC14099B/D