

# MC14581B

## 4-Bit Arithmetic Logic Unit

The MC14581B is a CMOS 4-bit ALU capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 14-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ( $\bar{P}$ ) and carry generate ( $\bar{G}$ ) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input ( $C_n$ ) and a ripple carry output ( $C_{n+4}$ ) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the  $\bar{A}$  and  $\bar{B}$  inputs is provided using the  $A = B$  output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the  $C_{n+4}$  output can be used to indicate relative magnitude as shown in this table:

Data Level	$C_n$	$C_{n+4}$	Magnitude
Active High	H	H	$A \leq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geq B$
Active Low	L	L	$A \leq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geq B$

- Functional and Pinout Equivalent to 74181.
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to $V_{SS}$ )

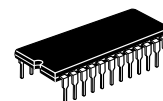
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient), per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

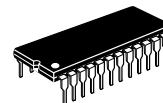
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



**L SUFFIX**  
CERAMIC  
CASE 623



**P SUFFIX**  
PLASTIC  
CASE 709



**DW SUFFIX**  
SOIC  
CASE 751E

### ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.

### PIN ASSIGNMENT

$\bar{B}0$	1	24	$V_{DD}$
$\bar{A}0$	2	23	$\bar{A}1$
S3	3	22	$\bar{B}1$
S2	4	21	$\bar{A}2$
S1	5	20	$\bar{B}2$
S0	6	19	$\bar{A}3$
$C_n$	7	18	$\bar{B}3$
MC	8	17	$\bar{G}$
$\bar{F}0$	9	16	$C_{n+4}$
$\bar{F}1$	10	15	$\bar{P}$
$\bar{F}2$	11	14	$A = B$
$V_{SS}$	12	13	$\bar{F}3$

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

[illegible]

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_I) = I_T(50 \text{ pF}) + (C_I - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_I$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.008$ .

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Sum in to Sum Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	705 250 180	1410 500 360	ns
Sum in to Sum Out (Logic Mode) $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 182 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 155 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	605 215 180	1210 430 360	ns
Sum in to A = B $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 870 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 297 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 220 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	955 330 245	1910 660 490	ns
Sum in to P or G $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 400 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	485 180 130	970 360 260	ns
Sum in to $C_{n+4}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 530 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 187 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 135 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	615 220 160	1230 440 360	ns
Carry in to Sum Out $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 295 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 112 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 80 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	380 145 105	760 290 210	ns
Carry in to $C_{n+4}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 220 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 60 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	305 120 85	610 240 170	ns

\* The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**AC TEST SETUP REFERENCE TABLE**

Test	AC Paths		DC Data Inputs		Mode	Fig. 3 Waveform
	Inputs	Outputs	To V <sub>SS</sub>	To V <sub>DD</sub>		
Sum <sub>in</sub> to Sum <sub>out</sub> Delay Time	$\bar{A}0$	Any $\bar{F}$	Remaining $\bar{A}$ 's $C_n$	All $\bar{B}$ 's	Add	#1
Sum <sub>in</sub> to $\bar{P}$ Delay Time	$\bar{A}0$	$\bar{P}$	Remaining $\bar{A}$ 's $C_n$	All $\bar{B}$ 's	Add	#1
Sum <sub>in</sub> to $\bar{G}$ Delay Time	$\bar{B}0$	$\bar{G}$	All $\bar{A}$ 's $C_n$	Remaining $\bar{B}$ 's	Add	#1
Sum <sub>in</sub> to $C_{n+4}$ Delay Time	$\bar{B}0$	$C_{n+y}$	All $\bar{A}$ 's $C_n$	Remaining $\bar{B}$ 's	Add	#2
$C_n$ to Sum <sub>out</sub> Delay Time	$C_n$	Any $\bar{F}$	All $\bar{A}$ 's	All $\bar{B}$ 's	Add	#1
$C_n$ to $C_{n+4}$ Delay Time	$C_n$	$C_{n+4}$	All $\bar{A}$ 's	All $\bar{B}$ 's	Add	#1
Sum <sub>in</sub> to A = B Delay Time	$\bar{A}0$	A = B	All $\bar{B}$ 's Remaining $\bar{A}$ 's	$C_n$	Sub	#2
Sum <sub>in</sub> to Sum <sub>out</sub> Delay Time (Logic Mode)	$\bar{B}0$	Any $\bar{F}$	All A's	M	Exclusive OR	#2

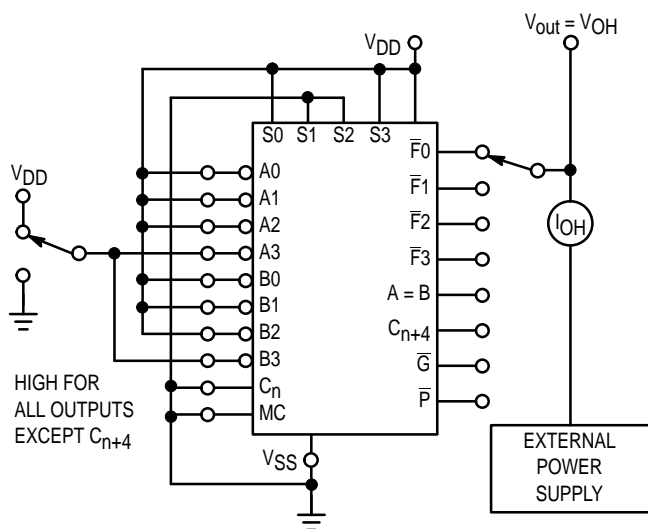


Figure 1. Typical Source Current Test Circuit

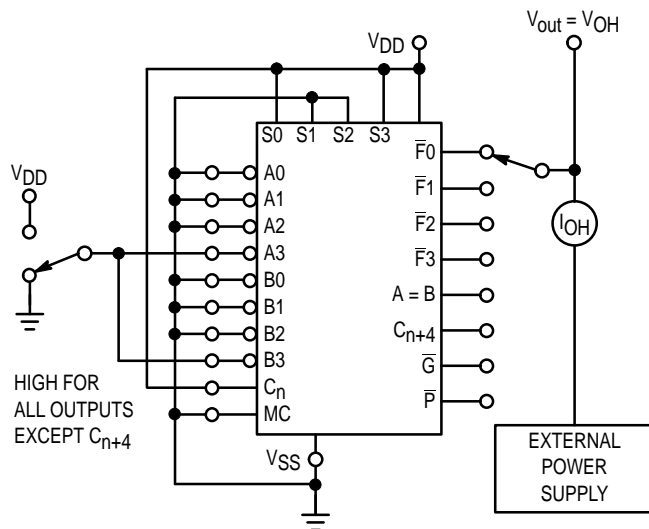


Figure 2. Typical Sink Current Test Circuit

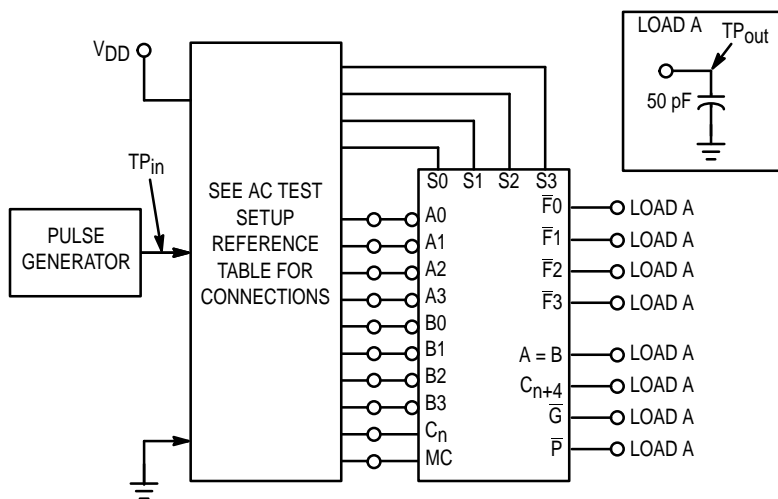


Figure 3. Switching Time Test Circuit and Waveforms

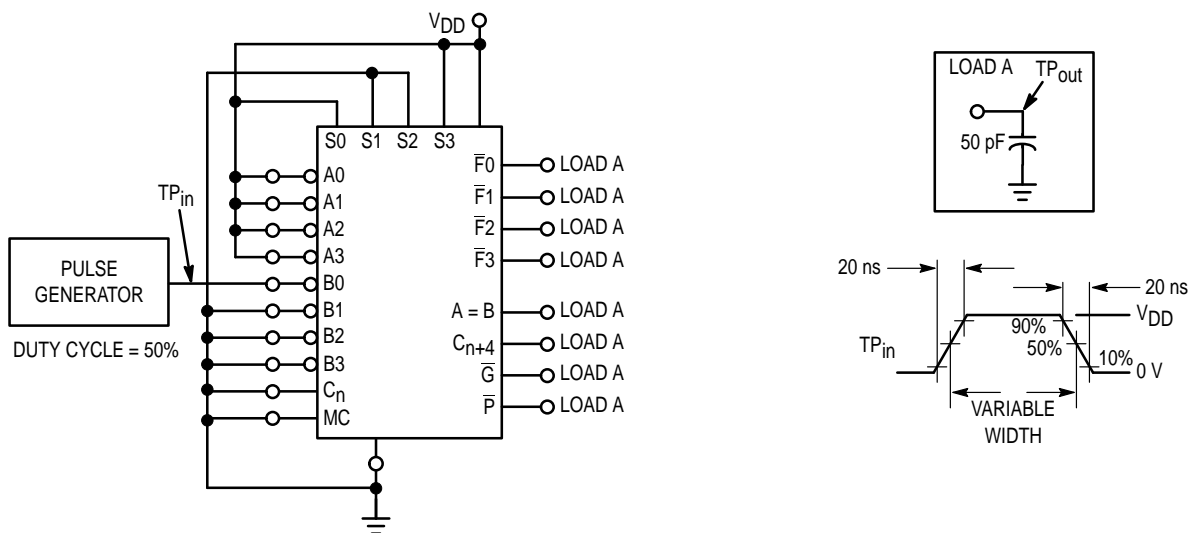
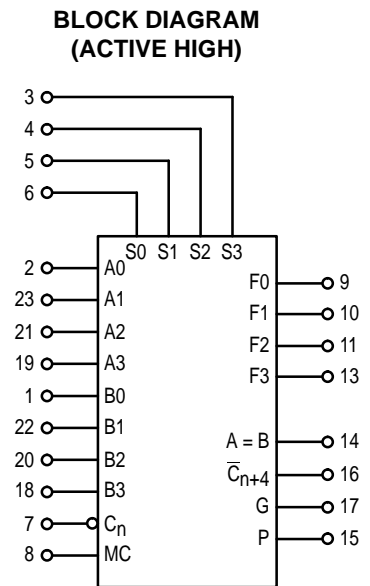
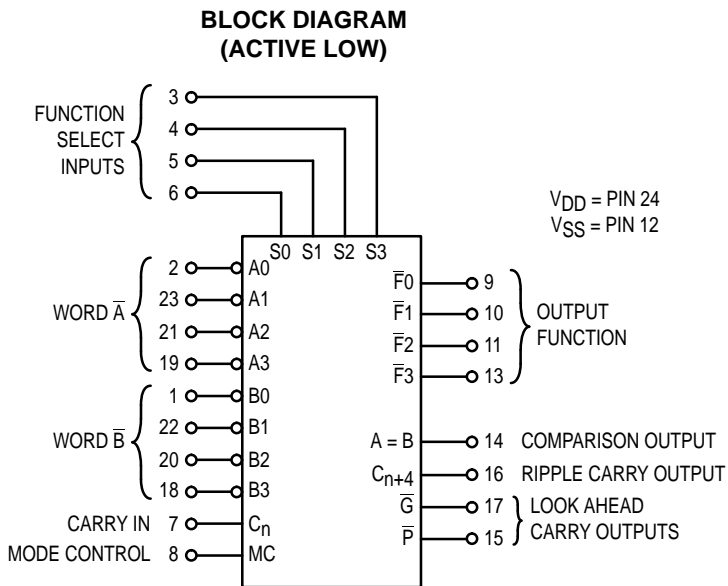


Figure 4. Dynamic Power Dissipation Test Circuit and Waveform



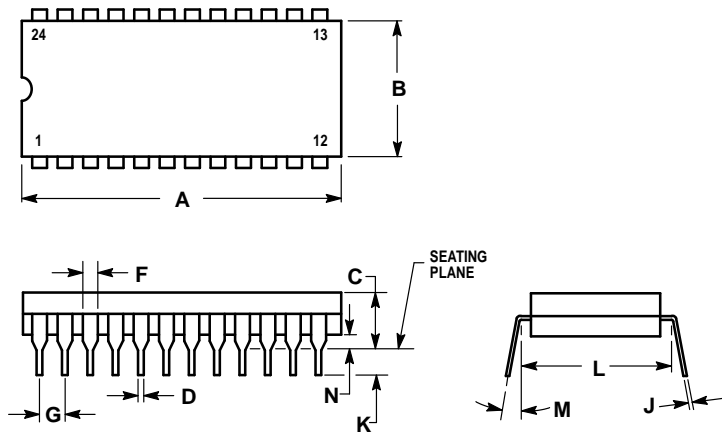
**TRUTH TABLE**

Function Select				Inputs/Outputs Active Low		Inputs/Outputs Active High	
S3	S2	S1	S0	Logic Function (MC = H)	Arithmetic* Function (MC = L, $C_n$ = L)	Logic Function (MC = H)	Arithmetic* Function (MC = L, $C_n$ = H)
L	L	L	L	$\bar{A}$	A minus 1	$\bar{A}$	A
L	L	L	H	$\bar{A}\bar{B}$	AB minus 1	$\bar{A} + \bar{B}$	A + B
L	L	H	L	$\bar{A} + B$	$A\bar{B}$ minus 1	$\bar{A}\bar{B}$	A + $\bar{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\bar{A} + \bar{B}$	A plus (A + $\bar{B}$ )	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$
L	H	L	H	$\bar{B}$	AB plus (A + $\bar{B}$ )	B	(A + B) plus $\bar{A}\bar{B}$
L	H	H	L	$\bar{A} \oplus \bar{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	A + $\bar{B}$	A + $\bar{B}$	$\bar{A}\bar{B}$	$\bar{A}\bar{B}$ minus 1
H	L	L	L	$\bar{A}\bar{B}$	A plus (A + B)	$\bar{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\bar{A} \oplus \bar{B}$	A plus B
H	L	H	L	B	$\bar{A}\bar{B}$ plus (A + B)	B	(A + $\bar{B}$ ) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	$\bar{A}\bar{B}$	AB plus A	A + $\bar{B}$	(A + B) plus A
H	H	H	L	AB	$\bar{A}\bar{B}$ plus A	A + B	(A + $\bar{B}$ ) plus A
H	H	H	H	A	A	A	A minus 1

\* Expressed as two's complements. For arithmetic function with  $C_n$  in the opposite state, the resulting function is as shown plus 1.

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 623-05 ISSUE M

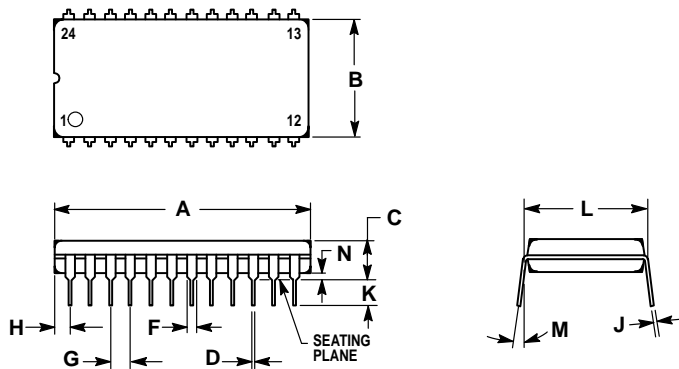


#### NOTES:

1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

### P SUFFIX PLASTIC DIP PACKAGE CASE 709-02 ISSUE C



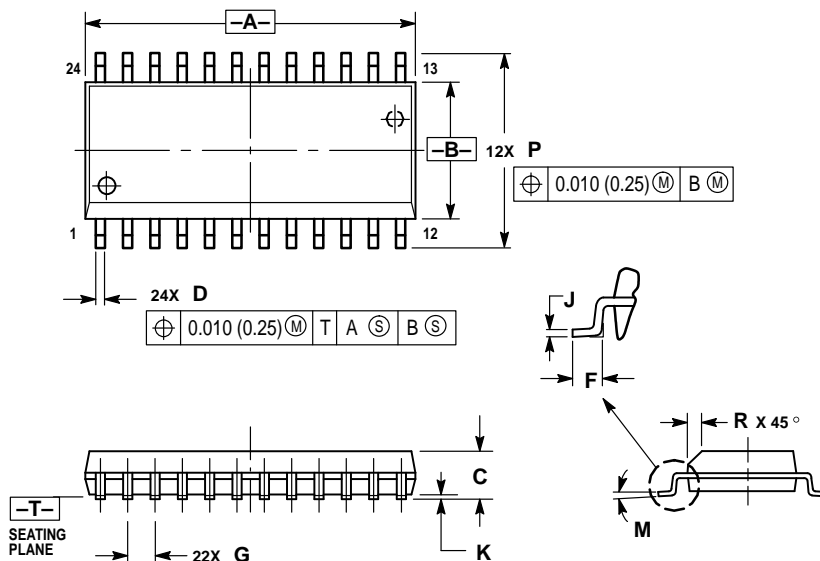
#### NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

## OUTLINE DIMENSIONS

### DW SUFFIX PLASTIC SOIC PACKAGE CASE 751E-04 ISSUE E



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC	0.050 BSC		
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

**MFAX:** RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609  
**INTERNET:** <http://Design-NET.com>

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,  
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MC14581B/D

