

## MC145152-2

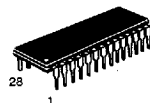
### Parallel-Input PLL Frequency Synthesizer

#### Interfaces with Dual-Modulus Prescalers

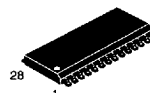
The MC145152-2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, two-output phase detector, 10-bit programmable divide-by-N counter, and 6-bit programmable +A counter.

The MC145152-2 is an improved-performance drop-in replacement for the MC145152-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Operating Temperature Range: -40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable +R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- +N Range = 3 to 1023, +A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates
- See Application Note AN980



**P SUFFIX**  
PLASTIC DIP  
CASE 710



**DW SUFFIX**  
SOG PACKAGE  
CASE 751F

#### ORDERING INFORMATION

|             |             |
|-------------|-------------|
| MC145152P2  | Plastic DIP |
| MC145152DW2 | SOG Package |

#### PIN ASSIGNMENT

|          |    |    |                    |
|----------|----|----|--------------------|
| $f_{in}$ | 1  | 28 | LD                 |
| VSS      | 2  | 27 | OSC <sub>in</sub>  |
| VDD      | 3  | 26 | OSC <sub>out</sub> |
| RA0      | 4  | 25 | A4                 |
| RA1      | 5  | 24 | A3                 |
| RA2      | 6  | 23 | A0                 |
| $\phi_R$ | 7  | 22 | A2                 |
| $\phi_V$ | 8  | 21 | A1                 |
| MC       | 9  | 20 | N9                 |
| A5       | 10 | 19 | N8                 |
| N0       | 11 | 18 | N7                 |
| N1       | 12 | 17 | N6                 |
| N2       | 13 | 16 | N5                 |
| N3       | 14 | 15 | N4                 |

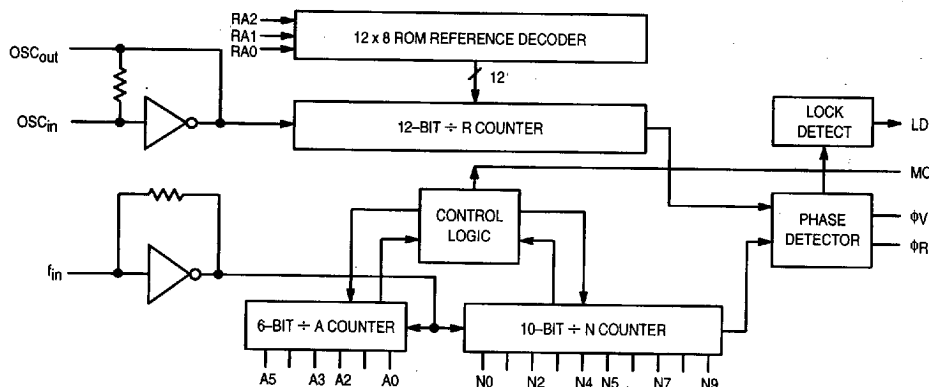
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# MC145152-2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull-up resistors that are not shown.

## PIN DESCRIPTIONS

### INPUT PINS

#### $f_{in}$ Frequency Input (Pin 1)

Input to the positive edge triggered  $\div N$  and  $\div A$  counters.  $f_{in}$  is typically derived from a dual-modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

#### RA0, RA1, RA2

#### Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

| Reference Address Code |     |     | Total Divide Value |
|------------------------|-----|-----|--------------------|
| RA2                    | RA1 | RA0 |                    |
| 0                      | 0   | 0   | 8                  |
| 0                      | 0   | 1   | 64                 |
| 0                      | 1   | 0   | 128                |
| 0                      | 1   | 1   | 256                |
| 1                      | 0   | 0   | 512                |
| 1                      | 0   | 1   | 1024               |
| 1                      | 1   | 0   | 1160               |
| 1                      | 1   | 1   | 2048               |

#### N0 – N9

#### N Counter Programming Inputs (Pins 11 – 20)

The N inputs provide the data that is preset into the  $\div N$  counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull-up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

#### A0 – A5

#### A Counter Programming Inputs (Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of  $f_{in}$  that require a logic 0 on the MC output (see **Dual-Modulus**

**Prescaling** section). The A inputs all have internal pull-up resistors that ensure that inputs left open will remain at a logic 1.

#### OSCin, OSCout Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSCin to ground and OSCout to ground. OSCin may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSCin, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSCout.

### OUTPUT PINS

#### ΦR, ΦV

#### Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop-error signal.

If the frequency  $f_V$  is greater than  $f_R$  or if the phase of  $f_V$  is leading, then error information is provided by  $\Phi_V$  pulsing low.  $\Phi_R$  remains essentially high.

If the frequency  $f_V$  is less than  $f_R$  or if the phase of  $f_V$  is lagging, then error information is provided by  $\Phi_R$  pulsing low.  $\Phi_V$  remains essentially high.

If the frequency of  $f_V = f_R$  and both are in phase, then both  $\Phi_V$  and  $\Phi_R$  remain high except for a small minimum time period when both pulse low in phase.

#### MC

#### Dual-Modulus Prescale Control Output (Pin 9)

Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the  $\div A$  counter has counted down from its programmed value. At this time, MC goes high and remains high until the  $\div N$  counter has counted the rest of the way down from its programmed value ( $N - A$  additional counts since both  $\div N$  and  $\div A$  are counting down during the first

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value  $(N_T) = N \cdot P + A$  where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

#### LD Lock Detector Output (Pin 28)

Essentially a high level when loop is locked ( $f_R$ ,  $f_V$  of same phase and frequency). Pulses low when loop is out of lock.

#### POWER SUPPLY

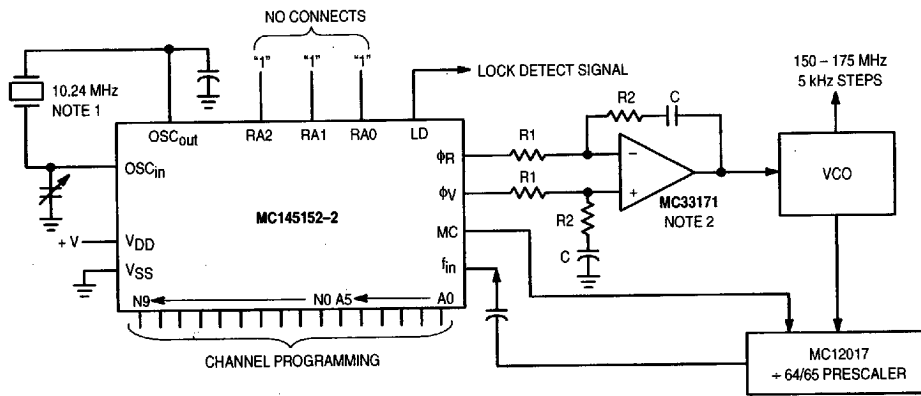
##### VDD Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to VSS.

##### VSS Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

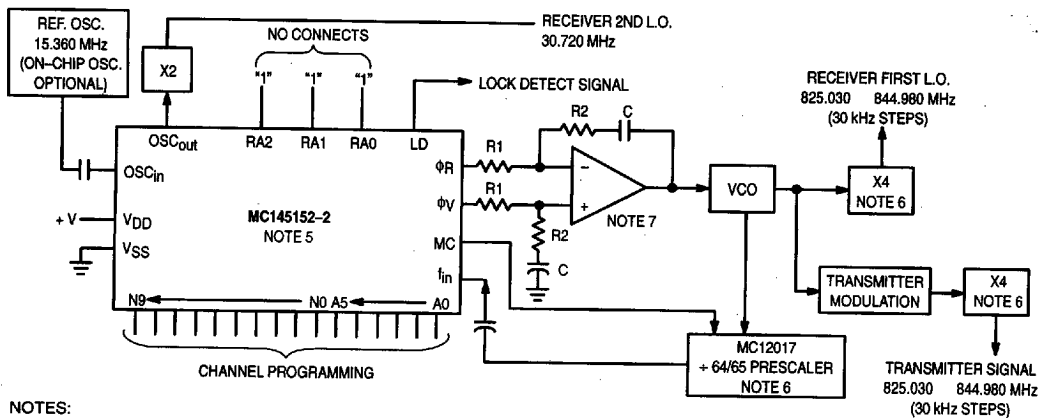
#### TYPICAL APPLICATIONS



#### NOTES:

1. Off-chip oscillator optional.
2. The  $\phi_R$  and  $\phi_V$  outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The  $\phi_R$  and  $\phi_V$  outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

Figure 1. Synthesizer for Land Mobile Radio VHF Bands



#### NOTES:

1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45 MHz receiver/transmit separation.
3.  $f_R = 7.5 \text{ kHz}$ ;  $\div R = 2048$ .
4.  $N_{\text{total}} = N \cdot 64 + A = 27501 \text{ to } 28166$ ;  $N = 429 \text{ to } 440$ ;  $A = 0 \text{ to } 63$ .
5. MC145158-2 may be used where serial data entry is desired.
6. High frequency prescalers (e.g., MC12018 [520 MHz] and MC12022 [1 GHz]) may be used for higher frequency VCO and  $f_{\text{ref}}$  implementations.
7. The  $\phi_R$  and  $\phi_V$  outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The  $\phi_R$  and  $\phi_V$  outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

**Figure 2. 666—Channel, Computer-Controlled, Mobile Radiotelephone Synthesizer for 800 MHz Cellular Radio Systems**

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