

Dual 4-Channel Analog Data Selector

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	− 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

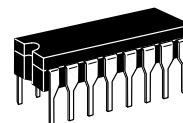
TRUTH TABLE (X = Don't Care)

ST _X	ST _Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X		High Impedance	

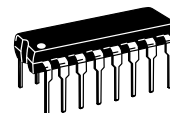
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

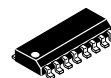
MC14529B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



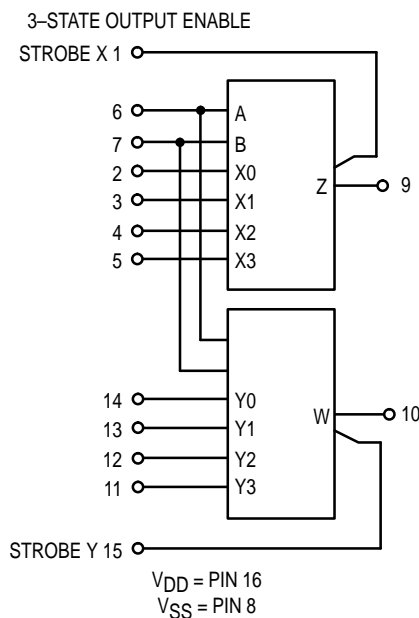
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = − 55° to 125°C for all packages.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})

Power Supply Voltage Range	V _{DD}	—	V _{DD} – 3.0 ≥ V _{SS} ≥ V _{EE}	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0 10 15	Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV**	— — —	1.0 1.0 2.0	— — —	0.005 0.010 0.015	1.0 1.0 2.0	— — —	60 60 120	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} – V _{out})/R _{on} , is not included.)	Typical						(0.07 μA/kHz) f + I _{DD} (0.20 μA/kHz) f + I _{DD} (0.36 μA/kHz) f + I _{DD}	μA

CONTROL INPUTS — INHIBIT, A, B (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V _{IH}	5.0 10 15	R _{on} = per spec, I _{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN/OUT AND COMMONS OUT/IN — W, Z (Voltages Referenced to V_{EE})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R _{on}	10 15	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	— —	400 240	— —	120 80	480 270	— —	560 350	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	10 15		— —	— —	— —	15 10	— —	— —	— —	Ω
Off-Channel Leakage Current (Figure 10)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel		± 100	—	± 0.05	± 100	—	± 1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Inhibit = V _{DD}	—	—	—	8.0	—	—	—	pF
Capacitance, Common O/I	C _{O/I}	—	Inhibit = V _{DD}	—	—	—	20	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

#Data labelled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

** For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Characteristic	Figure	Symbol	V _{SS}	V _{DD}	Min	Typ #	Max	Unit
V _{in} to V _{out} Propagation Delay Time (C _L = 50 pF, R _L = 1.0 kΩ)	7	t _{PLH} , t _{PHL}	0.0	5.0 10 15	— — —	20 10 8.0	40 20 15	ns
Propagation Delay Time, Control to Output, V _{in} = V _{DD} or V _{SS} (C _L = 50 pF, R _L = 1.0 kΩ)	8	t _{PLZ} , t _{PZL} , t _{PHZ} , t _{PZH}	0.0	5.0 10 15	— — —	140 70 50	400 160 120	ns
Crosstalk, Control to Output (C _L = 50 pF, R _L = 1.0 kΩ R _{out} = 10 kΩ)	9	—	0.0	5.0 10 15	— — —	5.0 5.0 5.0	— — —	mV
Control Input Pulse Frequency (C _L = 50 pF, R _L = 1.0 kΩ)	10	f _{in}	0.0	5.0 10 15	— — —	5.0 10 12	2.5 6.2 8.3	MHz
Noise Voltage (f = 100 Hz)	11, 12	—	0.0	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	nV/ √cycle
Sine Wave Distortion (V _{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R _L = 10 kΩ, f = 1.0 kHz)	—	—	– 5.0	5.0	—	0.36	—	%
Off-Channel Leakage Current (V _{in} = + 5.0 Vdc, V _{out} = – 5.0 Vdc) (V _{in} = – 5.0 Vdc, V _{out} = + 5.0 Vdc) (V _{in} = + 7.5 Vdc, V _{out} = – 7.5 Vdc) (V _{in} = – 7.5 Vdc, V _{out} = + 7.5 Vdc)	—	I _{off}	– 5.0 – 5.0 – 7.5 – 7.5	5.0 5.0 7.5 7.5	— — — —	± 0.001 ± 0.001 ± 0.0015 ± 0.0015	± 125 ± 125 ± 250 ± 250	nA
Insertion Loss (V _{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz) I _{loss} = 20 Log ₁₀ (V _{out} /V _{in}) (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	13	—	– 5.0	5.0	— — — —	2.0 0.8 0.25 0.01	— — — —	dB
Bandwidth (– 3 dB) (V _{in} = 1.77 Vdc RMS centered @ 0.0 Vdc) (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	—	BW	– 5.0	5.0	— — — —	35 28 27 26	— — — —	MHz
Feedthrough and Crosstalk 20 Log ₁₀ (V _{out} /V _{in}) = – 50 dB (R _L = 1.0 kΩ) (R _L = 10 kΩ) (R _L = 100 kΩ) (R _L = 1.0 MΩ)	—	—	– 5.0	5.0	— — — —	850 100 12 1.5	— — — —	MHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

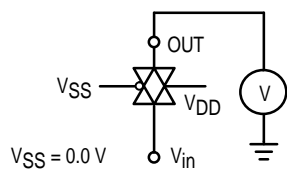
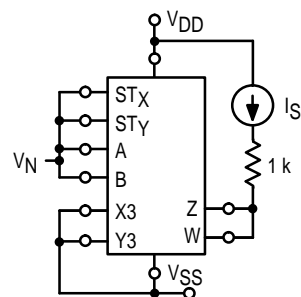


Figure 1. Output Voltage Test Circuit



Pins 2, 3, 4, 12, 13 and 14 are left open.

V_{IL} : V_C is raised from V_{SS} until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10 \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$
 $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH} : When $V_C = V_{IH}$ to V_{DD} , the switch is ON and the R_{ON} specifications are met.

Figure 2. Noise Immunity Test Circuit

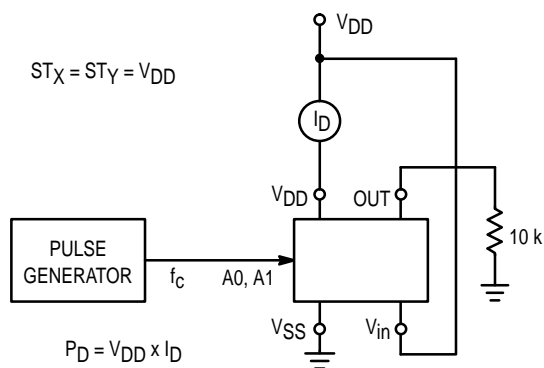


Figure 3. Quiescent Power Dissipation Test Circuit

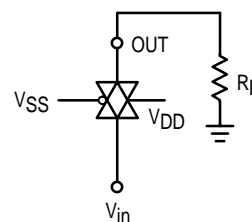


Figure 4. R_{ON} Characteristics Test Circuit

TYPICAL R_{ON} versus INPUT VOLTAGE

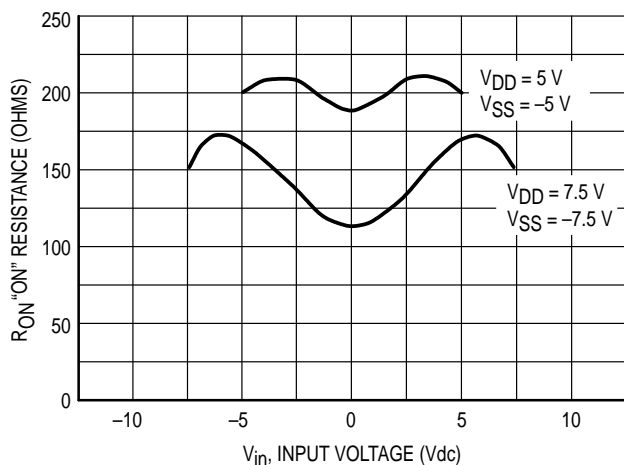


Figure 5.

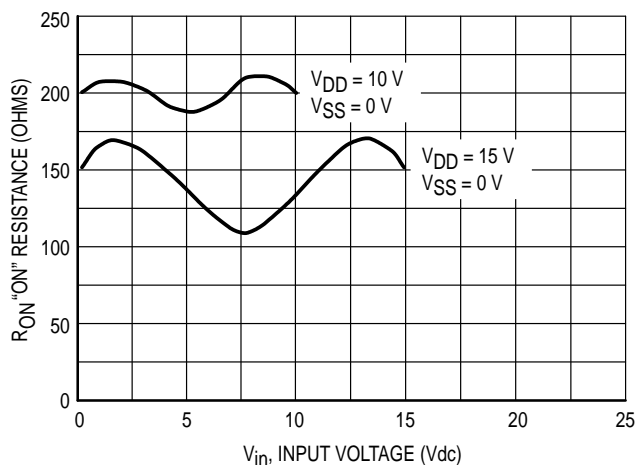


Figure 6.

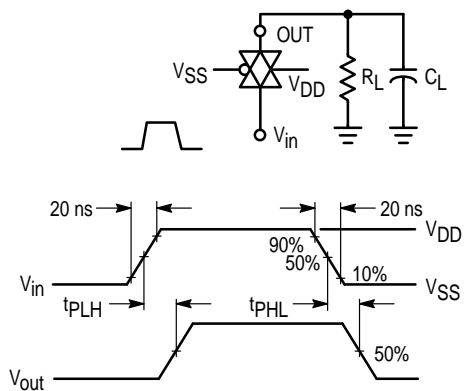


Figure 7. Propagation Delay Test Circuit and Waveforms

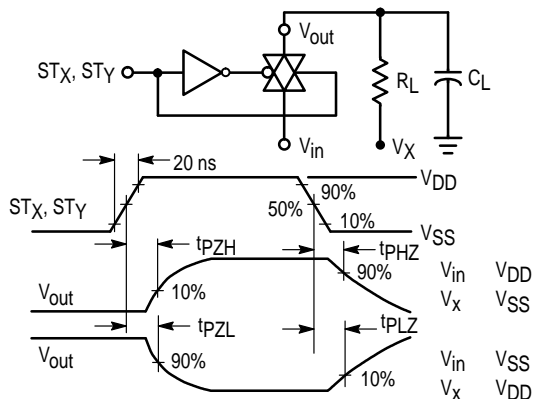


Figure 8. Turn-On Delay Time Test Circuit and Waveforms

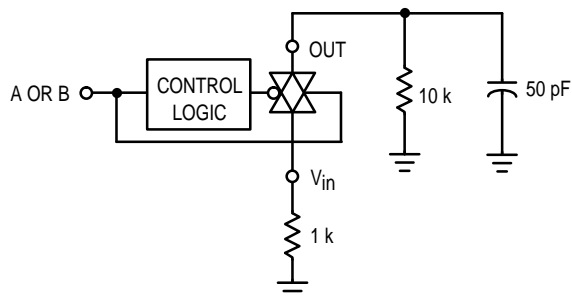


Figure 9. Crosstalk Test Circuit

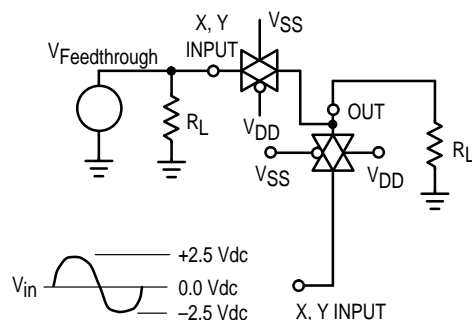


Figure 10. Frequency Response Test Circuit

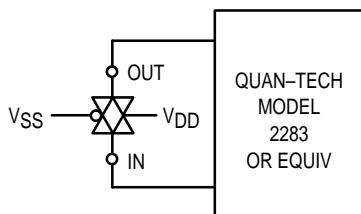


Figure 11. Noise Voltage Test Circuit

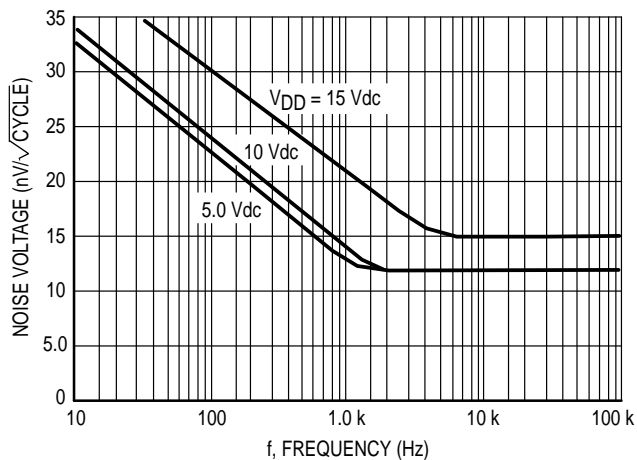


Figure 12. Typical Noise Characteristics

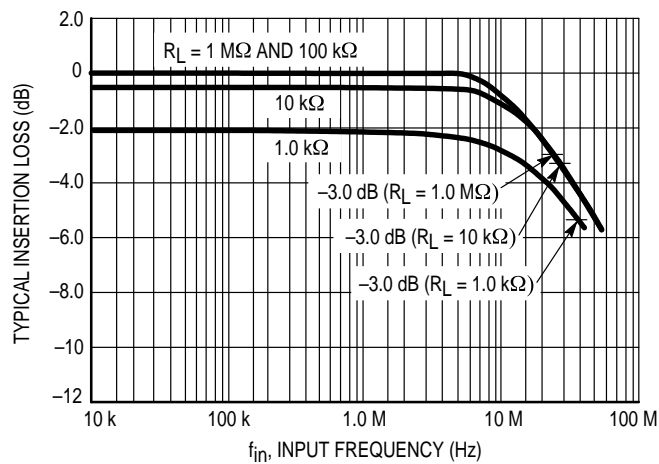
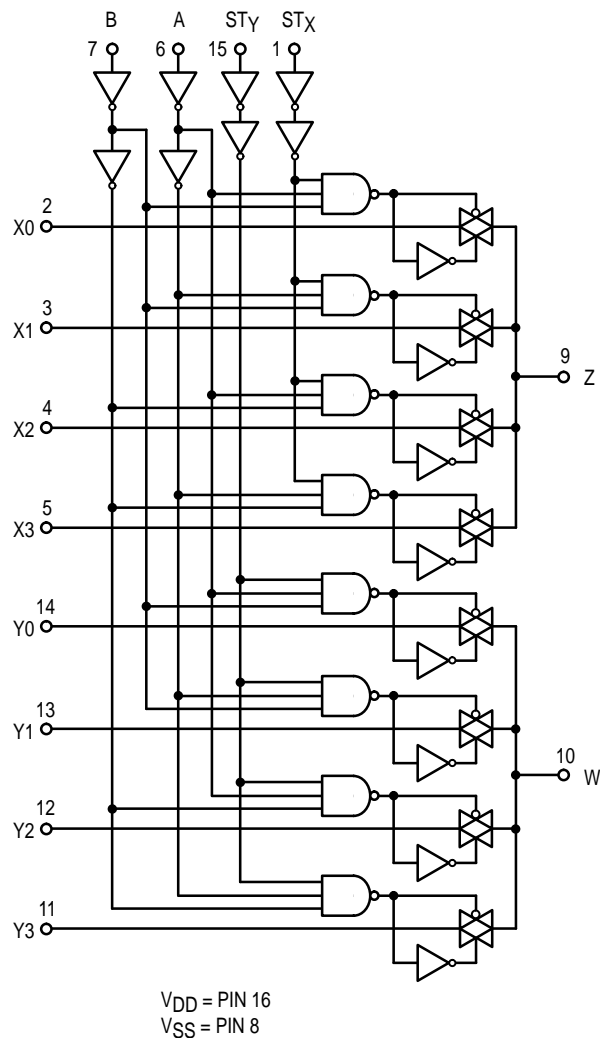


Figure 13. Typical Insertion Loss/Bandwidth Characteristics

PIN ASSIGNMENT

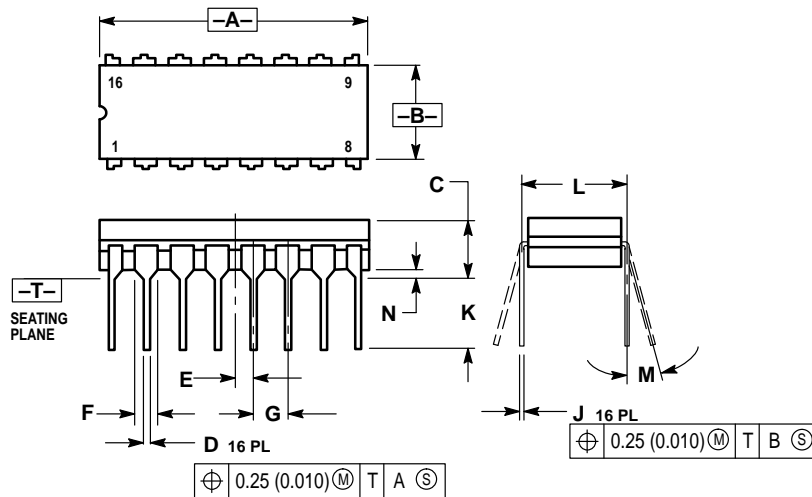
STX	1	16	V _{DD}
X0	2	15	ST _Y
X1	3	14	Y0
X2	4	13	Y1
X3	5	12	Y2
A	6	11	Y3
B	7	10	W
V _{SS}	8	9	Z

LOGIC DIAGRAM



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

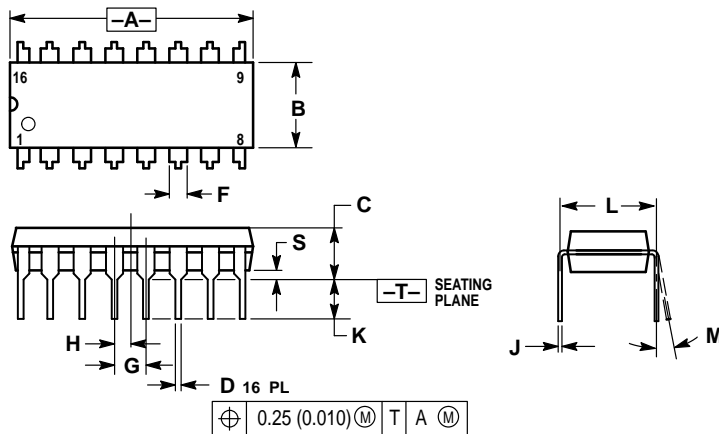


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



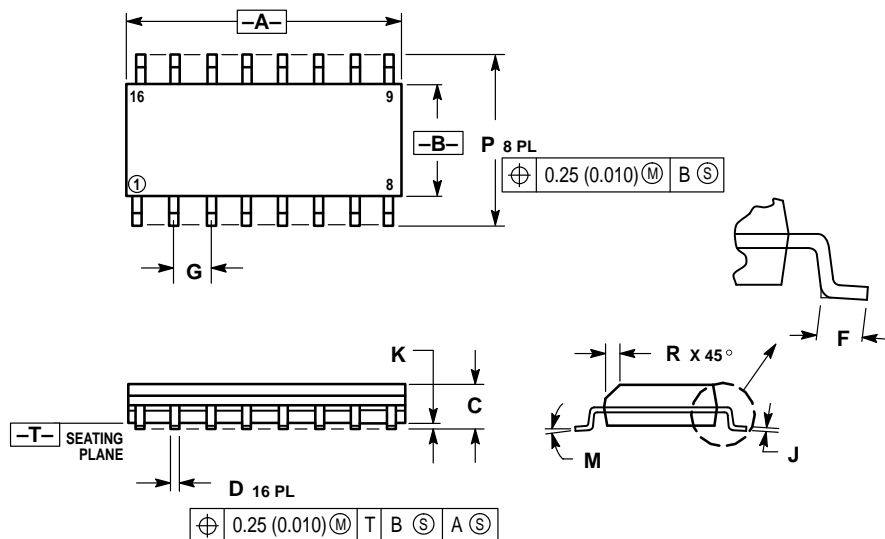
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MOTOROLA

MC14529B/D

