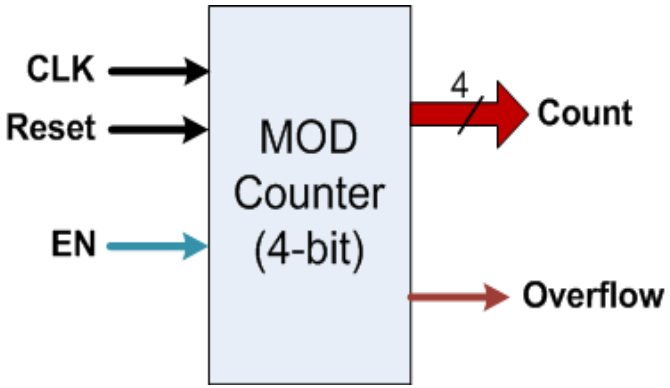
Programmable Electronics using FPGAs

Digital watches!

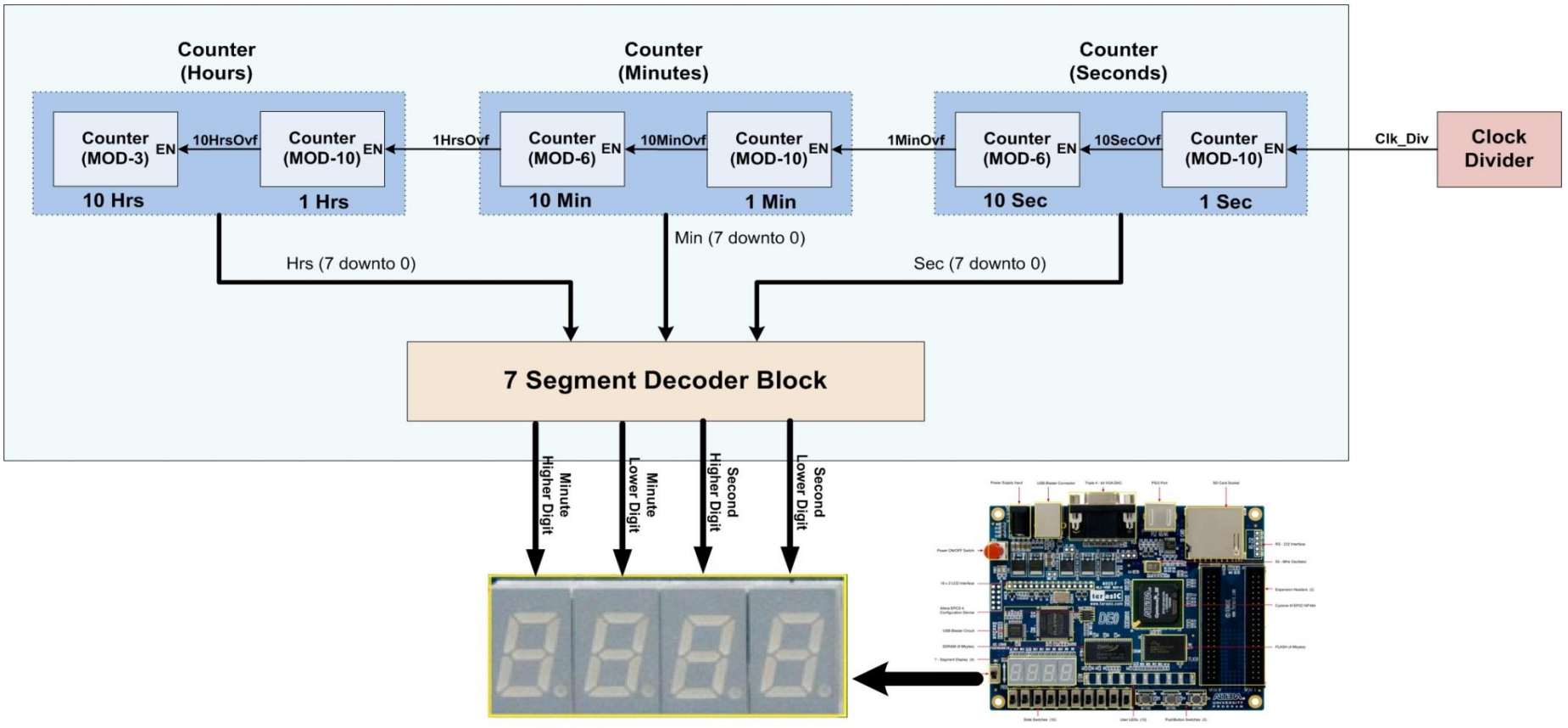
- Digital watch shows time in seconds, minutes and hours.
  - Seconds and minutes consist of 2 digits
    - 0-5, & 0-9
  - 4-bit MOD counter can be used for one digit



- In total six MOD-counters are needed:
  - 2x MOD-10 counters for LSD seconds and minutes (0..9)
  - 2x MOD-6 counters for MSD seconds and minutes (0..5)
  - 1x MOD-4 counter for LSD hours (0..3)
  - 1x MOD-3 counter for MSD hours (0..2)

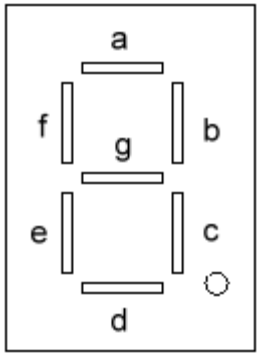
Digital watches!

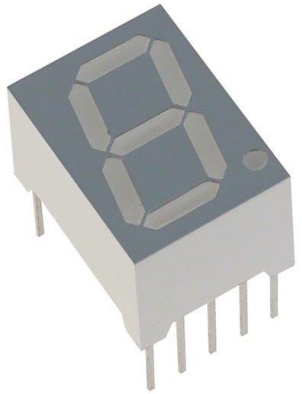
- Connect six MOD counters in such a way that overflow flag of a MOD counter acts as an enable input for the next MOD counter.
- Clock divider output acts as an enable input for the 1 second MOD-10 counter



Digital watches!

- The Altera DE0 Cyclone-III board has 4 seven segment display units.
- Each unit is based on 8 LEDs with common anode (low) logic.
  - 7 LEDs (***a*** to ***g***) are used for numeric display
  - 1 LED is for **Dp** display
- BCD (Binary coded Decimal) input is used.



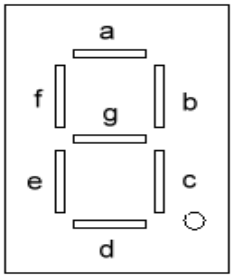


```
Entity SevenSeg_Driver
PORT (
   Enable      : IN     STD_LOGIC;
   Binary_Din : IN     STD_LOGIC_VECTOR (3 downto 0);
   Dec_Out    : OUT  STD_LOGIC_VECTOR (7 downto 0)
);
end SevenSeg_Driver;
```

Decimal	Binary				Seven segment codes							
	D	C	B	A	Dp	g	F	E	d	c	b	a
0	0	0	0	0	1	1	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	0	0	1
2	0	0	1	0	1	0	1	0	0	1	0	0
3	0	0	1	1	1	0	1	1	0	0	0	0
4	0	1	0	0	1	0	0	1	1	0	0	1
5	0	1	0	1	1	0	0	1	0	0	1	0
6	0	1	1	0	1	0	0	0	0	0	1	0
7	0	1	1	1	1	1	0	1	1	0	0	0
8	1	0	0	0	1	0	0	0	0	0	0	0
9	1	0	0	1	1	0	0	1	0	0	0	0

Truth table for converting decimal to binary to seven segment code
Conversion with common anode

Digital watches!



- BCD to 7-segment decoder is required.
  - It takes 4-bits binary input value and converts it into a decimal number.
  - For example, 4-bit binary input “0010” is decoded into 7-bit binary output “0100100”
- **Case statement** can be used for implementing the BCD to 7-segment decoder logic.

```
PROCESS ( Binary_Din )   BEGIN
      CASE Binary_Din IS
           when “0000”  =>  Dec_Out  <= “1000000”;    --   0
           when “0001”  =>  Dec_Out  <= “1111001”;    --   1
           when “0010”  =>  Dec_Out  <= “0100100”;    --   2
              ------------------.
           when “0111”  =>   Dec_Out  <= “1111000”;    --   7
           when “1000”  =>   Dec_Out  <= “0000000”;    --   8
           when “1001”  =>   Dec_Out  <= “0011000”;    --   9
             ------------------.
          when others   =>   Dec_Out  <= “1111111”;    --  Blank
END CASE;
END PROCESS;
```

Lab work :
Design your own digital watch

- We will provide these components
  - Clock divider
  - 4-bit MOD counter
  - Top level VHDL file for a digital watch without architecture part.
  - Board pinning le (EG3204-DE0.qsf)