Programmable Electronics using FPGAs

Lab 1 : familiarising ourselves with Quartus-II software

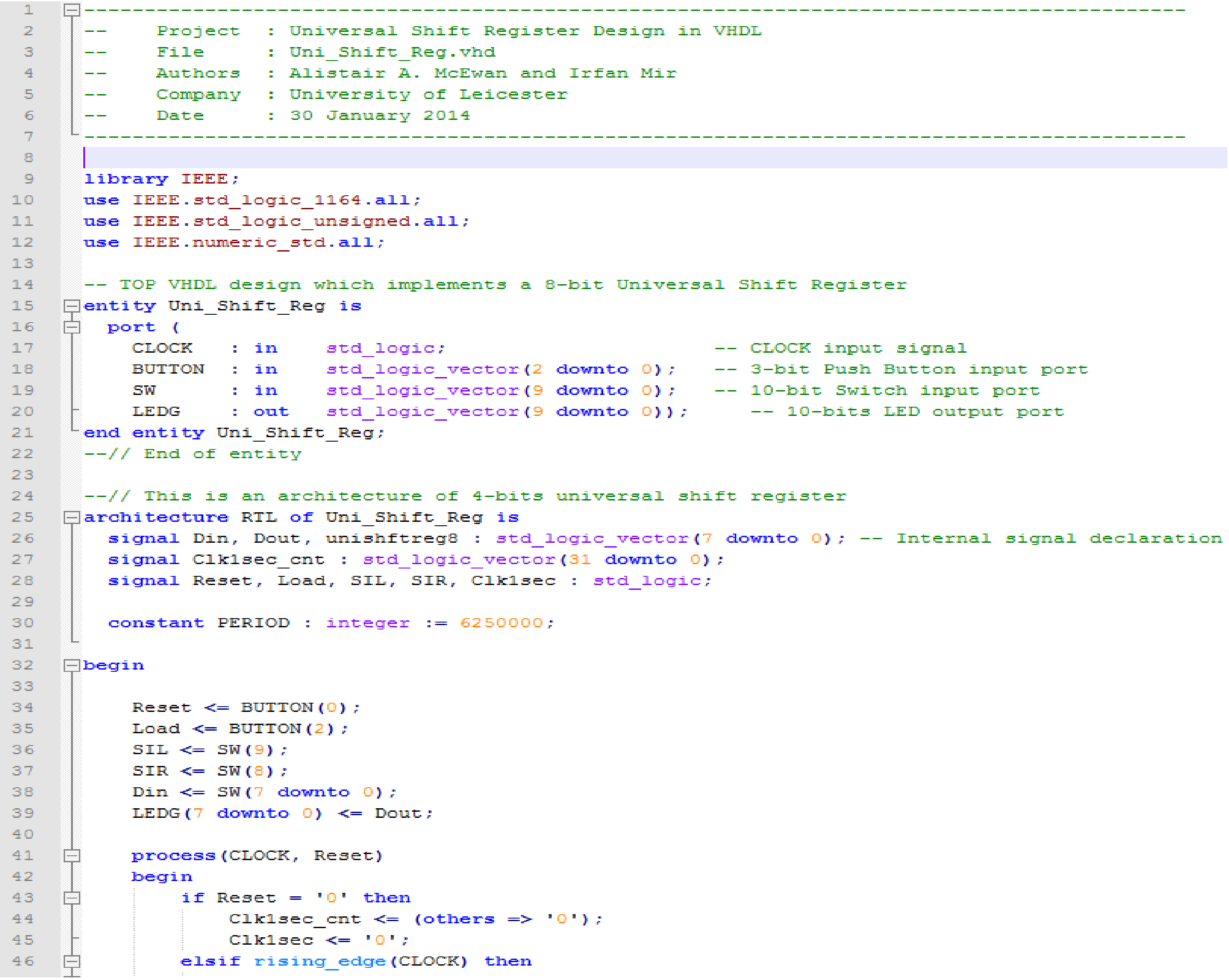
Alistair A. McEwan and Irfan Mir

This week…

- In this weeks lab, we will take an existing piece of VHDL code (provided on Blackboard)
- We will load this VHDL code into the Altera Quartus-II toolkit
- And build it for the FPGA
- The purpose of the lab is for you to become familiar with the process of using the tool, and the board
- So don’t be afraid to experiment!

RTL Design file

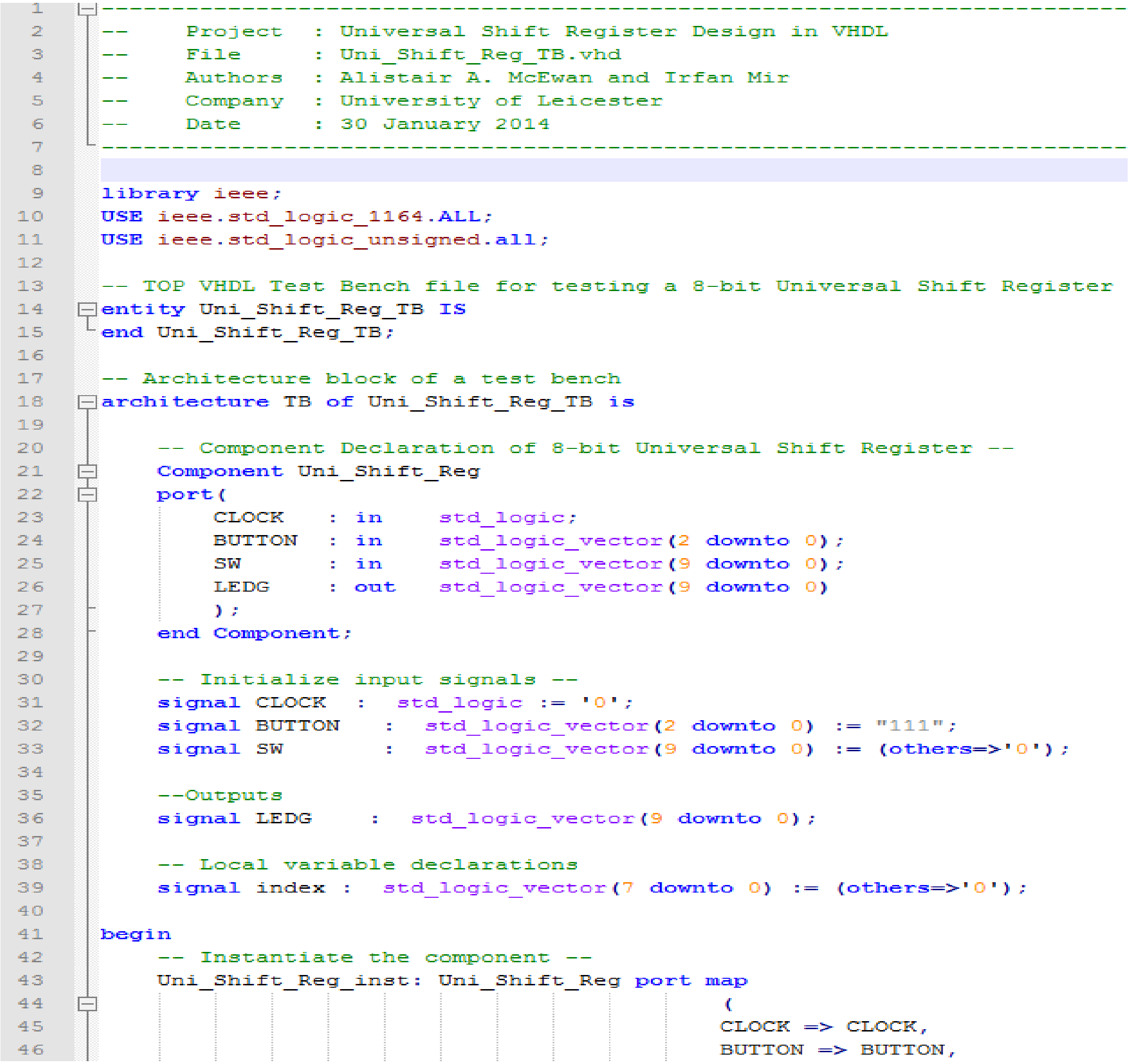
- Download the 8-bit universal shift register RTL design from blackboard.



```vhdl
-------------------------------------------------------------------------------------------
--     Project   : Universal Shift Register Design in VHDL
--     File      : Uni_Shift_Reg.vhd
--     Authors   : Alistair A. McEwan and Irfan Mir
--     Company   : University of Leicester
--     Date      : 30 January 2014
-------------------------------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
use IEEE.numeric_std.all;

-- TOP VHDL design which implements a 8-bit Universal Shift Register
entity Uni_Shift_Reg is
  port (
    CLOCK   : in    std_logic;                        -- CLOCK input signal
    BUTTON  : in    std_logic_vector(2 downto 0);     -- 3-bit Push Button input port
    SW      : in    std_logic_vector(9 downto 0);     -- 10-bit Switch input port
    LEDG    : out   std_logic_vector(9 downto 0));       -- 10-bits LED output port
end entity Uni_Shift_Reg;
--// End of entity

--// This is an architecture of 4-bits universal shift register
architecture RTL of Uni_Shift_Reg is
  signal Din, Dout, unishftreg8 : std_logic_vector(7 downto 0); -- Internal signal declaration
  signal Clk1sec_cnt : std_logic_vector(31 downto 0);
  signal Reset, Load, SIL, SIR, Clk1sec : std_logic;

  constant PERIOD : integer := 6250000;

begin

    Reset <= BUTTON(0);
    Load <= BUTTON(2);
    SIL <= SW(9);
    SIR <= SW(8);
    Din <= SW(7 downto 0);
    LEDG(7 downto 0) <= Dout;

    process(CLOCK, Reset)
    begin
        if Reset = '0' then
            Clk1sec_cnt <= (others => '0');
            Clk1sec <= '0';
        elsif rising_edge(CLOCK) then
```

Test bench file

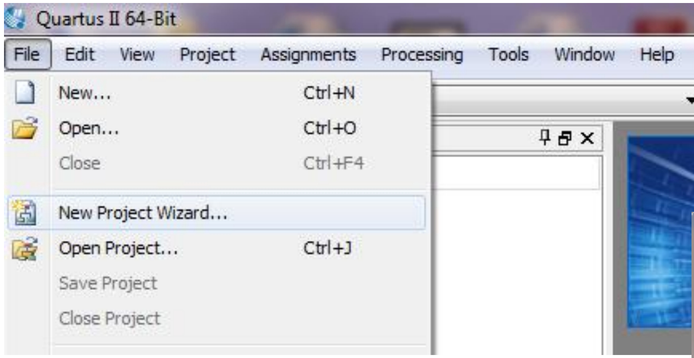
- Download the 8-bit universal shift register test bench from blackboard.



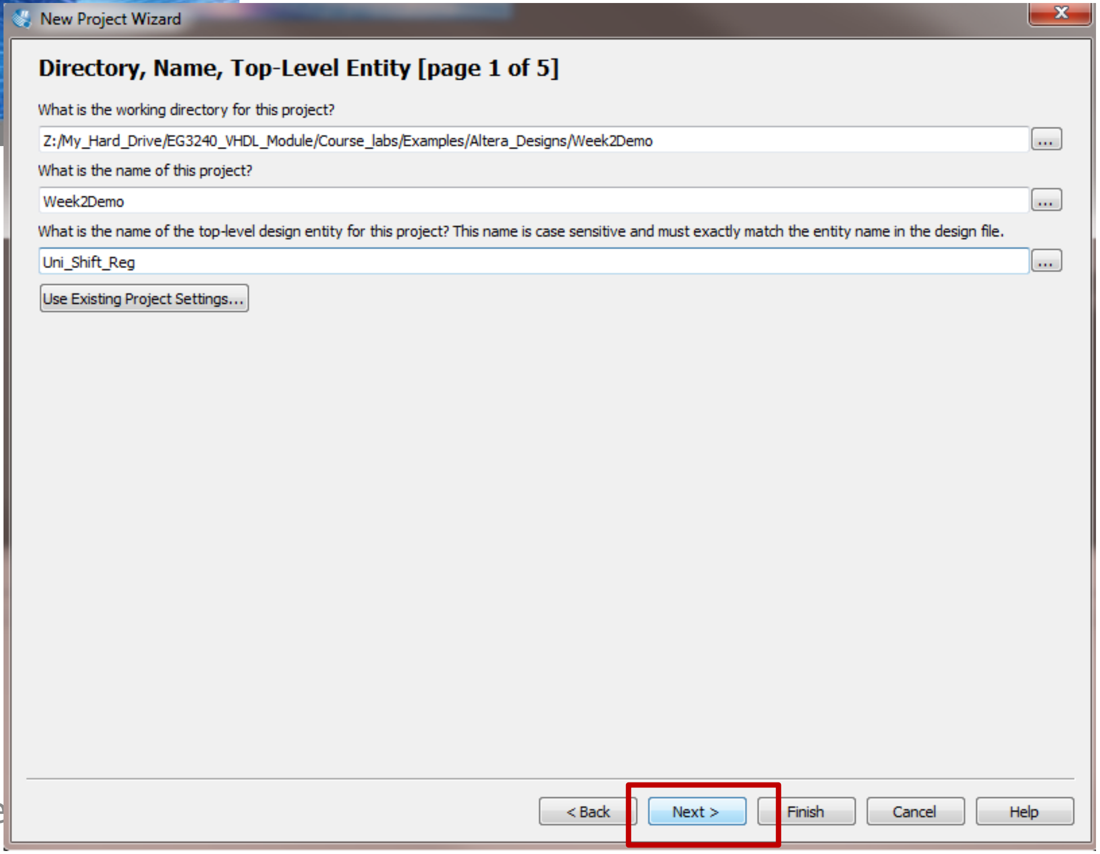
```vhdl
---------------------------------------------------------------------------------------
--      Project   : Universal Shift Register Design in VHDL
--      File      : Uni_Shift_Reg_TB.vhd
--      Authors   : Alistair A. McEwan and Irfan Mir
--      Company   : University of Leicester
--      Date      : 30 January 2014
---------------------------------------------------------------------------------------

library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;

-- TOP VHDL Test Bench file for testing a 8-bit Universal Shift Register
entity Uni_Shift_Reg_TB IS
end Uni_Shift_Reg_TB;

-- Architecture block of a test bench
architecture TB of Uni_Shift_Reg_TB is

    -- Component Declaration of 8-bit Universal Shift Register --
    Component Uni_Shift_Reg
    port(
        CLOCK    : in     std_logic;
        BUTTON   : in     std_logic_vector(2 downto 0);
        SW       : in     std_logic_vector(9 downto 0);
        LEDG     : out    std_logic_vector(9 downto 0)
        );
    end Component;

    -- Initialize input signals --
    signal CLOCK   :  std_logic := '0';
    signal BUTTON    :  std_logic_vector(2 downto 0)  := "111";
    signal SW        :  std_logic_vector(9 downto 0)  := (others=>'0');

    --Outputs
    signal LEDG     :  std_logic_vector(9 downto 0);

    -- Local variable declarations
    signal index :  std_logic_vector(7 downto 0)  := (others=>'0');

begin
    -- Instantiate the component --
    Uni_Shift_Reg_inst: Uni_Shift_Reg port map
                                             (
                                             CLOCK => CLOCK,
                                             BUTTON => BUTTON,
```

Getting started with Quartus-II

- Start up the Altera Quartus-II software using the Quartus-II Web Edition icon on the desktop. This opens the tool and allow us to create a new project.



- **To create a new project:**
  - Select New Project Wizard on the File menu.
  - Give your project a name and location – this should be in your home drive.
  - Make sure you enter the right name in the top-level design entity.



Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

Z:/My_Hard_Drive/EG3240_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo

What is the name of this project?

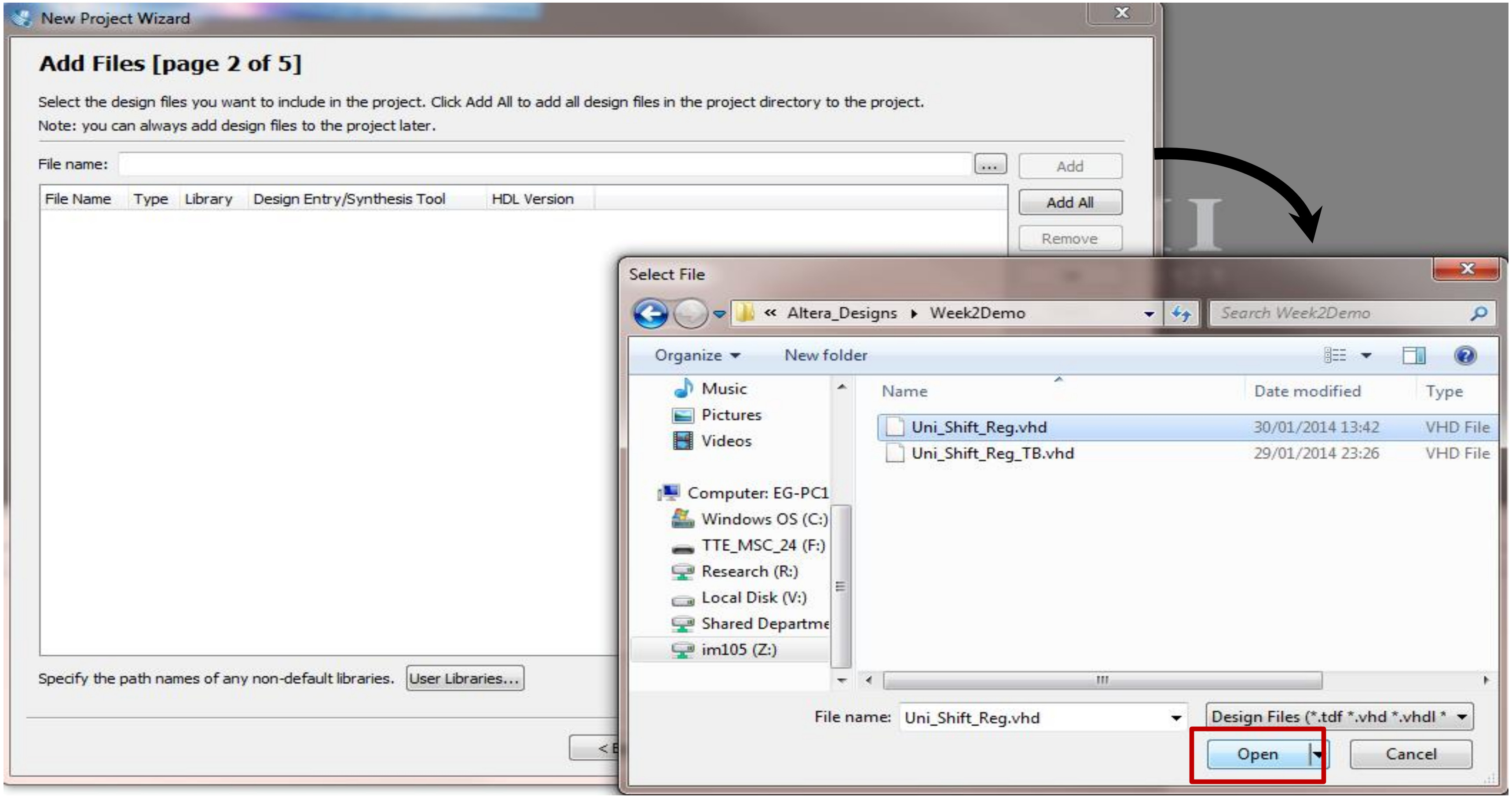
Week2Demo

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

Uni_Shift_Reg

Adding your VHDL design

- Normally, we will create our own VHDL template and write our own code.
  - (Next week we will show you how to do this)
- However this week, we will import an existing RTL design.



New Project Wizard
Add Files [page 2 of 5]
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.
File name:
...
Add
Add All
Remove
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
Specify the path names of any non-default libraries.
User Libraries...
< B
Select File
« Altera_Designs ▸ Week2Demo
Search Week2Demo
Organize ▾
New folder
Music
Pictures
Videos
Computer: EG-PC1
Windows OS (C:)
TTE_MSC_24 (F:)
Research (R:)
Local Disk (V:)
Shared Departme
im105 (Z:)
Open
Cancel

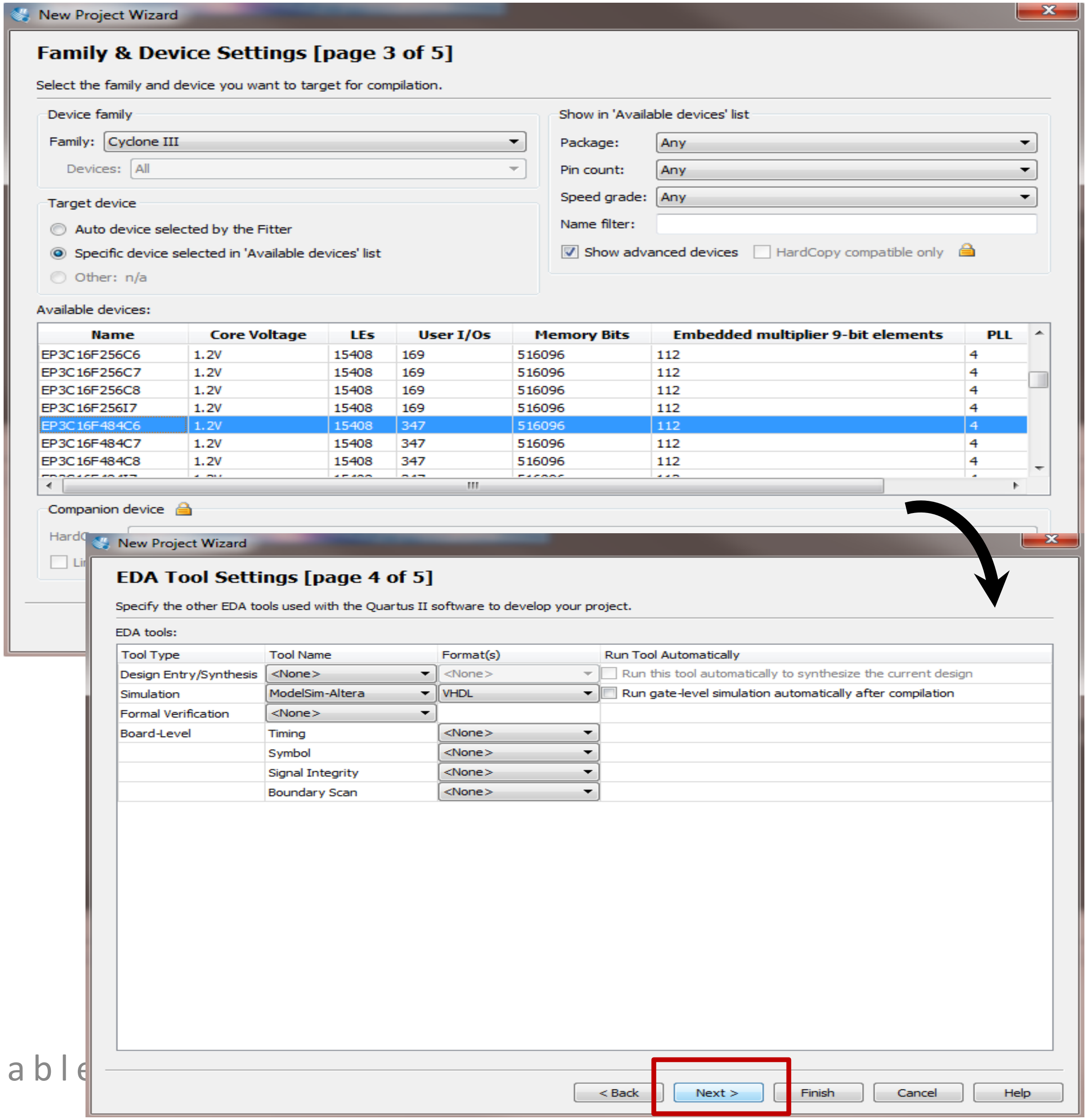
Name	Date modified	Type
Uni_Shift_Reg.vhd	30/01/2014 13:42	VHD File
Uni_Shift_Reg_TB.vhd	29/01/2014 23:26	VHD File

File name: Uni_Shift_Reg.vhd

Design Files (*.tdf *.vhd *.vhdl *

Choosing the board

- Project settings
  - Quartus-II is capable of building projects for many boards
  - Our is a <u>DE0 Development board</u> with a <u>Cyclone-III (EP3C16F484C6)</u> FPGA.
  - Select this option and click on <u>Next</u>
  - Make sure the Simulator is <u>ModelSim-Altera</u> and preferred language is VHDL.
  - Click on <u>Finish</u>



New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone III

Devices: All

Target device

○ Auto device selected by the Fitter

● Specific device selected in 'Available devices' list

○ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

☑ Show advanced devices □ HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL
EP3C16F256C6	1.2V	15408	169	516096	112	4
EP3C16F256C7	1.2V	15408	169	516096	112	4
EP3C16F256C8	1.2V	15408	169	516096	112	4
EP3C16F256I7	1.2V	15408	169	516096	112	4
EP3C16F484C6	1.2V	15408	347	516096	112	4
EP3C16F484C7	1.2V	15408	347	516096	112	4
EP3C16F484C8	1.2V	15408	347	516096	112	4

Companion device

New Project Wizard

EDA Tool Settings [page 4 of 5]

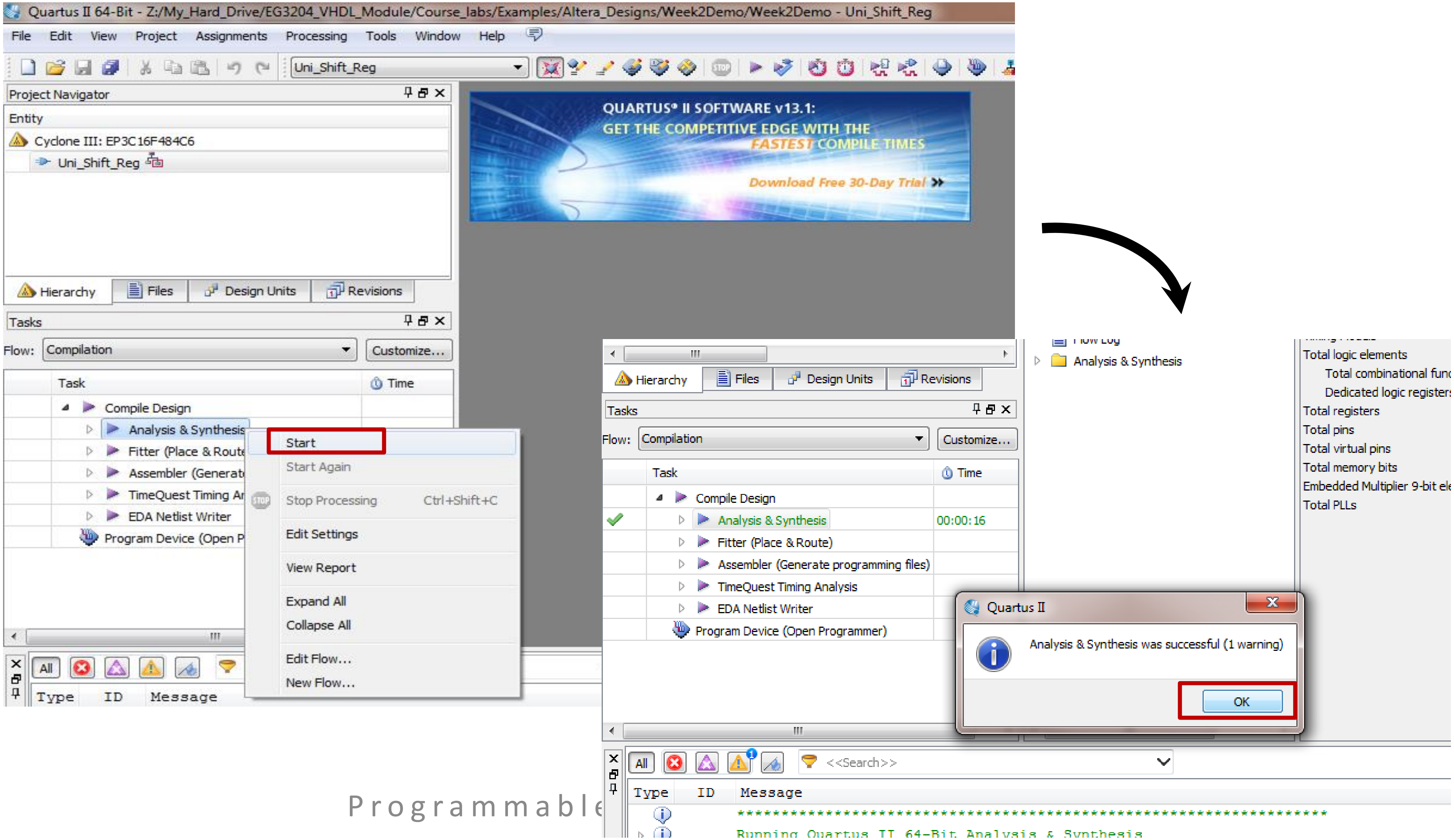
Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	□ Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	□ Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Synthesis (compiling) our code

- Click on Analysis & Synthesize under Compile Design to compile the VHDL design into netlist.



Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2Demo - Uni_Shift_Reg

Cyclone III: EP3C16F484C6

Uni_Shift_Reg

Flow: Compilation

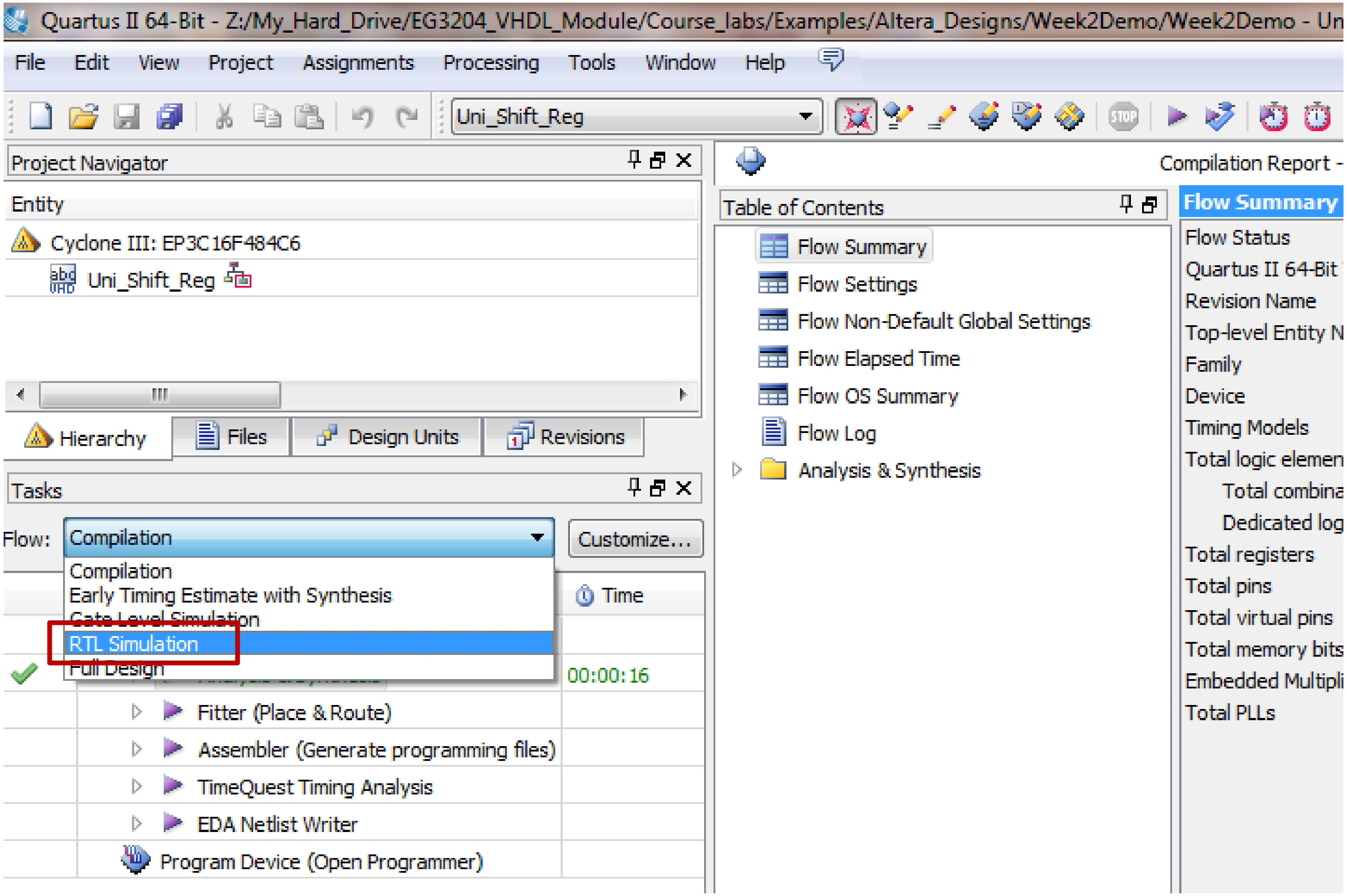
Quartus II

Analysis & Synthesis was successful (1 warning)

```
Type  ID  Message
          ************************************************************************
          Running Quartus II 64-Bit Analysis & Synthesis
```

Testing our hardware

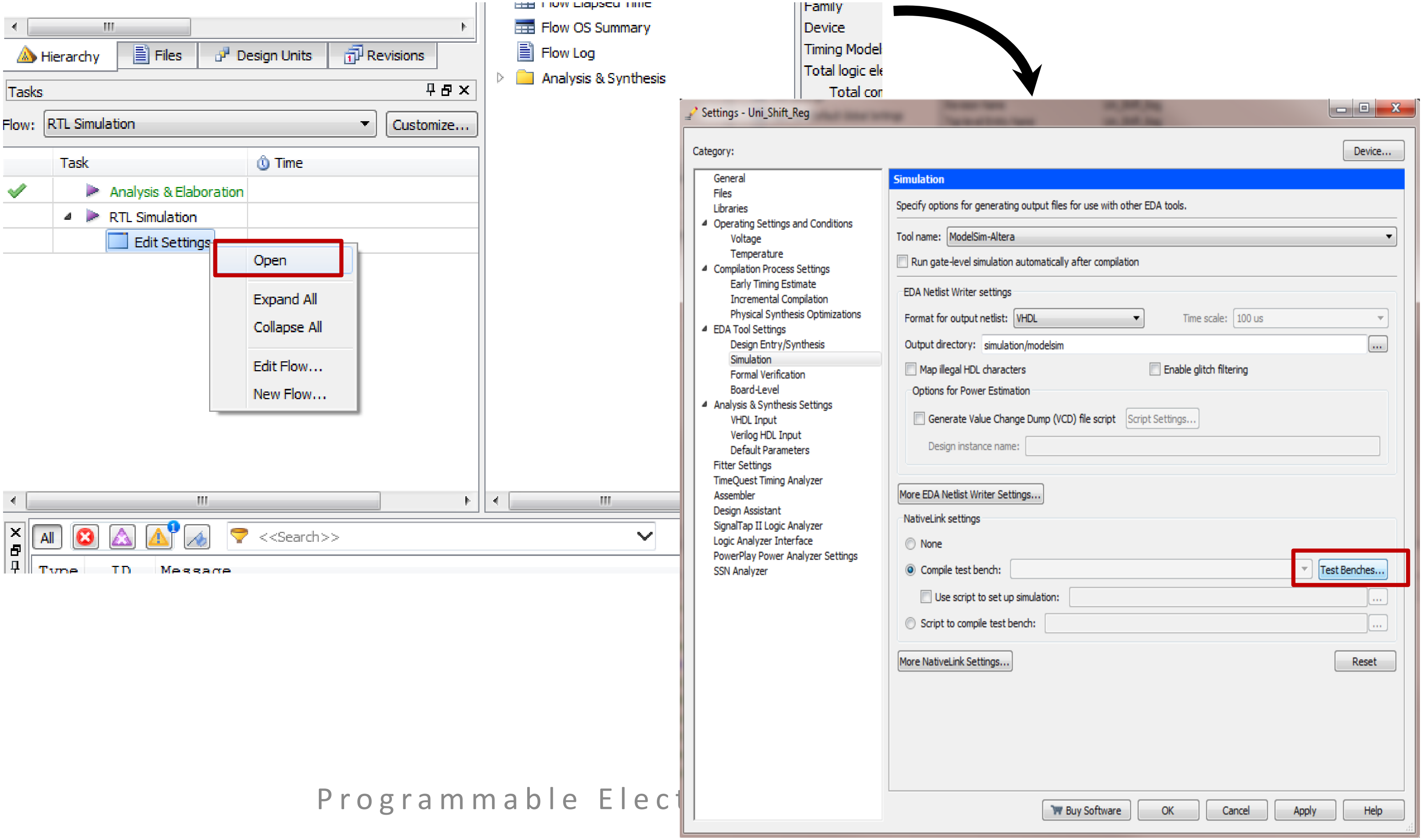
- Download the test bed from blackboard and set it up. First click on the RTL Simulation option in the Flow tab.



Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2Demo - Un

Testing our hardware

- Open Edit Settings in RTL Simulation option. In Settings window click on Test Benches option.



Settings - Uni_Shift_Reg

Category:

- General
- Files
- Libraries
- Operating Settings and Conditions
  - Voltage
  - Temperature
- Compilation Process Settings
  - Early Timing Estimate
  - Incremental Compilation
  - Physical Synthesis Optimizations
- EDA Tool Settings
  - Design Entry/Synthesis
  - Simulation
  - Formal Verification
  - Board-Level
- Analysis & Synthesis Settings
  - VHDL Input
  - Verilog HDL Input
  - Default Parameters
- Fitter Settings
- TimeQuest Timing Analyzer
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Settings
- SSN Analyzer

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim-Altera

□ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: VHDL Time scale: 100 us

Output directory: simulation/modelsim

□ Map illegal HDL characters □ Enable glitch filtering

Options for Power Estimation

□ Generate Value Change Dump (VCD) file script Script Settings...

Design instance name:

More EDA Netlist Writer Settings...

NativeLink settings

○ None

● Compile test bench: Test Benches...

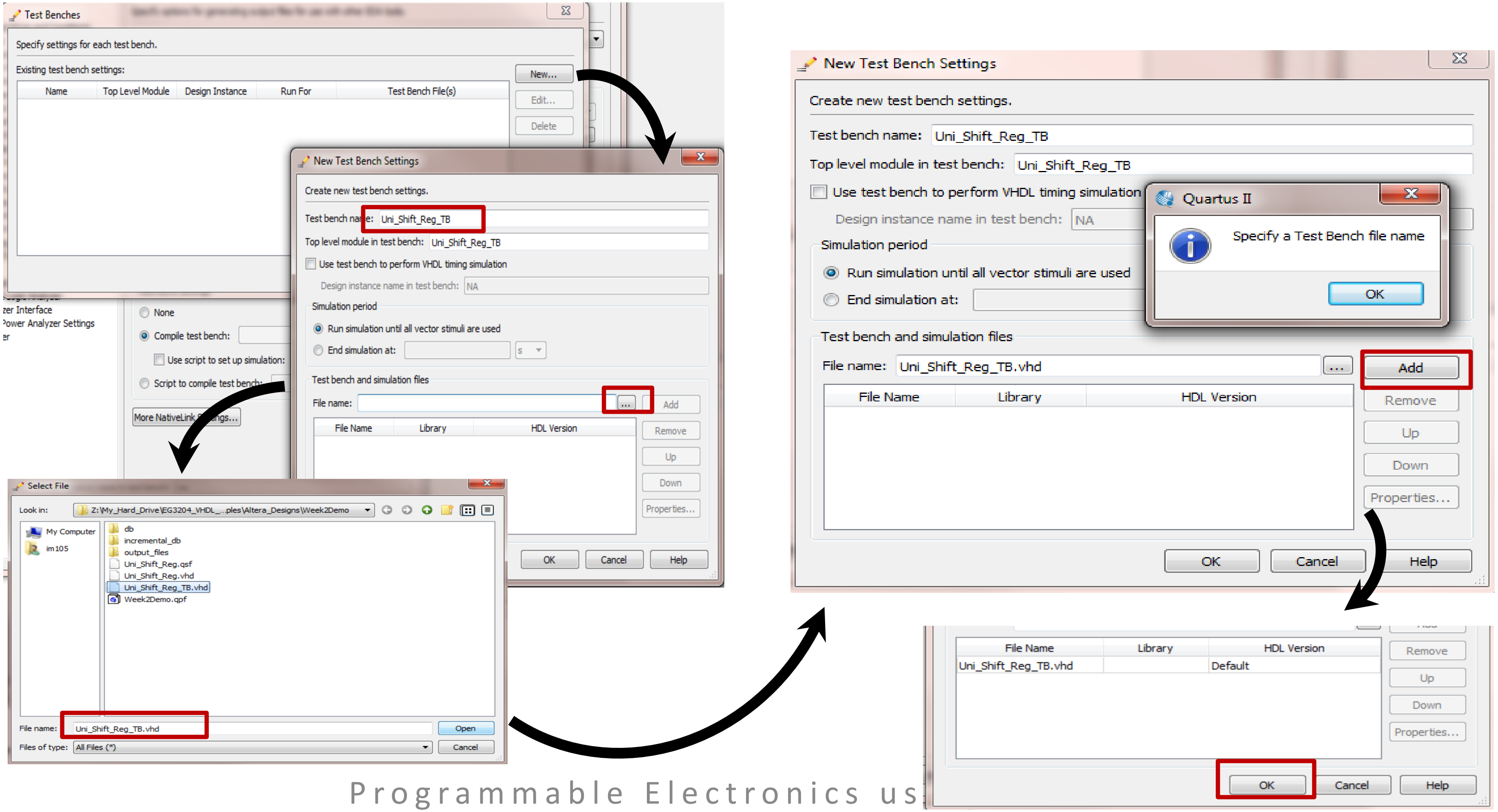
□ Use script to set up simulation:

○ Script to compile test bench:

More NativeLink Settings... Reset

Testing our hardware

- In the Test Benches window click on New. In New Test Bench Settings write your test bench's entity name in the Test Bench Name field. In File Name field assign your test bench file. Finally click on Add and then press OK.



Test Benches

Specify settings for each test bench.

Existing test bench settings:

Name	Top Level Module	Design Instance	Run For	Test Bench File(s)

New Test Bench Settings

Create new test bench settings.

Test bench name: Uni_Shift_Reg_TB

Top level module in test bench: Uni_Shift_Reg_TB

□ Use test bench to perform VHDL timing simulation

Design instance name in test bench: NA

Simulation period

● Run simulation until all vector stimuli are used

○ End simulation at:

Test bench and simulation files

File name:

File Name	Library	HDL Version

Select File

Look in: Z:\My_Hard_Drive\EG3204_VHDL_...ples\Altera_Designs\Week2Demo

My Computer

im105

db

incremental_db

output_files

Uni_Shift_Reg.qsf

Uni_Shift_Reg.vhd

Uni_Shift_Reg_TB.vhd

Week2Demo.qpf

File name: Uni_Shift_Reg_TB.vhd

Files of type: All Files (*)

New Test Bench Settings

Create new test bench settings.

Test bench name: Uni_Shift_Reg_TB

Top level module in test bench: Uni_Shift_Reg_TB

□ Use test bench to perform VHDL timing simulation

Design instance name in test bench: NA

Simulation period

● Run simulation until all vector stimuli are used

○ End simulation at:

Test bench and simulation files

File name: Uni_Shift_Reg_TB.vhd

File Name	Library	HDL Version

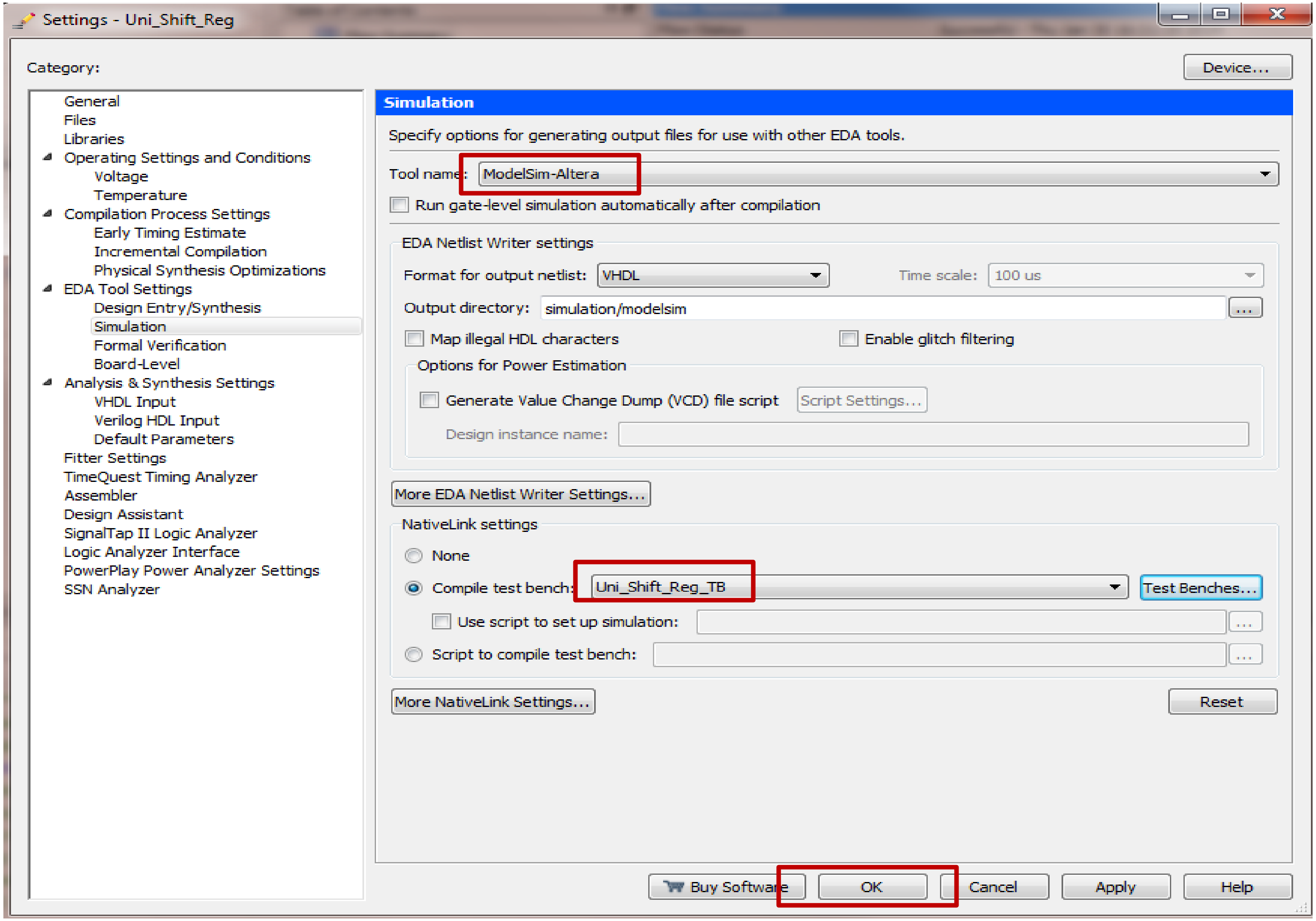
Quartus II

Specify a Test Bench file name

File Name	Library	HDL Version
Uni_Shift_Reg_TB.vhd		Default

Testing our hardware

- We will see your test bench file in Compile Test Bench option. Click on Apply and then press OK.



Settings - Uni_Shift_Reg

Category:

- General
- Files
- Libraries
- Operating Settings and Conditions
  - Voltage
  - Temperature
- Compilation Process Settings
  - Early Timing Estimate
  - Incremental Compilation
  - Physical Synthesis Optimizations
- EDA Tool Settings
  - Design Entry/Synthesis
  - Simulation
  - Formal Verification
  - Board-Level
- Analysis & Synthesis Settings
  - VHDL Input
  - Verilog HDL Input
  - Default Parameters
- Fitter Settings
- TimeQuest Timing Analyzer
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Settings
- SSN Analyzer

Device...

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: ModelSim-Altera

□ Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: VHDL   Time scale: 100 us

Output directory: simulation/modelsim ...

□ Map illegal HDL characters   □ Enable glitch filtering

Options for Power Estimation

□ Generate Value Change Dump (VCD) file script   Script Settings...

Design instance name:

More EDA Netlist Writer Settings...

NativeLink settings

○ None

● Compile test bench: Uni_Shift_Reg_TB   Test Benches...

□ Use script to set up simulation: ...

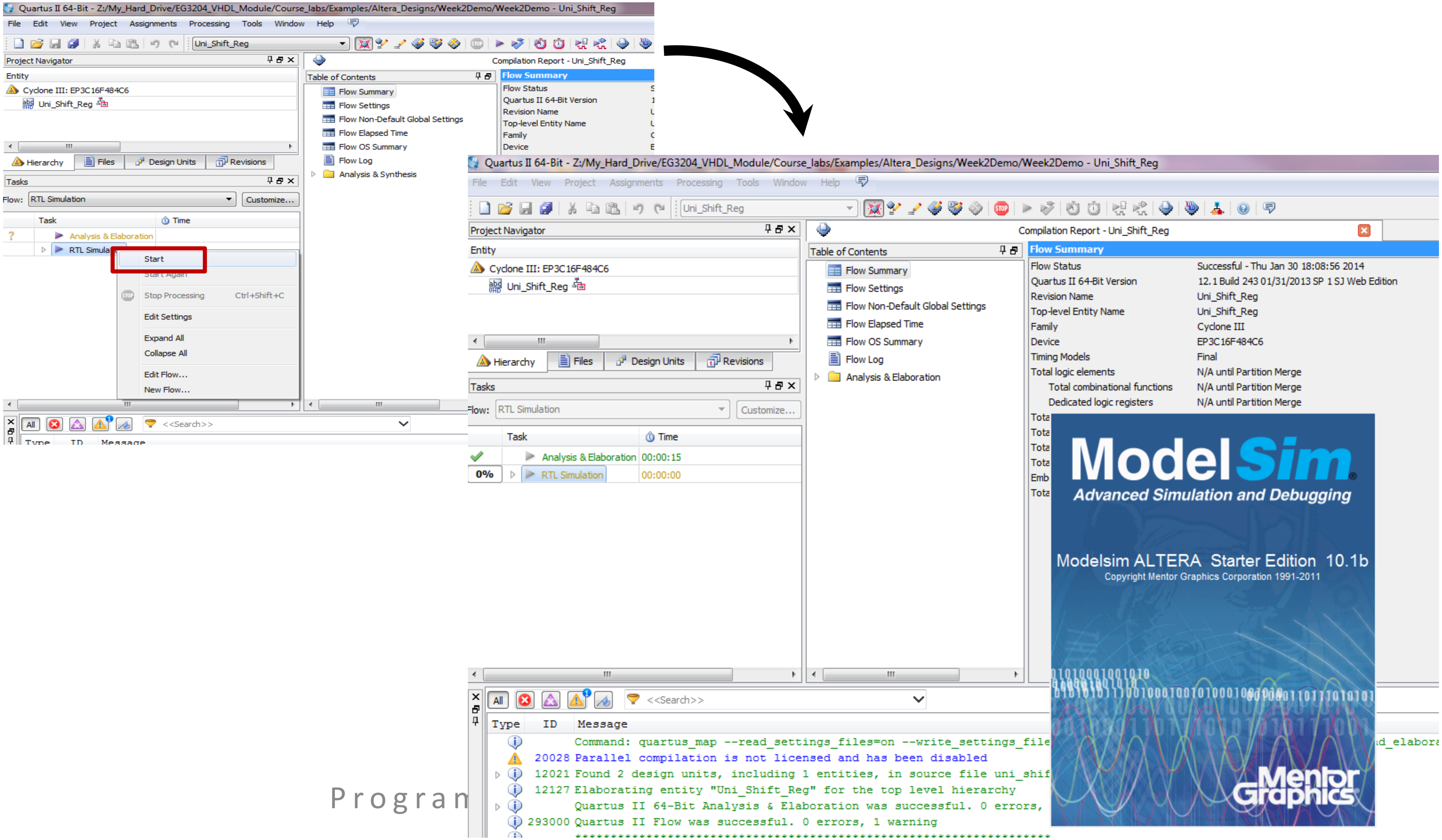
○ Script to compile test bench: ...

More NativeLink Settings...   Reset

Buy Software   OK   Cancel   Apply   Help

Testing our hardware

- Right click on RTL Simulation option under Flow tab and then click on Start. It will start the Altera-ModelSim simulator.

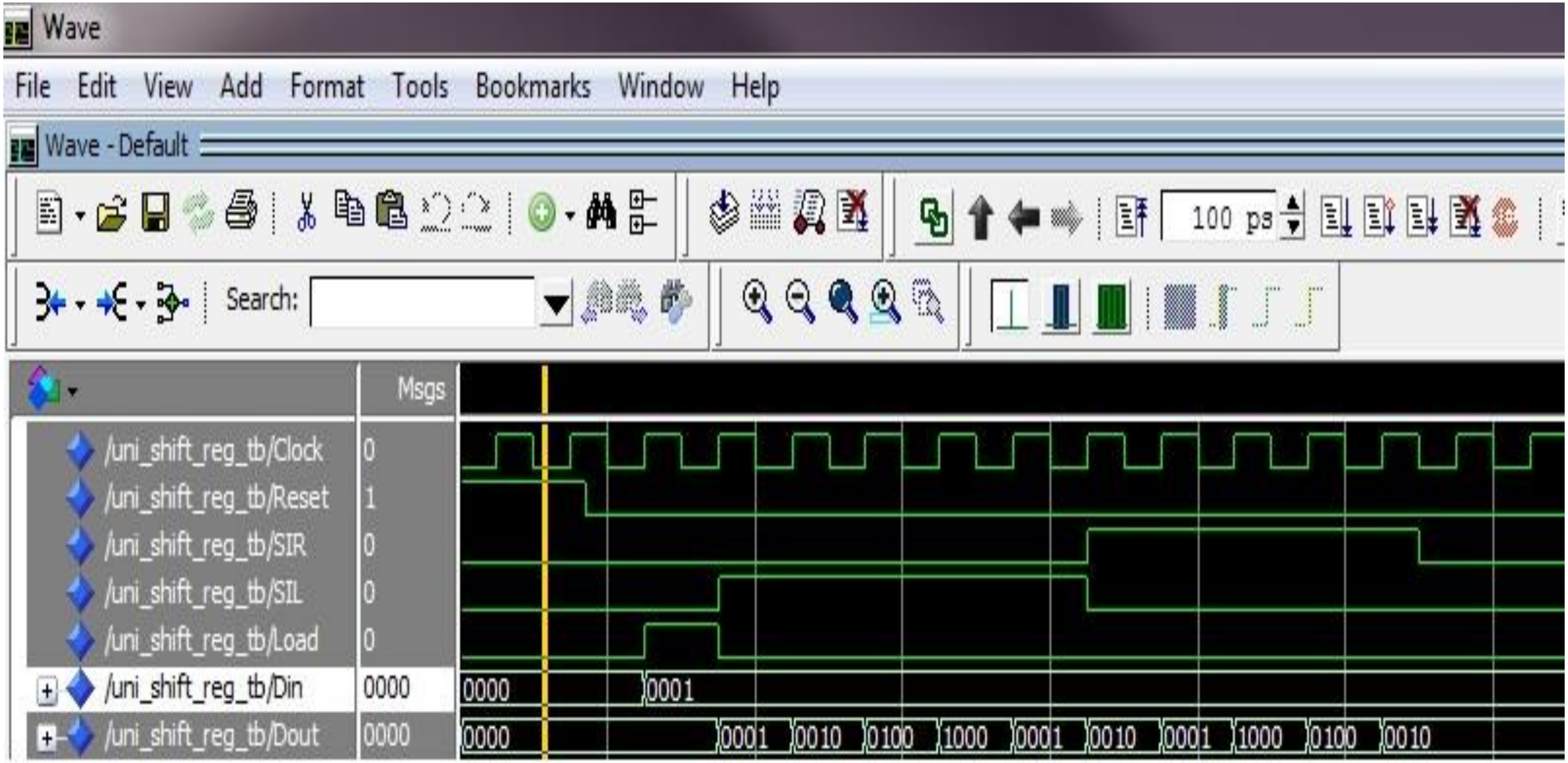

Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2Demo - Uni_Shift_Reg
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Project Navigator
Entity
Cyclone III: EP3C16F484C6
Uni_Shift_Reg
Hierarchy
Files
Design Units
Revisions
Tasks
Flow: RTL Simulation
Customize...
Task
Time
Analysis & Elaboration
RTL Simula
Start
Start Again
Stop Processing Ctrl+Shift+C
Edit Settings
Expand All
Collapse All
Edit Flow...
New Flow...
Compilation Report - Uni_Shift_Reg
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Analysis & Elaboration 00:00:15
0% RTL Simulation 00:00:00
All
<<Search>>
Model*Sim*
Advanced Simulation and Debugging
Modelsim ALTERA Starter Edition 10.1b
Copyright Mentor Graphics Corporation 1991-2011
Mentor Graphics

Flow Summary	
Flow Status	Successful - Thu Jan 30 18:08:56 2014
Quartus II 64-Bit Version	12.1 Build 243 01/31/2013 SP 1 SJ Web Edition
Revision Name	Uni_Shift_Reg
Top-level Entity Name	Uni_Shift_Reg
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Total logic elements	N/A until Partition Merge
Total combinational functions	N/A until Partition Merge
Dedicated logic registers	N/A until Partition Merge

```
Type  ID     Message
             Command: quartus_map --read_settings_files=on --write_settings_file
      20028  Parallel compilation is not licensed and has been disabled
      12021  Found 2 design units, including 1 entities, in source file uni_shif
      12127  Elaborating entity "Uni_Shift_Reg" for the top level hierarchy
             Quartus II 64-Bit Analysis & Elaboration was successful. 0 errors,
      293000 Quartus II Flow was successful. 0 errors, 1 warning
```

Testing our hardware

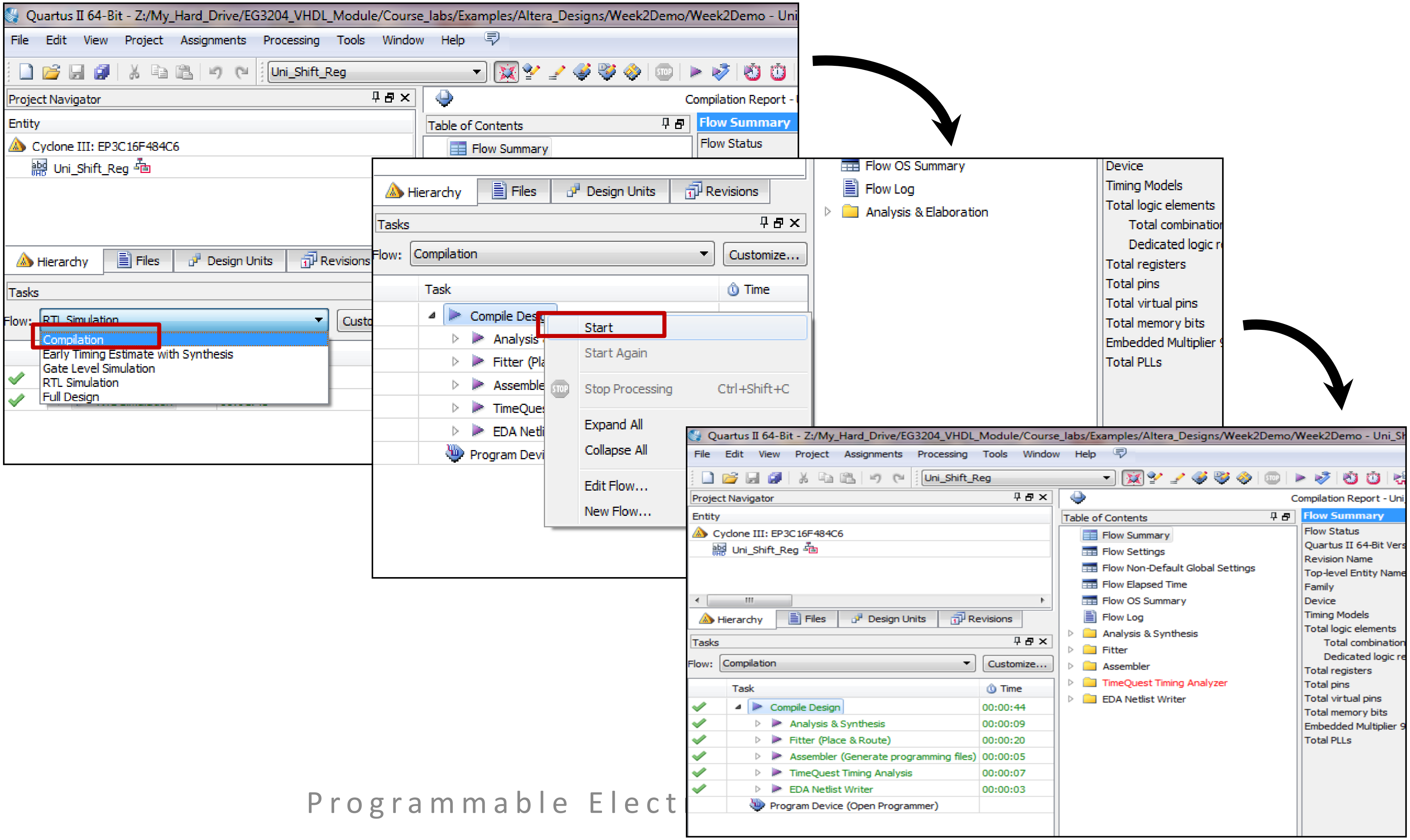
- The Altera-ModelSim simulator will show the waveforms for your inputs and outputs. Check that each input combination gives the output result you expect!



	Msgs	
/uni_shift_reg_tb/Clock	0	
/uni_shift_reg_tb/Reset	1	
/uni_shift_reg_tb/SIR	0	
/uni_shift_reg_tb/SIL	0	
/uni_shift_reg_tb/Load	0	
/uni_shift_reg_tb/Din	0000	0000 0001
/uni_shift_reg_tb/Dout	0000	0000 0001 0010 0100 1000 0001 0010 0001 1000 0100 0010

Preparation for DE0 FPGA Board

- Select the Compilation option in Flow tab. Right click on Compile Design and then Start.



Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2Demo - Uni

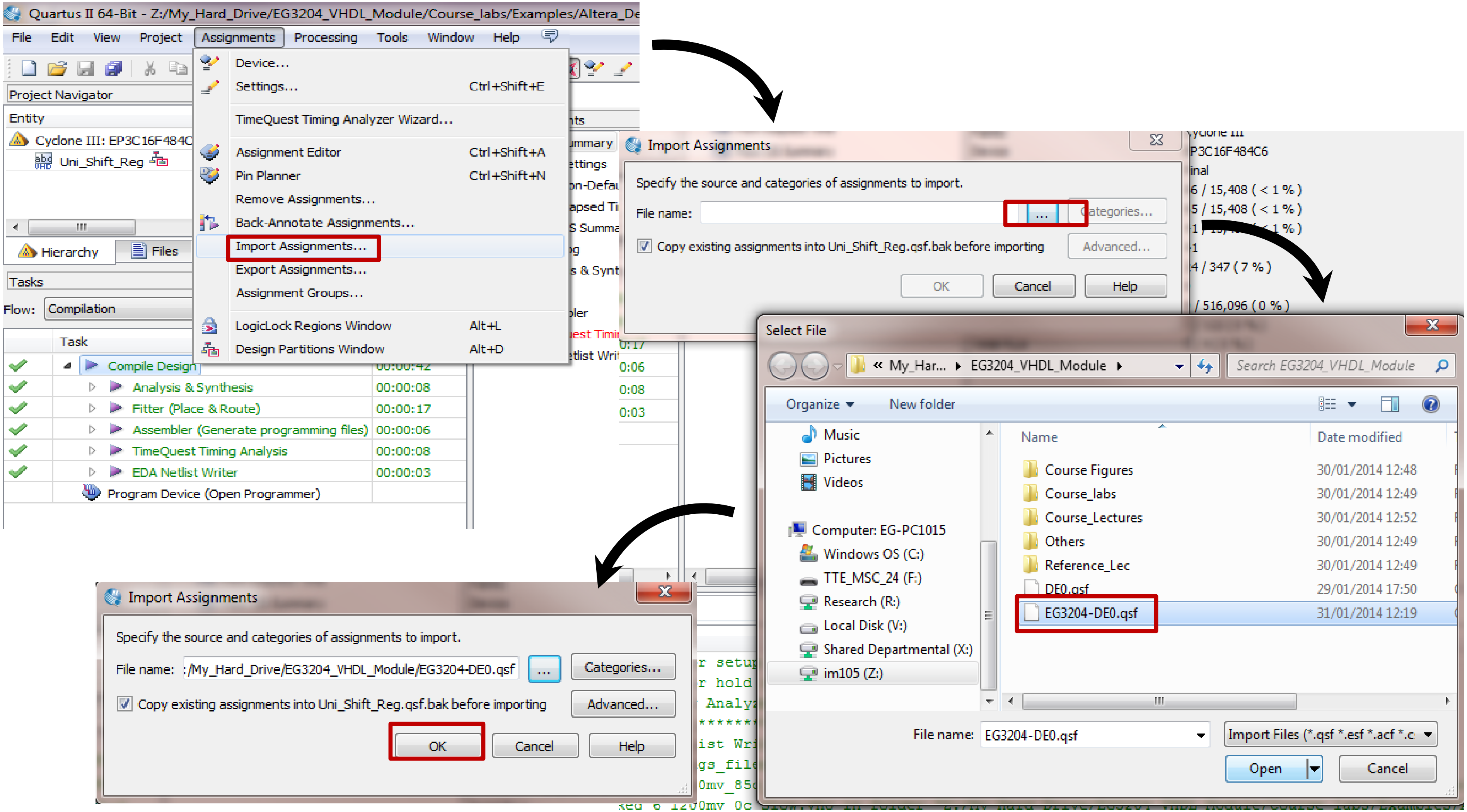
Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2Demo - Uni_Sh

Flow: Compilation

	Task	Time
✓	Compile Design	00:00:44
✓	Analysis & Synthesis	00:00:09
✓	Fitter (Place & Route)	00:00:20
✓	Assembler (Generate programming files)	00:00:05
✓	TimeQuest Timing Analysis	00:00:07
✓	EDA Netlist Writer	00:00:03
	Program Device (Open Programmer)	

Preparation for DE0 FPGA Board

- Download the pinning file EG3204-DE0.qsf from Blackboard and import it into the Quartus-II project. Open the Assignments tab and click on Import Assignments. Add the EG3204-DE0.qsf file and click OK.



Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_De

Project Navigator

Entity: Cyclone III: EP3C16F484C6 / Uni_Shift_Reg

Flow: Compilation

Task	
✓ Compile Design	00:00:42
✓ Analysis & Synthesis	00:00:08
✓ Fitter (Place & Route)	00:00:17
✓ Assembler (Generate programming files)	00:00:06
✓ TimeQuest Timing Analysis	00:00:08
✓ EDA Netlist Writer	00:00:03
Program Device (Open Programmer)	

Import Assignments

Specify the source and categories of assignments to import.

File name:

☑ Copy existing assignments into Uni_Shift_Reg.qsf.bak before importing

Select File

Name	Date modified
Course Figures	30/01/2014 12:48
Course_labs	30/01/2014 12:49
Course_Lectures	30/01/2014 12:52
Others	30/01/2014 12:49
Reference_Lec	30/01/2014 12:49
DE0.qsf	29/01/2014 17:50
EG3204-DE0.qsf	31/01/2014 12:19

File name: EG3204-DE0.qsf

Import Files (*.qsf *.esf *.acf *.c

Import Assignments

Specify the source and categories of assignments to import.

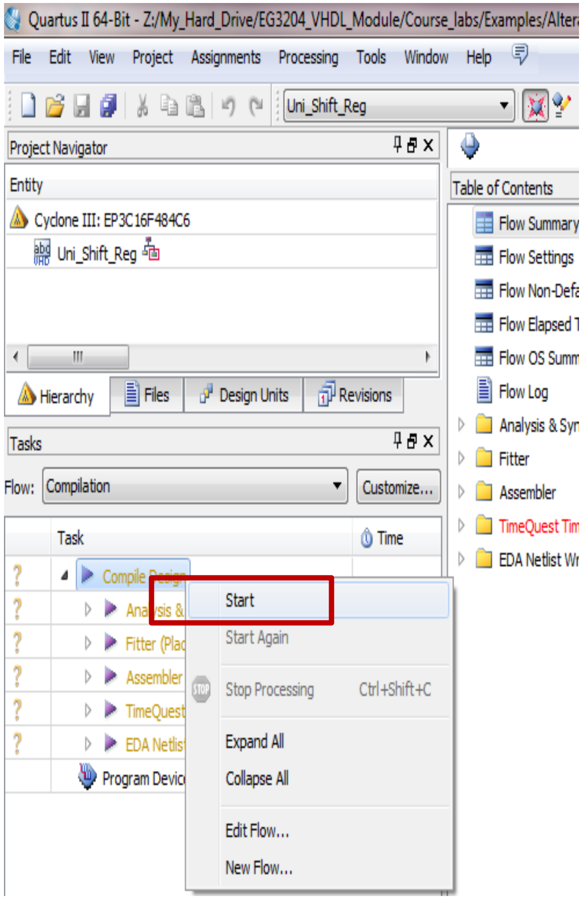
File name: :/My_Hard_Drive/EG3204_VHDL_Module/EG3204-DE0.qsf

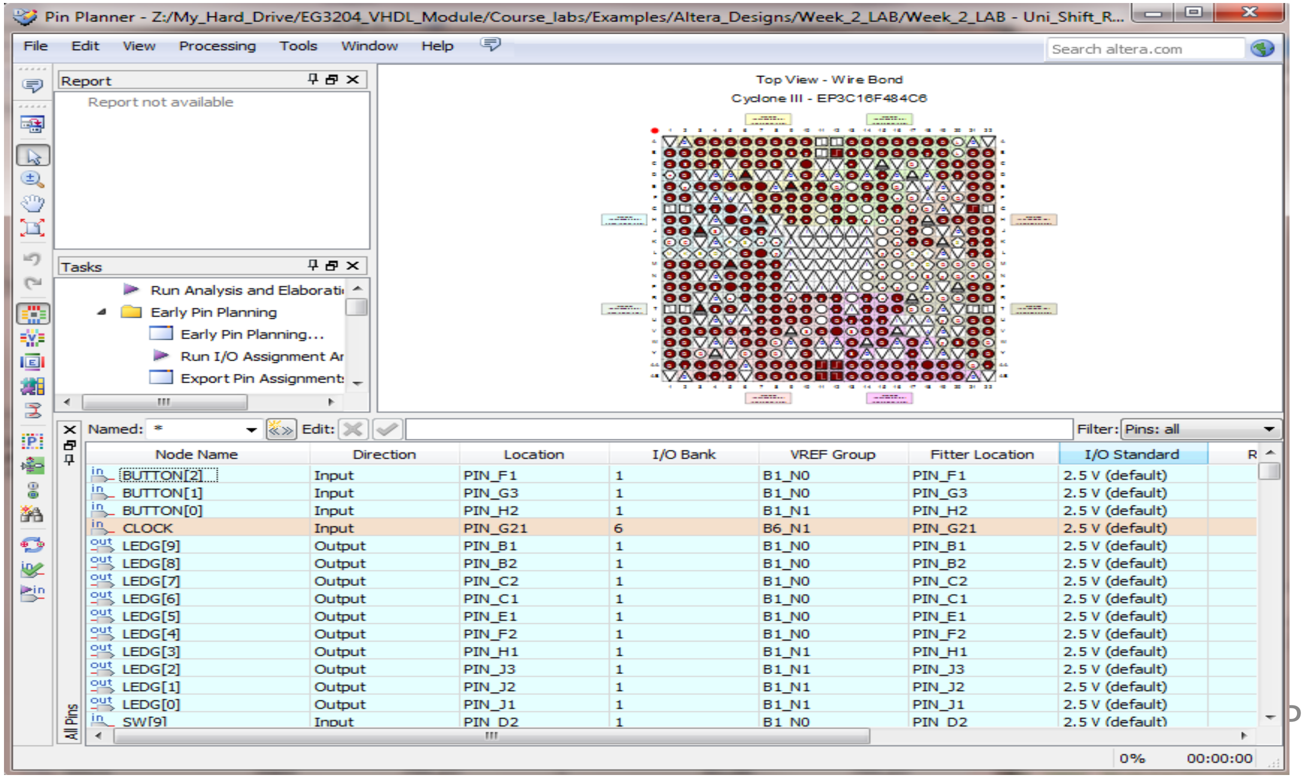
☑ Copy existing assignments into Uni_Shift_Reg.qsf.bak before importing

Finally compiling for the FPGA!

- Compile the design to update the FPGA pin connections to generate bit file (*.sof).

- The pinning (QSF) file EG3204-DE0.qsf will connect your VHDL design with FPGA board. You can see the pin assignments using Pin Planner under Assignments tab.

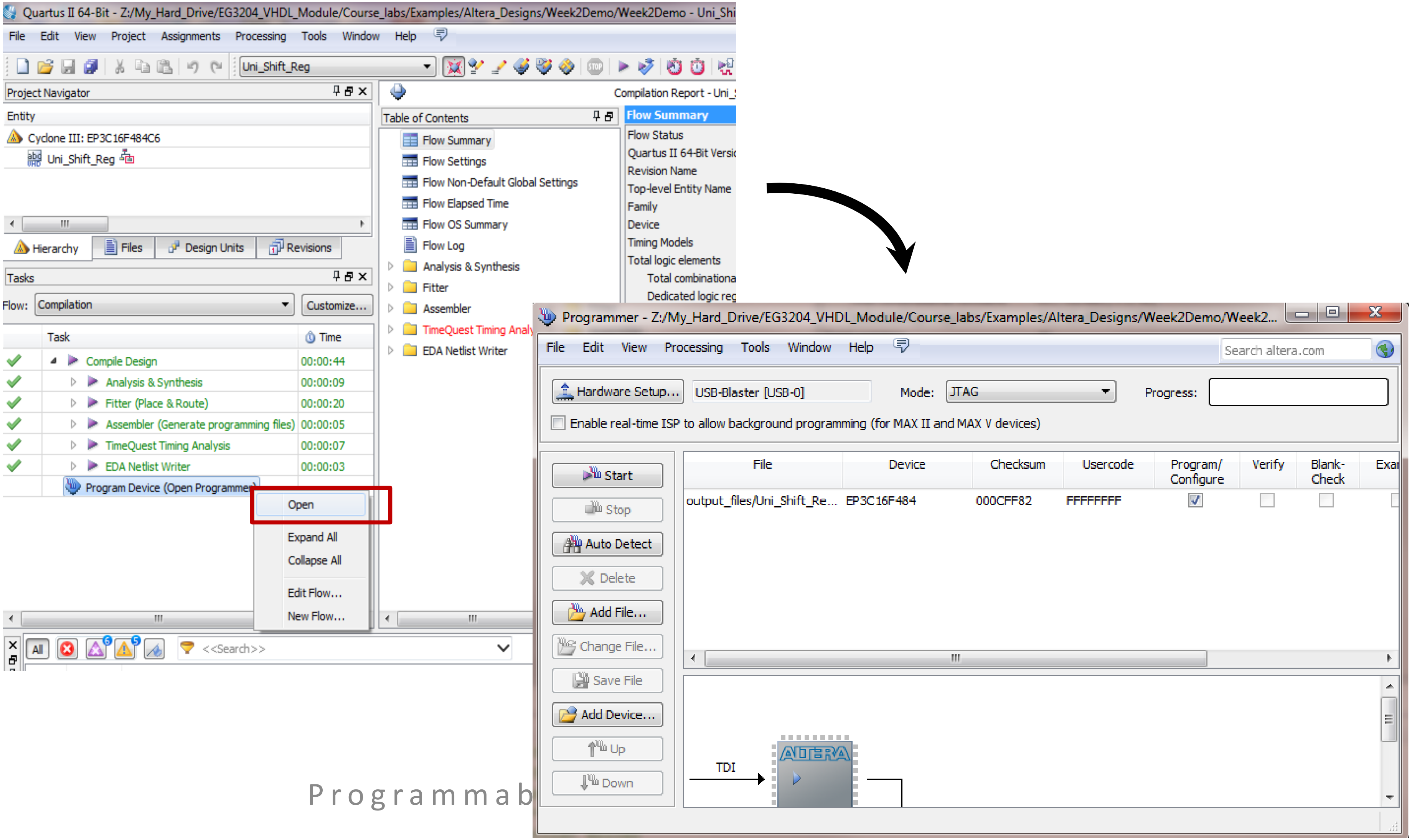



Pin Planner - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week_2_LAB/Week_2_LAB - Uni_Shift_R...
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Tasks
Run Analysis and Elaborati
Early Pin Planning
Early Pin Planning...
Run I/O Assignment Ar
Export Pin Assignment
Top View - Wire Bond
Cyclone III - EP3C16F484C6
Named: *
Edit:
Filter: Pins: all
All Pins
0%
00:00:00

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	R
BUTTON[2]	Input	PIN_F1	1	B1_N0	PIN_F1	2.5 V (default)	
BUTTON[1]	Input	PIN_G3	1	B1_N0	PIN_G3	2.5 V (default)	
BUTTON[0]	Input	PIN_H2	1	B1_N1	PIN_H2	2.5 V (default)	
CLOCK	Input	PIN_G21	6	B6_N1	PIN_G21	2.5 V (default)	
LEDG[9]	Output	PIN_B1	1	B1_N0	PIN_B1	2.5 V (default)	
LEDG[8]	Output	PIN_B2	1	B1_N0	PIN_B2	2.5 V (default)	
LEDG[7]	Output	PIN_C2	1	B1_N0	PIN_C2	2.5 V (default)	
LEDG[6]	Output	PIN_C1	1	B1_N0	PIN_C1	2.5 V (default)	
LEDG[5]	Output	PIN_E1	1	B1_N0	PIN_E1	2.5 V (default)	
LEDG[4]	Output	PIN_F2	1	B1_N0	PIN_F2	2.5 V (default)	
LEDG[3]	Output	PIN_H1	1	B1_N1	PIN_H1	2.5 V (default)	
LEDG[2]	Output	PIN_J3	1	B1_N1	PIN_J3	2.5 V (default)	
LEDG[1]	Output	PIN_J2	1	B1_N1	PIN_J2	2.5 V (default)	
LEDG[0]	Output	PIN_J1	1	B1_N1	PIN_J1	2.5 V (default)	
SW[9]	Input	PIN_D2	1	B1_N0	PIN_D2	2.5 V (default)	

Load programming file

- Once this is complete, click on Program Device (Open Programmer).
- This will load a file with the extension .sof



Quartus II 64-Bit - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2Demo - Uni_Shi

Entity: Cyclone III: EP3C16F484C6 — Uni_Shift_Reg

Flow: Compilation

Task	Time
✓ Compile Design	00:00:44
✓ Analysis & Synthesis	00:00:09
✓ Fitter (Place & Route)	00:00:20
✓ Assembler (Generate programming files)	00:00:05
✓ TimeQuest Timing Analysis	00:00:07
✓ EDA Netlist Writer	00:00:03
Program Device (Open Programmer)	

Programmer - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2...

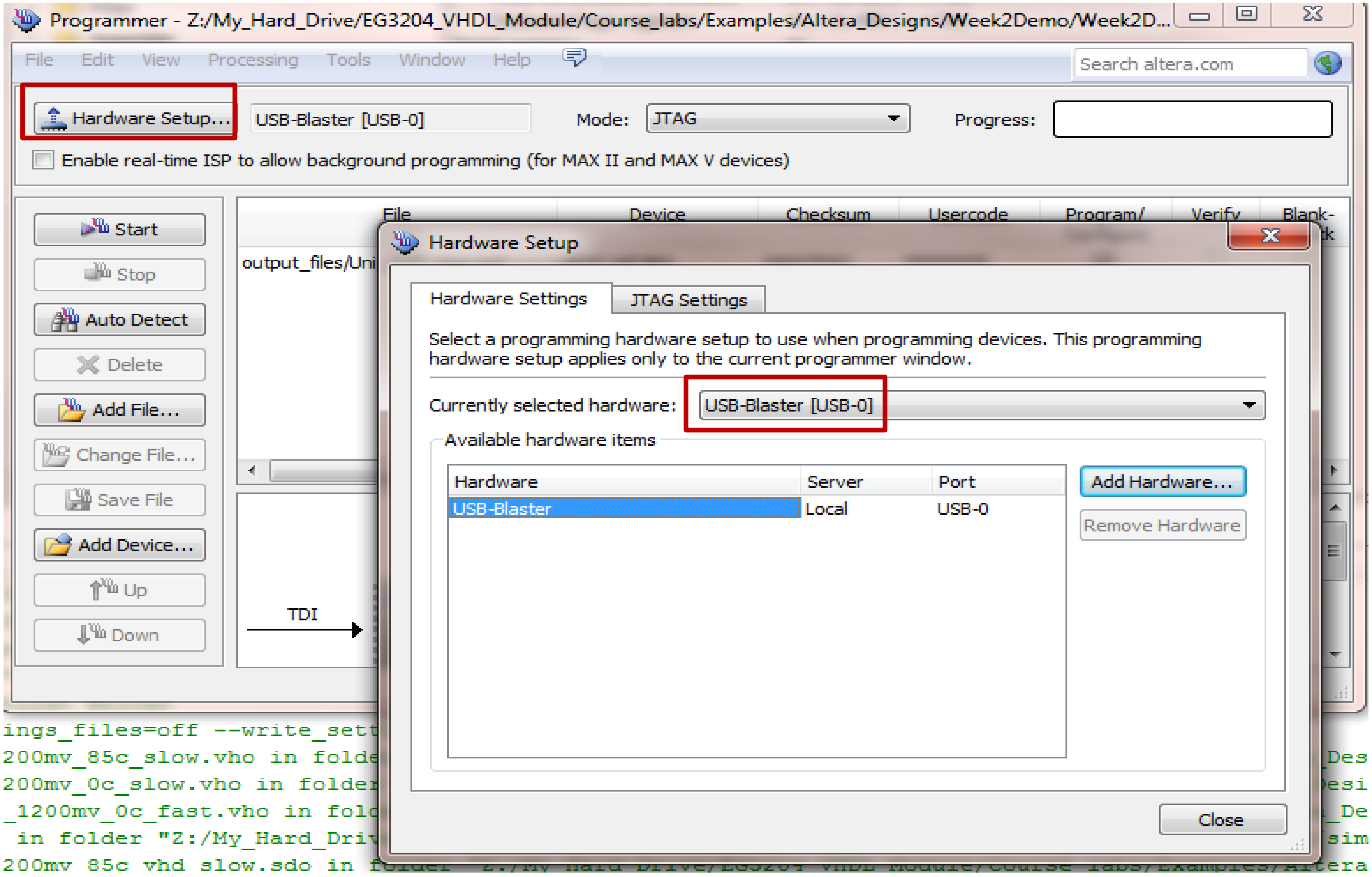
Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

□ Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check	Exa
output_files/Uni_Shift_Re...	EP3C16F484	000CFF82	FFFFFFFF	☑	□	□	□

Testing our hardware

- Turn in your DE0 board (the big red button!) and check the Hardware Setup
- Select the USB-Blaster [USB-0] option under hardware setting.



Programmer - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2D...

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress:

□ Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

Hardware Setup

Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.

Currently selected hardware: USB-Blaster [USB-0]

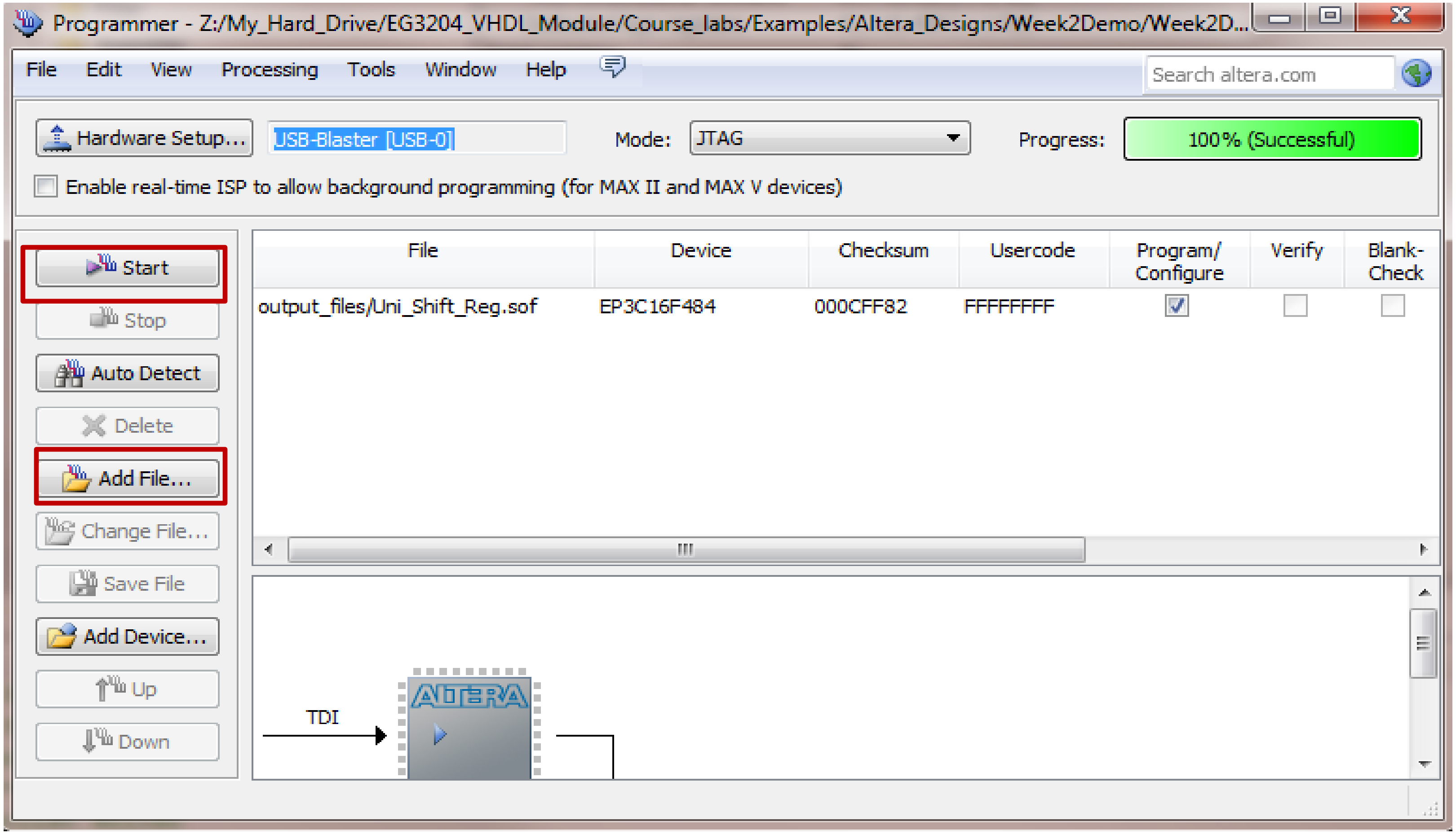
Available hardware items

Hardware	Server	Port
USB-Blaster	Local	USB-0

```
ings_files=off --write_sett
200mv_85c_slow.vho in folde                                            Des
200mv_0c_slow.vho in folder                                            esi
_1200mv_0c_fast.vho in fold                                            _De
 in folder "Z:/My_Hard_Driv                                            sim
200mv 85c vhd slow.sdo in folder "Z:/My Hard Drive/EG3204 VHDL Module/Course labs/Examples/Altera
```

Open Programmer tool

- Open Programmer should now tell you it has found the FPGA board.
- You can add the .sof file, if required.
- Click on Start to program the FPGA chip.



Programmer - Z:/My_Hard_Drive/EG3204_VHDL_Module/Course_labs/Examples/Altera_Designs/Week2Demo/Week2D...

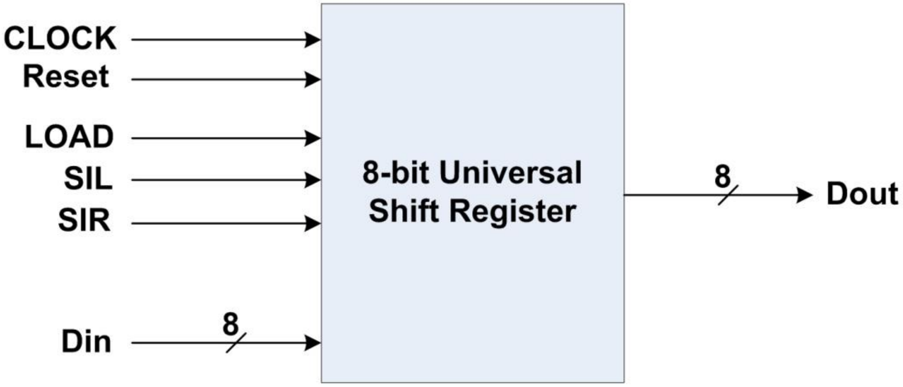
Hardware Setup... USB-Blaster [USB-0]   Mode: JTAG   Progress: 100% (Successful)

□ Enable real-time ISP to allow background programming (for MAX II and MAX V devices)

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank-Check
output_files/Uni_Shift_Reg.sof	EP3C16F484	000CFF82	FFFFFFFF	☑	□	□

Check the results on FPGA board

- If everything has worked, lights on your board should start flashing!



CLOCK	Reset	LOAD	SIL	SIR	
x	0	x	x	x	All zeros
↑	1	0	x	x	Load Data
↑	1	1	0	1	Right Shift
↑	1	1	1	0	Left Shift

Board Connections:

RESET → BUTTON(0)

LOAD → BUTTON(2)
SIL → SW(9)
SIR → SW(8)

Din(0) → SW(0)
Din(1) → SW(1)
Din(2) → SW(2)
Din(3) → SW(3)
Din(4) → SW(4)
Din(5) → SW(5)
Din(6) → SW(6)
Din(7) → SW(7)

Dout(0) → LEDG(0)
Dout(1) → LEDG(1)
Dout(2) → LEDG(2)
Dout(3) → LEDG(3)
Dout(4) → LEDG(4)
Dout(5) → LEDG(5)
Dout(6) → LEDG(6)
Dout(7) → LEDG(7)