EG3204 Programmable Electronics lab week 6
Identify, design, simulate, and test a circuit

In this weeks lab you will identify, design, simulate and test a given circuit. The gate-level diagram of a given circuit is shown in Figure . Here the interface of a circuit is described where the input ports are ***S0*** and ***S1*** and the output ports are ***Q0***, ***Q1***, ***Q2*** and ***Q3***. You need to complete this lab work in four steps:

- **Step 1:** Represent this circuit using a Boolean expressions and a truth table.
- **Step 2:** Implement this circuit in VHDL using dataflow modelling, and using behavioural modelling.
- **Step 3:** Create a test bench and compare the simulation with your truth table.
- **Step 4:** Implement your design on the FPGA board.

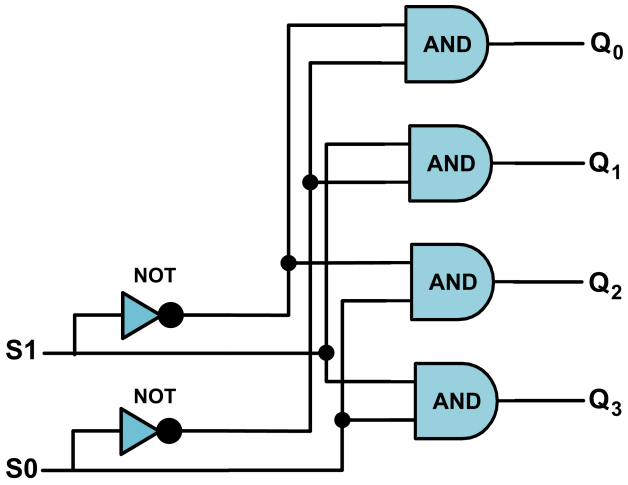

Figure 1: Gate-level diagram of a circuit.