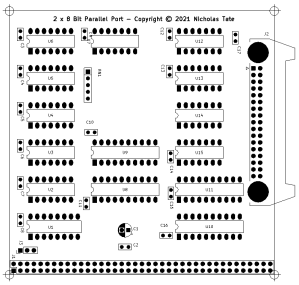
2x8 BIT PARALLEL PORT - KIT CONTENTS

Download users guide here: **https://github.com/ntate6630/Parallel_port**
Enquiries and technical support: **ntate6630@yahoo.co.uk**

1 x Interface PCB 

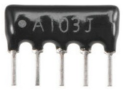
10 x 14 pin IC sockets - U2, U3, U4, U5, U6, U7, U12, U13, U14, U15 

1 x 16 pin IC socket - U1 

4 x 20 pin IC sockets - U8, U9, U10, U11 

1 x 100uF electrolytic capacitor - C1 

16 x 0.1uF ceramic capacitors - C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16 

1 x 10K SIL resistor array - RN1 

1 x 39 pin right angled single header strip 

1 x 78 pin right angled double header strip 

Either one or the other to be fitted in position – J1

1 x 34 way right angle locking IDC header - J2 

1x 3 pin header strip - J3 

1x 2 pin jumper 

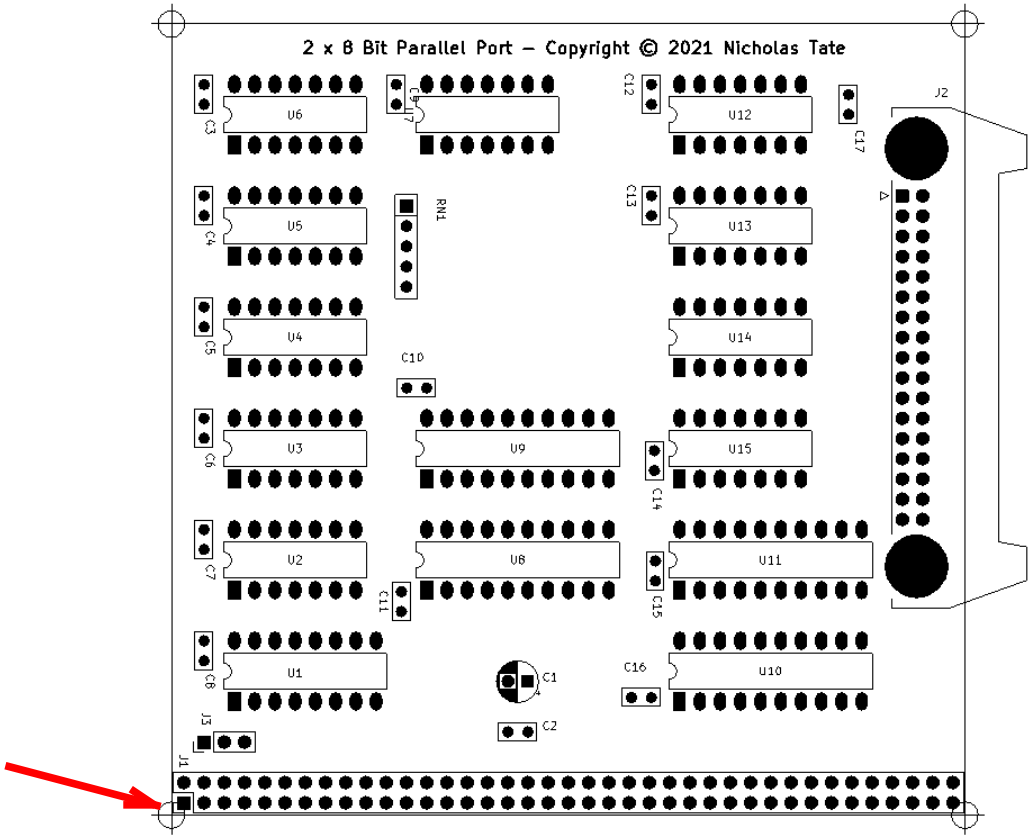
IC's

1 x 74xx139	- U1
1 x 74xx32	- U2
1 x 74xx14	- U3
1 x 74xx02	- U4
1 x 74xx74	- U5
2 x 74xx00	- U6, U7
3 x 74xx573	- U8, U9, U10
1 x 74xx244	- U11
4 x 74xx125	- U12, U13, U14, U15

NOTE: Due to semiconductor supply shortages you may receive IC's from any of the following logic families, 74HC, 74ALS, 74F series. All of these will work perfectly in whole sets or mixed combinations of different logic families.
Packaging will be from RECYCLED including: IC tubes, anti static bag, foam to hold IC sockets.

ASSEMBLY OF THE INTERFACE PCB

The printed component identifiers on the PCB are on the component side. Refer to this diagram and the parts list during assembly.



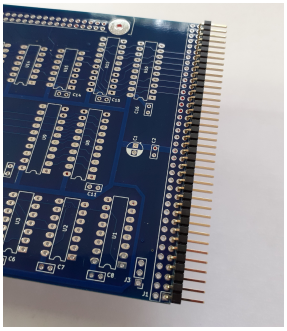
The interface board can be used in an RC2014 or compatible main-board or backplane fitted with either single or double row sockets.

If there are **single row sockets** on the main-board or backplane, fit a **single row right angled header strip** in the holes closest to the edge of the interface PCB in position **J1** indicated by the **red arrow**.

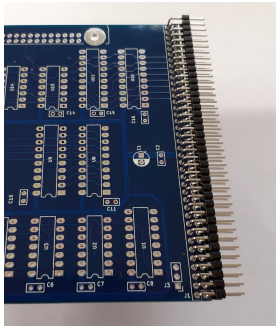
If there are **double row sockets** on the main-board or backplane, fit a double row **right angled header strip** to position **J1** on the interface PCB. This takes up both rows of holes.

The header strips are pre-cut to the required size. Fit and solder one of the header strips as shown in the photos.

For a single row header



For a double row header



Fit and solder all **IC sockets**, **U1 to U15**. Observe the correct orientation with the notch matching the PCB.

There's a dot on one end of component **RN1** (the 10K SIL resistor array) – The dot should face towards the square surrounding the hole of **RN1** on the PCB.

Fit the fifteen **0.1uF ceramic disc capacitors** in to **C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16.**

Fit and solder the **34 way right angle locking IDC header** to the PCB at position **J2**. The connector should lay flat against the PCB.

Fit the **100uF electrolytic capacitor - C1** making sure the polarity is correct with respect to the small **"+"** sign on the board.

Fit and solder the **3 pin header strip** supplied in the kit at position **J3**.

Now assembly is complete, Inspect your work carefully for solder bridges before fitting the IC's into the IC sockets.

NOTE: Due to semiconductor supply shortages you may receive IC's from the following logic families, 74HC, 74HCT, 74ALS, 74F series. All of these will work perfectly in whole sets or mixed combinations and for most users this will be fine.

SETTING THE ADDRESS JUMPER

With the jumper at **J3** 

in the right position the decoded addresses repeat every other four like this:
80, 81, 82, 83..... 88, 89, 8A, 8B..... and so on up to B8, B9, BA, BB

OR

With the jumper at **J3** 

in the left position the decoded addresses repeat every other four like this:
….. 84, 85, 86, 87..... 8C, 8D, 8E, 8F..... and so on up to BC, BD, BE, BF

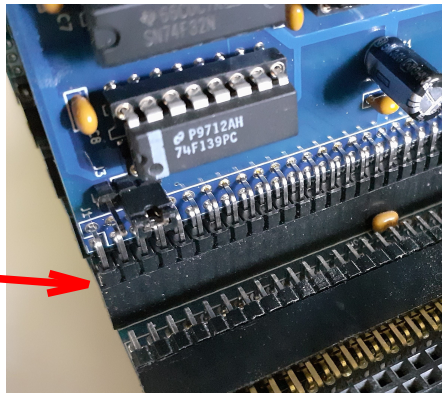
The blank spaces can be used to assign addresses to other I/O devices in a system unless two boards are used.

The alternating groups of four addresses is a good compromise between having a simpler logic design that takes up less PCB space and leaving some flexibility to add additional expansion boards. Two parallel port boards can be used at once taking up all the Z80 I/O address space between 0x80 and 0xBF. Set one board with jumper to the left and the other board with jumper to the right.

INSTALLATION TO A MAIN-BOARD

Inserting the PCB as shown with the board lining up at the left hand side of the connectors. There will be one empty space not used on the right hand side of the backplane.

Line up this side



PROGRAMMING THE PORTS

Port registers	Address jumper setting -	RIGHT	LEFT
PORT A control register		0x82	0c86
PORT A data register		0x83	0x87
PORT B control register		0x80	0x84
PORT B data register		0x81	0x85

Using Z80 assembler:

```
; PORT A can be set as either an 8 bit input port or an 8 bit output port.

        ; To set up PORT A as on output port.
                LD      A,      00h             3E      00              ; Only bit '0' is used.
                OUT     (82h),  A               D3      82              ; Set control register A to output mode.

        ; Writing data to PORT A.
                LD      A,      nn              3E      nn              ; Data 'nn' to be sent to PORT A.
                OUT     (83h),  A               D3      83              ; Write to PORT B data register.



        ; To set PORT A as an input port.
                LD      A, 01h                  3E      01              ; Only bit '0' is used.
                OUT     (82h),  A               D3      82              ; Set control register A to input mode.

        ; Reading data from PORT A.
                IN      A,      (83h)           DB      83              ; Read from PORT A data register.


; PORT B can have any of the 8 data lines set to inputs or outputs.

        ; To set up PORT B as all outputs.
                LD      A,      00h             3E      00              ; To set all 8 bits to outputs.
                OUT     (80h),  A               D3      80              ; Set control register B to '00000000'

        ; Writing data to PORT B
                LD      A,      nn              3E      nn              ; Data 'nn' to be sent to PORT B.
                OUT     (81),   A               D3      81              ; Write to PORT B data register.



        ; To set PORT B as all inputs.
                LD      A,      FFh             3E      FF              ; To set all 8 bits to inputs.
                OUT     (80h),  A               D3      80              ; Set control register B to '11111111'

                IN      A,      (81)            DB      81              ; Read from PORT B data register.



        ; To set PORT B with some bits as inputs and some bits as outputs.
                LD      A,      0Fh             3E      0F              ; To set D7 to D4 as outputs and D3 to D0 as inputs.
                OUT     (80),   A               D3      80              ; Set control register B to '00001111'

; Writing to PORT B  data register will affect only the bits set as outputs.
; When reading from PORT B data register, only the bits set as inputs will be valid data.
; The bits that are set as outputs will be undefined.

        ; After reading PORT B the undefined bits should be masked off with an instruction such as:-
                AND     0Fh                     E6      0F              ; Mask off the undefined high nibble in the Z80's
                                                                        ; register 'A'.
```