Pixie-16 Custom Firmware for ORNL

Prepared for:

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Document:	**Pixie-16 Custom Firmware for ORNL**		
Release Date:	12/01/2011	Version:	1.0
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REVISION HISTORY

12/01/2011:

Initial release.

1 Background

Dr. Krzysztof Rykaczewski at the Oak Ridge National Laboratory has purchased a custom firmware for a Pixie-16 data acquisition system. This firmware will be used for measuring positions in position sensitive single strip detectors during Super Heavy Experiments (SHE). The details of the custom firmware request are listed below:

For each pair of Pixie-16 inputs channel(n) and channel(n+1), a virtual channel(n') will be generated by summing ADC outputs of channel(n) and channel(n+1) to trigger data recording in channel(n) and channel(n+1) as well as the virtual channel itself. The virtual channel will have the pileup inspector activated and traces for channel(n) and channel(n+1) will be stored for all signals when pileup is detected in the virtual channel. This is essential to determine the positions of implantation and decay signal. Halting FIFOs in both channels n and n+1 should occur in the same time on condition of the trigger from virtual channel. For non-pileup signals, we will be collecting just energies and times plus the partial sums, in expectation, that from the partial sums we can determine the positions. We should preserve the "dead time" free operation, so after each pileup, we need to be able to detect normal signals instantaneously.

2 The Pixie-16 Custom Firmware

The operation of this Pixie-16 Rev-D ORNL SHE custom firmware is controlled by the DSP parameter ChanCSRA. In particular, a new bit, bit 18, was introduced to control whether trace should be captured or not when a single event is detected. If this bit is set to 1, a channel will record its trace even if its corresponding sum channel detects a single event. The following table shows the ChanCSRA bits applicable to this custom firmware.

ChanCSRA (Channel Control Status Register A)

Bit	Description	Value
0	Not used	0
1	Not used	0
2	**Good channel**	1
3	Not used	0
4	Not used	0
5	**Invert signal polarity if this bit is not set**	0
6	Not used	0
7	Not used	0
8	**Capture trace**	Always set to 1 in the firmware
9	**Capture QDC sums**	Always set to 1 in the firmware
10	**Enable CFD trigger**	0
11	Not used	0
12	Not used	0
13	Not used	0
14	**Switch between low and high analog gain**	0
15	Not used	0
16	Not used	0
17	Not used	0
18	**Enable trace capture for single event if this bit is set to 1**	0
19 : 31	Reserved	0

The trigger or energy filter parameters for the sum channel are the same as the channel(n) within a channel(n) and channel(n+1) group, for instance, in the channel 0 – 1 group of one Pixie-16 module, their sum channel will use parameters from channel 0, and in the channel 2 – 3 group, their sum channel will use parameters from channel 2, and so on.

3 The Custom Firmware Package

The custom firmware package is contained in file ***revd_ornl_she_firmware_12012011.zip***. It consists of the following folders and files:

\firmware\ fippixie16_revd_ornl_she_r21208.bin (Rev-D SHE variant FiPPI file)

\firmware\ syspixie16_revdgeneral_r20408.bin (latest Rev-D standard System FPGA file)

\dsp\Pixie16DSP_revd_ornl_she_r21201.ldr (Rev-D SHE variant DSP files)

\dsp\Pixie16DSP_revd_ornl_she_r21201.var

\dsp\Pixie16DSP_revd_ornl_she_r21201.lst

These custom firmware files can be used with the standard Pixie-16 Clib code, i.e. no special Clib code is required.

Please NOTE: these custom firmware files only support **list mode runs**. Please use standard Pixie-16 firmware files for MCA histogram runs.

4 Output Data Structure

Output data structure for the Pixie-16 ORNL SHE custom firmware system can be described as follows. Each event consists of data from the sum channel and the group of two neighboring channels. The sum channel outputs timestamp and energy (from the summed trace of two neighboring channels). For the group of two channels, there are three possible data outputs:

1) When pileup is detected in the sum channel, each channel will record timestamp, which is latched by the trigger in the sum channel, and trace, which is also recorded upon the detection of sum channel trigger;
2) When pileup is not detected in the sum channel, i.e. single event, each channel will record timestamp, which is latched by the trigger in the sum channel, and eight QDC sums;
3) When pileup is not detected in the sum channel, i.e. single event, but trace is also requested to be recorded (e.g. for diagnostic purpose), each channel will record timestamp, which is latched by the trigger in the sum channel, eight QDC sums, and trace.

The output data structure starts with data from the sum channel, which is followed by data from the 2-channel group. Please NOTE: the sum channel uses the same Chan #, SlotID, and CrateID as the first channel of each 2-channel group, i.e. for the channel 0 – 1 group of one Pixie-16 module, their sum channel will use Chan# = 0 as its identifier, and for the channel 2 – 3 group, their sum channel will use Chan# = 2 as its identifier, and so on.

4.1 Output data structure for pileup event

The following table shows the output data structure when pileup is detected in the sum channel.

<table>
<tr><th colspan="2">Index</th><th colspan="7">Data</th><th>Description</th></tr>
<tr><td rowspan="8">Sum Channel</td><td rowspan="2">0</td><td>[31]</td><td>[30]</td><td>[29:17]</td><td>[16:12]</td><td>[11:8]</td><td>[7:4]</td><td>[3:0]</td><td rowspan="2">Bits [3:0] – channel number; bits [7:4] – PXI slot number; bits [11:8] – PXI chassis number; bits [16:12] – header length; bits [29:17] – event length; bit [30] – ADC trace out of range flag (0 – in range; 1 – out of range); bit [31] – pileup flag (0 – single event; 1 – pileup event)</td></tr>
<tr><td>Pileup Flag</td><td>Out-of-range Flag</td><td>Event Length</td><td>Header Length</td><td>CrateID</td><td>SlotID</td><td>Chan#</td></tr>
<tr><td rowspan="2">1</td><td colspan="7">[31:0]</td><td rowspan="2">Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)</td></tr>
<tr><td colspan="7">EVTTIME_LO[31:0]</td></tr>
<tr><td rowspan="2">2</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event time (upper 16-bit of the 48-bit timestamp); Bits [31:16] – CFD fractional time × 65536 (0 if CFD trigger is not enabled)</td></tr>
<tr><td colspan="4">CFD Fractional Time</td><td colspan="3">EVTTIME_HI[15:0]</td></tr>
<tr><td rowspan="2">3</td><td colspan="5">[31:15]</td><td colspan="2">[14:0]</td><td rowspan="2">Bits [14:0] – energy of the summed signal; Bits [31:15] – not used (value set to 0)</td></tr>
<tr><td colspan="5">Not used (set to 0)</td><td colspan="2">Energy</td></tr>
<tr><td rowspan="10">Channel (n)</td><td rowspan="2">4</td><td>[31]</td><td>[30]</td><td>[29:17]</td><td>[16:12]</td><td>[11:8]</td><td>[7:4]</td><td>[3:0]</td><td rowspan="2">Bits [3:0] – channel number; bits [7:4] – PXI slot number; bits [11:8] – PXI chassis number; bits [16:12] – header length; bits [29:17] – event length; bit [30] – ADC trace out of range flag (0 – in range; 1 – out of range); bit [31] – pileup flag (0 – single event; 1 – pileup event)</td></tr>
<tr><td>Pileup Flag</td><td>Out-of-range Flag</td><td>Event Length</td><td>Header Length</td><td>CrateID</td><td>SlotID</td><td>Chan#</td></tr>
<tr><td rowspan="2">5</td><td colspan="7">[31:0]</td><td rowspan="2">Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)</td></tr>
<tr><td colspan="7">EVTTIME_LO[31:0]</td></tr>
<tr><td rowspan="2">6</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event time (upper 16-bit of the 48-bit timestamp); Bits [31:16] – not used (value set to 0)</td></tr>
<tr><td colspan="4">Not used (set to 0)</td><td colspan="3">EVTTIME_HI[15:0]</td></tr>
<tr><td rowspan="2">7</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – not used (value set to 0); Bits [31:15] – length of recorded trace (0 if no trace is recorded)</td></tr>
<tr><td colspan="4">Trace Length</td><td colspan="3">Not used (set to 0)</td></tr>
<tr><td rowspan="2">8</td><td>[31:28]</td><td colspan="2">[27:16]</td><td>[15:12]</td><td colspan="3">[11:0]</td><td rowspan="2">Packing of ADC Data #0 and #1</td></tr>
<tr><td>Not used</td><td colspan="2">ADC Data #1</td><td>Not used</td><td colspan="3">ADC Data #0</td></tr>
<tr><td rowspan="2">9</td><td>[31:28]</td><td colspan="2">[27:16]</td><td>[15:12]</td><td colspan="3">[11:0]</td><td rowspan="2">Packing of ADC Data #2 and #3</td></tr>
<tr><td>Not used</td><td colspan="2">ADC Data #3</td><td>Not used</td><td colspan="3">ADC Data #2</td></tr>
<tr><td>…</td><td colspan="7">…</td><td>Packing of ADC Data …</td></tr>
</table>

<table>
<tr><td rowspan="10">Channel (n+1)</td><td rowspan="2">N</td><td>[31]</td><td>[30]</td><td>[29:17]</td><td>[16:12]</td><td>[11:8]</td><td>[7:4]</td><td>[3:0]</td><td rowspan="2">Bits [3:0] – channel number; bits [7:4] – PXI slot number; bits [11:8] – PXI chassis number; bits [16:12] – header length; bits [29:17] – event length; bit [30] – ADC trace out of range flag (0 – in range; 1 – out of range); bit [31] – pileup flag (0 – single event; 1 – pileup event)</td></tr>
<tr><td>Pileup Flag</td><td>Out-of-range Flag</td><td>Event Length</td><td>Header Length</td><td>CrateID</td><td>SlotID</td><td>Chan#</td></tr>
<tr><td rowspan="2">N+1</td><td colspan="7">[31:0]</td><td rowspan="2">Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)</td></tr>
<tr><td colspan="7">EVTTIME_LO[31:0]</td></tr>
<tr><td rowspan="2">N+2</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event time (upper 16-bit of the 48-bit timestamp); Bits [31:16] – not used (value set to 0)</td></tr>
<tr><td colspan="4">Not used (set to 0)</td><td colspan="3">EVTTIME_HI[15:0]</td></tr>
<tr><td rowspan="2">N+3</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – not used (value set to 0); Bits [31:15] – length of recorded trace (0 if no trace is recorded)</td></tr>
<tr><td colspan="4">Trace Length</td><td colspan="3">Not used (set to 0)</td></tr>
<tr><td rowspan="2">N+4</td><td>[31:28]</td><td colspan="3">[27:16]</td><td>[15:12]</td><td colspan="2">[11:0]</td><td rowspan="2">Packing of ADC Data #0 and #1</td></tr>
<tr><td>Not used</td><td colspan="3">ADC Data #1</td><td>Not used</td><td colspan="2">ADC Data #0</td></tr>
<tr><td rowspan="2">N+5</td><td>[31:28]</td><td colspan="3">[27:16]</td><td>[15:12]</td><td colspan="2">[11:0]</td><td rowspan="2">Packing of ADC Data #2 and #3</td></tr>
<tr><td>Not used</td><td colspan="3">ADC Data #3</td><td>Not used</td><td colspan="2">ADC Data #2</td></tr>
<tr><td>…</td><td colspan="7">…</td><td>Packing of ADC Data …</td></tr>
</table>

4.2 Output data structure for single event (trace capture is NOT requested)

The following table shows the output data structure when single event is detected in the sum channel and trace capture is not requested.

<table>
<tr><th colspan="2">Index</th><th colspan="7">Data</th><th>Description</th></tr>
<tr><td rowspan="8">Sum Channel</td><td rowspan="2">0</td><td>[31]</td><td>[30]</td><td>[29:17]</td><td>[16:12]</td><td>[11:8]</td><td>[7:4]</td><td>[3:0]</td><td rowspan="2">Bits [3:0] – channel number; bits [7:4] – PXI slot number; bits [11:8] – PXI chassis number; bits [16:12] – header length; bits [29:17] – event length; bit [30] – ADC trace out of range flag (0 – in range; 1 – out of range); bit [31] – pileup flag (0 – single event; 1 – pileup event)</td></tr>
<tr><td>Pileup Flag</td><td>Out-of-range Flag</td><td>Event Length</td><td>Header Length</td><td>CrateID</td><td>SlotID</td><td>Chan#</td></tr>
<tr><td rowspan="2">1</td><td colspan="7">[31:0]</td><td rowspan="2">Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)</td></tr>
<tr><td colspan="7">EVTTIME_LO[31:0]</td></tr>
<tr><td rowspan="2">2</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event time (upper 16-bit of the 48-bit timestamp); Bits [31:16] – CFD fractional time × 65536 (0 if CFD trigger is not enabled)</td></tr>
<tr><td colspan="4">CFD Fractional Time</td><td colspan="3">EVTTIME_HI[15:0]</td></tr>
<tr><td rowspan="2">3</td><td colspan="5">[31:15]</td><td colspan="2">[14:0]</td><td rowspan="2">Bits [14:0] – energy of the summed signal; Bits [31:15] – not used (value set to 0)</td></tr>
<tr><td colspan="5">Not used (set to 0)</td><td colspan="2">Energy</td></tr>
<tr><td rowspan="8">Channel (n)</td><td rowspan="2">4</td><td>[31]</td><td>[30]</td><td>[29:17]</td><td>[16:12]</td><td>[11:8]</td><td>[7:4]</td><td>[3:0]</td><td rowspan="2">Bits [3:0] – channel number; bits [7:4] – PXI slot number; bits [11:8] – PXI chassis number; bits [16:12] – header length; bits [29:17] – event length; bit [30] – ADC trace out of range flag (0 – in range; 1 – out of range); bit [31] – pileup flag (0 – single event; 1 – pileup event)</td></tr>
<tr><td>Pileup Flag</td><td>Out-of-range Flag</td><td>Event Length</td><td>Header Length</td><td>CrateID</td><td>SlotID</td><td>Chan#</td></tr>
<tr><td rowspan="2">5</td><td colspan="7">[31:0]</td><td rowspan="2">Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)</td></tr>
<tr><td colspan="7">EVTTIME_LO[31:0]</td></tr>
<tr><td rowspan="2">6</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event time (upper 16-bit of the 48-bit timestamp); Bits [31:16] – not used (value set to 0)</td></tr>
<tr><td colspan="4">Not used (set to 0)</td><td colspan="3">EVTTIME_HI[15:0]</td></tr>
<tr><td rowspan="2">7</td><td colspan="4">[31:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – not used (value set to 0); Bits [31:15] – length of recorded trace (0 if no trace is recorded)</td></tr>
<tr><td colspan="4">Trace Length</td><td colspan="3">Not used (set to 0)</td></tr>
<tr><td>8</td><td colspan="7">QDC sum #0 [31:0]</td><td>8 QDC sums</td></tr>
</table>

	9	QDC sum #1 [31:0]							
	10	QDC sum #2 [31:0]							
	11	QDC sum #3 [31:0]							
	12	QDC sum #4 [31:0]							
	13	QDC sum #5 [31:0]							
	14	QDC sum #6 [31:0]							
	15	QDC sum #7 [31:0]							
Channel (n+1)	16	[31]	[30]	[29:17]	[16:12]	[11:8]	[7:4]	[3:0]	**Bits [3:0]** – channel number; bits [7:4] – PXI slot number; **bits [11:8]** – PXI chassis number; **bits [16:12]** – header length; **bits [29:17]** – event length; **bit [30]** – ADC trace out of range flag (0 – in range; 1 – out of range); **bit [31]** – pileup flag (0 – single event; 1 – pileup event)
		Pileup Flag	Out-of-range Flag	Event Length	Header Length	CrateID	SlotID	Chan#	
	17	[31:0]							Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)
		EVTTIME_LO[31:0]							
	18	[31:16]				[15:0]			**Bits [15:0]** – event time (upper 16-bit of the 48-bit timestamp); **Bits [31:16]** – not used (value set to 0)
		Not used (set to 0)				EVTTIME_HI[15:0]			
	19	[31:16]				[15:0]			**Bits [15:0]** – not used (value set to 0); **Bits [31:15]** – length of recorded trace (0 if no trace is recorded)
		Trace Length				Not used (set to 0)			
	20	QDC sum #0 [31:0]							8 QDC sums
	21	QDC sum #1 [31:0]							
	22	QDC sum #2 [31:0]							
	23	QDC sum #3 [31:0]							
	24	QDC sum #4 [31:0]							
	25	QDC sum #5 [31:0]							
	26	QDC sum #6 [31:0]							
	27	QDC sum #7 [31:0]							

4.3 Output data structure for single event (trace capture is requested)

The following table shows the output data structure when single event is detected in the sum channel and trace capture is requested.

Index		Data							Description
Sum Channel	0	[31]	[30]	[29:17]	[16:12]	[11:8]	[7:4]	[3:0]	**Bits [3:0]** – channel number; bits [7:4] – PXI slot number; **bits [11:8]** – PXI chassis number; **bits [16:12]** – header length; **bits [29:17]** – event length; **bit [30]** – ADC trace out of range flag (0 – in range; 1 – out of range); **bit [31]** – pileup flag (0 – single event; 1 – pileup event)
		Pileup Flag	Out-of-range Flag	Event Length	Header Length	CrateID	SlotID	Chan#	
	1	[31:0]							Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)
		EVTTIME_LO[31:0]							
	2	[31:16]				[15:0]			**Bits [15:0]** – event time (upper 16-bit of the 48-bit timestamp); **Bits [31:16]** – CFD fractional time × 65536 (0 if CFD trigger is not enabled)
		CFD Fractional Time				EVTTIME_HI[15:0]			
	3	[31:15]				[14:0]			**Bits [14:0]** – energy of the summed signal; **Bits [31:15]** – not used (value set to 0)
		Not used (set to 0)				Energy			
Channel (n)	4	[31]	[30]	[29:17]	[16:12]	[11:8]	[7:4]	[3:0]	**Bits [3:0]** – channel number; bits [7:4] – PXI slot number; **bits [11:8]** – PXI chassis number; **bits [16:12]** – header length; **bits [29:17]** – event length; **bit [30]** – ADC trace out of range flag (0 – in range; 1 – out of range); **bit [31]** – pileup flag (0 – single event; 1 – pileup event)
		Pileup Flag	Out-of-range Flag	Event Length	Header Length	CrateID	SlotID	Chan#	
	5	[31:0]							Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)
		EVTTIME_LO[31:0]							
	6	[31:16]				[15:0]			**Bits [15:0]** – event time (upper 16-bit of the 48-bit timestamp); **Bits [31:16]** – not used (value set to 0)
		Not used (set to 0)				EVTTIME_HI[15:0]			
	7	[31:16]				[15:0]			**Bits [15:0]** – not used (value set to 0); **Bits [31:15]** – length of recorded trace (0 if no trace is recorded)
		Trace Length				Not used (set to 0)			
	8	QDC sum #0 [31:0]							8 QDC sums

	9	QDC sum #1 [31:0]						
	10	QDC sum #2 [31:0]						
	11	QDC sum #3 [31:0]						
	12	QDC sum #4 [31:0]						
	13	QDC sum #5 [31:0]						
	14	QDC sum #6 [31:0]						
	15	QDC sum #7 [31:0]						
	16	[31:28]	[27:16]		[15:12]	[11:0]		Packing of ADC Data #0 and #1
		Not used	ADC Data #1		Not used	ADC Data #0		
	17	[31:28]	[27:16]		[15:12]	[11:0]		Packing of ADC Data #2 and #3
		Not used	ADC Data #3		Not used	ADC Data #2		
	…	…						Packing of ADC Data …
Channel (n+1)	N	[31]	[30]	[29:17]	[16:12]	[11:8]	[7:4]	[3:0]	**Bits [3:0]** – channel number; bits [7:4] – PXI slot number; **bits [11:8]** – PXI chassis number; **bits [16:12]** – header length; **bits [29:17]** – event length; **bit [30]** – ADC trace out of range flag (0 – in range; 1 – out of range); **bit [31]** – pileup flag (0 – single event; 1 – pileup event)
		Pileup Flag	Out-of-range Flag	Event Length	Header Length	CrateID	SlotID	Chan#	
	N+1	[31:0]							Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger in the sum channel)
		EVTTIME_LO[31:0]							
	N+2	[31:16]			[15:0]				**Bits [15:0]** – event time (upper 16-bit of the 48-bit timestamp); **Bits [31:16]** – not used (value set to 0)
		Not used (set to 0)			EVTTIME_HI[15:0]				
	N+3	[31:16]			[15:0]				**Bits [15:0]** – not used (value set to 0); **Bits [31:15]** – length of recorded trace (0 if no trace is recorded)
		Trace Length			Not used (set to 0)				
	N+4	QDC sum #0 [31:0]							8 QDC sums
	N+5	QDC sum #1 [31:0]							
	N+6	QDC sum #2 [31:0]							
	N+7	QDC sum #3 [31:0]							
	N+8	QDC sum #4 [31:0]							
	N+9	QDC sum #5 [31:0]							
	N+10	QDC sum #6 [31:0]							
	N+11	QDC sum #7 [31:0]							
	N+12	[31:28]	[27:16]		[15:12]	[11:0]			Packing of ADC Data #0 and #1
		Not used	ADC Data #1		Not used	ADC Data #0			

	N+13	[31:28]	[27:16]	[15:12]	[11:0]	Packing of ADC Data #2 and #3
		Not used	ADC Data #3	Not used	ADC Data #2	
	…	…				Packing of ADC Data …