Pixie-16 Setup Guide for the VANDLE Detector System

Document:	**Pixie-16 Setup Guide for the VANDLE Detector System**		
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REVISION HISTORY

7/22/2011:

Initial release.

2/6/2012:

Added section 2 “VANDLE Trigger Setup”.

10/10/2014:

Changed trigger configuration parameter settings to accommodate the new requirement for beta detectors pairwise coincidence.

Included instructions to select one of the three types of global validation trigger for either VANDLE or MoNA type of experiments.

1 Crate/Pixie-16 Modules Setup

The Pixie-16 system for reading out the VANDLE detector array consists of two PXI 14-slot 6U crates, 26 Pixie-16 modules, and two Pixie-16 Rear-IO trigger boards that connect the two crates together using Category 6 Ethernet cables. The following sections described how to install the hardware and how to set the jumpers on the Pixie-16 modules and trigger boards.

1.1 Installation of Pixie-16 Modules

The 26 Pixie-16 modules can be installed in two 14-slot Pixie-16 crates, #1 and #2, each with 13 Pixie-16 modules (one slot in each crate is taken by the controller). For clock distribution purpose, we call crate #1 the Master crate, where the system-wide global clock for all Pixie-16 modules is originated and crate #2 the Slave crate, which receives the global clock from the Master crate.

The Pixie-16 module installed in Slot 2 of the Master crate is designated as the System Director Module, whose local 50 MHz clock crystal will act as the source of the system-wide global clock. The Pixie-16 module installed in Slot 2 of the Slave crate is called the crate Master module, which is responsible for receiving the global clock from the Master crate and sending such clock to all modules in that crate through length-matched traces on the backplane. The System Director Module is also responsible for sending the global clock to all modules in the Master crate, so it is also a crate Master module. Other modules in these two crates are regular modules.

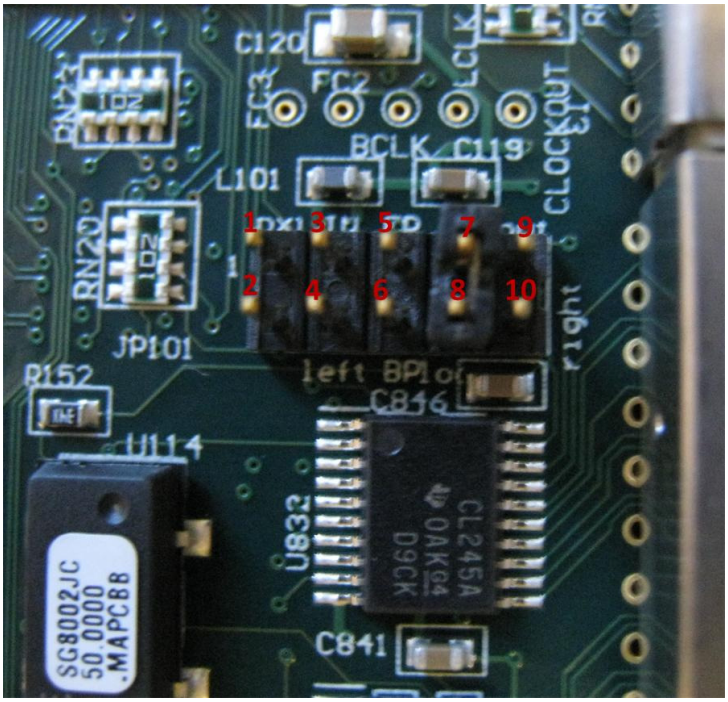
Crate #	**1**				
Slot #	**2**	**3**	···	**13**	**14**
Modules	System Director Module / Crate Master Module	Regular Module	···	Regular Module	Regular Module
Crate #	**2**				
Slot #	**2**	**3**	···	**13**	**14**
Modules	Crate Master Module	Regular Module	···	Regular Module	Regular Module

1.2 Clock Jumper (JP101) Settings on the Pixie-16 Modules

For all Pixie-16 modules in the two crates to use the same global clock, the clock jumper (JP101) in all modules should be set properly. The following table shows the jumper settings for the three types of modules that are described in the previous section.

System Director Module	Connect pins 1 and 3, 4 and 6, 8 and 10.
Crate Master Module	Connect pins 1 and 3, 4 and 6.
Regular Module	Connect pins 1 and 3.

To help locate the pins on JP101, the following picture shows the numbering of these pins.



1.3 Jumper Settings on the Trigger Boards

1.3.1 Trigger board #1

Trigger board #1 is installed in the rear slot #2 of crate #1. The rear slot #2 is located at the back of the crate and is at the direct opposite side of the front slot #2, which is located at the front of the crate. Care should be taken when installing the trigger board into the rear slot #2 by avoiding bending any pins of the rear side of the backplane. Please note pins 1, 2, and 3 for JP100-105 are counted from the right to the left. A tiny '1' label is painted on the right hand side of JP100-105, indicating pin 1.

JP1	Connect pins 1 and 2 for "P16"
JP20	Connect pins 2 and 3, 6 and 7
JP40	Connect pins 2 and 3, 6 and 7
JP60	Connect pins 1 and 2, 7 and 8
JP21	Connect pins 2 and 3
JP41	Connect pins 2 and 3
JP61	Connect pins 1 and 2
JP100	Connect pins 2 and 3 (connect to J4)
JP101	Connect pins 2 and 3 (connect to J4)
JP102	Connect pins 2 and 3 (connect to J4)
JP103	Connect pins 2 and 3 (connect to J4)
JP104	Connect pins 2 and 3 (connect to J4)
JP105	Connect pins 2 and 3 (connect to J4)

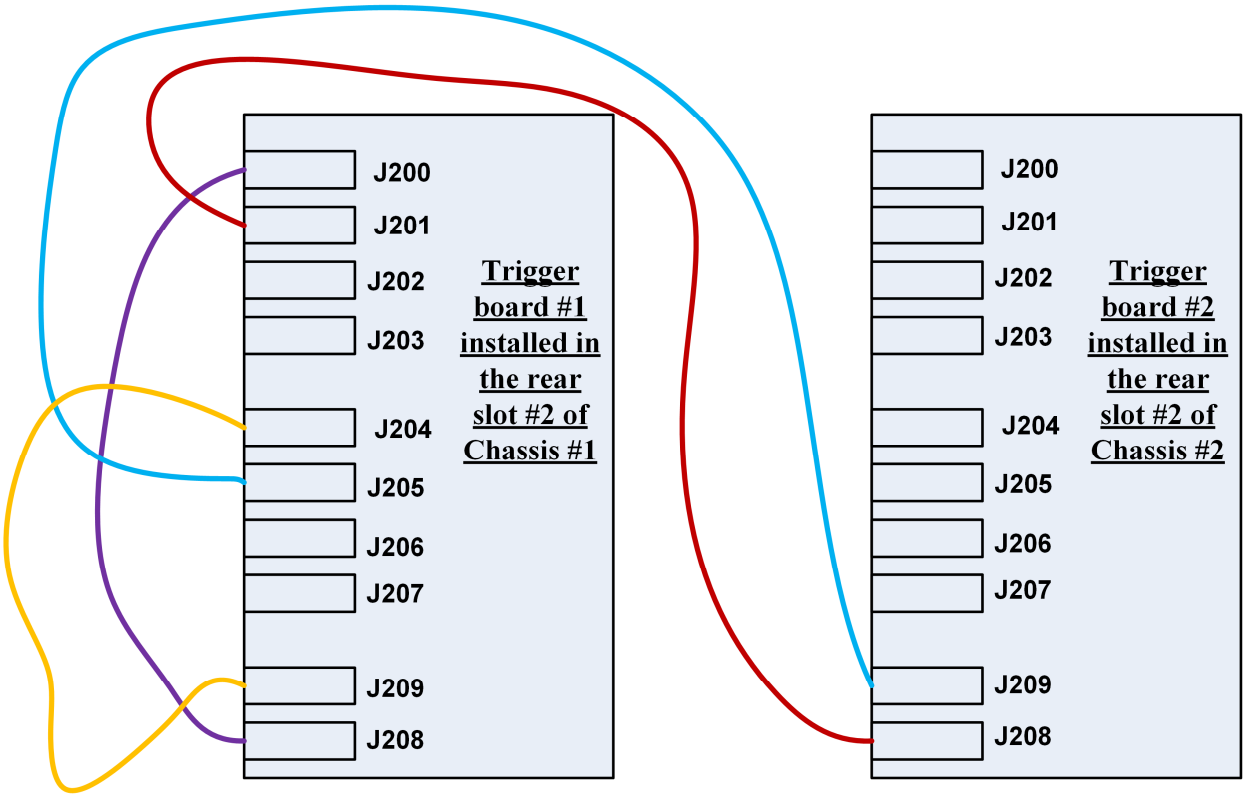
1.3.2 Trigger board #2

Trigger board #2 is installed in the rear slot #2 of crate #2. Please note pins 1, 2, and 3 for JP100-105 are counted from the right to the left.

JP1	Connect pins 2 and 3 for "loc"
JP20	Connect pins 1 and 2, 7 and 8
JP40	Connect pins 1 and 2, 7 and 8
JP60	Connect pins 2 and 3, 6 and 7
JP21	Don't connect any pin
JP41	Don't connect any pin
JP61	Connect pins 1 and 2
JP100	Connect pins 2 and 3 (connect to J4)
JP101	Connect pins 2 and 3 (connect to J4)
JP102	Connect pins 2 and 3 (connect to J4)
JP103	Connect pins 2 and 3 (connect to J4)
JP104	Connect pins 2 and 3 (connect to J4)
JP105	Connect pins 2 and 3 (connect to J4)

1.4 Rear I/O Trigger Boards Cable Connection

The following figure shows the cable connections from the Master crate to the Slave crate. Please NOTE: All connection cables are Category 6 cables and shall have the exactly same length.



Trigger boards setup for a 2-crate Pixie-16 System

2 VANDLE Trigger Setup

2.1 Detector connection restrictions

To facilitate the creation of VANDLE pairwise coincidence trigger, always connect a VANDLE bar's two ends to two consecutive Pixie-16 module channels, e.g. 0/1, 2/3, 4/5, etc. Also, always connect beta detectors to channels of the System Director Module. When pairwise coincidence trigger is also needed for the beta detectors, connect each pair of beta detectors to two consecutive Pixie-16 module channels.

For the example shown below to illustrate the appropriate settings for a few DSP parameters, we assume the System Director Module is the module #0 installed in slot #2 of crate #1.

Module Number	**0**	**1**	**2**	**3**	**4**	**5**	**6**
Slot Number	2	3	4	5	6	7	8
Accepted signals	beta, VANDLE	VANDLE	VANDLE	VANDLE	VANDLE	VANDLE	VANDLE

Module Number	**7**	**8**	**9**	**10**	**11**	**12**
Slot Number	9	10	11	12	13	14
Accepted signals	VANDLE	VANDLE	VANDLE	VANDLE	VANDLE	VANDLE

2.2 Trigger configurations

The original VANDLE detector system's global validation trigger is the logic AND of VANDLE bars' pairwise coincidence triggers and beta detectors' OR trigger. In a subsequent extension of the VANDLE system to the Modular Neutron Array (MoNA) at the National Superconducting Cyclotron Laboratory (NSCL), the new global validation trigger is the result of the following logic: (OR of Timing Detectors Triggers) AND (OR of Valid Detectors Triggers) AND (OR of VANDLE Pairwise Coincidence Triggers).

Recently, new beta trigger detectors were developed for VANDLE. These new beta trigger detectors follow similar philosophy as VANDLE, namely, "left-right" coincidence is required for 4 of these beta detectors for a total of 8 channels. An "OR" of those signals would then need to be in coincidence with the rest of VANDLE pairwise coincidences in order to generate the global validation trigger. Therefore, the new VANDLE detector system requires the following logic for the global validation trigger: (OR of Beta Pairwise Coincidence Triggers) AND (OR of VANDLE Pairwise Coincidence Triggers).

The latest VANDLE firmware supports all three types of global validation trigger:

a) (OR of Beta Detectors Triggers) **AND** (OR of VANDLE Pairwise Coincidence Triggers)
b) (OR of Timing Detectors Triggers) **AND** (OR of Valid Detectors Triggers) **AND** (OR of VANDLE Pairwise Coincidence Triggers)

c) (OR of Beta Pairwise Coincidence Triggers) **AND** (OR of VANDLE Pairwise Coincidence Triggers).

The selection of which type of global validation trigger to use is done through setting appropriate bits of the DSP parameter TrigConfig3, as detailed below.

To tell the system whether a Pixie-16 channel is connected to a VANDLE detector or beta detector, set appropriate bits of user module parameter TrigConfig2 (DSP parameter TrigConfig[2]) and TrigConfig3 (DSP parameter TrigConfig[3]) accordingly. Other bits of these two parameters are used to control the outputting of VANDLE and Beta triggers to the Pixie-16 crate backplane, select test signals output, or choose beta validation trigger source.

Bits of TrigConfig2	**Value & Description**
0	Select detector type for Channel 0: 0 – Valid detector; 1 – BETA detector
1	Select detector type for Channel 1: 0 – Valid detector; 1 – BETA detector
2	Select detector type for Channel 2: 0 – Valid detector; 1 – BETA detector
3	Select detector type for Channel 3: 0 – Valid detector; 1 – BETA detector
4	Select detector type for Channel 4: 0 – Valid detector; 1 – BETA detector
5	Select detector type for Channel 5: 0 – Valid detector; 1 – BETA detector
6	Select detector type for Channel 6: 0 – Valid detector; 1 – BETA detector
7	Select detector type for Channel 7: 0 – Valid detector; 1 – BETA detector
8	Select detector type for Channel 8: 0 – Valid detector; 1 – BETA detector
9	Select detector type for Channel 9: 0 – Valid detector; 1 – BETA detector
10	Select detector type for Channel 10: 0 – Valid detector; 1 – BETA detector
11	Select detector type for Channel 11: 0 – Valid detector; 1 – BETA detector
12	Select detector type for Channel 12: 0 – Valid detector; 1 – BETA detector
13	Select detector type for Channel 13: 0 – Valid detector; 1 – BETA detector
14	Select detector type for Channel 14: 0 – Valid detector; 1 – BETA detector
15	Select detector type for Channel 15: 0 – Valid detector; 1 – BETA detector
[31:16]	Reserved

Bits of TrigConfig3	**Value & Description**
0	Select detector type for Channel 0: 0 – VANDLE; 1 – BETA or Valid
1	Select detector type for Channel 1: 0 – VANDLE; 1 – BETA or Valid
2	Select detector type for Channel 2: 0 – VANDLE; 1 – BETA or Valid
3	Select detector type for Channel 3: 0 – VANDLE; 1 – BETA or Valid
4	Select detector type for Channel 4: 0 – VANDLE; 1 – BETA or Valid
5	Select detector type for Channel 5: 0 – VANDLE; 1 – BETA or Valid
6	Select detector type for Channel 6: 0 – VANDLE; 1 – BETA or Valid
7	Select detector type for Channel 7: 0 – VANDLE; 1 – BETA or Valid
8	Select detector type for Channel 8: 0 – VANDLE; 1 – BETA or Valid
9	Select detector type for Channel 9: 0 – VANDLE; 1 – BETA or Valid
10	Select detector type for Channel 10: 0 – VANDLE; 1 – BETA or Valid
11	Select detector type for Channel 11: 0 – VANDLE; 1 – BETA or Valid
12	Select detector type for Channel 12: 0 – VANDLE; 1 – BETA or Valid
13	Select detector type for Channel 13: 0 – VANDLE; 1 – BETA or Valid
14	Select detector type for Channel 14: 0 – VANDLE; 1 – BETA or Valid

<table>
<tr><td>15</td><td colspan="7">Select detector type for Channel 15: 0 – VANDLE; 1 – BETA or Valid</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>16</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #0</td></tr>
<tr><td>17</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #1</td></tr>
<tr><td>18</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #2</td></tr>
<tr><td>19</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #3</td></tr>
<tr><td>20</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #4</td></tr>
<tr><td>21</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #5</td></tr>
<tr><td>22</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #6</td></tr>
<tr><td>23</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #7</td></tr>
<tr><td>24</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #8</td></tr>
<tr><td>25</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #9</td></tr>
<tr><td>26</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #10</td></tr>
<tr><td>27</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #11</td></tr>
<tr><td>28</td><td colspan="7">Enable (1) or disable (0) sending this module's OR of 8 VANDLE pairwise coincidence triggers to backplane line #12</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>[30:29]</td><td colspan="7">Select Beta validation trigger source:
=00: OR of Beta pairwise coincidence triggers
=01: AND of (OR of Beta single triggers) and (OR of Valid single triggers)
=10: OR of Beta single triggers
=11: OR of Beta pairwise coincidence triggers</td></tr>
<tr><td rowspan="6">31</td><td rowspan="6">0</td><td>TEST0</td><td>FTRIG_DELAY</td><td rowspan="6">1</td><td>TEST0</td><td>FT[0]</td></tr>
<tr><td>TEST1</td><td>FTRIG_VAL</td><td>TEST1</td><td>FT[1]</td></tr>
<tr><td>TEST2</td><td>GLBETRIG_CE</td><td>TEST2</td><td>FT[2]</td></tr>
<tr><td>TEST3</td><td>CHANETRIG_CE</td><td>TEST3</td><td>VANDLE_PWA_OR</td></tr>
<tr><td>TEST4</td><td>VANDLE_PWA[0]</td><td>TEST4</td><td>BETA_PWA_TRIG_OR</td></tr>
<tr><td>TEST5</td><td>GLOBAL_TRIG</td><td>TEST5</td><td>BETA_VALIDATION_TRIG</td></tr>
</table>

Each module first makes its local VANDLE pairwise coincidence triggers (maximum 8 pairwise coincidence triggers if all of its 16 channels are connected to VANDLE detectors). It then makes an OR of all of those local VANDLE pairwise coincidence triggers. To output such VANDLE OR trigger to the backplane so that the crate Master module can see such information, set bits 16 to 28 of user module parameter TrigConfig3 (DSP parameter TrigConfig[3]) accordingly. **NOTE: Each module should set one and ONLY one bit of bits 16 to 28 of TrigConfig3 to 1, i.e. only select one backplane line to output its OR of 8 VANDLE pairwise coincidence triggers.**

After collecting such VANDLE OR triggers from all modules in the crate, the crate Master module then makes an OR of all of those VANDLE OR triggers. We call such OR trigger as the crate level VANDLE_PWA_OR trigger (i.e. VANDLE pairwise AND OR). In a multi-crate system, such VANDLE_PWA_OR trigger is sent from the slave crates to the master crate through the trigger cards, and the System Director Module in the master crate makes a global OR of all the VANDLE_PWA_OR triggers.

In the System Director Module to which the beta detectors are connected, the following triggers are also made:

1) OR of Beta pairwise coincidence triggers (BETA_PWA_TRIG_OR)
2) OR of Beta (timing detectors) single triggers
3) OR of Valid single triggers
4) AND of (OR of Beta single triggers) and (OR of Valid single triggers)

Based on the selection of the source for the beta validation trigger (BETA_VALIDATION_TRIG) by the user, the System Director Module generates the global validation trigger (GLOBAL_TRIG) by making an AND of the VANDLE_PWA_OR triggers with the beta validation trigger, and outputs such global trigger to all the modules in the system so that they can use it to validate its local data acquisition.

The setup of trigger parameters TrigConfig[2] and TrigConfig[3] largely depends on how the VANDLE and beta detectors are connected to the Pixie-16 modules. However, for bits [28:16] of TrigConfig[3] we must set only one bit to 1 while keeping all other bits at 0 for modules in either a single crate system or multi-crate system.

TrigConfig[3]		**Module Number**						
		0	**1**	**2**	**3**	**4**	**5**	**6**
[28:16]	Output a module's OR of VANDLE pairwise triggers to backplane	Set Bit **16** to 1	Set Bit **17** to 1	Set Bit **18** to 1	Set Bit **19** to 1	Set Bit **20** to 1	Set Bit **21** to 1	Set Bit **22** to 1

TrigConfig[3]		**Module Number**					
		7	**8**	**9**	**10**	**11**	**12**
[28:16]	Output a module's OR of VANDLE pairwise triggers to backplane	Set Bit **23** to 1	Set Bit **24** to 1	Set Bit **25** to 1	Set Bit **26** to 1	Set Bit **27** to 1	Set Bit **28** to 1

2.3 Setup for external trigger or external clock timestamps requirement

To require any Pixie-16 channel be gated with a pairwise coincidence trigger (either VANDLE detectors or beta detectors), set bit 13 of DSP parameter ChanCSRA to 1 (i.e. require channel trigger for validation). To require any Pixie-16 channel be gated with the global validation trigger, set bit 11 of DSP parameter ChanCSRA to 1 (i.e. require global trigger for validation). NOTE, for beta channels, bit 13 of ChanCSRA should be set to 1 if beta channels require pairwise coincidence, but should be set to 0 if no beta pairwise coincidence is required.

To enable recording of external clock timestamps in a channel's event header, set bit 21 of ChanCSRA to 1 in such a channel. This is required for the MoNA experiments where an external ~20 MHz clock signal is input to the System Director Module's front panel. This can be done by

setting bit 21 of ChanCSRA of Channel #0 of the System Director Module to 1 while keeping all other channels' bit 21 of ChanCSRA to 0. Thus only Channel #0 of System Director Module will record the external clock timestamps in its event header.

Channel Control Register A (CHANCSRA)

Bit name	Bit #	Description
CCSRA_FTRIGSEL	0	Fast trigger selection (local FiPPI trigger vs. external fast trigger from System FPGA)
CCSRA_EXTTRIGSEL	1	Module validation signal selection (module validation trigger from System FPGA vs. module GATE from front panel)
CCSRA_GOOD	2	Good channel
CCSRA_CHANTRIGSEL	3	Channel validation signal selection (channel validation trigger from System FPGA vs. channel GATE from front panel)
CCSRA_SYNCDATAACQ	4	Block data acquisition if trace or header DPMs are full
CCSRA_POLARITY	5	Input signal polarity control
CCSRA_VETOENA	6	Enable channel trigger veto
CCSRA_HISTOE	7	Histograms energy in the on-chip MCA
CCSRA_TRACEENA	8	Trace capture and associated header data
CCSRA_QDCENA	9	QDC summing and associated header data
CCSRA_CFDMODE	10	CFD for real time, trace capture and QDC capture
CCSRA_GLOBTRIG	11	Require module validation trigger
CCSRA_ESUMSENA	12	Record raw energy sums and baseline in event header
CCSRA_CHANTRIG	13	Require channel validation trigger
CCSRA_ENARELAY	14	Control input relay: 1: connect, 0: disconnect
CCSRA_PILEUPCTRL	15	Control normal pileup rejection
CCSRA_INVERSEPILEUP	16	Control Inverse pileup rejection
CCSRA_ENAENERGYCUT	17	Enable "no traces fro large pulses" feature
CCSRA_GROUPTRIGSEL	18	Group trigger selection (local FiPPI trigger vs. external group trigger from System FPGA)
CCSRA_CHANVETOSEL	19	Channel veto selection (front panel channel GATE vs. channel validation trigger)
CCSRA_MODVETOSEL	20	Module veto selection (front panel module GATE vs. module validation trigger)
CCSRA_EXTTSENA	21	Recording of external clock timestamps in event header - 1: enable; 0: disable
reserved	31:22	

Please note: Channel Control Register B (CHANCSRB) is not being used currently. Their values can be set to 0 in all modules.

2.4 Setup for System Director and Crate Master Modules

A few bits of DSP parameter Module Control Register B (ModCSRB) should be set appropriately for the System Director module and the crate Master module in either the single crate system or multi-crate system.

2.4.1 Single crate system

Module Type	Bits of ModCSRB				Value of ModCSRB
	0	**4**	**6**	**11**	
System Director Module and also Crate Master Module in slot #2	1	0	1	0	0x41
Regular Modules in other slots	0	0	0	0	0x00

2.4.2 Two-crate system

Module Type	Bits of ModCSRB				Value of ModCSRB
	0	4	6	11	
System Director Module and also Crate Master Module in slot #2 of crate #1	1	1	1	1	0x851
Crate Master Module in slot #2 of crate #2	1	0	1	1	0x841
Regular Modules in all other slots of either crate #1 or crate #2	0	0	0	1	0x800

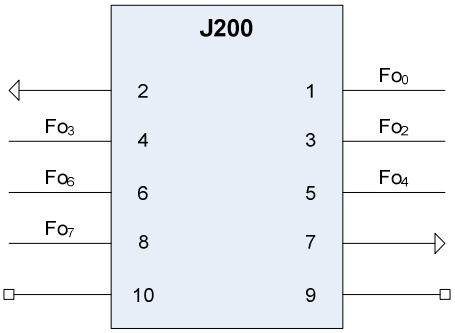
Module Control Register B (MODCSRB)

Bit name	Bit #	Description
MODCSRB_CPLDPULLUP	0	Control pullups for PXI trigger lines on the backplane through CPLD
reserved	3:1	
MODCSRB_DIRMOD	4	Set this module as the Director module
reserved	5	
MODCSRB_CHASSISMASTER	6	Set this module as chassis master
MODCSRB_GFTSEL	7	Select global fast trigger source (external validation trigger vs. external fast trigger, in case these two signals are swapped at the front panel)
MODCSRB_ETSEL	8	Select external trigger source (external fast trigger vs. external validation trigger, in case these two signals are swapped at the front panel)
reserved	9	
MODCSRB_INHIBITENA	10	Control the use of external INHIBIT signal
MODCSRB_MULTCRATES	11	Distribute clock and triggers in multiple crates
MODCSRB_SORTEVENTS	12	Sort events based on their timestamps
MODCSRA_BKPLFASTTRIG	13	Enable connection of fast triggers to backplane (only one module can enable this option in each PCI bus segment of a crate)
reserved	31:14	

Please note: Module Control Register A (MODCSRA) is not being used currently. Their values can be set to 0 in all modules.

2.5 Front panel test pins

To aid system setup by a user or for debugging purpose, Pixie-16 provides up to six test pins through the front panel connector J200. These test pins can be connected to various internal signals of the Pixie-16 to provide insight of the current status of the system. The following figure shows the layout of these test pins.



Layout of Pixie-16 front panel 3.3V I/O port (J200).

PIN #	PIN Name	Signal Name
1	Fo_0	Test[0]
2	GND	GND
3	Fo_2	Test[1]
4	Fo_3	Test[2]
5	Fo_4	Test[3]
6	Fo_6	Test[4]
7	GND	GND
8	Fo_7	Test[5]
9	N.C.	Not connected
10	N.C.	Not connected

2.6 Test signal outputs

Bit 15 of DSP parameter TrigConfig0 (DSP parameter TrigConfig[0]) can be used to control the output of test signals to the front panel J200 connector.

TrigConfig[0] Bit		Description			
		value	function	value	function
[15]	Enable/disable output of test signals to Pixie-16 front panel	0	Disable output of test signals	1	Enable output of test signals

As mentioned in section 2.2, bit 31 of parameter TrigConfig3 (DSP parameter TrigConfig[3]) can be used to select one of the two groups of test signals to the front panel J200 connector.

TrigConfig[3] Bit		Description					
[31]	Select test signals	0	TEST0	FTRIG_DELAY	1	TEST0	FT[0]
			TEST1	FTRIG_VAL		TEST1	FT[1]
			TEST2	GLBETRIG_CE		TEST2	FT[2]
			TEST3	CHANETRIG_CE		TEST3	VANDLE_PWA_OR
			TEST4	VANDLE_PWA[0]		TEST4	BETA_PWA_TRIG_OR
			TEST5	GLOBAL_TRIG		TEST5	BETA_VALIDATION_TRIG

Detailed description of the signals shown above is given below.

Signal Name	Description
FTRIG_DELAY	Delayed local fast trigger of channel 0
GND	Ground
FTRIG_VAL	Validated, delayed local fast trigger of channel 0
GLBETRIG_CE	Stretched external global validation trigger of channel 0
CHANETRIG_CE	Stretched channel validation trigger (i.e. pairwise coincidence trigger) of channel 0
VANDLE_PWA[0]	VANDLE pairwise coincidence trigger of channel #0 and #1
GLOBAL_TRIG	Global validation trigger

FT[0]	Fast trigger from channel 0
FT[1]	Fast trigger from channel 1
FT[2]	Fast trigger from channel 2
VANDLE_PWA_OR	Crate level OR of VANDLE pairwise coincidence triggers
BETA_PWA_TRIG_OR	OR of Beta pairwise coincidence triggers
BETA_VALIDATION_TRIG	Validation trigger of all Beta triggers

2.7 Timing adjustment

The following parameters can be adjusted by the user for achieving different timing characteristics.

2.7.1 Fast trigger stretch length

This is the user channel parameter FASTTRIGBACKLEN (DSP parameter FastTrigBackLen). It can be adjusted between 8 ns and 32.76 μs. It is used to stretch the fast trigger pulse before such trigger pulse is used to make coincidence or multiplicity decisions. Thus, it is essentially the coincidence window width.

2.7.2 Fast trigger delay length

This is the user channel parameter FtrigoutDelay (DSP parameter FtrigoutDelay). It can be adjusted between 0 ns and 1.016 μs. It is used to delay the fast trigger pulse before such trigger pulse is used to make coincidence or multiplicity decisions.

2.7.3 Extern delay

This is the user channel parameter ExternDelayLen (DSP parameter ExternDelayLen). It can be adjusted between 0 ns and 2.040 μs. It is used to delay the local fast trigger in order to compensate for the delayed arrival of the channel or global validation triggers.

2.7.4 External trigger stretch length

This is the user channel parameter ExtTrigStretch (DSP parameter ExtTrigStretch). It can be adjusted between 8 ns and 32.760 μs. It is used to stretch the external global validation trigger pulse.

2.7.5 Channel trigger stretch length

This is the user channel parameter ChanTrigStretch (DSP parameter ChanTrigStretch). It can be adjusted between 8 ns and 32.760 μs. It is used to stretch the channel validation trigger pulse.

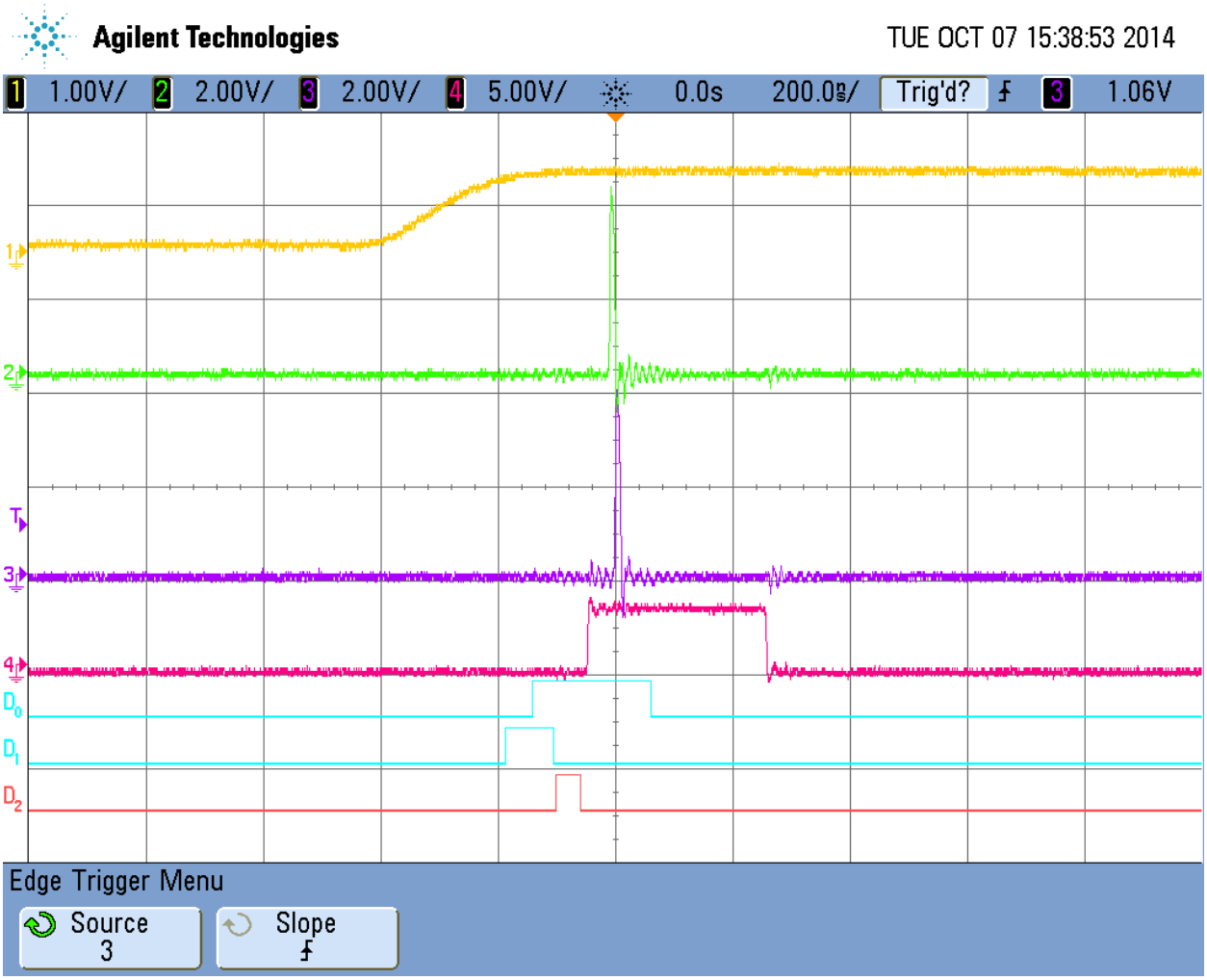
2.8 Sample signals for front panel test pins

The timing diagram shown below was acquired with a digital oscilloscope (MSO6054A) from Agilent Technologies. Shown on the top of the diagram was an analog pulse generated by a random pulser.

It shows a sample timing diagram of an event validated by validation triggers, including both the global validation trigger and channel coincidence trigger. This event's local fast trigger (signal #2) was validated by the presence of both validation triggers (signal #4 and signal D0), as shown by the signal #3, i.e. the validated local fast trigger. Signal D1 shows the VANDLE pairwise coincidence trigger, whereas signal D2 shows global validation trigger.

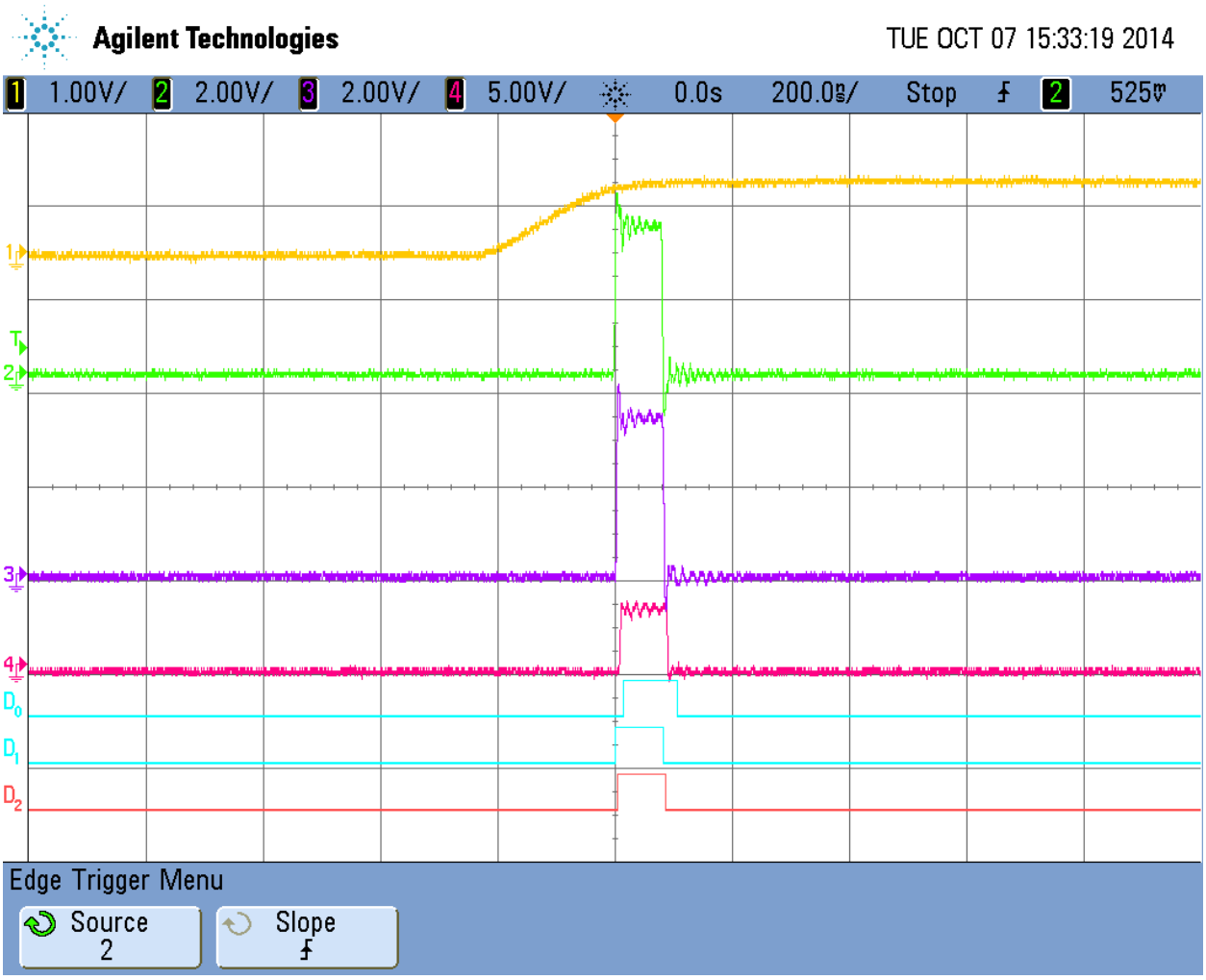
Please NOTE: **signal #3 is only present when a data run is in progress**. In contrast, signal #1 should be always present if pulses are coming into this channel, regardless of the data run status.

Signal #	Signal Name
1	PULSER PULSE
2	FTRIG_DELAY
3	FTRIG_VAL
4	GLBETRIG_CE
D0	CHANETRIG_CE
D1	VANDLE_PWA[0]
D2	GLOBAL_TRIG



Sample timing diagram showing an event validated by validation triggers.

Signal #	Signal Name
1	PULSER PULSE
2	FT[0]
3	FT[1]
4	FT[2]
D0	VANDLE_PWA_OR
D1	BETA_PWA_TRIG_OR
D2	BETA_VALIDATION_TRIG



Sample timing diagram showing beta and VANDLE detector triggers.

3 Output data structure

Output data for each recorded event consists of an event header plus trace if the recording of trace is enabled by the user. There are different types of output data options after enabling certain bits in the DSP parameter ChanCSRA. However, for all options the following 4 words will always be included in the event header as the first 4 words.

<table>
<tr><th>Index</th><th colspan="6">Data</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>[31]</td><td>[30:17]</td><td>[16:12]</td><td>[11:8]</td><td>[7:4]</td><td>[3:0]</td><td rowspan="2">Bits [3:0] – channel number; bits [7:4] – PXI slot number; bits [11:8] – PXI crate number; bits [16:12] – header length; bits [30:17] – event length; bit [31] – event finish code (0 – good event; 1 – piled-up event)</td></tr>
<tr><td>Finish Code</td><td>Event Length</td><td>Header Length</td><td>CrateID</td><td>SlotID</td><td>Chan#</td></tr>
<tr><td rowspan="2">1</td><td colspan="6">[31:0]</td><td rowspan="2">Event time (lower 32-bit of the 48-bit timestamp) recorded by the signal processing FPGA (latched by either the local fast trigger or CFD trigger)</td></tr>
<tr><td colspan="6">EVTTIME_LO[31:0]</td></tr>
<tr><td rowspan="2">2</td><td>[31]</td><td>[30]</td><td>[29:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event time (upper 16-bit of the 48-bit timestamp); bits [29:16] – CFD fractional time × 16384 (0 if CFD trigger is not enabled); bit [30] – CFD trigger source bit; bit [31] – CFD forced trigger bit</td></tr>
<tr><td>CFD forced trigger bit</td><td>CFD trigger source bit</td><td>CFD Fractional Time</td><td colspan="3">EVTTIME_HI[15:0]</td></tr>
<tr><td rowspan="2">3</td><td>[31]</td><td colspan="2">[30:16]</td><td colspan="3">[15:0]</td><td rowspan="2">Bits [15:0] – event energy; bits [30:16] – trace length (0 if no trace is recorded); bit [31] – trace out of range flag</td></tr>
<tr><td>Trace Out-of-Range Flag</td><td colspan="2">Trace Length</td><td colspan="3">Event Energy</td></tr>
</table>

The following sections illustrated different output data options.

3.1 Recording of raw energy sums and baseline ENABLED

Index	Data	Description
4	[31:0]	Trailing energy sum
	Energy sum - trailing	
5	[31:0]	Leading energy sum
	Energy sum - leading	
6	[31:0]	Gap energy sum
	Energy sum - gap	
7	[31:0]	Baseline value
	Baseline	

3.2 Recording of QDC sums ENABLED

Index	Data	Description
4	[31:0]	QDC sum #0
	QDCSum0	
5	[31:0]	QDC sum #1
	QDCSum1	
6	[31:0]	QDC sum #2
	QDCSum2	
7	[31:0]	QDC sum #3
	QDCSum3	
8	[31:0]	QDC sum #4
	QDCSum4	
9	[31:0]	QDC sum #5
	QDCSum5	
10	[31:0]	QDC sum #6
	QDCSum6	
11	[31:0]	QDC sum #7
	QDCSum7	

3.3 Recording of external clock timestamps ENABLED

Index	Data		Description
4	[31:0]		Lower 32-bit of the 48-bit external clock timestamp
	Ext_TS_Lo		
5	[31:16]	[15:0]	Upper 16-bit of the 48-bit external clock timestamp
	Not used, set to 0	Ext_TS_Hi	

3.4 Recording of energy sums/baseline, QDC sums and external timestamps ENABLED

Index	Data	Description
4	[31:0]	Trailing energy sum
	Energy sum - trailing	
5	[31:0]	Leading energy sum
	Energy sum - leading	
6	[31:0]	Gap energy sum
	Energy sum - gap	
7	[31:0]	Baseline value
	Baseline	
8	[31:0]	QDC sum #0

	QDCSum0		
9	[31:0]		QDC sum #1
	QDCSum1		
10	[31:0]		QDC sum #2
	QDCSum2		
11	[31:0]		QDC sum #3
	QDCSum3		
12	[31:0]		QDC sum #4
	QDCSum4		
13	[31:0]		QDC sum #5
	QDCSum5		
14	[31:0]		QDC sum #6
	QDCSum6		
15	[31:0]		QDC sum #7
	QDCSum7		
16	[31:0]		Lower 32-bit of the 48-bit external clock timestamp
	Ext_TS_Lo		
17	[31:16]	[15:0]	Upper 16-bit of the 48-bit external clock timestamp
	Not used, set to 0	Ext_TS_Hi	

3.5 Recording of trace ENABLED

If trace recording is enabled, trace data will immediately follow the last word of the event header. Since raw ADC data points are 12-bit numbers, two 12-bit numbers are packed into one 32-bit word, as shown below. Since the event header could have variable length (4 to 18 words) depending on the selection of various output data options, the header length, event length and trace length that are recorded in the first 4 words of the event header should be used to navigate through the output data stream.

Index	Data				Description
n	[31:0]				Last word of event header which could be 4, 8, 12, or 16 words long
	Last word of event header				
n+1	[31:28]	[27:16]	[15:12]	[11:0]	Packing of ADC Data #0 and #1
	Not used	ADC Data #1	Not used	ADC Data #0	
n+2	[31:28]	[27:16]	[15:12]	[11:0]	Packing of ADC Data #2 and #3
	Not used	ADC Data #3	Not used	ADC Data #2	
…	…				