Lab_screenshot_part:

Lab Synthesis

Results

```
Statistics for case statements in always block at line 164 in file
        '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthesis/work/
../../common/i2c_project/rtl/verilog/i2c_master_top.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|           166            |    auto/user     |
===============================================

Statistics for case statements in always block at line 179 in file
        '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthesis/work/
../../common/i2c_project/rtl/verilog/i2c_master_top.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|           194            |    auto/user     |
===============================================

Inferred memory devices in process
        in routine i2c_master_top line 160 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    wb_ack_o_reg     | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_top line 164 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    wb_dat_o_reg     | Flip-flop |   8   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_top line 179 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       txr_reg       | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|      prer_reg       | Flip-flop |  16   |  Y  | N  | N  | Y  | N  | N  | N  |
|       ctr_reg       | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

```
Inferred memory devices in process
        in routine i2c_master_top line 203 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       cr_reg        | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_top line 264 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    irq_flag_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|       al_reg        | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|      rxack_reg      | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|       tip_reg       | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_top line 288 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    wb_inta_o_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully. (i2c_master_top)
Elaborated 1 design.
Current design is now 'i2c_master_top'.
Information: Building the design 'i2c_master_byte_ctrl'. (HDL-193)
Warning:  /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthesis/work
/../../common/i2c_project/rtl/verilog/i2c_master_byte_ctrl.v:233: Case statement is not a full case. (
ELAB-909)

Statistics for case statements in always block at line 204 in file
        '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthesis/work/
../../common/i2c_project/rtl/verilog/i2c_master_byte_ctrl.v'
===============================================
|           Line           |  full/ parallel  |
===============================================
|           233            |    user/user     |
===============================================
```

```
Inferred memory devices in process
        in routine i2c_master_byte_ctrl line 176 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_byte_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       sr_reg        | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_byte_ctrl line 187 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_byte_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      dcnt_reg       | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_byte_ctrl line 204 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_byte_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     ack_out_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|    core_cmd_reg     | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|    core_txd_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|      shift_reg      | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|       ld_reg        | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     cmd_ack_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     c_state_reg     | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully. (i2c_master_byte_ctrl)
Information: Building the design 'i2c_master_bit_ctrl'. (HDL-193)
Warning:  /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthesis/work
/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v:408: Case statement is not a full case. (E
LAB-909)

Statistics for case statements in always block at line 386 in file
        '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthesis/work/
../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'
================================================
|           Line           |  full/ parallel   |
================================================
|           408            |    user/user      |
|           412            |    user/user      |
================================================
```

```
Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 195 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    dscl_oen_reg     | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 200 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|   slave_wait_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 210 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     clk_en_reg      | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
|       cnt_reg       | Flip-flop |  16   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 237 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      cSDA_reg       | Flip-flop |   2   |  Y  | N  | Y  | N  | N  | N  | N  |
|      cSCL_reg       | Flip-flop |   2   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 256 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|   filter_cnt_reg    | Flip-flop |  14   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

```
Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 350 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       al_reg        | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 360 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      dout_reg       | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine i2c_master_bit_ctrl line 386 in file
                '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_synthes
is/work/../../common/i2c_project/rtl/verilog/i2c_master_bit_ctrl.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     sda_chk_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     c_state_reg     | Flip-flop |  18   |  Y  | N  | Y  | N  | N  | N  | N  |
|     cmd_ack_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     scl_oen_reg     | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
|     sda_oen_reg     | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully. (i2c_master_bit_ctrl)
Current design is 'i2c_master_top'.

  Linking design 'i2c_master_top'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  saed14rvt_tt0p8v25c (library) /home/course/ee5252/lab_snps_flow/SAED14_EDK_LAB/SAED14_EDK_LAB/lib/st
dcell_rvt/db_nldm/saed14rvt_tt0p8v25c.db

Warning: no aliases matched 'cpu_isle' (CMD-029)
Warning: no aliases matched 'cpu_isle' (CMD-029)
Warning: no aliases matched 'hif2bt' (CMD-029)
Warning: no aliases matched 'sys_clk_sync' (CMD-029)
Warning: no aliases matched 'hosif' (CMD-029)
Warning: no aliases matched 'sync_regs' (CMD-029)
Warning: no aliases matched 'iccm_control' (CMD-029)
Warning: no aliases matched 'debug_port' (CMD-029)
```

```
****************************************
check_design summary:
Version:     R-2020.09-SP5
Date:        Mon Apr 15 13:53:11 2024
****************************************

                  Name                                                  Total
--------------------------------------------------------------------------------
No issues found.
--------------------------------------------------------------------------------


  Linking design 'i2c_master_top'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  saed14rvt_tt0p8v25c (library)
                           /home/course/ee5252/lab_snps_flow/SAED14_EDK_LAB/SAED14_EDK_LAB/lib/stdc
ell_rvt/db_nldm/saed14rvt_tt0p8v25c.db

Warning: Ignoring -power_effort option since there is no power constraint. (PWR-59)
Information: Evaluating DesignWare library utilization. (UISN-27)

============================================================================
| DesignWare Building Block Library  |         Version         | Available |
============================================================================
| Basic DW Building Blocks           | R-2020.09-DWBB_202009.5 |     *     |
| Licensed DW Building Blocks        |                         |           |
============================================================================


Information: There are 8 potential problems in your design. Please run 'check_design' for more informa
tion. (LINT-99)
```

```
Beginning Delay Optimization Phase
----------------------------------

                                TOTAL
 ELAPSED              WORST NEG SETUP    DESIGN
   TIME      AREA       SLACK    COST    RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:00:28     331.5      0.00       0.0       9.5
  0:00:28     331.5      0.00       0.0       9.5
  0:00:28     331.5      0.00       0.0       9.5


Beginning Design Rule Fixing  (min_capacitance)
----------------------------

                                TOTAL
 ELAPSED              WORST NEG SETUP    DESIGN
   TIME      AREA       SLACK    COST    RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:00:28     331.5      0.00       0.0       9.5


Beginning Area-Recovery Phase  (cleanup)
-----------------------------

                                TOTAL
 ELAPSED              WORST NEG SETUP    DESIGN
   TIME      AREA       SLACK    COST    RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:00:28     331.5      0.00       0.0       9.5
  0:00:28     331.5      0.00       0.0       9.5
  0:00:28     330.4      0.00       0.0       9.5
  0:00:28     330.1      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     329.8      0.00       0.0       9.5
  0:00:28     326.0      0.00       0.0       9.5
oading db file '/home/course/ee5252/lab_snps_flow/SAED14_EDK_LAB/SAED14_EDK_LAB/lib/stdcell_rvt/db_nl
m/saed14rvt_tt0p8v25c.db'


ote: Symbol # after min delay cost means estimated hold TNS across all active scenarios


 Optimization Complete
 ---------------------
```

Lab1 Floorplan

Results

```
... 3 cell libraries to build.


... checking whether need to build cell library: saed14rvt_tt0p8v25c.ndm (1/3)
... checking whether can reuse library under output directory
cannot reuse CLIBs/saed14rvt_tt0p8v25c.ndm under output directory: library not exists

... checking whether need to build cell library: saed14rvt_tt0p8v25c_physical_only.ndm
(2/3)
... checking whether can reuse library under output directory
cannot reuse CLIBs/saed14rvt_tt0p8v25c_physical_only.ndm under output directory: librar
y not exists

... checking whether need to build cell library: EXPLORE_physical_only.ndm (3/3)
... checking whether can reuse library under output directory
cannot reuse CLIBs/EXPLORE_physical_only.ndm under output directory: library not exists

... processing cell library: saed14rvt_tt0p8v25c.ndm (1/3)
... run lm_shell to build the cell library
............
created new cell library under output directory: CLIBs/saed14rvt_tt0p8v25c.ndm

... processing cell library: saed14rvt_tt0p8v25c_physical_only.ndm (2/3)
... run lm_shell to build the cell library
..................
created new cell library under output directory: CLIBs/saed14rvt_tt0p8v25c_physical_onl
y.ndm

... processing cell library: EXPLORE_physical_only.ndm (3/3)
... run lm_shell to build the cell library
.....................................................................
.....................................................................
................
created new cell library under output directory: CLIBs/EXPLORE_physical_only.ndm
```

```
Information: Successfully built 3 reference libraries: saed14rvt_tt0p8v25c.ndm saed14rv
t_tt0p8v25c_physical_only.ndm EXPLORE_physical_only.ndm. (LIB-093)
Warning: Technology used to create frame-view and current technology have inconsistency
: Min spacings are different for layer 'M1'. (FRAM-054)
Warning: Technology 'saed14rvt_1p9m.tf' used for frame-view creation in library 'saed14
rvt_tt0p8v25c', is inconsistent with the current technology 'saed14nm_1p9m_mw.tf' of li
brary 'i2c_master_top'. (NDM-102)
Warning: Technology used to create frame-view and current technology have inconsistency
: Min spacings are different for layer 'M1'. (FRAM-054)
Warning: Technology 'saed14rvt_1p9m.tf' used for frame-view creation in library 'saed14
rvt_tt0p8v25c_physical_only', is inconsistent with the current technology 'saed14nm_1p9
m_mw.tf' of library 'i2c_master_top'. (NDM-102)
Warning: Technology used to create frame-view and current technology have inconsistency
: Min spacings are different for layer 'M1'. (FRAM-054)
Warning: Technology 'saed14rvt_1p9m.tf' used for frame-view creation in library 'EXPLOR
E_physical_only', is inconsistent with the current technology 'saed14nm_1p9m_mw.tf' of
library 'i2c_master_top'. (NDM-102)
Loading verilog file '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal
_release/input/i2c_master_top.v'
Information: Reading Verilog into new design 'i2c_master_top' in library 'i2c_master_to
p'. (VR-012)
Number of modules read: 5
Top level ports: 35
Total ports in all modules: 185
Total nets in all modules: 890
Total instances in all modules: 719
Elapsed = 00:00:00.02, CPU = 00:00:00.01
Using libraries: i2c_master_top saed14rvt_tt0p8v25c saed14rvt_tt0p8v25c_physical_only E
XPLORE_physical_only
Linking block i2c_master_top:i2c_master_top.design
Information: User units loaded from library 'saed14rvt_tt0p8v25c' (LNK-040)
Design 'i2c_master_top' was successfully linked.
Information: Saving 'i2c_master_top:i2c_master_top.design' to 'i2c_master_top:i2c_maste
r_top_1_data_setup.design'. (DES-028)
Saving library 'i2c_master_top'
Closing block 'i2c_master_top:i2c_master_top.design'
Closing library 'i2c_master_top'
Maximum memory usage for this session: 359.85 MB
Maximum memory usage for this session including child processes: 1074.51 MB
CPU usage for this session:     21 seconds (  0.01 hours)
Elapsed time for this session:    613 seconds (  0.17 hours)
Thank you for using IC Compiler II.
```

```
Information: Loading library file '/home/course/ee525202/lab_snps_flow/lab_formal_relea
se/lab_formal_release/results/i2c_master_top' (FILE-007)
Information: Loading library file '/home/course/ee525202/lab_snps_flow/lab_formal_relea
se/lab_formal_release/lab1_planning/work/CLIBs/saed14rvt_tt0p8v25c.ndm' (FILE-007)
Information: Loading library file '/home/course/ee525202/lab_snps_flow/lab_formal_relea
se/lab_formal_release/lab1_planning/work/CLIBs/saed14rvt_tt0p8v25c_physical_only.ndm' (
FILE-007)
Information: Loading library file '/home/course/ee525202/lab_snps_flow/lab_formal_relea
se/lab_formal_release/lab1_planning/work/CLIBs/EXPLORE_physical_only.ndm' (FILE-007)
Warning: Technology used to create frame-view and current technology have inconsistency
: Min spacings are different for layer 'M1'. (FRAM-054)
Warning: Technology 'saed14rvt_1p9m.tf' used for frame-view creation in library 'saed14
rvt_tt0p8v25c', is inconsistent with the current technology 'saed14nm_1p9m_mw.tf' of li
brary 'i2c_master_top'. (NDM-102)
Warning: Technology used to create frame-view and current technology have inconsistency
: Min spacings are different for layer 'M1'. (FRAM-054)
Warning: Technology 'saed14rvt_1p9m.tf' used for frame-view creation in library 'saed14
rvt_tt0p8v25c_physical_only', is inconsistent with the current technology 'saed14nm_1p9
m_mw.tf' of library 'i2c_master_top'. (NDM-102)
Warning: Technology used to create frame-view and current technology have inconsistency
: Min spacings are different for layer 'M1'. (FRAM-054)
Warning: Technology 'saed14rvt_1p9m.tf' used for frame-view creation in library 'EXPLOR
E_physical_only', is inconsistent with the current technology 'saed14nm_1p9m_mw.tf' of
library 'i2c_master_top'. (NDM-102)
Information: Auto created reference libraries are up-to-date, no need to rebuild. (LIB-
084)
Information: User units loaded from library 'saed14rvt_tt0p8v25c' (LNK-040)
Information: Incrementing open_count of block 'i2c_master_top:temp_data_setup.design' t
o 2. (DES-021)
Using libraries: i2c_master_top saed14rvt_tt0p8v25c saed14rvt_tt0p8v25c_physical_only E
XPLORE_physical_only
Visiting block i2c_master_top:temp_data_setup.design
Design 'i2c_master_top' was successfully linked.
```

```
****************************************
Report : clock
Design : i2c_master_top
Mode   : default
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:20 2024
****************************************


Attributes:
    p - Propagated clock
    G - Generated  clock
    U - Unexpanded generated clock

Clock          Period   Waveform            Attrs     Sources
------------------------------------------------------------------------------
wb_clk_i         2.00   {0 1}                         {wb_clk_i}

****************************************
Report : clock_skew
Design : i2c_master_top
Mode   : default
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:20 2024
****************************************

              Min Rise  Min Fall  Max Rise  Max Fall     Hold          Setup        Rel
ated
Object          Delay     Delay     Delay     Delay   Uncertainty   Uncertainty      Cl
ock           Scenario      Origin
------------------------------------------------------------------------------------------
------------------------------------
wb_clk_i             -         -         -         -             -          0.30
 --           default         user

               Min Rise    Min Fall    Max Rise    Max Fall
Object        Transition  Transition  Transition  Transition  Scenario
------------------------------------------------------------------------
wb_clk_i            0.20        0.20        0.20        0.20  default

****************************************
Report : exceptions
Design : i2c_master_top
Mode   : default
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:20 2024
****************************************
```

```
Information: Timer using 1 threads
****************************************
Report : disable_timing
Design : i2c_master_top
Mode   : default
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:20 2024
****************************************

Attributes
    c - case-analysis
    C - Conditional arc
    d - default conditional arc
    f - false net-arc
    l - loop breaking
    L - db inherited loopbreaking
    m - mode
    p - propagated constant
    u - user-defined
    U - User-defined library arcs
    n - negative power supply


Cell or Port                From    To      Sense           Flag  Reason
--------------------------------------------------------------------------------
scl_pad_o                                                       scl_pad_o = 0
sda_pad_o                                                       sda_pad_o = 0
byte_controller/ack_out_reg CK      RD      removal_rise_clk_rise
                                                        C       SI = 0
byte_controller/ack_out_reg CK      Q       rising_edge     C       SI = 0
byte_controller/ack_out_reg CK      D       setup_clk_rise  C       SI = 0
byte_controller/ack_out_reg CK      D       hold_clk_rise   C       SI = 0
byte_controller/ack_out_reg CK      SI      setup_clk_rise  p       SI = 0
byte_controller/ack_out_reg CK      SI      hold_clk_rise   p       SI = 0
byte_controller/ack_out_reg CK      SI      setup_clk_rise  p       SI = 0
byte_controller/ack_out_reg CK      SI      hold_clk_rise   p       SI = 0
byte_controller/ack_out_reg CK      SE      setup_clk_rise  C       SI = 0
byte_controller/ack_out_reg CK      SE      hold_clk_rise   C       SI = 0
byte_controller/ack_out_reg CK      RD      recovery_rise_clk_rise
                                                        C       SI = 0
byte_controller/ack_out_reg CK      RD      removal_rise_clk_rise
                                                        C       SI = 0
byte_controller/ack_out_reg CK      RD      recovery_rise_clk_rise
                                                        C       SI = 0
byte_controller/ack_out_reg CK      RD      removal_rise_clk_rise
                                                        C       SI = 0
byte_controller/ack_out_reg CK      RD      recovery_rise_clk_rise
                                                        C       SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                            CK      SI      setup_clk_rise  p       SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                            CK      RD      recovery_rise_clk_rise
                                                        C       SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                            CK      RD      removal_rise_clk_rise
                                                        C       SI = 0
byte_controller/bit_controller/cSCL_reg[0]
```

```
byte_controller/bit_controller/cSCL_reg[0]
                              CK      RD      recovery_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      RD      removal_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      RD      recovery_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      RD      removal_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      SE      hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      SE      setup_clk_rise  C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      SI      setup_clk_rise  p     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      D       hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      D       setup_clk_rise  C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      Q       rising_edge     C     SI = 0
byte_controller/bit_controller/cSCL_reg[0]
                              CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      RD      recovery_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      D       hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      D       setup_clk_rise  C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      SI      setup_clk_rise  p     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      SE      setup_clk_rise  C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      SE      hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      RD      recovery_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      RD      recovery_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      RD      removal_rise_clk_rise
                                                      C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      SI      setup_clk_rise  p     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      Q       rising_edge     C     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                              CK      RD      removal_rise_clk_rise
```

```
byte_controller/bit_controller/cSCL_reg[1]
                            CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSCL_reg[1]
                            CK      RD      removal_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      SE      setup_clk_rise  C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      Q       rising_edge     C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      D       setup_clk_rise  C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      D       hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      SI      setup_clk_rise  p     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      SE      hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      RD      recovery_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      RD      removal_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      RD      recovery_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      RD      removal_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      RD      recovery_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      RD      removal_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[0]
                            CK      SI      setup_clk_rise  p     SI = 0
byte_controller/bit_controller/cSDA_reg[1]
                            CK      RD      recovery_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[1]
                            CK      SE      hold_clk_rise   C     SI = 0
byte_controller/bit_controller/cSDA_reg[1]
                            CK      RD      recovery_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[1]
                            CK      RD      removal_rise_clk_rise
                                                            C     SI = 0
byte_controller/bit_controller/cSDA_reg[1]
                            CK      SI      hold_clk_rise   p     SI = 0
byte_controller/bit_controller/cSDA_reg[1]
                            CK      RD      recovery_rise_clk_rise
```

```
Information: Saving 'i2c_master_top:temp_data_setup.design' to 'i2c_master_top:temp_flo
orplan_init.design'. (DES-028)
Information: The design specific attribute override for layer 'M1' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M2' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M3' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M4' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M5' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M6' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M7' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Information: The design specific attribute override for layer 'M1' is set in the curren
t block 'temp_data_setup', because the actual library setting may not be overwritten. (
ATTR-12)
Removing existing floorplan objects
Creating core...
Core utilization ratio = 20.11%
Unplacing all cells...
Creating site array...
Creating routing tracks...
Initializing floorplan completed.
Information: Starting 'place_pins' (FLW-8000)
Information: Time: 2024-04-19 16:34:20 / Session: 0.16 hr / Command: 0.00 hr / Memory:
284 MB (FLW-8100)
Information: The command 'place_pins' cleared the undo history. (UNDO-016)
Load DB...
CPU Time for load db: 00:00:00.00u 00:00:00.00s 00:00:00.01e:

Min routing layer: M1
Max routing layer: M7


CPU Time for Top Level Pre-Route Processing: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of block ports: 35
Number of block pin locations assigned from router: 0
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of PG ports on blocks: 0
Number of pins created: 35
CPU Time for Pin Creation: 00:00:00.01u 00:00:00.00s 00:00:00.03e:
Total Pin Placement CPU Time: 00:00:00.02u 00:00:00.00s 00:00:00.06e:
Information: Ending 'place_pins' (FLW-8001)
Information: Time: 2024-04-19 16:34:20 / Session: 0.16 hr / Command: 0.00 hr / Memory:
286 MB (FLW-8100)
Information: The command 'check_mv_design' cleared the undo history. (UNDO-016)
```

```
****************************************
Report : check_mv_design
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:20 2024
****************************************

---------- Power domain rule ----------
No errors or warnings.

---------- Supply set rule ----------
No errors or warnings.

---------- Supply net rule ----------
No errors or warnings.

---------- Supply port rule ----------
No errors or warnings.

---------- Isolation strategy rule ----------
No errors or warnings.

---------- Level shifter strategy rule ----------
No errors or warnings.

---------- Retention strategy rule ----------
No errors or warnings.

---------- Power switch strategy rule ----------
No errors or warnings.

---------- Repeater rule ----------
No errors or warnings.

---------- Terminal boundary rule ----------
No errors or warnings.

---------- Isolation cell rule ----------
No errors or warnings.

---------- Level shifter cell rule ----------
No errors or warnings.

---------- Retention cell rule ----------
No errors or warnings.

---------- Switch cell rule ----------
No errors or warnings.

---------- PGMUX rule ----------
No errors or warnings.
```

```
---------- Diode cell rule ----------
No errors or warnings.

---------- Model rule ----------
No errors or warnings.

---------- Isolation rule ----------
No errors or warnings.

---------- Voltage shifting rule ----------
No errors or warnings.

---------- Tie-off connection rule ----------
No errors or warnings.

---------- Analog net rule ----------
No errors or warnings.

---------- Physical block pin rule ----------
No errors or warnings.

---------- PG pin rule ----------
No errors or warnings.

---------- Signal pin rule ----------
No errors or warnings.

---------- Summary ----------
Information: Total 0 error(s) and 0 warning(s) from check_mv_design. (MV-082)
Information: Saving 'i2c_master_top:temp_data_setup.design' to 'i2c_master_top:temp_flo
orplane.design'. (DES-028)
Information: Starting 'create_placement' (FLW-8000)
Information: Time: 2024-04-19 16:34:21 / Session: 0.16 hr / Command: 0.00 hr / Memory:
286 MB (FLW-8100)
Creating appropriate block views (if needed)...
Multi-Processing Summary
  Max number of cores for parent process: 1; hostname: ws33
  No distributed processing
Command Option Settings Summary
  -floorplan -effort high
Information: All hard macros are fixed, no hard macro placement is done. (DPP-416)
Generating automatic soft blockages for temp_data_setup, hor/vert channel sizes are 2.4
/2.4
Placing top level std cells.
Warning: no valid parasitic for default corner(LATE) (NEX-018)
Warning: no valid parasitic for default corner(LATE) (NEX-018)
Warning: no valid parasitic for default corner(LATE) (NEX-018)
Warning: no valid parasitic for default corner(LATE) (NEX-018)
coarse place 0% done.
coarse place 33% done.
coarse place 67% done.
coarse place 100% done.
Running block placement.
Running timing driven standard cell placement
```

```
Running timing driven standard cell placement
No editable block found.
Running virtual optimization on full netlist ...
Cannot create estimated_corner because current_corner is the default corner without use
r settings.Creating appropriate block views (if needed)...
Generating automatic soft blockages for temp_data_setup, hor/vert channel sizes are 2.4
/2.4
Placing top level std cells.
Warning: no valid parasitic for default corner(LATE) (NEX-018)
Warning: no valid parasitic for default corner(LATE) (NEX-018)
Warning: no valid parasitic for default corner(LATE) (NEX-018)
Warning: no valid parasitic for default corner(LATE) (NEX-018)
coarse place 33% done.
coarse place 67% done.
coarse place 100% done.
Running block placement.
Floorplan placement done.
****************************************
Report : report_placement
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:23 2024
****************************************

  Wire length report (all)
  ==================
  wire length in design temp_data_setup: 4356.431 microns.
  wire length in design temp_data_setup (see through blk pins): 4356.431 microns.
  ------------------
  Total wire length: 4356.431 microns.

  Physical hierarchy violations report
  ====================================
  Violations in design temp_data_setup:
     0 cells have placement violation.
  ------------------------------------
  Total 0 cells have placement violation.

  Voltage area violations report
  ==================================
  Voltage area placement violations in design temp_data_setup:
     0 cells placed outside the voltage area which they belong to.
  ----------------------------------
  Total 0 macro cells placed outside the voltage area which they belong to.

  Hard macro to hard macro overlap report
  =======================================
  HM to HM overlaps in design temp_data_setup: 0
  ---------------------------------------
  Total hard macro to hard macro overlaps: 0

Information: Default error view temp_data_setup_dpplace.err is created in GUI error bro
wser. (DPP-054)
Information: Elapsed time for create_placement excluding pending time: 00:00:02.49. (DP
UI-902)
```

```
Information: CPU time for create_placement : 00:00:00.90. (DPUI-903)
Information: Peak memory usage for create_placement : 399 MB. (DPUI-904)
Information: Ending 'create_placement' (FLW-8001)
Information: Time: 2024-04-19 16:34:23 / Session: 0.16 hr / Command: 0.00 hr / Memory:
399 MB (FLW-8100)
Information: Starting 'legalize_placement' (FLW-8000)
Information: Time: 2024-04-19 16:34:23 / Session: 0.16 hr / Command: 0.00 hr / Memory:
399 MB (FLW-8100)
nplDplc2Placer::setParam(effort,1)
nplDplc2Placer::setParam(debug,0)
nplDplc2Placer::setParam(site_check,2)
nplDplc2Placer::setParam(app_firm_wgt,0)
Warning: Site master "unit" has neither X-Symmetry nor Y-Symmetry. The "legal orientati
ons" for the standard cells will be limited. (LGL-031)
Warning: Routing direction of metal layer PO is neither "horizontal" nor "vertical".  P
DC checks will not be performed on this layer. (PDC-003)
Warning: Routing direction of metal layer M8 is neither "horizontal" nor "vertical".  P
DC checks will not be performed on this layer. (PDC-003)
Warning: Routing direction of metal layer M9 is neither "horizontal" nor "vertical".  P
DC checks will not be performed on this layer. (PDC-003)
Warning: Routing direction of metal layer MRDL is neither "horizontal" nor "vertical".
 PDC checks will not be performed on this layer. (PDC-003)
PDC app_options settings =========
        place.legalize.enable_prerouted_net_check: 1
        place.legalize.num_tracks_for_access_check: 1
        place.legalize.use_eol_spacing_for_access_check: 0
        place.legalize.allow_touch_track_for_access_check: 1
        place.legalize.reduce_conservatism_in_eol_check: 0
        place.legalize.preroute_shape_merge_distance: 0.0
        place.legalize.enable_non_preferred_direction_span_check: 0

Layer M1: cached 0 shapes out of 0 total shapes.
Layer M2: cached 0 shapes out of 0 total shapes.
Layer M3: cached 0 shapes out of 0 total shapes.
Cached 0 vias out of 0 total vias.

Legalizing Top Level Design i2c_master_top ...
Information: Initializing classic cellmap without advanced rules enabled and without PD
C enabled
Information: The following app options are used in cellmap
        place.legalize.enable_color_aware_placement : false
        place.legalize.use_nll_query_cm : false
        place.legalize.enable_advanced_legalizer : false
        place.legalize.enable_prerouted_net_check : true
        place.legalize.enable_advanced_prerouted_net_check : false
        place.legalize.always_continue : true
        place.legalize.limit_legality_checks : false
        place.common.pnet_aware_density : 1.0000
        place.common.pnet_aware_min_width : 0.0000
        place.common.pnet_aware_layers : {}
        place.common.use_placement_model : false
        place.common.enable_advanced_placement_model : true
        cts.placement.cell_spacing_rule_style : maximum
```

```
Warning: Library cell saed14rvt_tt0p8v25c:SAEDRVT14_ISOFSDPQ_PECO_8.frame is missing su
pply pins. Its power structure cannot be determined. (LGL-050)
Warning: Library cell saed14rvt_tt0p8v25c:SAEDRVT14_DCAP_PV1ECO_12.frame is missing sup
ply pins. Its power structure cannot be determined. (LGL-050)
Total 0.1200 seconds to build cellmap data
Information: Creating classic rule checker.
Warning: Routing direction of metal layer PO is neither "horizontal" nor "vertical".  P
DC checks will not be performed on this layer. (PDC-003)
Warning: Routing direction of metal layer M8 is neither "horizontal" nor "vertical".  P
DC checks will not be performed on this layer. (PDC-003)
Warning: Routing direction of metal layer M9 is neither "horizontal" nor "vertical".  P
DC checks will not be performed on this layer. (PDC-003)
Warning: Routing direction of metal layer MRDL is neither "horizontal" nor "vertical".
 PDC checks will not be performed on this layer. (PDC-003)
=====> Processed 66 ref cells (25 fillers) from library

Bounds/Regions In This Design:
        Area    Num Cells  Exclusive Name
 (square um)
     1621.27          715        Yes DEFAULT_VA

Warning: max_legality_failures=5000 ignored.
        To use it, set limit_legality_checks to true.
Warning: max_legality_check_range=500 ignored.
        To use it, set limit_legality_checks to true.
Starting legalizer.
Warning: Exclusive bound 'DEFAULT' has no cells.
Optimizing Exclusive Bound 'DEFAULT_VA' (2/2)
    Done Exclusive Bound 'DEFAULT_VA' (2/2) (0 sec)
Legalization complete (0 total sec)

****************************************
  Report : Placement Attempts
  Site   : unit
****************************************

number of cells:                    715
number of references:                66
number of site rows:                 67
number of locations attempted:    12091
number of locations failed:           0  (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

****************************************
```

```
****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         715 (7343 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.177 um ( 0.30 row height)
rms weighted cell displacement:   0.177 um ( 0.30 row height)
max cell displacement:            0.386 um ( 0.64 row height)
avg cell displacement:            0.157 um ( 0.26 row height)
avg weighted cell displacement:   0.157 um ( 0.26 row height)
number of cells moved:              715
number of large displacements:        0
large displacement threshold:     3.000 row height

Displacements of worst 10 cells:
Cell: U313 (SAEDRVT14_INV_1)
  Input location: (43.3428,30.7844)
  Legal location: (43.374,30.4)
  Displacement:   0.386 um ( 0.64 row height)
Cell: byte_controller/bit_controller/U189 (SAEDRVT14_INV_1)
  Input location: (24.2727,32.528)
  Legal location: (24.282,32.2)
  Displacement:   0.328 um ( 0.55 row height)
Cell: U258 (SAEDRVT14_INV_1)
  Input location: (46.0584,39.077)
  Legal location: (45.89,38.8)
  Displacement:   0.324 um ( 0.54 row height)
Cell: byte_controller/U83 (SAEDRVT14_AOI21_0P5)
  Input location: (35.3364,37.3045)
  Legal location: (35.456,37.6)
  Displacement:   0.319 um ( 0.53 row height)
Cell: byte_controller/bit_controller/sub_228/U1 (SAEDRVT14_INV_1)
  Input location: (34.3013,26.4605)
  Legal location: (34.124,26.2)
  Displacement:   0.315 um ( 0.53 row height)
Cell: U185 (SAEDRVT14_OAI22_1)
  Input location: (40.5274,34.2912)
  Legal location: (40.414,34)
  Displacement:   0.313 um ( 0.52 row height)
Cell: byte_controller/bit_controller/U96 (SAEDRVT14_INV_1)
  Input location: (31.5646,30.7613)
  Legal location: (31.756,31)
  Displacement:   0.306 um ( 0.51 row height)
Cell: byte_controller/U56 (SAEDRVT14_NR2_MM_1)
  Input location: (47.6188,31.8987)
  Legal location: (47.592,32.2)
  Displacement:   0.302 um ( 0.50 row height)
Cell: byte_controller/bit_controller/U23 (SAEDRVT14_ND2_CDC_1)
  Input location: (22.5779,32.4641)
  Legal location: (22.432,32.2)
  Displacement:   0.302 um ( 0.50 row height)
Cell: U213 (SAEDRVT14_NR2_MM_1)
  Input location: (44.7469,36.1591)
  Legal location: (44.928,36.4)
  Displacement:   0.301 um ( 0.50 row height)

Legalization succeeded.
```

```
Total Legalizer CPU: 0.942
Total Legalizer Wall Time: 2.186
---------------------------------------------------------------
Information: Ending 'legalize_placement' (FLW-8001)
Information: Time: 2024-04-19 16:34:25 / Session: 0.16 hr / Command: 0.00 hr / Memory:
399 MB (FLW-8100)
Start Global Route ...
[Init] Elapsed real time: 0:00:00
[Init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Init] Stage (MB): Used    0  Alloctr    0  Proc    0
[Init] Total (MB): Used    7  Alloctr    7  Proc 2547
Printing options for 'route.common.*'

Printing options for 'route.global.*'

Begin global routing.
Warning: Layer M8 does not have a preferred direction, assigning to horizontal. (ZRT-02
5)
Warning: Layer M9 does not have a preferred direction, assigning to vertical. (ZRT-025)
Warning: Layer MRDL does not have a preferred direction, assigning to horizontal. (ZRT-
025)
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = M7
Turn off antenna since no rule is specified
Info: number of net_type_blockage: 0
Via on layer (VIA1) needs more than one tracks
Warning: Layer M1 pitch 0.074 may be too small: wire/via-down 0.074, wire/via-up 0.098.
 (ZRT-026)
Via on layer (VIA1) needs more than one tracks
Warning: Layer M2 pitch 0.060 may be too small: wire/via-down 0.098, wire/via-up 0.060.
 (ZRT-026)
Via on layer (VIA3) needs more than one tracks
Warning: Layer M3 pitch 0.074 may be too small: wire/via-down 0.060, wire/via-up 0.080.
 (ZRT-026)
Wire on layer (M4) needs more than one tracks
Via on layer (VIA3) needs more than one tracks
Via on layer (VIA4) needs more than one tracks
Warning: Layer M4 pitch 0.074 may be too small: wire/via-down 0.107, wire/via-up 0.105.
 (ZRT-026)
Via on layer (VIA4) needs more than one tracks
Warning: Layer M5 pitch 0.120 may be too small: wire/via-down 0.135, wire/via-up 0.107.
 (ZRT-026)
Via on layer (VIA8) needs more than one tracks
Warning: Layer M8 pitch 0.120 may be too small: wire/via-down 0.107, wire/via-up 0.135.
 (ZRT-026)
Wire on layer (M9) needs more than one tracks
Via on layer (VIA8) needs more than one tracks
Via on layer (VIARDL) needs more than one tracks
Warning: Layer M9 pitch 0.120 may be too small: wire/via-down 0.135, wire/via-up 1.570.
 (ZRT-026)
Via on layer (VIARDL) needs more than one tracks
Warning: Layer MRDL pitch 0.600 may be too small: wire/via-down 4.500, wire/via-up 0.60
0. (ZRT-026)
Transition layer name: M3(2)
When applicable Min-max layer allow_pin_connection mode will allow paths of length 0.98
 outside the layer range.
```

```
Warning: Standard cell pin SAEDRVT14_AN3_0P75/X has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_AO221_0P5/B1 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_AOI22_1P5/A1 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_AO32_1/A3 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_OA21_1/A1 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_OA32_U_0P5/A1 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_OA32_U_0P5/B1 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_AO2BB2_1/A2 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_AN4_1/A1 has no valid via regions. (ZRT-044)
Warning: Standard cell pin SAEDRVT14_EO2_V1_0P75/A1 has no valid via regions. (ZRT-044)
Current Stage stats:
[End of Read DB] Elapsed real time: 0:00:00
[End of Read DB] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Read DB] Stage (MB): Used   24  Alloctr   24  Proc    5
[End of Read DB] Total (MB): Used   31  Alloctr   31  Proc 2552
Constructing data structure ...
Design statistics:
Design Bounding Box (0.00,0.00,60.33,60.20)
Number of routing layers = 10
layer M1, dir Ver, min width = 0.034, min space = 0.026 pitch = 0.074
layer M2, dir Hor, min width = 0.034, min space = 0.026 pitch = 0.06
layer M3, dir Ver, min width = 0.034, min space = 0.026 pitch = 0.074
layer M4, dir Hor, min width = 0.06, min space = 0.04 pitch = 0.074
layer M5, dir Ver, min width = 0.06, min space = 0.04 pitch = 0.12
layer M6, dir Hor, min width = 0.06, min space = 0.04 pitch = 0.12
layer M7, dir Ver, min width = 0.06, min space = 0.04 pitch = 0.12
layer M8, dir Hor, min width = 0.06, min space = 0.04 pitch = 0.12
layer M9, dir Ver, min width = 0.06, min space = 0.04 pitch = 0.12
layer MRDL, dir Hor, min width = 2, min space = 2 pitch = 0.6
Current Stage stats:
[End of Build Tech Data] Elapsed real time: 0:00:00
[End of Build Tech Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Tech Data] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build Tech Data] Total (MB): Used   32  Alloctr   32  Proc 2553
Net statistics:
Total number of nets     = 738
Number of nets to route  = 736
Number of single or zero port nets = 2
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build All Nets] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Build All Nets] Total (MB): Used   32  Alloctr   33  Proc 2553
Average gCell capacity  6.82     on layer (1)    M1
Average gCell capacity  9.74     on layer (2)    M2
Average gCell capacity  8.05     on layer (3)    M3
Average gCell capacity  8.04     on layer (4)    M4
Average gCell capacity  4.96     on layer (5)    M5
Average gCell capacity  4.95     on layer (6)    M6
Average gCell capacity  4.96     on layer (7)    M7
Average gCell capacity  4.95     on layer (8)    M8
Average gCell capacity  0.00     on layer (9)    M9
Average gCell capacity  0.00     on layer (10)   MRDL
```

```
Average number of tracks per gCell 8.08  on layer (1)    M1
Average number of tracks per gCell 9.94  on layer (2)    M2
Average number of tracks per gCell 8.08  on layer (3)    M3
Average number of tracks per gCell 8.06  on layer (4)    M4
Average number of tracks per gCell 4.99  on layer (5)    M5
Average number of tracks per gCell 4.98  on layer (6)    M6
Average number of tracks per gCell 4.99  on layer (7)    M7
Average number of tracks per gCell 4.98  on layer (8)    M8
Average number of tracks per gCell 4.99  on layer (9)    M9
Average number of tracks per gCell 0.99  on layer (10)   MRDL
Number of gCells = 102010
Current Stage stats:
[End of Build Congestion map] Elapsed real time: 0:00:00
[End of Build Congestion map] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Congestion map] Stage (MB): Used    1  Alloctr    1  Proc    3
[End of Build Congestion map] Total (MB): Used   34  Alloctr   34  Proc 2556
Net Count 736, Total HPWL 4615 microns
HPWL   0 ~  100 microns: Net Count      736     Total HPWL       4615 microns
HPWL 100 ~  200 microns: Net Count        0     Total HPWL          0 microns
HPWL 200 ~  300 microns: Net Count        0     Total HPWL          0 microns
HPWL 300 ~  400 microns: Net Count        0     Total HPWL          0 microns
HPWL 400 ~  500 microns: Net Count        0     Total HPWL          0 microns
HPWL 500 ~  600 microns: Net Count        0     Total HPWL          0 microns
HPWL 600 ~  700 microns: Net Count        0     Total HPWL          0 microns
HPWL 700 ~  800 microns: Net Count        0     Total HPWL          0 microns
HPWL 800 ~  900 microns: Net Count        0     Total HPWL          0 microns
HPWL 900 ~ 1000 microns: Net Count        0     Total HPWL          0 microns
HPWL     > 1000 microns: Net Count        0     Total HPWL          0 microns
Number of user frozen nets = 0
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used    2  Alloctr    3  Proc    4
[End of Build Data] Total (MB): Used   34  Alloctr   34  Proc 2556
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Blocked Pin Detection] Stage (MB): Used  212  Alloctr  212  Proc  215
[End of Blocked Pin Detection] Total (MB): Used  246  Alloctr  246  Proc 2771
Information: Using 1 threads for routing. (ZRT-444)
multi gcell levels ON
```

```
Start GR phase 0
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Initial Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Initial Routing] Total (MB): Used  246  Alloctr  247  Proc 2772
Initial. Routing result:
Initial. Both Dirs: Overflow =    12 Max = 3 GRCs =    24 (0.12%)
Initial. H routing: Overflow =     8 Max = 3 (GRCs =  1) GRCs =    14 (0.14%)
Initial. V routing: Overflow =     3 Max = 1 (GRCs = 10) GRCs =    10 (0.10%)
Initial. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M2         Overflow =     8 Max = 3 (GRCs =  1) GRCs =    14 (0.14%)
Initial. M3         Overflow =     3 Max = 1 (GRCs = 10) GRCs =    10 (0.10%)
Initial. M4         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M5         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M6         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M7         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M8         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M9         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. MRDL       Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

Initial. Total Wire Length = 4773.31
Initial. Layer M1 wire length = 32.93
Initial. Layer M2 wire length = 2112.95
Initial. Layer M3 wire length = 2476.79
Initial. Layer M4 wire length = 150.65
Initial. Layer M5 wire length = 0.00
Initial. Layer M6 wire length = 0.00
Initial. Layer M7 wire length = 0.00
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 4480
Initial. Via VIA12SQ_C count = 1871
Initial. Via VIA23SQ_C count = 2575
Initial. Via VIA34SQ_C count = 34
Initial. Via VIA45SQ count = 0
Initial. Via VIA56SQ count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
```

```
Congestion utilization per direction:
Average vertical track utilization   =  2.13 %
Peak    vertical track utilization   = 42.11 %
Average horizontal track utilization =  1.92 %
Peak    horizontal track utilization = 37.04 %

Current Stage stats:
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used   -1  Alloctr   -1  Proc    0
[GR: Done] Total (MB): Used  245  Alloctr  246  Proc 2772
GR Total stats:
[GR: Done] Elapsed real time: 0:00:02
[GR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:01
[GR: Done] Stage (MB): Used  238  Alloctr  238  Proc  225
[GR: Done] Total (MB): Used  245  Alloctr  246  Proc 2772
Writing out congestion map...
Updating congestion ...
Updating congestion ...
[DBOUT] Elapsed real time: 0:00:00
[DBOUT] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[DBOUT] Stage (MB): Used  -24  Alloctr  -24  Proc    0
[DBOUT] Total (MB): Used   36  Alloctr   37  Proc 2772
Final total stats:
[End of Global Routing] Elapsed real time: 0:00:02
[End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:01
[End of Global Routing] Stage (MB): Used   29  Alloctr   29  Proc  225
[End of Global Routing] Total (MB): Used   36  Alloctr   37  Proc 2772
```

```
****************************************
Report : report_placement
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Fri Apr 19 16:34:28 2024
****************************************

  Wire length report (all)
  ================
  wire length in design temp_data_setup: 4354.517 microns.
  wire length in design temp_data_setup (see through blk pins): 4354.517 microns.

  Physical hierarchy violations report
  ================================
  Violations in design temp_data_setup:
     0 cells have placement violation.

  Voltage area violations report
  ================================
  Voltage area placement violations in design temp_data_setup:
     0 cells placed outside the voltage area which they belong to.

Information: Default error view temp_data_setup_dpplace.err is created in GUI error bro
wser. (DPP-054)
Information: Saving 'i2c_master_top:temp_data_setup.design' to 'i2c_master_top:temp_flo
orplane_placed.design'. (DES-028)
Information: Saving 'i2c_master_top:temp_data_setup.design' to 'i2c_master_top:i2c_mast
er_top_2_floorplan_ends.design'. (DES-028)
Saving library 'i2c_master_top'
Information: Decrementing open_count of block 'i2c_master_top:temp_data_setup.design' t
o 1. (DES-022)
Closing library 'i2c_master_top'
Maximum memory usage for this session: 624.72 MB
Maximum memory usage for this session including child processes: 624.72 MB
CPU usage for this session:     22 seconds (  0.01 hours)
Elapsed time for this session:    575 seconds (  0.16 hours)
Thank you for using IC Compiler II.
```

```
Successfully compiled PG.
Overall runtime: 0 seconds.
Loading cell instances...
Number of Standard Cells: 715
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 58
Number of VDD Vias: 144
Number of VDD Terminals: 41
Number of VSS Wires: 58
Number of VSS Vias: 144
Number of VSS Terminals: 41
**************Verify net VDD connectivity*****************
  Number of floating wires: 34
  Number of floating vias: 0
  Number of floating std cells: 715
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 1
  Number of floating hierarchical blocks: 0
************************************************************
**************Verify net VSS connectivity*****************
  Number of floating wires: 34
  Number of floating vias: 0
  Number of floating std cells: 715
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 1
  Number of floating hierarchical blocks: 0
************************************************************
Overall runtime: 0 seconds.
Information: Saving 'i2c_master_top:temp_floorplan_ends.design' to 'i2c_master_top:i2c_
master_top_3_powerplan_ends.design'. (DES-028)
Saving library 'i2c_master_top'
Information: Decrementing open_count of block 'i2c_master_top:temp_floorplan_ends.desig
n' to 1. (DES-022)
Closing library 'i2c_master_top'
Maximum memory usage for this session: 301.07 MB
Maximum memory usage for this session including child processes: 301.07 MB
CPU usage for this session:     20 seconds (  0.01 hours)
Elapsed time for this session:    601 seconds (  0.17 hours)
Thank you for using IC Compiler II.
```

Lab2 Placement & Route

Results

```
************************************************************
* CTS STEP: Summary
************************************************************
merge_clock_gates Statistics: Total
    ICG                     0
    Merged                  0
    Survived                0
    Removed                 0
    ICG at the end          0


Summary of messages during CTS:
============================================================
  Tag   Count  Type          Description
------------------------------------------------------------
 No error or warning message.
Number of Site types in the design = 1
Setting up Chip Core
Chip Core shape: (100000 100000) (503300 502000)
Number of VARs = 1
Number of unique PDs = 1
Number of Power Domains = 1
Number of Voltage Areas = 1
Number of supply Nets = 2
Number of used supplies = 0
Blocked VAs:
INFO: sweep stats: 0 gates / 0 nets gobbled, 0 gates (0 seq) simplified
Running initial placement
------------------------------------------------------------
running create_placement
Information: The RC mode used is VR for design 'i2c_master_top'. (NEX-022)
Information: Update timing completed net estimation for all the timing graph nets (TIM-
111)
Information: Net estimation statistics: timing graph nets = 736, routed nets = 0, acros
s physical hierarchy nets = 0, parasitics cached nets = 736, delay annotated nets = 0,
parasitics annotated nets = 0, multi-voltage nets = 0. (TIM-112)
************************************************************
Timer Settings:
Delay Calculation Style:                    auto
Signal Integrity Analysis:                  disabled
Timing Window Analysis:                     disabled
Advanced Waveform Propagation:              disabled
Variation Type:                             fixed_derate
Clock Reconvergence Pessimism Removal:      disabled
Advanced Receiver Model:                    disabled
************************************************************
Warning: Technology layer 'M4' setting 'pitch' is not valid (NEX-001)
Warning: Technology layer 'M8' setting 'routing-direction' is not valid (NEX-001)
Warning: Technology layer 'M9' setting 'routing-direction' is not valid (NEX-001)
Warning: Technology layer 'MRDL' setting 'routing-direction' is not valid (NEX-001)
Warning: Technology layer 'MRDL' setting 'pitch' is not valid (NEX-001)
Warning: Parasitic Tech Library layer 'M1' parameter 'SMIN' = 0.040 does not match 0.02
6 of technology file (NEX-007)
Warning: Parasitic Tech Library layer 'M2' parameter 'SMIN' = 0.040 does not match 0.02
6 of technology file (NEX-007)
```

```
Core Area = 21 X 21 ()
GRE layer bins: None-None, M1-M2, M3-M4, M5-M6

Bin                         Count      OptDist      MinLen
-------------------------------------------------------------
None-None                     736          0.0         0.0
M1-M2                           0          0.0         0.0
M3-M4                           0          0.0         0.0
M5-M6                           0          0.0         0.0
-------------------------------------------------------------
Total                           0


Roi-HfsDrc SN: 1798569713 435980330 0 (307.607178)

Processing Buffer Trees  (ROI) ...

    [1]  10% ...
    [2]  20% ...
    [2] 100%  Done

                 Deleted        Added
------------ ------------ ------------
    Buffers:           16            5
  Inverters:            5            1
------------ ------------ ------------
      Total:           21            6
------------ ------------ ------------

Number of Drivers Sized: 0 [0.00%]
                      P: 0 [0.00%]
                      N: 0 [0.00%]


Bin                         Count      OptDist      MinLen
-------------------------------------------------------------
None-None                     721          0.0         0.0
M1-M2                           0          0.0         0.0
M3-M4                           0          0.0         0.0
M5-M6                           0          0.0         0.0
-------------------------------------------------------------
Total                           0
```

```
    Scenario func_slow  WNS = 0.000000, TNS = 0.000000, NVP = 0

     ELAPSED  WORST NEG TOTAL NEG              MAX       MAX     BUFFER    INVERTER   L
VTH      LVTH      PEAK
      TIME      SLACK     SLACK     AREA    TRAN COST CAP COST    COUNT     COUNT     C
OUNT    PERCENT   MEMORY
     --------- --------- --------- --------- --------- --------- --------- --------- ---
------ --------- ---------
      0:11:17     0.000     0.000   325.008     0.000     0.000         5       155
     0     0.000       579


    Scenario func_slow  WNS = 0.000000, TNS = 0.000000, NVP = 0

     ELAPSED  WORST NEG TOTAL NEG              MAX       MAX     BUFFER    INVERTER   L
VTH      LVTH      PEAK
      TIME      SLACK     SLACK     AREA    TRAN COST CAP COST    COUNT     COUNT     C
OUNT    PERCENT   MEMORY
     --------- --------- --------- --------- --------- --------- --------- --------- ---
------ --------- ---------
      0:11:17     0.000     0.000   325.008     0.000     0.000         5       155
     0     0.000       579

Warning: Technology layer 'M4' setting 'pitch' is not valid (NEX-001)
Warning: Technology layer 'M8' setting 'routing-direction' is not valid (NEX-001)
Warning: Technology layer 'M9' setting 'routing-direction' is not valid (NEX-001)
Warning: Technology layer 'MRDL' setting 'routing-direction' is not valid (NEX-001)
Warning: Technology layer 'MRDL' setting 'pitch' is not valid (NEX-001)
Information: Ending place_opt / initial_drc / High Fanout Synthesis (FLW-8001)
Information: Time: 2024-04-19 17:12:29 / Session: 0.19 hr / Command: 0.01 hr / Memory:
579 MB (FLW-8100)


Information: Ending place_opt / initial_drc (FLW-8001)
Information: Time: 2024-04-19 17:12:29 / Session: 0.19 hr / Command: 0.01 hr / Memory:
579 MB (FLW-8100)

Information: Starting place_opt / initial_opto (FLW-8000)
Information: Time: 2024-04-19 17:12:29 / Session: 0.19 hr / Command: 0.01 hr / Memory:
579 MB (FLW-8100)


Information: Starting place_opt / initial_opto / Optimization (FLW-8000)
Information: Time: 2024-04-19 17:12:29 / Session: 0.19 hr / Command: 0.01 hr / Memory:
579 MB (FLW-8100)

Information: The net parasitics of block i2c_master_top are cleared. (TIM-123)
Information: The stitching and editing of coupling caps is turned OFF for design 'i2c_m
aster_top:temp_powerplan_ends.design'. (TIM-125)
```

```
    Scenario func_fast  WNS = 0.000000, TNS = 0.000000, NVP = 0
    Scenario func_slow  WNS = 0.000000, TNS = 0.000000, NVP = 0

     ELAPSED  WORST NEG TOTAL NEG             MAX       MAX     BUFFER    INVERTER   L
VTH      LVTH      PEAK
      TIME      SLACK     SLACK     AREA    TRAN COST CAP COST    COUNT     COUNT     C
OUNT    PERCENT   MEMORY
    --------- --------- --------- --------- --------- --------- --------- --------- ---
------ --------- ---------
      0:11:18     0.000     0.000   325.008     0.000     0.000         5       155
     0     0.000       579

Running initial optimization step.
Place-opt command begin                  CPU:    34 s (  0.01 hr )  ELAPSE:   679 s (
 0.19 hr )  MEM-PEAK:   579 MB
Warning: Cannot find any max transition constraint on the design. (OPT-070)

Place-opt timing update complete         CPU:    34 s (  0.01 hr )  ELAPSE:   679 s (
 0.19 hr )  MEM-PEAK:   579 MB

Place-opt initial QoR
_____________________
Scenario Mapping Table
1: func_fast
2: func_slow

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2reg_default**
5: **reg2out_default**
6: **in2out_default**
7: wb_clk_i
```

```
----------------------------------------------------------------------
PATHGROUP QOR
----------------------------------------------------------------------------------------------
----------------------------------------------------------------------
Scene  PG      WNS        TNS    NSV      WHV        THV    NHV
    1   1   0.0000     0.0000      0        -          -      -
    1   2   0.0000     0.0000      0        -          -      -
    1   3   0.0000     0.0000      0        -          -      -
    1   4   0.0000     0.0000      0        -          -      -
    1   5   0.0000     0.0000      0        -          -      -
    1   6   0.0000     0.0000      0        -          -      -
    1   7   0.0000     0.0000      0        -          -      -
    2   1   0.0000     0.0000      0        -          -      -
    2   2   0.0000     0.0000      0        -          -      -
    2   3   0.0000     0.0000      0        -          -      -
    2   4   0.0000     0.0000      0        -          -      -
    2   5   0.0000     0.0000      0        -          -      -
    2   6   0.0000     0.0000      0        -          -      -
    2   7   0.0000     0.0000      0        -          -      -
----------------------------------------------------------------------------------------------
----------------------------------------------------------------------
SCENARIO QOR
----------------------------------------------------------------------------------------------
----------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage
    1   *   0.0000     0.0000   0.0000      0        -          -      -        0     0
.0000        0 129079.828
    2   *   0.0000     0.0000   0.0000      0        -          -      -        0     0
.0000        0 129079.828
----------------------------------------------------------------------------------------------
----------------------------------------------------------------------
DESIGN QOR
----------------------------------------------------------------------------------------------
----------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage         Area    InstCnt     BufCnt     InvCnt
    *   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 129079.828       325.01        700          5        155
----------------------------------------------------------------------------------------------
----------------------------------------------------------------------

Place-opt initial QoR Summary       WNS        TNS   R2RTNS    NSV      WHV        THV
   NHV  MaxTrnV  MaxCapV    Leakage         Area    InstCnt
Place-opt initial QoR Summary    0.0000     0.0000   0.0000      0   0.0000     0.0000
     0        0        0 129079.828       325.01        700
Information: The netlist change observers are disabled for incremental extraction. (TIM
-126)
INFO: using 1 threads
```

```
 PDC checks will not be performed on this layer. (PDC-003)
=====> Processed 69 ref cells (25 fillers) from library

Bounds/Regions In This Design:
        Area    Num Cells  Exclusive Name
 (square um)
     1621.27          702        Yes DEFAULT_VA

Warning: max_legality_failures=5000 ignored.
        To use it, set limit_legality_checks to true.
Warning: max_legality_check_range=500 ignored.
        To use it, set limit_legality_checks to true.
Starting legalizer.
Warning: Exclusive bound 'DEFAULT' has no cells.
Optimizing Exclusive Bound 'DEFAULT_VA' (2/2)
    Done Exclusive Bound 'DEFAULT_VA' (2/2) (0 sec)
Legalization complete (0 total sec)

****************************************
  Report : Placement Attempts
  Site   : unit
****************************************

number of cells:                    702
number of references:                69
number of site rows:                 67
number of locations attempted:    17552
number of locations failed:           0  (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         702 (7338 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.205 um ( 0.34 row height)
rms weighted cell displacement:   0.205 um ( 0.34 row height)
max cell displacement:            0.600 um ( 1.00 row height)
avg cell displacement:            0.183 um ( 0.30 row height)
avg weighted cell displacement:   0.183 um ( 0.30 row height)
number of cells moved:              697
number of large displacements:        0
large displacement threshold:     3.000 row height
```

```
Displacements of worst 10 cells:
Cell: placeoptlc_7 (SAEDRVT14_TIE0_4)
  Input location: (10,10)
  Legal location: (10,10.6)
  Displacement:   0.600 um ( 1.00 row height)
Cell: byte_controller/bit_controller/U148 (SAEDRVT14_INV_1)
  Input location: (17.8408,32.0868)
  Legal location: (17.844,31.6)
  Displacement:   0.487 um ( 0.81 row height)
Cell: byte_controller/bit_controller/U217 (SAEDRVT14_AO221_0P5)
  Input location: (24.7036,44.0825)
  Legal location: (24.726,43.6)
  Displacement:   0.483 um ( 0.81 row height)
Cell: byte_controller/U92 (SAEDRVT14_INV_1)
  Input location: (30.4539,13.1326)
  Legal location: (30.424,13.6)
  Displacement:   0.468 um ( 0.78 row height)
Cell: byte_controller/U78 (SAEDRVT14_INV_1)
  Input location: (18.6501,17.9649)
  Legal location: (18.584,18.4)
  Displacement:   0.440 um ( 0.73 row height)
Cell: U203 (SAEDRVT14_OAI22_1)
  Input location: (30.6612,24.5778)
  Legal location: (30.646,25)
  Displacement:   0.422 um ( 0.70 row height)
Cell: byte_controller/bit_controller/U195 (SAEDRVT14_INV_1)
  Input location: (22.7624,34.6655)
  Legal location: (23.172,34.6)
  Displacement:   0.415 um ( 0.69 row height)
Cell: byte_controller/bit_controller/sub_260/U20 (SAEDRVT14_NR2_1)
  Input location: (33.8522,41.7006)
  Legal location: (33.458,41.8)
  Displacement:   0.407 um ( 0.68 row height)
Cell: byte_controller/bit_controller/sub_260/U25 (SAEDRVT14_OR2_0P5)
  Input location: (31.8352,31.3935)
  Legal location: (31.83,31)
  Displacement:   0.394 um ( 0.66 row height)
Cell: byte_controller/U58 (SAEDRVT14_INV_1)
  Input location: (19.4776,13.207)
  Legal location: (19.472,13.6)
  Displacement:   0.393 um ( 0.66 row height)
```

```
Information: Extraction observers are detached as design net change threshold is reache
d.
Completed Legalization, Elapsed time =   0: 0: 0
Moved 697 out of 702 cells, ratio = 0.992877
Total displacement = 148.478500(um)
Max displacement = 0.600000(um), placeoptlc_7 (10.000000, 10.600000, 4) => (10.000000,
10.600000, 0)
Displacement histogram:
  0 ~  10% cells displacement <=      0.07(um)
  0 ~  20% cells displacement <=      0.11(um)
  0 ~  30% cells displacement <=      0.14(um)
  0 ~  40% cells displacement <=      0.18(um)
  0 ~  50% cells displacement <=      0.21(um)
  0 ~  60% cells displacement <=      0.24(um)
  0 ~  70% cells displacement <=      0.27(um)
  0 ~  80% cells displacement <=      0.30(um)
  0 ~  90% cells displacement <=      0.33(um)
  0 ~ 100% cells displacement <=      0.60(um)
Information: The net parasitics of block i2c_master_top are cleared. (TIM-123)
Legalization succeeded.
----------------------------------------------------------------
Information: The stitching and editing of coupling caps is turned OFF for design 'i2c_m
aster_top:temp_powerplan_ends.design'. (TIM-125)
```

```
Layer bins has 1 layers:
-----------------------------------------
Layer bin    = 0
Routing rule = { MinLayer = M4(25)  MaxLayer = M7(31)  MaxVoltg = uninit }
Delay per mm = [0.069 0.065]
Stage delay  = [0.009865 0.009907] (ns)
Stage length = [144 152] (um)
Demand cost  = 1.000000
-----------------------------------------
APS-LA[ 1 ]: 0 block nets demoted in bin 0 (0 - 0)

Place-opt optimization Phase 37 Iter  1         0.00        0.00      0.00         0
     325.01   125152.38         702              0.20       686

Place-opt optimization Phase 38 Iter  1         0.00        0.00      0.00         0
     325.01   125152.38         702              0.20       686
Place-opt optimization Phase 38 Iter  2         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686

Disable clock slack update for ideal clocks
Place-opt optimization Phase 39 Iter  1         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686
INFO: cellmap features:  adv-rules=(N), pdc=(N), clock-rules=(Y)

Place-opt optimization Phase 40 Iter  1         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686
Place-opt optimization Phase 40 Iter  2         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686

Place-opt optimization Phase 41 Iter  1         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686

Place-opt optimization Phase 42 Iter  1         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686

Place-opt optimization Phase 43 Iter  1         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686

Place-opt optimization Phase 44 Iter  1         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686
Place-opt optimization Phase 44 Iter  2         0.00        0.00      0.00         0
     323.19   124223.53         702              0.20       686

Disable clock slack update for ideal clocks
```

```
=====> Processed 75 ref cells (25 fillers) from library

Bounds/Regions In This Design:
        Area    Num Cells  Exclusive Name
 (square um)
     1621.27          702        Yes DEFAULT_VA

Starting legalizer.
Warning: Exclusive bound 'DEFAULT' has no cells.
Optimizing Exclusive Bound 'DEFAULT_VA' (2/2)
    Done Exclusive Bound 'DEFAULT_VA' (2/2) (0 sec)
Legalization complete (0 total sec)

****************************************
  Report : Placement Attempts
  Site   : unit
****************************************

number of cells:                    702
number of references:                75
number of site rows:                 67
number of locations attempted:    15419
number of locations failed:           0  (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.
```

```
****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         702 (7283 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.000 um ( 0.00 row height)
rms weighted cell displacement:   0.000 um ( 0.00 row height)
max cell displacement:            0.000 um ( 0.00 row height)
avg cell displacement:            0.000 um ( 0.00 row height)
avg weighted cell displacement:   0.000 um ( 0.00 row height)
number of cells moved:               0
number of large displacements:       0
large displacement threshold:     3.000 row height

Displacements of worst 10 cells:
Cell: U143 (SAEDRVT14_AN3_0P5)
  Input location: (31.016,17.2)
  Legal location: (31.016,17.2)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U141 (SAEDRVT14_AN3_0P5)
  Input location: (33.014,17.8)
  Legal location: (33.014,17.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U67 (SAEDRVT14_AN3_0P5)
  Input location: (24.356,29.8)
  Legal location: (24.356,29.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U308 (SAEDRVT14_AN2_MM_1)
  Input location: (24.356,22)
  Legal location: (24.356,22)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U14 (SAEDRVT14_AN2_MM_1)
  Input location: (45.15,38.8)
  Legal location: (45.15,38.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U288 (SAEDRVT14_AN2_MM_1)
  Input location: (28.5,19.6)
  Legal location: (28.5,19.6)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U266 (SAEDRVT14_AN2_MM_1)
  Input location: (21.618,22.6)
  Legal location: (21.618,22.6)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U199 (SAEDRVT14_AN2_MM_1)
  Input location: (22.728,41.2)
  Legal location: (22.728,41.2)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U165 (SAEDRVT14_AN2_MM_1)
  Input location: (24.208,32.8)
  Legal location: (24.208,32.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U147 (SAEDRVT14_AN3_0P5)
  Input location: (35.012,16)
  Legal location: (35.012,16)
  Displacement:   0.000 um ( 0.00 row height)
```

```
Place-opt final QoR
____________________
Scenario Mapping Table
1: func_fast
2: func_slow

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2reg_default**
5: **reg2out_default**
6: **in2out_default**
7: wb_clk_i

--------------------------------------------------------------------------------
--------------------------------------------------------------------
PATHGROUP QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS    NSV      WHV        THV    NHV
    1   1   0.0000     0.0000      0   0.0000     0.0000      0
    1   2   0.0000     0.0000      0   0.0000     0.0000      0
    1   3   0.0000     0.0000      0   0.0000     0.0000      0
    1   4   0.0000     0.0000      0   0.0000     0.0000      0
    1   5   0.0000     0.0000      0   0.0000     0.0000      0
    1   6   0.0000     0.0000      0   0.0000     0.0000      0
    1   7   0.0000     0.0000      0   0.0000     0.0000      0
    2   1   0.0000     0.0000      0   0.0000     0.0000      0
    2   2   0.0000     0.0000      0   0.0000     0.0000      0
    2   3   0.0000     0.0000      0   0.0000     0.0000      0
    2   4   0.0000     0.0000      0   0.0000     0.0000      0
    2   5   0.0000     0.0000      0   0.0000     0.0000      0
    2   6   0.0000     0.0000      0   0.0000     0.0000      0
    2   7   0.0000     0.0000      0   0.0000     0.0000      0
--------------------------------------------------------------------------------
--------------------------------------------------------------------
```

```
--------------------------------------------------------------------
SCENARIO QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage
    1   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103504.695
    2   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103504.695
--------------------------------------------------------------------------------
--------------------------------------------------------------------
DESIGN QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage         Area    InstCnt     BufCnt     InvCnt
    *   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103504.695       323.37        702          5        155
--------------------------------------------------------------------------------
--------------------------------------------------------------------
```

```
Legalization complete (0 total sec)

****************************************
  Report : Placement Attempts
  Site   : unit
****************************************

number of cells:                    702
number of references:                75
number of site rows:                 67
number of locations attempted:    15419
number of locations failed:           0  (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         702 (7283 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.000 um ( 0.00 row height)
rms weighted cell displacement:   0.000 um ( 0.00 row height)
max cell displacement:            0.000 um ( 0.00 row height)
avg cell displacement:            0.000 um ( 0.00 row height)
avg weighted cell displacement:   0.000 um ( 0.00 row height)
number of cells moved:                0
number of large displacements:        0
large displacement threshold:     3.000 row height
```

```
****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         702 (7283 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.000 um ( 0.00 row height)
rms weighted cell displacement:   0.000 um ( 0.00 row height)
max cell displacement:            0.000 um ( 0.00 row height)
avg cell displacement:            0.000 um ( 0.00 row height)
avg weighted cell displacement:   0.000 um ( 0.00 row height)
number of cells moved:                0
number of large displacements:        0
large displacement threshold:     3.000 row height

Displacements of worst 10 cells:
Cell: U143 (SAEDRVT14_AN3_0P5)
  Input location: (31.016,17.2)
  Legal location: (31.016,17.2)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U141 (SAEDRVT14_AN3_0P5)
  Input location: (33.014,17.8)
  Legal location: (33.014,17.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U67 (SAEDRVT14_AN3_0P5)
  Input location: (24.356,29.8)
  Legal location: (24.356,29.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U308 (SAEDRVT14_AN2_MM_1)
  Input location: (24.356,22)
  Legal location: (24.356,22)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U14 (SAEDRVT14_AN2_MM_1)
  Input location: (45.15,38.8)
  Legal location: (45.15,38.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U288 (SAEDRVT14_AN2_MM_1)
  Input location: (28.5,19.6)
  Legal location: (28.5,19.6)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U266 (SAEDRVT14_AN2_MM_1)
  Input location: (21.618,22.6)
  Legal location: (21.618,22.6)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U199 (SAEDRVT14_AN2_MM_1)
  Input location: (22.728,41.2)
  Legal location: (22.728,41.2)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U165 (SAEDRVT14_AN2_MM_1)
  Input location: (24.208,32.8)
  Legal location: (24.208,32.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U147 (SAEDRVT14_AN3_0P5)
  Input location: (35.012,16)
  Legal location: (35.012,16)
  Displacement:   0.000 um ( 0.00 row height)

Legalization succeeded.
```

```
************************************************
Report           : create_qor_snapshot (place_qor_snp)
Design           : i2c_master_top
Version          : R-2020.09-SP3
Date             : Fri Apr 19 17:13:58 2024
Time unit        : 1.00ns
Resistance unit  : 1.00MOhm
Capacitance unit: 1.00fF
Voltage unit     : 1.00V
Current unit     : 1.00uA
Power unit       : 1.00pW
Location         : /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_rel
ease/lab2_pnr/work/./
************************************************
No. of scenario = 2
s1 = func_fast
s2 = func_slow
---------------------------------------------------------------------------
WNS of each timing group:                    s1        s2
---------------------------------------------------------------------------
wb_clk_i                                  1.3766    1.3631
---------------------------------------------------------------------------
Setup WNS:                                1.3766    1.3631      1.3631
Setup TNS:                                0.0000    0.0000      0.0000
Number of setup violations:                    0         0           0
Hold WNS:                                 0.0242    0.0247      0.0242
Hold TNS:                                 0.0000    0.0000      0.0000
Number of hold violations:                     0         0           0
Number of max trans violations:                0         0           0
Number of max cap violations:                  0         0           0
Number of min pulse width violations:          0         0           0
---------------------------------------------------------------------------
Area:                                                           323.365
Cell count:                                                         702
Buf/inv cell count:                                                 160
Std cell utilization:                                            0.1995
CPU(s):                                                             69
Mem(Mb):                                                           686
Host name:                                                        ws33
```

```
---------------------------------------------------------------------------
Histogram:              s1   s2
---------------------------------------------------------------------------
Max violations:          0    0
   above ~ -0.7   ---    0    0
    -0.6 ~ -0.7   ---    0    0
    -0.5 ~ -0.6   ---    0    0
    -0.4 ~ -0.5   ---    0    0
    -0.3 ~ -0.4   ---    0    0
    -0.2 ~ -0.3   ---    0    0
    -0.1 ~ -0.2   ---    0    0
       0 ~ -0.1   ---    0    0
---------------------------------------------------------------------------
Min violations:          0    0
  -0.06 ~ above   ---    0    0
  -0.05 ~ -0.06   ---    0    0
  -0.04 ~ -0.05   ---    0    0
  -0.03 ~ -0.04   ---    0    0
  -0.02 ~ -0.03   ---    0    0
  -0.01 ~ -0.02   ---    0    0
      0 ~ -0.01   ---    0    0
---------------------------------------------------------------------------
```

```
****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         713 (7470 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.000 um ( 0.00 row height)
rms weighted cell displacement:   0.000 um ( 0.00 row height)
max cell displacement:            0.000 um ( 0.00 row height)
avg cell displacement:            0.000 um ( 0.00 row height)
avg weighted cell displacement:   0.000 um ( 0.00 row height)
number of cells moved:                0
number of large displacements:        0
large displacement threshold:     3.000 row height

Displacements of worst 10 cells:
Cell: U143 (SAEDRVT14_AN3_0P5)
  Input location: (31.09,16.6)
  Legal location: (31.09,16.6)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U141 (SAEDRVT14_AN3_0P5)
  Input location: (32.57,17.8)
  Legal location: (32.57,17.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U67 (SAEDRVT14_AN3_0P5)
  Input location: (23.838,28.6)
  Legal location: (23.838,28.6)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/clockctmTdsLR_4_893 (SAEDRVT14_AN2_MM_0P5)
  Input location: (18.88,14.8)
  Legal location: (18.88,14.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U165 (SAEDRVT14_AN2_0P5)
  Input location: (24.208,32.8)
  Legal location: (24.208,32.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/U14 (SAEDRVT14_AN2_MM_0P5)
  Input location: (44.928,38.8)
  Legal location: (44.928,38.8)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/clockctmTdsLR_2_876 (SAEDRVT14_AN2_MM_0P5)
  Input location: (17.622,40)
  Legal location: (17.622,40)
  Displacement:   0.000 um ( 0.00 row height)
Cell: byte_controller/bit_controller/clockctmTdsLR_1_875 (SAEDRVT14_AN2_MM_0P5)
  Input location: (18.288,41.2)
  Legal location: (18.288,41.2)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U308 (SAEDRVT14_AN2_0P5)
  Input location: (22.358,21.4)
  Legal location: (22.358,21.4)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U147 (SAEDRVT14_AN3_0P5)
  Input location: (35.16,16)
  Legal location: (35.16,16)
  Displacement:   0.000 um ( 0.00 row height)

Legalization succeeded.
```

```
Global-route-opt final QoR
_________________________
Scenario Mapping Table
1: func_fast
2: func_slow

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2reg_default**
5: **reg2out_default**
6: **in2out_default**
7: wb_clk_i

--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
PATHGROUP QOR
--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS    NSV      WHV        THV    NHV
    1   1   0.0000     0.0000      0   0.0000     0.0000      0
    1   2   0.0000     0.0000      0   0.0000     0.0000      0
    1   3   0.0000     0.0000      0   0.0000     0.0000      0
    1   4   0.0000     0.0000      0   0.0000     0.0000      0
    1   5   0.0000     0.0000      0   0.0000     0.0000      0
    1   6   0.0000     0.0000      0   0.0000     0.0000      0
    1   7   0.0000     0.0000      0   0.0000     0.0000      0
    2   1   0.0000     0.0000      0   0.0000     0.0000      0
    2   2   0.0000     0.0000      0   0.0000     0.0000      0
    2   3   0.0000     0.0000      0   0.0000     0.0000      0
    2   4   0.0000     0.0000      0   0.0000     0.0000      0
    2   5   0.0000     0.0000      0   0.0000     0.0000      0
    2   6   0.0000     0.0000      0   0.0000     0.0000      0
    2   7   0.0000     0.0000      0   0.0000     0.0000      0
--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
SCENARIO QOR
--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage
    1   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103263.047
    2   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103263.047
--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
DESIGN QOR
--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage          Area    InstCnt     BufCnt     InvCnt
    *   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103263.047       331.67        713          5        145
--------------------------------------------------------------------------------------------
--------------------------------------------------------------------
```

```
Global-route-opt final QoR Summary         WNS        TNS   R2RTNS    NSV      WHV
   THV    NHV  MaxTrnV  MaxCapV    Leakage         Area    InstCnt
Global-route-opt final QoR Summary      0.0000     0.0000   0.0000      0   0.0000
0.0000      0        0        0 103263.047       331.67        713

Global-route-opt command complete                CPU:    84 s (  0.02 hr )  ELAPSE:   5
88 s (  0.16 hr )  MEM-PEAK:  1186 MB
Global-route-opt command statistics  CPU=25 sec (0.01 hr) ELAPSED=25 sec (0.01 hr) MEM-
PEAK=1.158 GB
Information: Running auto PG connection. (NDM-099)
Information: Ending 'clock_opt -from route_clock -to final_opto' (FLW-8001)
Information: Time: 2024-04-20 01:33:53 / Session: 0.16 hr / Command: 0.01 hr / Memory:
1187 MB (FLW-8100)
****************************************
Report          : create_qor_snapshot (clock)
Design          : i2c_master_top
Version         : R-2020.09-SP3
Date            : Sat Apr 20 01:33:55 2024
Time unit       : 1.00ns
Resistance unit : 1.00MOhm
Capacitance unit: 1.00fF
Voltage unit    : 1.00V
Current unit    : 1.00uA
Power unit      : 1.00pW
Location        : /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_rel
ease/lab2_pnr/work/./
****************************************
No. of scenario = 2
s1 = func_fast
s2 = func_slow
------------------------------------------------------------------------
WNS of each timing group:                    s1        s2
------------------------------------------------------------------------
wb_clk_i                                  1.3226    1.2999
------------------------------------------------------------------------
Setup WNS:                                1.3226    1.2999      1.2999
Setup TNS:                                0.0000    0.0000      0.0000
Number of setup violations:                    0         0           0
Hold WNS:                                 0.0265    0.0272      0.0265
Hold TNS:                                 0.0000    0.0000      0.0000
Number of hold violations:                     0         0           0
Number of max trans violations:                0         0           0
Number of max cap violations:                  0         0           0
Number of min pulse width violations:          0         0           0
------------------------------------------------------------------------
Area:                                                           331.668
Cell count:                                                        713
Buf/inv cell count:                                                150
Std cell utilization:                                           0.2046
CPU(s):                                                            85
Mem(Mb):                                                         1186
Host name:                                                       ws33
```

```
-------------------------------------------------------------------------
Histogram:              s1   s2
-------------------------------------------------------------------------
Max violations:          0    0
   above ~ -0.7  ---     0    0
    -0.6 ~ -0.7  ---     0    0
    -0.5 ~ -0.6  ---     0    0
    -0.4 ~ -0.5  ---     0    0
    -0.3 ~ -0.4  ---     0    0
    -0.2 ~ -0.3  ---     0    0
    -0.1 ~ -0.2  ---     0    0
       0 ~ -0.1  ---     0    0
-------------------------------------------------------------------------
Min violations:          0    0
  -0.06 ~ above  ---     0    0
  -0.05 ~ -0.06  ---     0    0
  -0.04 ~ -0.05  ---     0    0
  -0.03 ~ -0.04  ---     0    0
  -0.02 ~ -0.03  ---     0    0
  -0.01 ~ -0.02  ---     0    0
      0 ~ -0.01  ---     0    0
-------------------------------------------------------------------------
Snapshot (clock) is created and stored under "/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab2_pnr/work/./" directory
Information: The command 'save_block' cleared the undo history. (UNDO-016)
Information: Saving 'i2c_master_top:temp_place_ends.design' to 'i2c_master_top:i2c_master_top_5_clock_ends.design'. (DES-028)
Saving library 'i2c_master_top'
Information: Decrementing open_count of block 'i2c_master_top:temp_place_ends.design' to 1. (DES-022)
Closing library 'i2c_master_top'
Information: The net parasitics of block i2c_master_top are cleared. (TIM-123)
Maximum memory usage for this session: 1186.76 MB
Maximum memory usage for this session including child processes: 1186.76 MB
CPU usage for this session:     85 seconds (  0.02 hours)
Elapsed time for this session:    590 seconds (  0.16 hours)
Thank you for using IC Compiler II.
```

```
Visiting block i2c_master_top:temp_clock_ends.design
Design 'i2c_master_top' was successfully linked.
****************************************
Report : Ignored Layers
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Sat Apr 20 01:52:19 2024
****************************************
Layer Attribute                 Value
-------------------------------------------------------------------------------
Min Routing Layer               M1
Max Routing Layer               M9
RC Estimation Ignored Layers    PO MRDL
```

```
DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      6
        Less than minimum area : 6

[Iter 0] Elapsed real time: 0:00:03
[Iter 0] Elapsed cpu  time: sys=0:00:00 usr=0:00:03 total=0:00:03
[Iter 0] Stage (MB): Used   37  Alloctr   37  Proc   91
[Iter 0] Total (MB): Used   62  Alloctr   63  Proc 2577

End DR iteration 0 with 100 parts

Start DR iteration 1: non-uniform partition
Routed  1/9 Partitions, Violations =    5
Routed  2/9 Partitions, Violations =    5
Routed  3/9 Partitions, Violations =    3
Routed  4/9 Partitions, Violations =    2
Routed  5/9 Partitions, Violations =    0
Routed  6/9 Partitions, Violations =    0
Routed  7/9 Partitions, Violations =    0
Routed  8/9 Partitions, Violations =    0
Routed  9/9 Partitions, Violations =    0

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0

[Iter 1] Elapsed real time: 0:00:03
[Iter 1] Elapsed cpu  time: sys=0:00:00 usr=0:00:03 total=0:00:03
[Iter 1] Stage (MB): Used   37  Alloctr   37  Proc   91
[Iter 1] Total (MB): Used   62  Alloctr   63  Proc 2577

End DR iteration 1 with 9 parts


Switch back to normal partition bloat and recalculate DRC:

Begin full DRC check ...

Information: Using 1 threads for routing. (ZRT-444)
Checked 1/9 Partitions, Violations =    0
Checked 2/9 Partitions, Violations =    0
Checked 3/9 Partitions, Violations =    0
Checked 4/9 Partitions, Violations =    0
Checked 5/9 Partitions, Violations =    0
Checked 6/9 Partitions, Violations =    0
Checked 7/9 Partitions, Violations =    0
Checked 8/9 Partitions, Violations =    0
Checked 9/9 Partitions, Violations =    0
[DRC CHECK] Elapsed real time: 0:00:03
[DRC CHECK] Elapsed cpu  time: sys=0:00:00 usr=0:00:03 total=0:00:03
[DRC CHECK] Stage (MB): Used   37  Alloctr   37  Proc   91
[DRC CHECK] Total (MB): Used   62  Alloctr   63  Proc 2577
Finish DR since reached 0 DRC
```

```
Redundant via conversion report:
--------------------------------

  Total optimized via conversion rate =  0.00% (0 / 5201 vias)

    Layer VIA1       =  0.00% (0      / 1916    vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (1916    vias)
    Layer VIA2       =  0.00% (0      / 3082    vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (3082    vias)
    Layer VIA3       =  0.00% (0      / 193     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (193     vias)
    Layer VIA4       =  0.00% (0      / 10      vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (10      vias)

  Total double via conversion rate    =  0.00% (0 / 5201 vias)

    Layer VIA1       =  0.00% (0      / 1916    vias)
    Layer VIA2       =  0.00% (0      / 3082    vias)
    Layer VIA3       =  0.00% (0      / 193     vias)
    Layer VIA4       =  0.00% (0      / 10      vias)

  The optimized via conversion rate based on total routed via count =  0.00% (0 / 5201
vias)

    Layer VIA1       =  0.00% (0      / 1916    vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (1916    vias)
    Layer VIA2       =  0.00% (0      / 3082    vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (3082    vias)
    Layer VIA3       =  0.00% (0      / 193     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (193     vias)
    Layer VIA4       =  0.00% (0      / 10      vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (10      vias)


Total number of nets = 736
0 open nets, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = antenna checking not active
Information: Routes in non-preferred voltage areas = 0 (ZRT-559)
```

```
Route-opt initial QoR
_____________________
Scenario Mapping Table
1: func_fast
2: func_slow

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2reg_default**
5: **reg2out_default**
6: **in2out_default**
7: wb_clk_i

--------------------------------------------------------------------------------
--------------------------------------------------------------------
PATHGROUP QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS    NSV      WHV        THV    NHV
    1   1   0.0000     0.0000      0   0.0000     0.0000      0
    1   2   0.0000     0.0000      0   0.0000     0.0000      0
    1   3   0.0000     0.0000      0   0.0000     0.0000      0
    1   4   0.0000     0.0000      0   0.0000     0.0000      0
    1   5   0.0000     0.0000      0   0.0000     0.0000      0
    1   6   0.0000     0.0000      0   0.0000     0.0000      0
    1   7   0.0000     0.0000      0   0.0000     0.0000      0
    2   1   0.0000     0.0000      0   0.0000     0.0000      0
    2   2   0.0000     0.0000      0   0.0000     0.0000      0
    2   3   0.0000     0.0000      0   0.0000     0.0000      0
    2   4   0.0000     0.0000      0   0.0000     0.0000      0
    2   5   0.0000     0.0000      0   0.0000     0.0000      0
    2   6   0.0000     0.0000      0   0.0000     0.0000      0
    2   7   0.0000     0.0000      0   0.0000     0.0000      0
--------------------------------------------------------------------------------
----------------------------------------------------------------------
SCENARIO QOR
--------------------------------------------------------------------------------
----------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage
    1   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103262.922
    2   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103262.922
--------------------------------------------------------------------------------
----------------------------------------------------------------------
DESIGN QOR
--------------------------------------------------------------------------------
----------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage          Area    InstCnt
    *   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103262.922       331.67        713
--------------------------------------------------------------------------------
----------------------------------------------------------------------
```

```
Route-opt initial QoR Summary       WNS        TNS   R2RTNS    NSV      WHV        THV
   NHV  MaxTrnV  MaxCapV    Leakage          Area    InstCnt
Route-opt initial QoR Summary    0.0000     0.0000   0.0000      0   0.0000     0.0000
     0        0        0 103262.922       331.67        713
```

```
Route-opt final QoR
____________________
Scenario Mapping Table
1: func_fast
2: func_slow

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2reg_default**
5: **reg2out_default**
6: **in2out_default**
7: wb_clk_i

--------------------------------------------------------------------------------
--------------------------------------------------------------------
PATHGROUP QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS    NSV      WHV        THV    NHV
    1   1   0.0000     0.0000      0   0.0000     0.0000      0
    1   2   0.0000     0.0000      0   0.0000     0.0000      0
    1   3   0.0000     0.0000      0   0.0000     0.0000      0
    1   4   0.0000     0.0000      0   0.0000     0.0000      0
    1   5   0.0000     0.0000      0   0.0000     0.0000      0
    1   6   0.0000     0.0000      0   0.0000     0.0000      0
    1   7   0.0000     0.0000      0   0.0000     0.0000      0
    2   1   0.0000     0.0000      0   0.0000     0.0000      0
    2   2   0.0000     0.0000      0   0.0000     0.0000      0
    2   3   0.0000     0.0000      0   0.0000     0.0000      0
    2   4   0.0000     0.0000      0   0.0000     0.0000      0
    2   5   0.0000     0.0000      0   0.0000     0.0000      0
    2   6   0.0000     0.0000      0   0.0000     0.0000      0
    2   7   0.0000     0.0000      0   0.0000     0.0000      0
--------------------------------------------------------------------------------
--------------------------------------------------------------------
SCENARIO QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage
    1   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103220.945
    2   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103220.945
--------------------------------------------------------------------------------
--------------------------------------------------------------------
DESIGN QOR
--------------------------------------------------------------------------------
--------------------------------------------------------------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   Max
TranC  MaxCapV    Leakage         Area    InstCnt
    *   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0
.0000        0 103220.945       331.62        713
--------------------------------------------------------------------------------
--------------------------------------------------------------------
```

```
Route-opt final QoR Summary         WNS        TNS   R2RTNS    NSV      WHV        THV
   NHV  MaxTrnV  MaxCapV    Leakage          Area    InstCnt
Route-opt final QoR Summary      0.0000     0.0000   0.0000      0   0.0000     0.0000
     0        0        0 103220.945       331.62        713

Route-opt command complete                CPU:    29 s (  0.01 hr )  ELAPSE:   486 s (
 0.13 hr )  MEM-PEAK:   653 MB
Route-opt command statistics  CPU=5 sec (0.00 hr) ELAPSED=6 sec (0.00 hr) MEM-PEAK=0.63
8 GB
```

```
************************************************
Report          : create_qor_snapshot (route)
Design          : i2c_master_top
Version         : R-2020.09-SP3
Date            : Sat Apr 20 01:58:19 2024
Time unit       : 1.00ns
Resistance unit : 1.00MOhm
Capacitance unit: 1.00fF
Voltage unit    : 1.00V
Current unit    : 1.00uA
Power unit      : 1.00pW
Location        : /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_rel
ease/lab2_pnr/work/./
************************************************
No. of scenario = 2
s1 = func_fast
s2 = func_slow
---------------------------------------------------------------------------
WNS of each timing group:                    s1       s2
---------------------------------------------------------------------------
wb_clk_i                                 1.3403    1.3200
---------------------------------------------------------------------------
Setup WNS:                               1.3403    1.3200      1.3200
Setup TNS:                               0.0000    0.0000      0.0000
Number of setup violations:                   0         0           0
Hold WNS:                                0.0277    0.0294      0.0277
Hold TNS:                                0.0000    0.0000      0.0000
Number of hold violations:                    0         0           0
Number of max trans violations:               0         0           0
Number of max cap violations:                 0         0           0
Number of min pulse width violations:         0         0           0
---------------------------------------------------------------------------
Area:                                                           331.624
Cell count:                                                         713
Buf/inv cell count:                                                 150
Std cell utilization:                                            0.2045
CPU(s):                                                             33
Mem(Mb):                                                           653
Host name:                                                        ws27
```

```
------------------------------------------------------------------------
Histogram:              s1    s2
------------------------------------------------------------------------
Max violations:          0     0
   above ~ -0.7   ---    0     0
    -0.6 ~ -0.7   ---    0     0
    -0.5 ~ -0.6   ---    0     0
    -0.4 ~ -0.5   ---    0     0
    -0.3 ~ -0.4   ---    0     0
    -0.2 ~ -0.3   ---    0     0
    -0.1 ~ -0.2   ---    0     0
       0 ~ -0.1   ---    0     0
------------------------------------------------------------------------
Min violations:          0     0
  -0.06 ~ above   ---    0     0
  -0.05 ~ -0.06   ---    0     0
  -0.04 ~ -0.05   ---    0     0
  -0.03 ~ -0.04   ---    0     0
  -0.02 ~ -0.03   ---    0     0
  -0.01 ~ -0.02   ---    0     0
      0 ~ -0.01   ---    0     0
------------------------------------------------------------------------
Snapshot (route) is created and stored under "/home/course/ee525202/lab_snps_flow/lab_f
ormal_release/lab_formal_release/lab2_pnr/work/./" directory
Warning: Layer M8 does not have a preferred direction, skipped.
Warning: Layer M9 does not have a preferred direction, skipped.
Warning: Layer MRDL does not have a preferred direction, skipped.
****************************************
Report : congestion
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Sat Apr 20 01:58:19 2024
****************************************

Layer     |    overflow     |              # GRCs has
Name      |  total  |  max  | overflow (%)      | max overflow
------------------------------------------------------------
Both Dirs |      53 |     4 |      24  ( 0.12%) |       4
H routing |      53 |     4 |      24  ( 0.24%) |       4
V routing |       0 |     0 |       0  ( 0.00%) |       0

Information: The command 'save_block' cleared the undo history. (UNDO-016)
Information: Overwriting block 'i2c_master_top_6_complete.design' in library 'i2c_maste
r_top'. (DES-025)
Saving library 'i2c_master_top'
```

```
****************************************
Report : Data Mismatches
Version: R-2020.09-SP3
Date   : Sat Apr 20 01:58:20 2024
****************************************
No mismatches exist on the design.
----------------------------------------
Number of Written DEF Constructs
----------------------------------------
VERSION                       : 1
DIVIDERCHAR                   : 1
BUSBITCHARS                   : 1
DESIGN                        : 1
UNITS                         : 1
PROPERTYDEFINITIONS           : 1
DIEAREA                       : 1
ROW                           : 67
TRACKS                        : 20
VIAS                          : 4
NONDEFAULTRULES               : 1
COMPONENTS                    : 713
PINS                          : 35
PINPROPERTIES                 : 35
SPECIALNETS                   : 7
NETS                          : 734
Information: The command 'write_parasitics' cleared the undo history. (UNDO-016)
Information: Design temp_clock_ends has 736 nets, 0 global routed, 734 detail routed. (
NEX-024)
```

Lab StarRC

Results

```
Extracted 31935 capacitors, 30178 resistors, 29582 nodes
Reduced to 1283 nodes,  (95.6629%)
Reduced to 549 resistors,  (98.1808%)
Reduced to 7618 capacitors: 6335 Cc and 1283 Cg (76.1453%)
  Warnings: 102    Errors: 0    (See file summary/xtract.sum)
  xTract        Elp=00:00:04 Cpu=00:00:01 Usr=1.3    Sys=0.2    Mem=522.9
Done

xTract Post Process DB:  Sat Apr 20 20:32:12 2024
  Warnings: 0    Errors: 0
  xTractPP      Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=338.8
Done

Report Violations:  Sat Apr 20 20:32:14 2024
WARNING: Found vias with one or no connection (see file vias.sum) (SX-0959)
WARNING: Found shorted nets (see file shorts_all.sum). The capacitances of these nets m
ay be
         unreliable due to the shorts. (SX-0955)
WARNING: Found vias with one or no connection (see file vias.sum) (SX-0959)
  Warnings: 3    Errors: 0    (See file summary/report_violations.sum)
  ReportViolations Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.2
Done

Report Opens:  Sat Apr 20 20:32:17 2024
  Warnings: 0    Errors: 0
  ReportOpens   Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.1
Done

GPD Post Process:  Sat Apr 20 20:32:20 2024
  Warnings: 0    Errors: 0
  GPD_PostProcess Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.5
Done

GPD Converter Part 1:  Sat Apr 20 20:32:23 2024
  Warnings: 0    Errors: 0
  GPD_Converter1 Elp=00:00:00 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=334.0
Done

GPD Converter Part 2:  Sat Apr 20 20:32:27 2024
  Warnings: 0    Errors: 0
  GPD_Converter2 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.6
Done

GPD Converter Merge Corner 1:  Sat Apr 20 20:32:29 2024
  Warnings: 0    Errors: 0
  GPD_Converter_merge_c1 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.5
Done

GPD Converter Merge Corner 2:  Sat Apr 20 20:32:32 2024
  Warnings: 0    Errors: 0
  GPD_Converter_merge_c2 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.5
Done
```

```
GPD Converter Merge Corner 2:  Sat Apr 20 20:32:32 2024
  Warnings: 0    Errors: 0
  GPD_Converter_merge_c2 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.5
Done

Setup                 Elp=00:00:35 Cpu=00:00:01 Usr=1.6    Sys=0.0    Mem=545.9
Layers                Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=545.9
HN                    Elp=00:00:00 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=551.8
Cells                 Elp=00:00:01 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=554.5
Translate             Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=546.1
NetlistSetup          Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.2
GPD_XtractSetup       Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=546.0
GPD_NameMap           Elp=00:00:01 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.5
xTract                Elp=00:00:04 Cpu=00:00:01 Usr=1.3    Sys=0.2    Mem=522.9
xTractPP              Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=338.8
ReportViolations      Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.2
ReportOpens           Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.1
GPD_PostProcess       Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=480.5
GPD_Converter1        Elp=00:00:00 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=334.0
GPD_Converter2        Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.6
GPD_Converter_merge_c1 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.5
GPD_Converter_merge_c2 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.5

Done          Elp=00:00:41 Cpu=00:00:03 Usr=3.2    Sys=0.2    Mem=554.5
date >  run_StarRC_cmd
date >  all
```

Lab PrimeTime

Results

```
#########################################################################
#    Fix ECO Power Cell Downsize Section                                #
#########################################################################
fix_eco_power -pba_mode none -verbose
Information: Checked out license 'PrimeTime-ADV' (PT-019)
Information: Starting down-sizing at [ Mon Apr 22 08:03:39 2024 ]...

Information: Use current library for down-sizing.
Information: 0 setup violating endpoints located.
Initial cell usage:
Cell Group            Count                    Area
-----------------------------------------------------------
Combinational           560 ( 79%)          166.99 ( 50%)
Sequential              153 ( 21%)          164.64 ( 50%)
Clock                     0 (  0%)            0.00 (  0%)
Others                    0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                   713 (100%)          331.62 (100%)
```

```
Final cell usage:
Cell Group            Count                    Area
-----------------------------------------------------------
Combinational           560 ( 79%)          164.24 ( 50%)
Sequential              153 ( 21%)          164.55 ( 50%)
Clock                     0 (  0%)            0.00 (  0%)
Others                    0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                   713 (100%)          328.78 (100%)

Final ECO Summary:
-----------------------------------------------------------
Number of size_cell commands                          304
Initial total cell area                            331.62
Final total cell area                              328.78
Total cell area decreased                            2.84
Percentage of total cell area decreased              0.9%
Percentage of datapath cell area decreased           0.9%

Information: Elapsed time [              42 seconds ]
Information: Completed at [ Mon Apr 22 08:03:41 2024 ]
```

```
1
#########################################################################
#    Save PT Session                                                    #
#########################################################################
save_session ./pt_workspace/slow/$PT_SESSION_DIR
Saving environmental constraints.....
Saving netlist information.....
Saving miscellaneous application information.....
Saving timing information.....
Saving variable information.....
Information: At least 4 MB of free disk space in pt_tmp_dir will be required to restore
 this session.  (SR-044)
```

```
Suppressed Messages Summary:
Id          Severity      Occurrences   Suppressed
-------------------------------------------------------------------------------
SDF-036     Warning               293          193
LNK-041     Information            33           33
Total 2 types of messages are suppressed

Timing updates: 5 (4 implicit, 1 explicit) (3 incremental, 2 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 2952.68 MB
CPU usage for this session: 9 seconds
Elapsed time for this session: 191 seconds
Diagnostics summary: 101 warnings, 378 informationals

Thank you for using pt_shell!
date >  run_pt
date >  all
```

Lab4 Chip Finishing

Results

```
DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0

[Iter 2] Elapsed real time: 0:00:20
[Iter 2] Elapsed cpu  time: sys=0:00:00 usr=0:00:20 total=0:00:20
[Iter 2] Stage (MB): Used   67  Alloctr   67  Proc  205
[Iter 2] Total (MB): Used   93  Alloctr   94  Proc 2637

End DR iteration 2 with 1 parts

Finish DR since reached 0 DRC

[DR] Elapsed real time: 0:00:20
[DR] Elapsed cpu  time: sys=0:00:00 usr=0:00:20 total=0:00:20
[DR] Stage (MB): Used   30  Alloctr   30  Proc  205
[DR] Total (MB): Used   56  Alloctr   57  Proc 2637

Redundant via insertion finished with 0 open nets, of which 0 are frozen

Redundant via insertion finished with 0 violations

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0



Total Wire Length =                    7081 micron
Total Number of Contacts =             4946
Total Number of Wires =                5853
Total Number of PtConns =              593
Total Number of Routed Wires =       5853
Total Routed Wire Length =           6661 micron
Total Number of Routed Contacts =       4946
        Layer                   M1 :         14 micron
        Layer                   M2 :       2897 micron
        Layer                   M3 :       3761 micron
        Layer                   M4 :        368 micron
        Layer                   M5 :         42 micron
        Layer                   M6 :          0 micron
        Layer                   M7 :          0 micron
        Layer                   M8 :          0 micron
        Layer                   M9 :          0 micron
        Layer                 MRDL :          0 micron
        Via            VIA45SQ_1x2 :          9
        Via            VIA45SQ_2x1 :          1
        Via         VIA34SQ_C(rot) :          4
        Via     VIA34SQ_C(rot)_1x2 :        211
        Via     VIA34SQ_C(rot)_2x1 :          5
        Via            VIA34SQ_1x2 :          4
        Via            VIA34SQ_2x1 :          2
        Via              VIA23SQ_C :        473
        Via     VIA23SQ_C(rot)_1x2 :         16
        Via     VIA23SQ_C(rot)_2x1 :          4
        Via          VIA23SQ_C_1x2 :        121
        Via          VIA23SQ_C_2x1 :       1069
        Via        VIA23BAR1_C_1x2 :         92
        Via        VIA23BAR1_C_2x1 :         13
```

```
****************************************
Report : check_mv_design
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Mon Apr 22 11:09:38 2024
****************************************

---------- Power domain rule ----------
No errors or warnings.

---------- Supply set rule ----------
No errors or warnings.

---------- Supply net rule ----------
No errors or warnings.

---------- Supply port rule ----------
No errors or warnings.

---------- Isolation strategy rule ----------
No errors or warnings.

---------- Level shifter strategy rule ----------
No errors or warnings.

---------- Retention strategy rule ----------
No errors or warnings.

---------- Power switch strategy rule ----------
No errors or warnings.

---------- Repeater rule ----------
No errors or warnings.

---------- Terminal boundary rule ----------
No errors or warnings.

---------- Isolation cell rule ----------
No errors or warnings.

---------- Level shifter cell rule ----------
No errors or warnings.

---------- Retention cell rule ----------
No errors or warnings.

---------- Switch cell rule ----------
No errors or warnings.

---------- PGMUX rule ----------
No errors or warnings.
```

```
---------- Switch cell rule ----------
No errors or warnings.

---------- PGMUX rule ----------
No errors or warnings.

---------- Diode cell rule ----------
No errors or warnings.

---------- Model rule ----------
No errors or warnings.

---------- Isolation rule ----------
No errors or warnings.

---------- Voltage shifting rule ----------
No errors or warnings.

---------- Tie-off connection rule ----------
No errors or warnings.

---------- Analog net rule ----------
No errors or warnings.

---------- Physical block pin rule ----------
No errors or warnings.

---------- PG pin rule ----------
No errors or warnings.

---------- Signal pin rule ----------
No errors or warnings.

---------- Summary ----------
Information: Total 0 error(s) and 0 warning(s) from check_mv_design. (MV-082)
1
```

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
        -input_pins
        -crosstalk_delta
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Mon Apr 22 11:09:39 2024
****************************************

  Startpoint: byte_controller/bit_controller/cnt_reg[6] (rising edge-triggered flip-flo
p clocked by wb_clk_i)
  Endpoint: byte_controller/bit_controller/cnt_reg[0] (rising edge-triggered flip-flop
clocked by wb_clk_i)
  Mode: func
  Corner: slow
  Scenario: func_slow
  Path Group: wb_clk_i
  Path Type: max

  Point                                             Delta     Incr      Path
  ---------------------------------------------------------------------------
  clock wb_clk_i (rise edge)                                  0.00      0.00
  clock network delay (ideal)                                 0.00      0.00

  byte_controller/bit_controller/cnt_reg[6]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)
                                                              0.00      0.00 r
  byte_controller/bit_controller/cnt_reg[6]/Q (SAEDRVT14_FDPRBQ_V2LP_0P5)
                                                              0.07      0.07 f
  byte_controller/bit_controller/U98/A (SAEDRVT14_INV_S_0P5)
                                                              0.00      0.07 f
  byte_controller/bit_controller/U98/X (SAEDRVT14_INV_S_0P5)
                                                              0.02      0.08 r
  byte_controller/bit_controller/U15/A4 (SAEDRVT14_AN4_0P5)
                                                              0.00      0.08 r
  byte_controller/bit_controller/U15/X (SAEDRVT14_AN4_0P5)
                                                              0.02      0.11 r
  byte_controller/bit_controller/U57/A1 (SAEDRVT14_AN4_0P5)
                                                              0.00      0.11 r
  byte_controller/bit_controller/U57/X (SAEDRVT14_AN4_0P5)
                                                              0.02      0.13 r
  byte_controller/bit_controller/U55/A2 (SAEDRVT14_OR4_1)
                                                              0.00      0.13 r
```

```
  byte_controller/bit_controller/U55/X (SAEDRVT14_OR4_1)   0.03      0.16 r
  byte_controller/bit_controller/U13/A (SAEDRVT14_INV_S_0P75)
                                                           0.00      0.16 r
  byte_controller/bit_controller/U13/X (SAEDRVT14_INV_S_0P75)
                                                           0.05      0.21 f
  byte_controller/bit_controller/U54/A2 (SAEDRVT14_ND2_ECO_1)
                                                           0.00      0.21 f
  byte_controller/bit_controller/U54/X (SAEDRVT14_ND2_ECO_1)
                                                           0.07      0.28 r
  byte_controller/bit_controller/U14/A1 (SAEDRVT14_AN2_MM_0P5)
                                                           0.00      0.28 r
  byte_controller/bit_controller/U14/X (SAEDRVT14_AN2_MM_0P5)
                                                           0.07      0.35 r
  byte_controller/bit_controller/U104/A2 (SAEDRVT14_AO221_0P5)
                                                           0.00      0.35 r
  byte_controller/bit_controller/U104/X (SAEDRVT14_AO221_0P5)
                                                           0.04      0.39 r
  byte_controller/bit_controller/cnt_reg[0]/D (SAEDRVT14_FDPRBQ_V2LP_0P5)
                                                           0.00      0.39 r
  data arrival time                                                  0.39

  clock wb_clk_i (rise edge)                               2.00      2.00
  clock network delay (ideal)                              0.00      2.00
  byte_controller/bit_controller/cnt_reg[0]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)
                                                           0.00      2.00 r
  clock uncertainty                                       -0.30      1.70
  library setup time                                       0.00      1.70
  data required time                                                 1.70
  ------------------------------------------------------------------------
  data required time                                                 1.70
  data arrival time                                                 -0.39
  ------------------------------------------------------------------------
  slack (MET)                                                        1.31
```

```
****************************************
Report : Data Mismatches
Version: R-2020.09-SP3
Date   : Mon Apr 22 11:09:39 2024
****************************************
No mismatches exist on the design.
----------------------------------------
Number of Written DEF Constructs
----------------------------------------
VERSION                     : 1
DIVIDERCHAR                 : 1
BUSBITCHARS                 : 1
DESIGN                      : 1
UNITS                       : 1
PROPERTYDEFINITIONS         : 1
DIEAREA                     : 1
ROW                         : 67
TRACKS                      : 20
VIAS                        : 27
NONDEFAULTRULES             : 1
COMPONENTS                  : 4427
PINS                        : 35
PINPROPERTIES               : 35
FILLS                       : 2
SPECIALNETS                 : 98
NETS                        : 734
```

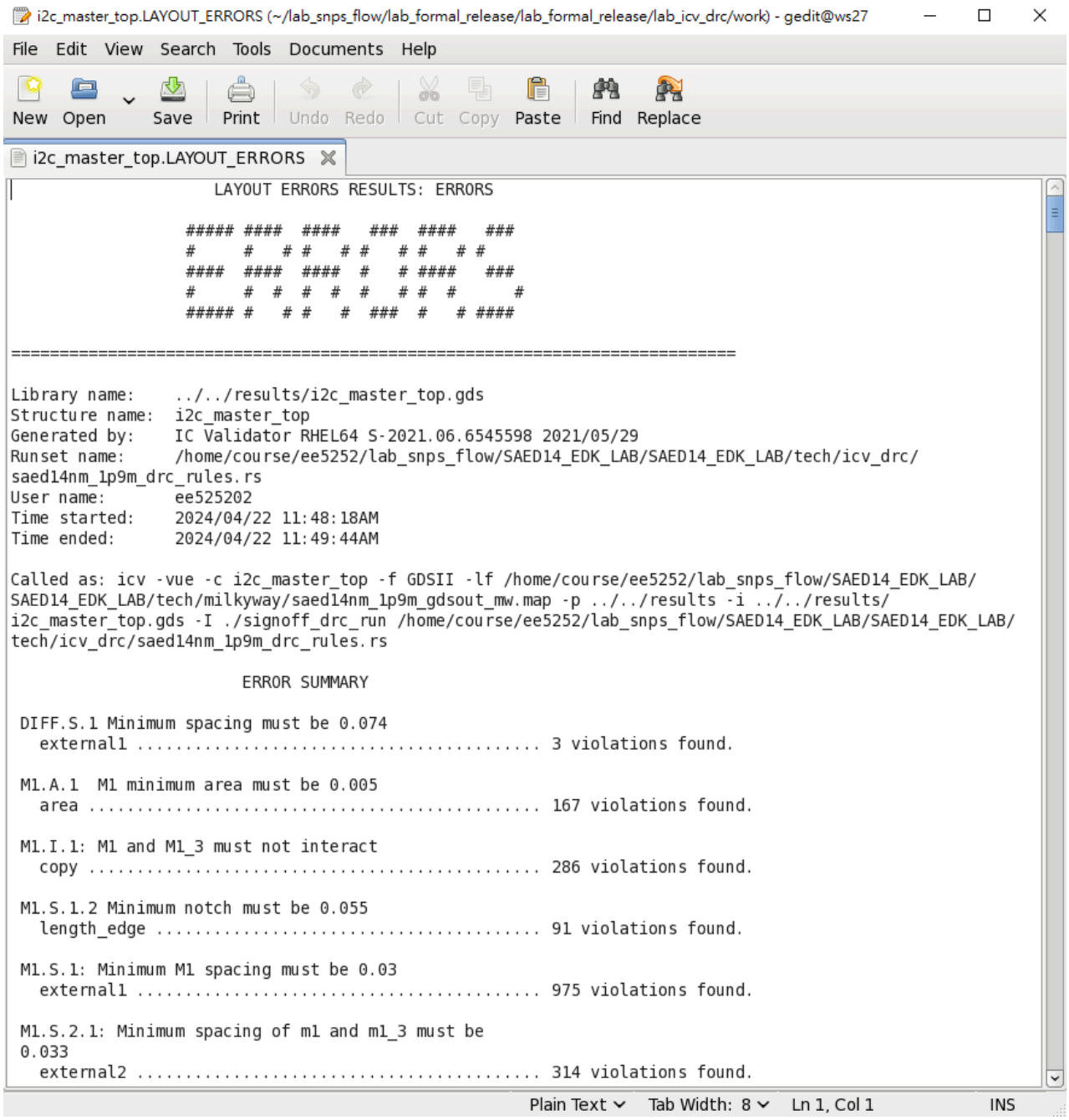
```
#############################################################################Save_Bl
ock
save_block
Information: Saving block 'i2c_master_top:temp_route_ends.design'
1
save_lib
Saving library 'i2c_master_top'
1
close_block
Information: Decrementing open_count of block 'i2c_master_top:temp_route_ends.design' t
o 1. (DES-022)
1
close_lib
Closing library 'i2c_master_top'
Information: The net parasitics of block i2c_master_top are cleared. (TIM-123)
1
exit
Maximum memory usage for this session: 519.22 MB
Maximum memory usage for this session including child processes: 2518.76 MB
CPU usage for this session:     48 seconds (  0.01 hours)
Elapsed time for this session:    715 seconds (  0.20 hours)
Thank you for using IC Compiler II.
date >  step7_finishing
date > all
```

Lab IC Validator - DRC

Results

```
Host startup begins.
Host startup done: 2 successes, 0 failures.
        ws27: 2 total cores, maximum 2 commands in parallel.
Selecting "ws27" as Primary host

System Startup Time=0:00:42 User=0.01 Sys=0.06 Mem=1.054 GB


Command execution begins.  Details recorded in the summary and log files:
    /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_icv_d
rc/work/run_details/i2c_master_top.sum
    /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_release/lab_icv_d
rc/work/run_details/saed14nm_1p9m_drc_rules.dp.log

Running ...
  ICV_Engine run is   1% complete.    Elapsed Time=0:01:31
  ICV_Engine run is   2% complete.    Elapsed Time=0:01:50
  ICV_Engine run is   3% complete.    Elapsed Time=0:01:50
  ICV_Engine run is   4% complete.    Elapsed Time=0:01:51
  ICV_Engine run is   5% complete.    Elapsed Time=0:01:51
  ICV_Engine run is  10% complete.    Elapsed Time=0:01:52
  ICV_Engine run is  15% complete.    Elapsed Time=0:01:52
  ICV_Engine run is  20% complete.    Elapsed Time=0:01:53
  ICV_Engine run is  25% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  30% complete.    Elapsed Time=0:01:55
  ICV_Engine run is  35% complete.    Elapsed Time=0:01:56
  ICV_Engine run is  40% complete.    Elapsed Time=0:01:57
  ICV_Engine run is  45% complete.    Elapsed Time=0:01:57
  ICV_Engine run is  50% complete.    Elapsed Time=0:01:59
  ICV_Engine run is  55% complete.    Elapsed Time=0:02:00
  ICV_Engine run is  60% complete.    Elapsed Time=0:02:00
  ICV_Engine run is  65% complete.    Elapsed Time=0:02:01
  ICV_Engine run is  70% complete.    Elapsed Time=0:02:01
  ICV_Engine run is  75% complete.    Elapsed Time=0:02:02
  ICV_Engine run is  80% complete.    Elapsed Time=0:02:04
  ICV_Engine run is  85% complete.    Elapsed Time=0:02:04
  ICV_Engine run is  90% complete.    Elapsed Time=0:02:05
  ICV_Engine run is  95% complete.    Elapsed Time=0:02:06
  ICV_Engine run is 100% complete.    Elapsed Time=0:02:08

Completing error storage...
  Overall error storage time: User=1.74 Sys=0.18 Mem=0.025 GB

Generating i2c_master_top.LAYOUT_ERRORS...
  Generation Time=0:00:02  User=1.25 Sys=0.10 Mem=0.001 GB

   Check Time=0:00:02  User=0.01 Sys=0.00 Mem=0.004 GB

IC Validator Run: Time=0:02:22
```

```
-------------

IC Validator Machine Memory Report
ws27         : Average = 1.410 GB, Peak = 2.398 GB

Overall Disk Usage Disk=0.006 GB
Network Disk Usage Peak=0.006 GB (no group)
Group File Disk Usage Peak=0.000 GB
Overall engine Time=0:02:22 Highest command Mem=0.101 GB

Overall Master Mem=3.505 GB
IC Validator is done.
date >  run_icv_DRC
date >  all
```



Lab IC Validator – LVS

Results

```
Processing Duplicate Cells
WARNING: Multiple cells with the same name are found in input netlist, see file "dupCel
l.log" for the details.
Processing Hierarchy ...
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'A1' not declared for cell 'SA
EDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'A2' not declared for cell 'SA
EDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'A3' not declared for cell 'SA
EDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'B1' not declared for cell 'SA
EDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'B2' not declared for cell 'SA
EDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'B3' not declared for cell 'SA
EDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'X' not declared for cell 'SAE
DRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'VDD' not declared for cell 'S
AEDRVT14_AO33_1'.
GNFwarning: i2c_master_top/U15=SAEDRVT14_AO33_1 --> Port 'VSS' not declared for cell 'S
AEDRVT14_AO33_1'.
GNFwarning: Dummy pin 'icv_floatnet_1' connected to the port 'vdd' of cell 'SAEDRVT14_A
O33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_2' connected to the port 'vss' of cell 'SAEDRVT14_A
O33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_3' connected to the port 'vbp' of cell 'SAEDRVT14_A
O33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_4' connected to the port 'vbn' of cell 'SAEDRVT14_A
O33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_5' connected to the port 'x' of cell 'SAEDRVT14_AO3
3_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_6' connected to the port 'a1' of cell 'SAEDRVT14_AO
33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_7' connected to the port 'a2' of cell 'SAEDRVT14_AO
33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_8' connected to the port 'a3' of cell 'SAEDRVT14_AO
33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_9' connected to the port 'b1' of cell 'SAEDRVT14_AO
33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_10' connected to the port 'b2' of cell 'SAEDRVT14_A
O33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_11' connected to the port 'b3' of cell 'SAEDRVT14_A
O33_1' is inserted on instance 'U15' of cell 'i2c_master_top'.
GNFwarning: Dummy pin 'icv_floatnet_12' connected to the port 'VBP' of cell 'SAEDRVT14_
AO21B_0P5' is inserted on instance 'U66' of cell 'i2c_master_top'.
```

```
Running ...
  ICV_Engine run is   1% complete.    Elapsed Time=0:01:23
  ICV_Engine run is   2% complete.    Elapsed Time=0:01:32
  ICV_Engine run is   3% complete.    Elapsed Time=0:01:32
  ICV_Engine run is   4% complete.    Elapsed Time=0:01:50
  ICV_Engine run is   5% complete.    Elapsed Time=0:01:50
  ICV_Engine run is  10% complete.    Elapsed Time=0:01:51
  ICV_Engine run is  15% complete.    Elapsed Time=0:01:53
  ICV_Engine run is  20% complete.    Elapsed Time=0:01:53
  ICV_Engine run is  25% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  30% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  35% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  40% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  45% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  50% complete.    Elapsed Time=0:01:54
  ICV_Engine run is  55% complete.    Elapsed Time=0:01:55
  ICV_Engine run is  60% complete.    Elapsed Time=0:01:55
  ICV_Engine run is  65% complete.    Elapsed Time=0:01:56
  ICV_Engine run is  70% complete.    Elapsed Time=0:01:57
  ICV_Engine run is  75% complete.    Elapsed Time=0:01:58
  ICV_Engine run is  80% complete.    Elapsed Time=0:01:58
  ICV_Engine run is  85% complete.    Elapsed Time=0:02:00
  ICV_Engine run is  90% complete.    Elapsed Time=0:02:02
  ICV_Engine run is  95% complete.    Elapsed Time=0:02:32
Comparing schematic and layout netlists.
LVS compare start time    : 2024-04-22 12:01:39
  ICV_Compare run is   0% complete.    Elapsed Time=0:00:41
  ICV_Compare run is   5% complete.    Elapsed Time=0:00:41
  ICV_Compare run is  10% complete.    Elapsed Time=0:00:41
  ICV_Compare run is  15% complete.    Elapsed Time=0:00:41
  ICV_Compare run is  20% complete.    Elapsed Time=0:00:41
  ICV_Compare run is  25% complete.    Elapsed Time=0:00:41
  ICV_Compare run is  30% complete.    Elapsed Time=0:00:41
  ICV_Compare run is 100% complete.    Elapsed Time=0:00:42
LVS compare end time      : 2024-04-22 12:02:21
Total runtime for LVS compare Time=0:00:42  User=1.26 Sys=0.15 Mem=0.028 GB
   Check Time=0:00:41  User=0.03 Sys=0.01 Mem=0.012 GB

  ICV_Engine run is 100% complete.    Elapsed Time=0:03:58

Completing error storage...
  Overall error storage time: User=0.01 Sys=0.01 Mem=0.001 GB

Generating i2c_master_top.LAYOUT_ERRORS...
```

```
Generating i2c_master_top.LAYOUT_ERRORS...
  Generation Time=0:00:00  User=0.00 Sys=0.00 Mem=0.001 GB

   Check Time=0:00:00  User=0.00 Sys=0.00 Mem=0.004 GB

IC Validator Run: Time=0:04:11

-------------

IC Validator Machine Memory Report
ws27         : Average = 1.607 GB, Peak = 2.464 GB

Overall Disk Usage Disk=0.030 GB
Network Disk Usage Peak=0.010 GB (no group)
Group File Disk Usage Peak=0.019 GB
Overall engine Time=0:04:11 Highest command Mem=0.352 GB

Overall Master Mem=3.534 GB
IC Validator is done.
date >  run_icv_LVS
date >  all
```

i2c_master_top.LAYOUT_ERRORS (~/lab_snps_flow/lab_formal_release/lab_formal_release/lab_icv_lvs/work) - gedit@ws27

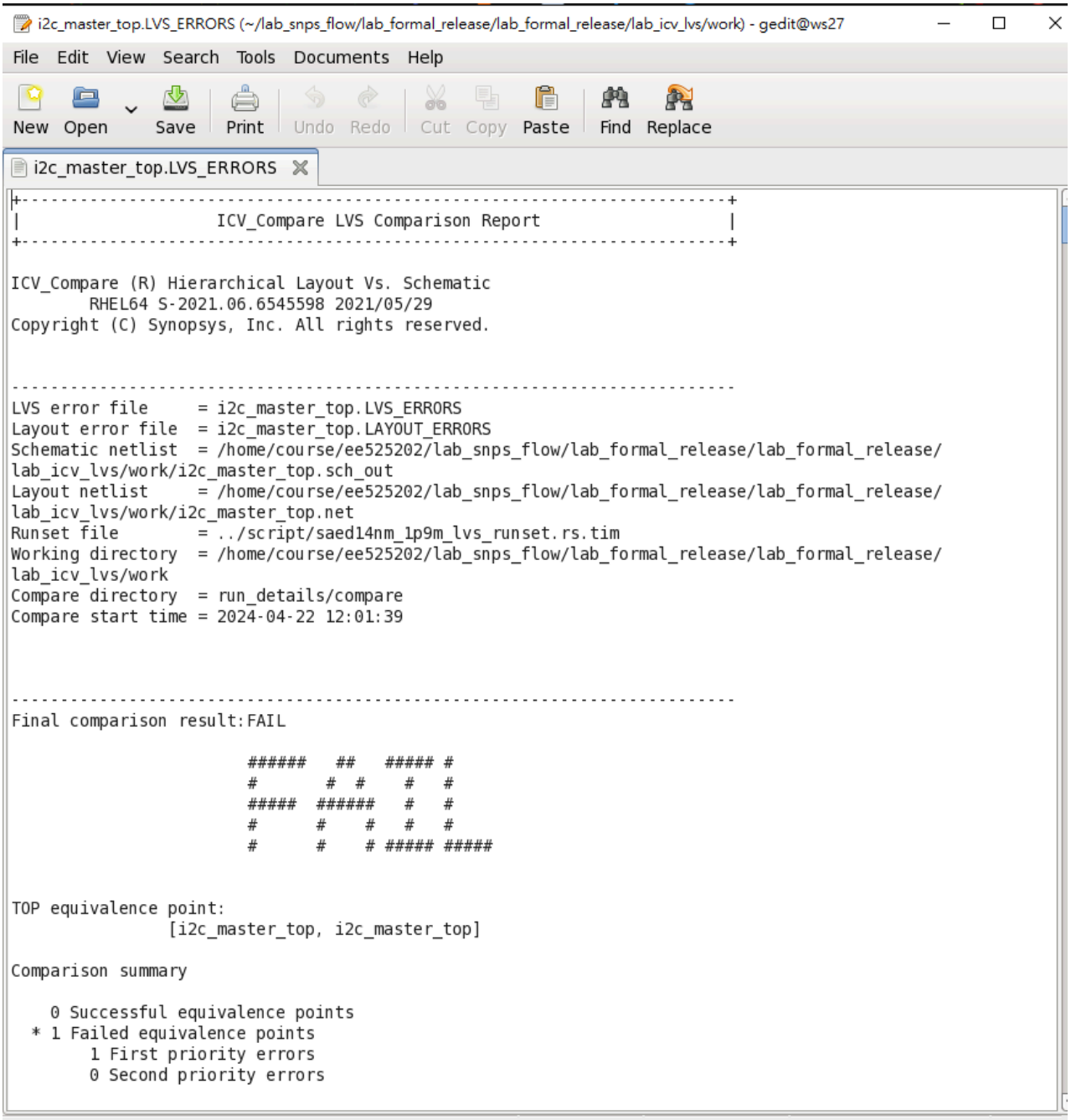
File Edit View Search Tools Documents Help

New Open Save Print Undo Redo Cut Copy Paste Find Replace

i2c_master_top.LAYOUT_ERRORS

```
                 ##### ####  ####   ###  ####   ###
                 #     #   # #   # #   # #   # #
                 ####  ####  ####  #   # ####   ###
                 #     #  #  #  #  #   # #  #      #
                 ##### #   # #   #  ###  #   # ####

================================================================================

Library name:     ../../results/i2c_master_top.gds
Structure name:   i2c_master_top
Generated by:     IC Validator RHEL64 S-2021.06.6545598 2021/05/29
Runset name:      ../script/saed14nm_1p9m_lvs_runset.rs.tim
User name:        ee525202
Time started:     2024/04/22 11:59:46AM
Time ended:       2024/04/22 12:03:04PM

Called as: icv -vue -vueshortALL -create_lvs_short_outputALL -i ../../results/i2c_master_top.gds -c
i2c_master_top -s ./netlist2spice.sp -stc i2c_master_top -sf SPICE ../script/
saed14nm_1p9m_lvs_runset.rs.tim

                        ERROR SUMMARY

 Violation
   text_net:text_short ............................... 1 violation found.




                        ERROR DETAILS


--------------------------------------------------------------------------------
Violation
--------------------------------------------------------------------------------

../script/saed14nm_1p9m_lvs_runset.rs.tim:961:text_net:text_short
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
Structure      NetId Used Text     layerNo dtype (position x, y)   TextOn       TextFrom
                      Text     layerNo dtype (position x, y)   TextOn       TextFrom
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
i2c_master_top N266   *   arst_i   40      0     (41.3760, 0.7355) m3pin_marker LAYER
                          wb_clk_i 40      0     (56.2500, 0.7355) m3pin_marker LAYER
```

Plain Text Tab Width: 8 Ln 1, Col 1 INS



Lab formality

Results

```
************ Library Checking Summary ************
Warning:  62 unlinked power cell(s) with unread pg pins.
Warning:  603 unlinked power cell(s) with no power down functions on outputs.
Warning:  2 unlinked power cell(s) with unread backup pg pins.
Warning:  238 unlinked power cell(s) with no power down function on an ff or latch.
        Use 'report_libraries -defects all' for more details.
************************************************

Top design successfully set to 'r:/WORK/i2c_master_top'
Reference design set to 'r:/WORK/i2c_master_top'
1
#implement design (the target design)
read_verilog -i /home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal_relea
se/lab_formal/work/../../results/i2c_master_top.pt.v.gz
No target library specified, default is WORK
Loading verilog file '/home/course/ee525202/lab_snps_flow/lab_formal_release/lab_formal
_release/results/i2c_master_top.pt.v.gz'
Current container set to 'i'
1
set_top i:WORK/i2c_master_top
Setting top design to 'i:/WORK/i2c_master_top'
Status:  Implementing inferred operators...

************ Library Checking Summary ************
Warning:  62 unlinked power cell(s) with unread pg pins.
Warning:  603 unlinked power cell(s) with no power down functions on outputs.
Warning:  2 unlinked power cell(s) with unread backup pg pins.
Warning:  238 unlinked power cell(s) with no power down function on an ff or latch.
        Use 'report_libraries -defects all' for more details.
************************************************

Top design successfully set to 'i:/WORK/i2c_master_top'
Implementation design set to 'i:/WORK/i2c_master_top'
1
set verification_set_undriven_signals BINARY
BINARY
set verification_check_gate_reserve_gating true
true
verify
Reference design is 'r:/WORK/i2c_master_top'
Implementation design is 'i:/WORK/i2c_master_top'
    Info:  Detected netlists in reference and implementation designs.
           Starting fast netlist verification mode.
Status:  Checking designs...
    Warning: 0 (11) undriven nets found in reference (implementation) design; see forma
lity.log for list (FM-399)
Status:  Building verification models...
Status:  Matching...
```

```
****************************************************************************************
*

Status:  Verifying...

********************************** Matching Results **********************************
*
 167 Compare points matched by name
 0 Compare points matched by signature analysis
 0 Compare points matched by topology
 19 Matched primary inputs, black-box outputs
 0(0) Unmatched reference(implementation) compare points
 0(0) Unmatched reference(implementation) primary inputs, black-box outputs
 2(0) Unmatched reference(implementation) unread points
****************************************************************************************
*


******************************** Verification Results ********************************
*
Verification SUCCEEDED
----------------------
 Reference design: r:/WORK/i2c_master_top
 Implementation design: i:/WORK/i2c_master_top
 167 Passing compare points
----------------------------------------------------------------------------------------
-
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTA
L
----------------------------------------------------------------------------------------
-
Passing (equivalent)           0       0       0       0      14     153       0     16
7
Failing (not equivalent)       0       0       0       0       0       0       0
0
****************************************************************************************
*
1
quit

Maximum memory usage for this session: 615 MB
CPU usage for this session: 3.16 seconds ( 0.00 hours )
Current time: Mon Apr 22 12:26:36 2024
Elapsed time: 107 seconds ( 0.03 hours )

Thank you for using Formality (R)!
date > run_formality_cmd
date >  all
```