A TLM-SPICE Interconnection Framework for Coupled Field and Circuit Analysis in the Time Domain

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***Abstract*—A general SPICE–transmission-line matrix (TLM) interconnection framework has been developed. The connection algorithm is based on the representation of the TLM network by equivalent Thévenin and/or Norton sources. Fundamental issues such as source equivalence and SPICE–TLM interconnection options have been examined. The framework opens new and far-reaching possibilities for hybrid global microwave and high-speed digital circuit modeling in the time domain because it combines the extensive circuit and device models of SPICE with general three-dimensional field solutions.**

***Index Terms*—Active devices and hybrid SPICE–transmission-line matrix (SPICE–TLM) connection, distributed device embedding, lumped device embedding, nonlinear devices, time-domain modeling, transmission-line matrix (TLM) method.**

I. Introduction

THE transmission-line matrix (TLM) method models field equations in terms of transmission line networks [1]. Park *et al.* [2] have investigated a number of techniques for embedding lumped and distributed devices in the TLM mesh. We have generalized these techniques based on the representation of the TLM network by equivalent Thévenin voltage and/or Norton current sources [3]. The interconnection framework allows designers to combine the extensive circuit and device modeling capability of SPICE with a field-based TLM engine in real time. Thus, it opens new avenues for hybrid analysis in high-frequency and digital circuit engineering. The new framework allows embedding of SPICE models into TLM, as well as embedding of TLM substructures into SPICE.

As mentioned in [2]–[6], lumped elements can be connected to a TLM mesh either at the nodes or at the cell boundaries. The major difference between these two approaches lies in the treatment of voltage impulses incident on the device. Node implementation places the device at the center of a TLM cell; impulses emerging from the device depend on the incident impulses and the device characteristics. On the other hand, boundary implementation places the device at the location halfway between two nodes; TLM scattering at nodes is not affected in the latter case, but the impulses emerging from the modeling boundary back into the TLM nodes depend on the device characteristics. The two approaches give identical results as long as the device is truly lumped.

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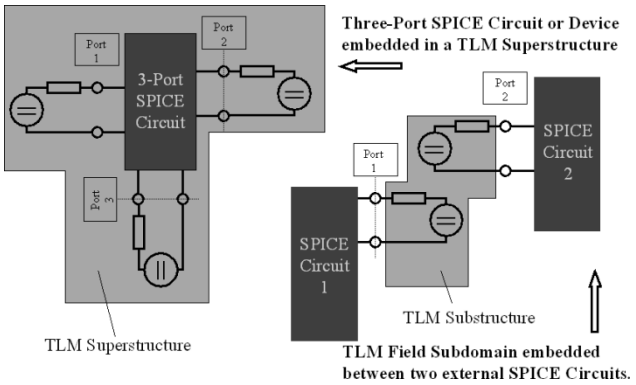


Fig. 1. Interconnection between TLM and SPICE structures.

In many practical situations, the device to be modeled may occupy a volume that is comparable to or even exceeds the size of a single TLM cell, yet its dimensions remain small compared to the spatial wavelength of interest. In other words, the device may be distributed over several TLM cells but remains quasi-lumped from a field perspective. This calls for a distributed interconnection between device and field. The interconnection framework in [3] allows for both quasi-lumped and distributed device embedding into the field space.

In this paper, we further generalize the interconnection framework so that the SPICE–TLM interface boundary can be position at three different locations. As will be shown in the following sections, by properly selecting the timing and magnitude of the impulse returned by the SPICE model to the TLM mesh, the SPICE–TLM interface can be placed either at a cell center, cell boundary, or halfway between them. Our simulation results confirmed that, when the circuit does not contain resonant structures, all three approaches give accurate results. However, when the circuit does contain resonant structures, only the last option offers a stable and lossless implementation.

II. Interconnection Framework

Fig. 1 depicts two possible scenarios of a general SPICE–TLM interconnection. In one case, the TLM structure is much larger than the SPICE circuit. In the other case, the TLM structure occupies only a small portion of a larger SPICE circuit. In both cases, the SPICE circuit may consist of lumped and distributed elements. As shown in the figure, the SPICE circuits can only be coupled to the TLM network at well-defined

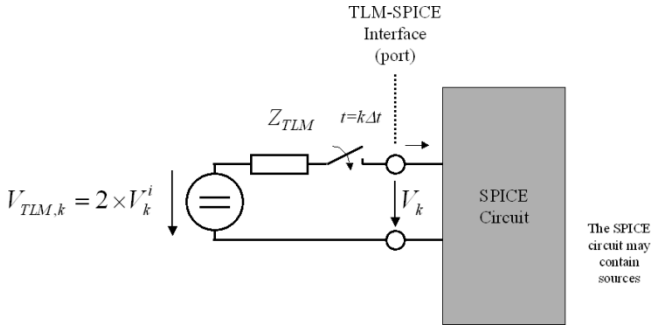


Fig. 2. SPICE circuit driven by a Thévenin equivalent source that represents the TLM structure. The switch indicates that SPICE is working in the transient analysis mode.

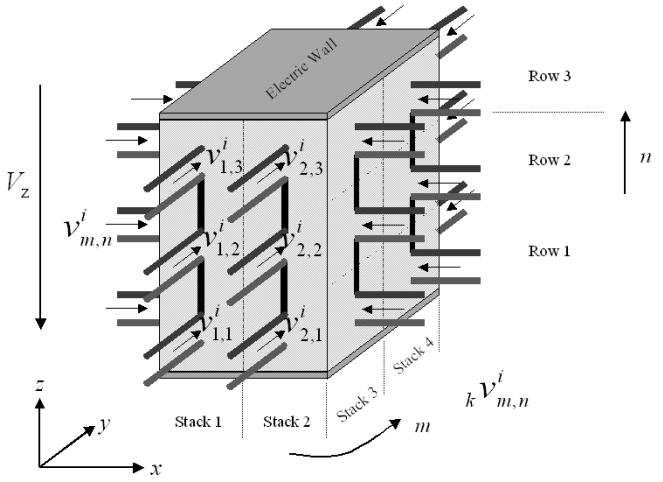


Fig. 3. Stacks of TLM cells that combine into a Thévenin equivalent voltage source.

ports. Hence, the problem of interconnecting them boils down to defining Thévenin and/or Norton equivalent sources for the TLM mesh. Since these two types of sources are equivalent, either of them can be used to drive the SPICE circuits.

As TLM and SPICE are both time-domain solvers, the internal resistance Z_{TLM} of the Thévenin source (see Fig. 2) is determined exclusively by a combination of the characteristic impedances of the link lines connected to the ports of the SPICE circuit. The instantaneous open-circuit voltage of the Thévenin source is found by combining the voltage impulses incident in these lines. At time $k\Delta t$, the open-circuited voltage of the source is

$$V_{\mathrm{TLM},k} = 2 \times V_k^i \tag{1}$$

where V_k^i is a combination of all voltage impulses incident on the link lines coupled to the device. In Fig. 3, a voltage-driven two-terminal SPICE device is represented by a cuboid volume sandwiched between two conducting surfaces. The TLM link lines polarized in the direction of the device voltage V_z form M stacks of N series-connected lines. The link lines polarized normal to V_z (not shown) are open-circuited on the device sidewalls. Assuming that all link lines have the same characteristic impedance, the total equivalent incident voltage is the average

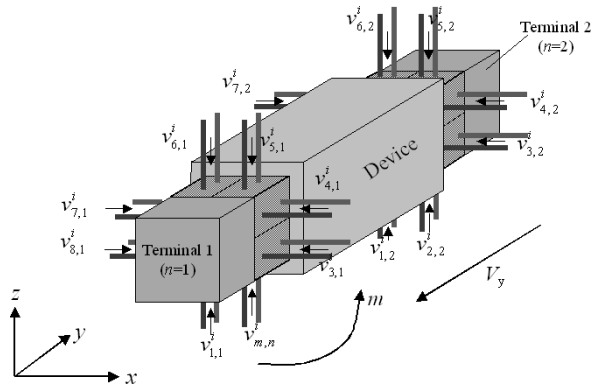


Fig. 4. Blocks of TLM cells that combine to Norton equivalent-current sources at the terminals.

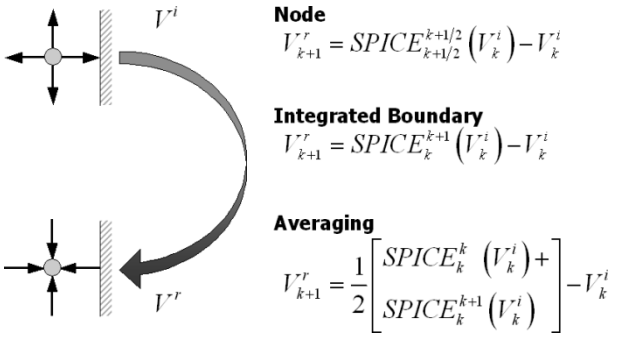


Fig. 5. Different implementations for calculating the returning impulse at the SPICE–TLM interface. $\mathrm{SPICE}_k^{k'}(V_k^i)$ denotes a SPICE-based integration process that begins at $k\Delta t$ and stops at $k'\Delta t$; the magnitude of its Thévenin voltage source is $2 \times V_k^i$.

of the M stack voltages, and the equivalent TLM impedance is the shunt combination of the stack impedances

$$V_{\mathrm{TLM},k} = 2 \times V_k^i = \frac{2}{M} \sum_m \sum_n k v_{m,n}^i \tag{2}$$

$$Z_{\mathrm{TLM}} = \frac{1}{M} \sum_m Z_{m,n}. \tag{3}$$

For a current-driven SPICE circuit, instead of finding the Thévenin voltage sources, we must obtain the Norton current sources. The procedure is a dual of the previous description. The TLM cells at the terminal interfaces constitute the loops of integration for finding the current entering and leaving the device terminals. Using the stack and row numbering convention shown in Fig. 4, the equivalent Thévenin voltage and impedance for terminal n with M pairs of link lines are

$$V_{\mathrm{TLM},k} = 2 \times V_k^i = \frac{2}{M} \sum_m k v_{m,n}^i \tag{4}$$

$$Z_{\mathrm{TLM}} = \frac{1}{M} \sum_m Z_{m,n}. \tag{5}$$

Once the equivalent source at the interface port is found, the problem of connecting the two simulation domains reduces to computing the returning impulse at the SPICE–TLM interface (Fig. 2). As shown in Fig. 5, three different scenarios are possible. The node implementation places the SPICE element at the

cell center. The incident impulse arriving at the cell boundary is allowed to travel down the link line. As soon as the impulse reaches the center, the total voltage is computed by SPICE, and a reflected voltage impulse, equal to the difference between the total voltage and the original incident voltage impulse, is reflected back into the link line. This impulse returning process can be expressed as

$$V^r_{k+1/2} = \mathrm{SPICE}^{k+1/2}_{k+1/2}\left(V^i_{k+1/2}\right) - V^i_{k+1/2}. \tag{6}$$

where $\mathrm{SPICE}^b_a(V^i_a)$ denotes a SPICE-based integration process that begins at $a\Delta t$ and stops at $b\Delta t$; the magnitude of its Thévenin voltage source is $2\times V^i_k$. Hence, $\mathrm{SPICE}^{k+1/2}_{k+1/2}\left(V^i_{k+1/2}\right)$ would be the instantaneous total voltage computed by SPICE at $(k+1/2)\Delta t$. Because the link line is nondispersive and lossless, the voltage impulse incident on the boundary at $k\Delta t$ is equal to the impulse incident on the cell center at $(k+1/2)\Delta t$, i.e., $V^i_k = V^i_{k+1/2}$. Similarly, the impulse emerging from the SPICE circuit at $(k+1/2)\Delta t$ is equal to the impulse returning to the boundary at $(k+1)\Delta t$, i.e., $V^r_{k+1} = V^r_{k+1/2}$. The above equation can be rewritten to relate the impulses V^i_k and V^r_{k+1} at two successive TLM time steps

$$V^r_{k+1} = \mathrm{SPICE}^{k+1/2}_{k+1/2}\left(V^i_k\right) - V^i_k. \tag{7}$$

This node implementation seems to be the most natural way to interconnect SPICE and TLM. However, as will be shown later, the node implementation may be unstable when resonant structures are present in the circuit.

Instead of placing the SPICE–TLM interface at the cell center, it could be placed in the cell boundary. A straightforward way to implement a boundary scheme is

$$V^r_k = \mathrm{SPICE}^k_k\left(V^i_k\right) - V^i_k. \tag{8}$$

However, this would use the instantaneous voltage computed by SPICE at $k\Delta t$. Such a choice would have the same destabilizing effect associated with the node implementation mentioned earlier; it also advances the unstable phenomena by $\Delta t/2$. The integrated boundary implementation in Fig. 5 places the SPICE–TLM interface at the cell boundary with an integration process. SPICE starts its integration process as soon as the incident impulse arrives at the boundary (at time $k\Delta t$). The total voltage at $(k+1)\Delta t$ is used to computed the voltage reflected to the TLM region

$$V^r_{k+1} = \mathrm{SPICE}^{k+1}_k\left(V^i_k\right) - V^i_k. \tag{9}$$

The integrated boundary implementation may be nonphysical because of the delayed response coupled with an integration process. The $1\Delta t$ integration interval equals the transit time of $1\Delta l$, which is the round-trip distance between the cell boundary and the cell center. Coupled with the integration process, this places the SPICE–TLM boundary effectively at the cell boundary. This will be validated in the next section. Our simulation results indicated that the integrated boundary implementation could indeed eliminate the aforementioned unstable effect. Even though it is stable, the integrated boundary implementation could be lossy if the circuit contains resonant elements.

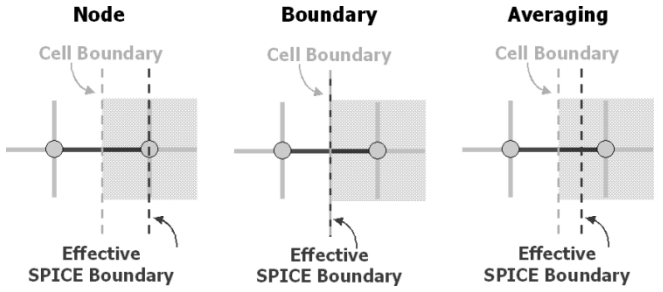


Fig. 6. Effective SPICE–TLM boundary for different impulse returning implementation. The position of cell boundary remains the same for all the cases.

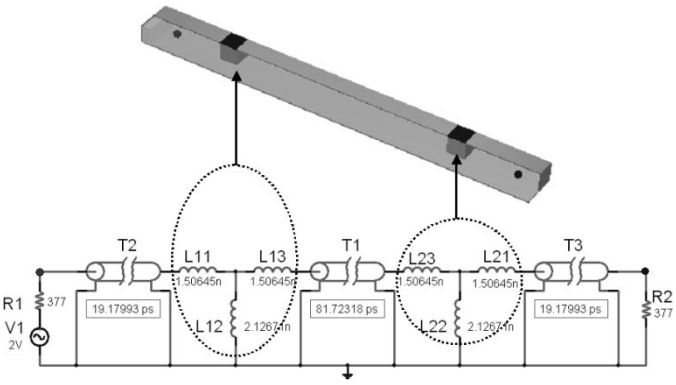


Fig. 7. Two SPICE subcircuits embedded in a parallel plate transmission line and the corresponding SPICE schematic. The spacing between the two subdomains is 24 mm. The 81.732 18 ps in transmission line T1 corresponds to a $24.5\Delta t$ delay for the averaging implementation. The inductances are: $L11 = L13 = L23 = L21 = 1.50645$ nH and $L12 = L22 = 2.12671$ nH.

The averaging implementation in Fig. 5 is a combination of the previous two approaches

$$V^r_{k+1} = \frac{1}{2}\left[\mathrm{SPICE}^k_k\left(V^i_k\right) + \mathrm{SPICE}^{k+1}_k\left(V^i_k\right)\right] - V^i_k. \tag{10}$$

Our simulation results show that the averaging approach is lossless and remains stable even in the presence of resonant structures. The effective position of the SPICE–TLM boundary is also the average of the node and the integrated boundary implementation (Fig. 6).

All three implementations give accurate results when the SPICE–TLM circuit does not contain resonant structures. We have tested these implementations with passive and active SPICE elements and found that the averaging implementation works well under all tested situations.

III. Validation

We have thoroughly tested the above interconnection framework. The first set of numerical experiments is to verify the three different SPICE–TLM interconnection schemes. Fig. 7 shows two SPICE subcircuits embedded in a parallel plate transmission line modeled by a TLM mesh. The size of each SPICE subdomain in the TLM mesh is $2\times 2\times 2$ mm^3. The spacing between the two subdomains is 24 mm. The propagation delay for 1 mm is 3.33564 ps. The delays for node, integrated boundary,

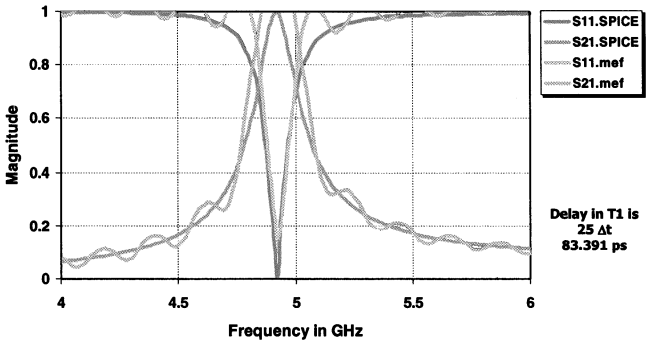


Fig. 8. Node implementation: both SPICE and SPICE–TLM yield the same center frequency, but the S-parameters of SPICE–TLM are obviously incorrect.

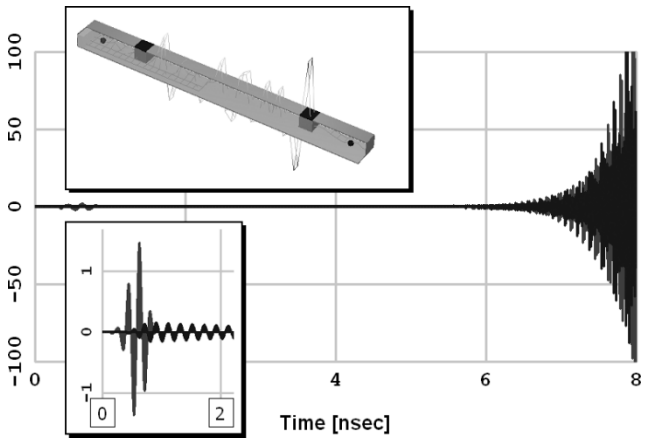


Fig. 9. Node implementation: due to the resonant nature of the topology, unstable spurious oscillation occurred after a lengthy simulation. The inserts show the voltage magnitudes at the input and output ports from 0 to 2 ps and the spurious field distribution at the oscillating stage.

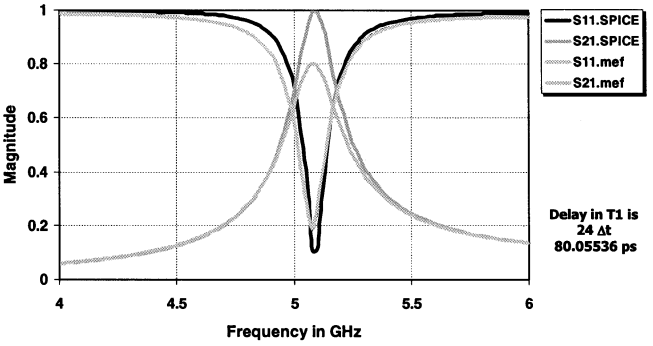
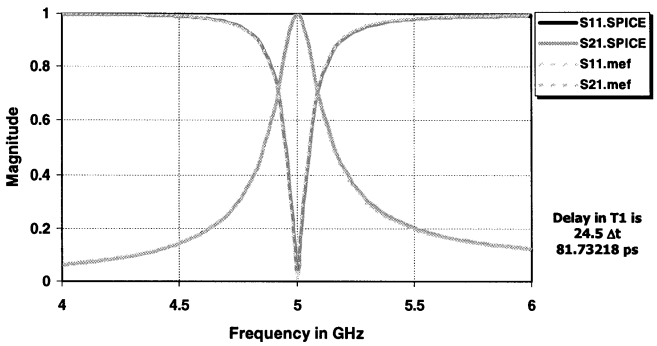


Fig. 10. Boundary implementation: both SPICE and SPICE–TLM yield the same center frequency. However, the reduction in magnitude of the S-parameters computed with SPICE–TLM indicates that the boundary implementation is lossy.

and averaging implementations are 25, 24, and 24.5 Δt, which correspond to 83.391, 80.05536, and 81.73218 ps, respectively.

Fig. 8 compares the S-parameters obtained with PSPICE and the node implementation. Both methods give similar center frequencies, but the SPICE–TLM result is obviously incorrect. This is due to an unstable spurious oscillation caused by the node implementation (Fig. 9). Fig. 10 compares the S-parameters obtained with PSPICE and the boundary implementation. The reduction in magnitude of the S-parameters computed



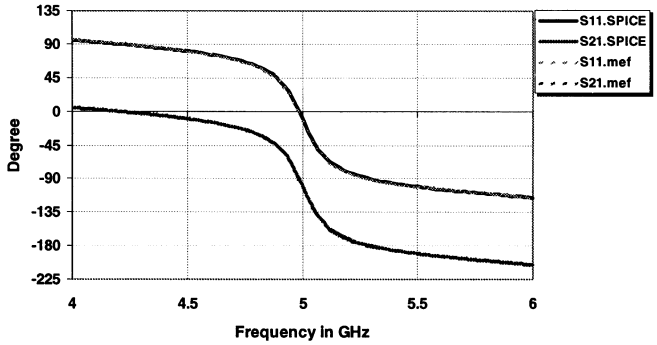


Fig. 11. Averaging implementation: the results obtained with SPICE and SPICE–TLM are in excellent agreement.

with SPICE–TLM indicates that the boundary implementation is lossy.

Fig. 11 compares the S-parameters obtained with PSPICE and the averaging implementation. Since the SPICE–TLM boundary is halfway between the cell center and the cell boundary, the length of the three transmission lines in the PSPICE schematic would be 5.75, 24.5, and 5.75 mm. The associated delays are 19.17993, 81.73218, and 19.17993 ps, respectively. Both the magnitude and phase of the S-parameters obtained with SPICE–TLM and PSPICE are in excellent agreement.

The next set of numerical experiments demonstrates the nonlinear capability of SPICE–TLM. Note that the TLM part is kept as simple as possible without loss of generality. This enables us to compare the hybrid SPICE–TLM combination to a pure SPICE representation. Fig. 12 depicts a parallel plate transmission line with a SPICE element at the center of the first transmission line. The second line is used as a reference to yield the amplitude of the incident input signal. The lines are discretized with a $3\Delta l \times 3\Delta l \times 40\Delta l$ mesh, $\Delta l = 1$ mm.

Figs. 13 and 14 depict the responses of a diode and a BJT network excited by a 2-GHz sinusoidal excitation. Fig. 15 depicts the responses of a common base BJT amplifier excited by a similar sinusoidal voltage source. In all the cases, the SPICE and SPICE–TLM results are in excellent agreement. The node, integrated boundary and averaging interconnection schemes were used to simulate the above circuits, and the results obtained with all three methods were virtually identical. Fig. 16 shows the discrepancy between these methods for the common base BJT amplifier experiment. The maximum voltage difference at the am-

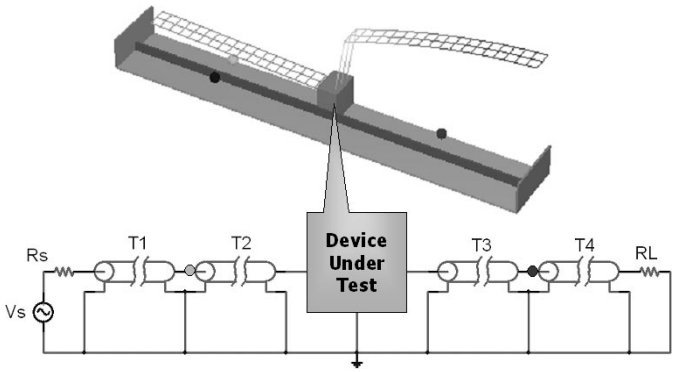


Fig. 12. Testing setup. A 377-Ω parallel plate transmission lines and its SPICE schematic. A 2-GHz sinusoidal voltage source is used to drive the structure; T2 and T3 each have a delay of 32.5 ps.

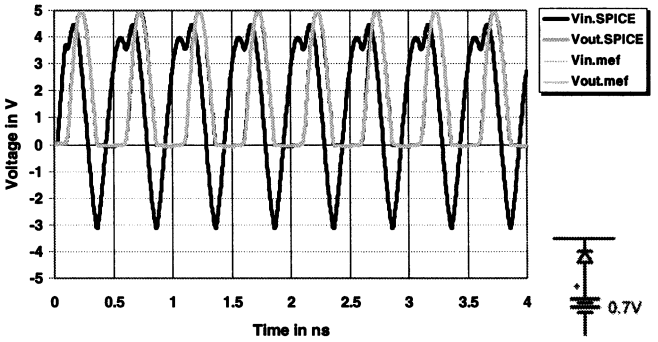


Fig. 13. Responses of a diode circuit inserted in the parallel plate structure in Fig. 12. The TLM excitation source is a 5-V 2-GHz sinusoidal signal. The SPICE and SPICE–TLM results are in excellent agreement.

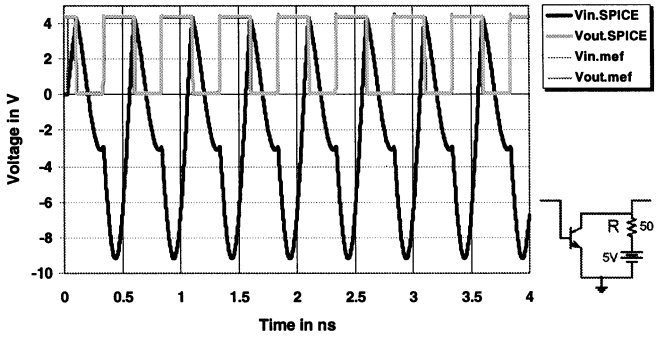


Fig. 14. Responses of a BJT circuit insert in the parallel plate structure in Fig. 12. The TLM excitation source is a 5-V 2-GHz sinusoidal signal. The SPICE and SPICE–TLM results are in excellent agreement.

plifier's terminal is less than 0.4%. The formulas for computing the voltage difference are

$$100\% \times \frac{(V_{\text{in.BI}} - V_{\text{in.AI}})}{\text{Max}\,\{V_{in.AI}\}}$$

$$100\% \times \frac{(V_{\text{in.NI}} - V_{\text{in.AI}})}{\text{Max}\,\{V_{\text{in.AI}}\}}$$

$$100\% \times \frac{(V_{\text{out.BI}} - V_{\text{out.AI}})}{\text{Max}\,\{V_{\text{out.AI}}\}}$$

and

$$100\% \times \frac{(V_{\text{out.NI}} - V_{\text{out.AI}})}{\text{Max}\,\{V_{\text{out.AI}}\}}$$

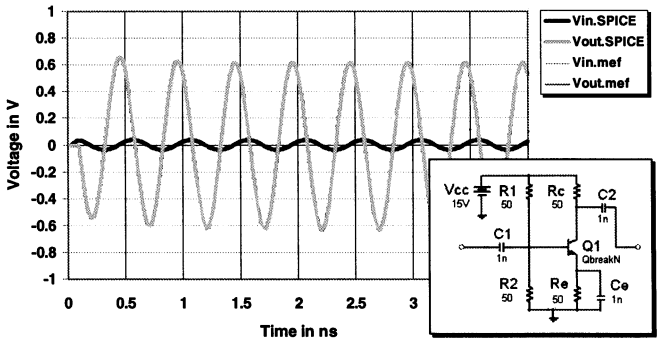


Fig. 15. Response of a common emitter amplifier insert in the parallel plate structure in Fig. 12. The circuit is driven by a 0.05-V 2-GHz sinusoidal voltage source. The node, integrated boundary and averaging interconnection schemes give virtually identical results, which are in excellent agreement with the results from PSPICE. The discrepancies between the different interconnection schemes are shown in Fig. 16.

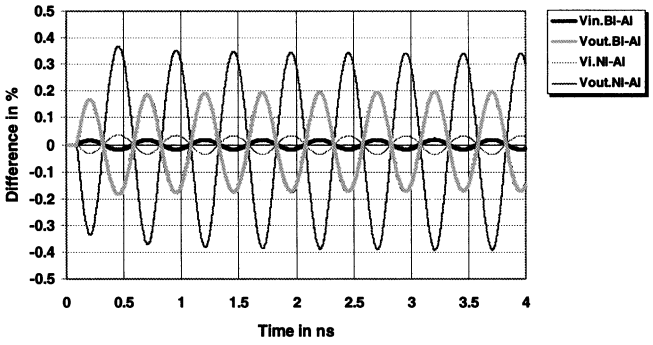


Fig. 16. Amplifier circuit in Fig. 15 has been analyzed with all three interconnection schemes; note that, in the legend, AI, BI, and NI stand for averaging, boundary, and node implementation, respectively. Using the averaging scheme as a reference, the plots show the percentage difference between the schemes.

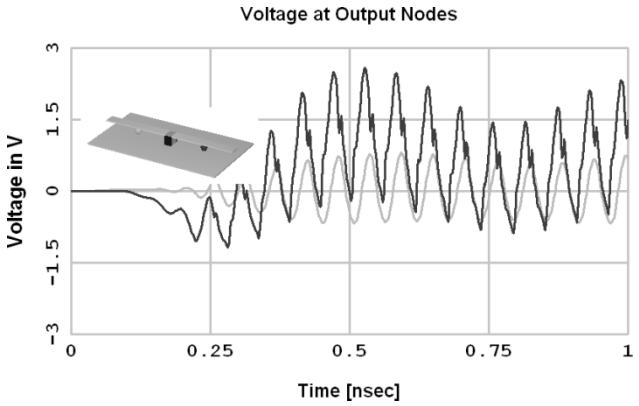


Fig. 17. Common emitter circuit in microstrip. The circuit is driven by a 0.05-V 2-GHz sinusoidal voltage source. Unlike the response in Fig. 15, this one has a very high frequency oscillation caused by the parasitic feedback in the microstrip environment.

where AI, BI, and NI stand for averaging, boundary, and node implementation, respectively.

As a final experiment, the common emitter circuit in the previous example has been placed in a microstrip environment. Due to the presence of unwanted parasitic feedback, the circuit oscillates at a high frequency, Fig. 17. The oscillation can be eliminated by placing a resistive loading circuit at the collector terminal of the SPICE sub-circuit. The field distribution and time response of the modified circuit are shown in Fig. 18.

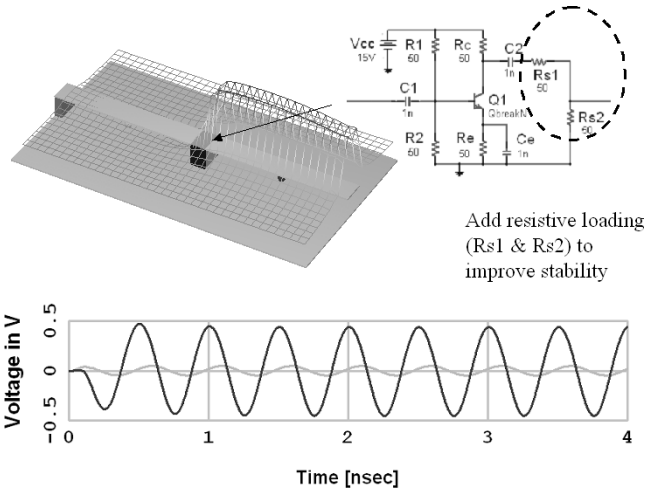


Fig. 18. Loading resistors $Rs1 = Rs2 = 50\,\Omega$ are added to the collector end to stabilize the circuit.

IV. Conclusion

A general SPICE–TLM interconnection framework with different connection implementations has been presented. The node, boundary, and averaging implementations have been used to analyze nonresonant structures, and the results are virtually identical. This indicates that all three implementations are valid as long as the circuit does not contain resonant structures. Our simulation results indicated that the averaging implementation is lossless and stable even in the presence of resonant elements. Under these circumstances, the node and integrated boundary implementation become unstable and lossy, respectively. SPICE–TLM has been applied to the analysis of microwave circuits with nonlinear elements; all the connection schemes give accurate results. This framework allows TLM and SPICE to couple field and circuit analysis in the time-domain. Such a combination has great potential for global microwave and high-speed and/or digital circuit modeling.

Acknowledgment

The SPICE–TLM interconnection framework has been implemented with MEPHISTO from the Faustus Scientific Corporation, and a public-domain version of SPICE from the University of California at Berkeley. Circuit schematics and independent SPICE results were obtained using PSPICE from Cadence Design Systems.

References

[1] P. B. Johns, "A symmetrical condensed node for the TLM method," *IEEE Trans. Microwave Theory Tech.*, vol. 35, pp. 370–377, Apr. 1987.

[2] J. W. Park, P. P. M. So, and W. J. R. Hoefer, "Lumped and distributed device embedding techniques in time domain TLM field models," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001.

[3] P. P. M. So and W. J. R. Hoefer, "A generalized framework for SPICE–TLM interconnection," presented at the IEEE MTT-S Int. Microwave Symp., Seattle, WA, June 3–7, 2002, Paper WE4E-1.

[4] P. Russer, P. P. M. So, and W. J. R. Hoefer, "Modeling of nonlinear active regions in TLM," *IEEE Microwave Guided Wave Lett.*, vol. 1, pp. 10–13, Jan. 1991.

[5] P. Russer, M. Righi, C. Eswarappa, and W. Hoefer, "Lumped element equivalent circuit parameter extraction of distributed microwave circuits via TLM simulation," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1994, pp. 887–890.

[6] L. Cascio, G. Tardioli, and W. Hoefer, "Modeling of nonlinear active and passive devices in three dimensional TLM networks," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Denver, CO, June 8–13, 1997, pp. 383–386.

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