A 2.4GHz Fully CMOS Integrated RF Transceiver for 802.11b Wireless LAN Application

Weixin Kong, Chianghua Ye*, H. C. Lin

ECE, University of Maryland, College Park, MD

* Maryland Semiconductor Inc., Clarksburg, MD

Abstract - **A fully CMOS integrated RF transceiver for 802.11b wireless LAN application is implemented and measured. The IC is fabricated in 0.25um CMOS process and packaged in TQFP package. The single chip transceiver incorporates an I/Q modulator and demodulator, an integrated IF and RF synthesizer with on-chip VCOs, an on-chip LNA, and PA pre-driver amplifier. The chip fully complies with the IEEE 802.11b WLAN standard. The transmitter achieves less than 7.5% EVM and the receiver sensitivity is –86dBm for 11Mbps mode. The chip uses 3V power supply and the current consumption is 60mA for receiver and 70mA for transmitter.**

Index terms - **CMOS, integrated circuits, RF, transceiver, wireless LAN.**

1. INTRODUCTION

Wireless local area networks (WLANs) in the 2.4GHz range [1] have experienced tremendous growth in the recent years. For high-volume portable applications, low cost and low power implementations become critical. CMOS technology could provide lower cost than Si Bipolar or SiGe HBT technologies. This paper describes design techniques for a fully CMOS integrated RF transceivers to be used in WLAN 802.11b applications. The adopted architecture and implementations of some building blocks are described. The measurement results of the IC are reported.

As discussed in [2], contrary to the conventional wisdom, for 2.4GHz WLAN applications the super-heterodyne architecture has the potential to consume less power and have lower cost than a direct conversion transceiver. The image problem can be solved using careful frequency planning and narrow band response of LNA without the troublesome image rejection filter. The dual conversion method does not need differential LNA and PA, thus eliminating the baluns and reducing the current. The IF SAW filter can be shared in receiver and transmitter path thanks to Time Division Duplex (TDD) of 802.11b. The high IF frequency makes this architecture more robust to issues such as flicker noise, DC offset and LO pulling of other low IF and direct conversion architectures [3,4]. In [2], the CMOS RF front end of an 802.11b transceiver is implemented and compared with a SiGe technology based commercial product. But the VCO is not integrated on chip and the IF-to-baseband circuits are not implemented. In this paper, we will present a single chip complete transceiver that incorporates an I/Q modulator and demodulator, an integrated IF and RF synthesizer with on-chip VCOs, an on-chip LNA, and PA pre-driver amplifier. This implementation makes it possible to make a fair comparison with other architectures.

2. TRANSCEIVER ARCHTECTURE

2.1 Receiver Path

Fig. 1 shows the block diagram of the CMOS transceiver that employs the super-heterodyne architecture. The receiver down-converts the RF signal to baseband in two steps. The IF is chosen to make the image band falls in a quiet band. Then the image can be sufficiently rejected by external band selection filter, and on chip narrow band LNA. With an IF of 374MHz and the implemented 2.4GHz LNA, the image at 1.7GHz is rejected by more than 50dB which is enough for this application. In the RX path, the LNA uses a common-source amplifier with cascode transistors to maximize reverse isolation, and inductor degeneration to achieve the real-part impedance of 50ohm. The LNA incorporates two gain settings to meet the maximum signal requirement of -10dBm. The RF mixer uses an open-drain double-balanced Gilbert cell. After down-converted to IF, the signal goes off chip and filtered by a SAW filter. The SAW filter rejects the strong adjacent channel interferences and reduced the dynamic range requirement of the following IF-to-baseband strip. A variable gain amplifier (VGA) is used in IF stage to achieve high gain and large IF bandwidth simultaneously. The IF VGA has a gain range of more than 70dB which is required by the dynamic range of 802.11b standard. A RSSI circuit is included to help the baseband chip implement closed loop automatic gain control (AGC) function. The IF mixer is a Gilbert cell multiplier with resistor degeneration. An anti-alias LPF is implemented as a 3-order bessel gm-C

filter with 7.5MHz cutoff frequency. Though the DC offset problem is not as serious as that in direct conversion, the DC offset due to LO self-mixing in IF mixer and component mismatch in differential path still degrades the receiver performance if it is not properly handled. The common way to deal with this static DC offset is using AC coupling or some digital feedback scheme. Here a simple DC correction circuit based on voltage follower structure is used. The final ADC referred DC offset is less than 10mV.

2.2 Transmitter Path

In the TX path, the modulated baseband I and Q signals are low-pass filtered before being applied to the IF mixer. In order to minimize LO leakage, the DC correction circuit is inserted between the baseband and IF mixer to remove the DC offset. In the IF stage, an VGA amplifier provides about 17dB power control range and a driver amplifier is used to drive external SAW filter. A double balanced mixer up converts the IF signal to the final 2.4GHz band. The double balanced topology is allowed here because the side band image is suppressed by the following PA and RF band pass filter. To further suppress the side band image, an on chip LC tank is used as the load of the up-conversion mixer to select the desired band. The two stages PA pre-driver is capable of driving up to 0dBm output to external PA.

2.3 RF and IF LO path

Channel selection is performed with the RF LO, and its frequency varies from 2038MHz to 2110MHz. The tank of the fully integrated RF VCO is implemented with two spiral inductors and two NMOS in n-well accumulation mode varactors. The RF PLL compares the divided VCO frequency to a 0.5MHz reference and achieves a phase noise of –115dBc/Hz at a 1MHz offset. To drive the LO ports of the up and down conversion mixer, some buffer stages are required in the RF LO path. The conventional method to get gain in this high frequency is using tuned load and will consume lots of area and current. A gain boosting amplifier based on cross coupled topology is used in this design. It achieves the desired gain without using any inductor.

The IF VCO uses two external inductors and is fixed at 748MHz by IF PLL. The IF I/Q LO signal is derived by a divide-by-two circuit. To reduce to sensitivity of the quadrature accuracy to the duty cycle of VCO signal, the VCO signal is first AC coupled and limited before applying to the D flip-flops. This results in less than 1 degree of quadrature error.

3. BUILDING BLOCKS

3.1 Pre-driver

A power amplifier (PA) pre-driver consisting of a pre-amplifier and a driver stage delivers a nominal power of 0dBm to a 50ohm load (Fig. 2). The pre-amplifier uses a cascode scheme to provide isolation from the PA output to its input, and to maintain stability. The matching to 50ohmis performed by a series capacitor and choke inductor, that also provides the DC current path to the PA output. The PA has an adjustable output power of –17dBm to 0dBm. The transmitter measured OIP3 is 16dBm, and the output 1-dB compression point is 6dBm. Hence, a worst-case power back-off of 6dB is achieved to meet the required spectrum mask. An off-chip PA further amplifies the radio output to a maximum of 18dBm.

3.2 LNA

The low-noise amplifier (LNA) is an inductively degenerated common source amplifier tuned to 2.4GHz. To tolerate the large desired inputs, the LNA gain is programmable between 17 and –13 dB and is adjusted by the baseband chip. The LNA also rejects the 1.7GHz image signal by more than 20dB.

3.3 LO Buffer

The LO buffer is based on a differential structure with cross-coupled NMOS load, Fig. 3. The positive feedback due to the cross-coupled NMOS pair boosts the gain at high frequency without using inductor. The biasing current, size of cross-coupled NMOS pair and resistors are carefully selected to center the peaked frequency at 2GHz with enough bandwidth.

3.4 DC Correction Circuit

A simple DC correction circuit based on voltage follower structure, shown in Fig 4, is used to correct the DC offset due to LO self-mixing in IF mixer and component mismatch in differential path at baseband. The DC level of the signal is pulled to the reference voltage while AC signal passes to the output directly. By inserting this block in both paths of the differential circuits, the DC level of both paths are forced to the same reference voltage and DC offset is removed. The Op-Amp used here is based on a complementary wide swing structure [5].

4. MEASUREMENT RESULTS

The transceiver is implemented in 0.25um CMOS technology with die area of 3x2.5 mm^2. The IC is packaged in a 64-pin TQFP package and tested on a FR-4 evaluation board with external matching, SAW filer, T/R switch and RF band pass filter but no antenna.

The chip fully complies with the IEEE 802.11b WLAN standard. The receiver sensitivity of –86dBm is measured at 8% Packet Error Rate (PER) in 11Mbps mode. The maximum input signal level for 8% PER is –4dBm. The sensitivity and maximum signal level exceeds the standard by 10 and 6dB respectively. The image rejection is found by inject an –30dBm image signal at 1.7GHz. The desired RF signal at –70dBm can still achieves 8% PER. Assuming a SNR ratio of 10dB, image rejection is –30-(-70-10)=50dB. One typical transmitter measurement result is given in Fig. 5. It achieves less than 7.5% EVM for a 0dBm power out. The measured power spectrum mask is shown in Fig. 6. It achieves the Adjacent Power Rejection Ratio (ACPR) of 38dBc which is higher than the standard requirements of 30dBc by 8dB.

The measured performance of the transceiver is summarized in Table 1. The performance and current consumption is comparable to the latest published 802.11b radio based on direct conversion architecture [6,7].

5. REFERENCES

[1] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: Higher-speed Physical Layer Extension in the 2.4GHz band, IEEE Std 802.11b.

[2] Xi Li, J. R. Paviol, B. A. Myers, K. K. O, "A CMOS 802.11b Wireless LAN Transceiver," *Proc. of 2003 RFIC Symposium*, pp. 41-44, June 2003.

[3] J. Crols and M. Steyaert, "Low-IF Topologies for High-Performance Analog Front Ends of Fully Integrated Receivers," *IEEE Transactions on Circuits and Systems II*, vol.45, no. 3, pp. 269-282, March 1998.

[4] B. Razavi, "Design Considerations for Direct-Conversion Receivers," *IEEE Transactions on Circuits and Systems II*, vol. 44, no. 6, pp. 428-435, June 1997.

[5] M. Steyaert and W. Sansen, "A High-Dynamic-Range CMOS Op Amp with Low Distortion Output Structure," *IEEE Journal of Solid State Circuits*, vol.22, no.6, pp. 1204-1207, December 1987.

[6] P. M. Stroet, R. Mohindra, S. Hahn, A. Schuur, E. Riou, "A Zero-IF Single-Chip Transceiver for up to 22Mb/s QPSK 802.11b Wireless LAN," *IEEE International Solid State Circuits Conference Digest of Technical Papers*, pp. 204-205, Feb. 2001.

[7] H. Darabi, et al., "A Dual Mode 802.11b/Bluetooth Radio in 0.35um CMOS," *IEEE International Solid State Circuits Conference Digest of Technical Papers*, pp.86-87, Feb. 2003.

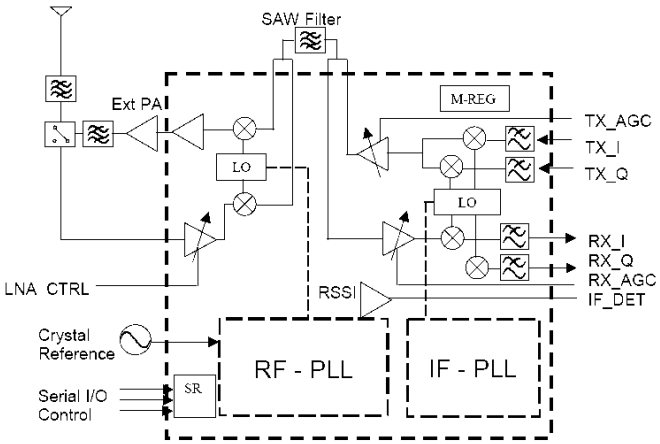

Figure 1. Transceiver Block Diagram

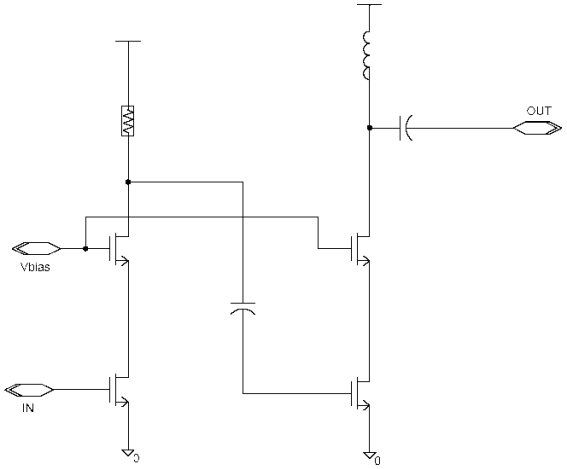

Figure 2. PA Pre-driver

Sensitivity	-86 dBm
IIP3 (High/Low gain)	-15 dBm/ +13 dBm
Tx output power	0 dBm nominal
Tx P1dB	6 dBm
Composite phase noise	2 degree RMS (10kHz-10MHz)
Rx current	60 mA
Tx current	70 mA
Die size	3x2.5 mm2
Package	64-pin TQFP

Table 1. Performance summary

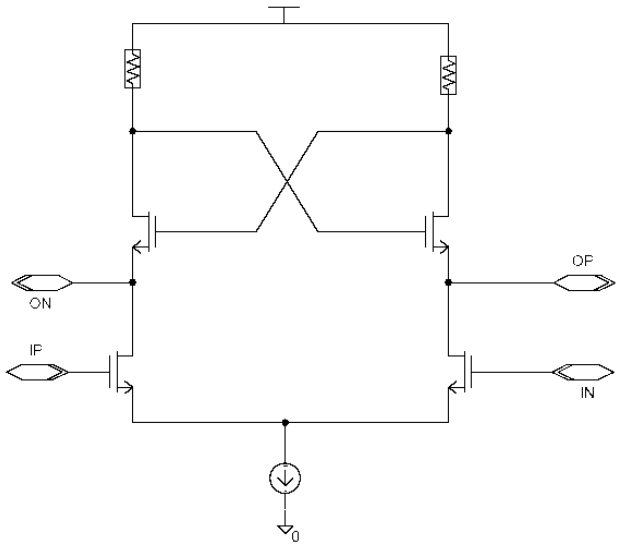

Figure 3. LO Buffer

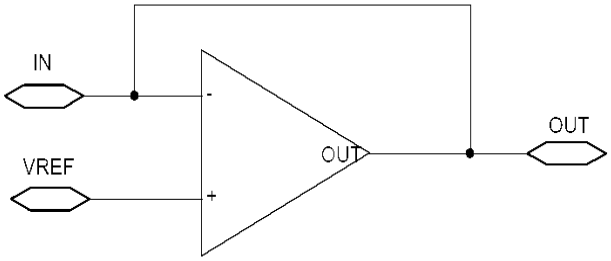

Figure 4. DC Correction Circuit

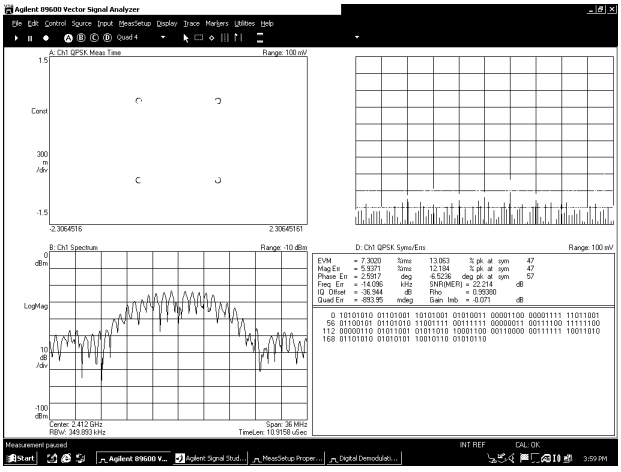

Figure 5. Measured transmitter EVM

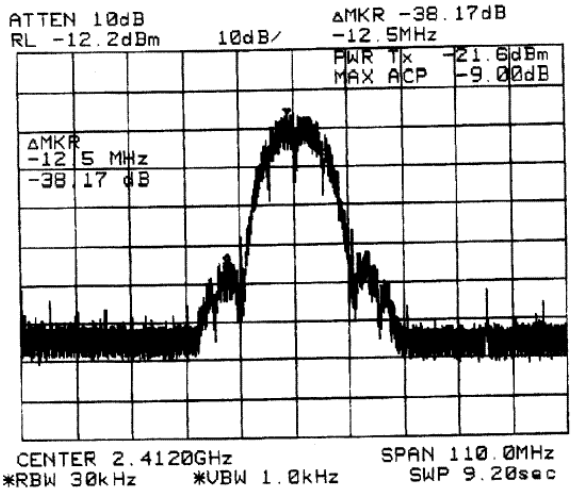

Figure 6. Measured transmitter spectrum