

# Heterostructure Field Effect Transistors

# Outline

**HEMT (HFET) principle of operation.**

**HFET material systems**

**HFET modeling**

**Gate leakage in HFETs and MESFETs**

**HFET design**

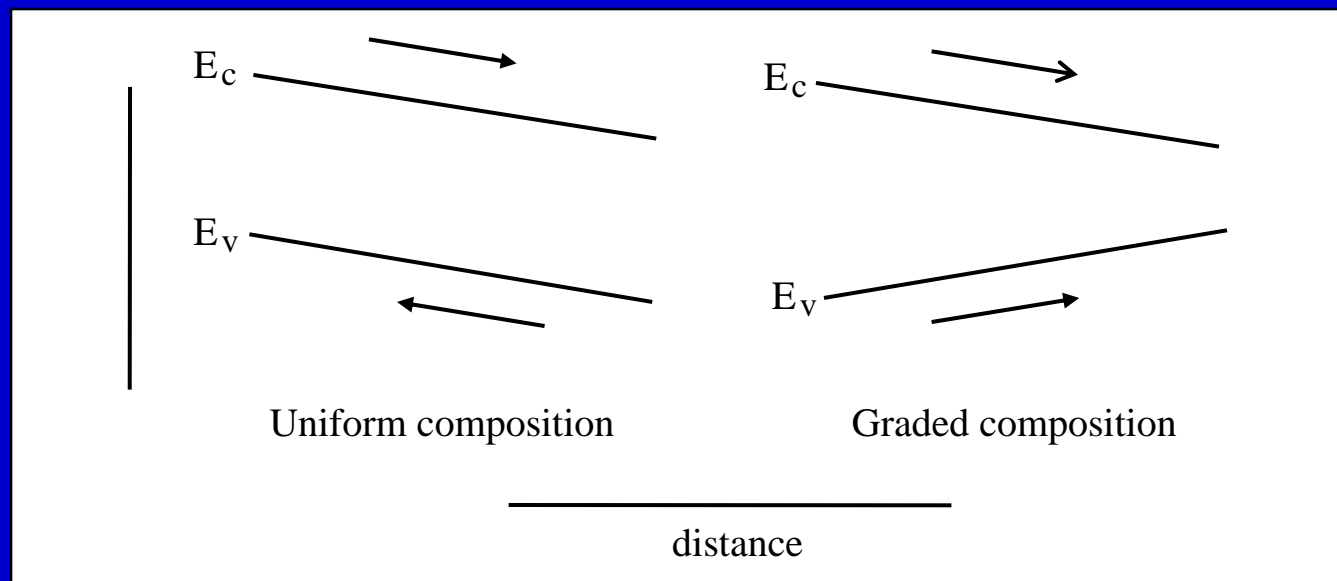
**HFET characterization.**

**Complementary HFETs**

**HFET and MESFET scaling.**

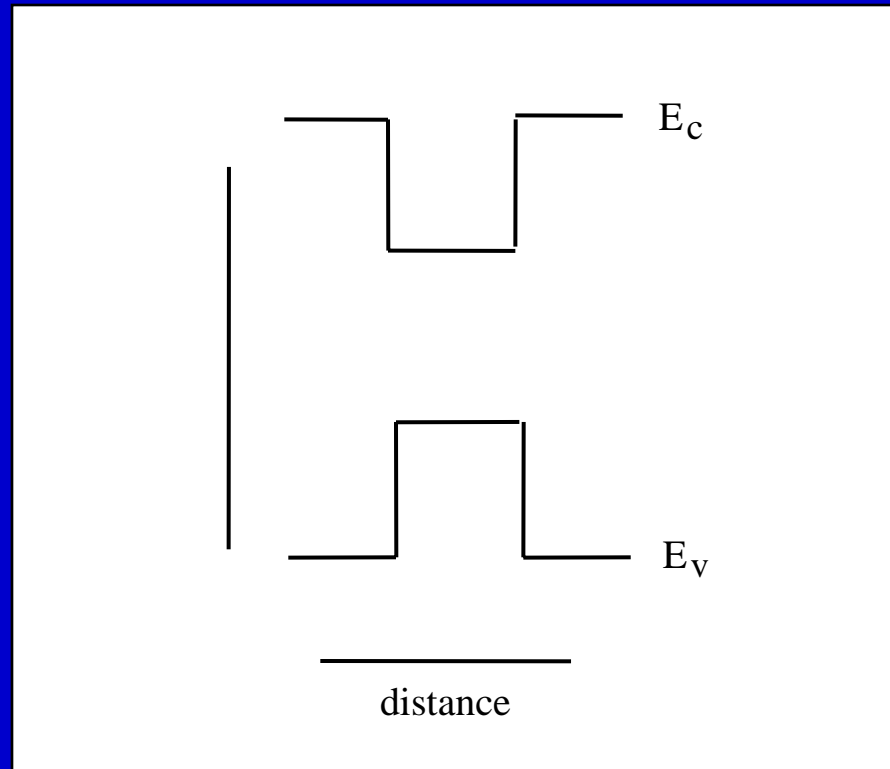
# Heterojunctions

The *conventional p-n diode* uses doping profiles to control current. Using *variation in material composition* gives additional degrees of freedom.



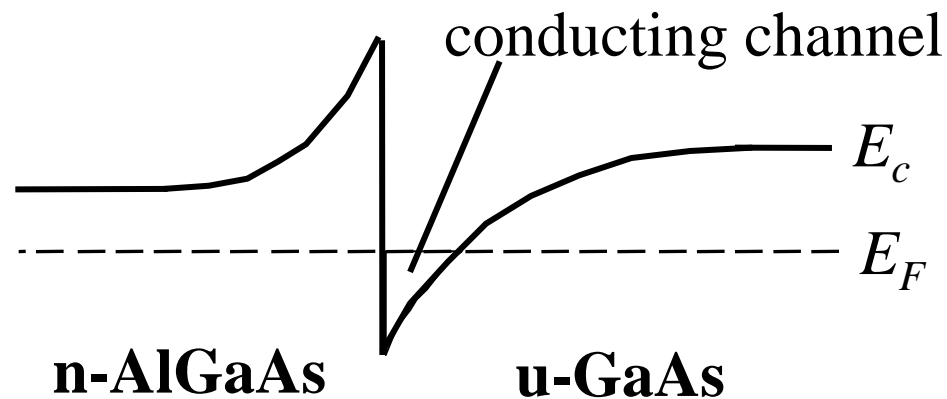
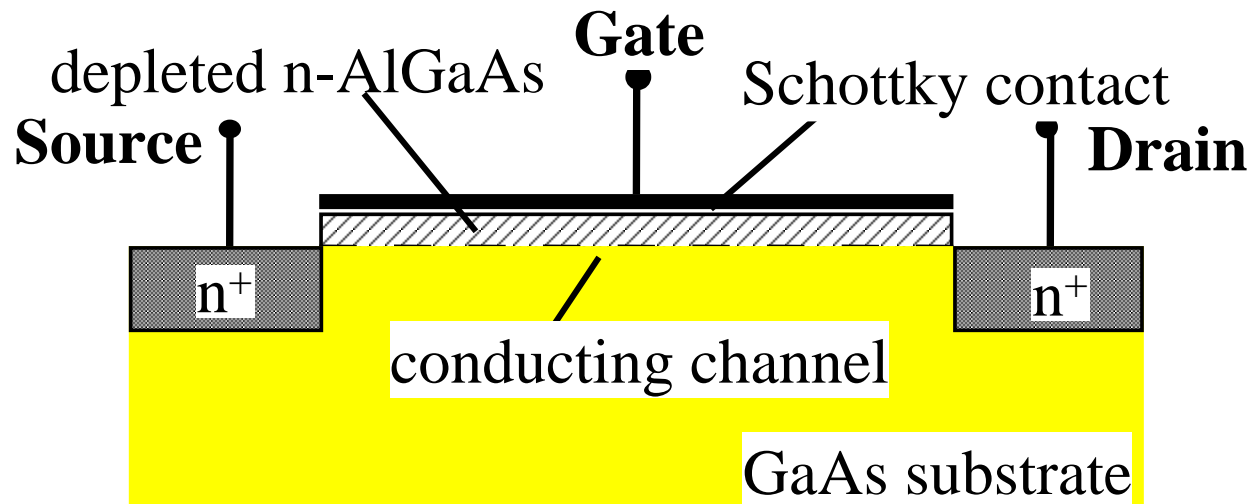
**Graded composition:** May give a different built-in electric field for electrons and holes

# Abrupt Composition

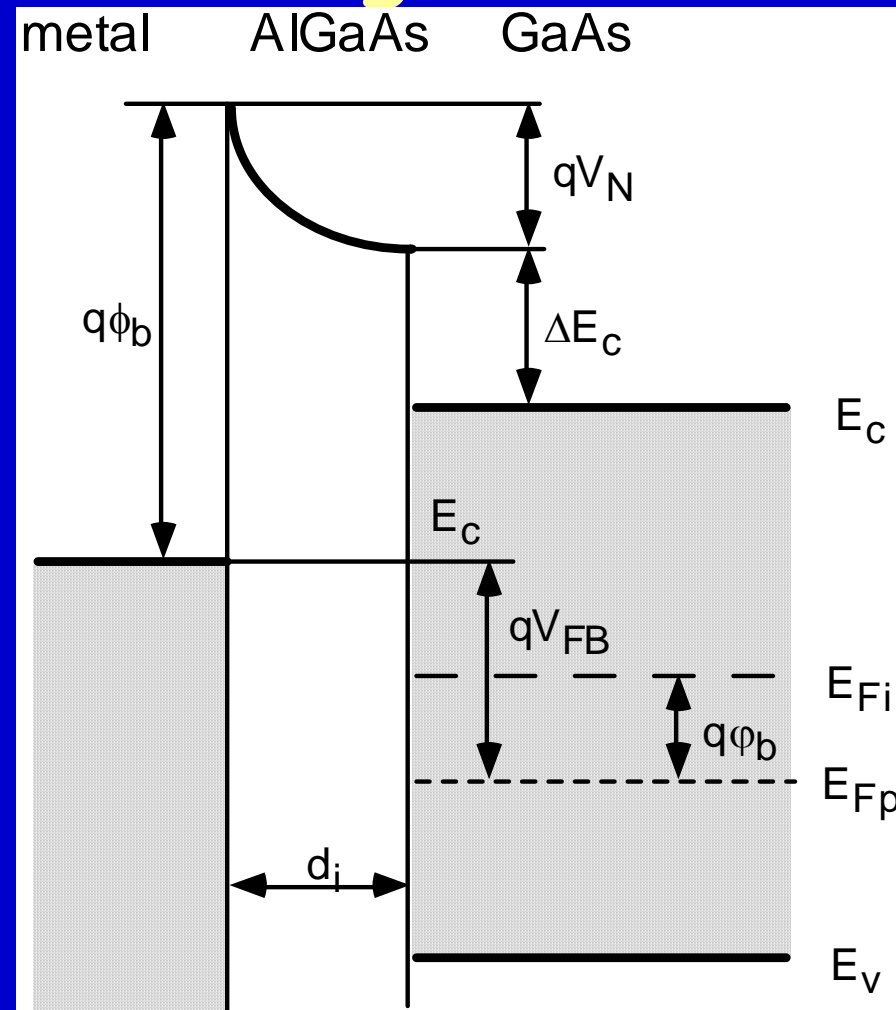


**Abrupt composition:** Forms energy wells and superlattices

# Basic HFET (HEMT) Operation



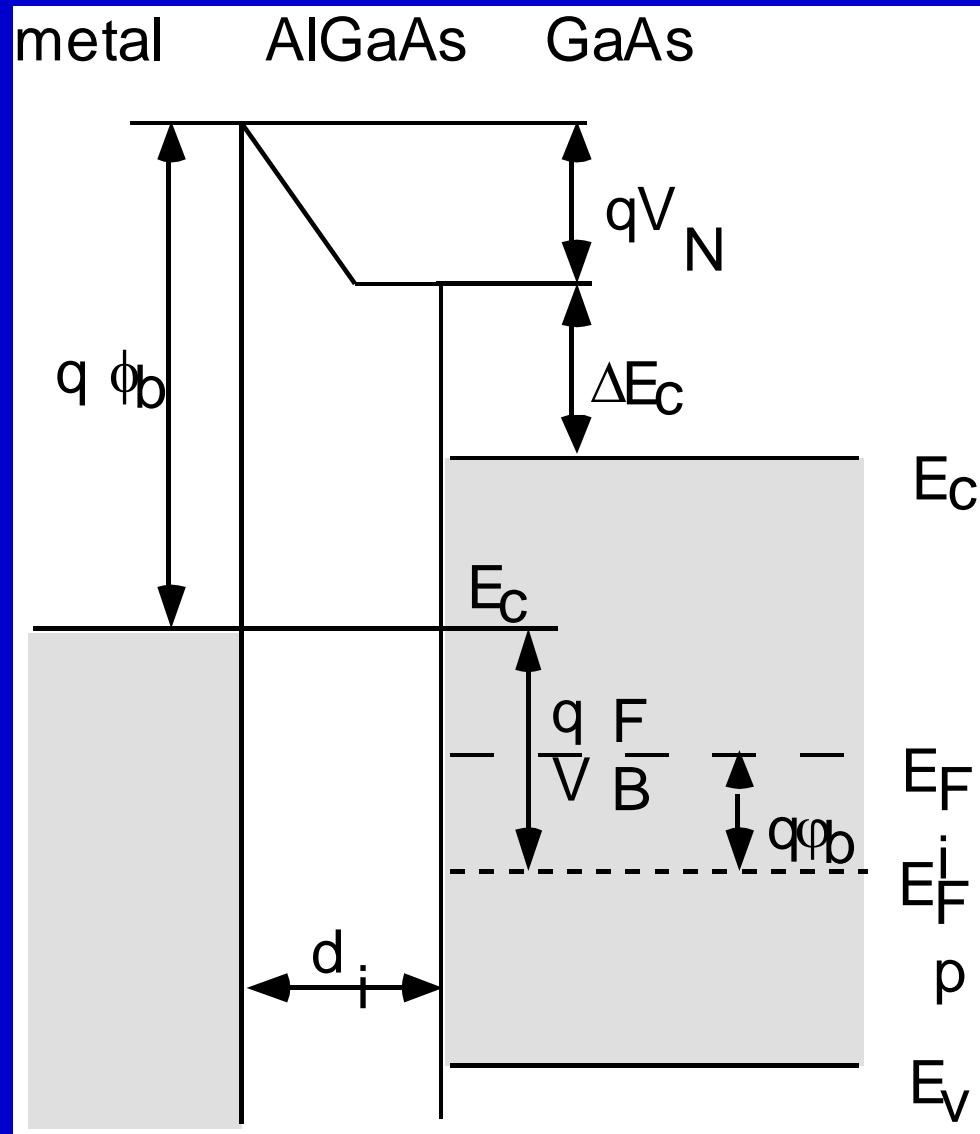
# HFET Band Diagram at Flat Band



from T. A. Fjeldly, T. Ytterdal, M. S. Shur, Introduction to Device Modeling and Circuit Simulation for VLSI, Wiley, 1998

## Delta-doped HFET

# 18



# Threshold voltage

Uniform doping

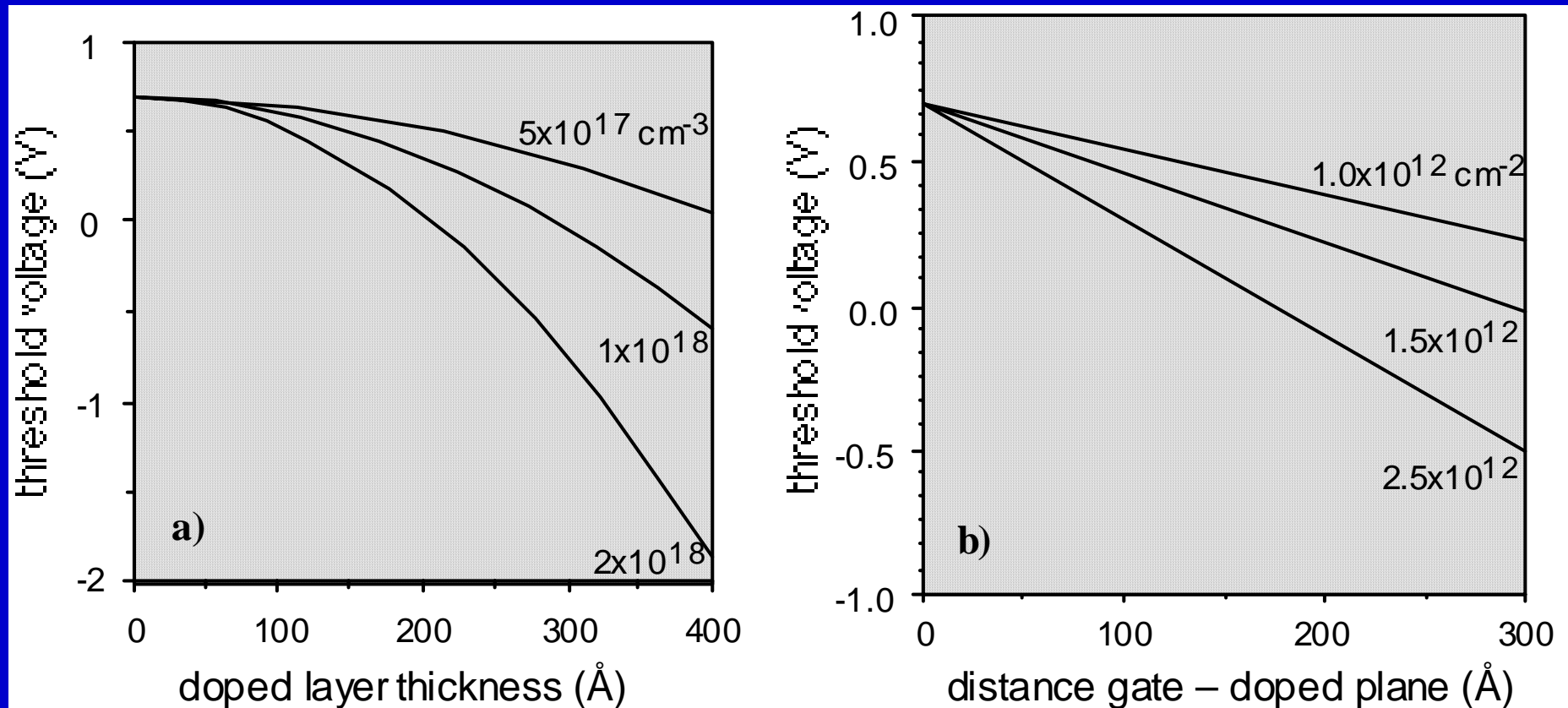
$$V_T \approx \phi_b - \frac{qN_d d_i^2}{2\varepsilon_i} - \Delta E_c / q$$

Delta doping

$$V_T \approx \phi_b - qn_\delta d_\delta / \varepsilon_i - \Delta E_c / q$$



# Threshold voltage versus design parameters



# Basic HFET Operation

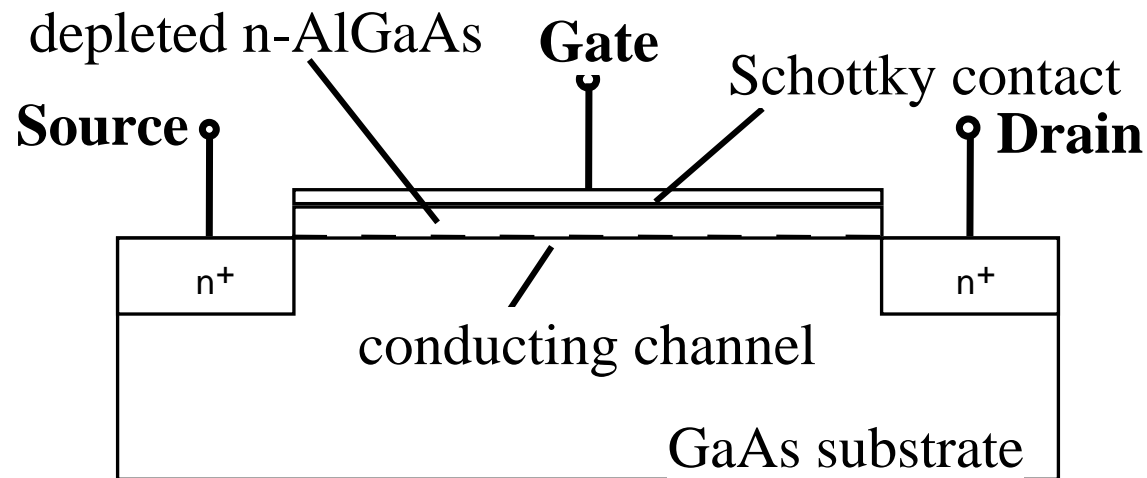
Material system: Typically GaAs/AlGaAs

Channel: Defined by electrons populating the  
quantum well at the GaAs/AlGaAs interface

Operation: Similar to MOSFET

Very fast device –  $f_T > 300$  GHz

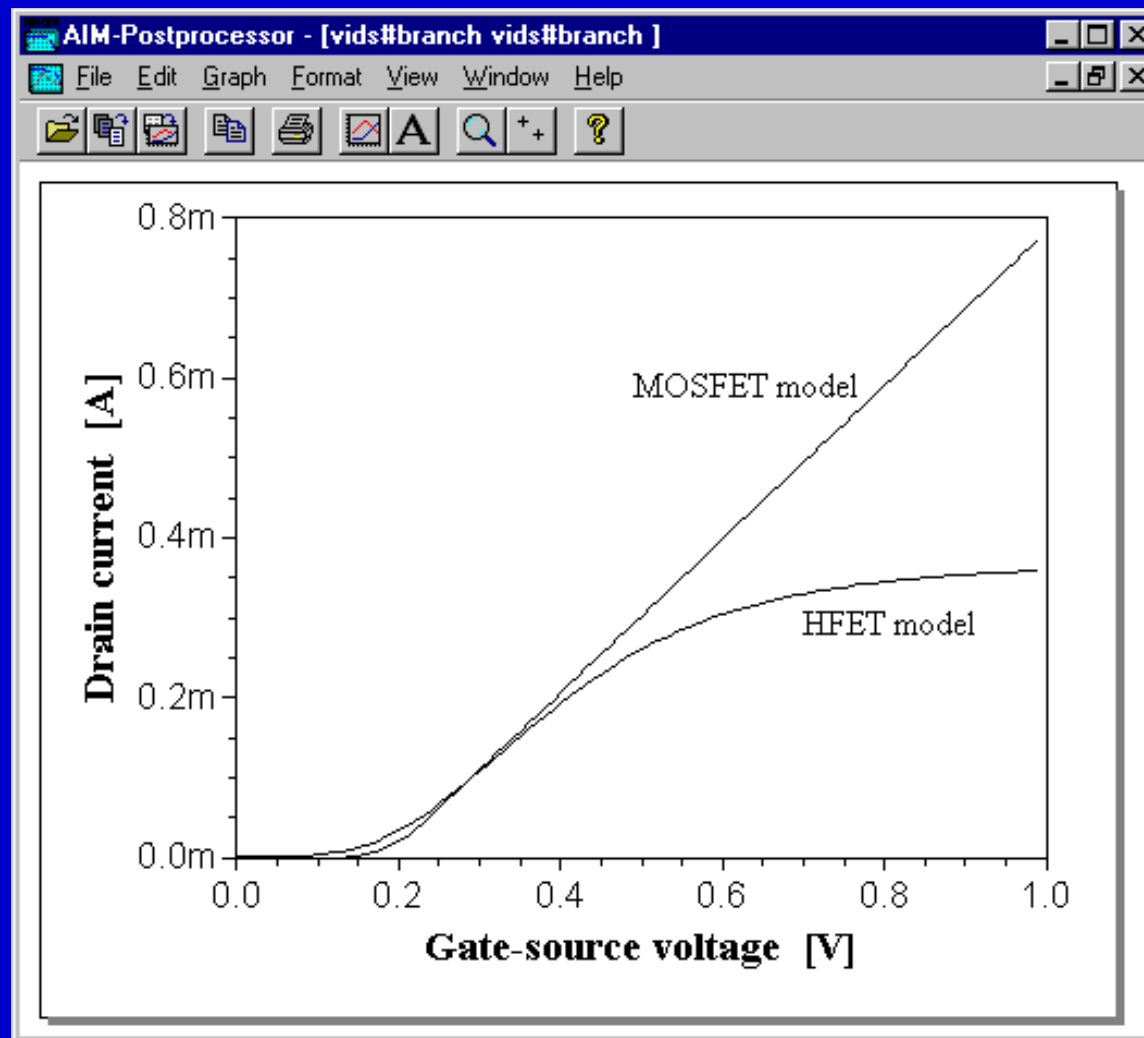
# Basic HFET Model



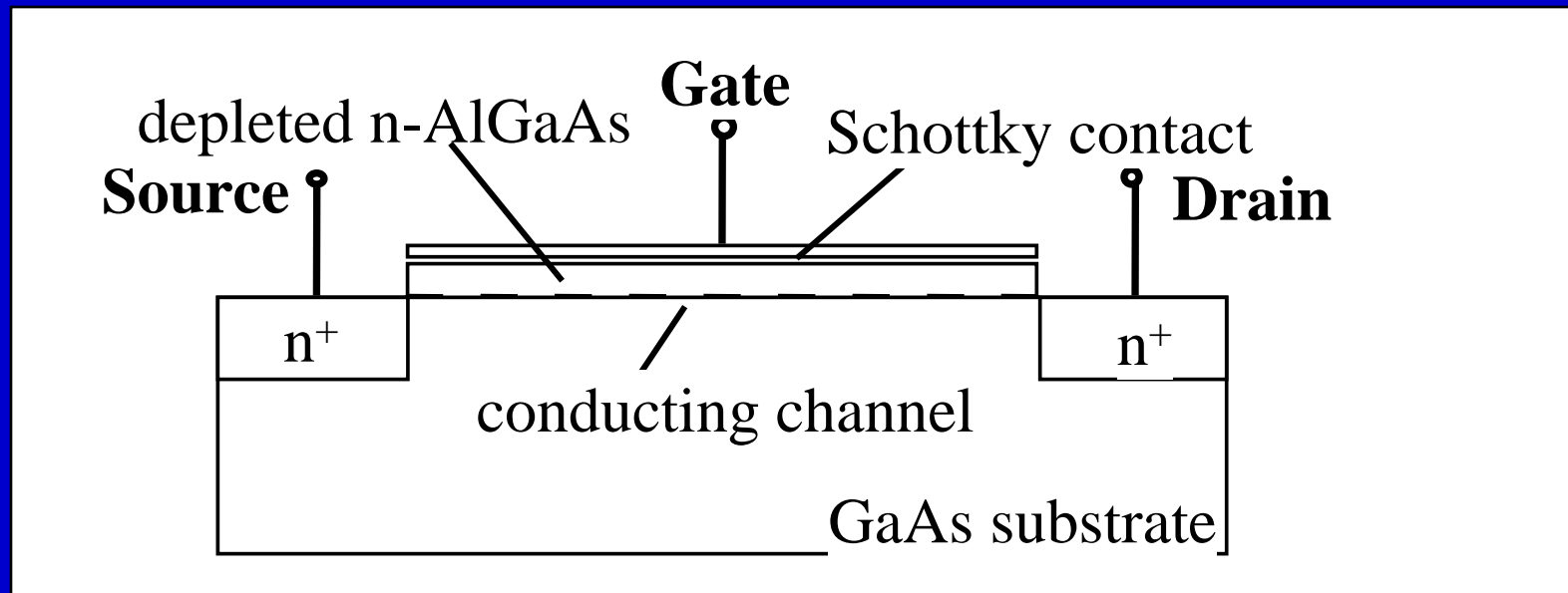
We can use a MOSFET model because of the similarities between HFET and MOSFET.

Quiz: Which parameters should be adjusted?

# Example: HFET Transfer Characteristics



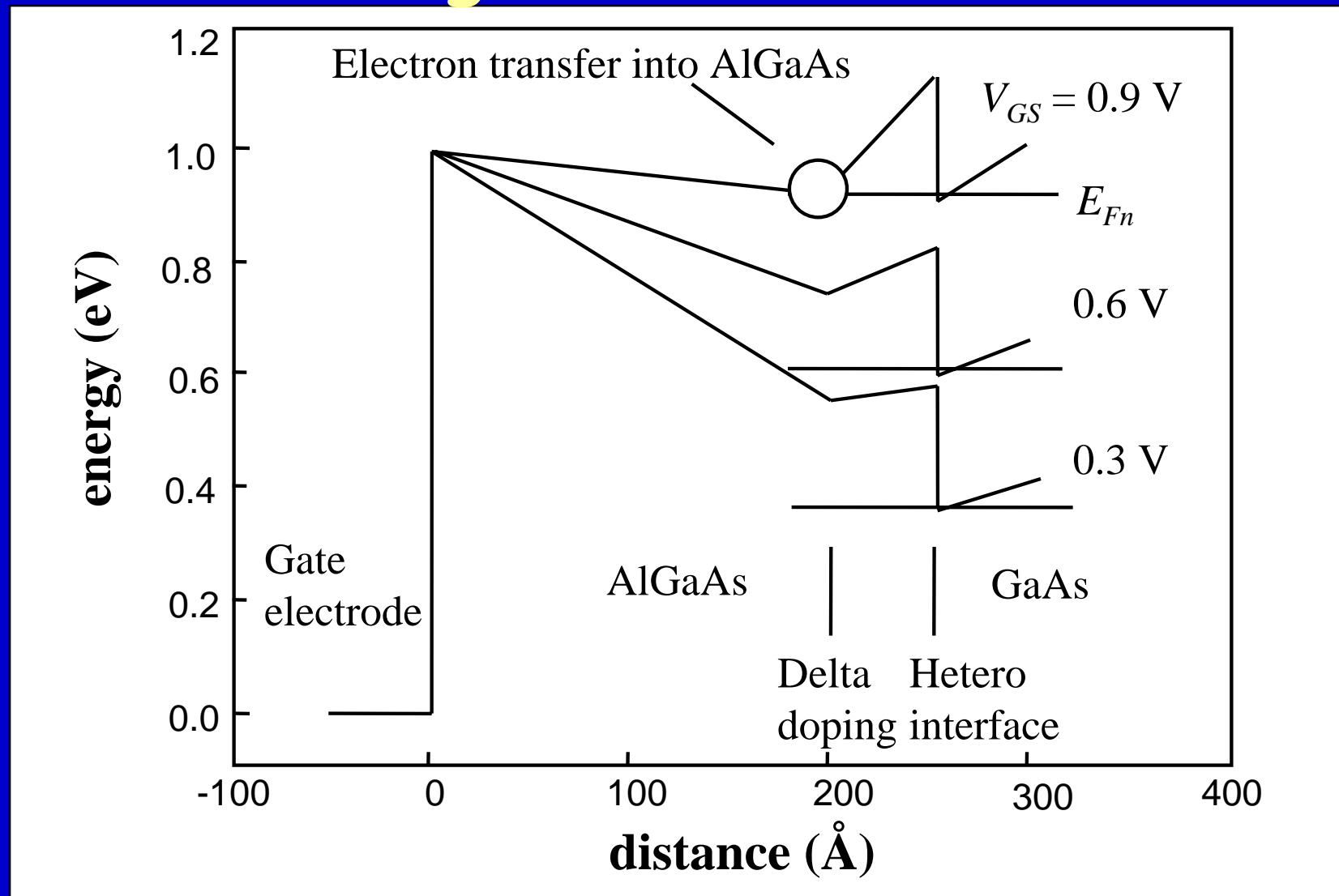
# Universal HFET (HEMT) Model



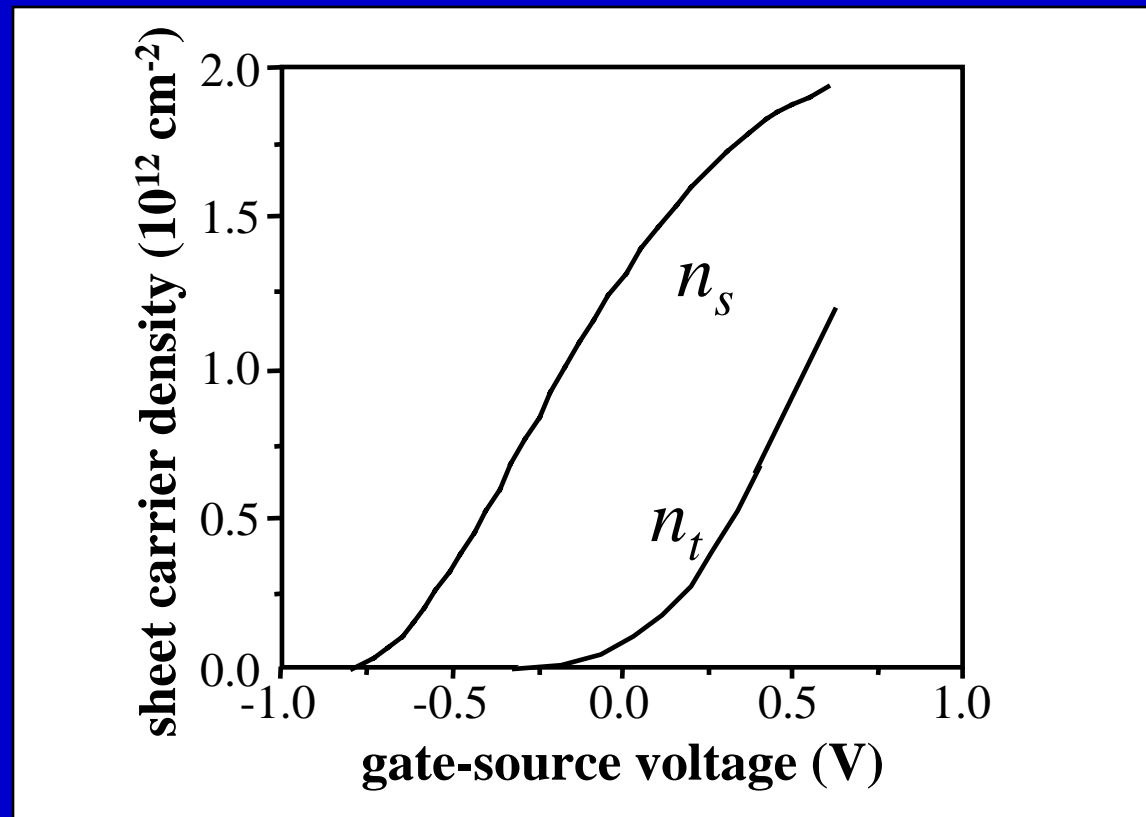
## Two major differences from the MOSFET:

- Charge transfer to the wide band gap semiconductor
- Gate leakage current

# Charge Transfer in HFETs



# Charge Transfer in HFETs (Cont.)



Charge transfer leads to saturation of channel charge and channel current at high gate bias.

# HFET $I_{ds}$ Model

Same as for MOSFET except for:

$$n_{s\_hfet} = \frac{n_{s\_mosfet}}{\left[1 + \left(n_{s\_mosfet} / n_{\max}\right)^{\gamma}\right]^{1/\gamma}}$$



# HFET Capacitance Model

Same as for MOSFET model: Unified Meyer Model:

$$C_{GD} = \frac{2}{3} C_{ch} \left[ 1 - \left( \frac{V_{GTe}}{2V_{GTe} - V_{DSe}} \right)^2 \right] \quad C_{GS} = \frac{2}{3} C_{ch} \left[ 1 - \left( \frac{V_{GTe} - V_{DSe}}{2V_{GTe} - V_{DSe}} \right)^2 \right]$$

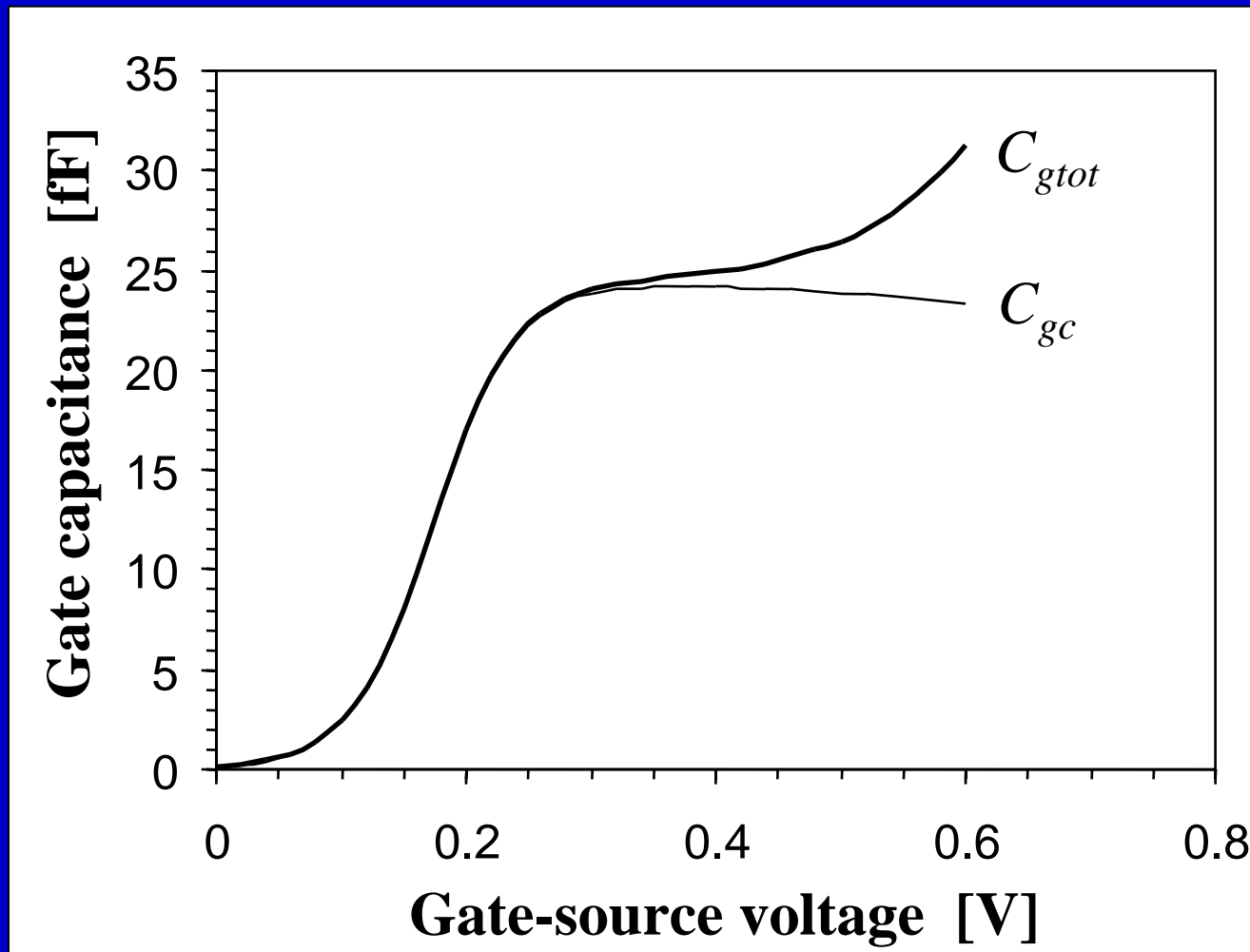
Channel capacitance:

$$C_{ch} = WLq \frac{dn_s}{dV_{GS}}$$

“Parallel channel” capacitance (MOSFET-like):

$$C_{g1} = \frac{C_{i1}}{1 + 2 \exp \left[ -\frac{V_{GS} - V_{T1}}{\eta_1 V_{th}} \right]}$$

# HFET Capacitance Model (Cont.)



# Universal HFET AIM-Spice Model

*Implementation similar to that of the universal MOSFET model*

Major differences:

Gate leakage current included (diode model for  $G-S$  and  $G-D$  junctions)

Use MOSFET expressions and include saturation in  $n_s$

Extra capacitance due to transferred charge

# Example

**Sketch proposed dimensions, material composition, and doping profiles for an HFET with the threshold voltage,  $V_T = -1$  V, and the device transconductance at zero gate bias in the saturation region of at least 300 mS/mm.**

**Justify your choices.**

# Solution:

## Estimate for maximum gm

$$g_m = dI_{ds}/dV_{gs}$$

$$I_{dsmax} = q n_s v_s W$$

$n_s$  is the sheet electron density

$v_s$  is saturation velocity

$$g_{max} = dI_{dsmax}/dV_{gs}$$

$$g_{max} = q v_s W dn_s/dV_{gs}$$

$$n_s = C (V_{gs} - V_t)/q$$

$$C = \epsilon_s/d_i$$

$$g_{max} = q v_s \epsilon_s W/d_i$$

# Solution (continued)

Since the required values of the device transconductance are not very high, we can use a standard  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$  system (as opposed to a pseudomorphic HFET) and a  $1\text{ }\mu\text{m}$  gate geometry. The maximum device transconductance is smaller than .

$$g_{\max} = \frac{\epsilon_s v_s}{d_i} \left( \frac{mS}{mm} \right)$$

where  $\epsilon_s = 1.14 \times 10^{-10} \text{ F/m}$ ,  $v_s$  is the electron saturation velocity,  $d_i$  is the gate-to-channel separation. Assuming a conservative value of  $v_s = 1 \times 10^5 \text{ m/s}$  and estimating  $g_m(V_g=0) = g_{\max}/2$ , we find

$$d_i = \frac{\epsilon_s v_s}{2g_m} = \frac{1.14 \times 10^{-10} \times 10^5}{2 \times 300} = 1.9 \times 10^{-8} (m)$$

Hence, we choose  $d_i = 200 \text{ \AA}$ .

## Solution (continued)

We choose a  $\delta$ -doped design, and place the doping plane at the distance of  $d_\delta = 150 \text{ \AA}$  from the gate. The device threshold voltage can be estimated as

$$V_T = \Phi_b - \Delta E_c - \frac{qN_\delta d_\delta}{\epsilon_s}$$

where the barrier height  $\Phi_b = 1 \text{ eV}$ , the conduction band discontinuity,  $\Delta E_c = 0.3 \text{ eV}$ ,  $q = 1.602 \times 10^{-19} \text{ C}$  is the electronic charge,  $N_\delta$  is the surface density of ionized donors in the  $\delta$ -doped plane. Hence,

$$N_\delta = \frac{\epsilon_s (\Phi_b - \Delta E_c - V_T)}{q d_\delta} = \frac{1.14 \times 10^{10} (1 - 0.3 + 1)}{1.602 \times 10^{-19} \times 1.5 \times 10^{-8}} = 8.06 \times 10^{16} \text{ (m}^{-2}\text{)}$$

We can now check if this design meets the specs.

## Solution, continued 1

The intrinsic HFET drain saturation current in the above threshold regime is given by

$$I_{sat} = \beta V_L^2 \left[ \sqrt{1 + \left( \frac{V_{GT}}{V_L} \right)^2} - 1 \right]$$

where  $V_{GT} = V_{GS} - V_T$ ,  $V_L = v_s L / \mu$ ,  $\beta = \frac{\epsilon_s \mu}{(d_i + \Delta d)} \frac{W}{L}$   $\mu$  is the mobility (we assume  $\mu = 0.5 \text{ m}^2/\text{Vs}$ ),  $\Delta d$  is the effective thickness of the 2d electron gas ( $\Delta d \sim 50 \text{ \AA}$ ),  $L$  is the gate length ( $1 \text{ }\mu\text{m}$ ),  $W$  is the gate width. (For simplicity, we assume equal dielectric permittivities for AlGaAs and GaAs.). Differentiating this equation with respect to  $V_{GS}$ , we find the intrinsic transconductance

$$g_{mi} = \frac{\beta V_{GT}}{\sqrt{1 + \left( \frac{V_{GT}}{V_L} \right)^2}}$$



## Solution, continued 2

For the chosen device parameters

$$\beta = \frac{1.14 \times 10^{-10} \times 0.5 \times 10^{-3}}{(200 + 50) \times 10^{-10} \times 10^{-6}} = 2.28 \left( \frac{S}{Vmm} \right)$$

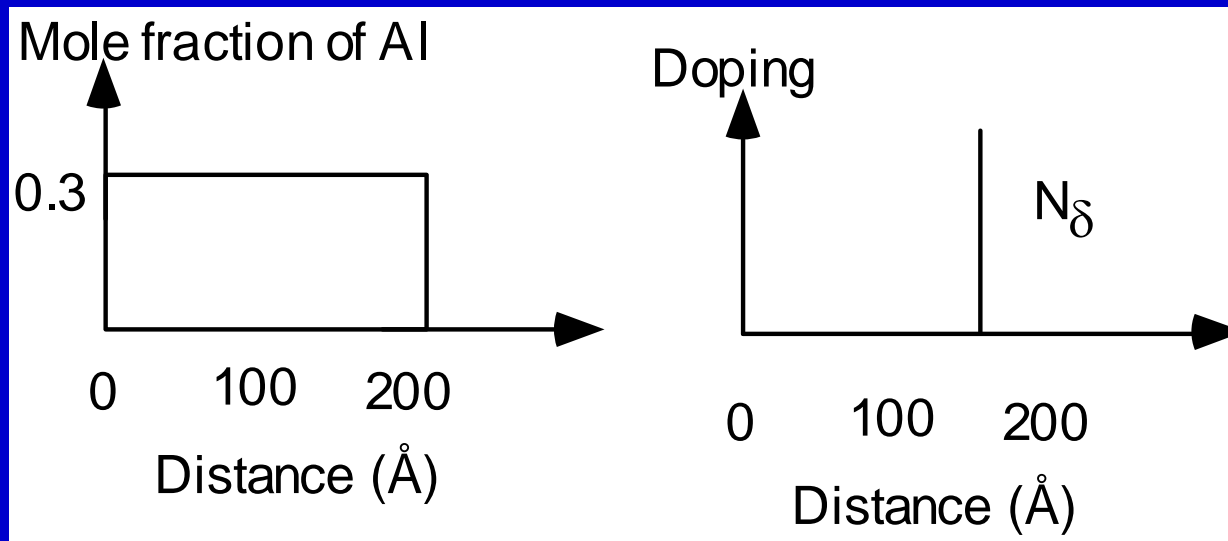
$$V_L = 0.2 \text{ V}$$

$$g_{mi} = \frac{2.28 \times 1}{\sqrt{1 + \left( \frac{1}{0.2} \right)^2}} = 0.447 \left( \frac{S}{mm} \right) = 447 \left( \frac{mS}{mm} \right)$$

Assuming a source series resistance  $R_s = 0.5 \text{ ohm mm}$ , we find

$$g_m = \frac{g_{mi}}{1 + g_{mi} R_s} = \frac{0.447}{1 + 0.447 \times 0.5} = 0.365 \left( \frac{S}{mm} \right) = 365 \left( \frac{mS}{mm} \right)$$

# Composition and doping profiles



## Solution (numerics)

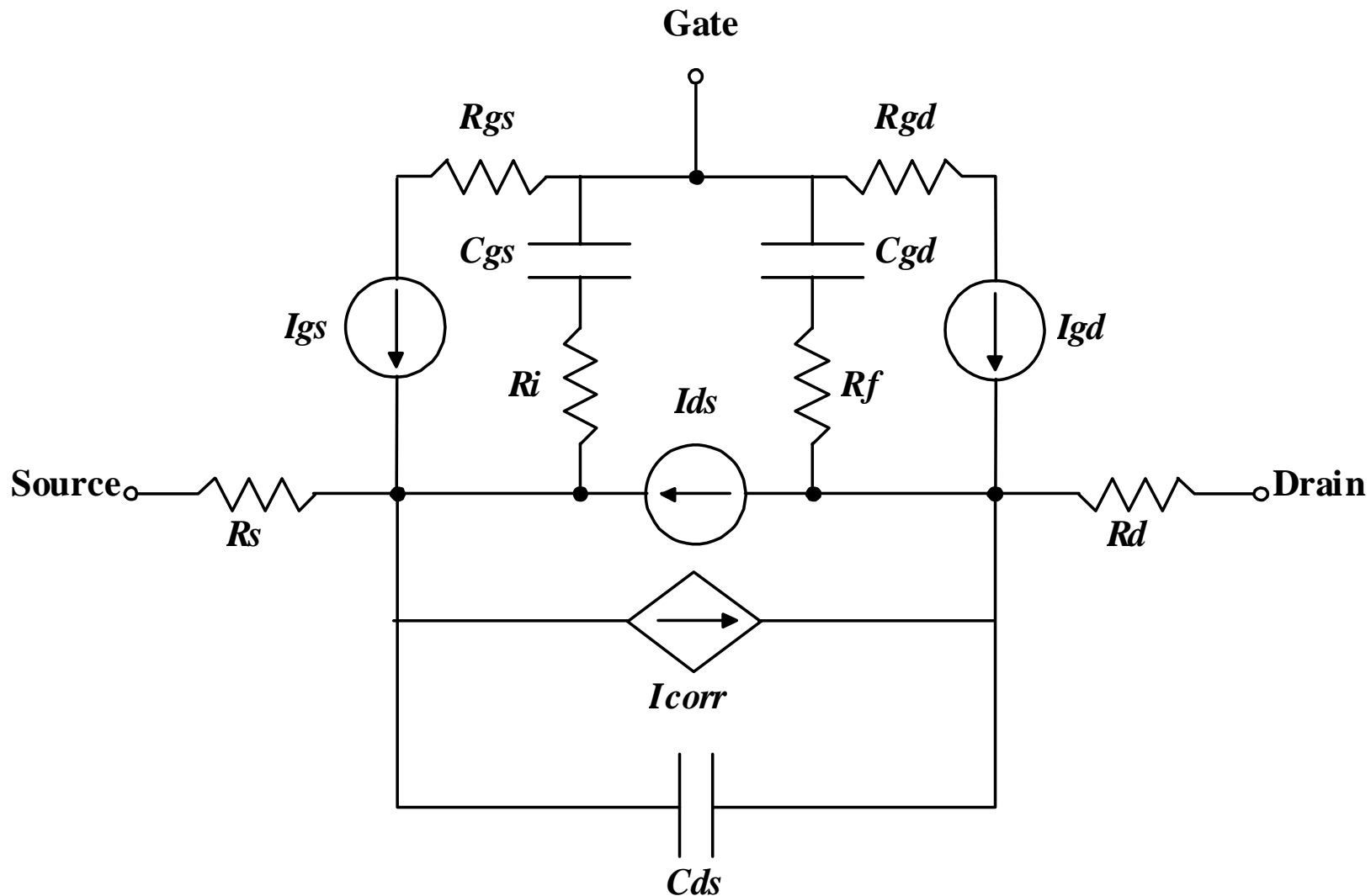
For the chosen device parameters

$$V_L = 0.2 \text{ V}$$

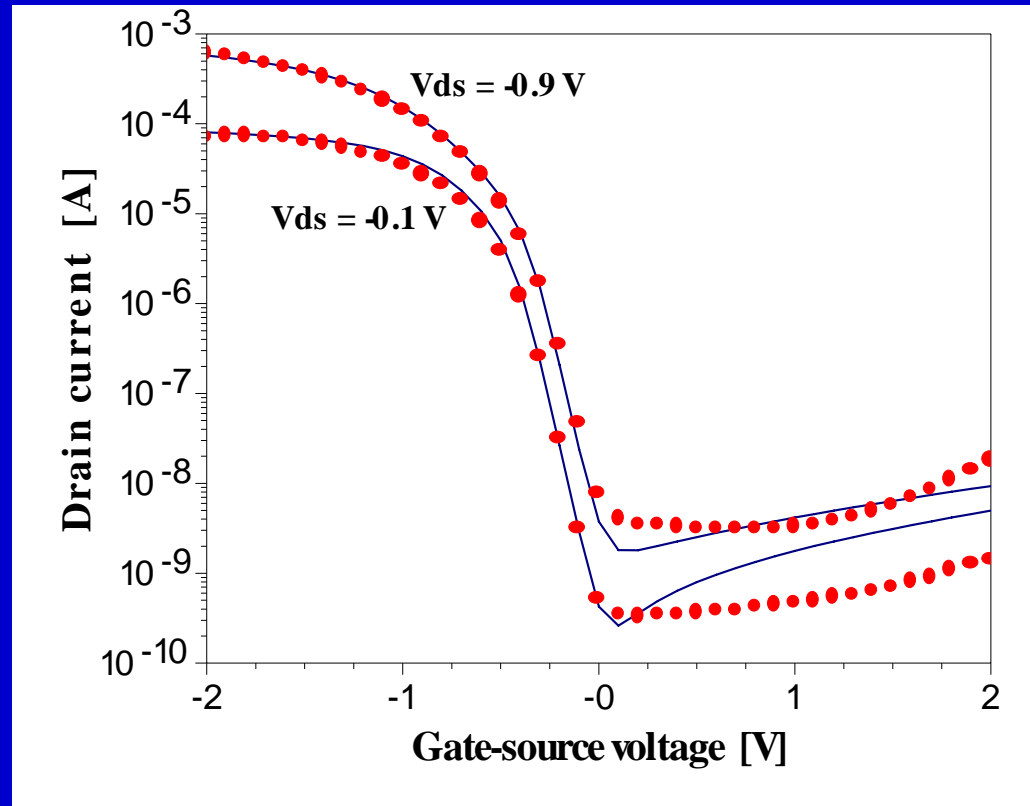
Assuming a source series resistance  $R_s = 0.5 \text{ ohm-mm}$ , we find

Hence, our design is satisfactory.

# HEMT equivalent circuit

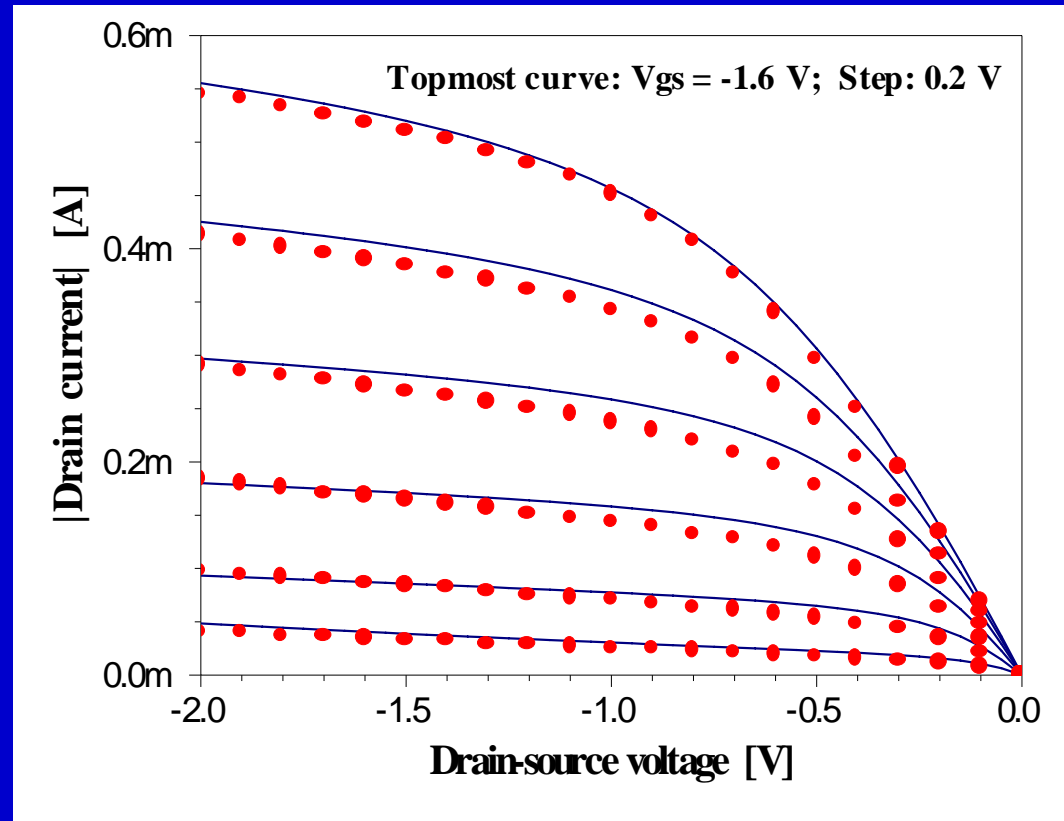


# P-channel HFET



T. Ytterdal, Tor A. Fjeldly, Michael S. Shur, S. Baier, R. Lucero, Complementary Heterostructure Field Effect Transistor Models for Mixed Mode Applications, Proceedings of ISDRS-97, pp. 619-622, Charlottesville, VA, Dec. (1997)

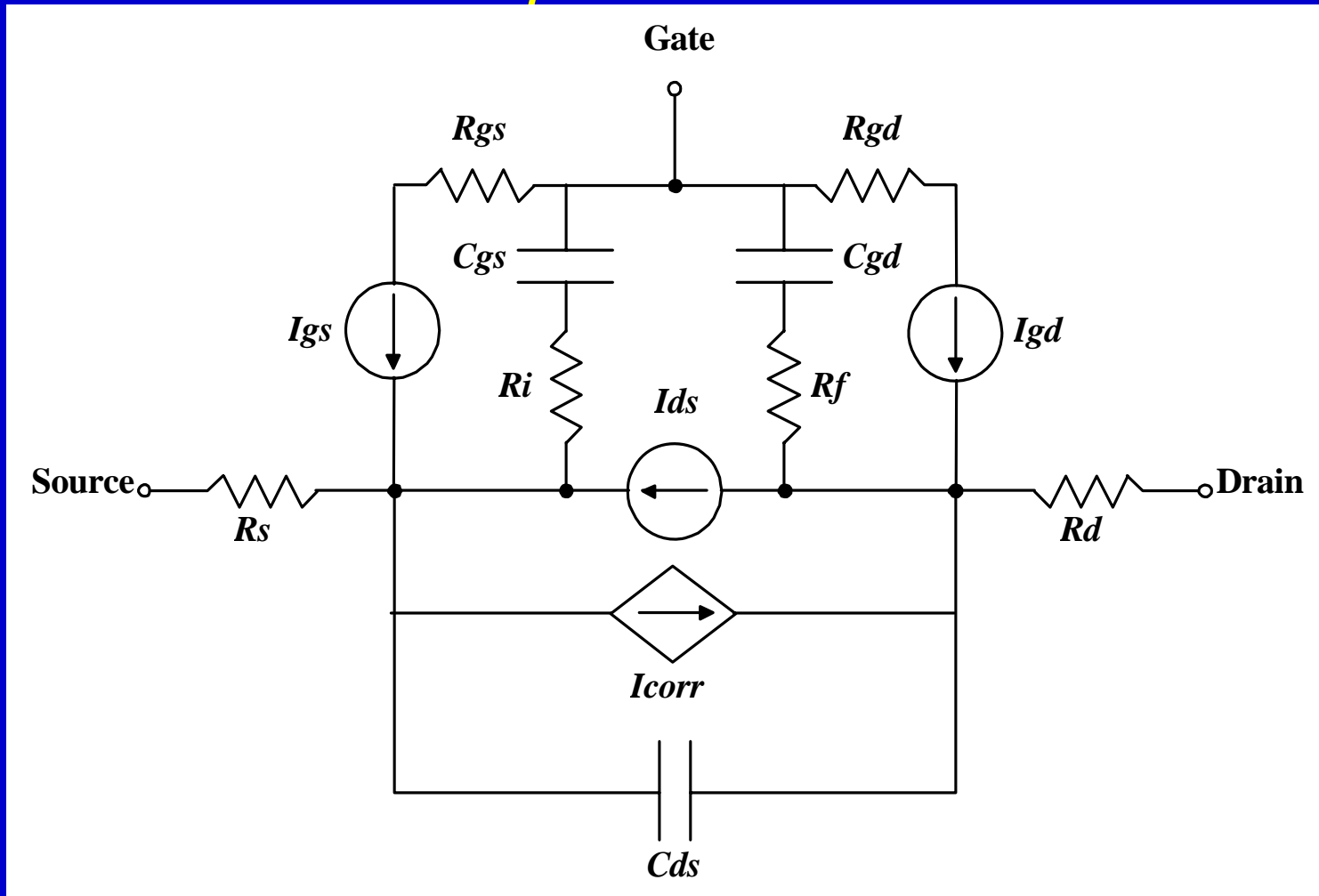
# P-channel HFET ( $I_{ds}$ versus $V_{ds}$ )



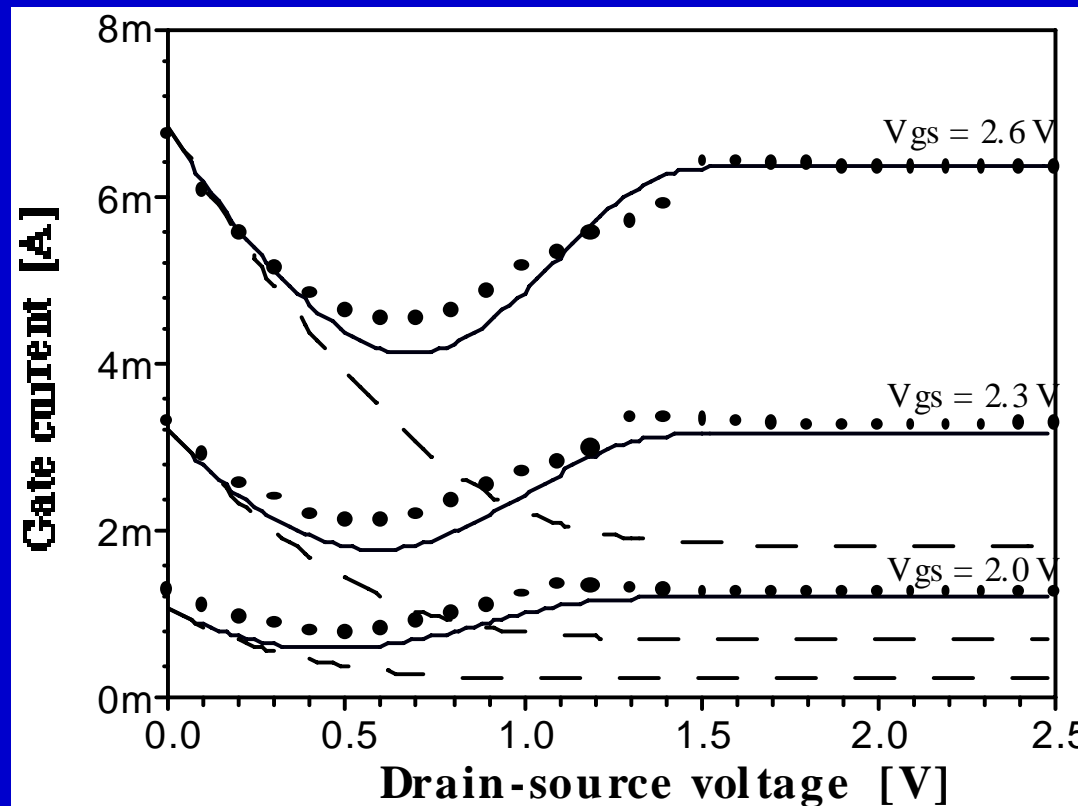
T. Ytterdal, Tor A. Fjeldly, Michael S. Shur, S. Baier, R. Lucero, Complementary Heterostructure Field Effect Transistor Models for Mixed Mode Applications, Proceedings of ISDRS-97, pp. 619-622, Charlottesville, VA, Dec. (1997)

# The AIM-Spice HFET Model

## *Equivalent Circuit*



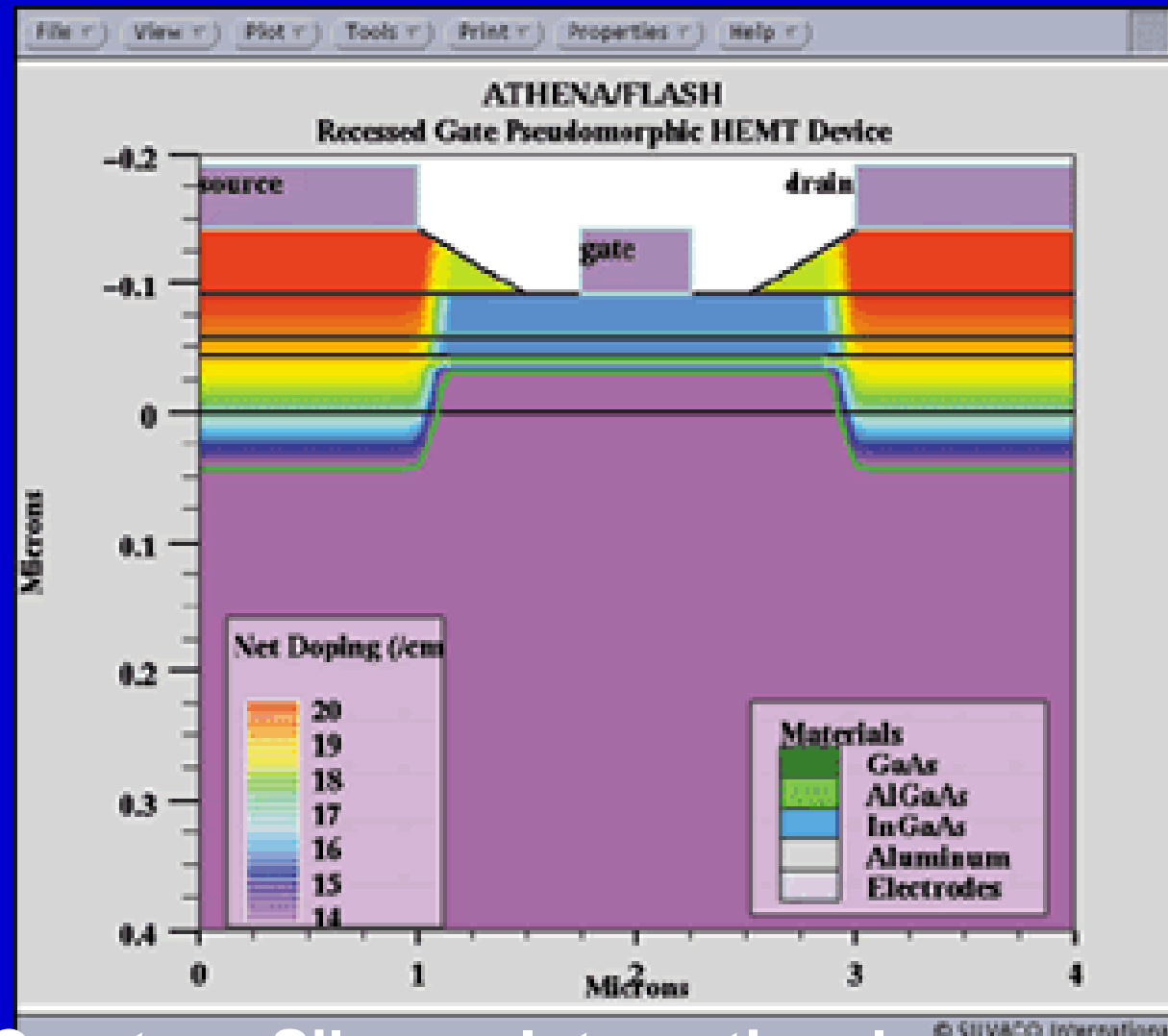
# Gate leakage



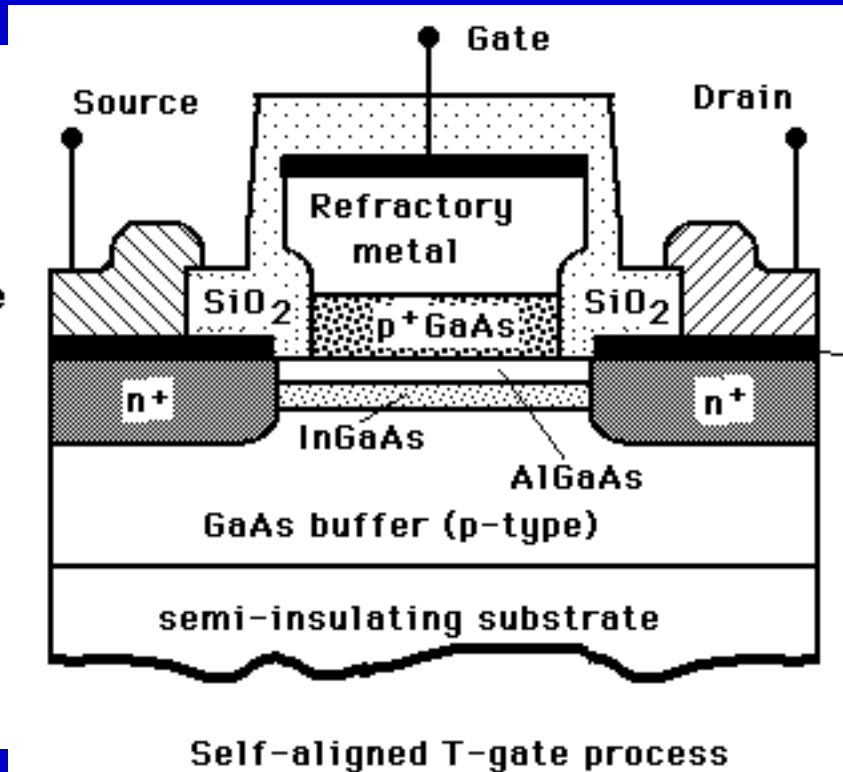
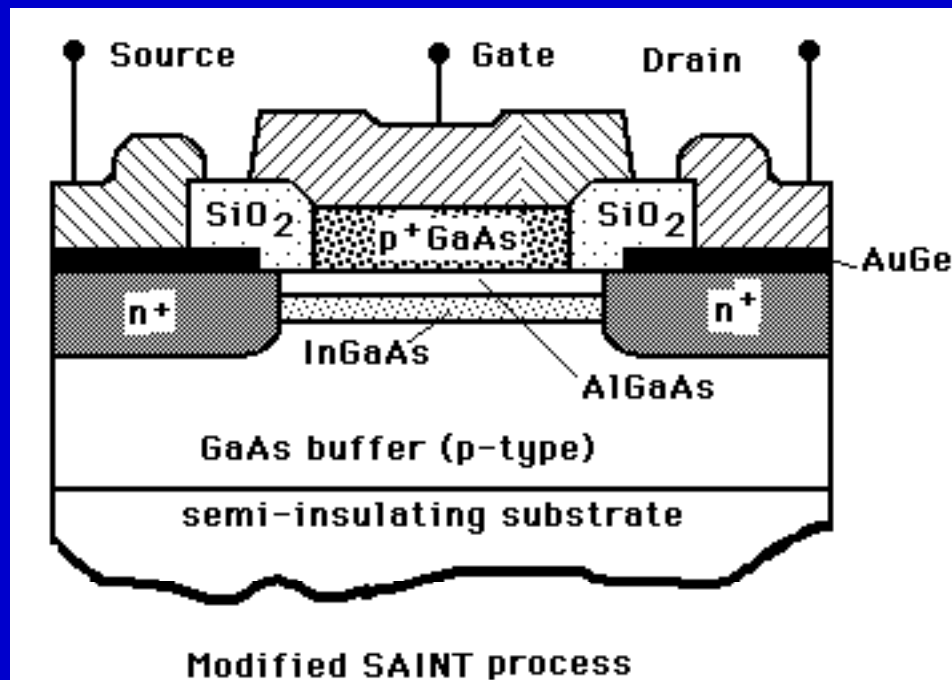
T. Ytterdal, Tor A. Fjeldly, Michael S. Shur, S. Baier, R. Lucero, Complementary Heterostructure Field Effect Transistor Models for Mixed Mode Applications, Proceedings of ISDRS-97, pp. 619-622, Charlottesville, VA, Dec. (1997)



# 2D Simulation Using Silvaco Flash

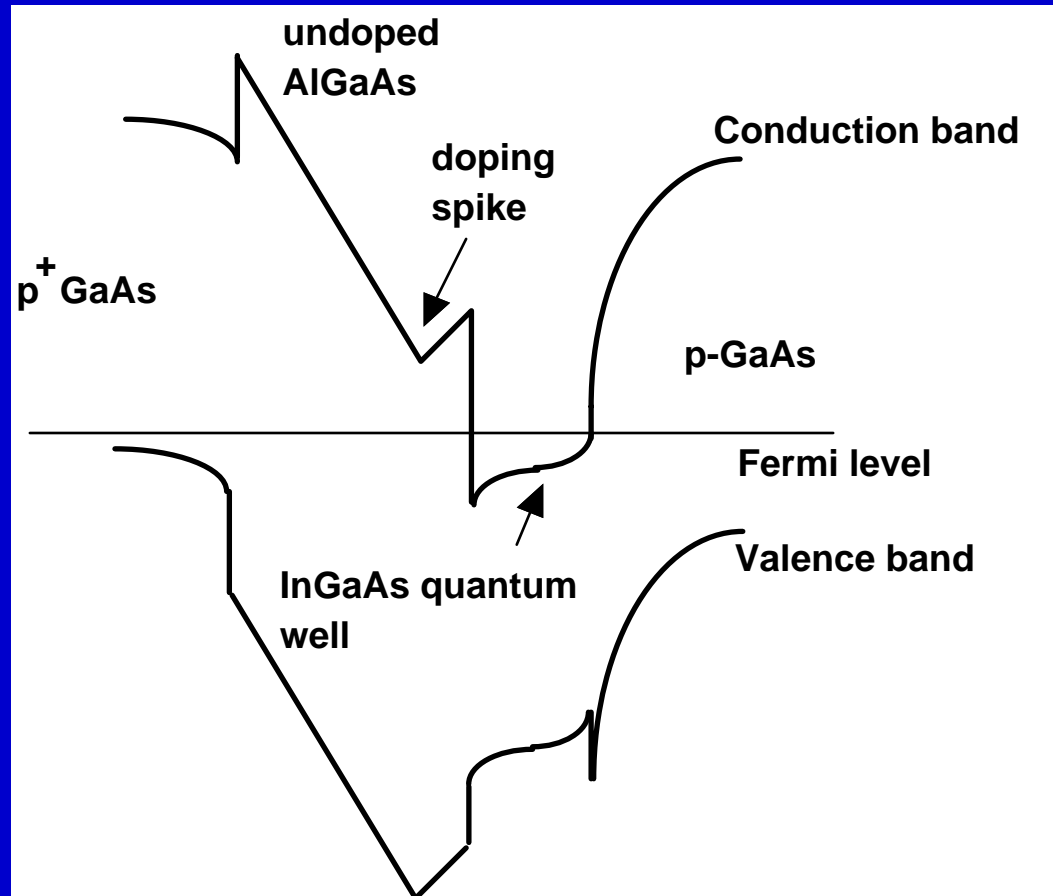


Courtesy Silvaco, International

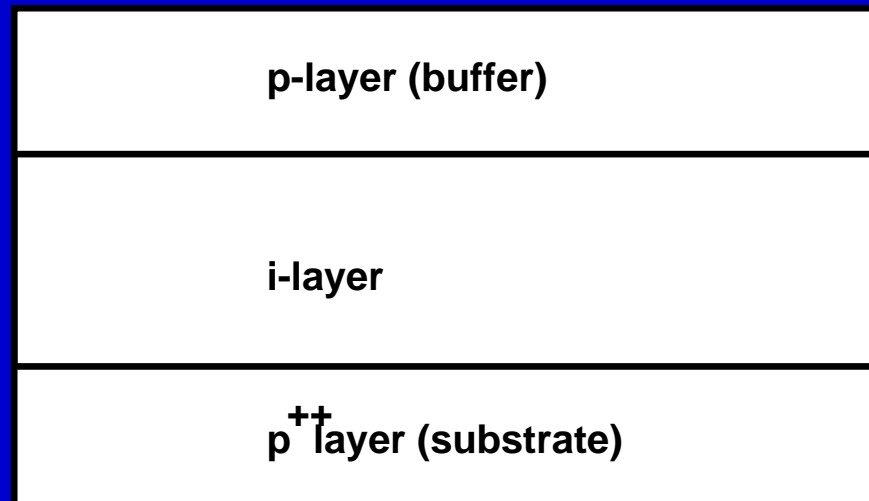
$\pi$ -HFET

Two possible implementations of  $\pi$ -HFET fabricated using a modified SAINT process (a) and modified T-gate process (b).

# $\pi$ -HFET Band Diagram

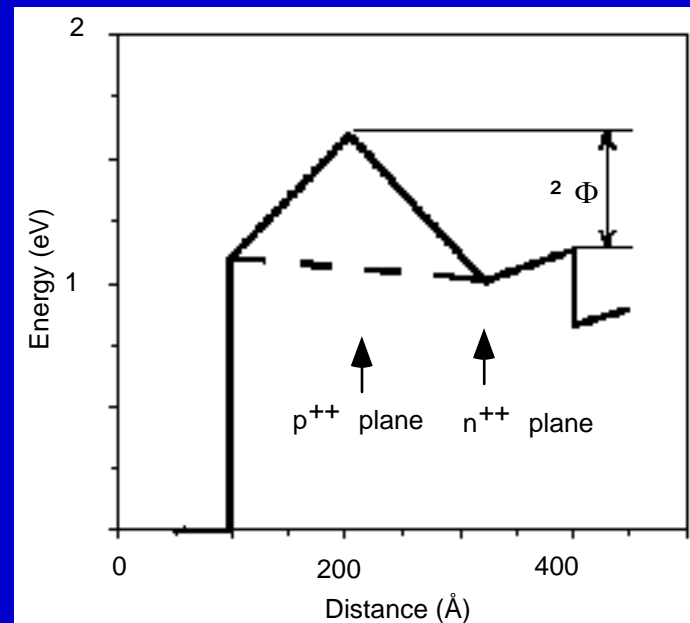


# p-i-p<sup>+</sup> Buffer



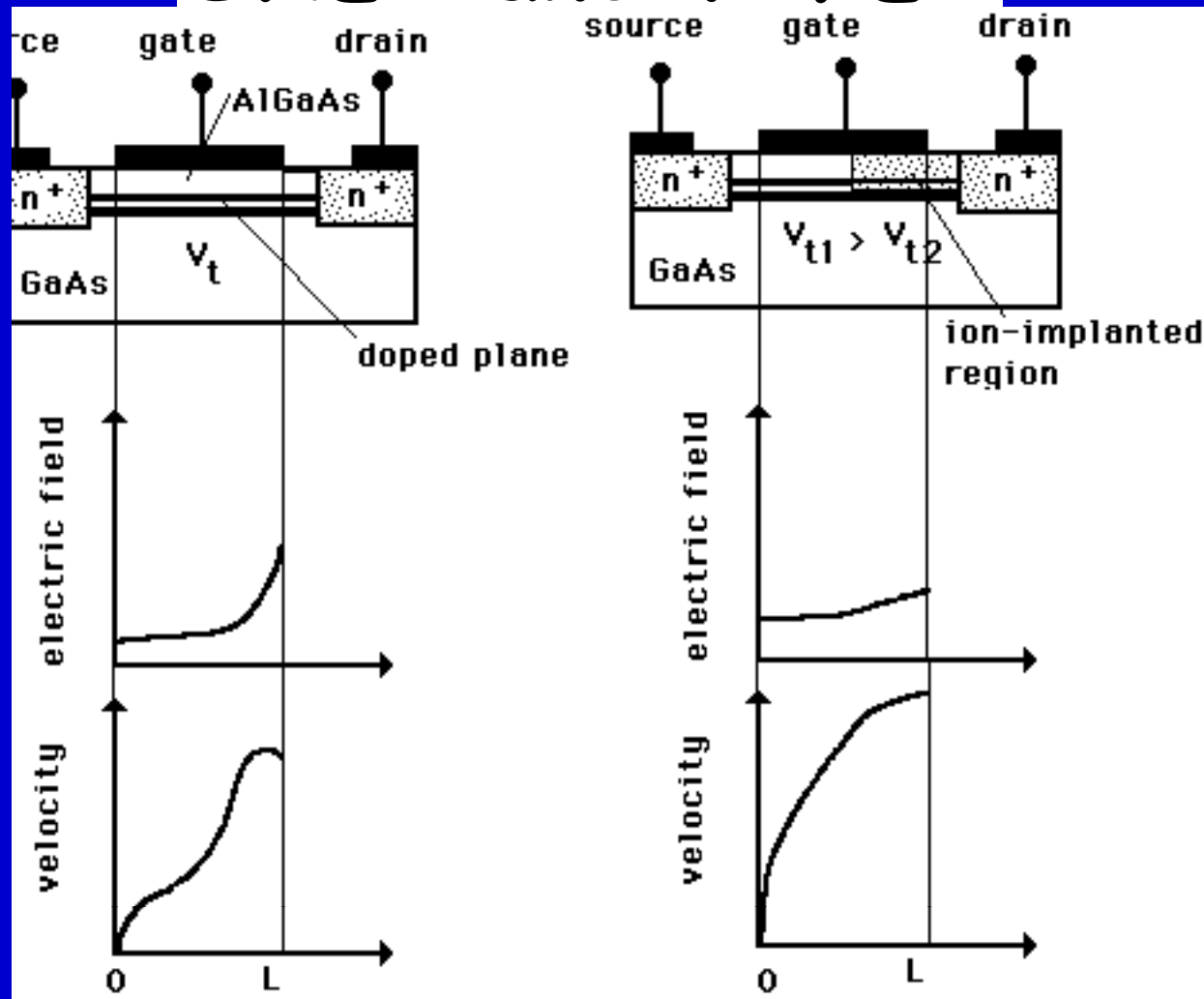
Layer structure replacing the p-type buffer layer. Here, the heavily doped  $p^{++}$  layer provides the low impedance ground plane, thus reducing the electrical noise, sidegating, and unintentional backgating. The  $i$ -layer between the  $p$ -type buffer layer and the  $p^{++}$  layer reduces the parasitic capacitance. (from Lee and Shur (1990)).

# Conventional and Dipole HFET



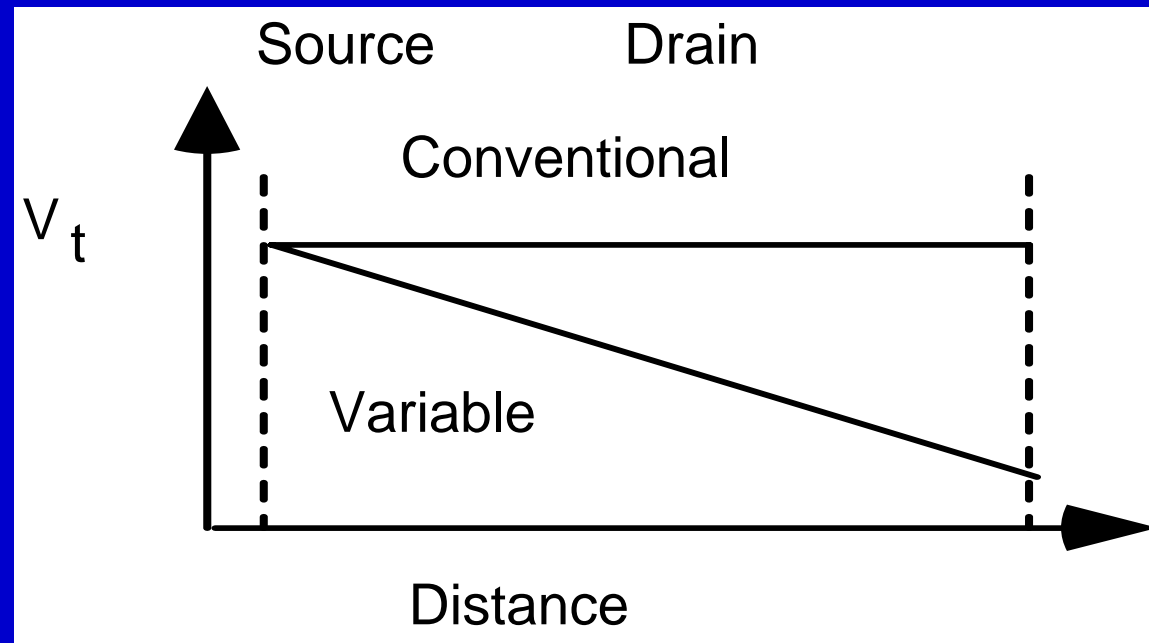
Band diagrams of conventional  $\delta$ -doped HFET (dashed line) and Dipole HFET (solid line) for the same density of 2D electron gas

# SHET and VTFET

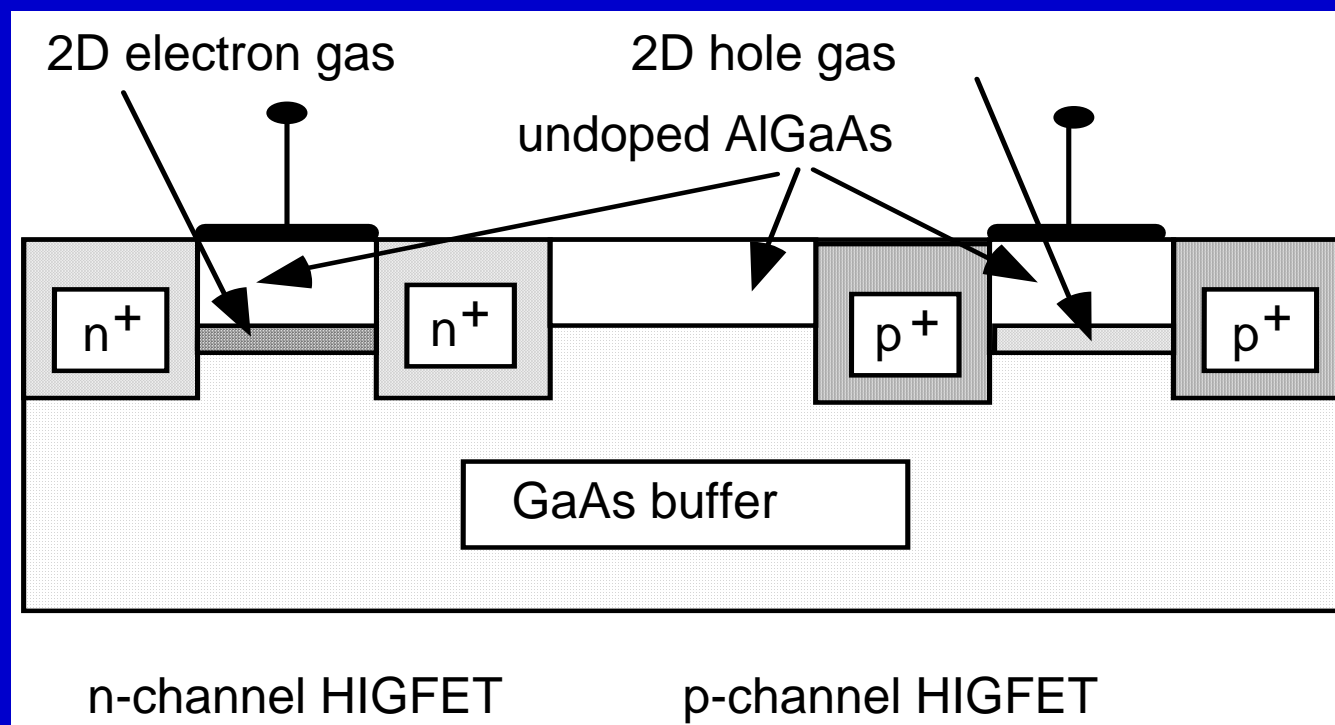


Qualitative velocity and electric field profiles versus distance for uniform and variable-threshold FETs (from Shur (1989)).

# Threshold Voltage in VTFET

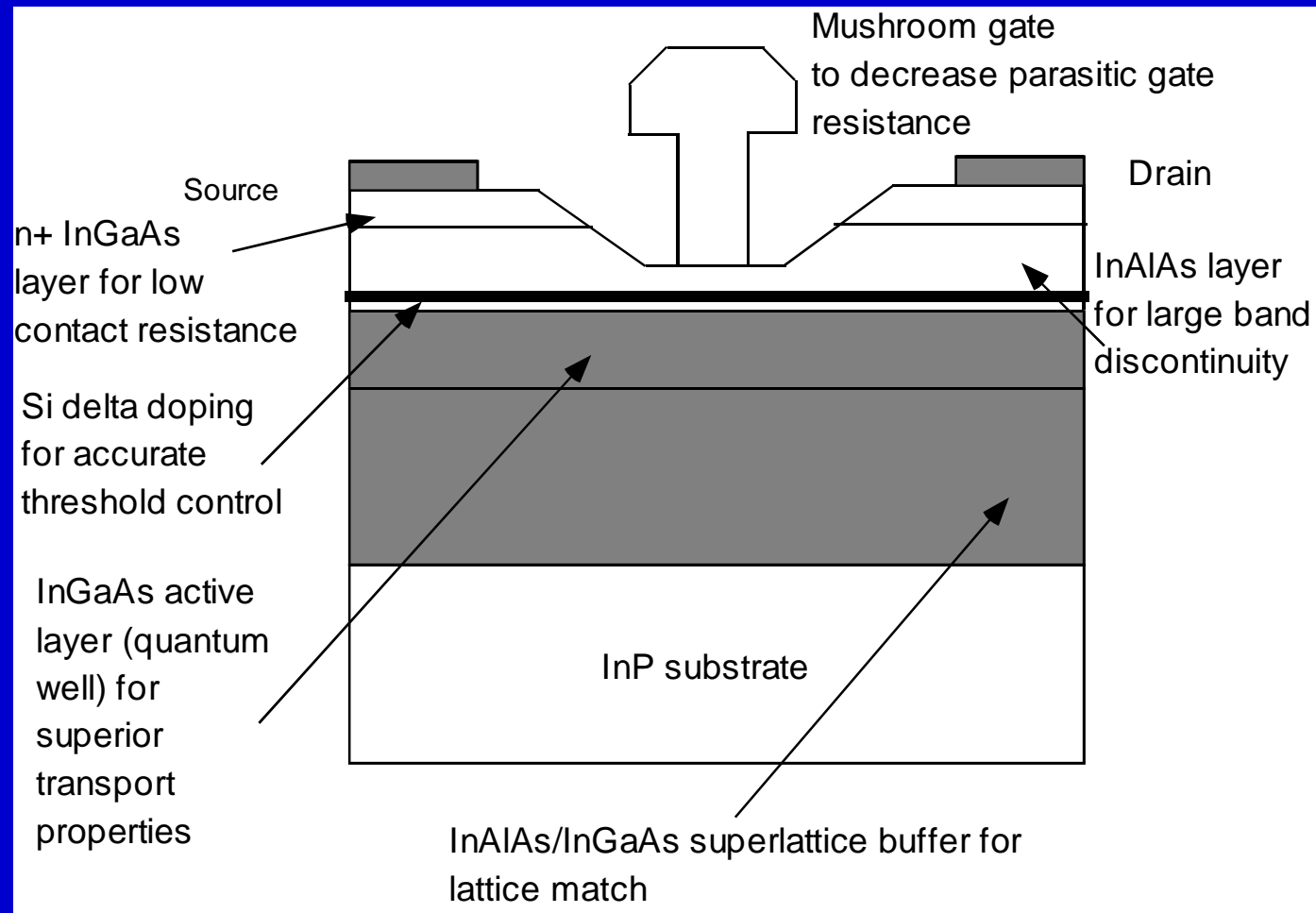


# Complementary n-channel and p-channel HIGFETs





# InP based HFETs



# Advantages of InP based HFETs

**Lower noise**

**Higher cutoff frequency**

**Higher gain**

**Operating voltage below 3 V**

T. Shuemitsu et al. (NTT) reported on InP-based HEMT with the gatelength of 30 nm with cutoff frequency of 350 GHz (1998IEDM conference)

# Metamorphic HEMT on GaAs Substrate (MM-HEMT)

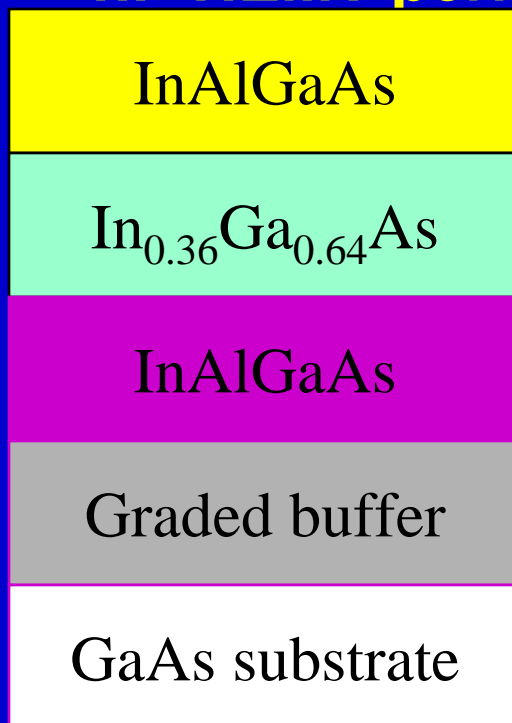
$\text{In}_y\text{Al}_{1-y}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$  system

y and x chosen to match the lattice constants of  
 $\text{In}_y\text{Al}_{1-y}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}$  layers

A metamorphic buffer ( $\text{In}_z\text{Al}_{1-z}\text{As}$  or  $\text{In}_z\text{Ga}_{1-z}\text{As}$   
with  $0 < z < x$ ) is grown at low temperature to  
accommodate the mismatch between the  
GaAs substrate and the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  active  
layer

# Metamorphic HEMT (example)

## InP HEMT performance on GaAs substrate



Room temperature mobility 7,500  $\text{cm}^2/\text{V-s}$   
(for GaAs 6,600  $\text{cm}^2/\text{V-s}$ )

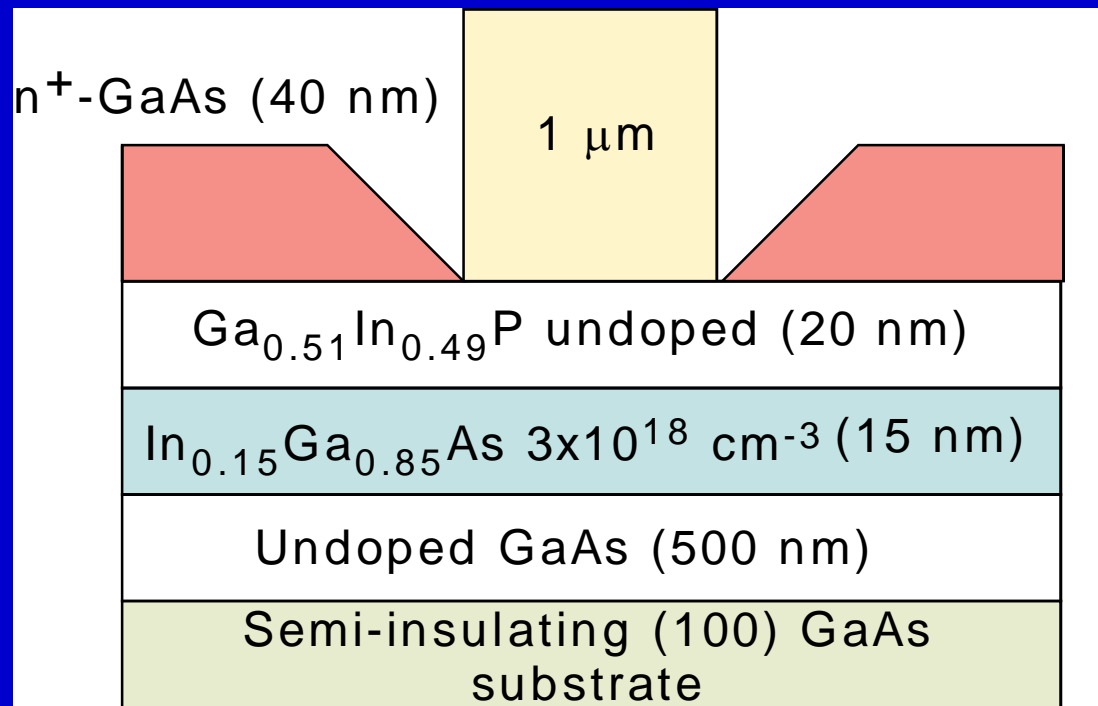
Liquid N temperature mobility 22,000  $\text{cm}^2/\text{V-s}$   
(for GaAs 16,000  $\text{cm}^2/\text{V-s}$ )

## MM-HEMT simulation

H. Happy, S. Bollaert, H. Foure, and A. Cappy,  
Numerical Analysis of Device Performance of  
Metamorphic  $\text{In}_y\text{Al}_{1-y}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}$  ( $0.3 < x < 0.6$ ) HEMT's on GaAs Substrate, IEEE Trans.  
Electron Dev., ED-45, No 10, p. 2089, October  
(1998)

Prediction:  $x = 0.4$  is optimum

# GaInP/InGaAs Doped Channel HFET



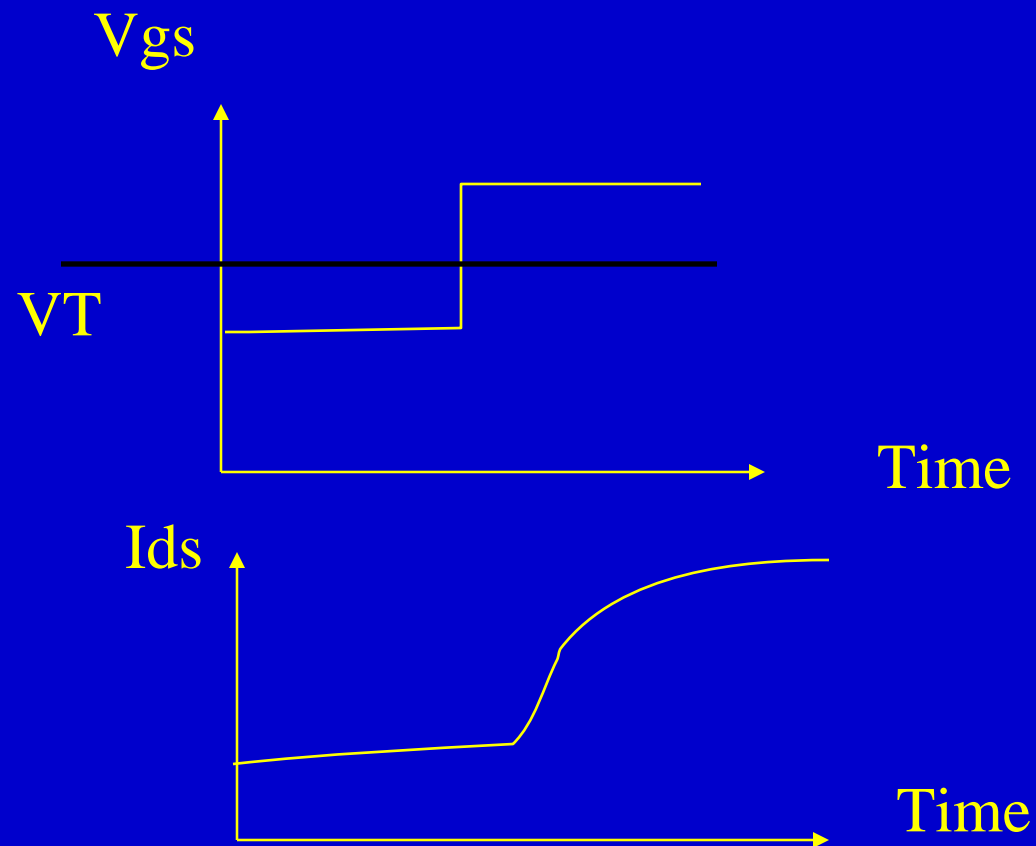
(After S.S. Lu, Y.W. Hsu, C.-C. Meng, and L. P. Chen, IEEE EDL, vol. 20, No 1, pp. 21-23)

# Problems with HEMTs

Gate lag

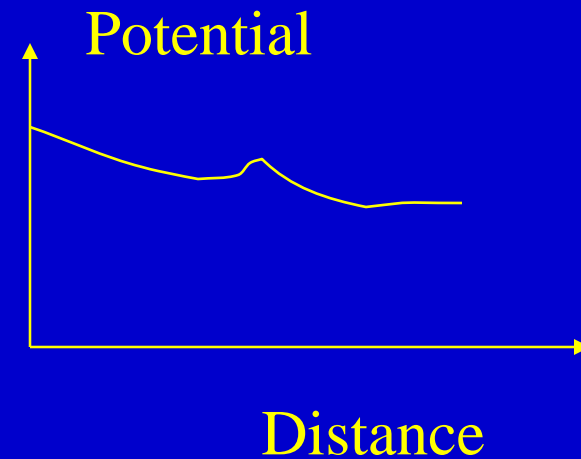
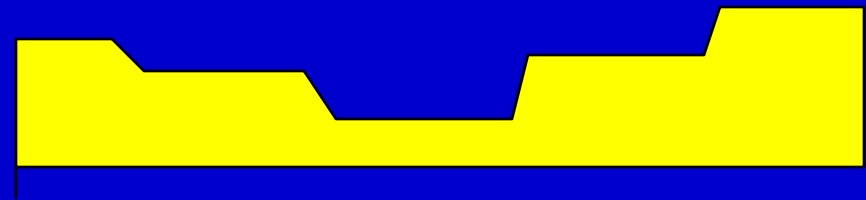
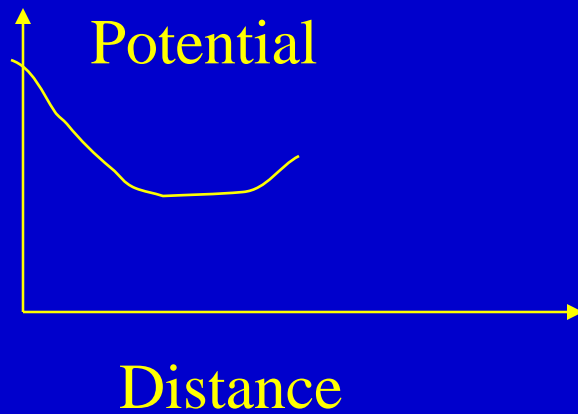
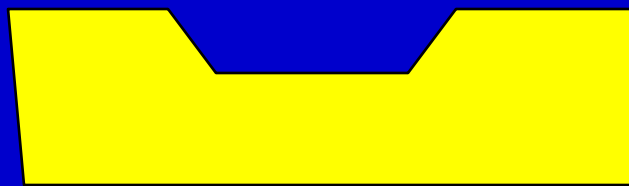
Gate breakdown

# Gate Lag Problem





# Double Recesses Gate



# MESFET, HFET, HBT Comparison

	MESFET	HFET	HBT
1/f noise	High	High	Lower
RF performance	OK	Very good	Good
Breakdown	OK	Low	High
Power level	Up to 1 W/mm	Up to 1 W/mm	Up to 3 W/mm
Price		Least expensive	