

A 5GHz pHEMT Transformer-Coupled VCO

Ping Wing Lai and Stephen I. Long

Dept. of Electrical and Computer Engineering, University of California Santa Barbara, CA 93106-9560
long@ece.ucsb.edu

Abstract:

A transformer-coupled technique is shown to be an area-efficient method for reducing oscillator phase noise. Higher signal amplitude and inductor Q can be achieved without breakdown. A pHEMT process was used to fabricate the 5GHz VCO. The measured phase noise at 3MHz offset frequency is -129 dBc/Hz. The VCO dissipates 9 mW.

1. Introduction

The requirement for low phase noise in integrated oscillators has been driven by wireless applications. In order to reduce the phase noise of the oscillator, a large signal amplitude in the resonant tank is needed, but the large voltage swing ($I_d R_p$) is constrained by breakdown mechanisms in the devices and the supply voltage. Phase noise can be reduced with the same resonator voltage swing by coupling several (N) identical oscillators [3-4] to each other, and the phase noise will be reduced by a factor of $1/N$ [5]. But the chip area will be increased in the same proportion. In [6], a transformer-based area-saving coupled oscillator was proposed. Two individual oscillators were coupled by a transformer with improvement in phase noise of 1-3 dB. In this paper, this approach has been extended to four oscillators. The benefits of transformer-coupled inductor resonators are clearly described and compared with single LC and series connected oscillators. Benefits in amplitude, resonator Q, self-resonant frequency (SRF), lead to a 12 dB theoretical improvement in phase noise. Tuning range is retained while breakdown can be avoided by reduction in R_p .

A commercial p-HEMT foundry process [9] was used to fabricate a 5 GHz VCO that employs 4 transformer coupled oscillators. Phase noise of -129 dBc/Hz was measured at a 3 MHz offset with a VDD of 2.5V and current of 3.6 mA.

2. Circuit Design

In a recent paper, it [1-2] states that Leeson's hypothesized equation

$$L(\omega_m) = \frac{4FkTR_p}{V_{rms}^2} \left(\frac{\omega_o}{2Q\omega_m} \right)^2 \quad (1)$$

holds, and the oscillator's noise factor F of a current-biased differential CMOS LC oscillator is

$$F = 1 + \frac{4\gamma I_d R_p}{\pi \sqrt{2} V_{rms}} + \gamma \frac{4}{9} g_{m_{bias}} R_p \quad (2)$$

where V_{rms} is the rms oscillation amplitude, I_d is the bias current, γ is the FET noise factor, R_p is the equivalent parallel resistance of the resonator and $g_{m_{bias}}$ is the gm of the FET current source. The first term in (2) is the noise contributed by R_p . The second term is the phase noise induced by differential pair thermal noise and is independent of the specifics of the transistors. The last term is the noise contributed by the current source. Equation (1) and (2) show that the relative contribution of the resonator loss is fixed. In the current-limited regime, where the FET current source remains in saturation, the oscillation amplitude V_{rms} is proportional to $I_d R_p$, so the differential pair contributes noise proportional to γ . The last term in equation (2) is proportional to gm of the current source. The same equation can be applied to a pHEMT LC oscillator with a different γ [7].

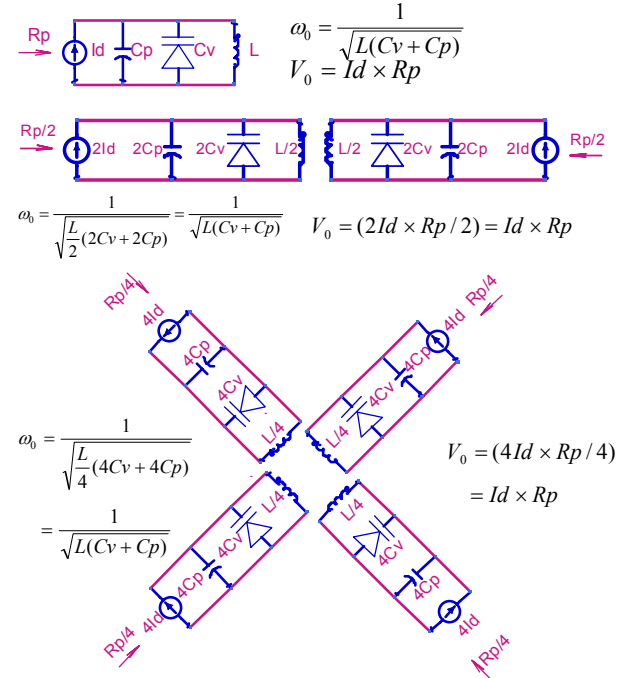


Figure 1 Circuit transformation from simple inductor into 1:1 transformer [6] (the center one), into 1:1:1:1 transformer (the bottom one)

In [7], it is shown that phase noise can be reduced by increasing current, I_d , if R_p is reduced while $I_d R_p$ is kept constant. It is because the noise factor as

shown in equation (2) will not change if $I_d R_p$ is kept constant. One way to reduce the R_p while keeping $I_d R_p$ constant is to divide a simple inductor into several coupled inductors, a transformer. The idea is shown in Figure 1. In this example, inductance and R_p are reduced by a factor of 4. Therefore, the current in each oscillator can also be increased by 4 times without exceeding breakdown. The improvement in phase noise by this mechanism can be deduced to be

$$L(\omega_m) \propto \frac{1}{I_{bias}^2 R_p Q^2} \quad (3)$$

reduced by 6dB for the same voltage swing. In addition, now 4 oscillators are coupled together, so the net phase noise will be further reduced by $\frac{1}{4} = 6\text{dB}$ [5], thus the total reduction will be 12dB. But 16 times more power is consumed than a single LC resonator oscillator.

Also, the tuning range of the transformer coupled VCO is the same as a normal LC VCO, since four times larger current is drawn, four times larger parasitic capacitance is introduced by the four times larger differential pair, but the resonator will only consist of $\frac{1}{4}$ of the total inductance due to the 1:1:1:1 transformer.

The physical transformation from simple inductor into coupled inductor is shown in figure 2. The transformer is layed out in such a way that each coupled inductor will be geometrically symmetric. Moreover, since identical varactor and differential pair transistors are used at each coupled inductor, the tuning capacitance from the varactor and the parasitic capacitance from the transistor are equally distributed in each resonant tank. Therefore, the current distribution through each coupled inductor will be the same, so the mutual inductance among the coupled inductors is maximized to obtain highest Q.

An eight turn octagonal coupled inductor is shown in Figure 2. An extra outer loop is used to couple the signal out from the oscillator to the buffer. The size of the transformer is $640 \times 640 \text{ um}^2$. The transformer is simulated in the Agilent Momentum EM simulator. The definition of Q and inductance of the transformer has been determined when it is parallel resonated with an ideal capacitor. The resulting Q of this parallel resonant circuit can be extracted from the phase stability [8].

$$Q = \frac{\omega_o}{2} \left| \frac{d\theta}{d\omega} \right|_{\omega=\omega_o} \quad (4)$$

The resulting inductance can be extracted at low resonant frequency. In order to calculate a Q versus frequency characteristic for the coupled inductor, four ideal capacitances were added in parallel with the four coupled inductors and were swept in value to achieve a range of resonant frequencies. The Q of a simple eight turn octagonal inductor and coupled inductor are compared in Figure 3. The inductance of each coupled inductor is simulated to be 5.4nH.

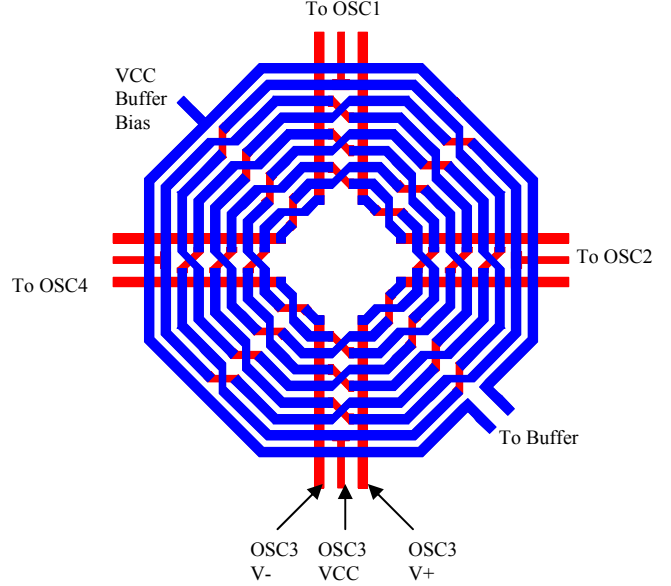


Figure 2 Layout of the coupled inductor

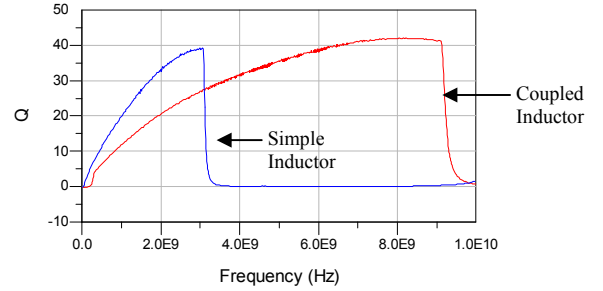


Figure 3 Q value of the simple inductor and coupled inductor

From Figure 3, the self resonant frequency (SRF) of a simple eight turn inductor is 3GHz, but the eight turn coupled inductor of Fig. 2 is around 9GHz, a 3 times improvement. The increase in SRF is because the total parasitic capacitance of the whole inductor is shared among four coupled inductors. Therefore, a larger inductor can be used for the oscillator thereby providing higher Q. Or, a higher frequency oscillator can be achieved because of the higher SRF. If thick metal is available for both metal layers, the Q of the simple and coupled inductors are quite close at low frequencies and the peak Q of the coupled inductor exceeds 50.

	LC	Series 2X	Transformer-coupled 4X
Voltage swing	1x	1x	1x
Tuning range	1x	1x	1x
Supply voltage	1x	1x	1x
Current bias	1x	2x	16x
Chip Area	1x	2x	1x
Phase noise	0dB	-3dB	-12dB

Table 1. Comparison of series-coupled and transformer coupled oscillators with simple LC oscillator.

A series-coupled 2X oscillator [3-4] and a transformer-based 4X coupled oscillator are compared to a basic LC oscillator in Table 1.

The pHEMT VCO consists of 4 differential cross-coupled oscillators as shown in Fig. 4 coupled together by a 1:1:1:1 transformer. The outer turn of the transformer is connected to the buffer circuit fig. 5. The negative Gm cell of the individual oscillator is made by a pair of cross coupled pHEMT transistors. Two varactor arrays are connected back-to-back for frequency tuning. The varactor diode consists of the gate to drain and source diode of the pHEMT transistor. By paralleling minimum size pHEMT varactors together, a higher Q is obtained by reducing series resistance. In order to reduce the 1/f noise up-converted into the carrier, a resistor is used as a current source and a capacitor is connected in parallel with the resistor to suppress the high frequency white noise from the resistor. A common collector stage is used as a buffer to minimize the loading on the VCO. This buffer can directly drive the off-chip 50ohm load.

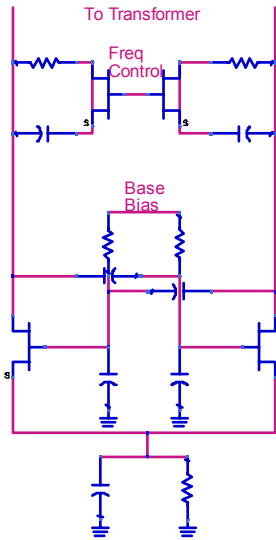


Figure 4 VCO Circuit diagram

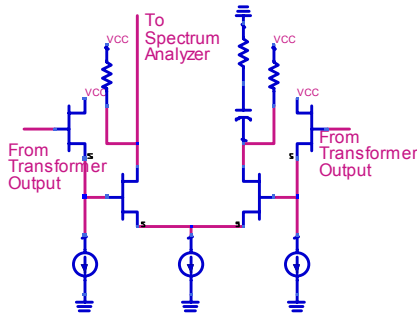


Figure 5 Buffer Circuit diagram

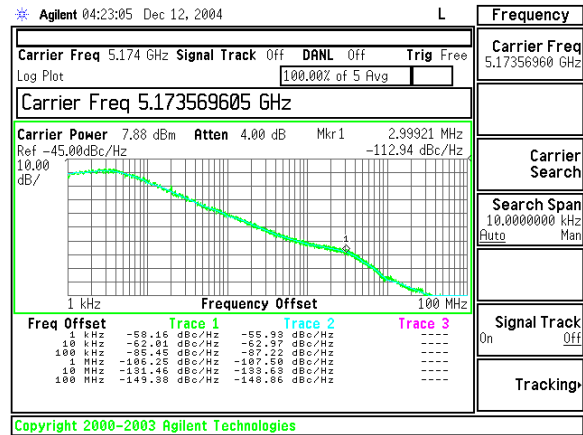
3. Measurement Results

The circuit is fabricated in a 0.13 μm pHEMT process from Triquint Semiconductor [9]. The process provides a semi-insulating substrate and one thick metal

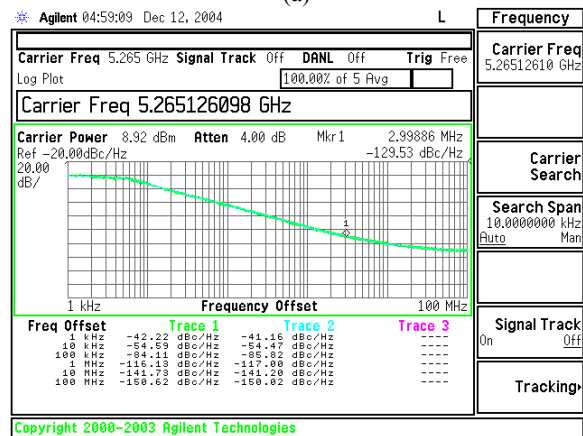
layer. An Agilent E4440A spectrum analyzer with phase noise option is used to measure the phase noise of the oscillator. The phase noise plots are shown in Fig. 6. With the pHEMT devices, the phase noise is dominated by 1/f noise beyond a 1 MHz offset frequency. Fig. 7 shows the frequency dependence on control voltage yielding a tuning range from 5135 to 5260 MHz with 2.5V supply voltage. The variation of phase noise under different control voltages across the tuning range is shown in Fig. 8. The die photo in Fig. 9 shows that the VCO area is 1.5mm x 1.3mm. A summary of the performance is given in Table 2. Note that power dissipation is only 9 mW even with four oscillators.

VDD (V)	2.5
Core current bias (mA)	3.6
Tuning range (MHz)	5135-5260
Phase noise @1MHz (dBc/Hz)	-117
Phase noise @3MHz (dBc/Hz)	-129.5

Table 2 Summary of Measured VCO Performance



(a)



(b)

Figure 6 Measured phase noise at different tuning voltage (a) 2.5V, (b) 0V

A commonly accepted quantity used for comparing various oscillators is the figure of merit (FOM) that is defined as below

$$FOM = 10 \log \left[\left(\frac{f_o}{f_{off}} \right)^2 \frac{1}{P} \right] - L(f_{off}) \text{ dB} \quad (4)$$

where P is the power dissipation of the oscillator in milliwatts, f_o is the center frequency, f_{off} is the frequency offset from the center, and $L(f_{off})$ is the phase noise measured at f_{off} offset frequency. It is shown that our oscillators have a FOM of 185 dB at 3MHz offset.

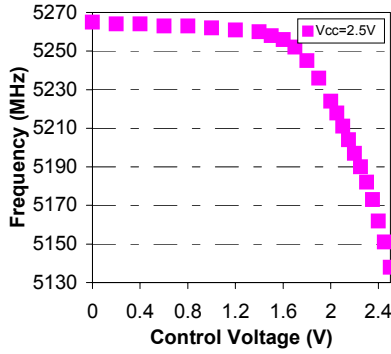


Figure 7 Frequency versus control voltage

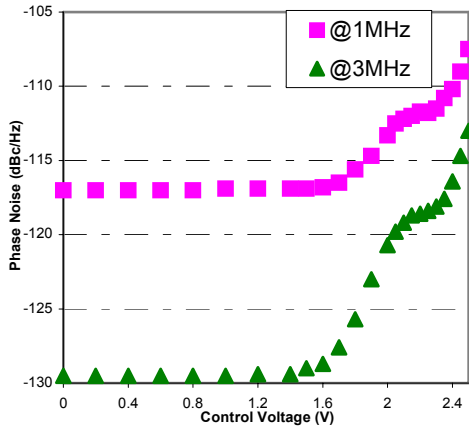


Figure 8 Phase noise at 1 & 3MHz offset versus control voltage

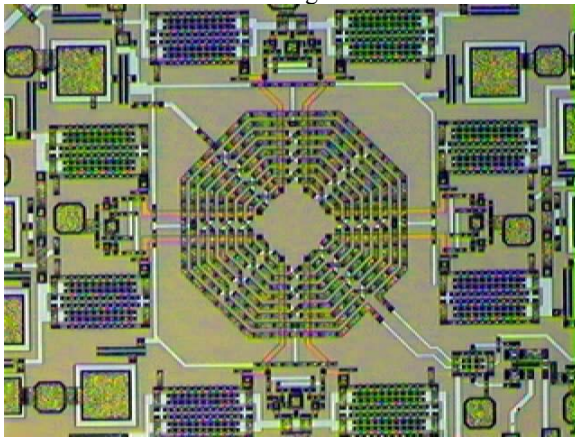


Figure 9 Die photo

4. Conclusion

One of the most efficient methods of reducing phase noise is to increase the signal amplitude in the resonator. However, the maximum resonator signal

amplitude is limited by breakdown mechanisms in the devices and supply voltage. A transformer coupled oscillator is introduced to allow a higher current swing in the tank in order to reduce the phase noise without increasing area. Close coupling and current balance enhances the Q and increases self resonance for the coupled case. A figure of merit of 185 dB was obtained for a 5 GHz pHEMT VCO.

5. Acknowledgment

The authors gratefully acknowledge the fabrication support of Triquint Semiconductor, Hillsboro, OR. The authors would also like to thank Prof. Robert York and Chris Sanabria for their support in testing and Vikas Manan for helpful discussions

6. References.

- [1] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential LC oscillator," in Proc. CICC 2000, pp.569-572
- [2] E. Hegazi, H. Sjöland and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise", IEEE JSSC, Vol.36, No.12, Dec 2001, pp.1921-1930
- [3] T. Liu, "1.5V 10-12.5GHz Integrated CMOS oscillators," IEEE Symposium on VLSI Circuits 1999, pp. 55-56
- [4] S. Gierkink, "A Low-Phase-Noise 5-GHz CMOS Quadrature VCO Using Superharmonic Coupling," IEEE JSSC, Vol.38, No.7, Jul 2003, pp.1148-1154
- [5] H. Chang, X. Cao, U. K. Mishra, R. A. York, "Phase noise in coupled oscillators theory and experiment", IEEE Trans. MTT, Vol 45, No 5, May 1997, pp. 604-615
- [6] H. Jacobsson, et al. "Very Low Phase-Noise Fully-integrated Coupled VCOs," IEEE RFIC symposium 2002, pp. 467-470
- [7] P. Lai, L. Dobos, S. Long, "A 2.4GHz SiGe Low Phase-Noise VCO Using On Chip Tapped inductor," IEEE ESSCIRC 2003, pp.
- [8] O. Kenneth, "Estimation Methods for Quality Factors of Inductors Fabricated in Silicon Integrated Circuit Process Technologies", IEEE JSSC, Vol. 33, No. 8, Aug. 1998
- [9] Triquint Semiconductor, TQP13 process, Hillsboro, OR.