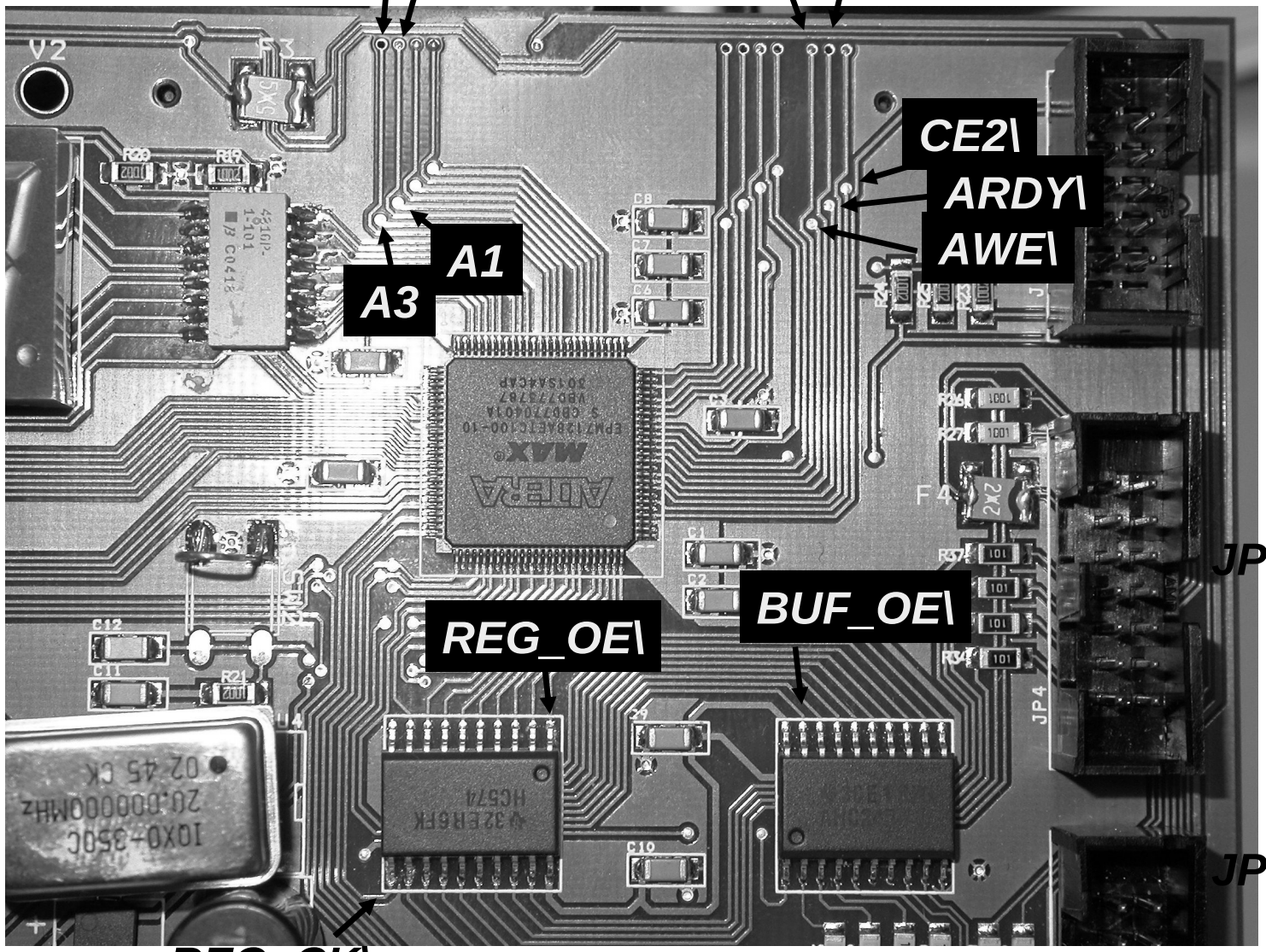
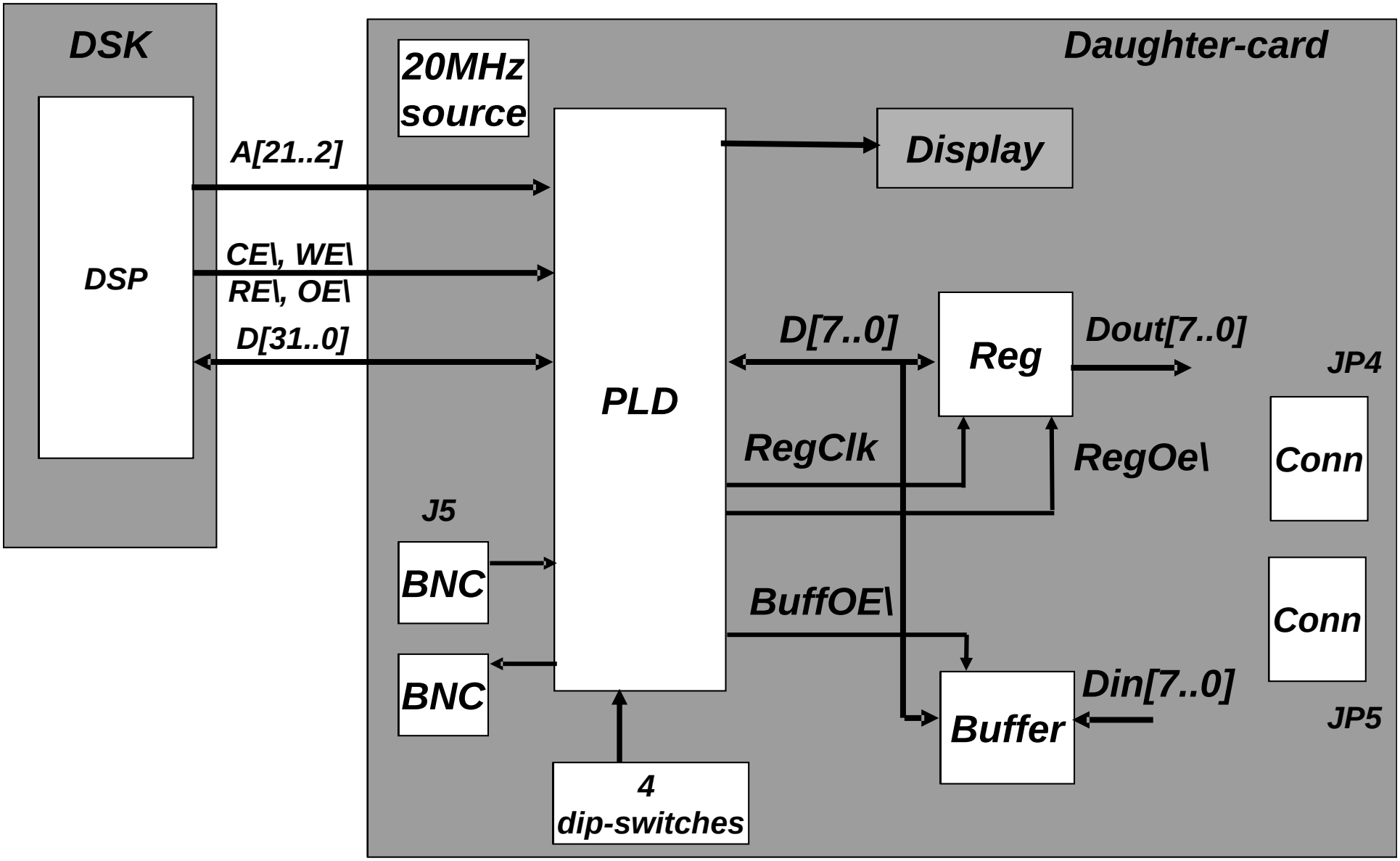
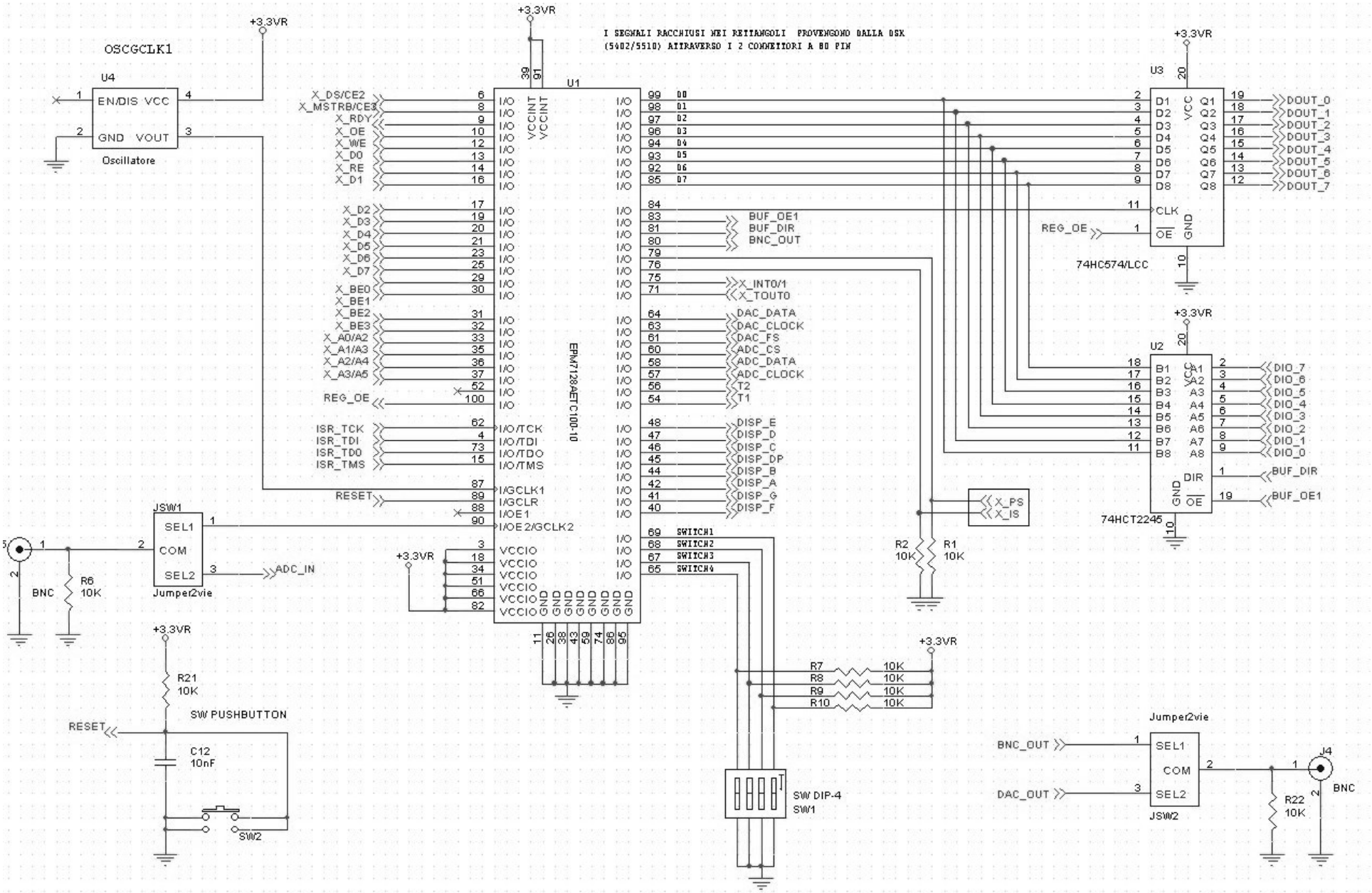
Daughter card: test points



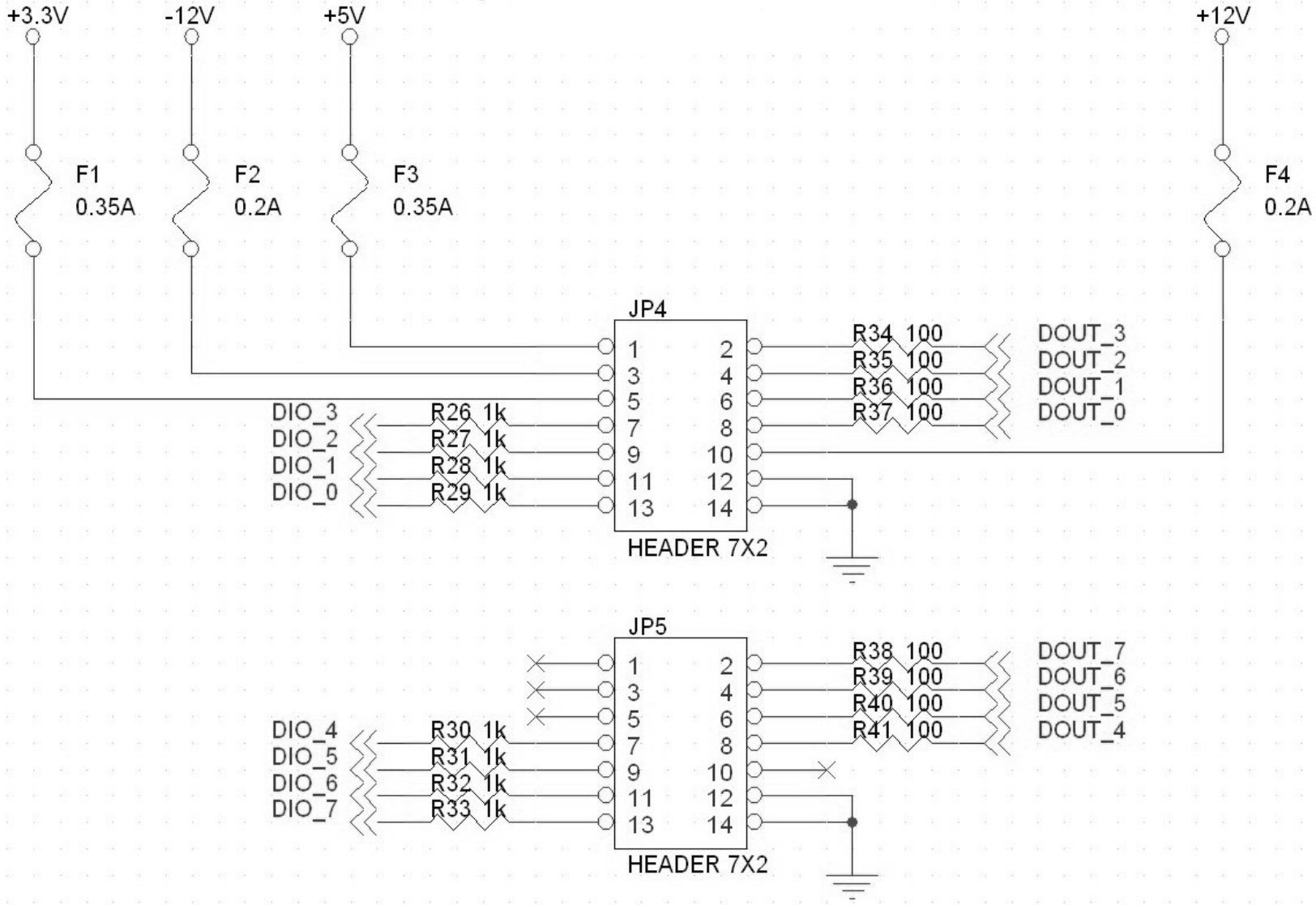
Daughter card: Schema a blocchi



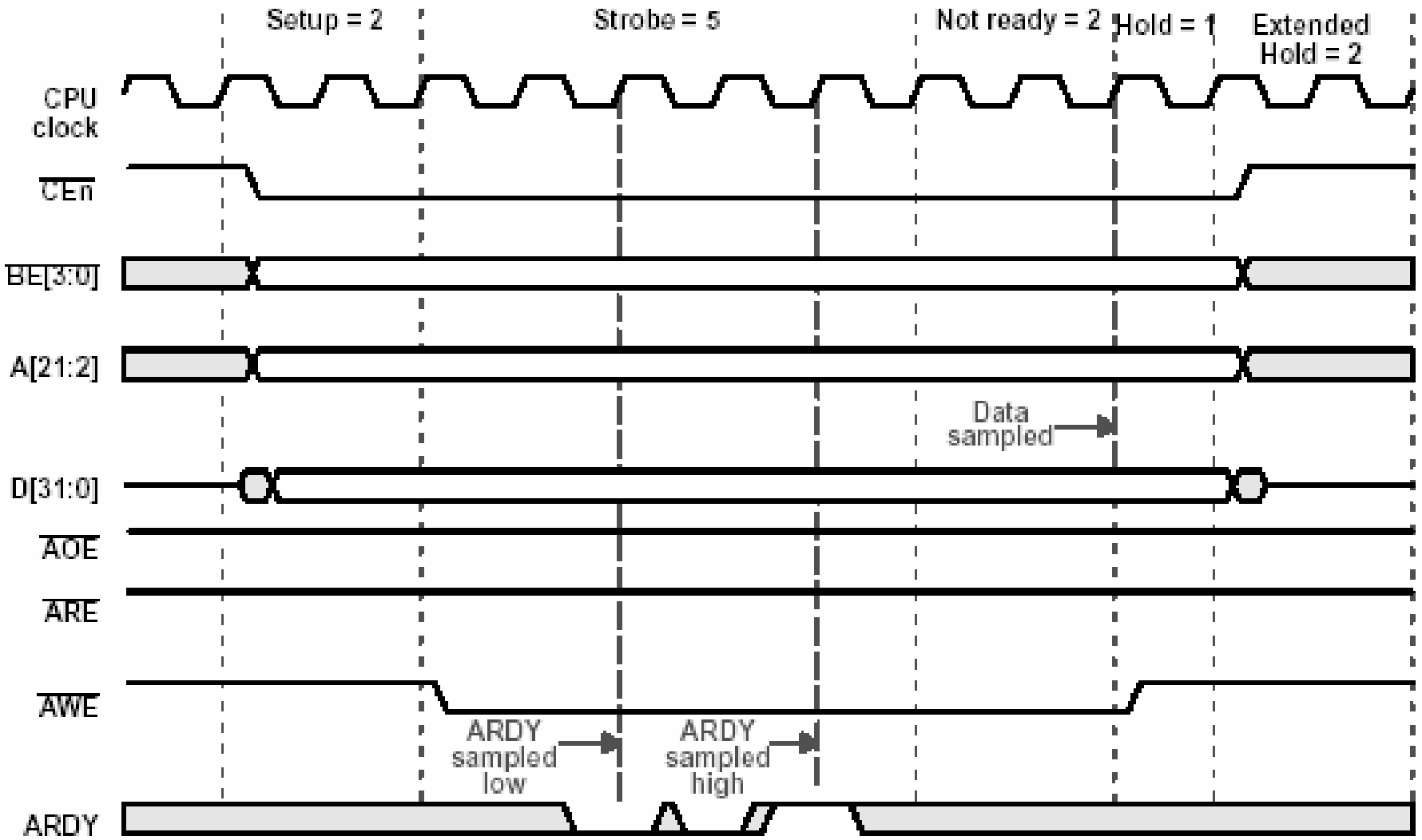
Daughter card: Schema elettrico #1



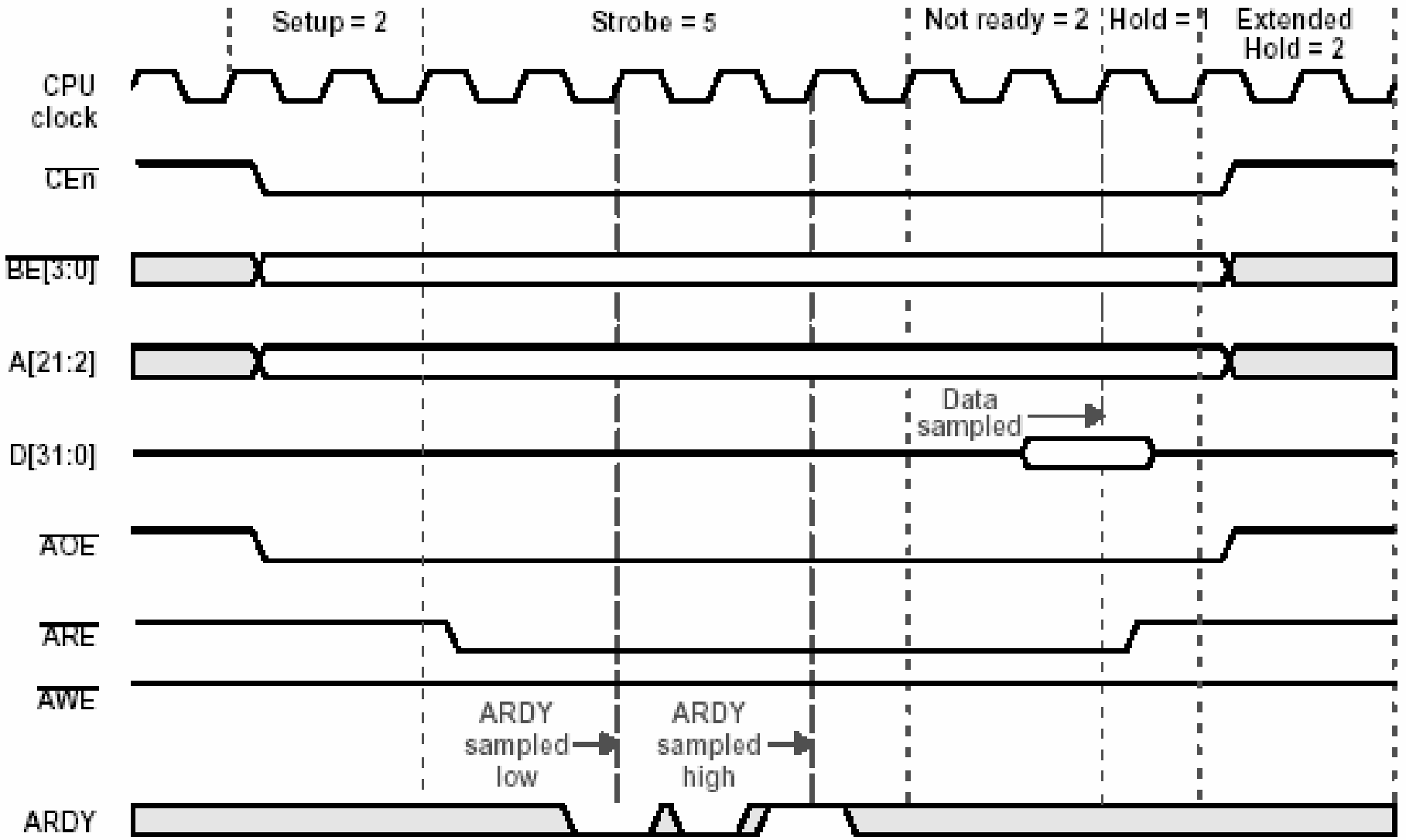
Daughter card: schema elettrico #2



CPU timings - write

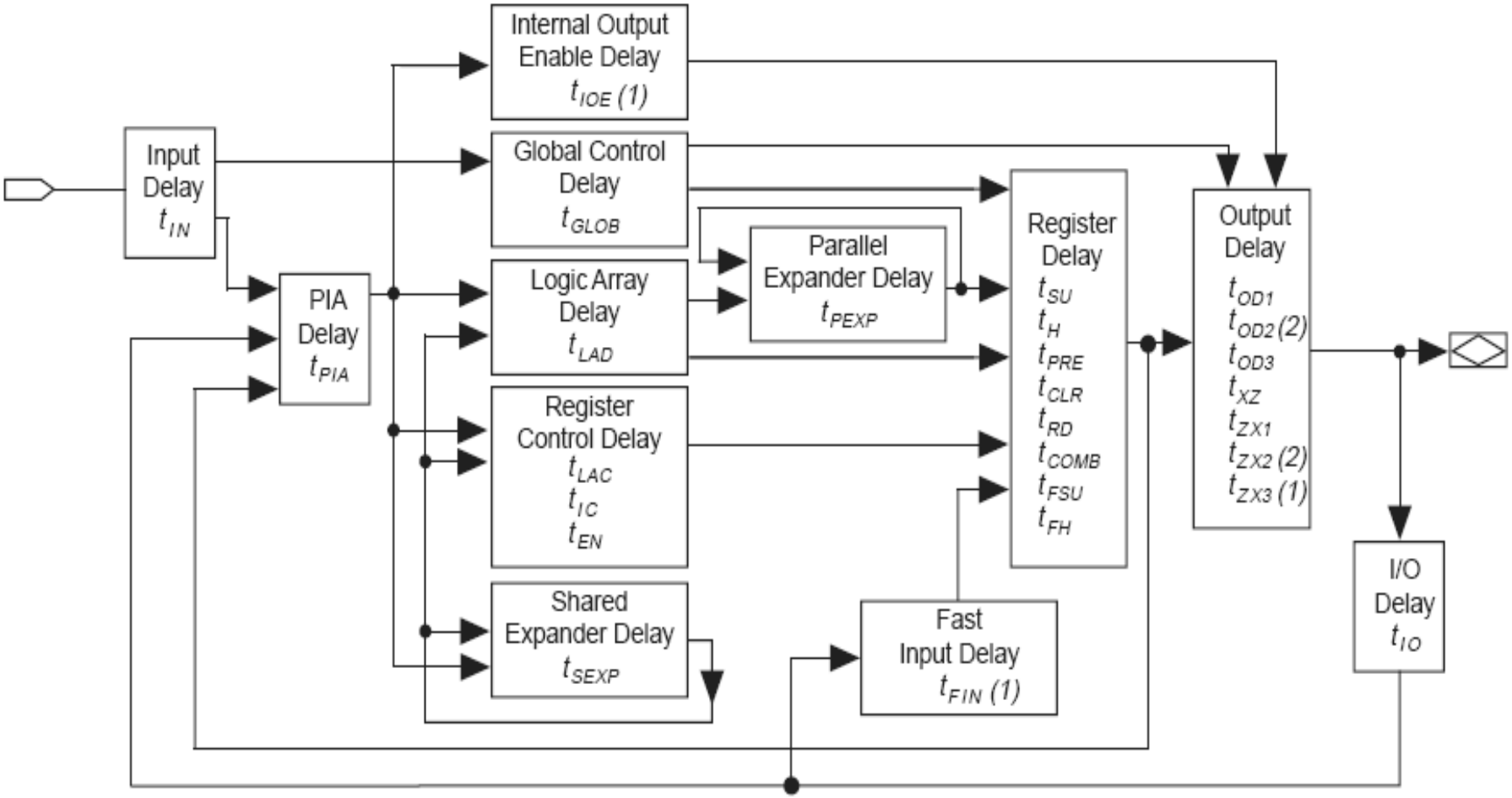


CPU timings - read

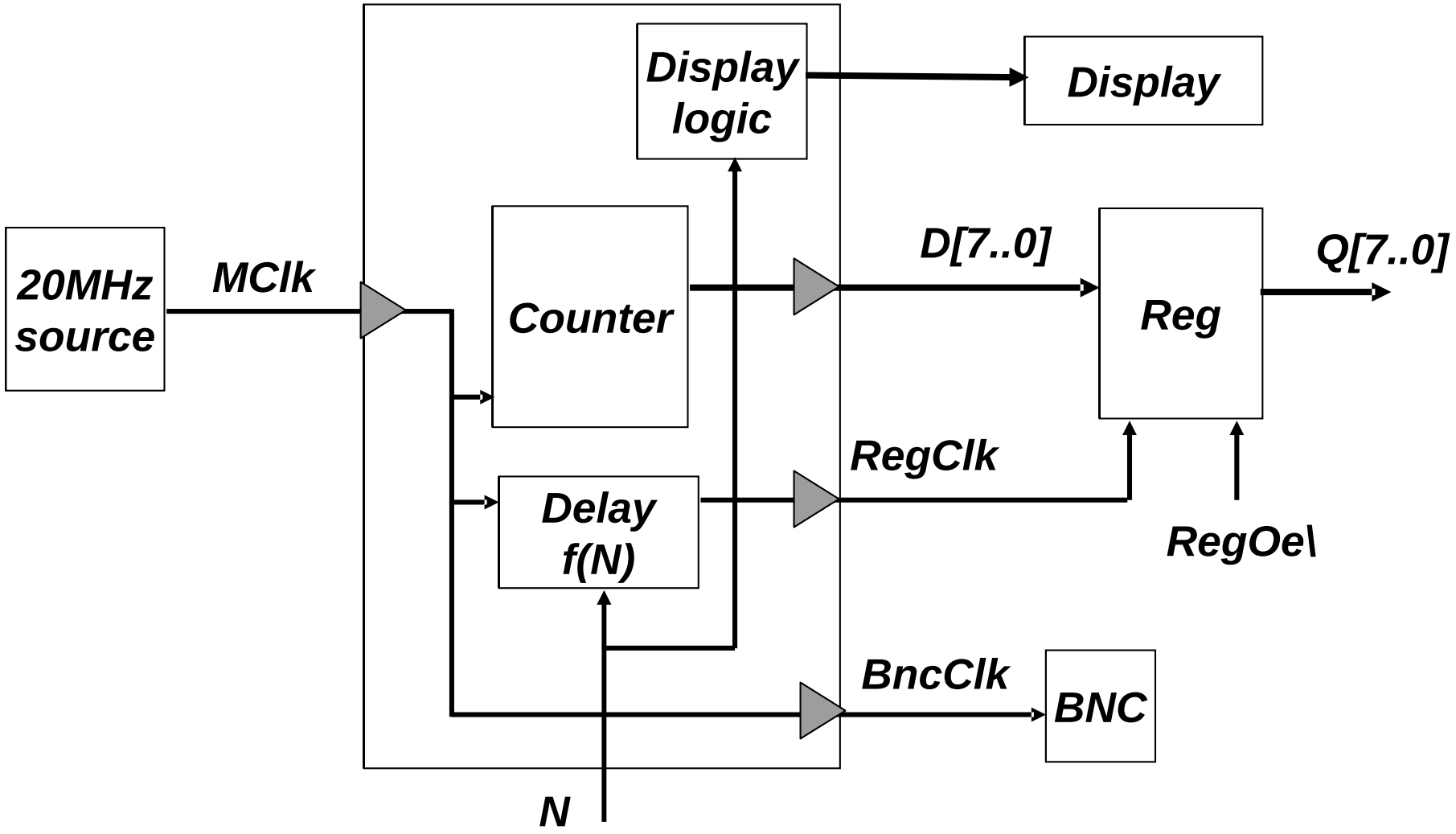


PLD: timing model

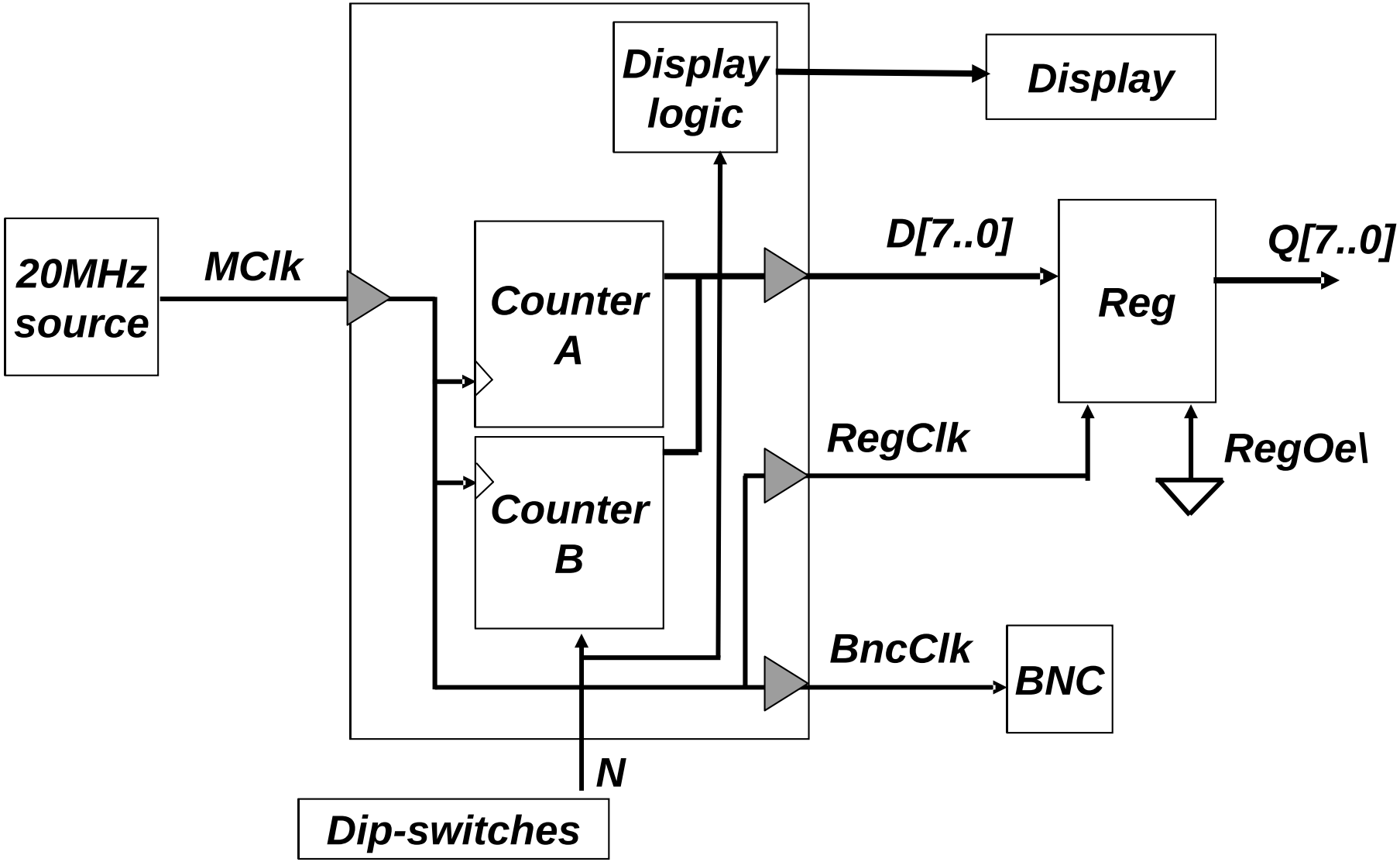
Figure 12. MAX 7000 Timing Model



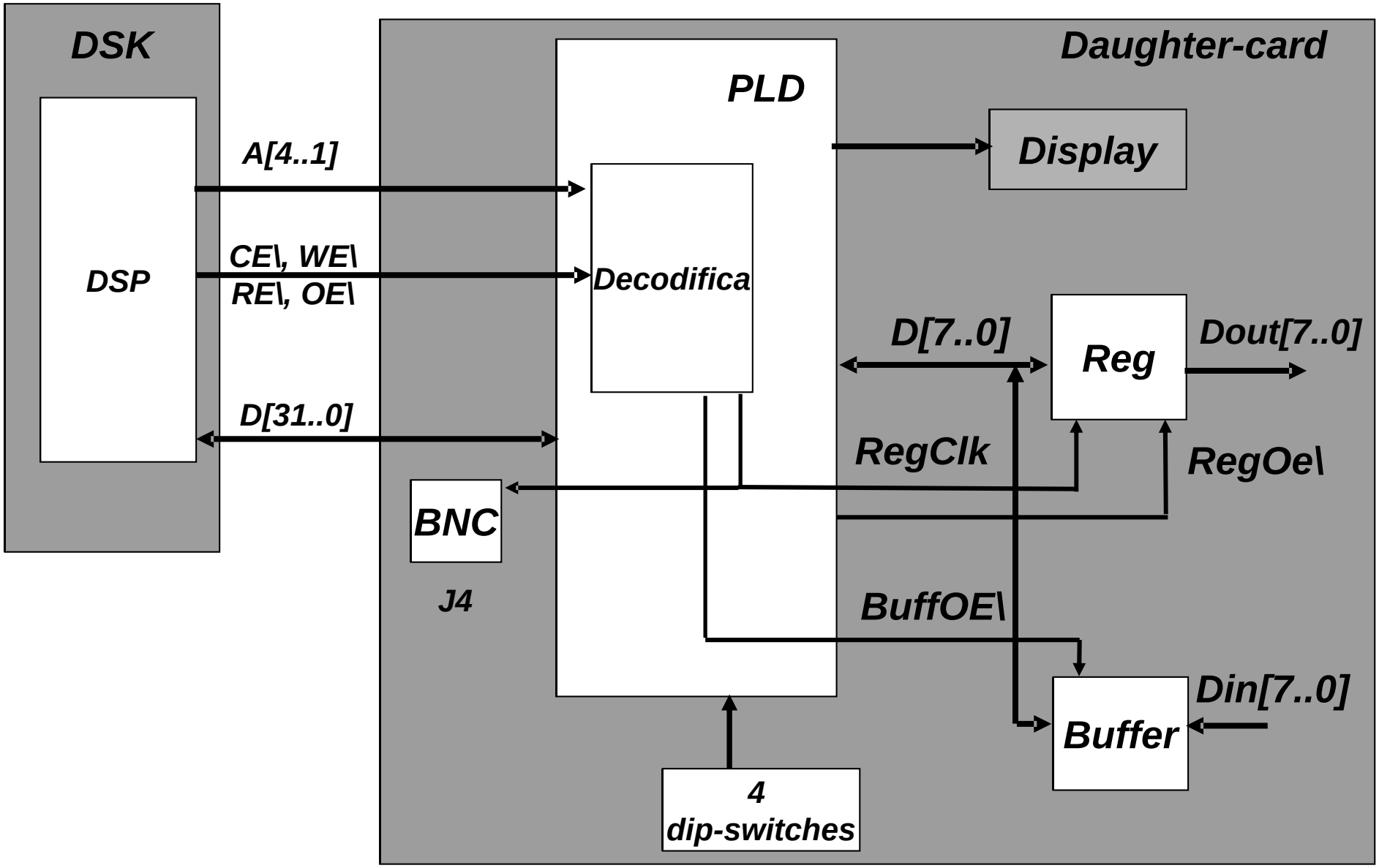
Schema esercitazione 8/3/07



Schema esercitazione 15/3/07



Schema esercitazione 23/3/07



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