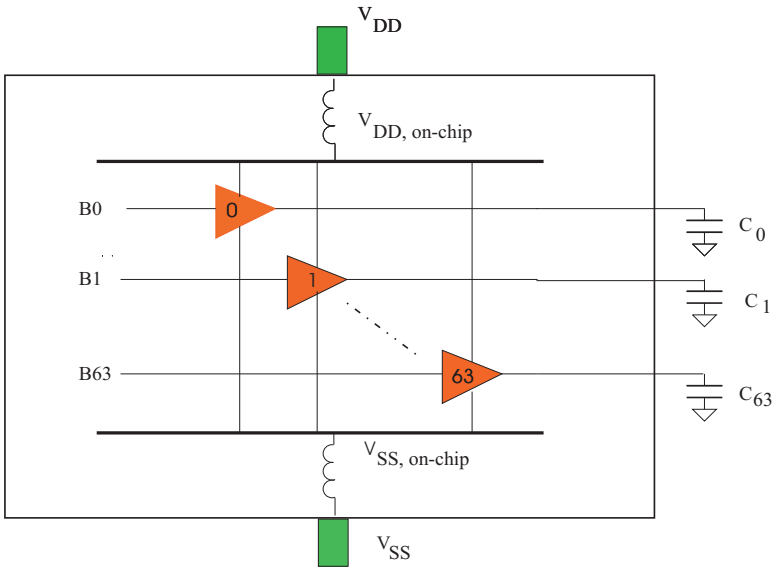
ELE863/EE8501 VLSI Systems

Simultaneous Switching Noise (SSN)



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Preface

▷ This chapter deals with simultaneous switching noise (SSN). The reduction of SSN is critical for mixed-mode circuits. In this chapter, we investigate the sources of SSN and the effect of SSN. Techniques that reduce the effect of SSN are examined in detail. The design criteria for SSN are studied. The grounding schemes of analog and digital circuits are investigated.

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OUTLINE

- **Simultaneous Switching Noise (SSN)**
- **Effect of SSN**
- **Analysis of SSN**
- **SSN Reduction Techniques**
- **Design Criteria for SSN**
- **Analog and Digital Grounding**

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SSN

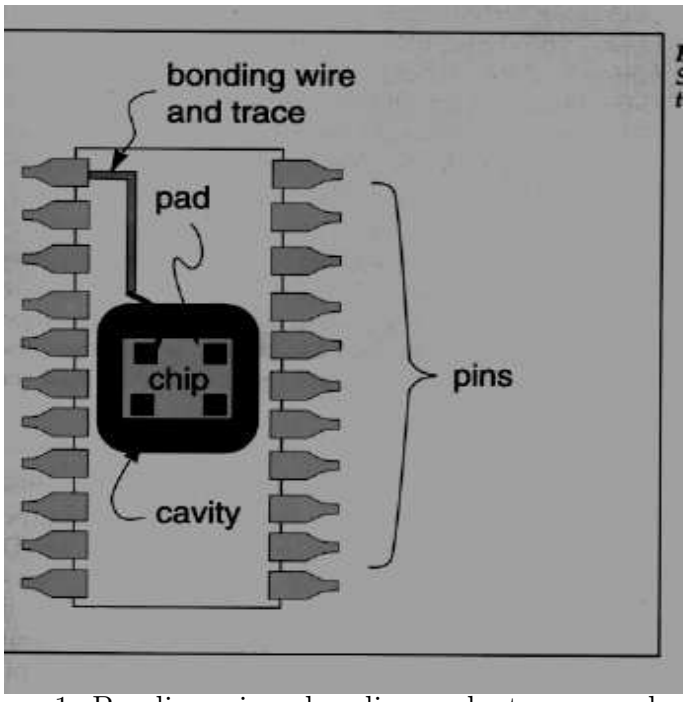

Figure 1: Bonding wires, bonding pads, traces, and pins.

- ▷ Bonding wires, bonding pads, traces, and pins form the interface path between circuits on the chip and circuits on boards.

- ▷ The resistance, capacitance, and inductance of the interface paths largely determine the performance of systems.

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SSN (cont'd)

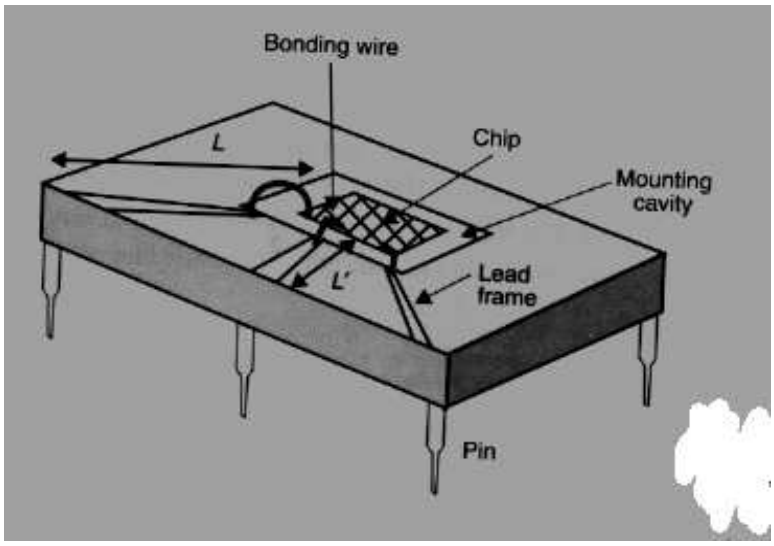

Figure 2: Bonding wires, bonding pads, traces, and pins.

- ▷ Bonding wires at the corners are the longest - These wires have the largest resistance and inductance.

- ▷ The use of the bonding pads at the corners and the bonding wires connected to these pads should be avoided.

- ▷ The design rules of most CMOS technologies typically prohibit the use of the bonding pads at the corners. These pads should be used as "dummy", i.e. no electrical connections to these pads.

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SSN (cont'd)

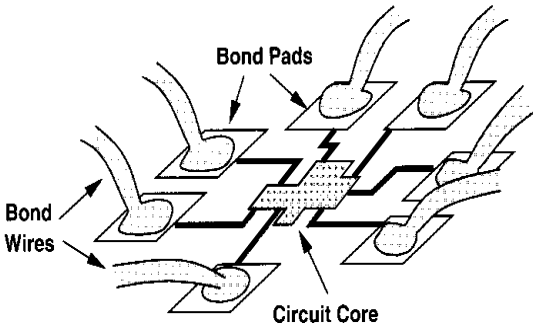

Figure 3: Bond pads and bond wires.

• Bond Pads

- ▷ Bond pads are on-chip metal rectangles large enough to be soldered to leads, typically 70x70 μm^2 - 100x100 μm^2.
- ▷ Each pad is typically formed by the two top-most metal layers connected to each other by many vias on the perimeter in order to avoid the *lift-off* of the top metal layer during bonding.
- ▷ Some CMOS processes require that all metal layers to be connected together for bond pads. Because the top metal layer has a smaller capacitance to the substrate as compared with the bottom metal layer, connecting all bond-pad metal layers together will dramatically increase the capacitance of the pad to the substrate.
- ▷ Do not lay pads at the corners of the chip. Add dummy pads at the corners instead.

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SSN (cont'd)

▷ The capacitance of bond pads consists of two components : (i) the area capacitance and (ii) the fringe capacitance

$$C_{Pad} \approx \epsilon_{ox} \left[1.15 \frac{A}{H} + 2.8 \left(\frac{T}{H} \right)^{0.222} P \right], \tag{1}$$

where A=pad area, P=pad periphery, H=height of pad above conductive silicon substrate, T=thickness of pad, ϵ_{ox}=dielectric constant of silicon dioxide. The first term gives the area capacitance whereas the second term quantifies the fringe capacitance (Ref. T. Sakurai and K. Tamaru, "Simple formulas for two- and three-dimensional capacitances," *IEEE Trans. Electron Devices*, Vol.30, No. 2, pp.183-185, Feb. 1983.)

▷ H increases $\longrightarrow$ C_{pad} decreases. For high-speed applications, only the top metal layers, such as top two metal layers, should be used for signal pads. For V_{DD} and V_{DD} pads, all metal layers can be connected together to form pads.

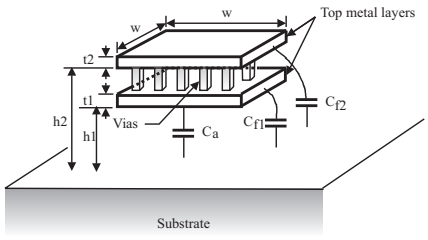

Figure 4: Bonding pads are formed by topmost metal layers.

▷ Typically $C_{pad} = 0.2 - 0.4$ pF for a $100 \times 100 \mu m$ pad.

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SSN (cont'd)

• Inductance of Package

▷ Self-Inductance:

$$L_{ij} = \frac{\psi_{ij}}{I_j} = \frac{\int\int \mathbf{B}_{ij} \bullet d\mathbf{s}_{ij}}{I_j}, \tag{2}$$

ψ_{ij} and $\mathbf{B}_{ij}$ are the flux and intensity of the magnetic field that is generated by I_j and passes through loop i. L_{jj}, is called the self-inductance quantifying the relation between the magnetic flux of loop j and the current of loop j, L_{ij}, $i \neq j$ is called mutual inductance.

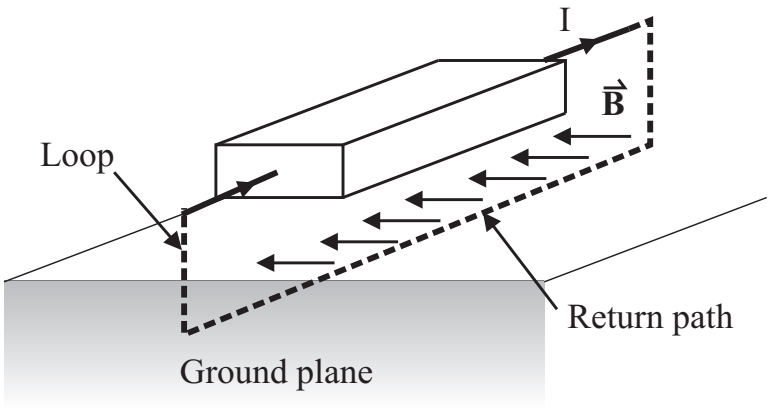

Figure 5: Self-inductance definition.

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SSN (cont'd)

• Inductance of Package (cont'd)

▷ Self inductance of a round bond wire

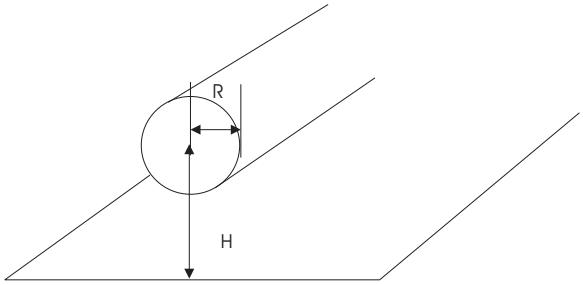

Figure 6: Self-inductance of a round wire.

$$L \approx \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2H}{R}\right) - 0.75\right], \tag{3}$$

where L=inductance per unit length, R=radius of the conductor, H distance from the conductive substrate, and μ_o=permittivity of free space. Typically, $L \approx$1nH/mm for bond wires. (Ref. T. Lee, *The Design of COS Radio-Frequency Integrated Circuits*, 2nd ed., Cambridge University Press, 2004).

▷ Self-Inductance of a rectangular trace

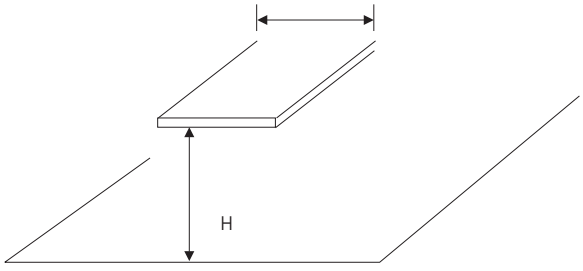

Figure 7: Self-inductance of a rectangular trace.

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$$L \approx \frac{1.6}{K_f}\left[\frac{H}{W}\right], \tag{4}$$

where L= inductance per unit length, $K_f \approx 0.72(\frac{H}{W}) + 1$ (fringe factor), W=width of the trace and H=distance from the trace to the conductive substrate.

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SSN (cont'd)

▷ Mutual Inductance of two round wires of equal length

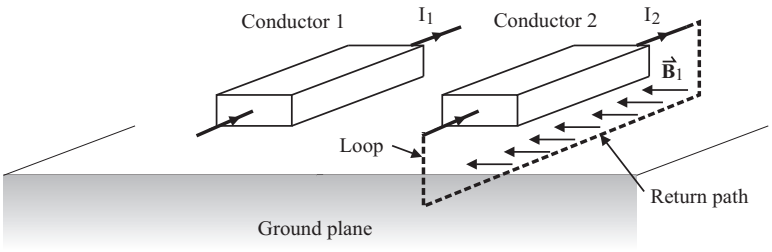

Figure 8: Mutual-inductance definition.

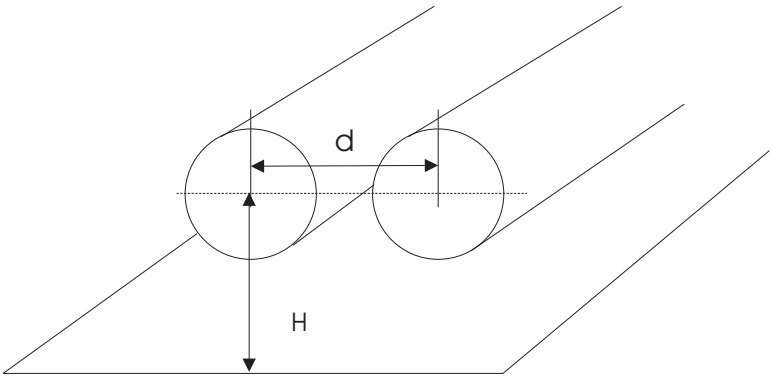

Figure 9: Mutual-inductance of two round wires.

▷

$$M = \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right], \tag{5}$$

where L=inductance per unit length, l=length of bond wires, d=distance between bond wires

▷ For 10-mm length and 1-mm spacing, $M \approx 4$ nH. Since $L \approx 10$ nH, the coupling coefficient is 40% approximately.

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SSN (cont'd)

• The Max. Frequency of Interfaces

▷ The capacitance of band pads and the inductance of bond wires form a 2nd-order low-pass. The upper limit of I/O frequency is set by the cutoff frequency of the low-pass. From

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1}{s^2 L_{wire} C_{total} + 1}, \tag{6}$$

where V_{in} and V_o are the voltage at the pin and the pad of the interface, respectively, we have

$$\omega_{-6dB} = \frac{1}{\sqrt{L_{wire} C_{total}}}, \tag{7}$$

where $C_{total} = C_{pad} + C_{pkg}$.

▷ When choosing packages, the highest design frequency of your design must not exceed the cutoff frequency of the I/O package.

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SSN (cont'd)

• Lumped Model of Bond Wires

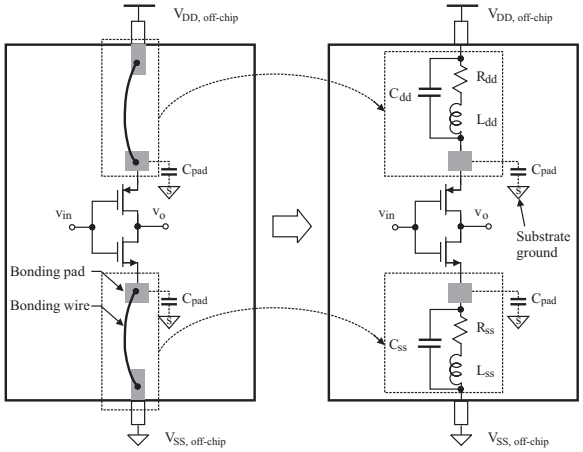

Figure 10: Lumped model of bond wires.

▷ R_{ss}=series resistance of bonding wires, L_{ss}=self and mutual inductances of bonding wires, C_{ss}=package capacitance.

▷ Bond wires are mainly inductive at high frequencies. Typical $L_{ss} \geq$5nH, and are usually modeled as an inductor.

▷ If a high-frequency current flows through a bonding wire, a voltage drop across the bonding wire quantified by $V_L(t) = L_{ss}\dfrac{di(t)}{dt}$ is generated.

▷ This voltage drop affects on-chip V_{DD} and V_{ss} for V_{DD} and V_{ss} pads and on-chip signals for signal pads.

SSN (cont'd)

• Output Buffers

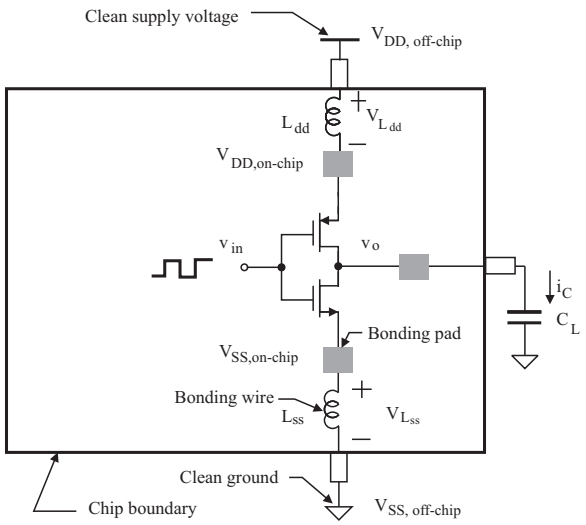

Figure 11: On-chip V_{DD} & V_{ss} fluctuate due to switching noise.

▷ Load capacitance of the inverter includes (1) Output capacitance of output buffer, (2) Capacitance of bond pads, (3) Capacitance of package, and (4) Capacitance of off-chip printed-circuit-board (PCB) traces.

▷ Off-chip capacitances are typically much larger than on-chip capacitances.

▷ To meet timing constraints, large output buffers (wide inverters) are needed to drive off-chip capacitive loads.

$W/L\uparrow \longrightarrow R_{on}\downarrow \longrightarrow \tau\downarrow$.

$W/L\uparrow \longrightarrow C_{out}\uparrow \longrightarrow C_L\uparrow$.

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SSN (cont'd)

- **Output Buffers (cont'd)**

  ▷ The load capacitance is typically $1 \sim 30$ pF. Typical size of output buffers $500 \sim 1000\mu m$.

  ▷ The size of inverter should be increased by a factor of $e = 2.71828$. The optimal number of inverters is such that the input capacitance of the last inverter should be $1/e$ that of the load capacitance (Ref. C. Mead and L. Conway, *Introduction to VLSI systems*, Addison-Wesley, 1980).

  ▷ Typical ratio of $4 \sim 5$ is used in sizing output buffers in order to save silicon area.

  ▷ Static inverter-based output buffers can be used for clock speed up to a few hundred MHz. These output buffers can not be used for very high-speed clock speeds.

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SSN (cont'd)

• Charging/discharging Currents of Output Buffers

▷ Large charging/discharging current spikes

1) C_L is large, because $i_C(t) = C_L \frac{v_C(t)}{dt} \longrightarrow i_C(t)$ is large.

2) Sharp rising/falling edges $\longrightarrow \frac{v_C(t)}{dt}$ is large $\longrightarrow i_C(t)$ is large.

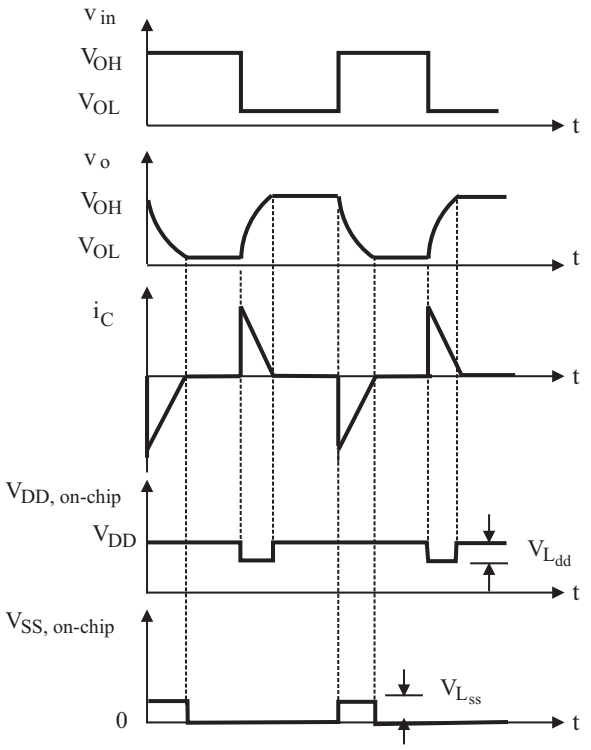

Figure 12: Large charging/discharging current spikes and the fluctuation of on-chip V_{DD} and V_{ss}.

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SSN (cont'd)

- **Switching Noise**

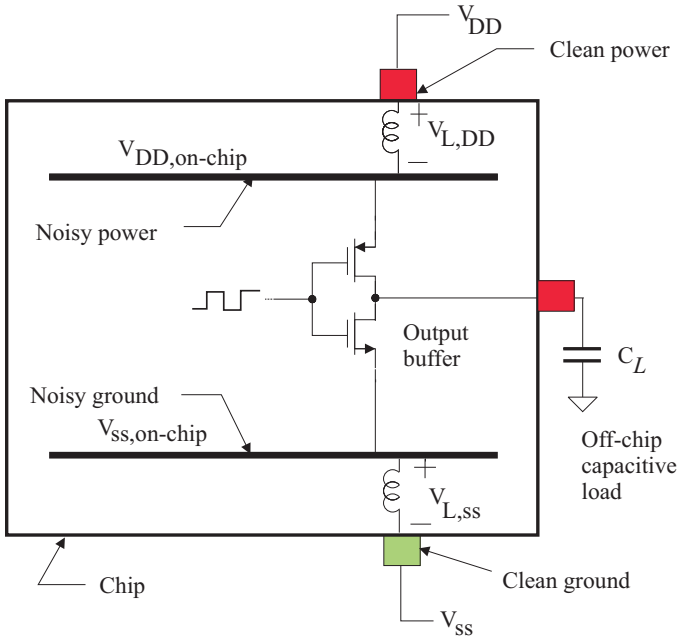

Figure 13: Noisy on-chip V_{DD} & V_{ss}.

▷ When sharp charging/discharging currents of output buffers flow through the bond wires of V_{DD} and V_{ss}, large voltage drops $v_{L,DD}$ and $v_{L,ss}$ across the bond wires are generated

▷ On-chip V_{DD} and V_{ss} vary with switching $\longrightarrow$ power fluctuation and ground bouncing:

$$\begin{aligned} v_{DD,on-chip} &= V_{DD} - v_{L,DD} \\ v_{SS,on-chip} &= V_{ss} - v_{L,ss} \end{aligned} \tag{8}$$

SSN (cont'd)

- **Simultaneous Switching Noise (SSN)**

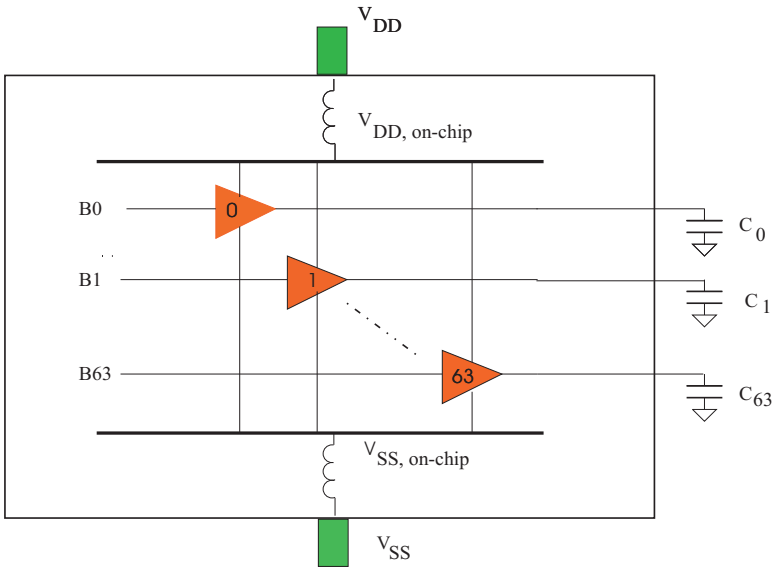

Figure 14: Simultaneous switching noise.

▷ Large switching noise at power and ground rails exist if multiple buffers switch simultaneously ⟶ Simultaneous switching noise (the Worst Case).

$$V_{DD,on-chip} = V_{DD} - v_{L,DD},$$
$$v_{L,DD} = L_{DD}\frac{i_{DD}}{dt} = L_{DD}\sum_{n=0}^{63}\frac{di_{C,n}}{dt}. \quad (9)$$

Effects of SSN

- **Fluctuation of on-chip V_{DD} and V_{ss}.**

$$\begin{aligned} V_{DD,on-chip} &= V_{DD} - v_{L,DD}, \\ V_{ss,on-chip} &= v_{L,ss}. \end{aligned} \tag{10}$$

- **Reduce noise margins of digital circuits**

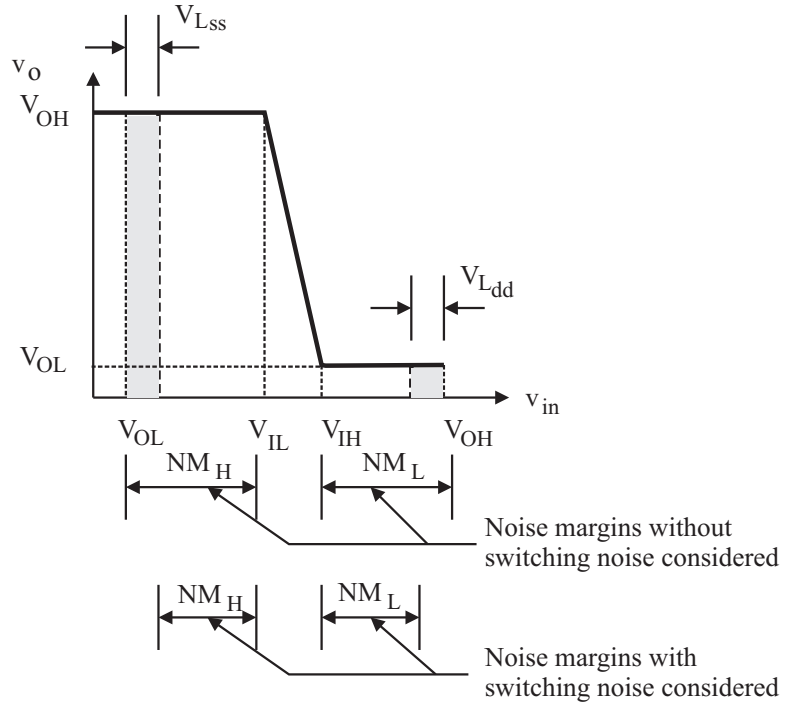

Figure 15: Reduction of noise margins due to switching noise.

$$\begin{aligned} NM_L &= (V_{OH} - V_{L_{dd}}) - V_{IH}, \\ NM_H &= V_{IL} - (V_{OL} + V_{L_{ss}}). \end{aligned} \tag{11}$$

Effects of SSN

• Change the Operating Point of Analog Circuits

▷ Consider a MOSFET biased in saturation, the transconductance g_m is given by $g_m = \dfrac{\partial i_D}{\partial v_{GS}} \approx \dfrac{2I_D}{V_{GS} - V_T}$, where I_D and V_{GS} are channel current and gate-source voltage at dc biasing point. Both I_D and V_{GS} are functions of $V_{DD,on-chip}$.

▷ SSN imposes stringent requirements on analog circuits. Analog circuits need to be differentially configured in mixed analog/digital circuits $\longrightarrow$ increased circuit complex.

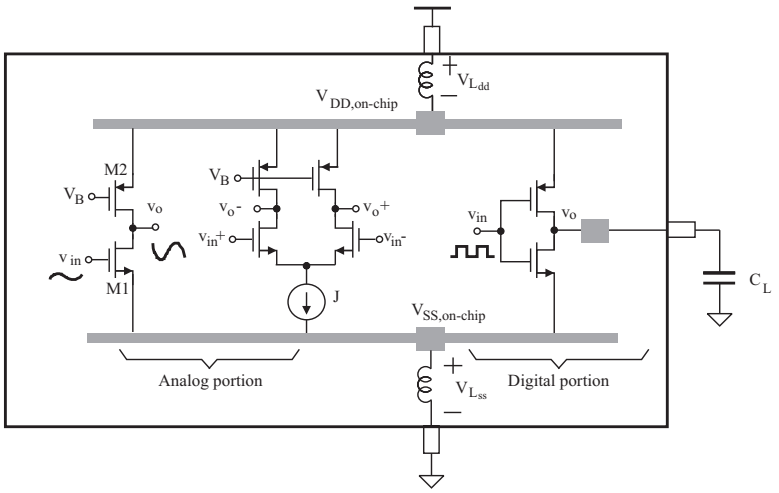

Figure 16: Mixed analog/digital circuits.

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Effects of SSN (cont'd)

- **Change of Operating Point of Analog Circuits (cont'd)**

  ▷ High power noise rejection $\longrightarrow$ difficult to design. If V_{DD} fluctuation is of a critical concern, Fig.17(a) should be used. The head biasing current source behaves as an OPEN-CIRCUIT for V_{DD} switching noise and isolates the circuit from V_{DD} rail.

  ▷ If V_{ss} fluctuation is of a critical concern, Fig.17(b) should be used. The tail biasing current source behaves as an OPEN-CIRCUIT for V_{ss} switching noise and isolates the circuit from V_{ss} rail.

  ▷ Cascodes and regulated cascodes are widely used in realizing these biasing current sources to maximize the resistance of the current sources.

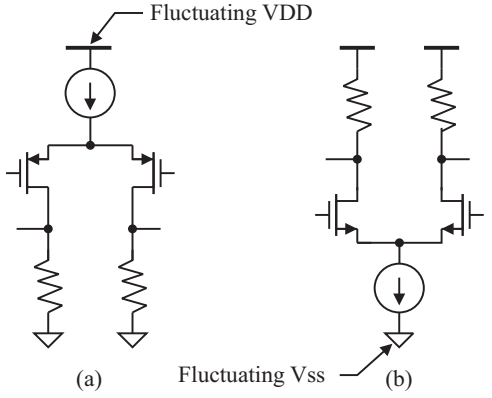

Figure 17: Differential configurations.

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Effects of SSN (cont'd)

- **Increase the Timing Jitter of Oscillators/Clocks**

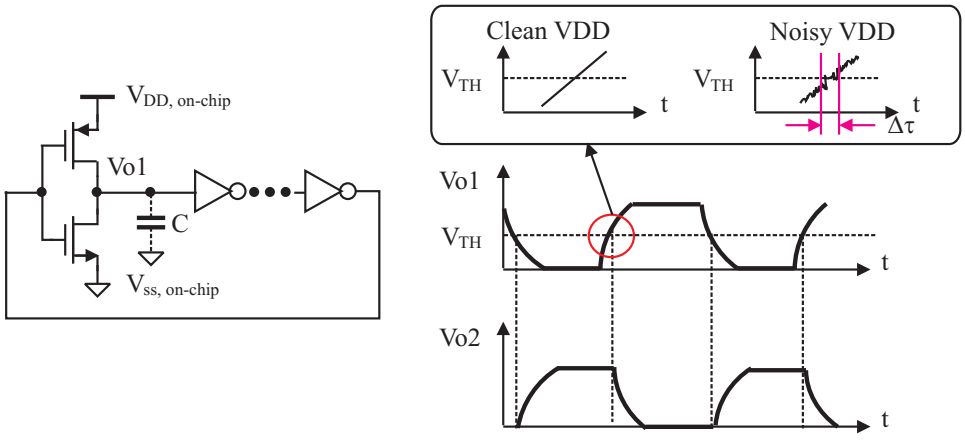

Figure 18: Timing jitter due to switching noise.

▷ The threshold crossing points of ring oscillators vary due to the noise (thermal and flicker noise) of the transistors. Such a variation is quantified by $\overline{\Delta\tau}^2$ - the timing jitter.

▷ Assume threshold voltage $V_{TH} = V_{DD,on-chip}/2$. For rising edge,

$$V_{DD,on-chip} = v_C + R_p C \frac{dv_C}{dt}, \tag{12}$$

where R_p is the equivalent channel resistance of pMOS. It is seen that v_C, subsequently, the threshold-crossing point, vary with $V_{DD,on-chip}$, which is a function of switching noise.

Analysis of SSN

- **Simplified Analysis of SSN**
- **SSN in Sub-micron CMOS Circuits**

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Simplified Analysis of SSN

- **Assumptions**
  - ▷ Triangle waveform of charging/discharging current.
  - ▷ Neglect channel resistance of transistors.

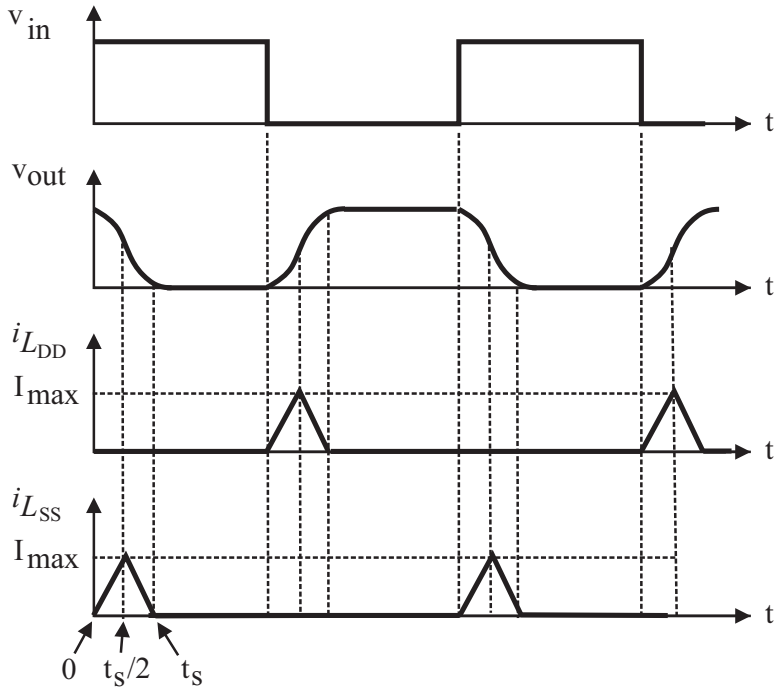

Figure 19: Simplified analysis of SSN.

Simplified Analysis of SSN (cont'd)

- **Analysis**

  ▷ Total charge stored in C_L before discharging $Q = C_L V_{DD}$.

  ▷ Total charge through L when C_L is completely discharged $Q = \int_0^{t_s} i_L(t)dt = I_{avg} t_s = \frac{I_{max}}{2} t_s$.

  ▷ Charge conservation : $C_L V_{DD} = \frac{I_{max}}{2} t_s$

  ▷ Because $\left[\frac{i_L(t)}{dt}\right]_{max} = \frac{I_{max}-0}{t_s/2-0} = \frac{2I_{max}}{t_s}$, we have

$$\left[\frac{di_L}{dt}\right]_{max} = \frac{4C_L V_{DD}}{t_s^2} \tag{13}$$

  ▷ Example: $L = 5$nH, $t_s = 5$ns, $C_L = 10$pF, $V_{DD} = 5$V, $L\left[\frac{di_L}{dt}\right]_{max}$=40 mV.

  ▷ SSN is extremely sensitive to t_s. Trade-offs between speed (t_s) and SSN are made in design of output buffers. The speed of output buffers should be set to the lowest possible value to minimize switching noise.

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SSN in Sub-micron CMOS Circuits

• Sub-micron MOSFETs

▷ Sub-micron : channel length is less than 1μm.

▷ Sub-micron MOS transistors exhibit velocity saturation due to excessive lateral electric field and mobility degradation due to excessive vertical electric field.

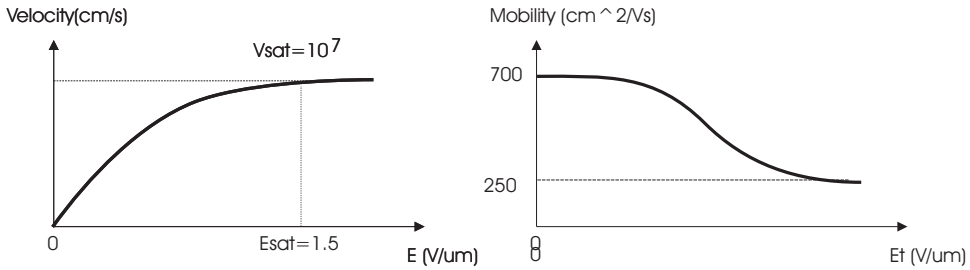

Figure 20: Velocity saturation and mobility degradation.

▷ Square-law does not hold for sub-micron MOS transistors. Instead, α-power law applies.

$$i_D = \begin{cases} 0 & \text{if} v_{GS} < V_T \text{ (cutoff)} \\ k_l(v_{GS} - V_T)^{\alpha/2} & \text{if} v_{DS} < v_{DS,sat} \text{ (Triode)} \\ k_s(v_{GS} - V_T)^{\alpha} & \text{if} v_{DS} > v_{DS,sat} \text{ (Saturation)} \end{cases} \tag{14}$$

where $k_l = \mu_n C'_{ox}(W/L)$, $k_s = \frac{1}{2}\mu_n C'_{ox}(W/L)$. Typically, $1 < \alpha < 1.2$

SSN in Sub-micron CMOS Circuits (cont'd)

- **Analysis**

  ▷ For a total of n output drivers that switch simultaneously, the total current

$$i_{DS,total} = ni_{DS} = nk_s(v_{in} - V_T - v_n)^{\alpha} \tag{15}$$

  ▷ SSN

$$\begin{aligned} v_n &= L_{ss}\frac{di_{DS,total}}{dt} \\ &= L_{ss}nk_s\alpha(v_{in} - V_T - v_n)^{\alpha-1}\frac{d(v_{in} - v_n)}{dt} \end{aligned} \tag{16}$$

  ▷ Because $a \approx 1$, $(v_{in} - V_T - v_n)^{\alpha-1} \approx 1$ We therefore have

$$\begin{aligned} v_n &= L_{ss}nk_s\alpha\frac{(dv_{in} - v_n)}{dt} \\ &= L_{ss}nk_s\alpha\frac{dv_{in}}{dt} - L_{ss}nk_s\alpha\frac{dv_n}{dt} \end{aligned} \tag{17}$$

  This gives

$$\frac{dv_n}{dt} + \frac{v_n}{\alpha n L_{ss}k_s} = \frac{dv_{in}}{dt} \tag{18}$$

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SSN in Sub-micron CMOS Circuits (cont'd)

▷ Input waveform

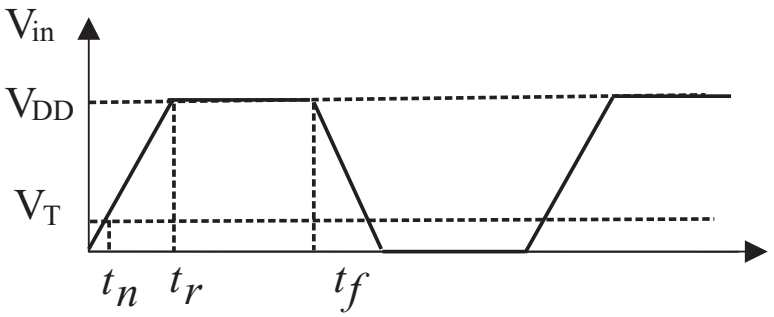

Figure 21: SSN analysis.

▷ Slopes

Slope of the rising section of the input

$$\frac{dv_{in}}{dt} = S_r = \frac{V_{DD}}{t_r} \tag{19}$$

▷ Equation for the rising section

Substituting the slope (the rising section of the input)

$$\frac{dv_n}{dt} + \frac{v_n}{\alpha n L_{ss} k_s} = S_r, \qquad v_n(t_n) = 0, t_n = \frac{V_T}{S_r}, t_n \leq t \leq t_r \tag{20}$$

This is a first-order ODE.

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SSN in Sub-micron CMOS Circuits (cont'd)

▷ Solution

- Homogeneous ODE - general solution

$$\frac{dv_n}{dt} = -\frac{v_n}{\alpha n L_{ss} k_s} \tag{21}$$

$$v_n = Ae^{-\frac{(t-t_n)}{\alpha n k_s L_{ss}}}, t \geq t_n \tag{22}$$

- Special solution ($v_n = C$ (constant))

$$\frac{C}{\alpha n k_s L_{ss}} = \frac{V_{DD}}{t_r} \tag{23}$$

which gives

$$C = \frac{V_{DD}}{t_r} n k_s L_{ss} \tag{24}$$

- Complete solution

$$v_n(t) = \frac{V_{DD}}{t_r} \alpha n k_s L_{ss} + Ae^{-\frac{(t-t_n)}{\alpha n k_s L_{ss}}} \tag{25}$$

- Match the initial condition at $t_n = \frac{V_T}{S_r}, v_n(t_n) = 0$

$$A = -\frac{V_{DD} \alpha n k_s L_{ss}}{t_r} \tag{26}$$

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SSN in Sub-micron CMOS Circuits (cont'd)

- **Complete solution**

$$v_n(t) = \frac{V_{DD}\alpha n k_s L_{ss}}{t_r}\left[1 - e^{-\frac{(t-t_n)}{\alpha n k_s L_{ss}}}\right],\ t_n \leq t \leq t_r. \tag{27}$$

▷ Remarks:

▷ $v_n(t)$ is proportional to

- n (number of switching buffers)
- L_{ss} (bond wire inductance)
- $k_s = \frac{1}{2}\mu_n C'_{ox}(W/L)_n$ (buffer size)
- $1/t_r$ (switching time)

▷ The maximum SSN

$$V_{n,max} = \frac{\alpha V_{DD} n k_s L_{ss}}{t_r} \tag{28}$$

▷ For a reliable operation, $V_{n,max} \leq V_T$ is generally required. This yields the limiting condition

$$\frac{\alpha V_{DD} n k L_{ss}}{t_r} = V_T \tag{29}$$

from which n and W can be determined for given V_T and t_r.

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SSN Reduction Techniques

- **Separate power and ground pins and pads for analog and digital circuits whenever possible**

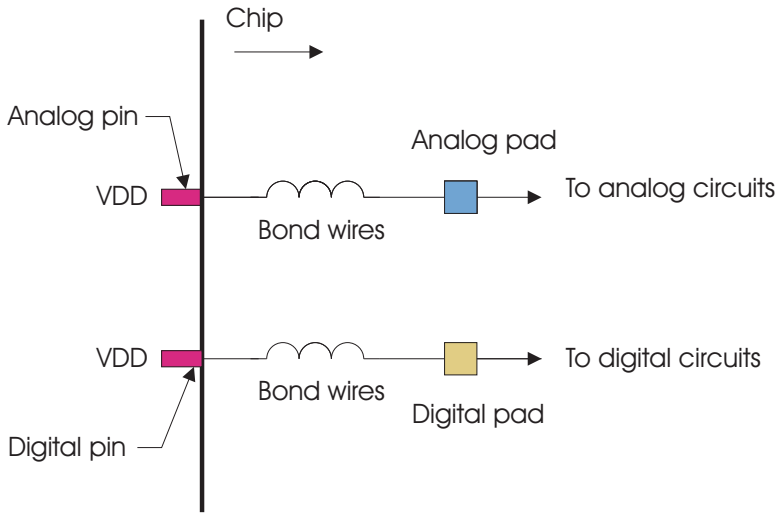

Figure 22: Separate analog and digital pins and pads.

▷ Switching noise generated by the digital portion of the system will not affect the operation of the analog portion of the systems.

SSN Reduction Techniques (cont'd)

- **Multiple pads and pins for power and ground**

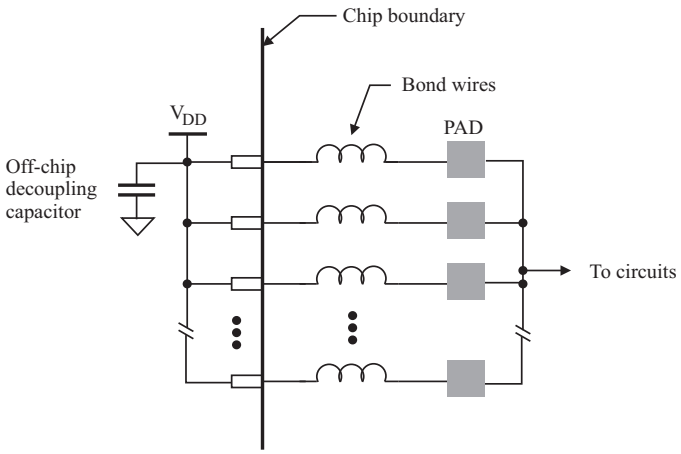

Figure 23: Multiple pins and pads.

▷ Increase the number of pins ⟶ smaller inductance ⟶ lower SSN.

SSN Reduction Techniques (cont'd)

- **Multiple pads and pins for power and ground (cont'd)**

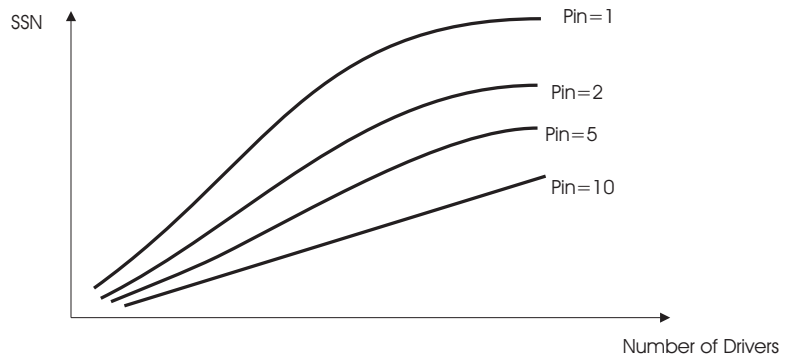

Figure 24: Effect of multiple pins.

▷ Increase the number of pins $\longrightarrow$ better linearity of SSN.

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SSN Reduction Techniques (cont'd)

- **Avoid using corner pads**
  - ▷ Corner pads have long bonding wires $\longrightarrow$ large self-inductances.
  - ▷ Most design rules require dummy pads (pads with no connection) at corners.
- **Use center pads for V_{DD} and V_{ss} $\longrightarrow$ smaller inductance, smaller SSN.**
  - ▷ Short bond wires, small self-inductances.

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SSN Reduction Techniques (cont'd)

- **Pre-driver skewing**

  ▷ To prevent the entire buffer (multi-finger layout - multiple smaller inverters connected in parallel) to switch at the same time.

  ▷ Use RC Delay Lines

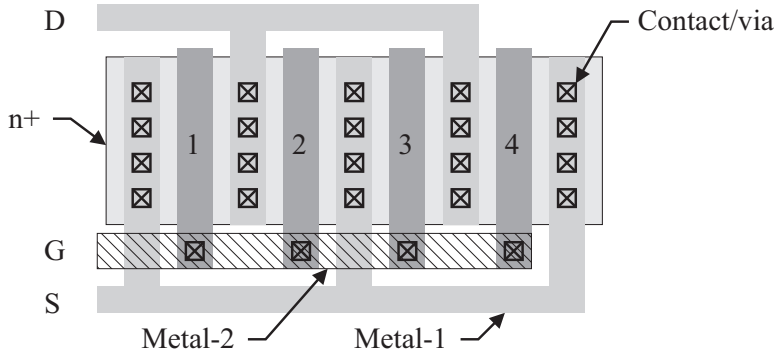

Figure 25: Multi-finger layout of output buffers. Both drain and source are shared by neighboring fingers.

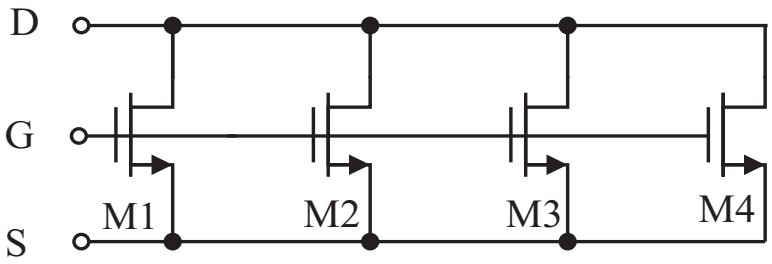

Figure 26: Schematic of the equivalent circuit of output buffers with a multi-finger layout.

SSN Reduction Techniques (cont'd)

- **Pre-driver skewing (cont'd)**

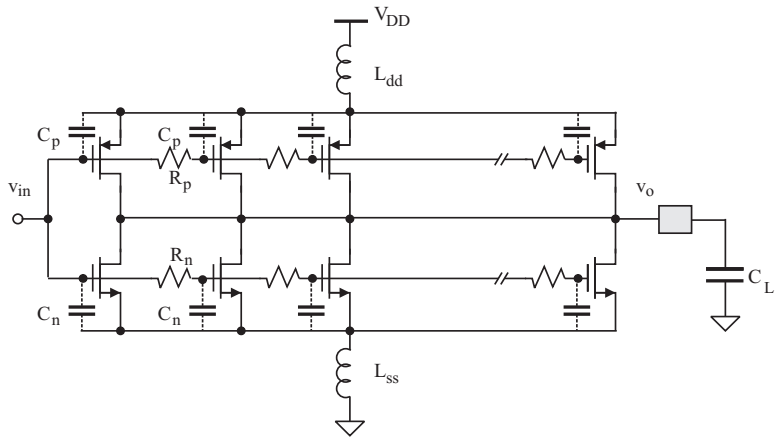

Figure 27: Output buffer with pre-skew.

▷ R_n, R_p = lumped n-well or poly resistors, C_n, C_p = gate-source capacitance. P_1/N_1 turn on first, P_1/N_1 turn on second, and P_M/N_M turn on the last.

▷ Drawback - reduced speed. Compromise between SSN and speed must be made.

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SSN Reduction Techniques (cont'd)

- **Pre-driver skewing (cont'd)**

  ▷ Use Gate Series Resistance for skewing

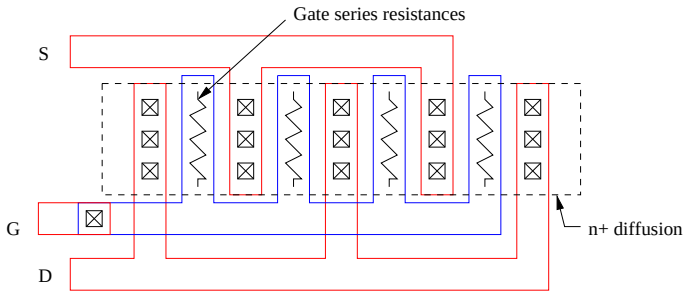

Figure 28: Pre-driver skewing using the gate series resistance.

  ▷ Less effective for silicide processes because the sheet resistance of gate ploy is small (approximately $7\Omega/\square$).

SSN Reduction Techniques (cont'd)

• On-chip decoupling (bypass) capacitors

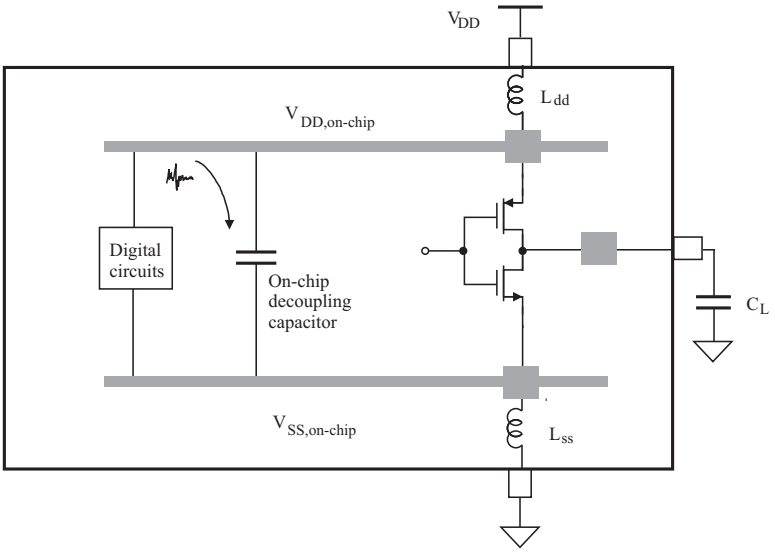

Figure 29: On-chip decoupling (bypass) capacitors.

▷ On-chip decoupling capacitors are effective in reducing SSN generated by internal logic circuits because they prevent current spikes generated by the internal logic circuits from going to L_{ss} and L_{DD} by providing a local AC path. On-chip decoupling capacitors serve as local charge reservoirs.

▷ On-chip decoupling capacitors must be very large in order to be effective, usually comparable to the total area of all transistors on chip (10-20% of total silicon area) - very expensive !

▷ Resistance is needed to avoid the self resonance formed by the on-chip decoupling capacitors and bond wires $\longrightarrow$ on-chip decoupling capacitors are typically implemented using MOS capacitors. The channel resistance of MOS capacitors are beneficial in minimizing the self resonance of the preceding LC networks.

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- Most CMOS fabrication processes require certain percentage of metal fill ratio for each metal layers (required for minimizing mechanical stress reasons). Dummy metal sections are often employed in each metal layer to fulfill this requirement. These dummy metal sections can be arranged in such a way that they form on-chip decoupling capacitors to improve the performance of designed chips.

SSN Reduction Techniques (cont'd)

- **Hierarchy of decoupling capacitors (cont'd)**

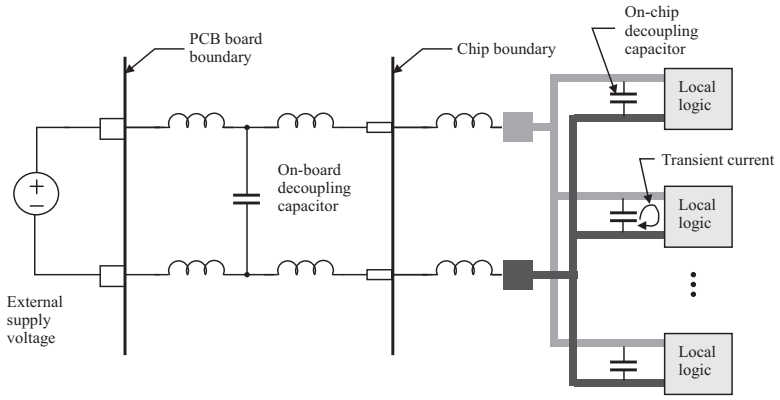

Figure 30: Hierarchy of on-chip de-coupling capacitors.

▷ Both off-chip and on-chip decoupling capacitors are required to minimize switching noise.

▷ Decoupling capacitors must be placed as close as possible to hot spots (noise sources) to eliminate generated switching noise locally.

▷ Traces and interconnects for decoupling capacitors must have a low impedance at high frequencies such that a low-impedance path exists to eliminate switching noise.

SSN Reduction Techniques (cont'd)

- **Fully-balanced buffers**

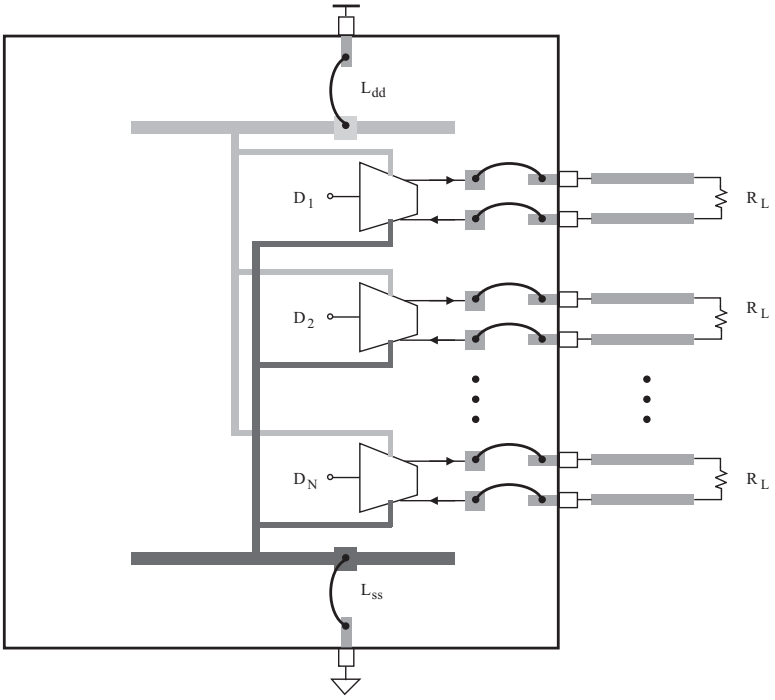

Figure 31: Balanced buffers.

▷ Each buffer conveys a fully differential current to the channel. Each buffer draws a constant current from the supply and injects a constant current to the ground. No net rate change of the current flowing through V_{DD} and ground pins - no switching noise.

SSN Reduction Techniques (cont'd)

- **Fully-balanced buffers (cont'd)**

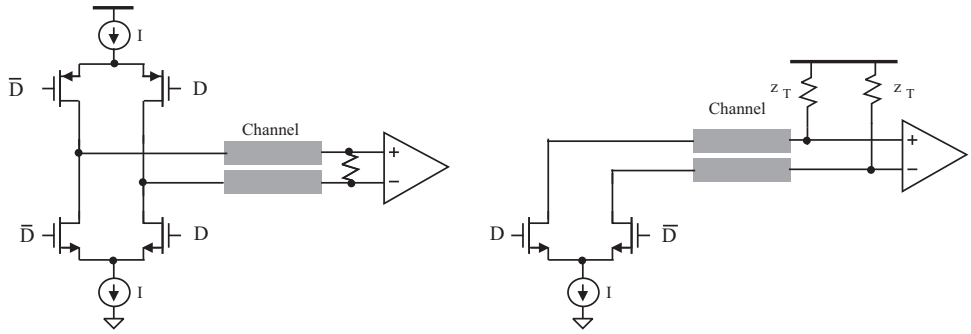

Figure 32: Balanced buffers.

▷ In the left figure, low-voltage-differential-signaling (LVDS) is used. The logic state of the output is represented by the direction of the output current. The channel is terminated at the far end by the termination resistor. The resistor also converts the current into a voltage.

▷ In the right figure, the channel is terminated with the line characteristic impedance at the near end of the channel.

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SSN Reduction Techniques (cont'd)

• Current-mode logic circuits

▷ Use logic circuits that draw a constant current from V_{DD} and inject a constant current to V_{ss}. Current-mode logic (CML) circuits, fully differential logic circuits belong to this category.

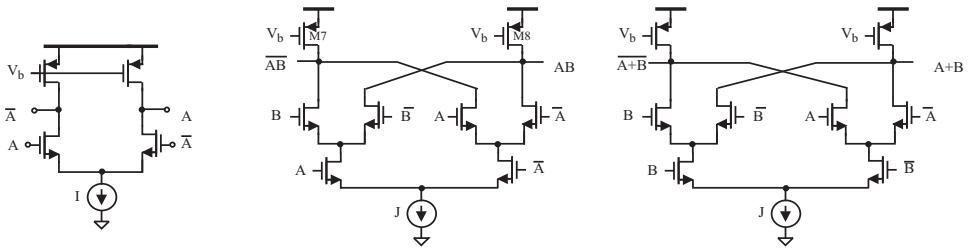

Figure 33: Current-mode logic gates.

▷ CML circuits draw a constant static current from V_{DD} regardless of its logic states $\longrightarrow C_L \dfrac{di_L}{dt} = 0$, resulting in zero switching noise.

▷ CML circuits consume static power. They are typically used for I/Os or in applications where switching noise is critical.

▷ CML circuits consume less power as compared with static logic circuits at very high frequencies. This is because the dynamic power consumption of static circuits is governed by $P_d = aCfV_{DD}^2$, where a=switching activity parameter, f=frequency. It is evident that P_d is directly proportional to f. The power consumption of CML circuits is independent of f!

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Design Criteria for SSN

• SSN must less than Threshold Voltages

▷ For a reliable operation, $V_{n,max} < V_T$ is generally required.

▷ Switching noise derived before

$$v_n(t) = \frac{\alpha V_{DD} n k_s L_{ss}}{t_r}\left[1 - e^{-\frac{(t-t_n)}{\alpha n k_s L_{ss}}}\right], \quad t_n \leq t \leq t_r. \tag{30}$$

This yields

$$\frac{\alpha V_{DD} n k L_{ss}}{t_r} = V_T, \tag{31}$$

from which n and W can be determined for given V_T, f, and t_r.

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Analog and Digital Grounding

• Substrate Modeling

▷ Resistive paths exist from p+ contacts to p-substrate. A voltage change of p+ contacts affects the voltage of substrate.

▷ Capacitive paths exist from p+/n-well, n+/p-substrate, and n-well/p-substrate junctions.

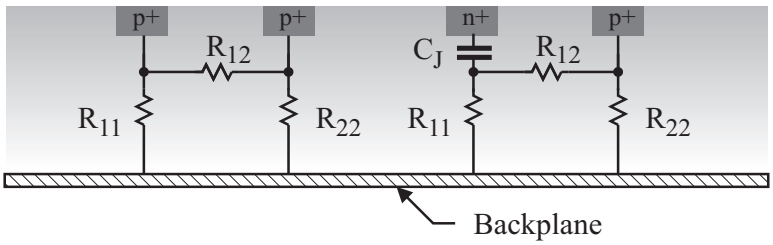

Figure 34: Lumped models of heavily doped substrates.

▷ $R_{12} \gg R_{11}, R_{22}$. R_{12} = resistance between contacts, R_{11}, R_{22}=resistance from contacts to the backplane. Most of substrate noise will travel vertically down to the backplane. The backplane must be grounded properly to avoid the distribution of substrate noise to the entire chip. (Ref.: B. Owens et al. "Simulation and measurement of supply and substrate noise in mixed-signal ICs," *IEEE J. Solid-State Circuits*, Vol.40, No.2, pp. 382-391, Feb. 2005).

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Analog and Digital Grounding (cont'd)

- **Separate analog and digital power pads and bonding wires for analog and digital circuits.**

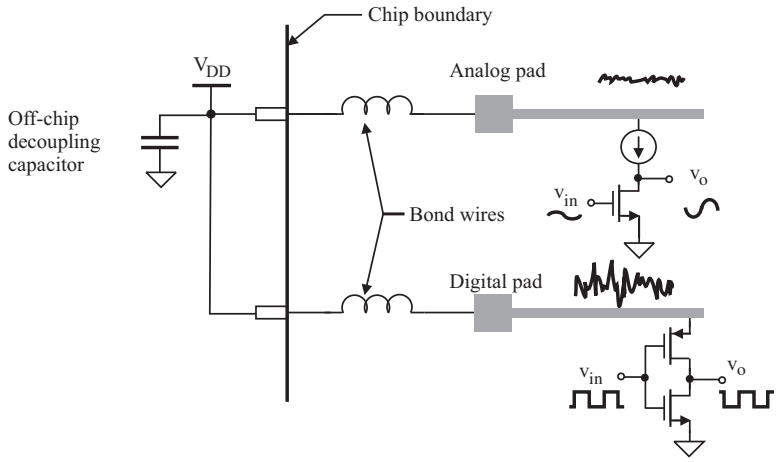

Figure 35: Separate analog and digital V_{DD} pads and bonding wires for analog and digital circuits.

▷ Digital V_{DD} rails are much more noisy as compared with analog V_{DD}.

Analog and Digital Grounding (cont'd)

- **Separate analog and digital ground pads and bonding wires for analog and digital circuits.**

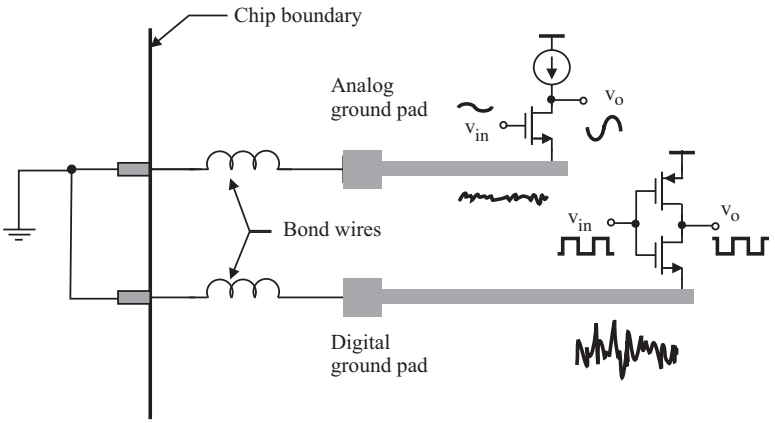

Figure 36: Separate analog and digital V_{ss} pads and bonding wires for analog and digital circuits.

▷ Digital V_{ss} rails are much more noisy as compared with analog V_{ss}.

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Analog and Digital Grounding (cont'd)

- **Separate analog and digital substrate connections.**

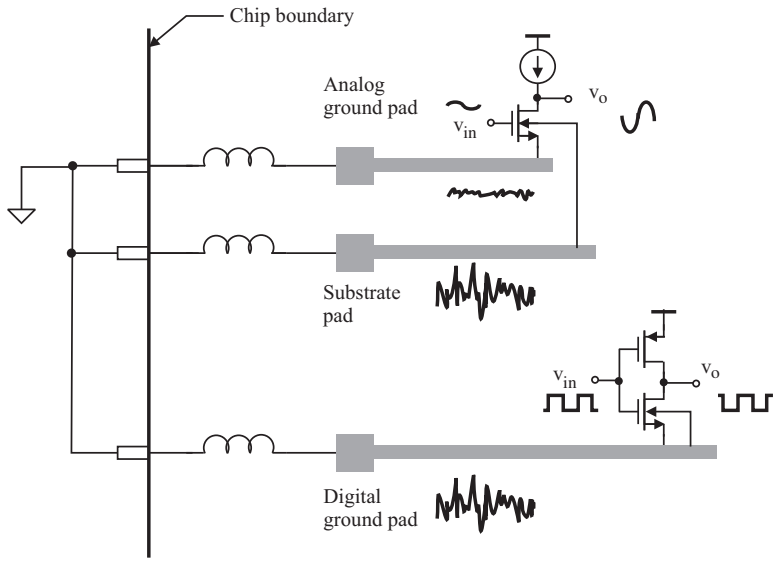

Figure 37: Separate analog and digital substrate connections.

▷ Analog substrates are typically protected by guard rings. They are less noisy as compared with digital substrates.

▷ Connecting analog substrate to the outside ground directly can lower the voltage fluctuation of the analog substrate. Downside: body effect occurs as $V_T = V_{To} + \gamma\left(\sqrt{V_{sb} + |2\phi_F|}\right) - \sqrt{|2\phi_F|}$), where γ is body-effect coefficient and $\phi_F \approx 0.6$V is the Fermi potential.

▷ If analog substrates are well protected, then the source of MOSFETs and analog substrates can be tied together to eliminate the body effect. Example - differential pairs.

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Analog and Digital Grounding (cont'd)

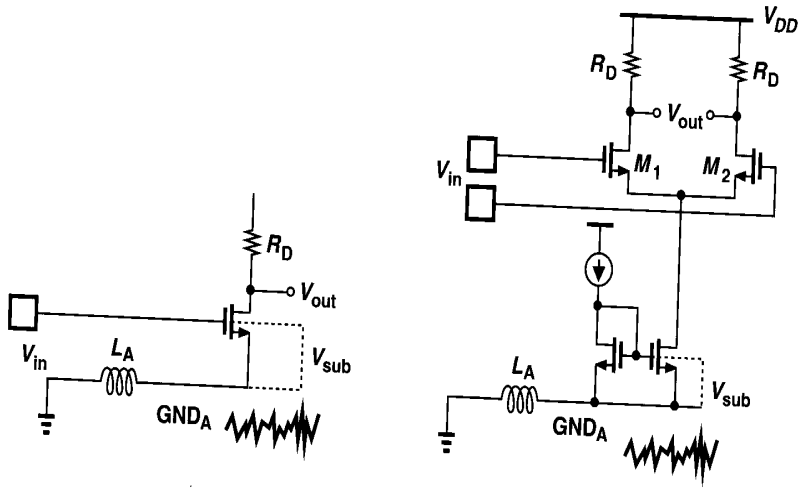

Figure 38: Differential configuration.

▷ Single-ended configuration - v_{GS} is directly affected by ground bouncing.

▷ The output of differential-mode configurations is insensitive of SSN as the biasing circuitry provides a constant biasing current to the differential pair regardless of ground bouncing.

▷ Deep sub-micron MOS transistors have a small output impedance, reducing the effectiveness of the biasing circuitry. Cascode is generally mandatory in biasing circuits to minimize the effect of ground bounding.

Analog and Digital Grounding (cont'd)

- **Passive Guard-Rings**

  ▷ Use passive guard-rings to isolate sensitive circuits from noisy digital circuits.

  ▷ p+ guard rings - p+ diffusion contacts on p-substrate to collect holes. n+ guard rings - n+ diffusion contacts in n-wells to collect electrons.

  ▷ Guard ring resistance should be made as low as possible ⟶ guard rings should be made as wide as possible.

  ▷ Guard rings should be placed as close as possible to noise sources.

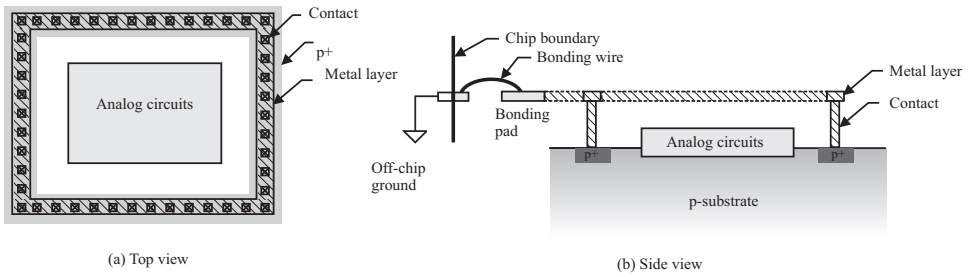

Figure 39: p-type passive guard rings.

Analog and Digital Grounding (cont'd)

- **Active Guard Rings**

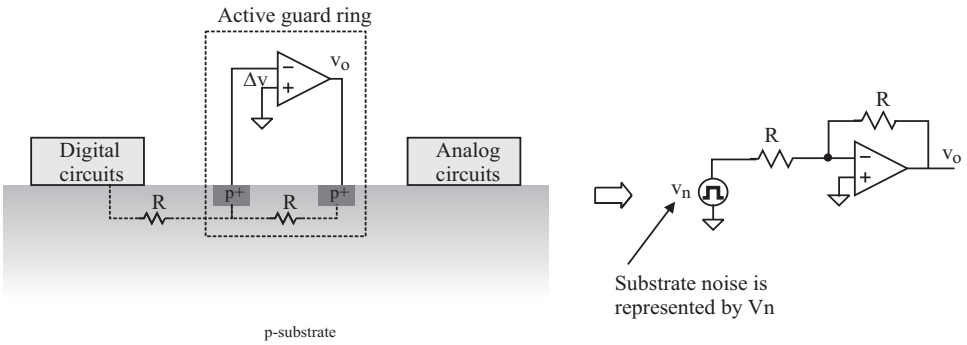

Figure 40: Active passive guard rings (Ref. K. Fukuda et al., "Substrate noise reduction using active grant band filters in mixed-signal integrated circuits," *IEICE Trans. Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E80-A, pp.313-320, Feb. 1997).

▷ Use active guard-rings to ACTIVELY isolate sensitive circuits from noisy digital circuits. Active guard rings perform better as compared with passive guard rings.

▷ The inverting voltage buffer must have a large bandwidth in order to be effective in suppressing substrate noise. This is because v_n contains a significantly large number of high-frequency components and these components must appear at the output of the buffer in order to suppress substrate noise.

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