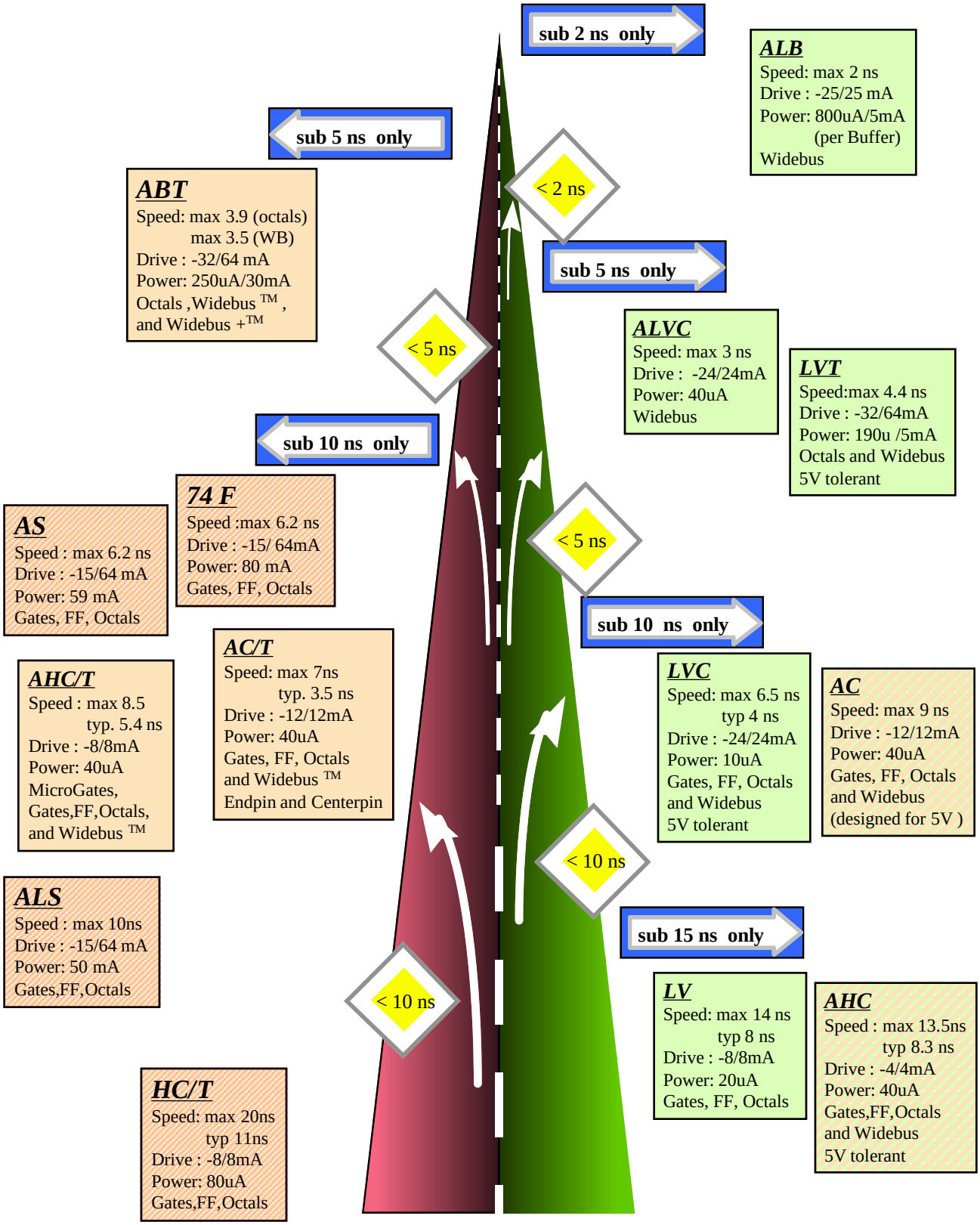
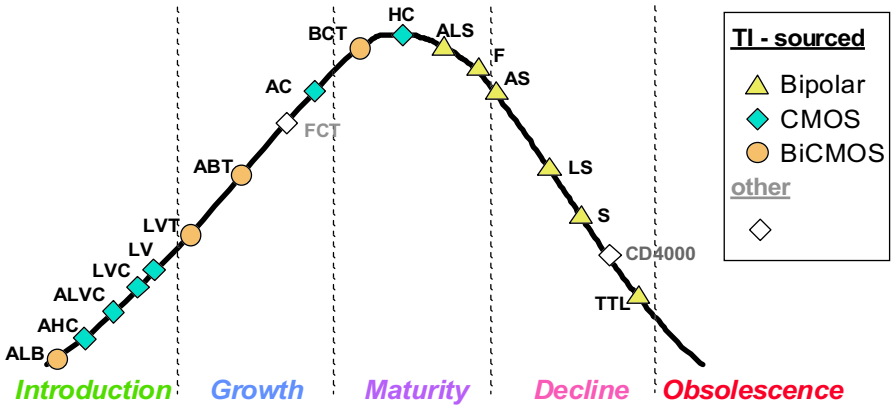
Logic Families

5Volt ASL - ROAD 3.3Volt



Digital Design Seminar

Product Life Cycle



- ★ TI remains committed to be the last supplier in the older families.
- ★ Investment levels for new products are at an all time high while end equipment requirements are accelerating new product introduction.

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The Product Life Cycle curve shows all available logic families from TI.

This cycle is divided into 5 sections, beginning on the left side with the introduction phase and ending on the right side with obsolescence.

One can find that all bipolar families are in the decline phase. Those are not recommended to be used in new designs.

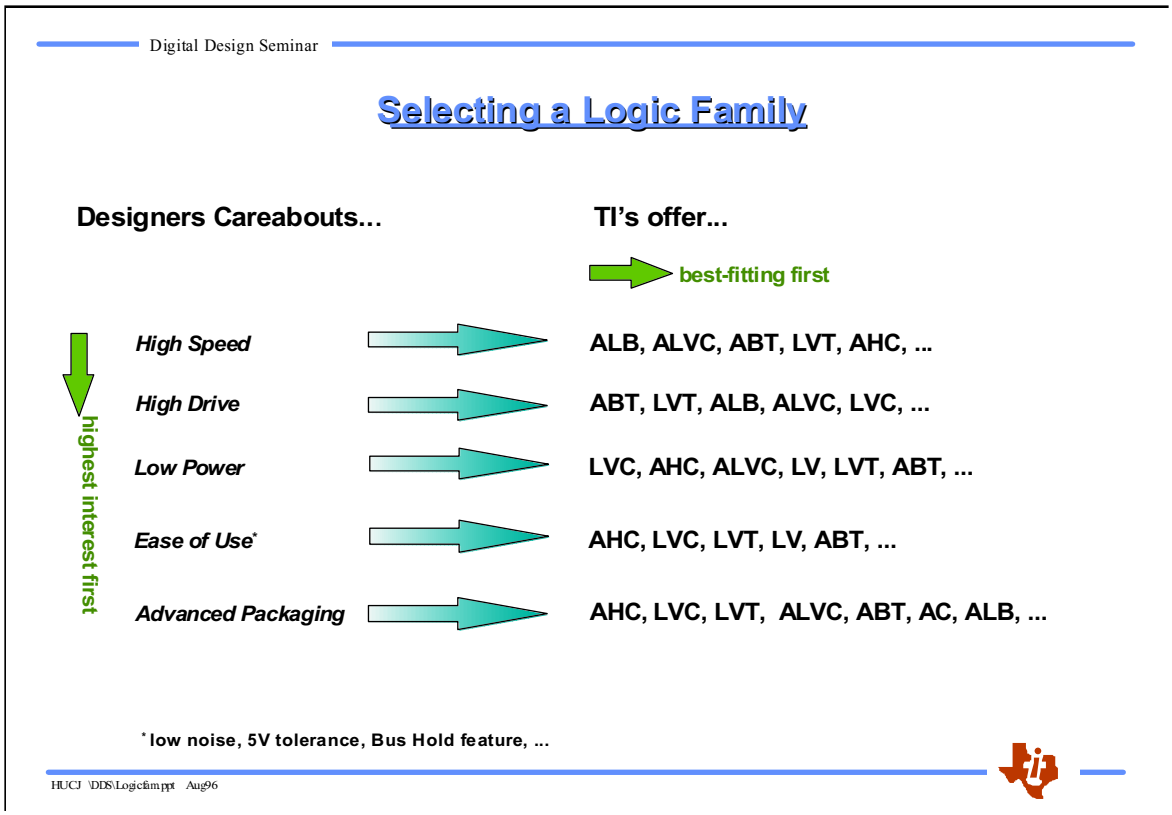
Today's system trends, such as increased packaging density, higher operating frequencies and reduced heat generation (e.g. no need for a cooling fan), lead to a strong need to reduce the power consumption or to change to low power technologies. This limits the use of mature technologies like LS and F. Even for HCMOS there is an improved version available: AHC Advanced HCMOS.

With the development of BiCMOS, a combination of Bipolar and CMOS technologies, the high drive capability and low noise characteristic of bipolar technology and the low power consumption of CMOS technology have been combined.

TI has true second source agreements with Philips Semiconductor and Hitachi Semiconductor for the Advanced BiCMOS Technology (ABT) family as well as for the low-voltage families (LV, LVC, LVT, ALVC). The agreement with Philips has recently been extended to also cover ALVT and AHC.

Investments for new products are at an all time high while end equipment requirements are accelerating new product introduction.

On the other side, TI remains committed to be the last supplier in the older families.



Customer careabouts for selecting the optimum logic family are diverse depending on application needs and targetted end-equipments. From a survey, recently conducted by TI, the ranking of customer careabouts are as shown above.

According to this survey the careabouts have been sorted by importance from top to bottom.

The logic families have been sorted from left to right with regard to the most suitable family for a given criteria.

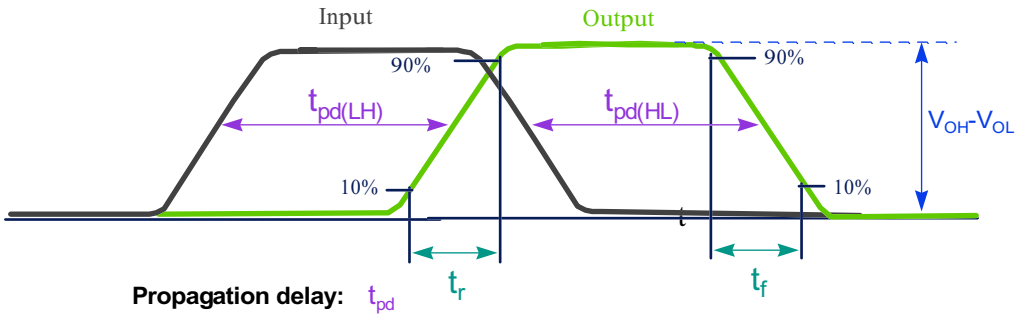
For example: you are looking for the fastest logic family ?

Choose the row 'High Speed' and look for the first family in 'TI's offer': ALB

It doesn't matter which focus you have; TI offers always the optimum logic family for your application.

Digital Design Seminar

Basic Definitions: Speed



Propagation delay: t_{pd}

Transition time: t_r *(rise time)* or t_f *(fall time)*

Voltage swing: $V_{OH} - V_{OL}$

Slew rate: $\frac{dv}{dt} = \frac{(V_{OH} - V_{OL}) \times 80\%}{t_r \text{ (or } t_f)}$

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There are two parameters, a designer may have in mind when mentioning "speed". The more frequently used refers to the circuit's propagation delay, t_{pd}.

The shorter the t_{pd}, the higher the speed.

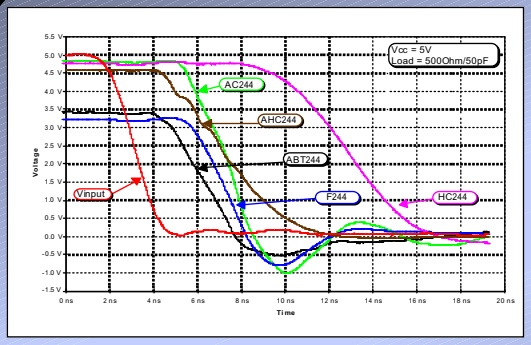
Some engineers, however, also refer to "circuit speed" in the context of a device's signal slew rate. As can be seen from the formula, a circuit's slew rate corresponds to the transition (rise or fall) time of the output signal.

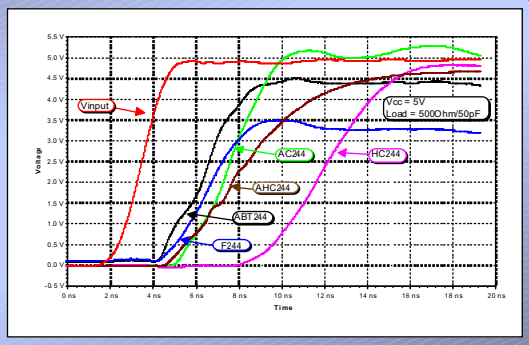
The shorter the rise or fall time, the higher the slew rate.

As will be shown on the next page, propagation delay and slew rate are not necessarily proportional.

Digital Design Seminar

Switching Characteristic
Slew Rate - 5-V Logic





	F	ABT	HC	AHC	AC	
Slew rate (tphl):	1.3	1.0	0.9	0.8	1.8	V/ns

	F	ABT	HC	AHC	AC	
Slew rate (tplh):	0.9	1.0	0.8	0.7	1.5	V/ns

This and the next page show propagation delays (t_{pd}), voltage swing (V_{OH} - V_{OL}) and slew rates (dv/dt) for selected 5V and 3V logic families.

F, ABT, HC, AHC and AC are operating from a 5V supply voltage, while LVT, ALVC, LVC, AHC and LV have a 3.3V supply (next page).

The data may indicate that t_{pd} and dv/dt show common trends, but a closer look points out that there is no direct link between the two parameters. For example, the fastest family (ABT) is not the one with the highest slew rate. Another example is AHC, which is characterised by a three-fold speed improvement over HCMOS, but shows lower slew rates.

As will be discussed later in this section, high slew rates are often unfavourable, as this leads to high noise levels generated by the components. The worst technology in this respect is 5V AC, while AHC gives very positive results.

Slew rates must be considered especially when designing high speed systems.

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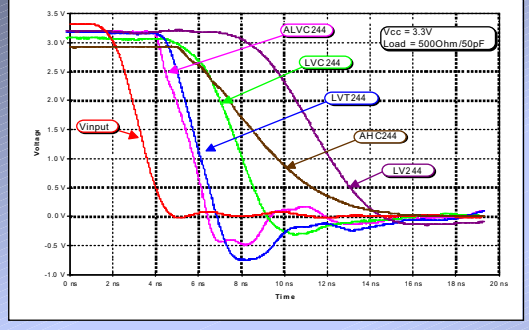
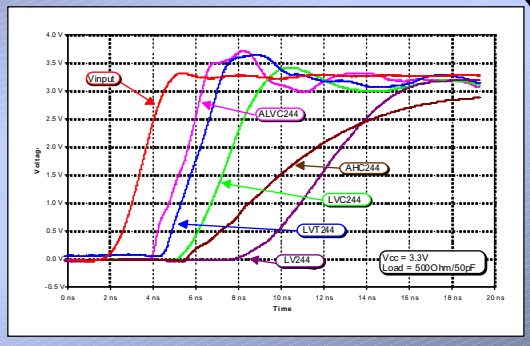
Switching Characteristic
Slew Rate - 3-V Logic





	LVT	ALVC	LVC	AHC	LV	
Slew rate (tphl):	1.2	1.3	0.9	0.5	0.7	V/ns

	LVT	ALVC	LVC	AHC	LV	
Slew rate (tplh):	1.0	1.2	0.8	0.4	0.5	V/ns

These graphs show propagation delays (t_{pd}), voltage swing (V_{OH} - V_{OL}) and slew rates (dv/dt) for selected 3V logic families (LVT, ALVC, LVC and LV) and AHC operated at Vcc=3.3V (as specified in the datasheet).

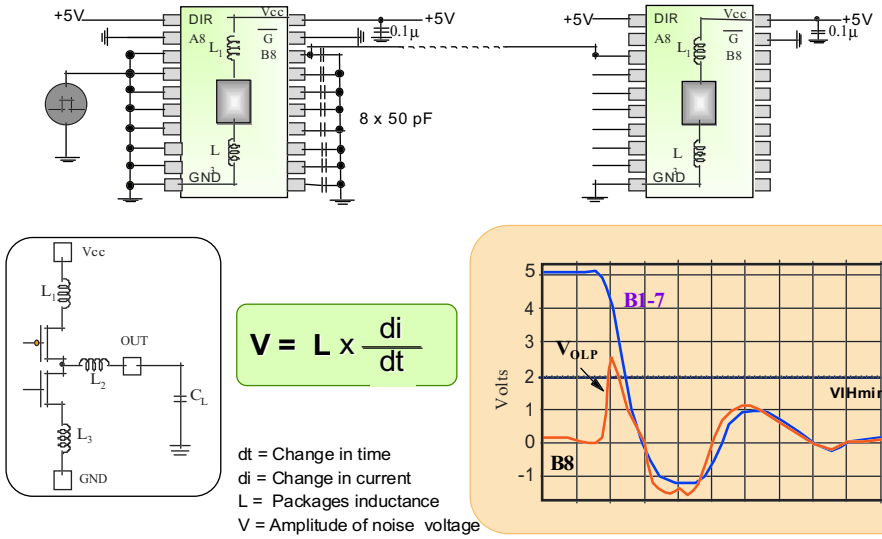
In comparison to 5V logic, all of the low voltage technologies have somewhat lower signal slew rates.

It should be especially noted that ALVC, the fastest of all technologies shown, exhibits an uncritically low slew rate.

Circuit design techniques and the use of SSOP or TSSOP packages makes this favourable characteristic available.

Digital Design Seminar

Simultaneous Switching and Ground Bounce



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A widely accepted method of measuring ground bounce is to switch (N-1) device outputs, while keeping the Nth input at a Low level.

The outputs of the drivers which are switching react with a certain delay to the changes at the inputs, whilst the unswitched output should remain undisturbed at “L” level. But, crosstalk from the neighbouring pins, a brief dip in the supply voltage and a brief rise of the groundlevel (resulting from the inductance of the Vcc and ground connections) automatically cause a reaction at the corresponding output.

The best results are achieved by the 48 pin Widebus package. This is primarily because of the 8 distributed GND pins for the 16 integrated drivers. The traditional 8 bit ‘corner pin’ devices are provided with only one GND pin and therefore show poor behaviour.

It is also necessary to mention that the measured values of noise level depend on the process technology used.

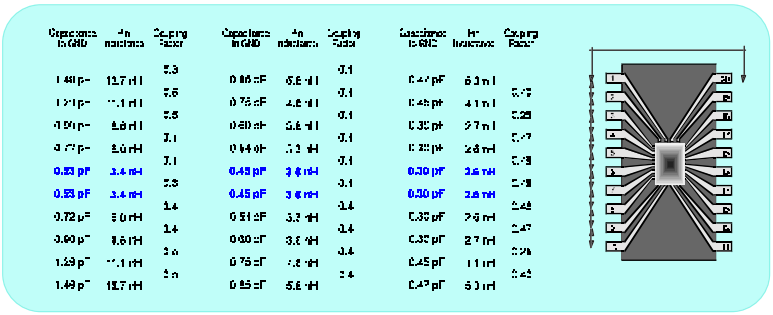
Whereas with BiCMOS and bipolar devices the threshold level will normally not be exceeded, with fast CMOS logic 2V or more may be reached as a result of the steeper pulse slope of CMOS signals, and consequently higher effect on the lead inductance.

Digital Design Seminar

Package Inductance drives Noise Voltage

- ★ Noise levels depend on package inductance and current slew rates (di/dt)
- ★ Noise voltages induced in switching outputs will be cross-coupled into quiet output(s)
- ★ Packages with multiple V_{CC}/GND pins (e.g. Widebus™) typically show much lower noise
- ★ Slew rate control helps reduce noise

DIP **SOP** **SSOP**



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There are three factors which determine the electrical characteristics of a package:

1) the capacitance of a pin to ground

2) the inductance of a pin

3) the coupling factors of the pins to each other

In particular, the supply voltage pin should have a low inductance, and all signal lines of a good package should have as low as possible of all these three parameters.

The table above shows capacitance, inductance and coupling factor of each two neighboured pins. These parameters are determined by:

• the length of the connections to the pin within the package,

• the spacing between these connections,

• the length of the wirebonds.

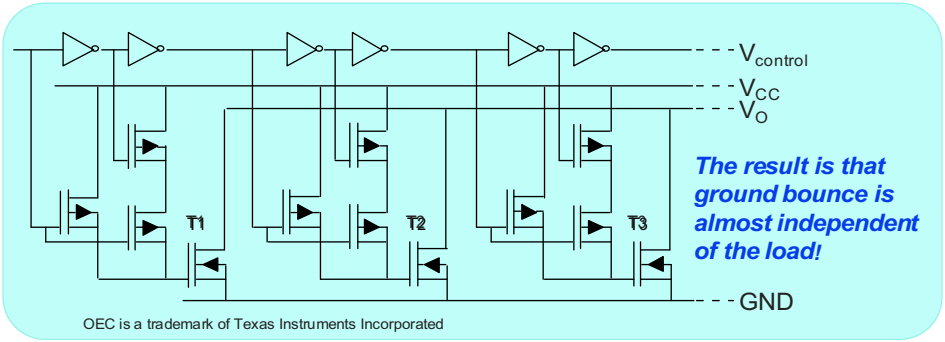
A DIP package has significantly longer internal connections than SOP or SSOP (and TSSOP). A long connection results in a high inductance and a high coupling factor; additionally the increased area caused by the long connections results also in a high capacitance.

However, the reduction in coupling factor achieved by the short connections is partly be offset by the smaller spacing between them.

Digital Design Seminar

Output Edge Control Circuitry (OEC™)

- ★ **Gradual turn-on of output transistors by splitting the output in multiple stages**
- ★ **Dynamic smoothing circuit by softening the turn-on to obtain gradual takeover of current (di/dt control)**



Signal slew rate improvements seen in Advanced Logic circuits have mainly been achieved by designing the circuits' output stages such that the change in output current (di/dt) and correspondingly the change in output voltage (dv/dt), are under control.

For this purpose, Texas Instruments has developed a technique called

Output **E**dge **C**ontrol (**OEC™**)

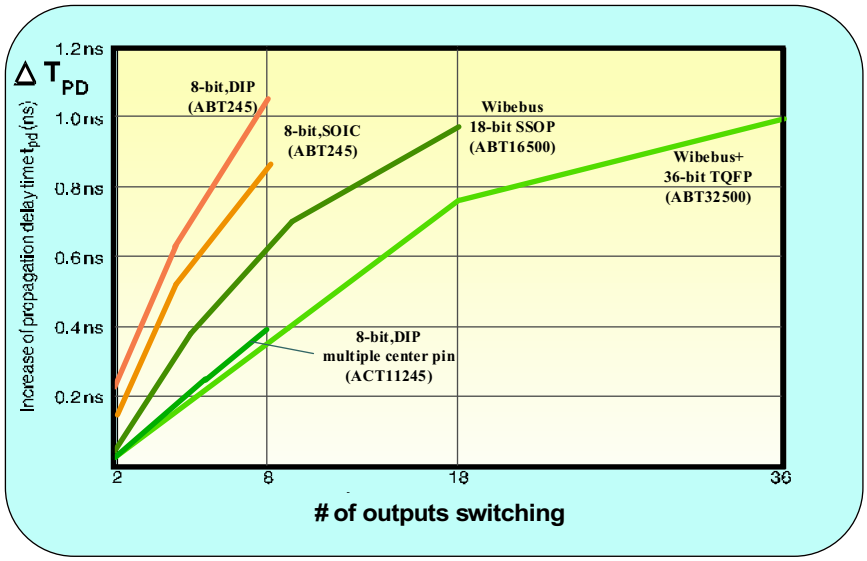
The use of parallel output transistors that are turned on one after the other limits the signal slew rate.

A side effect is that the output noise levels are almost independent from the circuit load.

OEC has been implemented in AC, LVC and LVT.

Digital Design Seminar

ΔT_{PD} vs Number of Outputs Switching



The propagation delay of the component depends also on the number of simultaneously switched outputs.

The reason can be found in the inductance of the supply leads acting as "current brakes" .

For devices in conventional packages (DIP and SOP) additional delay of 150 to 200 ps for each output switched needs to be taken into account.

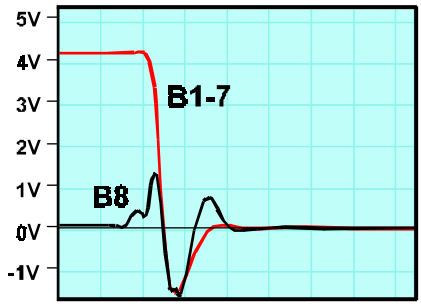
For example, an SN74F244 will have a maximum delay tp_{HL} = 7.5 to 8 ns, if all eight outputs switch simultaneously.

In this respect, the multiple V_{CC} leads in Widebus™ circuits are of advantage. They may not eliminate the effect, but at least they insure that the loss of speed is no greater than in octal bus drivers, even though twice as many outputs are switched.

Digital Design Seminar

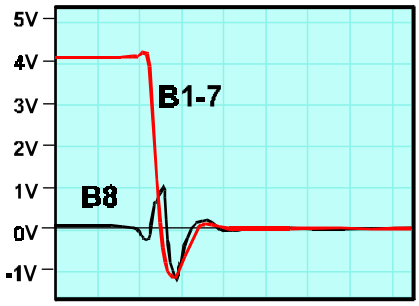
Simultaneous Switching with Bipolar and BiCMOS Logic

SN74F245



Critical with F/AS in poor designs

SN74ABT245

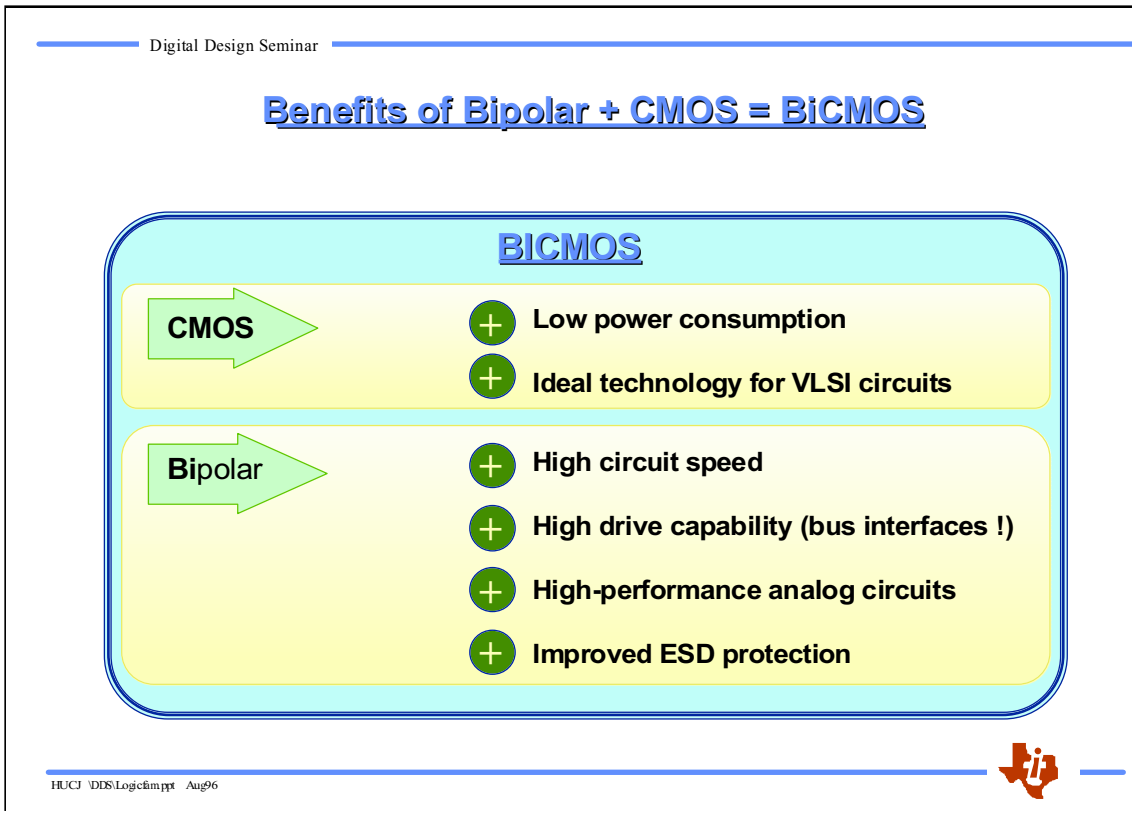


Not critical with BCT/ABT/LVT

Comparing ABT with 74F logic on simultaneous switching noise, one can recognize that the device of the F-family shows a more critical behaviour than the ABT device.

The maximum undershoot of the F device is greater than -1.5 V, while the ABT devices show a maximum value of about -800mV only.

Ground bounce behaviour must be taken into acount very carefully for the design of digital systems using fast bipolar and CMOS technology families as F/AS or AC/FCT.



Advanced BiCMOS technology (ABT) is available from Texas Instruments, to help designers in developing high performance bus systems.

It was designed to provide speeds equivalent to existing advanced bipolar solutions with 90% less power consumption.

ABT employs a submicron 0.8µm process technology.

It combines elements of both bipolar and CMOS circuits onto a single silicon chip.

ABT is based on a CMOS core-circuit structure with an NPN bipolar output transistor module added.

From a power (current) consumption standpoint, the use of bipolar in the output stage is advantageous for two reasons:

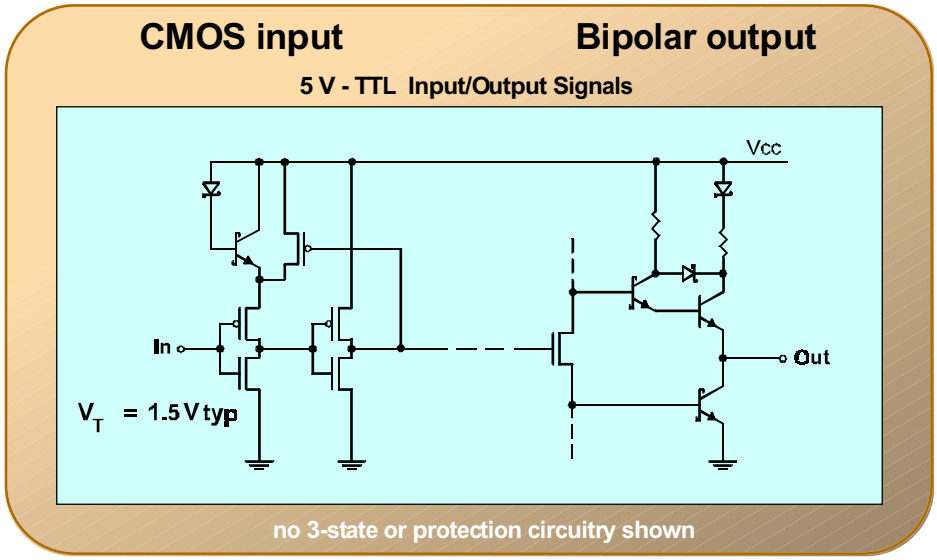
1) the voltage swing is less than that of a CMOS output. The power consupmed when charging or discharging internal circuit capacitances and the external load capacitance is reduced.

2) the bipolar transistors are capable of turning off more efficiently than CMOS transistors. The wasteful flow of current from V_{cc} to GND is reduced.

Although bipolar does tend to have a high static power consumption, its lower dynamic power consumption allows for better overall power performance at high frequencies than either pure bipolar or CMOS as the dynamic power makes up the majority of a device's overall power consumption.

Digital Design Seminar

BICMOS Inner Circuitry



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Simplified input and output stages of an ABT transceiver are shown on this slide.

The inputs are designed to offer TTL- compatible levels with guaranteed switching between a V_{IH} minimum of 2V and a V_{IL} maximum of 0.8V.

As these inputs are implemented in CMOS circuitry they offer high impedance for low leakage and low capacitance for minimal bus loading.

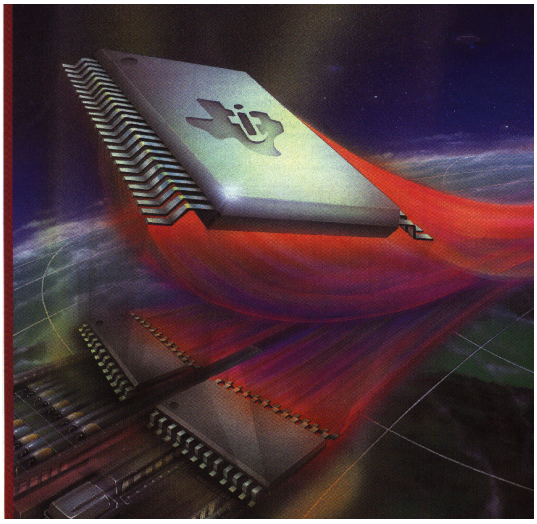
(The CMOS supply voltage of the input stage is dropped by diode D1 and transistor Q1, centering the threshold around 1.5V).

ABT outputs utilizes bipolar circuitry to provide the speed and drive necessary for a bus interface. A major advantage of using bipolar circuitry in the output stage is the reduced voltage swing, which lowers ground noise, improves signal integrity and reduces dynamic power consumption.

Because of its small process geometry, tight metal pitch and shallow junctions, ABT can provide for strong output drive currents (sink current 64mA, source current 32mA) and low capacitances. As a result of these enhancements, internal propagation delay are very fast and show a good behaviour regarding noise.

Digital Design Seminar

Widebus™ Devices Reduce Component Count



- Significant noise improvement
- More than 50% PCB space savings
- Significant speed improvement

Widebus is a trademark of Texas Instruments Incorporated

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Widebus™ circuits offer designer substantial advantages, when it comes to designing advanced systems.

With the growing performance demands that are being made of computer systems, one has to expand the width of bus systems to 16 or 32 bits, so that high data throughput can be achieved. As the available space for a circuit is limited, this can only be implemented with components like Widebus™, which support wide bus architectures at an attractive cost.

As circuits become faster, the electrical characteristic of the package becomes more and more the focal point. Besides the unavoidable capacitances of the leads, it is primarily their inductances that determine the response of fast digital circuits and which, in some cases, limit their usage.

In addition, doubling the transfer channels in the new circuits reduces the component count by 50%.

Each of these new components is no bigger than a conventional 24-pin SO package, as the new circuit uses only 50% of the area previously used.

Digital Design Seminar

WIDEBUS / Widebus +™

	16 Bits				18 Bits				20+bits		
ABT Advanced BiCMOS Technology	16240	H16245	16543	16833	16500B	162601	16843	H18646	16260	H18504A	32245
	16241	16373A	16623	16853	162500	16823	16863		162260	162827	32316
	16244A	16374A	16640	16952	16501	H16823	18245A		16460	16841	32318
	162244	16470	16646		162501	162823	H18502A		162460	162841	32501
	16245A	16540	16652		16600	16825	H18504A		16821		32543
	162245	16541	16657		16601	162825	18640		16827		
AC/T Advanced CMOS	16240	16374	16623	16833			16472		16821		
	16241	16470	16640	16952			16474		16827		
	16244	16540	16646				16475		16841		
	16245	16541	16648				16823		16861		
	16254	16543	16651				16825				
	16255	16544	16652				16863				
	16373	16620	16657				16864				
AHC/T Advanced High-Speed CMOS	16244	16245	16373	16374							
LVC Low Voltage CMOS	16240A	162244	16374A	16543							
	16241A	16245A	16540	16646							
	16244A	16373A	16541A	16652							
ALVC Advanced Low Voltage CMOS	H16240	164245	H16827		H16524	H16835	H16601		16260	H16344	H162820
	16244A	H16254			H16525	H16863	H162601		H162260	H16721	16821
	H16244	H16373			H162525	H16901			H162268	H162721	16827
	H162245	H16374			H16821	H16500			16269	HR162409	162827
	H16245	H16543			H16825	H16501			HR162269	H16409	H162721
	HR162245	H16646			H16823	H16600			16270	H16820	H16841
LVT Low Voltage Technology	16244A	16373	16952			16500	182502		18504		
	162244	16374				16501			182504		
	16245A	16543				16835					
	162245	16646				18502					

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The offer of Widebus™ functions comprises more than 160 devices.

The excellent electrical behaviour of Widebus™ packaging is used for devices operating from 5V and 3V supply voltage.

For 5V families TI offers ABT and AC as well as some functions of the new AHC family.

For 3.3V supply voltage Widebus™ is available for LVC, ALVC and LVT.

Widebus+™ supports up to 36 bits within one single package.

Nomenclature: SN74 FAM H 16 2 xxx A DL ,

FAM = Logic family H (optional) - BusHold-feature,

16 - Widebus™ ,18 - Widebus™ with JTAG

32 - Widebus+™ 2 - Series damping resistor

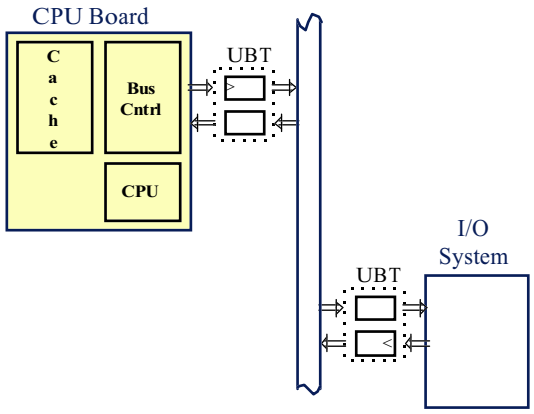
A - Die Revision DL - Package

Digital Design Seminar

Special Products (Example): UBT™

A flexible Bus Interface Concept (Universal Bus Transceivers)

- ✶ UBTs can replace nearly all common bus interface logic parts (‘245, ‘543, ‘2952, etc.)
- ✶ Clocked storage "out" Latched or Transparent "in"
- ✶ Shortens time to market with common t_{su}, t_h and min times



Device	UBT™ Part Types *
‘ALVC16409	9-bit 4-Port
‘ABT’/‘LVT16500 ‘ALVC16500	18-bit, Neg Clock
‘ABT/‘ALVC16600	18-bit, Neg Clock w/CLKEN
‘ABT’/‘LVT16501 ‘ALVC16501	18-bit, POS Clock
‘ABT’/ALVC16601	18-bit, POS Clock w/CLKEN
‘ALVC16901	18-bit, w/parity generator/checkers
‘ABT32501 ‘ABT32316 ‘ABT32318	36-bit, POS Clock w/CLKEN 16-bit, Tri-Port 18-bit, Tri-Port

* Series damping memory driver options available

UBT is a trademark of Texas Instruments Incorporated

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Many high performance applications require more than one mode for accessing their system bus, because different parts of the system have different data access and processing speeds. While some may be able to work in transparent mode (fully synchronous to the data source), others will require data to be latched, to meet setup and hold time requirements. When designing CPU access to the bus, clocked storage is the easiest method.

UBT™’s are bi-directional transceivers that can be configured as

★transparent,

★data-flow-through transceivers (e.g. ‘245 function),

★latch-enabled transceivers (e.g ‘543 function) ,

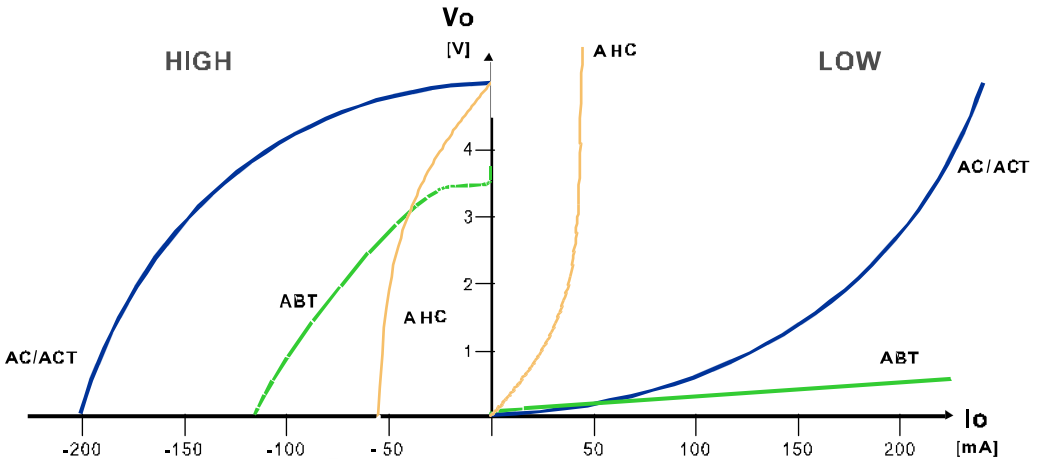
★clocked registered transceivers (like the‘646er function),

★and clock-enabled registered transceivers (like the ‘952er function).

Designed specifically for workstations bus-interface applications, the UBT™ is perfect as an interface to many different microprocessor architectures and system backplane specifications available. It may also be a cost effective alternative to several different interface functions, purchased in low volumes.

Digital Design Seminar

Advanced 5 V Logic
Output Characteristics (Drive capability)



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The curves show the drive capability in the logic 'high' and 'low' - states for various logic families.

The steeper the H- (L-) curve, the higher the drive capability.

To be noticed: ABT is a BICMOS family and delivers TTL levels at their outputs

(typical output high: 3.6 V).

These curves can be taken as base for the graphical calculation of over- and undershoots of a certain family.

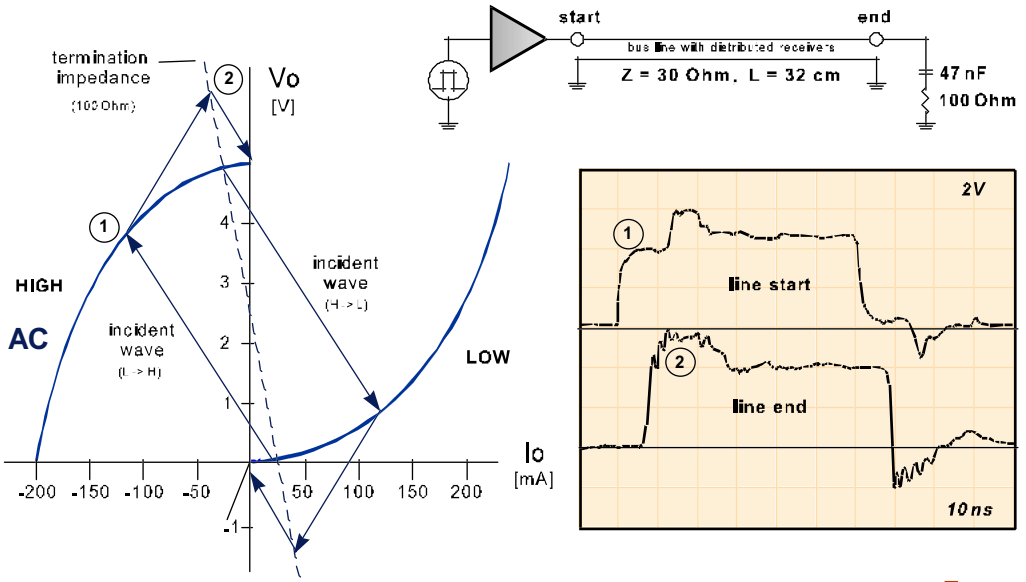
For the Bergeron method, as mentioned earlier, two more parameters are necessary:

the **line impedance** and the value of the **line termination resistor**.

An example is given on the next page.

Digital Design Seminar

Low-Impedance Line Driving with Advanced CMOS



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As example for the graphical Bergeron method a low impedance line is evaluated.

The setup is as follows: A line driver AC is connected to a line which impedance is Z0= 30 Ohm, the length of the line is 32 cm. The line is terminated with 47nF in series with 100 Ohm. The generator delivers a digital signal, duty cycle 50%.

The first step to solve this problem graphically is to choose the output characteristics of the AC driver.

The termination resistor of the setup results together with the duty cycle (50%) in the dashed straight line. The line impedance results (Z0) in the steepness of the progressing waves (solid arrows).

Each crossing of Output characteristic and the solid arrow can be recognized as voltage value at the begin of the line (Output driver).

Each crossing of termination curve and the solid arrow can be recognized as voltage value at the end of the line (termination resistor)

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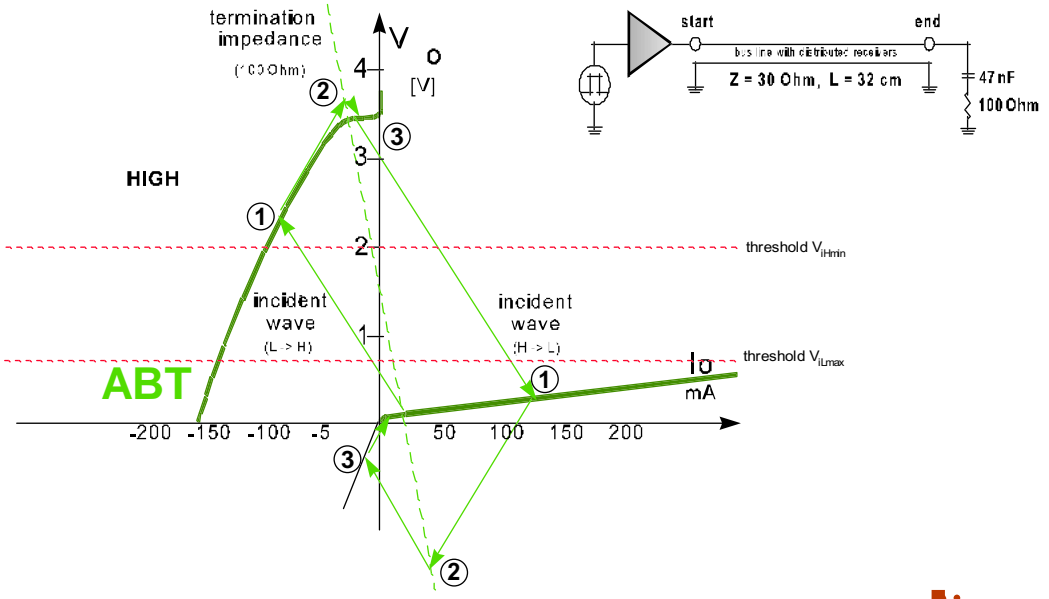
Low-Impedance Line Driving with Advanced BiCMOS



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For the same set-up as before, the Bergeron method is applied, using an ABT device instead of the AC driver.

The graph shows that again with the 1.wave a change of the logic level is ensured.

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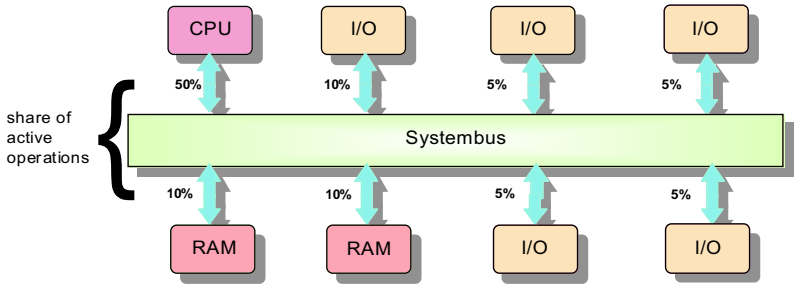
Static Power Consumption
Application Example



5 V				in Application	3 V			
ABT245	74F245	ALS245	A(H)CT	Family	LVT245	LVC245	ALVC245	LV245
7.5 mA	106 mA	54 mA	0.02 mA	1 x Icc(50%)	3.1 mA	0.01 mA	0.02 mA	0.01 mA
4.5 mA	318 mA	114 mA	0.012 mA	3 x Icc(10%)	1.8 mA	0.006 mA	0.012 mA	0.06 mA
3.0 mA	424 mA	230 mA	0.008 mA	4 x Icc (5%)	1.2 mA	0.004 mA	0.008 mA	0.004mA
15 mA	848 mA	398 mA	0.04mA	Icc tot	6.1 mA	0.02 mA	0.04 mA	0.02 mA
5 V	5 V	5 V	5 V	Vcc	3.3 V	3.3 V	3.3 V	3.3 V
1	56.5	26	0.03	Factor (Vxl)	0.25	0.00075	0.0015	0.00075
3.9	7	10	7	tpd max	4	6.5	2.9	14

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This foil shows an application example in a computer system.

CPU, RAM and I/O ports are connected via a bus. The percentage value shows the share of activity on the bus (e.g. the CPU uses the bus for 50% of the time). If we assume that all components used for this application are taken from the same family and set up four identical systems, we can compare the performance of those systems.

The 74F family uses the highest power consumption for the application. This family is made in bipolar technology and consumes in tristate the same current as during active operation. Also the propagation delay time is the slowest with 7 ns.

ABT has improved performance in both: power consumption and speed. ABT devices are made in BiCMOS Technology. During tristate-mode the power consumption is decreased down to 190 microamps. The speed is increased by 44% against the 74 F family.

A comparison with ALVC shows that only 0.15% of the ABT power consumption is used by ALVC. Also the propagation delay is improved to a value of T_{pd}=2.9 ns.

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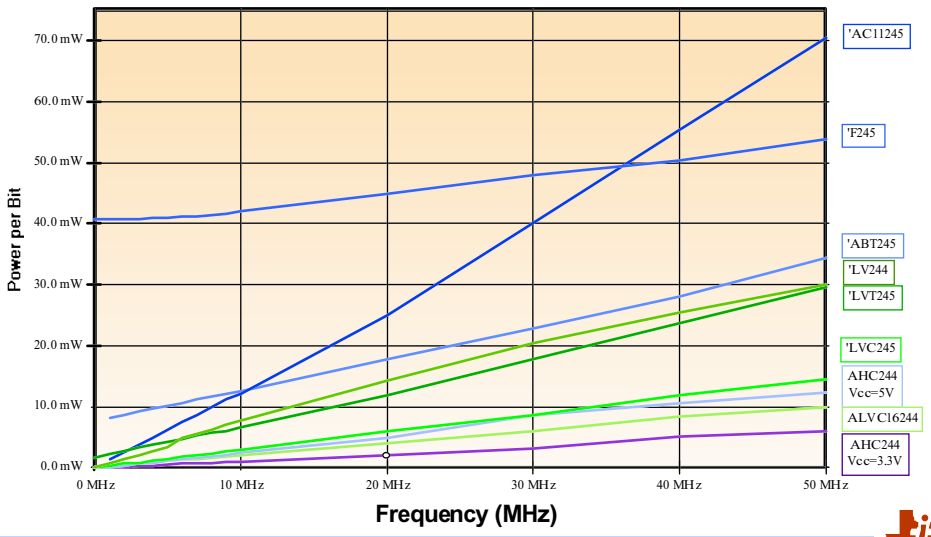
Logic Families:
Power vs Frequency Comparison

'245/'16245 TYPE; SINGLE OUTPUT SWITCHING; C_{Load} = 50 pF



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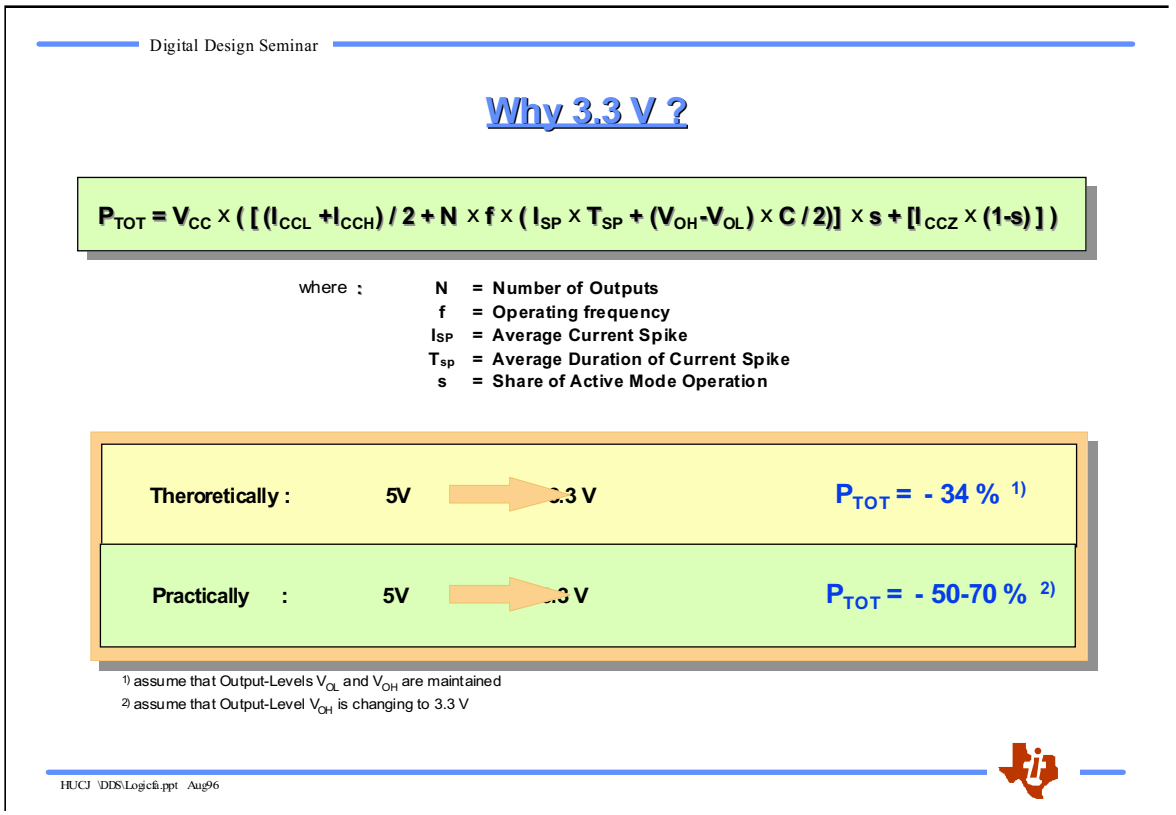
This foil shows the dynamic power consumption of different 5V and 3.3V Logic families.



The answer to the question : ”Why 3.3V” is given by the formula for determination of the power consumption related to logic circuits .

A logic circuit’s total power consumption, P_{TOT}, is strongly influenced by a number of parameters. If we investigate this formula, we can split this into two parts:

1) V_{CC}

2) the ‘rest’ , which is determined by various parameters such as number of outputs,
frequency, average current spike, etc.

Some are inherent to the technology, like the static I_{CC} currents and the so-called “current spike” (I_{SP}), that flows across the output during circuit switching. Others depend on load conditions, operating frequency, and so on.

However, the parameter with the most significant effect on the overall power consumption, is V_{CC}.

The theoretical saving of power dissipation is 34%, if you reduce the voltage from 5V down to 3.3V.

Practically, the power saving will be about 50-70%, because other parameters, like current spikes, are also improved by reducing the supply voltage.

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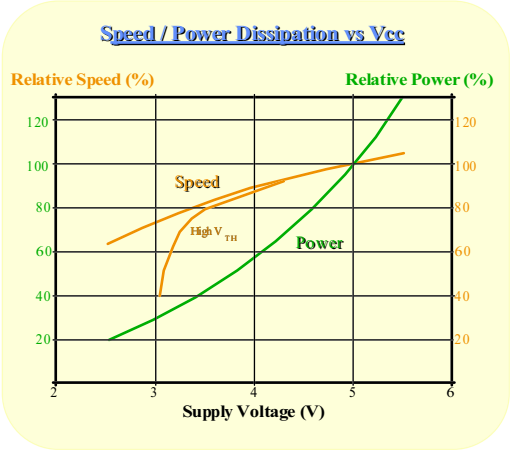
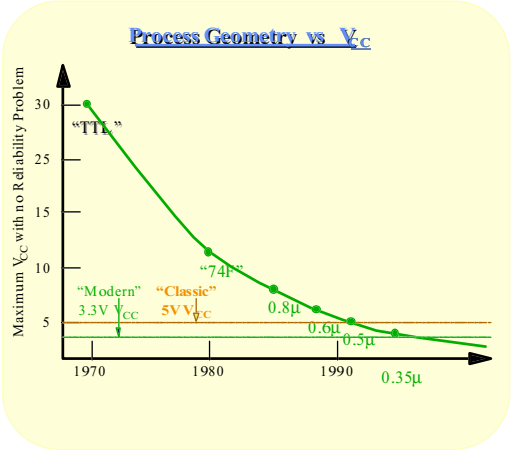
2 Factors driving Lower Voltage

1. Power Dissipation
2. Process Geometry





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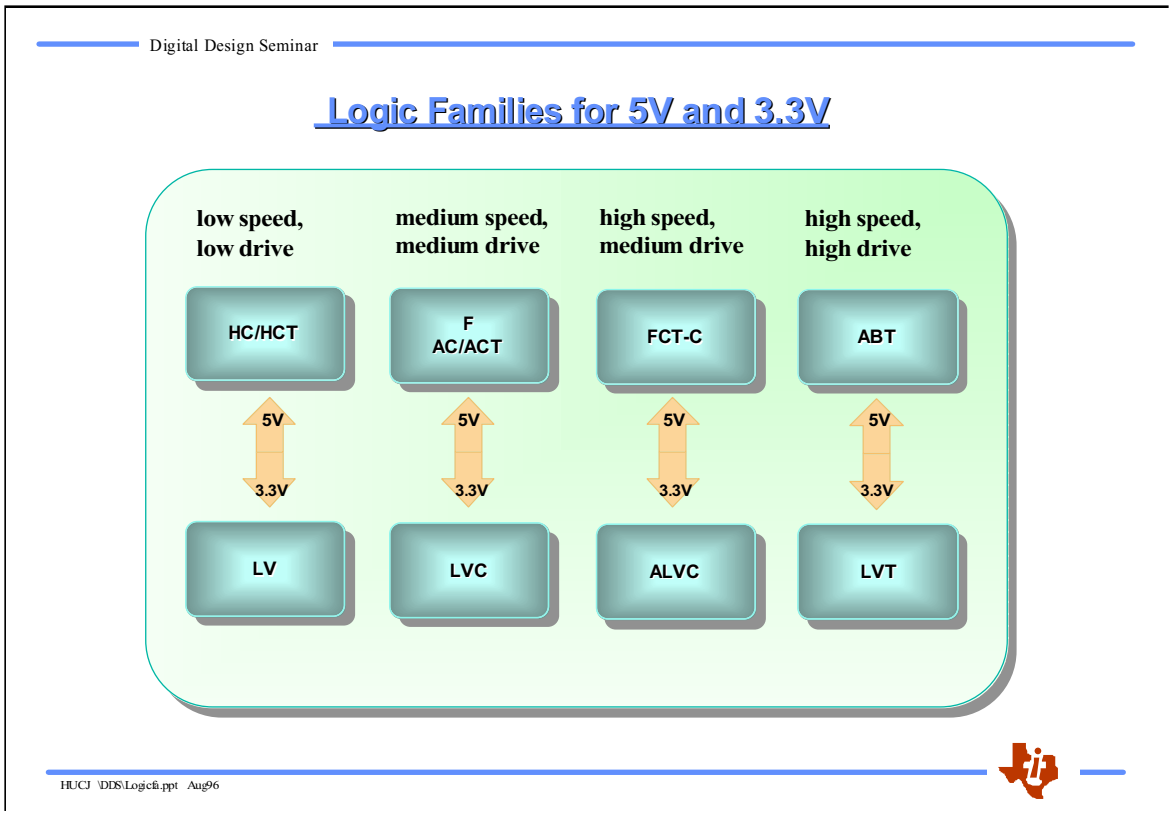
Migrating a system's V_{CC} from 5V to 3.3V by reducing a circuit's supply voltage will deteriorate its speed performance. However, as the left figure shows, the relative speed performance loss is much lower than the improvement in power consumption.

Practically, most system designs do not allow for any speed degradation. The way out for suppliers is to use process technologies with smaller feature sizes that (often even over-) compensate the speed loss. This results in the availability of 3.3V logic families that offer the same or higher speeds than the 5V families they replace, in combination with a drastic reduction of the power consumed.

The significant improvement in power consumption is only one reason why there is such a strong momentum in the industry to migrate towards reduced supply voltages.

Another strong push to reduce V_{CC} is driven by the accelerated use of small process geometries. Advanced microprocessors or ASICs sometimes employ several millions of transistors. This demands process feature sizes of 0.5 micron and below. Unfortunately, such small process geometries start to show reliability problems, if operated with a 5V supply voltage. Some types of equipment, e.g. industrial control systems, are therefore frequently forced to change their V_{CC} to 3.3V, although their operating environment would still allow for the high power consumption of 5V designs.



Texas Instruments' Low Voltage Logic families have been designed to provide a performance that is at least equivalent to, but usually even better than, that of commonly used 5V devices.

If you are in the situation to design a new application with 3.3V logic, but are only familiar with the performances of the 5V logic families, this foil will help you.

LV is somewhat comparable to the well-known LS and HC/HCT families, but features improved speed.

LVC addresses the medium performance range, where families like F or AC are predominant in 5V applications.

Two different solutions are available for high performance 3.3V system design:

ALVC combines medium output drive with very high speed performance (unmatched by any other 3.3V logic family).

LVT, which is the 3.3V equivalent to the 5V ABT family of bus interface devices, combines speed with a drive capability that is high enough for reliable operation of large backplanes.

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LVT / LVC / ALVC / LV Comparison

Product Family	SN74LVT	SN74LVC	SN74ALVC	SN74LV
Speed ['245 type]	tpd(typ) = 2.4ns tpd(max) = 4.0ns	tpd(typ) = 4.0ns tpd(max) = 6.5ns	tpd(typ) = 2.1ns tpd(max) = 2.9ns	tpd(typ) = 8.0ns tpd(max) = 14.0ns
Drive	IOH = -32mA IOL = 64mA	IOH = -24mA IOL = 24mA	IOH = -24mA IOL = 24mA	IOH = -8mA IOL = 8mA
Current consumption	ICCH/Z = 190µA ICCL = 8.8mA	ICCH/Z = 10µA	ICCH/Z = 40µA	ICCH/Z = 20µA
Vcc range	← Vcc = 2.7 - 3.6 V →			
Temperature range	← -40 ... +85 degrees Celcius →			
Switching noise	← Ground-Bounce less than 800 mV →			
Package	SOIC / SSOP / TSSOP	SOIC / SSOP / TSSOP	SSOP /TSSOP	SOIC / SSOP / TSSOP
Price Similarity	~ABT	~AC	~FCT	~HC
Special user benefit	✶ Bus hold cells ✶ High impedance at power down ✶ Very low noise ✶ 5V tol. I/O	✶ Very low noise ✶ 5V tol. I/O ✶ Broad product spectrum incl. Gates/FF/MSI...	✶ Bus hold cells ✶ Very low noise ✶ pure 3.3 V	✶ Very low noise ✶ Specification at Vcc=5V available

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These four families of 3.3 V logic devices can be used for portable applications from electronic games up to high performance engineering workstations.

The LVT family is the only low voltage family using BiCMOS technology.

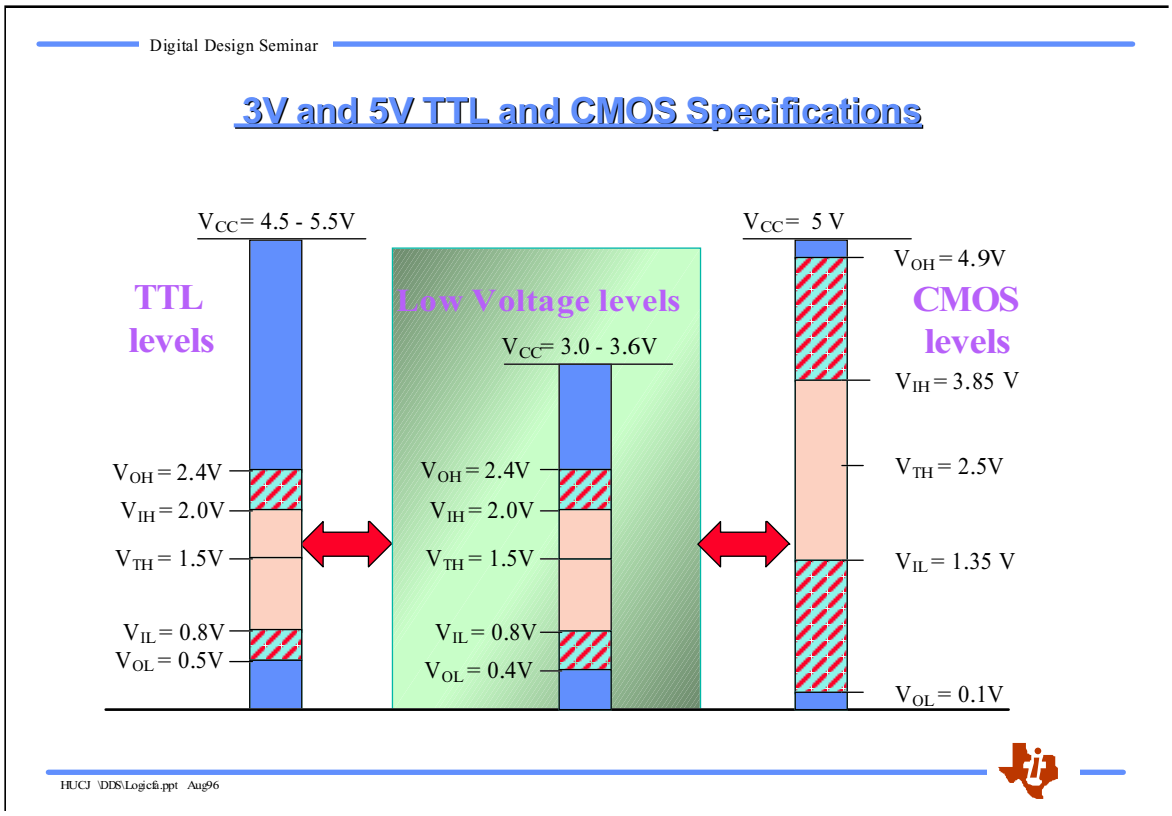
LV, ALVC and LVC families are manufactured in CMOS technology.

The LVC and the LV families are designed for low cost 3V Systems such as consumer equipment, portable computers, electronic games, toys, portable telecom equipment that require medium performance at low cost.

The ALVC family, with a typical propagation delay time of 2 ns has been designed to meet the requirements of high speed systems including engineering workstations and interfaces to SDRAM-modules.

The LVT family, with its high drive capability, can be used for Backplane/Bus Driving applications, high-performance engineering workstations, desktop-PC's and telecom transmission/switching equipments.

TI has second source agreements with Philips and Hitachi for all of these four Low Voltage Logic families. The agreement with Philips has recently been extended to cover other new logic families like ALVT and AHC.



Before discussing the special requirements of mixed mode designs (i.e. systems, where there is a need to interface between the 5V and the 3.3V part), we would like to briefly discuss the different voltage level specifications used in both environments.

During the development of the 3.3V specification in JEDEC, there were basically two “interest groups” endorsing slightly different proposals.

The LV-CMOS proposal was mainly targeted to mobile applications, where battery operation requires a V_{CC} min of 2.7V.

This proposal favoured a concept that basically copied the 5V CMOS one, i.e. an output voltage swing that almost equals V_{CC}, where V_{OL} ~ 0V and V_{OH} ~ V_{CC}. This would allow the proper operation of existing 5V CMOS devices from 3.3V (“Scaled CMOS”).

On the other hand, the LV-TTL proposal favoured V_O/V_I specifications that are identical with 5V TTL, such that interfacing the two worlds is greatly eased.

Fortunately, the final 3.3V specification agreed upon by JEDEC covers both proposals.

It specifies a 2.7-3.3V V_{CC} range, in which the max/min values of the logic input levels are identical with the 5V TTL spec (0.8/2.0V) and max/min values of the logic output levels are matching with the CMOS spec.

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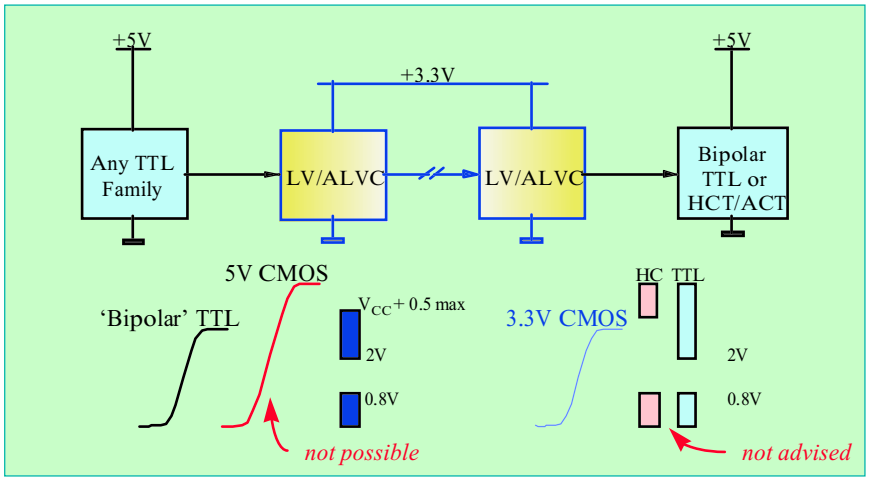
5 Volt 3.3 Volt Interfacing: LV and ALVC



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As has been explained on the previous page, both LV and ALVC do not allow input voltages to be any higher than V_{CC} + 0.5V.

However, this does not necessarily mean that these technologies are unable to interface with 5V signals.

If a 5V TTL signal is applied, its High level will typically be about 3.2V. This does not violate the LV or ALVC inputs specifications. One will have to make sure, however, that no overshoots can occur on the line which might again cause trouble.

On the output side, both LV and ALVC can directly drive 5V inputs that are TTL-compatible. No additional provisions will have to be made.

If the 5V receiver expects to see CMOS levels special 'Level-Shifter' are required.

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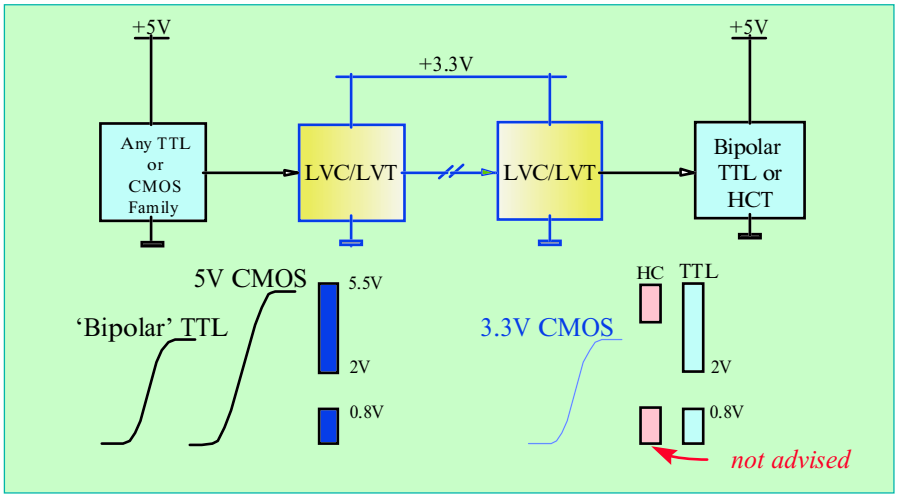
5 Volt 3.3 Volt Interfacing: LVT and LVC



- LVCxxxA and LVT devices allow direct interface from 5V TTL- and 5V CMOS - devices
- The direct interfacing to 5 V CMOS is not adviced

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Both LVC and LVT allow input voltages to go up to 6.5V.

It means that these technologies can interface directly to 5V signals. Care needs to be taken, however, when driving the inputs from a 5V CMOS device, as possible overshoots may lead to the maximum LVC/LVT input voltage being exceeded.

On the output side, LVC and LVT can again (like LV and ALVC) directly drive 5V inputs that are TTL-compatible. No additional provisions will have to be made.

If the 5V receiver expects to see CMOS levels special 'Level-Shifter' are required.

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5 Volt ⟷ 3.3 Volt Interfacing Capability

from \ to	SN74LVT	SN74LVC	SN74ALVC	SN74LV	5V CMOS (CMOS levels)	5V TTL, ACT/ HCT/AHCT
SN74LVT	✓	✓	✓	✓	use pull-up resistor to 5V	✓
SN74LVC	✓	✓	✓	✓	use pull-up resistor to 5V	✓
SN74ALVC	✓	✓	✓	✓	use Levelshifter '4245 or 164245	✓
SN74LV	✓	✓	✓	✓	use Levelshifter '4245 or 164245	✓ *
5V CMOS (HC/AC/AHC/..)	✓	✓	use input voltage devider	use input voltage devider	✓	✓ *
5V TTL (ALS/F/AS/..)	✓	✓	✓	✓	use pull-up resistor to 5V	✓
ACT/HCT	✓	✓	use input voltage devider	use input voltage devider	✓	✓ *

* limited by output drive capability of HC(T) , AHC (T) , LV

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Four different signal level constellations may have to be addressed in mixed mode design:

5V TTL → *3.3V TTL*
3.3V TTL → *5V TTL*
5V CMOS → *3.3V TTL*
3.3V TTL → *5V CMOS*

While the first two are very easy to address, the latter two often represent an issue, as a certain technology may not support their requirements. LVC and LVT have I/Os that are 5V CMOS-tolerant. Interfacing a 3.3V part to a 5V system that expects CMOS levels, however, usually requires a dedicated level shifter. CMOS levels are specified as follows:

$$V_{IL} = 0.3 \times V_{CC}$$
$$V_{IH} = 0.7 \times V_{CC}$$

The driver should at least be able to deliver:

$$V_{OL} < 0.3 \times V_{CCmin} = 1.35V \quad (\text{with } V_{CCmin} = 4.5V)$$
$$V_{OH} > 0.7 \times V_{CCmax} = 3.85V \quad (\text{with } V_{CCmax} = 5.5V)$$

This also implies that a standard 3.3V output does not deliver a high enough output voltage to reliably drive 5V CMOS inputs.

Even with a pull-up resistor

$$V_{Omax} = V_{CCmin} + 0.7V \text{ (diode)} = 3.7V < 3.85V$$

the result is the following: special '**Level-Shifter**' are required.

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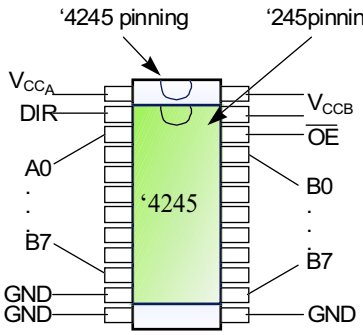
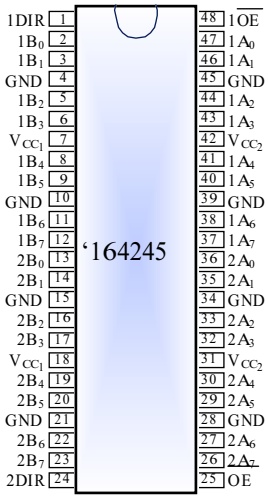
Special Level Shifters: 'LVC4245 and 'ALVC164245



The dual V_{CC} level shifters ALVC164245 and LVC4245 have 3.3V and 5V V_{CC} pins (dual V_{CC})

In this way, a full mixed mode system can be designed.



This solution is compatible to a 3.3V-only system: Both can be replaced later with 3.3V parts without PCB redesign

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Certain applications will require 'Level-Shifter' between 3.3V and 5V that are able to provide 5V output signals. Examples are:

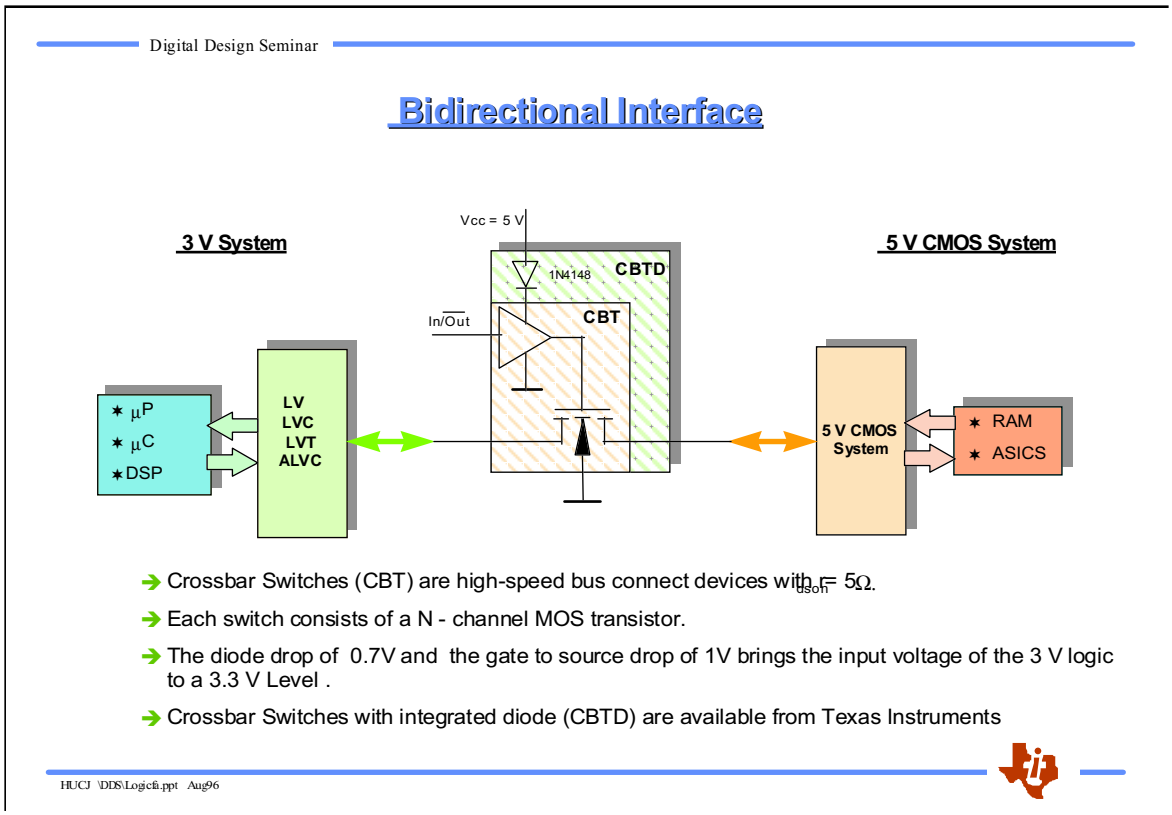
1) interfaces to 5V CMOS-level devices which, as shown on the previous page,
cannot be operated reliably from 3.3V outputs, or

2) 5V memory modules that should be connected to 3.3V components.

In the latter case a designer might want to provide a true 5V input signal to the memory, even if it has a TTL-type input, as the memory circuit's current consumption will otherwise be increased.

In these cases a dual V_{CC} level shifter will be required. This is a device that is connected both to the 5V and the 3.3V supply voltages such that it can independently access to and interface between both sides.

Here are two level shifter examples. The LVC4245 is an 8-bit version and the ALVC164245 is a 16-bit version, both with true 5V ↔ 3.3V level translation. Both devices are being or will be offered by Texas Instruments.



Crossbar Technology (CBT) Switches

If a device with the capability to switch bus signals -on or -off is needed, then TI's CBT devices can be used to support easy bus communication.

CBT devices serve a number of unique applications in PC, Workstation, Bus Board, Telecom, Industry and Hard Drive end-equipment markets.

A CBT switch consists of a simple n-channel MOS transistors. When the switch is open, it provides isolation (3-state) for the bus line. When the switch is closed, it imposes a near-zero propagation delay on the line (250 ps).

In multiprocessor systems, CBT can be used for extremely fast bus connections, bus exchanges in crossbar systems, memory interleaving, bus byte-swapping and a variety of other switching functions. CBT switches also serve as 5-V to 3.3-V bus translators, helping designers to mix devices of different voltage levels in the same system.

Crossbar Scwitches with integrated diode (CBTD) are available from Texas Instruments.

Extremely low propagation delays of 250 ps make CBT devices an effective replacement for drivers and receivers in high-speed systems, where signal buffering is not required.

In addition, low power consumption helps improving battery life between charges in portable systems. Small-foot-print packages save board space in most applications.

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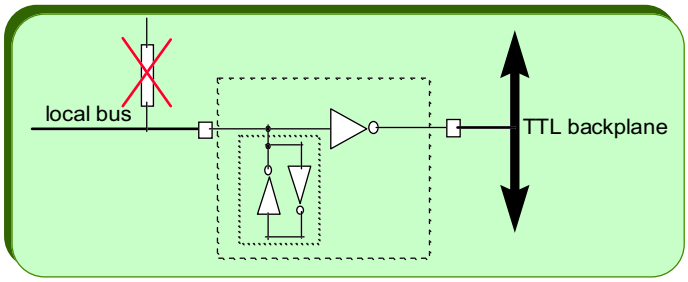
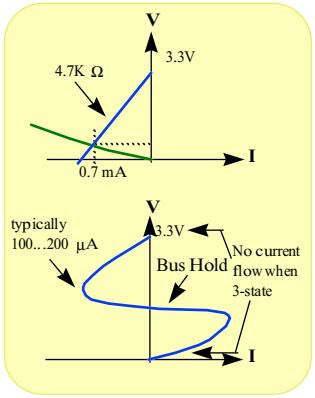
Bus Hold Input Characteristic





- Holds the last known state of the inputs
- Provides for +/- 74µA of holding current at 0.8 and 2.0V
- Bus Hold current does **not** load the driving output at a valid logic level
- Negligible impact to input/output capacitance (0.5pF)
- Eleminates the need for external resistor on unused or floating I/O pins
- Reduces the number of passive components per board
- Implemented in LVT,ALVC,selected LVC's and ABT's functions

Bus Hold nomenclature : SN74xxxHxxx; e.g. SN74LVCH245

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TI has addressed many important design issues including testability, memory driving, bus termination, low skew requirements, and low-impedance line driving with specialized, advanced logic devices that improve overall system performance.

This figure shows the typical V-I characteristics of a bus line with pull-up resistors versus a bus line using a bus interface device with integrated bus hold. The bus hold circuit basically consists of a non-inverting driver that will drive a small current (typically peak value is about 100-200 µA) back into the bus, to pull it back to proper signal levels, if the bus is floating.

As can be seen, the pull-up solution causes a constant current to flow on both ends. The bus hold circuit, on the other hand, not only consumes much less current, but also does not represent any static loading to the bus. This means that it will not consume any current, as long as the bus is at a proper Low or High level.

The Bus Hold feature has been implemented in the LVT and ALVC family as well as in selected LVC and ABT functions.

Look for the 'H' within a device nomenclature.

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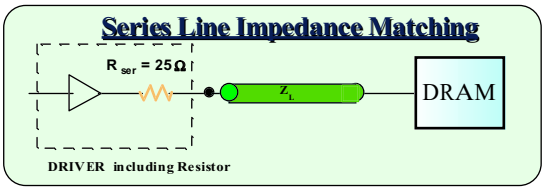
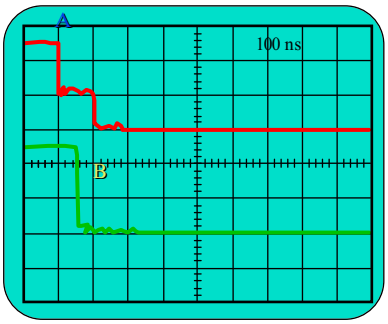
Series Termination - Devices





- Avoids under- and overshoots by matching the output impedance of the line driver to the line impedance. Power dissipation is not increased (recommended in CMOS systems).
- Preferable solution for point-to-point connects or to drive 'concentrated' loads, e.g. address lines of memory arrays.
- Integrated solution: logic devices with series output resistor (e.g. LVT16244).

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One special line termination technique is the so-called Series Termination.

As opposed to most other termination techniques (where the lines are terminated at the end), the method used here is to match the driver output impedance with the line impedance by adding a series resistor. This means that no reflection will occur on the driver side. As the oscillogram shows, this will result in a step function in the signal waveform on the driver side but a very clean signal transition on the receiver side. It is thus a very efficient method when designing a point-to-point connection or a line driving a concentrated load. This technique is especially useful when driving memory array address lines as it suppresses signal under- and overshoots which may otherwise lead to data losses.

Several 3.3V logic devices are also available with an integrated output resistor. The resistor value is typically around 25Ω, leading to an effective output resistance of about 30Ω. As a certain impedance mismatch is acceptable, these circuits will be feasible for line impedances up to approximately 75Ω.

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Series Termination - Devices

- Series Resistor at Outputstage
- Short propagation delays & low power consumption
- Supports highest system performance and use of slower memories
- Reduces component count, board space, mounting costs

Function	Decription	Family				Function	Decription	Family			
		ABT	LVT	ALVC	LVC			ABT	LVT	ALVC	LVC
'2240	8- bit mem. drv.	✓				'162245	16- bit mem. drv.	✓	✓	✓	✓
'2241	8- bit mem. drv.	✓				'162260	12-to 24- bit mem. drv/mux	✓			
'2244	8- bit mem. drv.	✓			✓	'162460	4 to 1 bit mem. drv/mux	✓			
'2245	8- bit mem. drv.	✓			✓	'162500	18-bit memory UBT™	✓			
'2827	10- bit mem. drv.					'162501	18-bit memory UBT™	✓			
'2828	10- bit mem. drv.					'162601	18-bit memory UBT™	✓		✓	
'5400	11- bit mem. drv.	✓				'162820	10-bit FF w dual Output	✓			
'5401	11- bit mem. drv.	✓				'162823	18-bit Bus Interf. FF	✓			
'5402	12- bit mem. drv.	✓				'162825	18-bit mem.drv	✓			
'5403	12- bit mem. drv.	✓				'162827	20-bit mem. drv.	✓			
'162244	16- bit mem. drv.	✓	✓	✓	✓						

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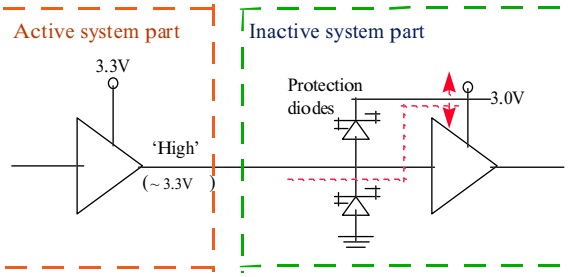
Potential Problems in Live Insertion Applications

- Unexpected device behaviour during power up or power down causes malfunction
- Input signals start sourcing circuitry through input protection diodes



Along with the power reduction trend that drove the transition to 3.3V, live insertion has become of much more interest in system design. Also, so-called "partial power down" is being applied more frequently, where the supply voltage V_{CC} will be switched off in certain parts of the system, while these are not in use.

In both cases (live insertion and partial power down), there are two potential problems that need to be addressed. First, there is a risk of unexpected device behaviour during the power transition. All logic circuits available in the market have specifications that guarantee proper circuit operation only within a certain V_{CC} range. During power up or power down, the circuit will be operated outside this range, which may lead to an unpredictable device response. For example, the output may start sinking large currents or, worst case, even start oscillating.

Second, the block diagram shows a constellation, where an active device output is connected to a device, whose V_{CC} has been switched off. In this special case, the inactive circuit uses protection diodes as its inputs. This method is being used in many CMOS circuits for ESD protection. Unfortunately, a High signal applied to this input will be fed to the circuit's V_{CC} connection via the protection diode. The V_{CC} level of the inactive circuit will be about 3.0V, which is high enough to activate this circuit and (via the V_{CC} path) the remaining devices in the inactive system part. This may result in all kinds of unexpected system behaviour.

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Live Insertion Support Aspects of Logic Families

	HC/ HCT	AC/ ACT	ALS/ F/AS	ABT	LV	LVC/ ALVC	LVT
Diode connects Inputs to V_{CC} if V_{CC}=0V	✗	✗	-	-	✗	-	-
Diode connects Outputs to V_{CC} if V_{CC}=0V	✗	✗	-	-	✗	-	-
V_{CC} above which the circuit will typically work*	1.5V	2V	3.5V	2.5V	1.5V	2V	1.8V
Outputs will be tri-stated below this limit				✓			✓

* Circuit will be functional but may still be outside AC specifications

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This table illustrates the feasibility of using certain logic families for live insertion applications.

As can be seen, the 5V families HC/HCT and AC/ACT, as well as the 3.3V family LV, will be difficult to use in any live insertion applications. This is mainly, because they all use protection diodes that connect the inputs and outputs to V_{CC}.

Those families that do not use protection diodes to V_{CC} will be easier to design with. However, only 5V ABT and 3.3V LVT circuits feature full live insertion support, as they also comprise a “power up 3-state” circuitry that will 3-state the device outputs, if V_{CC} is below a certain limit. A system designer can thus easily design interfaces that allow reliable power down operation.

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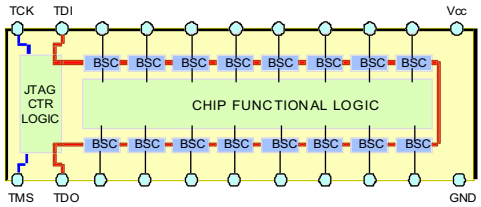
Texas Instruments IEEE 1149.1 Products

Boundary scan products allow easy test of high-density boards

- ✶ SCOPE™ bus drivers support most applications demanding boundary scan functions
- ✶ Path support functions allow easy handling of scan path's in large systems



IEEE1149.1 was developed by the Joint Test Action Group (JTAG)

SCOPE (System Controllability Oberservability Partitioning Environment) is a trademark of Texas Instruments Incorporated

Benefits using IEEE1149.1

- ✶ Test node access on high-density board
- ✶ Inexpensive test adapters
- ✶ Std interface for ICs, boards, systems
- ✶ Easy to implement in ASICs
- ✶ Broad spectrum of bus driver functions
- ✶ 3.3-volt drivers already on the market
- ✶ Support from IC and ATE vendors

Product features

- ✶ State-of-the-art technics used
- ✶ Popular bus driver functions available
- ✶ 3.3-volt versions
- ✶ Universal-Bus-Transceivers available
- ✶ Functions for large systems available

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ScopeTM products from Texas Instruments are compliant with the IEEE1149.1 specification.

Scope products are offered in BICMOS technology (ABT and LVT) and Advanced CMOS (ACT).

The nomenclature includes an '8' to express its testability feature (e.g SN74ABT8245, which is a 245er function additionally supporting the testability (IEEE1149.1).

The widebus devices including this feature can be recognized with the '18' instead of the '16' (e.g SN74.LVT18502).

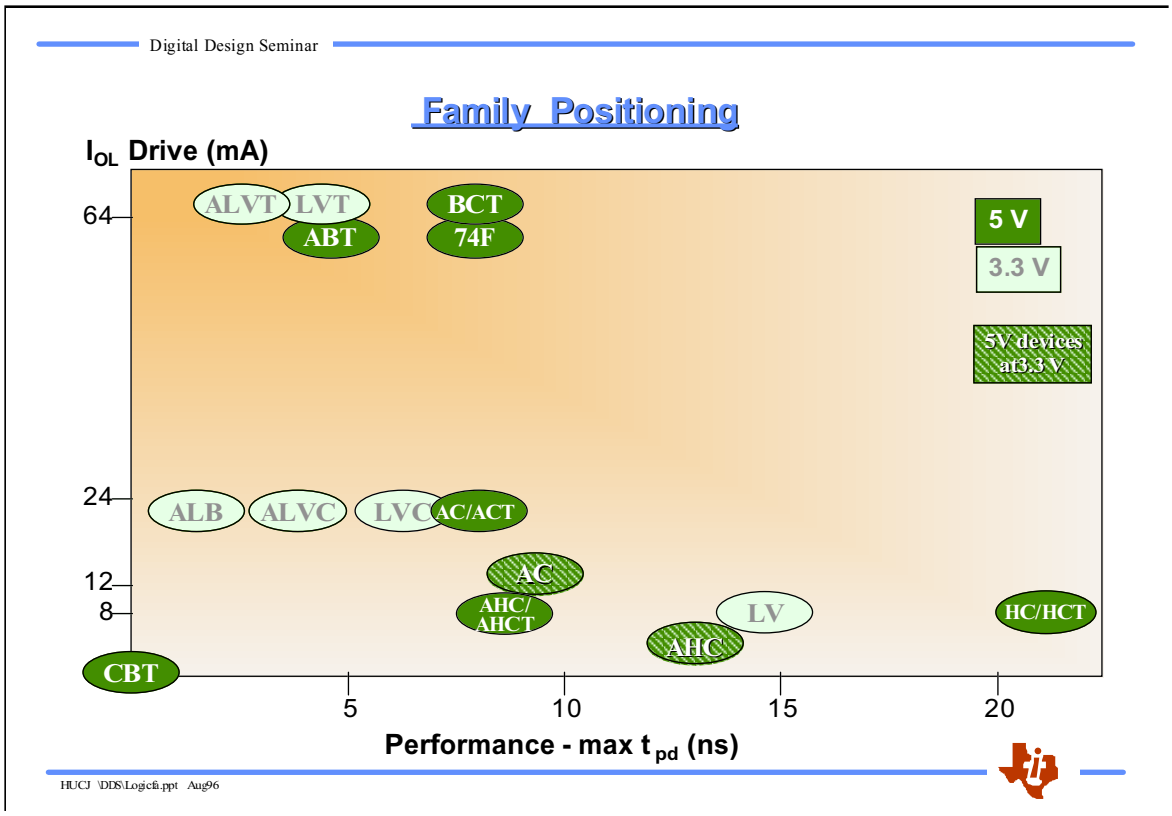
The generic IEEE1149.1 function:

Between each IC pin (input and output) and the chip functional logic there is a boundary scan cell (BSC).

All BSCs are connected to a serial scan path with the function of a shift register.

The BSCs are to be controlled via 4 control pins: TCK (test clock), TMS (test mode select), TDI (test data input), TDO (test data output).

The BSC allows capturing data from and providing data to the chip data path.



In an I_{OL} vs t_{pd} positioning, the 3.3V families (ALB, LV, LVC, ALVC, LVT and ALVT) and the 5V logic families (ABT, AC/T, AHC/T and CBT) cover the whole range of required performance nodes.

For reference, 5V families (AHC and AC) are also shown with their performance parameters, when operated with 3.3V.