Section 2

Data Conversion

NOTICE

This presentation is a single chapter from the 1996 Mixed Signal Products Seminar.

This presentation includes notes which can be read in the notes page view.

Texas Instruments

MSP Seminar

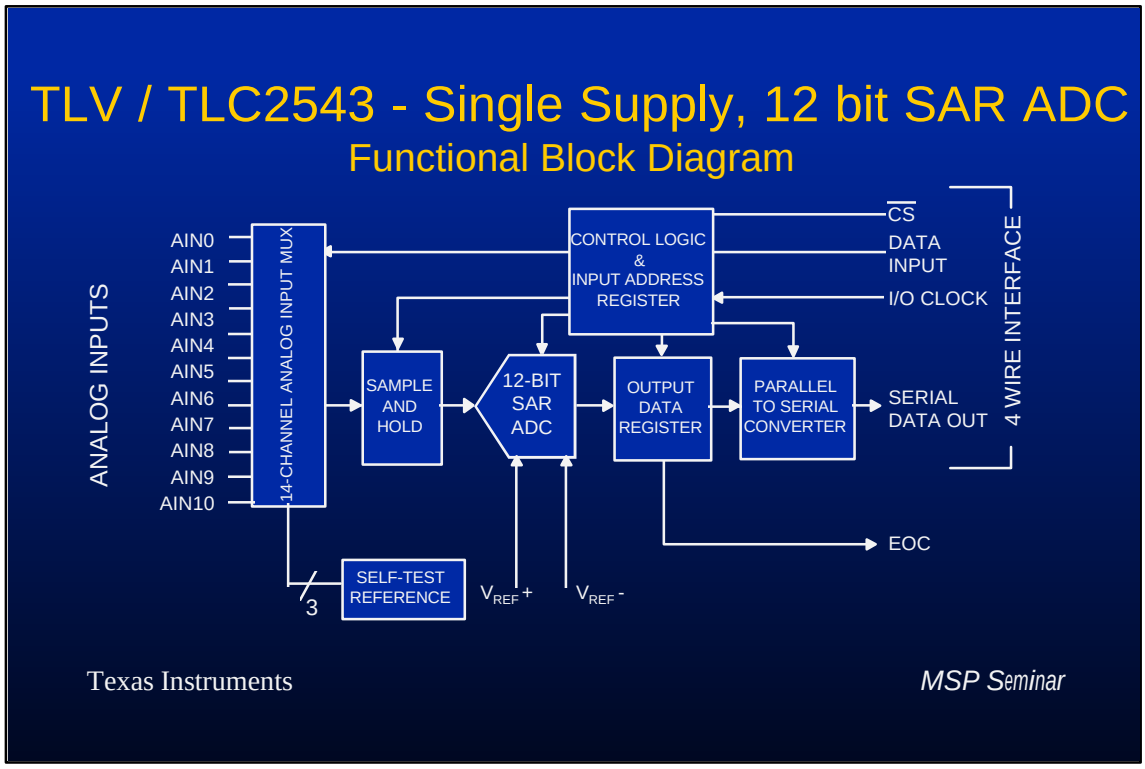


Figure 2-7 TLV2543 - +3V Supply, 12 bit ADC - Functional Block Diagram

TLV/TLC2543

The functional block diagram of the TLV/TLC2543 is shown in Figure 2-6. It includes an analog multiplexer which allows any one of 11 inputs to be selected via the serial data I/O bus. This SAR ADC offers an on-board sample-hold, on-chip system clock and a programmable power-down mode as well as numerous other programmable features.

This single-supply SAR ADC operates at a very low power (1 mA typical, 2.5 mA max) while delivering 12-bits of resolution at a 66 KSPS throughput rate. A software-programmable power-down mode enables the device to only consume a maximum of 25 µA (4 µA typical) of current. This allows for a reduction in power when A/D conversion are not needed without requiring the cost of an extra pin on the device. A built-in 14-channel MUX provides inputs for up to 11 single-ended analog input signals plus three internal test modes. The onboard conversion clock further simplifies system design. This high level of functionality and system integration assures the lowest possible total system cost for a 12-bit data acquisition system. Its generic serial interface provides an easy interface to virtually all types of processors equipped with a 4-wire serial interface. It is available in both 3V (TLV2543) and 5V (TLC2543) versions.

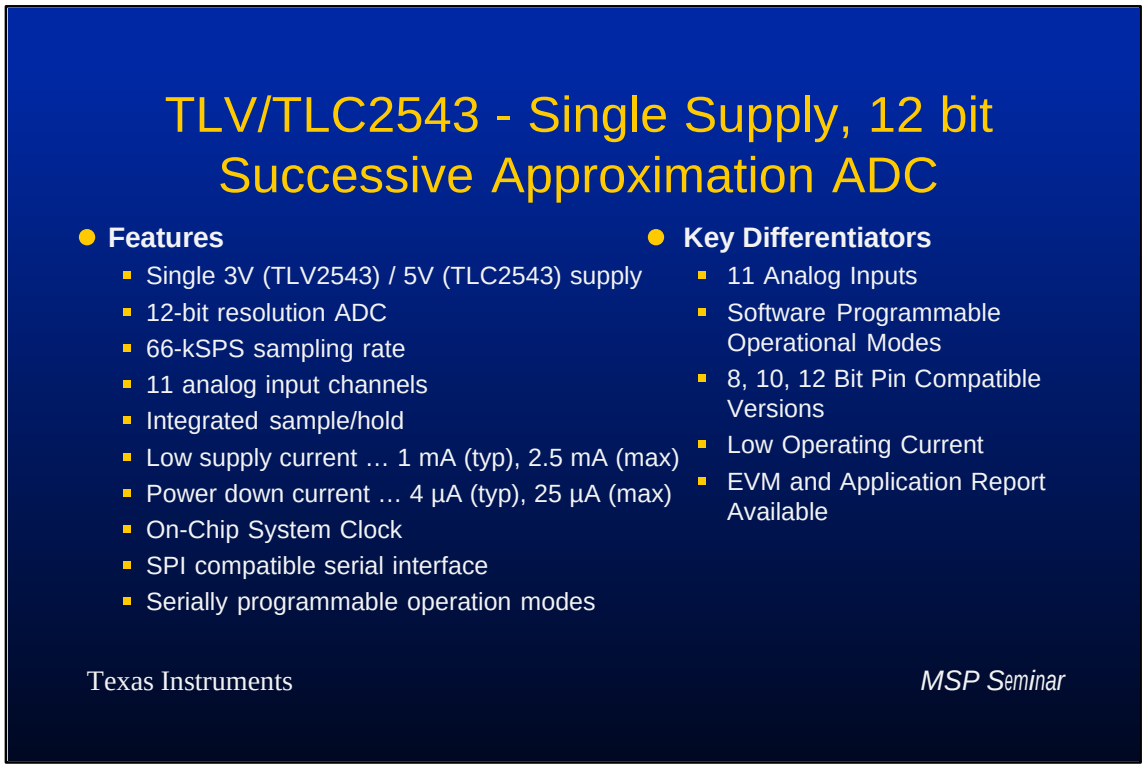


Figure 2-8 TLV/TLC2543 Single Supply, 12-Bit SAR ADC

TLV/TLC2543

The TLV/TLC2543 also maximizes the design/manufacturing flexibility by offering the same pinout for 8, 10 and 12 bit pin-compatible versions (TLC542, TLV/TLC1543 and TLV/TLV2543 respectively). This compatibility can be used to easily upgrade an existing 10-bit design using TLV/TLC1543 with the 12-bit TLV/TLC2543. Or if after completing system integration, it is determined a 10 bit ADC is acceptable, a more cost effective 10 bit version (TLC1543) can be used in production. Manufacturers will be able to build a family of products with different price points comparable to each feature set based on a single platform or to offer upgradability to a higher performance later on.

Battery powered process monitoring and testing can be implemented with this low-power low-cost high-performance ADC to achieve longer battery life. Next generation PDA and cellular phone manufacturers that require higher quality pen digitizer interfaces can benefit from the small SSOP package and lots of input channels available for temperature, battery voltage, panel brightness and the management of other system variables. Other applications include pixel conversion in color printers, offset adjust in instrumentation, datalogging and many many others. The TLV/TLC2543 is available in 20-pin DIP, SO and SSOP packages.

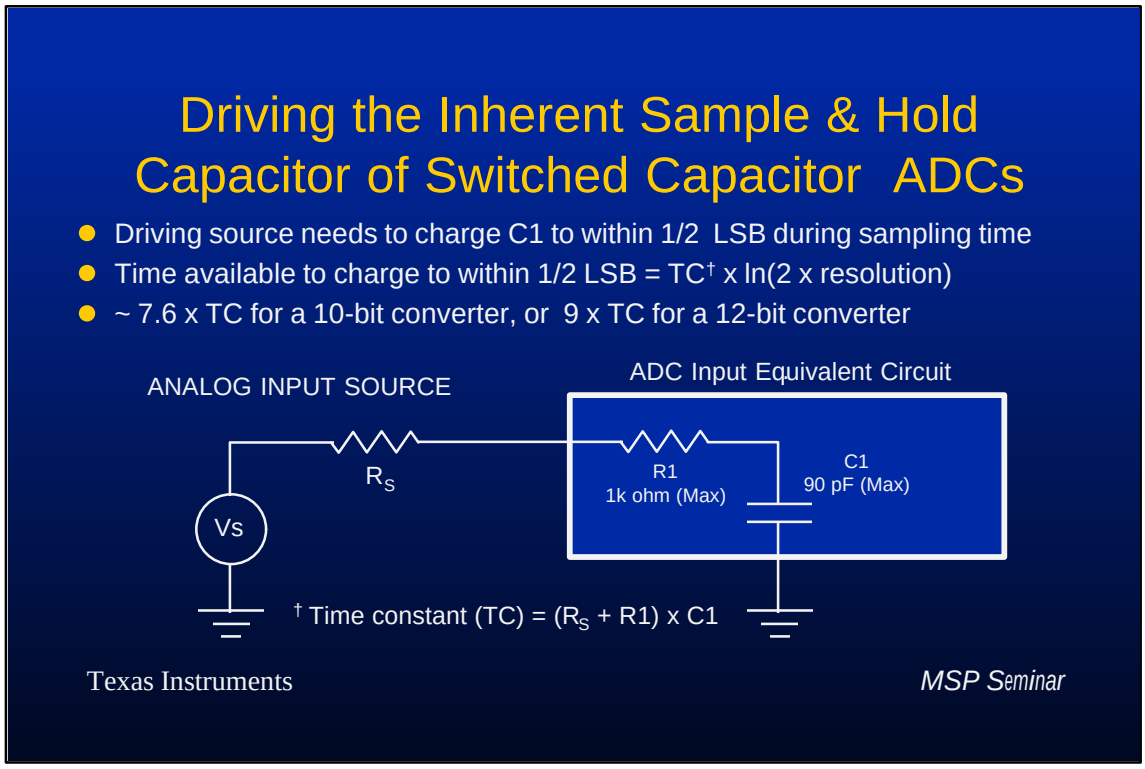


Figure 2-9 Driving the Input of a Switched Capacitor Filter

Switched Capacitor ADCs

Switched capacitor ADCs offer an inherent sample-hold function at their input. This avoids the need to provide an external sample-hold but care should be taken to ensure that sufficient time is allowed during the sampling phase of the conversion process to allow for the input sample-hold capacitor to charge up to the required level of accuracy.

The minimum time required for charging to a particular level of accuracy is calculated as shown in Figure 2-9. If the sample period needs to be extended due, for example, to increased source impedance, this can be achieved by slowing down the I/O clock of the ADC. Unfortunately this will also have the effect of increasing the data transfer time. The small (90 pF) sample and hold capacitor allows a relatively high source impedance to be used.

For instance with the TLC2543, 8 clock cycles are required for sampling. If the I/O clock is run at 1 MHz this gives an available charging time of 8 µs. To charge to 0.5 LSB will require 9 time constants for a 12 bit ADC. Therefore:

charging time = TC * 9, where charging time is the I/O CLK period * 8

TC = charging time / 9 = C1 (Rs + R1). Solving this for Rs:

Rs = (charging time/ (9* C1) - R1

Rs = 8 µs / (9 * 90 pF) - 1K = 8.9 kΩ maximum source impedance.

This foil highlights that the inherent sample and hold for TI Switched-Capacitor SAR ADCs is quite easy to use. The key is to control the source impedance well enough to drive the 90 pF capacitor.

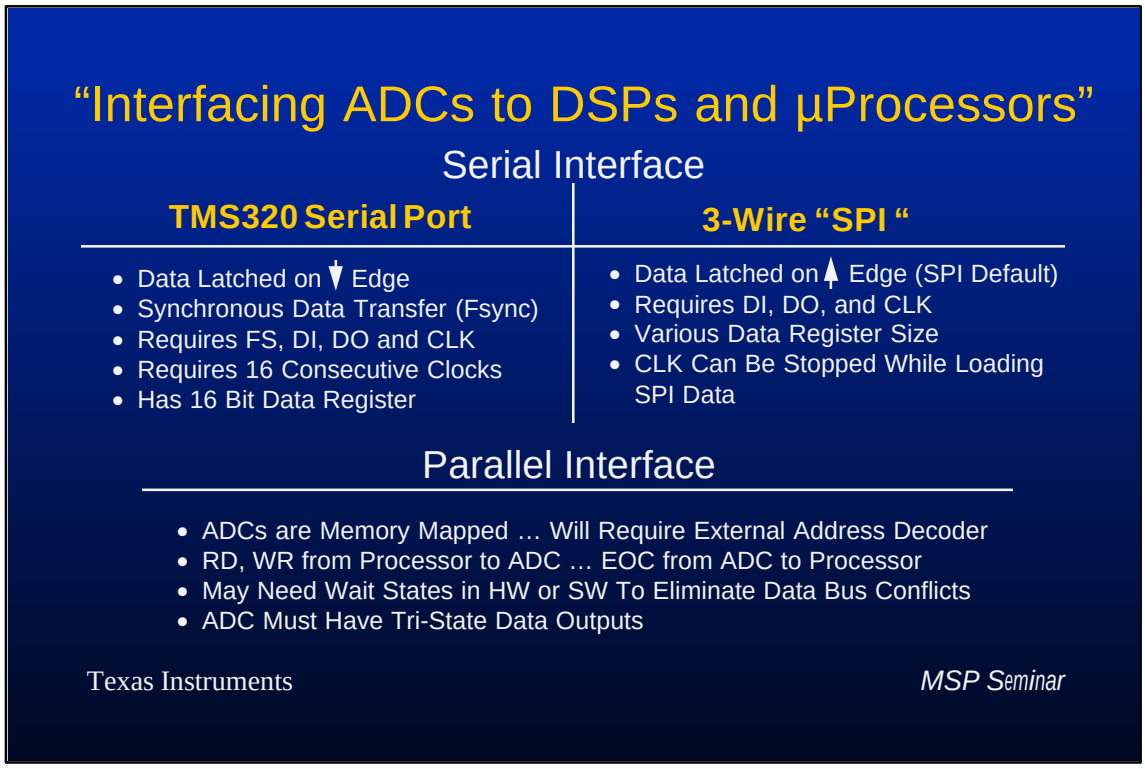


Figure 2-10 Interfacing ADCs to DSPs and µProcessors

TI Data Converters can be interfaced to a variety of processor data ports. For a parallel interface, the differences between µPs and DSPs are minimal. All interfaces will require a memory mapped scheme with address decoding and usually the connection of /RD, /WR and /EOC pins between processor and ADC.

There are variety of serial ports available today with TI TMS320Cxxx DSP and Serial Peripheral Interface (SPI) being the major serial ports. The table 2-10 tries to highlight some of the general differences between the 2 serial ports. There may be specific processors from various vendors that may have some differences.

For the TMS320 DSP family, the above table shows a baseline for the serial ports. Newer DSPs may have enhanced serial ports that may have a different data register size.

- Synchronous Serial Port - 8 / 16 Bit
- Buffered Serial Port - 8/10/12/16 Bit
- Enhanced Serial Port - T1 / E1 support

ADCs and DACs with a Frame Sync input (slave mode for DSP) have the ability to synchronize with a command from the DSP. This is equivalent to a handshaking signal.

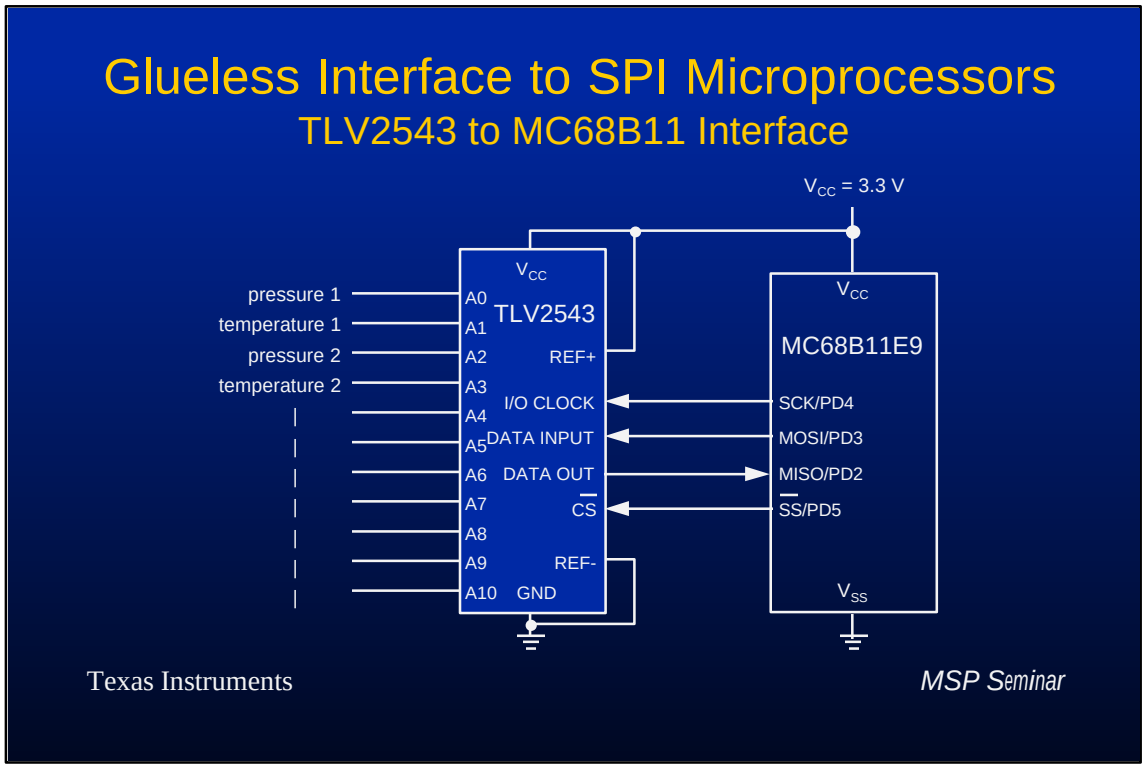


Figure 2-11 Glueless Interface to SPI Microprocessor

Microcontroller Interface

The TLV2543 can be easily interfaced to 3V and 5V supply microcontrollers (such as the MC68B11) which include a serial peripheral interface (SPI) port. The interface connections for the MC68B11 are shown in figure 2-11.

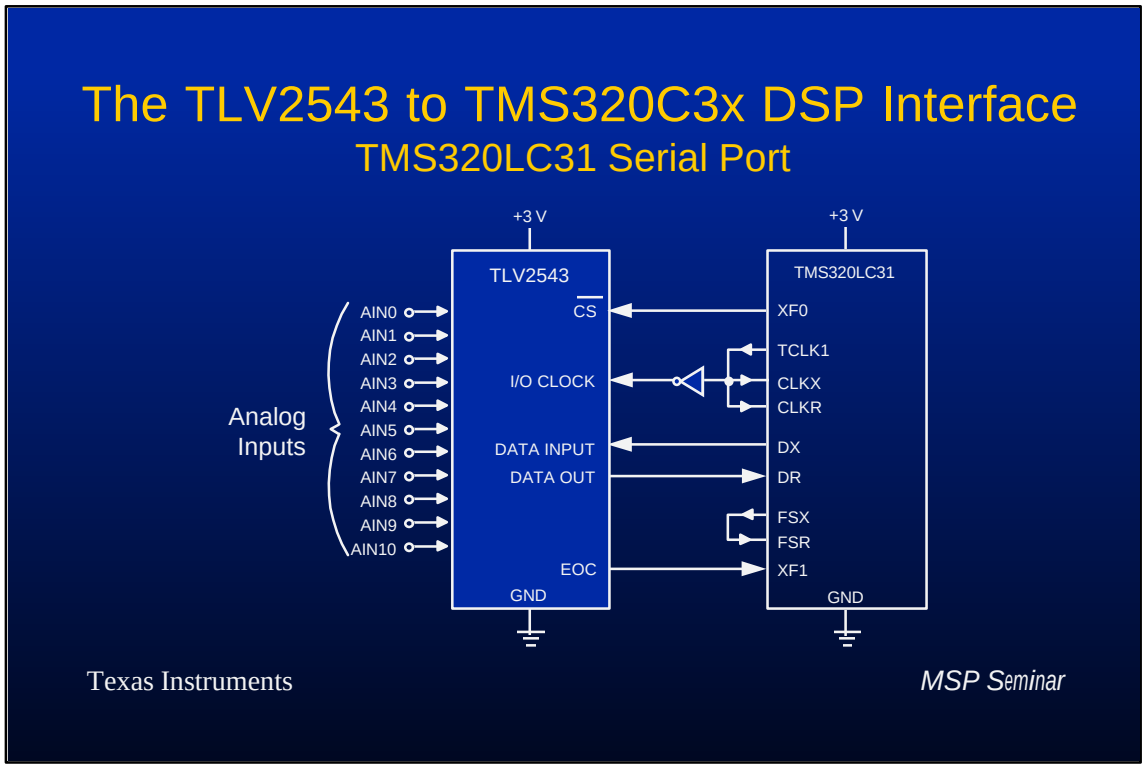


Figure 2-12 Glueless Interface to TI DSP

DSP Interface: TLV2543 to TMS320LC31

The TLV2543 can easily be interfaced to the TMS320C3x family of DSPs. This interface is implemented using the circuit shown in Figure 2-12. Notice that the EOC (End of Convert) signal of the TLV2543 is connected to the external flag input XF1 of the TMS320C3x and signifies when valid data is ready to be read into the data receive (DR) pin of the ‘C3x.

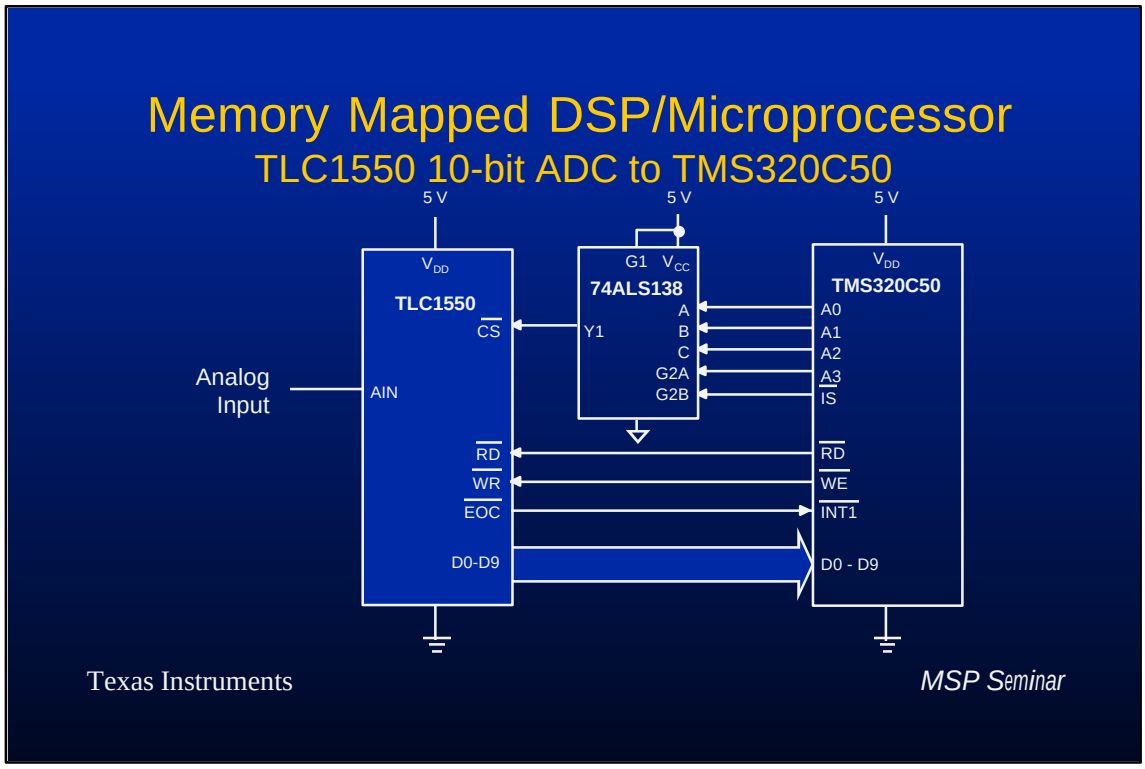


Figure 2-13 TLC1550 10-bit ADC to TMS320C50 - Parallel Interface

Higher speed interfacing between ADC and DSP can be achieved by using a converter with a parallel data output structure. An example of such a device is the TLC1550 10-bit successive approximation ADC. A typical interface of the TLC1550 to the TMS320C50 DSP is shown in Figure 2-13.

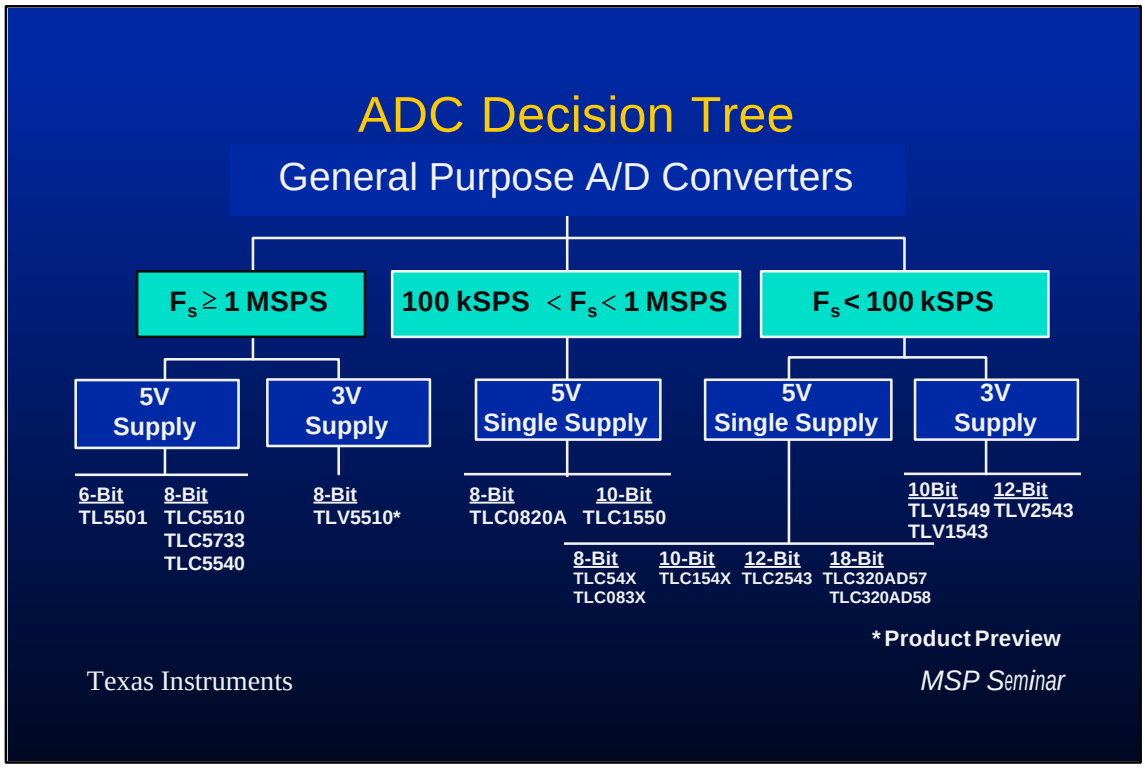


Figure 2-14 ADC Decision Tree

The above decision tree is a condensed version showing the types of ADCs offered by TI and the internal architecture that is used. Note that not all of TI's ADCs are shown in this table; please consult the 1995 Data Acquisition Circuits Data Book for a complete listing of products.

Flash	Semi-Flash	Sigma-Delta	SAR
TL5501	**TLC0820A** **TLC5510** **TLC5733** **TLC5540** **TLV5510***	**TLC320AD57** **TLC320AD58**	**TLC083X** **TLC1550** **TLV1549** **TLV2543** **TLV1543** **TLC54X** **TLC154X** **TLC2543**

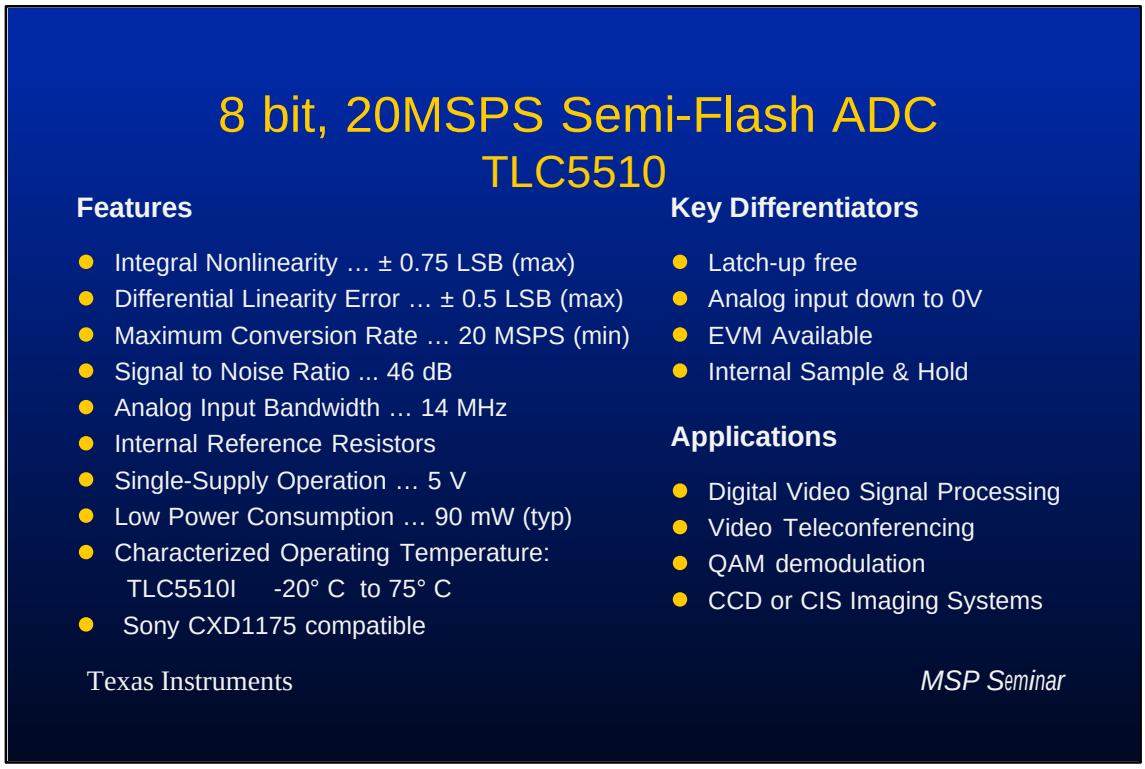


Figure 2-15 TLC5510 - 8 Bit, 20 MSPS ADC

The TLC5510INSLE 8-bit, 20 MSPS ADC provides a combination of high speed, low power and low price. By implementing a CMOS, multi-stage, semi-flash architecture the TLC5510 provides significantly lower power consumption and cost than traditional flash architectures, while maintaining conversion rates of 20 MSPS and DNL accuracy of ± 0.5 LSB.

This part is designed to be easily interfaced to a DSP. The 8 bit parallel data outputs are capable of high-impedance mode. An internal resistor network is provided to generate a 2V reference from +5V supply and only a conversion clock must be supplied. The TLC5510 consumes 90 mW of power, requires only +5V supply, has an internal S/H and is provided in a 24 pin surface mount package. The TLC5510INSLE is characterized for operation from -20°C to 75°C.

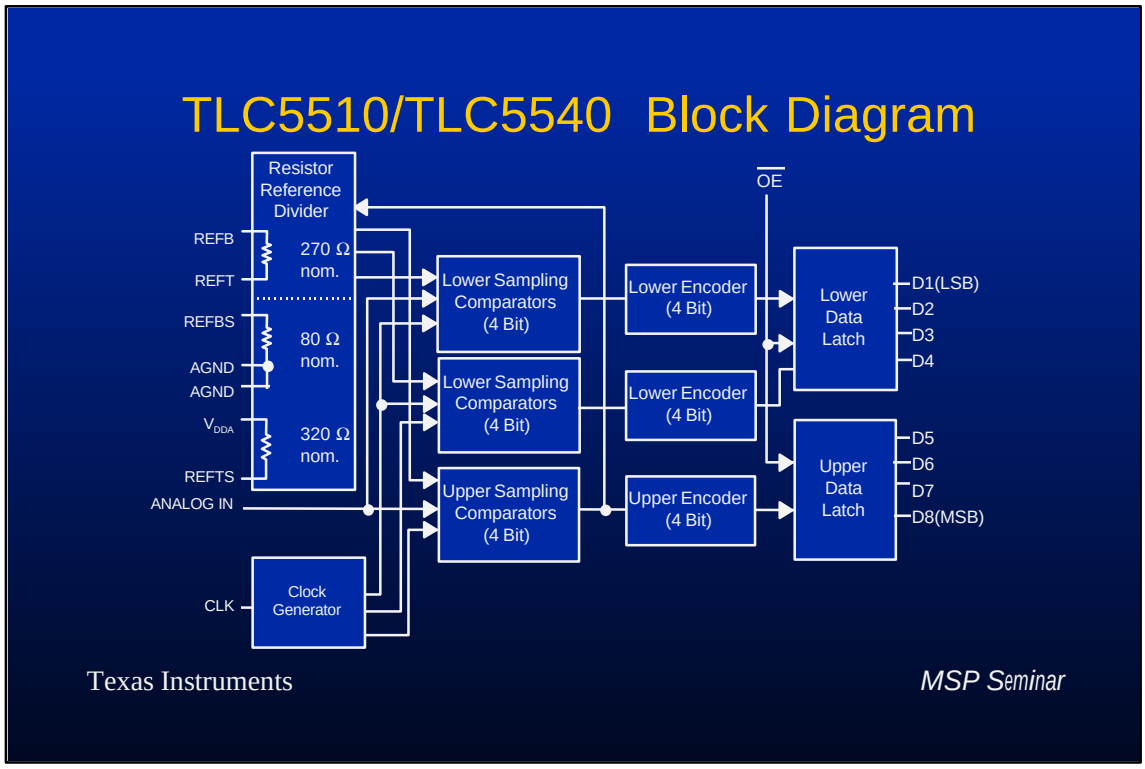


Figure 2-16 TLC5510/TCL5540 Block Diagram

Figure 2-16 shows the block diagram for both the TLC5510 and TLC5540 semi-flash ADCs Note that the upper sampling comparators (4 bits) requires only one block but the lower sampling comparator (4 bits) requires 2 blocks. The upper block converts the 4 MSBs which do not require as fast a settling time. The lower 4 bits ”ping-pong” between the 2 blocks with each block converting every other sample. This is done to meet the settling time requirement for 20 and 40 MSPS ADCs.

The TLC5510 is also latch up free. TI’s strength in CMOS processing has produced a CMOS ADC that is tolerant to power supply variation. In many CMOS ADCs, if the difference between VDDA and VDDD becomes too large, an internal diode will forward bias causing an effective short to ground and latching up the ADC. These competitive ADCs place a more stringent requirement on the quality (and lack of noise spikes) of both supplies. The TLC5510 allows the VDDA and VDDD delta to be a non-issue in a system design considerations, within the given specifications of the data sheet.

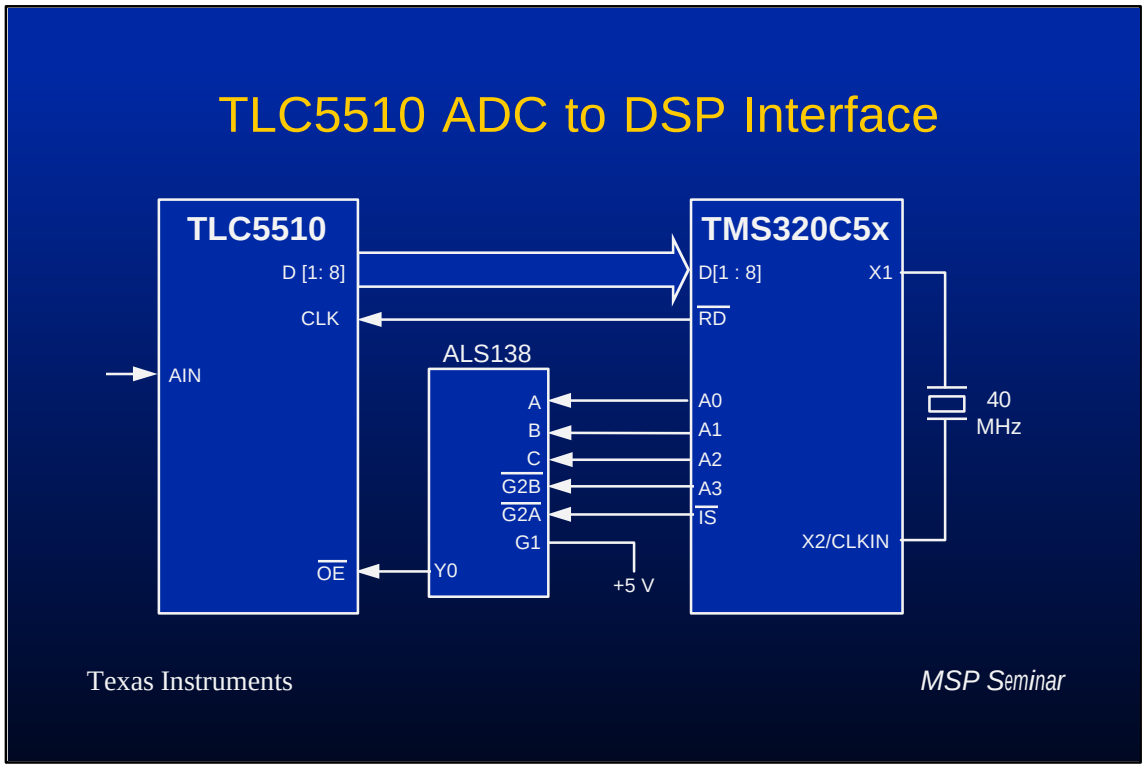


Figure 2-17 TLC5510 Flash ADC to DSP Interfaces

The TLC5510 8-bit flash ADC can be directly interfaced to the TMS320C5x as shown in figure 2-17. With the repeated block move instruction (BLDD), it is possible to read a sample from the TLC5510 and store it into internal memory in one instruction cycle, thus achieving 20 MSPS data transfer with the DSP clocked at 40 MHz. The analog input is sampled on the falling edge of CLK. The converted digital data appears at the outputs D[1:8] 2.5 clocks later. This delay is know as a 2.5 clock latency. Once past the initial 2.5 clock latency, digital output data is output on the rising edge of each clock.

The TMS320C5x is a 16-bit fixed-point family of DSPs utilizing an advanced Harvard architecture with separate strobes for program (/PS), data (/DS) and I/O space (/IS), each of them with a 64k address range.

The TLC5510 is connected to the lower 8 bits of the ‘C5x data bus; the CLK signal is connected with the read signal (/RD) of the DSP and is active when external memory is accessed. The corresponding strobe signal stays low during consecutive reads.

When the I/O strobe (/IS) is active, the TLC5510 is accessed through the memory mapped I/O space.

The interconnect line length should be as short as possible. A line matching series resistor for the CLK signal can be used to reduce overshoot and ringing.

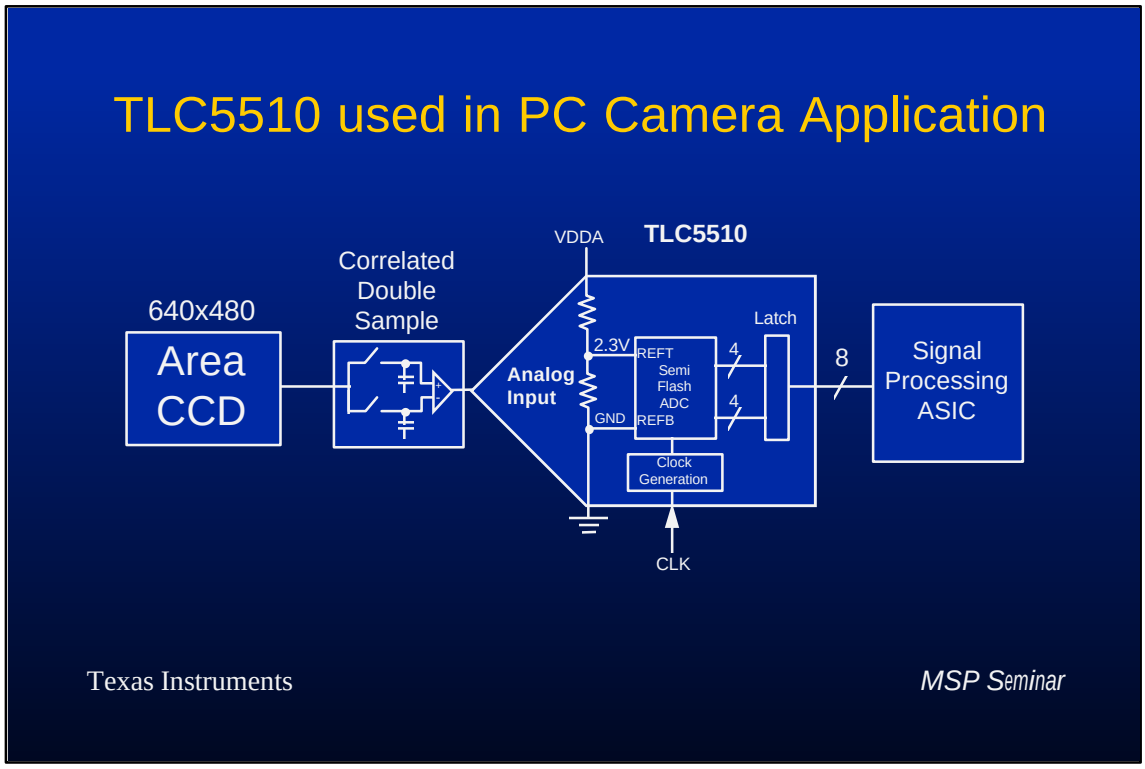


Figure 2-18 TLC5510 used in PC Camera Application

Figure 2-18 highlights some advantages of the semi-flash architecture of the TLC5510. For applications using a charge coupled device (CCD) sensor, it is common to use a correlated double sampler (CDS) to process the CCD signal. The CDS will sample both the reference voltage and the active video and then output the difference of the two. This is typically 0V (minimum intensity) and 2V (maximum intensity). Since the TLC5510 allows analog inputs as low as 0V, the CDS output to can be directly connected input of the ADC. Several competitive ADCs require the analog input to be ~ 2V. This type of ADC then requires the user to add a level shifting stage which increases the system cost and complexity.

The TLC5510 also provides internal reference resistors so that $V_{ref}+$ of 2.3V and $V_{ref}-$ of AGND can be created using no external components.

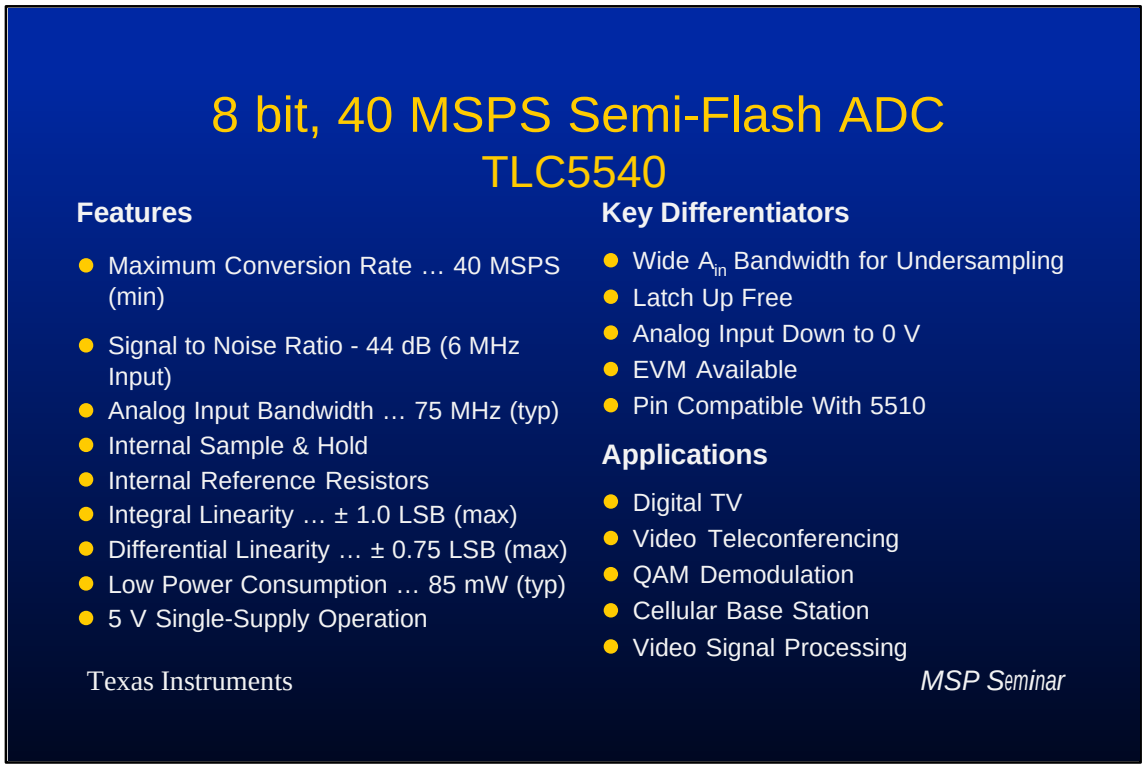


Figure 2-19 TLC5540 - Semi-Flash 8 Bit, 40 MSPS ADC

The TLC5540 is a semi-flash architecture with the same block diagram as shown in Figure 2-16. This part is a direct replacement for the TLC5510 allowing designers the flexibility of changing the sampling rate of the ADC without changing the pwb's or system timing. This part also follows the industry standard pinout. The single-supply CMOS ADC consumes only 85 mW of power at F_s = 40 MSPS. It also is fully characterized for AC specifications such as SNR, SFDR and effective bits.

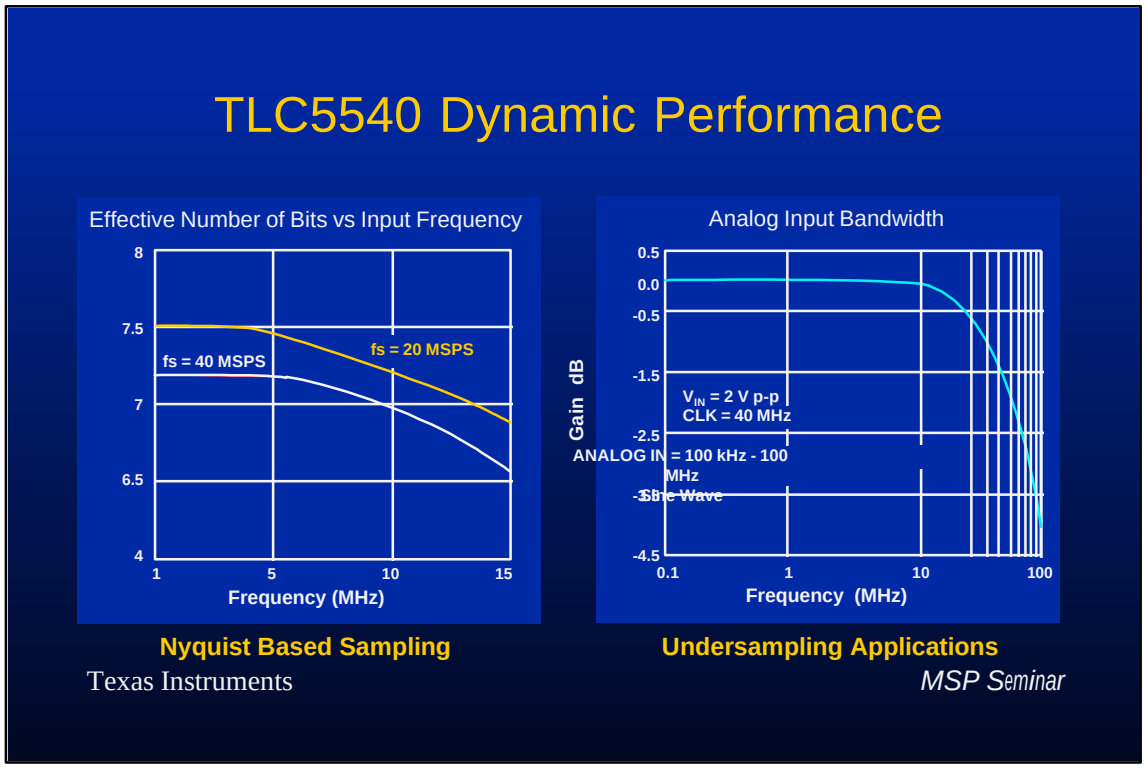


Figure 2-20 TLC5540 Dynamic Performance

TLC5540 Dynamic Performance

The TLC5540 combines high speed with low power consumption and low cost to deliver a new price/performance point for high speed (video grade) applications. For traditional Nyquist-based DSP applications, the TLC5540 delivers 7.0 effective bits at 40 MSPS. In undersampling applications, the wide analog input bandwidth (75 MHz @ -3 dB) eliminates costly analog down converter components.

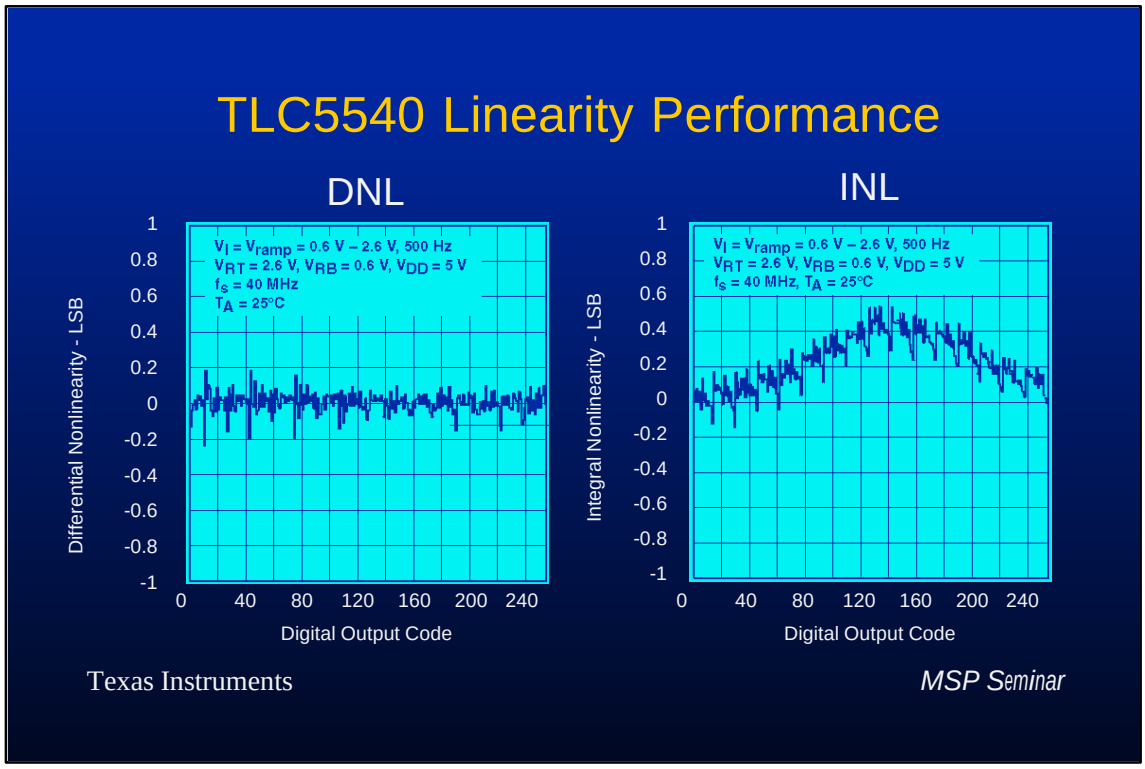


Figure 2-21 TLC5540 Linearity Performance

TLC5540 Linearity Performance

Figure 2-21 shows typical Differential Non-linearity (DNL) and Integral Non-linearity (INL) for the TLC5540. The DNL error ± 0.3 LSB with F_s = 40 MSPS indicates very low distortion in the step width of the ADC.

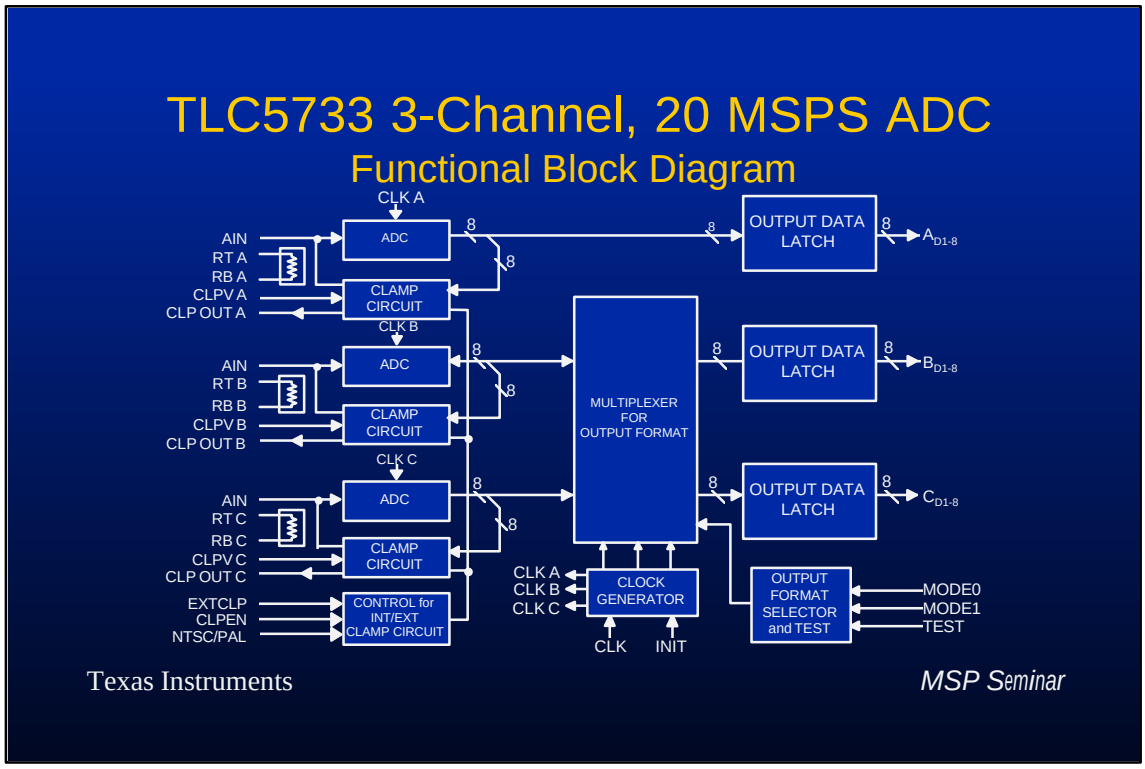


Figure 2-22 TLC5733 3-Channel, 20 MSPS ADC - Functional Block Diagram

The functional block diagram of the TLC5733 3-channel, 8-bit, 20 MSPS, Semi-Flash ADC is shown in Figure 2-22. The TLC5733 contains a feed-back type high-precision clamp circuit for each ADC channel for video (YUV) applications and a clamp pulse generator that detects COMPOSITE SYNC pulses automatically. A clamp pulse can also be supplied externally. The resistors connected between terminals RTA and RBA, RTB and RBB, and RTC and RBC are each nominally 220 Ω. They allow the full scale input signal range of each ADC (sections A, B & C) to be trimmed to a nominal value of 2 volts for video signals. This is done by a connecting an external resistor between RTA and the positive analog supply (AV_{CC}) and another between RBA and ground for section A. Similar resistor connections are used to establish the voltage for sections B and C.

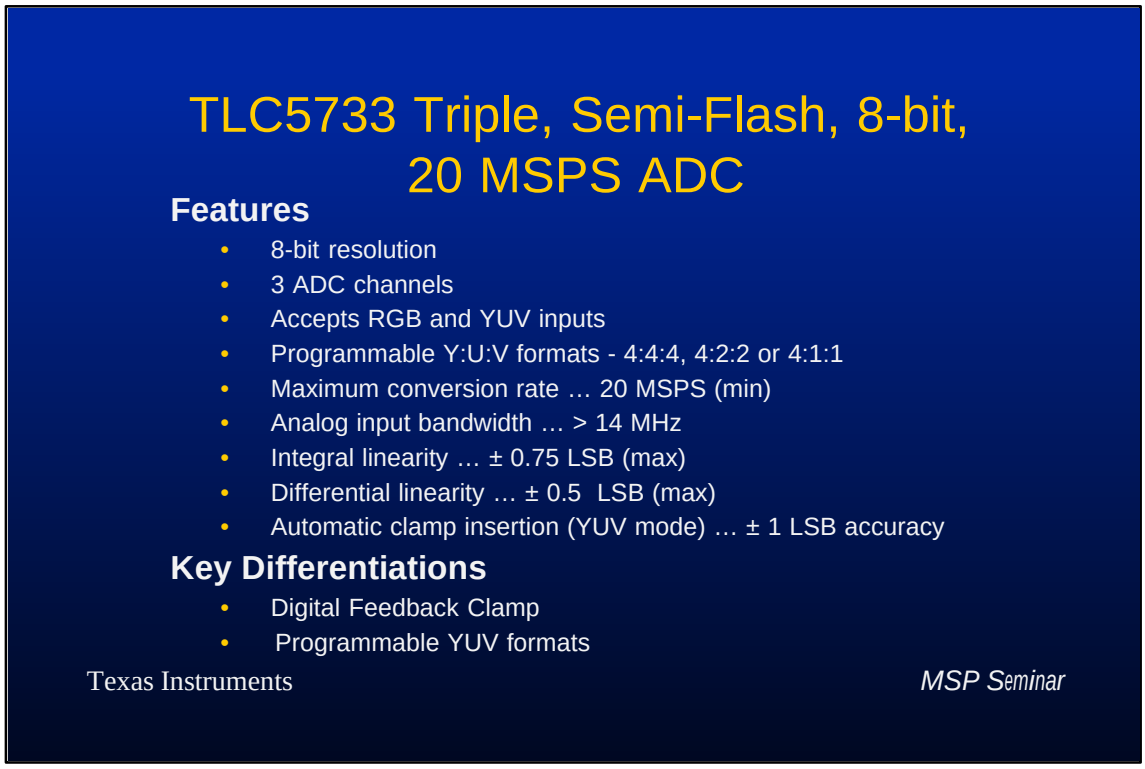


Figure 2-23 TLC5733 Triple, Semi-Flash, 8-bit, 20 MSPS ADC

The advantages of the modified semi-flash converter method are further emphasized by its use in the TLC5733 which includes three such ADCs on a single IC. Each converter operates at 20 MSPS. The three channel device can be programmed to accept either YUV or RGB analog video signals. In YUV mode the TLC5733 produces output data in 4:4:4, 4:2:2 or 4:1:1 format. For RGB applications, the output is available in 4:4:4 format.

In YUV mode the TLC5733 offers automatic clamp pulse generating facility. This detects whether the composite sync pulse has occurred in the correct time interval and automatically inserts a clamp pulse at the correct time. The digital clamp is optimized for NTSC or PAL YUV component

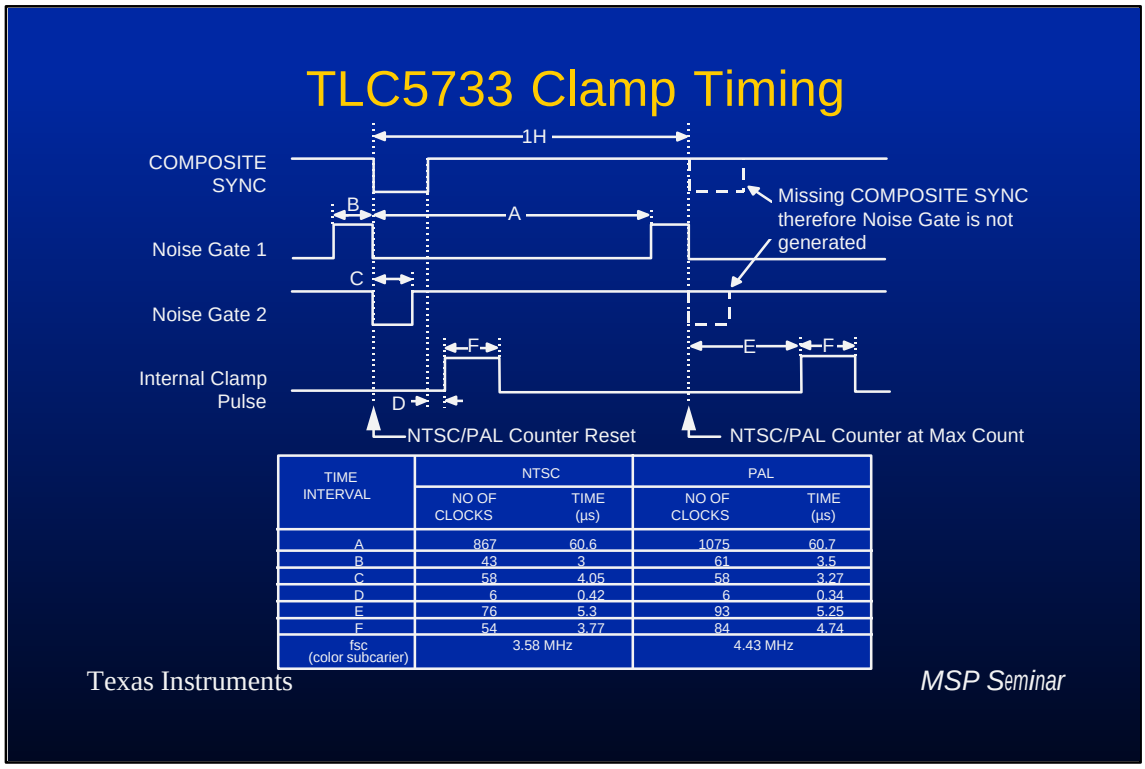
The TLC5733 is designed for low-power 5-V single-supply operation and is characterized over the -20ºC to 75ºC temperature range.

Applications

Digital Television

Camcorders

Digital Video recording



TIME INTERVAL	NTSC		PAL	
	NO OF CLOCKS	TIME (µs)	NO OF CLOCKS	TIME (µs)
A	867	60.6	1075	60.7
B	43	3	61	3.5
C	58	4.05	58	3.27
D	6	0.42	6	0.34
E	76	5.3	93	5.25
F	54	3.77	84	4.74
fsc (color subcarier)	3.58 MHz		4.43 MHz	

Figure 2-24 TLC5733 Clamp Timing

As previously mentioned, the TLC5733 can deliver the output YUV data in 4:4:4, 4:2:2 and 4:1:1 form. Figure 2-24 shows the timing diagram for the automatic clamp insertion using the composite sync signal. The TLC5733 contains a clamp insertion facility which detects the presence and position in time of the composite sync pulse. If the composite sync pulse is not detected or is incorrectly positioned in time, a clamp pulse is automatically inserted at the correct time. This facility can be programmed for NTSC or PAL timing by placing a low or high level voltage respectively on the NT/PAL pin.

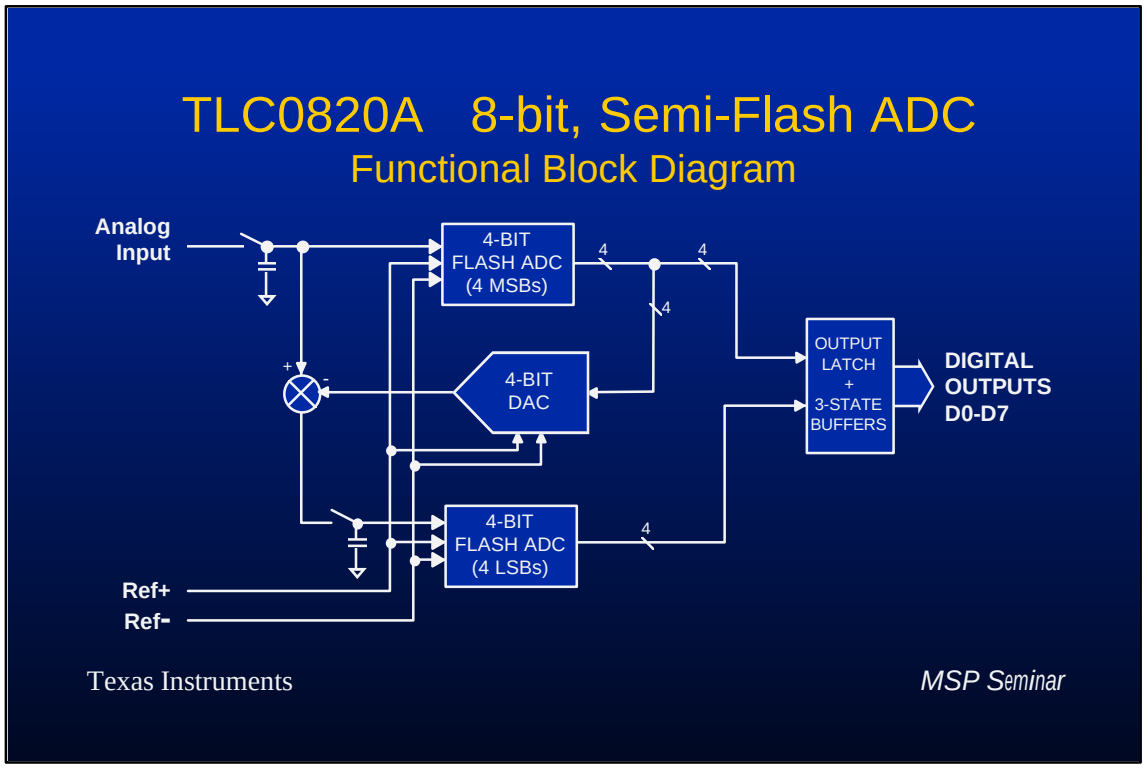


Figure 2-25 TLC0820A 8-bit, Semi-Flash ADC

The TLC0820 is an Advanced LinCMOS™ Semi-Flash 8-bit analog-to-digital converter consisting of two 4-bit flash converters, a 4-bit digital-to-analog converter, a summing (error) amplifier, control logic and a result latch circuit. An on-chip track-and-hold circuit has a 100-ns sample window and allows these devices to convert continuous analog signals having slew rates of up to 100 mV/µs without external sampling components. TTL-compatible 3-state output drivers and two modes of operation allow interfacing to a variety of processors.

Features

- 8-Bit Resolution
- Differential Reference Inputs
- Parallel Microprocessor Interface
- 2.5 µs (max) Conversion and Access Time
- No External Clock or Oscillator Components Required
- On-Chip Track-and-Hold
- Single 5-V Supply
- Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T