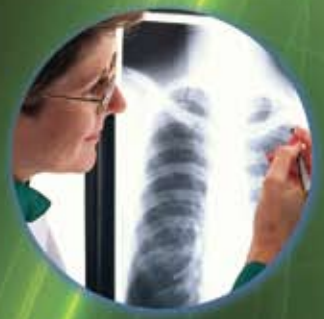
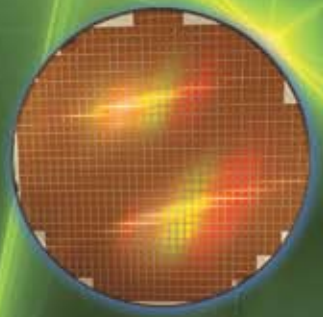
Altera Product Catalog







Contents

Innovation you can count on

At Altera, innovation is not a promise made, but a promise kept. Since we invented the first reprogrammable logic device more than 25 years ago, we've continued our commitment to delivering innovative custom logic devices that you can count on.

Our product portfolio includes:

- The industry's most advanced FPGAs, CPLDs, and ASICs
- A fully integrated software development environment
- Versatile embedded processors
- Optimized intellectual property (IP) cores
- An array of development kits, including partner offerings
- Reference designs and design examples

Leading the way at 40 nm

In May 2008, we introduced the market's first 40-nm custom logic devices—our Stratix® IV FPGAs and our HardCopy® IV ASICs, both available with transceiver options. We're continuing to collaborate closely with Taiwan Semiconductor Manufacturing Company (TSMC), our manufacturing partner, to build 40-nm devices that address an array of design challenges, from power consumption to performance to cost.

Now, we're pleased to extend our 40-nm leadership with additional transceiver-based FPGAs:

- Our new Arria® II GX FPGAs, along with our Quartus® II design software and SOPC Builder system development tool, ease the process of building transceiver solutions. With up to 16 3.75-Gbps transceivers, Arria II GX FPGAs are optimized for power, performance, and cost for 3G applications. These devices are ideal for cost-sensitive communications and video processing applications.
- Our new Stratix IV GT FPGAs bring low-power, high-density devices to the 40G/100G space. With integrated transceivers at speeds up to 11.3 Gbps, Stratix IV GT devices are well suited for wireline applications in the areas of access, enterprise, service provider, and transmission, as well as systems in the medical, test, and military industries.

Supporting a variety of markets

Using our devices and design resources, design engineers develop applications in a wide array of industries:

Automotive: Graphics processing, car networking, infotainment, driver assistance

Broadcast: Video head-end, production studio, video processing

Computer and storage: Storage, servers, high-performance computing, multi-function peripherals

Consumer: Video displays and projectors, digital TVs and set-top boxes, home networking, portable devices

Industrial: Industrial automation, industrial Ethernet, human machine interface, programmable logic controllers

Medical: Diagnostic imaging, electromedical, life sciences

Military: Radar and sensors, electronic warfare, secure communications

Test and measurement: Communication test, semiconductor ATE, general purpose

Wireless: 3G infrastructure, WiMAX, 3GPP Long-Term Evolution (LTE)

Wireline: Access, networking, transmission

For white papers, webcasts, handbooks, and more, logon to our website.

FOR MORE INFORMATION Altera www.altera.com

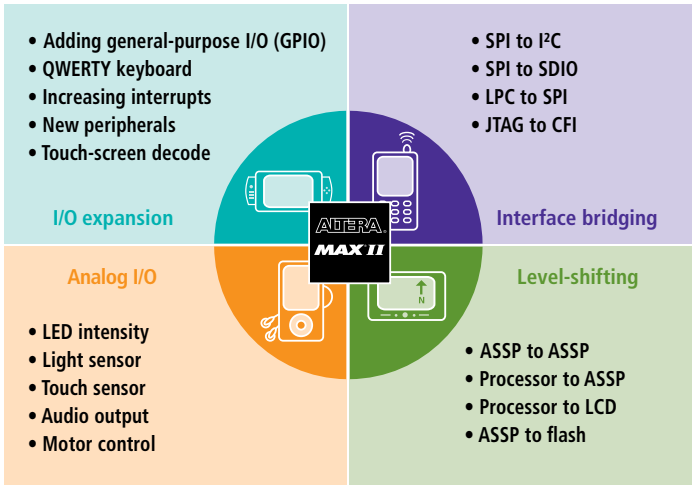
MAX CPLD series

Altera's market-leading MAX® series of CPLDs are world-class, low-cost devices designed for virtually any digital and some analog control functions. As non-volatile, single-chip solutions, MAX CPLDs are easy to incorporate into your system. With the devices, you can solve board-level issues such as insufficient I/O pins on a processor; manage analog I/Os for light, sound, and motion; apply level-shifting signals or busses between components; and inexpensively convert incompatible interfaces (a.k.a. "glue logic"). Designed to be hassle-free with intuitive device behavior and software, MAX CPLDs give you the freedom to focus on your more complex design challenges.

Key features

- Low cost
- Zero-power options
- Ultra-small packages
- Instant-on and non-volatile
- In-system programmability (ISP)
- Free Quartus® II Web Edition software support
- Free ModelSim®-Altera® Web Edition software support

MAX IIZ application areas



MAX® II

The market's lowest-cost CPLDs

MAX II devices are based on a groundbreaking architecture that combines the best of FPGAs and CPLDs. The performance and density benefits of a four-input look-up table (LUT) architecture are merged with the usability and cost advantages of a non-volatile architecture. The result? A first-in-its-class, new architecture that sets standards for cost, power consumption, performance, and density for CPLDs.

With MAX II CPLDs, you can reduce your system costs by integrating a larger amount of logic into a single device. This instant-on, non-volatile device family targets general-purpose logic applications, and comes in three variants: MAX II, MAX IIG, and MAX IIZ CPLDs.

The zero-power MAX IIZ CPLDs are the newest addition to the family. Ideal for portable and other power-, space-, and price-constrained applications, MAX IIZ devices come in ultra-small packages packed with more logic and I/O resources than are offered by traditional macrocell-based CPLDs in the same package size.

MAX II family features summary

Cost-optimized architecture	Revolutionary MAX II architecture delivers 4X the density at half the price of competing CPLDs.
Low power/zero power	Reduces power consumption and increases system reliability. The new zero-power MAX IIZ devices deliver the industry's lowest power consumption (standby and dynamic).
Highest-density CPLDs	Implements more applications in a single, low-cost device.
Small packages	Integrates on average 50 percent more user I/O pins and logic per board area (mm^2) than competing CPLDs with 0.5-mm pitch ball-grid array (BGA) packages. MAX IIZ devices come in two new ultra-small Micro FineLine BGA (MBGA) packages that deliver up to 6X the density and 3X the I/O resources in the same space as traditional macrocell-based CPLDs.
Non-volatile and instant-on functionality	Reduces system cost and board space with a single-chip solution.
User flash memory	Minimizes system cost and chip count by integrating discrete serial or parallel non-volatile storage onto MAX II devices.
Real-time ISP	Reduces maintenance costs by enabling updates while the device is in operation.
MultiVolt core	Operates with a 1.8V, 2.5V, or 3.3V power supply, minimizing power rails and simplifying board design.
MultiVolt I/O interface	Interfaces seamlessly to other devices at 1.5V, 1.8V, 2.5V, or 3.3V logic levels.
Parallel flash loader	Simplifies board management by using MAX II devices to configure external non-JTAG-compliant flash devices.

MAX®

General-purpose CPLDs

Altera's 3.3V MAX 3000A devices are cost-optimized for high-volume applications, while the 5.0V, 3.3V, and 2.5V MAX 7000 families offer world-class, high-performance solutions for a broad array of applications.

The non-volatile, EEPROM-based MAX 3000A and MAX 7000 families provide instant-on capability and offer densities from 32 to 512 macrocells. These devices support ISP and can be easily reconfigured in the field.

MAX 3000A family features summary

Low price per macrocell	Ideal for low-cost, high-volume applications.
4.5-ns propagation delays	Provides fast system performance.
5.0V tolerant I/O pins	Inherently interfaces to 5.0V devices.
Commercial and industrial temperature	Reduces overall system cost for temperature-sensitive applications.

MAX 7000 family features summary

4.5-ns propagation delays	Provides fast system performance.
5.0V tolerant I/O pins	Inherently interfaces to 5.0V devices.
Support for advanced I/O standards	Supports GTL+ and SSTL-2/-3 I/O standards (MAX 7000B CPLDs).
Programmable power-saving mode	Reduces power consumption by over 50 percent.
Commercial, industrial, and extended temperatures	Provides support for all environmental conditions.

MAX CPLD series package and I/O matrix

- Device available in commercial temperature. Contact Altera for industrial temperature.
- Device available in commercial and industrial temperatures.
- Device available in commercial and industrial, and qualified to extended temperatures.
- 36 Number indicates available user I/O pins.
- Vertical migration (Same V_{CC}, GND, ISP, and input pins).

		MAX II CPLDs 3.3V, 2.5V, 1.8V				MAX 3000A CPLDs 3.3V					MAX 7000AE CPLDs 3.3V				
		EPM240/G/Z	EPM570/G/Z	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Density and speed	**Macrocells[1]**	192	440	980	1,700	32	64	128	256	512	32	64	128	256	512
	Logic elements (LEs)	240	570	1,270	2,210	–	–	–	–	–	–	–	–	–	–
	Pin-to-pin delay (ns)[2]	4.7, 4.7, 7.5	5.4, 5.4, 9.0	6.2, 6.2	7.0, 7.0	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	7.5, 10	7.5, 10	4.5, 7.5, 10	4.5, 7.5, 10	5.0, 7.5, 10	5.5, 7.5, 10	7.5, 10, 12
PLCC (L)[3]	**44 pin**					34	34				36	36			
	84 pin												68		
TQFP (T)[4]	**44 pin**					34	34				36	36			
	100 pin	80	76				66	80				68	84	84	
	144 pin		116	116				96	116				100	120	120
PQFP (Q or R)[5]	**208 pin**								158	172				164	176
BGA (B)[6]	**256 pin**														212
FBGA (F)[7]	**100 pin**	80	76									68	84	84	
	256 pin		160	212	204			98	161	208			100	164	212
	324 pin				272										
MBGA (M)[8]	**68 pin**	54													
	100 pin	80	76												
	144 pin		116												
	256 pin		160	212											

[1] Typical equivalent macrocells for MAX II devices
[2] MAX IIZ data is preliminary
[3] Plastic J-lead chip carrier
[4] Thin quad flat pack
[5] Plastic quad flat pack
[6] Ball-grid array (1.27 mm)
[7] FineLine BGA (1.0 mm)
[8] Micro FineLine BGA (0.5 mm)

MAX CPLD series features

		MAX II CPLDs 3.3V, 2.5V, 1.8V				MAX 3000A CPLDs 3.3V					MAX 7000AE CPLDs 3.3V				
		EPM240/G/Z	EPM570/G/Z	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE
Features	User flash memory (Kbit)	8				–					–				
	Boundary scan JTAG	✓				✓					✓				
	JTAG ISP	✓				✓					✓				
	Fast input registers	✓				–					✓				
	Programmable register power-up	✓				–					✓				
	Programmable ground pins	✓				–					✓				
	Open-drain outputs	✓				✓					✓				
	Programmable pull-up resistors	✓				–					–				
	Bus hold	✓				–					–				
	JTAG translator	✓				–					–				
	Real-time ISP	✓				–					–				
	0.5-mm BGA packages[1]	✓				–					–				
Core voltage and I/O options	Core voltage (V)	1.8				3.3					3.3				
	MultiVolt core (V)	3.3, 2.5, 1.8[2]				–					–				
	MultiVolt I/Os (V)	3.3, 2.5, 1.8, 1.5				5.0, 3.3, 2.5					5.0, 3.3, 2.5				
	I/O power banks	2	2	4	4	1					1				
	Maximum I/O pins	80	160	212	272	34	66	98	161	208	36	68	100	164	212
	Maximum output enables	80	160	212	272	6	6	6	6	10	6	6	6	6	10
	Transistor-to-transistor logic (TTL) (5.0V tolerance)	–	–	✓[3]	✓[3]	✓					✓				
	LVTTL/LVCMOS	✓				✓					✓				
	32-bit, 66-MHz PCI compliant	–	–	✓	✓	–					–				
	GTL+/SSTL-2, SSTL-3, all class I and class II	–				–					–				
	Schmitt triggers	✓				–					–				
	Programmable slew rate	✓				✓					✓				
	Programmable drive strength	✓				–					–				

[1] Package not available for EPM2210/G devices
[2] MAX IIG and MAX IIZ devices require 1.8V core voltage supply
[3] An external series resistor must be used for 5.0V tolerance

FOR MORE INFORMATION

MAX II CPLDs	www.altera.com/max2
MAX 3000A CPLDs	www.altera.com/products/devices/max3k
MAX 7000 CPLDs	www.altera.com/products/devices/max7k
Training	www.altera.com/training

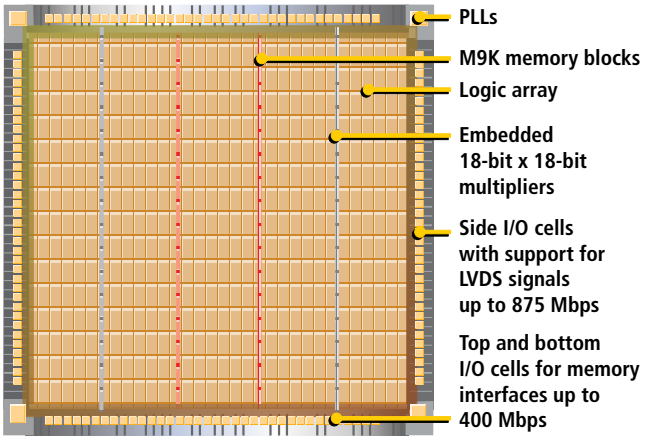
Cyclone FPGA series

For your cost-sensitive, high-volume applications, Altera offers our Cyclone® FPGA series—the industry's only FPGAs designed from the ground up for low cost. Each family member is individually optimized for cost, and delivers a high-volume solution that's competitive with ASICs and ASSPs. This series of FPGAs—including the 65-nm Cyclone III, 90-nm Cyclone II, and 130-nm Cyclone families—delivers a customer-defined feature set, industry-leading performance, and the lowest power consumption.

Key features

- The industry's lowest-cost FPGAs
- High-performance digital signal processing (DSP)
- Low-cost embedded processing
- Free Quartus® II Web Edition software support
- Free ModelSim®-Altera® Web Edition software support
- Available in commercial, industrial, and automotive temperature grades

Cyclone III floorplan



Cyclone III

65-nm low-cost FPGAs

Cyclone III FPGAs, the newest offering in this series of low-cost devices, features an unprecedented combination of low power, high functionality, and low cost to deliver more, sooner, and for less—even for your most cost-sensitive, high-volume applications. Built on TSMC's 65-nm low power (LP) process technology, Cyclone III FPGAs were designed to provide customers with the flexibility and application-optimized features to enable the highest levels of design possibilities and productivity while meeting the most stringent cost and power budgets. What's more, this can be accomplished without the high NRE costs associated with ASICs.

Because our engineers defined, designed, and developed Cyclone III FPGAs with customer feedback in mind, the devices provide the ideal features to meet your needs. The logic-, memory-, and DSP-rich architecture enables you to enhance system integration for your applications. From video and image processing to displays and wireless applications, the opportunities for Cyclone III devices are unlimited.

Cyclone III family features summary

Cost-optimized architecture	Offers from 5,136 to 119,088 LEs—70 percent more than the Cyclone II FPGA family for enhanced system integration.
Low-power architecture	Altera's innovative power-saving features and TSMC's 65-nm LP process technology come together to minimize both standby and dynamic power consumption. Quartus II design software provides a power-aware design flow to enable optimization for minimal power usage. Compared to Cyclone II FPGAs, Cyclone III devices deliver up to 50 percent lower power.
Embedded memory	Up to 4 Mbits of embedded memory for memory-intensive applications such as video line buffers.
Embedded multipliers	Up to 288 dedicated 18-bit x 18-bit multipliers for high-bandwidth parallel processing applications.
External memory interfaces	Support for high-speed external memory interfaces including DDR, DDR2, SDR SDRAM, and QDR II SRAM at up to 400 megabits per second (Mbps). The autocalibrating external memory interface PHY feature eases timing closure and eliminates variations over process, voltage, and temperature (PVT).
Robust clock management	Up to 4 phase locked loops (PLLs) per device with 5 outputs per PLL providing up to 20 global clocks. Supports dynamic reconfiguration for frequency and phase changes.
Differential signaling	Supports up to 875-Mbps receive and 840-Mbps transmit LVDS signaling. Ability to use reduced swing differential signaling (RSDS), LVDS, and point-to-point differential signaling (PPDS) without external resistors.
Commodity parallel configuration	Support for low-cost configuration options.
Remote system upgrade	Allows storage of multiple configuration images in a single configuration device for field upgrades. Automatic error correction circuitry restores factory image if error detected.
Temperature support	Automotive, industrial, and commercial

Cyclone III family features summary (continued)

Automatic single event upset (SEU) detection circuitry	Features automatic SEU detection circuitry utilizing 32-bit cyclic redundancy check (CRC).
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
MegaCore® IP library	Shorten design time using a broad portfolio of more than 200 Altera and partner intellectual property (IP) cores. Altera IP can be evaluated in hardware before purchase.
Nios® II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Cyclone III FPGAs offers up to 195-DMIPS performance.
Free software support	The free, downloadable Quartus II Web Edition software supports the entire Cyclone III family. Quartus II Web Edition software offers productivity and performance features, including TimeQuest timing analysis, PowerPlay power optimization, and SOPC Builder, providing the fastest path to design completion for Cyclone III FPGAs.

Cyclone II

90-nm low-cost FPGAs

As the second-generation offering in the Cyclone series, the Cyclone II FPGA family offers more density and features at dramatically lower costs, compared with its predecessor. Based on a 1.2V, 90-nm, low-k dielectric process, the devices include dedicated DSP circuitry for very low-cost DSP solutions. If you're implementing Nios II embedded processors on Cyclone II FPGAs, you can create cost-effective processing solutions for price-sensitive and compute-intensive applications.

Cyclone II family features summary

Cost-optimized architecture	Offers from 4,608 to 68,416 LEs—3.5X the density of first-generation Cyclone FPGAs—and the lowest cost per LE.
Embedded memory	Up to 1.1 Mbits of RAM via 4,608-bit memory blocks capable of 250-MHz performance. Support for multiple configurations, including true dual-port and single-port RAM, ROM, and FIFO buffers.
Embedded multipliers	150 18-bit x 18-bit embedded multipliers running at 250 MHz can implement common DSP functions such as finite impulse response (FIR) filters and fast Fourier transforms (FFTs). Each 18-bit x 18-bit multiplier can be configured as two independent 9-bit x 9-bit multipliers.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Cyclone II FPGAs offers up to 145-DMIPS performance.
Differential and single-ended I/O standards support	Support for LVTTL, LVCMOS, PCI, PCI-X, PCI Express[1], SSTL, and high-speed transceiver logic (HSTL) single-ended I/O standards. Differential signaling support for LVDS (805-Mbps receiving and 640-Mbps transmitting), mini-LVDS, RSDS, LVPECL, SSTL, and HSTL system interfaces.
External memory interfaces	Dedicated interfaces supporting external memory devices at 167 MHz for integration with external SDR, DDR, DDR2 SDRAM, and QDR II SRAM devices. Altera offers DDR, DDR2, and QDR II memory controller MegaCore functions free with Quartus II software subscriptions.
Clock management circuitry	16 low-skew, global clock networks span the entire device, fed by 16 dedicated input clock pins. Four PLLs provide complete system clock management on and off chip. Each PLL has three output taps, and features programmable bandwidth, programmable duty cycle, spread-spectrum clocking, lock detection, and frequency synthesis with phase-shifting capabilities.
On-chip termination (OCT)	Single-ended OCT support for driver impedance matching and series termination eliminates the need for external resistors, improves signal integrity, and simplifies board design.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	Features automatic SEU detection circuitry utilizing 32-bit CRC.

[1] Requires external PHY device

Cyclone™

130-nm low-cost FPGAs

Cyclone devices provide application-focused features such as embedded memory, external memory interfaces, and clock management circuitry at price points optimal for high-volume applications.

Cyclone family features summary

Cost-optimized architecture	Offers from 2,910 to 20,060 LEs; built for low cost.
Embedded memory	288 Kbits of RAM through 4,608-bit memory blocks can be configured to support a wide range of operation modes, including RAM, ROM, FIFO buffers, and single-port and dual-port modes.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Cyclone FPGAs offers up to 130-DMIPS performance.
Single-ended I/O support	Supports a variety of single-ended I/O interface standards, such as the 3.3V, 2.5V, 1.8V, LVTTL, LVCMOS, SSTL, and PCI standards needed for today's systems.
External memory interfaces	Dedicated external memory interfaces allow you to integrate external SDR and DDR SDRAM devices into complex system designs without degrading data access performance.
Differential I/O support	Support for 129 LVDS and RSDS channels with 640-Mbps LVDS data rates and 311-Mbps RSDS data rates.
Clock management circuitry	Features up to two programmable PLLs and eight global clock lines that provide robust clock management and frequency synthesis capabilities enabling on- and off-chip system clock management. PLLs offer advanced features such as frequency synthesis, programmable phase shift, programmable delays, and external clock output.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures that Cyclone devices operate no matter how the system is powered up.
Automatic SEU detection circuitry	Utilizes 32-bit CRC to minimize radiation problems.

Cyclone FPGA series features

		Cyclone III family (1.2V)							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Density and speed	LEs	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
	Total RAM (Kbits)[1]	414	414	504	594	1,134	2,340	2,745	3,888
	M9K block (8 Kbits + 512 parity bits)[1]	46	46	56	66	126	260	305	432
	Speed grades (fastest to slowest)[2]	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-7, -8
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others							
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	23/46	23/46	56/112	66/132	126/252	156/312	244/488	288/576
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓
	Global clock networks	10	10	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mbits)	2.8	2.8	3.9	5.5	9.1	14.2	19	27.2
I/O features	I/O voltage levels supported	1.5, 1.8, 2.5, 3.0, 3.3							
	I/O standards supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), 1.5V Differential HSTL (I and II), 1.8V Differential HSTL (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), PCI, PCI-X, PCI Express[3], LVTTL, LVCMOS, PPDS							
	LVDS maximum data rate (Mbps) (receive/transmit)	875/840							
	LVDS channels	66	66	136	79	223	159	177	229
	RSDS maximum data rate (Mbps) (transmit)	360							
	Mini-LVDS maximum data rate (Mbps) (transmit)	400							
	Series OCT	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory device supported	QDR II, DDR2, DDR, SDR							
	MegaCore controller with clear text datapath	✓							
	System timing and analysis	✓							
	Board layout guideline	✓							

[1] Kbits = 1,024 bits

[2] Not all packages are supported in all speed grades

[3] Requires external PHY device

Cyclone FPGA series features

		Cyclone II family (1.2V)							Cyclone family (1.5V)				
		EP2C5/A	EP2C8/A	EP2C15A	EP2C20/A	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Density and speed	LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416	2,910	4,000	5,980	12,060	20,060
	Total RAM (Kbits)[1]	117	162	234	234	473	581	1,125	59	77	90	234	288
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	26	36	52	52	105	129	250	13	17	20	52	64
	Speed grades (fastest to slowest)	-6, -7, -8							-6, -7, -8				
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others							Nios II processor, as well as partner processors from ARM, Freescale, and others				
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	13/26	18/36	26/52	26/52	35/70	86/172	150/300	–	–	–	–	–
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	8	8	16	16	16	16	16	8	8	8	8	8
	PLLs/unique outputs	2/6	2/6	4/12	4/12	4/12	4/12	4/12	1/3	2/6	2/6	2/6	2/6
	Configuration file size (Mbits)	1.26	1.98	3.89	3.89	6.85	9.96	14.31	0.63	0.93	1.17	2.32	3.56
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3							1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), 1.5V Differential HSTL (I and II), 1.8V Differential HSTL (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), PCI, PCI-X, PCI Express[2], LVTTL, LVCMOS							LVDS, RSDS, Differential SSTL-2, SSTL-2 (I and II), SSTL-3 (I and II), PCI, LVTTL, LVCMOS				
	LVDS maximum data rate (Mbps) (receive/transmit)	805/640	805/640	805/640	805/640	805/640	805/640	805/640	640/640	640/640	640/640	640/640	640/640
	LVDS channels	60	79	136	136	209	197	265	34	129	72	103	129
	RSDS maximum data rate (Mbps) (transmit)	311	311	311	311	311	311	311	311	311	311	311	311
	Mini-LVDS maximum data rate (Mbps) (transmit)	311	311	311	311	311	311	311	–	–	–	–	–
	Series OCT	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	QDR II, DDR2, DDR, SDR							DDR, SDR				
	MegaCore controller with clear text datapath	✓							✓				
	System timing analysis	✓							✓				
	Board layout guidelines	✓							✓				

[1] Kbits = 1,024 bits

[2] Requires external PHY device

Cyclone FPGAs Cyclone II FPGAs Cyclone III FPGAs

Cyclone FPGA series comparative table

Device	LEs	Embedded RAM blocks[1]	RAM Kbits	18-bit x 18-bit multipliers	PLLs	Clock outputs per PLL	I/O banks	Max LVDS channels[2]
EP1C3	2,910	13	58	-	1	3	4	34
EP1C4	4,000	17	76	-	2	3	4	129
EP2C5	4,608	26	119	13	2	3	4	61
EP3C5	5,136	46	414	23	2	5	8	62
EP1C6	5,980	20	90	-	2	3	4	72
EP2C8/A	8,256	36	165	18	2	3	4	75
EP3C10	10,320	46	414	23	2	5	8	62
EP1C12	12,060	52	234	-	2	3	4	103
EP2C15A	14,448	52	239	26	4	3	8	128
EP3C16	15,408	56	504	56	4	5	8	128
EP1C20	20,000	64	288	-	4	3	4	129
EP2C20/A	18,752	52	239	35	4	3	8	128
EP3C25	24,624	66	594	66	4	5	8	71
EP2C35	33,216	105	483	35	4	3	8	201
EP3C40	39,600	126	1,134	126	4	5	8	215
EP2C50	50,528	129	594	86	4	3	8	189
EP3C55	55,856	260	2,340	156	4	5	8	151
EP2C70	68,416	250	1,152	150	4	3	8	257
EP3C80	81,264	305	2,745	244	4	5	8	169
EP3C120	119,088	432	3,888	288	4	5	8	221

1 Cyclone and Cyclone II FPGAs have 4-Kbit RAM blocks; Cyclone III FPGAs have 9-Kbit RAM blocks.

2 Bidirectional I/O pins can be used as inputs or outputs; does not include dedicated clock input pins.

Cyclone FPGA series package matrix and maximum user I/Os

Device	Package/package size (mm)														
	T100 16 x 16	E144 22 x 22	T144 22 x 22	M164 8x8	Q208 30 x 30	Q240 35 x 35	F256 17 x 17	U256 14 x 14	F324 19 x 19	F400 21 x 21	F484 23 x 23	U484 19 x 19	F672 27 x 27	F780 29 x 29	F896 31 x 31
EP1C3	65		104												
EP1C4									249	301					
EP2C5			89		142		158								
EP3C5		94		106			182	182							
EP1C6			98			185	185								
EP2C8/A			85		138		182								
EP3C10		94		106			182	182							
EP1C12						173	185		249						
EP2C15A							152				315				
EP3C16		84		92		160	168	168			346	346			
EP1C20									233	301					
EP2C20/A						142	152				315				
EP3C25		82				148	156	156	215						
EP2C35											322	322	475		
EP3C40						128			195		331	331		535	
EP2C50											294	294	450		
EP3C55											327	327		377	
EP2C70													422		622
EP3C80											295	295		429	
EP3C120											283			531	

FOR MORE INFORMATION

Cyclone III FPGAs	www.altera.com/cyclone3
Cyclone II FPGAs	www.altera.com/cyclone2
Cyclone FPGAs	www.altera.com/cyclone
Training	www.altera.com/training

Arria FPGA series

Arria® series FPGAs optimize power, performance, and cost for applications requiring 3G transceivers. This series is ideal for a wide range of applications using mainstream protocols such as PCI Express, CPRI, SDI, Gigabit Ethernet, and more. With the integrated Quartus® II design environment, IP, reference designs, design examples, and development kits, you'll get your design up and running in no time.

Key features

- Optimized power, performance, and cost for 3G applications
- Proven transceiver architecture with best-in-class signal integrity
- Highly productive, easy-to-use common design environment
- Ready-to-use reference designs, design examples, and IP

Easy-to-use, low-power transceiver FPGAs up to 3.75 Gbps

Arria® II GX FPGAs are the easy-to-use FPGAs for up to 3.75-Gbps applications. Our software and integration tools, IP, reference designs, design examples, and protocol IP packs will ensure you finish faster. Optimized for power, performance and cost, Arria II GX FPGAs are ideal for 3G applications, such as remote radio heads, studio and access equipment, and more. With the Arria II GX family, you get just the right amount of programmable logic, external memory interfaces, and transceivers for smaller designs. Pair that with low power, and the Arria II FPGA family is the right fit for your next generation products.

It's so easy with Arria II GX FPGAs, you can get a working PCI Express design in 45 minutes.

Arria II GX features summary

Easy-to-use design tools	Award-winning Quartus II design suite with the fastest compile time in the industry. IP, Megawizard™ plug in, SOPC Builder, and DSP Builder make design entry and connectivity easy. For board design and simulation, use the power distribution network (PDN) tool and board design guidelines along with IBIS and SPICE models for simulation.
Ready-to-use reference designs, design examples, and IP	Suite of designs and IP to jump start your design for a wide range of applications including remote radio head, broadcast, and access equipment.
45 minutes to a working PCI Express design	Get a working design that integrates a DMA controller, on-chip block memory, and PCI Express x4 connectivity in 45 minutes.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Arria II FPGAs offers over 250-DMIPS performance.
Low-power, cost-optimized multi-gigabit transceivers	Up to 16 transceivers running at 3.75 Gbps, support for mainstream protocols, and the flexibility of a high-bandwidth FPGA. Each channel consumes less than 100 mW power running at 3.125 Gbps.
Protocol support and IP	Support mainstream protocols to increase productivity, including PCI Express, CPRI, Gigabit Ethernet, triple-rate SDI, and Serial RapidIO® (SRIO).
Dynamic transceiver configuration	Provides design flexibility to support multiple protocols or data rates on the same transceiver channel without resetting the FPGA.
PCI Express hard IP block	PCI Express v1.1 support without license fees. Hard IP block implementation with PHY-MAC, data link, and transaction layers reduces design time and cost.
Best-in-class signal integrity	Signal integrity optimized for 3G protocols for easy board design with minimal external components. Choose equalization and pre-emphasis settings to compensate for board trace differences.
Core architecture	8-input ALM-based core architecture; power-, performance-, and cost-optimized for 3G transceiver applications.
Embedded memory blocks (M9K)	Up to 8.5 Mbits of memory in 9K blocks optimal for applications such as packet processing, video line buffers, data storage, and FIFOs.
MLABs	Up to 5 Mbits of 640-bit memory logic array blocks (MLABs) provide fast access and flexibility for FIFO buffers.
DSP blocks	Up to 736 multipurpose configurable 18x18 multipliers with input registers, make finite impulse response (FIR) filter and DSP processing design easy.
Clock management circuitry	Up to 6 PLLs with 7 outputs each, provide abundant on-chip clocks for design ease and flexibility.
External memory interfaces	Auto-calibrating PHY allows fast and easy timing closure over PVT for popular memory interfaces including DDR2, DDR3, and QDR II.
High-speed differential signaling	Dedicated circuitry for implementing differential signals including LVDS from 150 Mbps to 1 Gbps.
DPA and soft-CDR	Receiver circuitry automatically compensates from "channel-to-channel" and "channel-to-clock" skew in source synchronous interfaces.
ACJTAG	Support board level diagnostics for multi-gigabit transceivers using boundary scan.
Design security	Volatile and non-volatile 256-bit AES key for IP security against tampering and reverse engineering.
SEU mitigation	Built-in error detection circuitry for data corruption due to soft errors.

[1] All data is preliminary

Arria II GX transceiver protocol support

Protocol	Data rate (Gbps)
ASI	0.27
Basic (proprietary)	0.6-3.75
CPRI	0.6144, 1.2288, 2.4576, 3.072
10G Ethernet (XAUI)	3.125
Gigabit Ethernet	1.25
GPON	1.244 Uplink, 2.488 Downlink
HiGig+	3.75
OBSAI	0.768, 1.536, 3.072
PCI Express Gen1	2.5
PCI Express Cable	2.5
SAS	1.5, 3
SATA	1.5, 3
3G-SDI	2.97
SDI SD/HD	0.27/1.485
SerialLite II	0.6-3.75
Serial RapidIO®	1.25, 2.5, 3.125
SONET OC-3/OC-12/OC-48	0.155, 0.622, 2.488
SPAUI	3.125

FPGAs with 3.125 Gbps transceivers

With our Arria GX FPGAs, you can quickly and easily connect custom logic to devices with transceiver speeds up to 3.125 Gbps. Arria GX devices use Altera's proven transceiver technology that supports a variety of serial protocols, for bridging, wireless, and wireline applications. This family offers logic densities ranging from 20K to 90K LEs and supports a number of ready-made IP cores to get your designs up and running.

Arria GX FPGAs are backed by years of Altera® transceiver expertise: a physical coding sublayer (PCS) and physical medium attachment (PMA) interface are protocol-optimized, low-power versions of those in Stratix® II GX FPGAs. Arria GX devices support protocols including PCI Express Gen1, CPRI, Serial RapidIO, and Gigabit Ethernet, providing an easy way to interface custom logic to mainstream protocols at a very low total cost of ownership. You'll also benefit from Altera's extensive set of reliable tools and comprehensive support infrastructure.

Arria GX features summary

Complete solution	Fully tested IP is available for PCI Express (x1 and x4), Gigabit Ethernet, SDI, Serial RapidIO, XAUI, and more for up to 3.125 Gbps. A simple and inexpensive development kit with reference designs is also available to demonstrate the simplicity of designing transceiver interfaces with Arria GX devices.
Best-in-class signal integrity	The Arria GX transceiver is based on the proven Stratix II GX transceiver and built with flip-chip packages. For those protocols supported by Arria GX FPGAs, you'll get signal integrity that's close to what can be achieved by a Stratix II GX FPGA.
Unparalleled software tools	The award-winning Quartus II Web Edition, as well as the subscription version, supports all members of the Arria GX family. This makes designing with this family easy and inexpensive.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Arria GX FPGAs offers over 200-DMIPS performance.
Extensive support network	Altera's team of several hundred field applications engineers (FAEs) worldwide are available to help drive your success. This team is also backed by a global team of applications engineers in several Regional Service Centers around the world.

Arria GX transceiver protocol support

Protocol	Data rate (Gbps)
PCI Express Gen1	2.5
10G Ethernet (XAUI)	3.1250
Serial RapidIO	1.25, 2.5, 3.125
Gigabit Ethernet	1.25
3G-SDI	2.97
SDI, SD/HD	0.27/1.48
SerialLite II	0.6–3.125
Basic mode	Up to 3.125
Common Public Radio Interface (CPRI)	0.6144, 1.2288, 2.4576, 3.072
Open Base Station Architecture Initiative (OBSAI)	0.768, 1.536, and 3.072

Arria FPGA series package and I/O matrix

36 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins).

All Arria GX devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

Arria II GX FPGAs (0.9V)[1], 3.75-Gbps transceivers

		EP2AGX20C	EP2AGX30C	EP2AGX45C	EP2AGX45D	EP2AGX65C	EP2AGX65D	EP2AGX95D	EP2AGX95E	EP2AGX125D	EP2AGX125E	EP2AGX190E	EP2AGX190F	EP2AGX260E	EP2AGX260F
UBGA (U)	**358 pin**	156	156	156	156	156	156								
FBGA (F)	**572 pin**	252	252	252	252	252	260	260	260	260	260				
	780 pin			364	364	364	364	372	372	372	372				
	1,152 pin							452	452	452	452	612	612	612	612

[1] All data is preliminary

36 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins).

All Arria GX devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

Arria GX FPGAs (1.2V) 3.125-Gbps transceivers

		EP1AGX20	EP1AGX35	EP1AGX50	EP1AGX60	EP1AGX90
FineLine BGA (F)	**484 pin**	255	255	254	254	
	780 pin	366	366	395	395	
	1,152 pin			563	583	607

Arria II GX FPGA family features

Part 1 of 2

		Arria II GX FPGAs (0.9V)[1], 3.75-Gbps transceivers				
		EP2AGX20C	EP2AGX30C	EP2AGX45C	EP2AGX45D	EP2AGX65C
Density and speed	Equivalent LEs	15,950	27,000	45,125	45,125	63,250
	Adaptive logic modules (ALMs)	6,380	10,800	18,050	18,050	25,300
	M9K memory blocks	87	144	319	319	495
	Embedded memory (M9K in Kbits)	783	1,296	2,871	2,871	4,455
	Total on-chip memory (M9K + MLAB)	982	1,634	3,435	3,435	5,246
	18-bit x 18-bit embedded multipliers	56	128	232	232	312
	Speed grades (fastest to slowest)	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others				
	Global clock networks	16	16	16	16	16
	Regional clock networks	48	48	48	48	48
	Periphery clock networks	33	33	50	50	50
	PLLs/unique outputs	4/28	4/28	4/28	4/28	4/28
	Design security	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported	1.2, 1.5, 1.8, 2.5, 3.0				
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS				
	True-LVDS data rate (Mbps)	150 – 1,000				
	Number of LVDS channels (receive/transmit)	57/56	57/56	85/84	85/84	85/84
	Embedded DPA circuitry	✓	✓	✓	✓	✓
	Series and differential on-chip termination (OCT)	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps – 3.75 Gbps with PCS + PMA				
	Transceiver (SERDES) channels	4	4	4	8	4
	PCIe hard IP block Gen1.1	1	1	1	1	1
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II				
Configuration file sizes	Configuration file size (Mbits)	52	52	52	102	102

[1] All data is preliminary

Arria II GX FPGA family features

Arria II GX FPGAs (0.9V)[1], 3.75-Gbps transceivers

EP2AGX65D	EP2AGX95D	EP2AGX95E	EP2AGX125D	EP2AGX125E	EP2AGX190E	EP2AGX190F	EP2AGX260E	EP2AGX260F
63,250	93,675	93,675	124,100	124,100	190,300	190,300	256,500	256,500
25,300	37,470	37,470	49,640	49,640	76,120	76,120	102,600	102,600
495	612	612	730	730	840	840	950	950
4,455	5,508	5,508	6,570	6,570	7,560	7,560	8,550	8,550
5,246	6,679	6,679	8,121	8,121	9,939	9,939	11,756	11,756
312	448	448	576	576	656	656	736	736
-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6	-4, -5, -6
Nios II processor, as well as partner processors from ARM, Freescale, and others								
16	16	16	16	16	16	16	16	16
48	48	48	48	48	48	48	48	48
50	59	59	59	59	84	84	84	84
4/28	6/42	6/42	6/42	6/42	6/42	6/42	6/42	6/42
✓	✓	✓	✓	✓	✓	✓	✓	✓
1.2, 1.5, 1.8, 2.5, 3.0								
LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS								
150 – 1,000								
85/84	88/88	105/104	105/104	105/104	145/144	145/144	145/144	145/144
✓	✓	✓	✓	✓	✓	✓	✓	✓
✓	✓	✓	✓	✓	✓	✓	✓	✓
✓	✓	✓	✓	✓	✓	✓	✓	✓
600 Mbps – 3.75 Gbps with PCS + PMA								
8	8	12	8	12	12	16	12	16
1	1	1	1	1	1	1	1	1
DDR3, DDR2, DDR, QDR II								
102	102	140	140	140	140	140	140	189

[1] All data is preliminary

Arria GX FPGA family features

		Arria GX FPGAs (1.2V) 3.125-Gbps transceivers				
		EP1AGX20	EP1AGX35	EP1AGX50	EP1AGX60	EP1AGX90
Density and speed	Equivalent LEs	21,580	33,520	50,160	60,100	90,220
	ALMs	8,632	13,408	20,064	24,040	36,088
	Adaptive look-up tables (ALUTs)	17,264	26,816	40,128	48,080	72,176
	Total RAM (Kbits)[1]	1,229	1,348	2,475	2,529	4,478
	M512 RAM blocks (512 bits + 64 parity bits)	166	197	313	326	478
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	118	140	242	252	400
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	1	1	2	2	4
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	40/80	56/112	104/208	128/256	176/352
	Speed grades	-6	-6	-6	-6	-6
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others				
	DSP blocks	10	14	26	32	44
	I/O registers per I/O element	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓
	Global and regional clock networks	48	48	48	48	48
	PLLs/unique outputs	4	4	4 or 8	4 or 8	8
	Design security	–	–	–	–	–
	HardCopy® II device support	–	–	–	–	–
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS				
	True-LVDS data rate (Mbps)	125 – 840				
	True-LVDS channels (receive/transmit)	31/29	31/29	42/42	42/42	47/45
	Embedded DPA circuitry	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓
	Programmable drive strength	–	–	–	–	–
	Transceiver (SERDES) data rate range	600 Mbps – 3.125 Gbps with PCS + PMA				
	Transceiver (SERDES) channels	4	4 or 8	4 or 8	4, 8 or 12	12
External memory interfaces	Memory devices supported	DDR2, DDR, SDR				
Configuration file sizes	Configuration file size (Mbits)	10	10	17	17	28

[1] Kbits = 1,024 bits

FOR MORE INFORMATION

Arria II GX FPGAs	www.altera.com/arria2gx
Arria GX FPGAs	www.altera.com/arriagx
Training	www.altera.com/training

Stratix FPGA series

The Stratix® FPGA series enables you to deliver high-performance, state-of-the-art products to market faster with lower risk and higher productivity. With its high density, high performance, and rich feature set, you can integrate more functions and maximize performance. Using the Quartus® II design software suite, along with a broad portfolio of IP, you can gain the highest level of productivity for large and complex team-based designs. Also contributing to the total solution are HardCopy® ASICs, which provide a seamless migration path to low-cost volume production. Backed by Altera's track record as a reliable and high-quality supplier, the Stratix FPGA series delivers the technology resources you need to design with confidence.

Key features

- Industry's biggest and fastest FPGAs
- Lowest power high-end FPGAs
- Only FPGAs with integrated 11.3-Gbps transceivers
- Flexible and high-performance I/O pins
- Highest DSP and memory capabilities
- Path to low-cost, lowest risk HardCopy ASICs, including transceiver option
- Volatile and non-volatile design security
- Quartus II design software for highest performance and productivity

Stratix® IV

40-nm high-performance, high-end FPGAs with 11.3-Gbps transceiver option

Stratix IV FPGAs are the lowest power, high-density, high-performance FPGAs. Three variants meet the diverse application needs of large designs: Stratix IV GT FPGAs, Stratix IV GX FPGAs, and Stratix IV E FPGAs. Stratix IV GT FPGAs offer the only single chip solution for 10G/40G/100G applications with integrated 11.3-Gbps transceivers. Stratix IV GX FPGAs deliver unprecedented system bandwidth with superior signal integrity. With Stratix IV E FPGAs, you get the highest density available for your non-transceiver applications. All Stratix FPGA variants include the industry's most efficient and highest-performance logic, embedded memory, and DSP capabilities. Additionally, the Stratix IV GX and Stratix IV E device variants deliver a seamless, low-risk path to production volumes with our HardCopy IV ASICs, which include the option of integrated transceivers up to 6.5 Gbps. Stratix IV FPGAs are your best total solution for high-end system-on-a-chip (SOC) design.

Stratix IV family features summary

Stratix IV GT FPGAs	**Multi-gigabit transceivers**	Up to 24 high-speed transceiver channels (full duplex) operating from 2.488 Gbps to 11.3 Gbps. Up to 12 additional channels at 2.488 Gbps to 8.5 Gbps and up to 12 additional channels at 2.488 Gbps to 6.5 Gbps.
	Enhanced transceiver block	Two central clock management units (CMUs) per transceiver block, used for reference clock inputs and transmit PLLs. CMUs can be configured as transmit PLLs or as additional channels 5 and 6 in the transceiver block. In addition, up to four 6G and two 10G LC oscillators provide enhanced jitter and performance. Embedded PCS pattern detector, word aligner with programmable pattern byte reordering, 8b/10b encoder/decoder, protocol-specific hardware for PCI Express (PIPE) interface, XAUI, Gigabit Ethernet, and SONET.
	Protocol support	Support for 10G Ethernet, 10G Fibre Channel, SONET/SDH OC-192/STM-64, G.709 OUT-2, 40G/100G IEEE 802.3ba, Interlaken, SPAUI, DDR-XAUI, SFI-4.2, SFI-5.1, SF1-5.2, and SFI-S. Supports all Stratix IV GX protocols with data rates at 2.488 Gbps and higher, and 1 x4 PCI Express Gen1 and Gen2 hard IP block.
	Low-power transceiver	Typical PMA power consumption of 171 mW at 10.3 Gbps.
Stratix IV GX FPGAs	**Multi-gigabit transceivers**	Up to 48 high-speed transceiver channels (full duplex) with PLL-based clock data recovery (CDR). Up to 32 channels operating from 600 Mbps to 8.5 Gbps (6.5 Gbps industrial) and superior signal integrity. Up to 16 additional channels at 600 Mbps to 6.5 Gbps.
	Enhanced transceiver block	Two CMUs per transceiver block, used for reference clock inputs and transmit PLLs. CMUs can be configured as transmit PLLs or as additional channels 5 and 6 in the transceiver block. In addition up to four 6G LC oscillators provide enhanced jitter and performance. Embedded PCS pattern detector, word aligner with programmable pattern byte reordering, 8b/10b encoder/decoder, protocol-specific hardware for PCI Express (PIPE interface), XAUI, Gigabit Ethernet, and SONET.
	Protocol support	Support for PCI Express Gen1 and Gen2 (x1, x4, x8), XAUI/HiGig/HiGig+, Gigabit Ethernet, SRIO, Interlaken, CEI-6G, SONET OC-3/12/48, HyperTransport™ 3.0, SDI, ASI, GPON, SATA/SAS, CPRI, OBSAI, and 3G and 6G basic modes with rule-based protocol configuration.
	Plug & Play Signal Integrity	Support for adaptive equalization and hot socketing.
	PCI Express hard IP	Complete protocol solution with embedded PCI Express hard IP blocks, Gen1 and Gen2 (x1, x4, x8), that implement the PHY-MAC layer, data-link layer, and transaction layer functionality.
	Dynamic transceiver reconfiguration	Provides the capability to support multiple protocols and data rates on the same transceiver channel without reprogramming the FPGA.
	Low-power transceiver	Typical PMA power consumption of 100 mW at 3.125 Gbps and 135 mW at 6.375 Gbps per channel.

[1] All data is preliminary

Stratix IV family features summary (GT, GX, and E)

ALMs	With up to 530K equivalent LEs on the GT and GX variants and up to 680K equivalent LEs on the E variant, Stratix IV ALMs provide industry-leading performance and logic density with a patented fracturable eight-input LUT, two dedicated adders, and two registers. ALMs can integrate 80 percent more logic than competitive LUT architectures along with more registers, resulting in increased performance through reduced total logic levels and associated routing.
Performance	Fastest FPGA in the industry, through a high-speed fabric plus the most efficient routing architecture, as well as the industry's most efficient embedded memory and DSP architecture.
Programmable Power Technology	Every programmable logic array block (LAB), DSP block, and memory block delivers high speed or low power, depending on your design requirements. Using Programmable Power Technology in Stratix IV FPGAs, all functional blocks in the array, except those designated as timing critical, are set to low-power mode. Having only the timing-critical blocks set to high-speed mode reduces power dissipation in Stratix IV devices by up to 50 percent.
External memory interface circuitry	Stratix IV FPGAs provide the industry's highest performance external DRAM and SRAM memory interfaces, including DDR3, DDR2, QDR II, QDR, RLDRAM II, and RLDRAM. The dynamic self-calibrating PHY continuously compensates for PVT variations during operation. You can achieve higher performance, up to 1,067 Mbps (533 MHz), better signal integrity, increased robustness, expanded design margin, and lower power in your designs. Complete solutions including easy-to-use IP, hardware development platforms, and comprehensive timing analysis are available to minimize risk and speed time to market.
HardCopy ASIC series support	The HardCopy ASIC migration path is now available for both Stratix IV GX and E variants, with a single toolset across Stratix IV and HardCopy IV devices for enhanced productivity. All of the Stratix IV devices and the HardCopy IV ASICs are supported in Quartus II software.
MultiTrack interconnect	Connections between ALMs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure. Compared to competitors, the MultiTrack interconnect offers nearly 3X the number of one-hop interconnects between LABs, maximizing performance for challenging, time-critical logic. The interconnect has the industry's largest single-hop span of five LABs, minimizing routing congestion and further improving performance and routability. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.
TriMatrix memory	TriMatrix memory offers three memory block sizes to suit complex design needs: 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks. With up to 23 Mbits of memory performing at over 600 MHz and features such as dual-port RAM and integrated error correction code (ECC), TriMatrix memory is more flexible and efficient, and provides higher memory bandwidth than any other memory architecture. All three configurations support parity checking.
DSP blocks	Stratix IV DSP blocks provide more than twice as many multiplier resources as competing architectures, delivering the industry's fastest performance with up to 1,360 18-bit by 18-bit multipliers. DSP blocks include all associated pipelining, adders, and accumulators. They are configurable to support 9-bit x 9-bit, 12-bit x 12-bit, 18-bit x 18-bit, 18-bit x 36-bit, or 36-bit x 36-bit multipliers at up to 550 MHz and 748 giga multiply-accumulate operations per second (GMACS), making Stratix IV FPGAs ideal for custom-built DSP replacement, as well as coprocessing for hardware acceleration.
High-speed single-ended I/O support	Up to 24 modular I/O banks with programmable slew rate, programmable drive strength, programmable output delay, OCT, and dynamic trace compensation. Maximizes I/O flexibility and performance for over 40 industry standards to optimally match your system requirements.
High-speed differential I/O support	Optimized LVDS I/O pins at between 150-MHz and 1.6-GHz performance provide high performance and excellent signal integrity with half the capacitance of competitive devices. Stratix IV LVDS supports hard dynamic phase alignment (DPA) and serializer/deserializer (SERDES) blocks with clock forwarding for soft CDR in high-speed chip-to-chip applications. MegaWizard™ plug-ins make differential I/O configuration straightforward and easy.
DPA	As a feature of the LVDS high-speed differential I/O support, DPA minimizes bit errors and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
OCT	Serial, parallel, dynamic, and differential OCT simplifies design and reduces component count. Dynamic OCT enables support for next-generation memory interface designs that must dynamically switch between serial and parallel termination. Digital calibration circuitry provides industry-leading OCT tolerance within 10 percent.
Clock management features	Each variant has up to 12 PLLs with up to 10 unique customizable outputs per PLL ranging from 5 to 720 MHz. There are also up to 16 global, 88 quadrant, and 132 periphery clocks. Advanced clock management features include PLL reconfiguration, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	Volatile and non-volatile design security protects FPGA design and IP against copying, reverse engineering, and tampering.
Remote system upgrades	This capability enables reliable and safe deployment of in-system enhancements and bug fixes.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	Automatic SEU detection circuitry utilizes 32-bit CRC with criticality processor to determine the importance of error.
Nios® II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Stratix IV FPGAs offers up to 340-DMIPS[1] performance.

[1] All data is preliminary

Stratix IV transceiver protocol support

Protocol	Stratix IV GT data rates (Gbps)	Stratix IV GX data rates (Gbps)
ASI	-	0.27
Basic (proprietary)	2.488 - 11.3	0.6-8.5
CEI-6G (SR,LR)	4.976-6.375	4.976-6.375
CPRI	3.072	0.6144, 1.2288, 2.4576, 3.072
10G Ethernet (XAUI)	3.125	3.125
10G Ethernet (XFI, SFI)	10.3125	-
40G, 100G Ethernet	10.3125	-
Gigabit Ethernet	1.25 (LVDS based)	1.25
Fibre Channel	4.25, 8.5, 10.51875	1.0625, 2.125, 4.25, 8.5
GPON	2.488 downlink	1.244 uplink, 2.488 downlink
G.709 OTU-2	10.7	-
OTN 10 Gigabit Ethernet w/FEC	11,1, 11.3	
HiGig+	3.75	3.75
HyperTransport™ 3.0	2.8, 3.2	0.4, 2.4, 2.8, 3.2
Interlaken	3.125-6.375	3.125-6.375
OBSAI	3.072	0.768, 1.536, 3.072
PCI Express Gen1, Gen2	2.5, 5	2.5, 5
PCI Express Cable	2.5	2.5
RXAUI	6.25	6.25
SAS	3, 6	1.5, 3, 6
SATA	3, 6	1.5, 3, 6
3G-SDI	2.97	2.97
SDI SD/HD	-	0.27/1.485
SerialLite II	2.488-6.375	0.6-6.375
Serial RapidIO®	2.5, 3.125	1.25, 2.5, 3.125
SFI-5.1	2.488-3.125	2.488-3.125
SFI-5.2	9.9-11.3	-
SONET OC-3/OC-12/OC-48/OC-192	NA/NA/2.488/9.954	0.155/0.622/2.488/NA

Stratix® III

65-nm high-performance, high-end FPGAs

Altera's Stratix III FPGAs were designed to address your design and business challenges, anticipate the unforeseen, and help you win in your market. The Stratix III family supports your applications' increased levels of integration and complexity with higher densities and performance, while decreasing power consumption. Its flexible and efficient logic architecture, enhanced memory blocks, and high-capacity DSP blocks meet your system's most demanding requirements.

Specifically designed for ease of use and rapid system integration, the Stratix III FPGA family offers two variants optimized to meet different application needs. Stratix III L FPGAs deliver balanced logic, memory, and DSP resources for general-purpose applications; Stratix III E FPGAs provide enhanced memory and DSP resources for memory- and DSP-intensive applications. Both variants include fast, flexible, and robust I/O connectivity, providing DDR3 DIMM memory interface support up to 1,067 Mbps/533 MHz.

Stratix III family features summary

HardCopy ASIC series support	This pin-compatible HardCopy ASIC reduces cost and power for volume applications.
Programmable Power Technology	The core logic, routing, memory, and DSP blocks in Stratix III FPGAs have fine-grained control over whether a specific tile is in high-speed mode or low-power mode. Quartus II design software automatically applies the high-speed mode to all parts of the design that require the highest performance, utilizing the low-power mode for all other parts of the FPGA. Leakage power is reduced by about 70 percent for the portions of the design implemented with low-power mode.
Selectable core voltage	The core voltage of Stratix III FPGAs can be set depending on performance requirements—to the 1.1V setting for the highest performance and 0.9V for the lowest power. The 0.9V setting reduces dynamic power by 55 percent over previous-generation 1.2V devices. The core voltage setting is independent of Programmable Power Technology.
ALMs	ALMs provide industry-leading performance and logic density with a patented fracturable eight-input LUT, two dedicated adders, and two registers. ALMs integrate 80 percent more logic than competitive LUT architectures along with more registers, resulting in increased performance through reduced total logic levels and associated routing.
MultiTrack interconnect	Connections between ALMs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure. Compared to competitors, the MultiTrack interconnect offers nearly 3X the number of one-hop interconnects between LABs, maximizing performance for challenging, time-critical logic. The interconnect has the industry's largest single-hop span of five LABs, minimizing routing congestion and further improving performance and routability. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.
TriMatrix memory	TriMatrix memory offers three memory block sizes to suit complex design needs: 640-bit MLABs, 9-Kbit M9K blocks, and 144-Kbit M144K blocks. With up to 21 Mbits of memory performing at over 600 MHz and features such as dual-port RAM and integrated ECC, TriMatrix memory is more flexible and efficient, and provides higher memory bandwidth than any other memory architecture. All three configurations support parity checking.
DSP blocks	DSP blocks provide twice as many multiplier resources as competing architectures, with up to 896 18-bit x 18-bit multipliers on the EP3SE110 device. DSP blocks include all associated pipelining, adders, and accumulators. They are configurable to support 9-bit x 9-bit, 12-bit x 12-bit, 18-bit x 18-bit, 36-bit x 36-bit, or 18-bit x 36-bit multipliers at up to 550 MHz.
External memory interface circuitry	Stratix III FPGAs provide the industry's highest performance external DRAM and SRAM memory interfaces, including DDR3, up to 1,067-Mbps DIMM memory interface support, PVT-compensated dedicated hard I/O structures with OCT, trace compensation, read/write leveling, and half- and full-rate registered outputs. Complete solutions, including easy-to-use IP, hardware development platforms, and comprehensive timing analysis, are available to minimize risk and speed time to market.
High-speed single-ended I/O support	Up to 24 modular I/O banks with dedicated DQ/DQS circuitry, programmable slew rate, programmable drive strength, programmable output delay, OCT, and dynamic trace compensation maximize I/O flexibility and performance for over 40 industry standards to optimally match your system requirements.
High-speed differential I/O support	Optimized LVDS I/O pins provide high performance and excellent signal integrity with half the capacitance of competitive devices. Stratix III LVDS supports hard DPA and SERDES blocks with clock forwarding for clock data recovery in high-speed chip-to-chip applications. Wizards make differential I/O configuration straightforward and easy.
DPA	DPA minimizes bit errors and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
OCT	Serial, parallel, dynamic, and differential OCT simplifies design and reduces component count. Dynamic OCT enables support for next-generation memory interface designs that must dynamically switch between serial and parallel termination. Digital calibration circuitry provides industry-leading OCT tolerance within 10 percent.
Clock management features	Each product family has up to 12 PLLs with up to 10 unique customizable outputs per PLL ranging from 5 to 720 MHz. There are also up to 16 global, 88 quadrant, and 208 periphery clocks. Advanced clock management features include PLL reconfiguration, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	To prevent IP theft and product tampering, the devices feature configuration bitstream encryption using the Advanced Encryption Standard (AES) and 256-bit key. Stratix III FPGAs are the industry's only design security solution with both non-volatile and volatile key options. The non-volatile key is more practical, easy to use, and low cost, while the volatile key is reprogrammable.
Remote system upgrades	This capability enables reliable and safe deployment of in-system enhancements and bug fixes.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	The devices feature automatic SEU detection circuitry utilizing 32-bit CRC with criticality processor to determine the importance of error.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Stratix III FPGAs offers up to 340-DMIPS performance.

Stratix II

90-nm high-performance, high-density FPGAs with 6.375-Gbps transceiver option

Stratix II devices are the industry's leading 90-nm high-density, high-performance FPGAs. Built on an ALM logic structure to maximize performance and minimize power, Stratix II devices on average deliver 50 percent faster performance than prior-generation FPGAs. The Stratix II device family has variants both with and without transceivers. The Stratix II GX devices are the family's transceiver variant with 20 low-power, high-speed channels and data rates from 600 Mbps to 6.375 Gbps. Dynamically configurable transmit pre-emphasis and receiver equalization optimizes signal integrity under adverse channel conditions. The transceivers are capable of driving FR-4 backplanes at 6.375 Gbps and have proven to be interoperable with backplanes and transceivers from multiple vendors. In addition, the PCS hard IP, which is part of the transceiver block, saves valuable logic resources and simplifies protocol support.

Stratix II GX features summary

Excellent signal integrity, 600 Mbps to 6.375 Gbps	The transmitter has low jitter generation and up to 500 percent pre-emphasis. The receiver has excellent jitter tolerance and up to 17-dB of equalization.
Low power	The transceiver (including both PMA and PCS blocks) dissipates 200 mW per channel at 6.375 Gbps and only 140 mW per channel at 3.125 Gbps.
PCS support (hard IP)	The transceiver supports the following PCS blocks: PCI Express, PIPE-compliant PCS, CEI-6G, 8b/10b encoder/decoder, XAUI state machine and channel bonding, Gigabit Ethernet state machine, SONET, and 8/10/16/20/32/40-bit interface (to logic).
System-level diagnostics	Serial loopback, reverse serial loopback, psuedo-random binary sequence (PRBS) generator checker, and register-based interface facilitate dynamic reconfiguration of pre-emphasis, equalization, and differential output voltage.

Stratix II family features summary (with and without GX transceivers)

HardCopy II ASIC support	This pin-compatible HardCopy ASIC reduces cost and power for volume applications. (Not available for Stratix II GX transceiver variant.)
ALMs	ALMs provide industry-leading performance and logic density with a patented fracturable eight-input LUT, two dedicated adders, and two registers. ALMs deliver 80 percent greater logic density than competitive architectures along with more registers, resulting in increased performance through reduced total logic levels and associated routing.
MultiTrack interconnect	Connections between ALMs, TriMatrix memory blocks, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure. Compared to competitors, the MultiTrack interconnect offers nearly 3X the number of one-hop interconnects between LABs, maximizing performance for challenging, time-critical logic. The interconnect has the industry's largest single-hop span of five LABs, minimizing routing congestion and further improving performance and routability. The Quartus II compiler automatically places critical design paths on faster interconnects to maximize performance.
TriMatrix memory	TriMatrix memory in Stratix II FPGAs provides up to 9 Mbits of memory in three block sizes: 512 bits in the M512, 4 Kbits in the M4K, and 500 Kbits in the M-RAM blocks. TriMatrix memory includes parity checking and is capable of up to 550-MHz performance.
DSP blocks	Each DSP block includes multipliers with associated pipelining, adders, and accumulators. Stratix II FPGAs include up to 96 DSP blocks offering 384 18-bit x 18-bit multipliers that operate at up to 450 MHz. Each multiplier can be configured as 9-bit x 9-bit, 18-bit x 18-bit, or 36-bit x 36-bit multipliers.
External memory interface circuitry	Fully characterized and hardware-validated circuitry provides flexible, high-performance interfaces to the latest external DRAM and SRAM memory technologies. Complete solutions, including easy-to-use IP, hardware development platforms, and comprehensive timing analysis, are available to minimize risk and speed time to market.
High-speed differential I/O support	Optimized LVDS I/Os with DPA and SERDES capability provides high performance and excellent signal integrity. Wizards make differential I/O configuration straightforward and easy.
DPA	DPA maximizes signal integrity and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.

Stratix II family features summary (with and without GX transceivers) (continued)

OCT	Serial and differential OCT simplifies design and reduces component count. Digital calibration circuitry provides industry-leading OCT tolerance within five percent.
Clock management features	Up to 12 PLLs and up to 48 system clocks. Advanced clock management features include PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	Configuration bitstream encryption using 128-bit AES prevents IP theft and product tampering. The non-volatile key storage makes the solution reliable, easy to use, and low cost.
Remote system upgrades	Enables reliable and safe deployment of in-system enhancements and bug fixes.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Automatic SEU detection circuitry	Features automatic SEU detection circuitry utilizing 32-bit CRC.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for Stratix II FPGAs offers up to 250-DMIPS performance.

Stratix II GX protocol support

Protocol	Data rate (Gbps)
ASI	0.27
CEI-6G/SR/LR	6.375/4.976–6.375/4.976–6.375
CPRI	0.6144, 1.2288, 2.4576, 3.072
Ethernet-XAUI	4 x 3.125
Fibre Channel	1.0625, 2.125, 4.25
Gigabit Ethernet	1.25
HiGig+	3.75
HiGig2	4.0625
Interlaken	3.125–6.375
OBSAI	0.768, 1.536, 3.072
PCI Express 1.1/2.0	2.5, 5
PCI Express Cable	2.5
3G-SDI	2.97
Serial RapidIO	1.25, 2.5, 3.125
SONET OC-3/OC-12/OC-48	0.155, 0.622, 2.488

Stratix FPGA series package and I/O matrices

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices only offered in industrial temperatures (0°C to 100°C).

Stratix IV GT FPGAs (0.9V) up to 11.3-Gbps transceivers [1]

	Pin count	EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3	EP4S100G4	EP4S100G5
FBGA (F)	1,517 pin	636	636[2]	636			636[2]
	1,932 pin				754	754	754

[1] All data is preliminary

[2] Hybrid package (flip chip) FBGA

368 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

Stratix IV GX FPGAs (0.9V) up to 8.5-Gbps transceivers [1]

	Pin count	EP4SGX70D	EP4SGX70H	EP4SGX110D	EP4SGX110F	EP4SGX110H	EP4SGX180D	EP4SGX180F	EP4SGX180H	EP4SGX180K	EP4SGX230D	EP4SGX230F	EP4SGX230H	EP4SGX230K	EP4SGX290F	EP4SGX290H	EP4SGX290K	EP4SGX290N	EP4SGX360F	EP4SGX360H	EP4SGX360K	EP4SGX360N	EP4SGX530H	EP4SGX530K	EP4SGX530N
FBGA (F)	780 pin	368		368			368				368				288[2]				288[2]						
	1,152 pin				368			560				560			560				560						
	1,152 pin		480			480			560				560			560				560			560[2]		
	1,517 pin									736				736			736				736			736[2]	
	1,760 pin																864				864			864	
	1,932 pin																	904				904			904

[1] All data is preliminary

[2] Hybrid package (flip chip) FBGA

Stratix FPGA series package and I/O matrices

288 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

		Stratix III[2] L FPGAs Balanced logic, memory, and DSP						Stratix III[2] E FPGAs Memory/DSP Enhanced				Stratix IV[1] E FPGA High-density, high-performance, low-power					
	Pin count	EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340	EP3SE50	EP3SE80	EP3SE110	EP3SE260[3]	EP4SE110	EP4SE230	EP4SE290	EP4SE360	EP4SE530	SP4SE680
FBGA (F)	484 pin	288	288					288									
	780 pin	480	480	480	480	480[2]		480	480	480	480[2]	480	480	480[2]	480[2]		
	1,152 pin			736	736	736	736[2]		736	736	736			736	736	736[2]	736[2]
	1,517 pin					960	960				960			864	864	960[2]	960
	1,760 pin						1,104									960	1,104

[1] All data is preliminary

[2] Hybrid package (flip chip) FBGA

[3] EP3SE260 FPGAs are the optimum solution for both logic (Stratix III L FPGA) and DSP/memory (Stratix III E FPGA) applications at this density.

342 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

		Stratix II FPGAs (1.2V) High density, high performance						Stratix II GX FPGAs (1.2V) 6.375-Gbps transceivers							
	Pin count	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180	EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
FBGA (F)	484 pin (flip chip)	342	342	334											
	672 pin (flip chip)	366	500	492											
	780 pin				534	534		361	361	364	364				
	1,020 pin			718	758	742	742								
	1,152 pin											534	558		
	1,508 pin				902	1,126	1,170							650	734
Hybrid FBGA (H)	484 pin				308										

Stratix FPGA series features

		Stratix IV GT FPGAs (0.9V) up to 11.3-Gbps transceivers[1]					
		EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3	EP4S100G4	EP4S100G5
Density and speed	Equivalent LEs	228,000	531,200	228,000	291,200	353,600	531,200
	ALMs	91,200	212,480	91,200	116,480	141,440	212,480
	Registers[2]	182,400	424,960	182,400	232,960	282,880	424,960
	M9K memory blocks	1,235	1,280	1,235	936	1,248	1,280
	M144K memory blocks	22	64	22	36	48	64
	Embedded memory (Mbits)	13.9	20.3	13.9	13.3	17.7	20.3
	MLAB memory (Kbits)	2,850	6,640	2,850	3,640	4,420	6,640
	Maximum 18-bit x 18-bit multipliers	1,288	1,024	1,288	832	1,024	1,024
	Speed grades (fastest to slowest)	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others					
	Global clock networks	16	16	16	16	16	16
	Regional clock networks	64	88	64	88	88	88
	Periphery clock networks	88	112	88	112	112	112
	PLLs/unique outputs	8/68	12/96	8/68	12/96	12/96	12/96
	Design security	✓	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)					
	Emulated LVDS channels	192	256	192	256	256	256
	Number of LVDS channels, 1.6 Gbps (receive/transmit)	44/44	44/44	44/44	44/44	44/44	44/44
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) channels (2.488 Gbps - 11.3 Gbps with PCS + PMA)	12	12	24	24	24	24
	Transceiver (SERDES) channels[4] (2.488 Gbps - 8.5 Gbps with PCS + PMA)	12	12	0	8	8	8
	Transceiver (SERDES) channels[4] (2.488 Gbps - 6.5 Gbps with PMA only)	12	12	12	16	16	16
	PCI Express hard IP blocks	0	0	0	1	1	1
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					
Configuration file sizes	Configuration file size (Mbits)	102	189	102	189	189	189

[1] All data is preliminary. Available in industrial temperatures only (0ºC to 100ºC).

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

[3] 3.3V compliant, requires a 3.0V power supply

[4] These are additional transceivers; total transceiver count is sum of 11.3-Gbps transceivers plus 8.5-Gbps transceivers plus 6.5-Gbps transceivers.

Stratix FPGA series features

		Stratix IV E FPGAs (0.9V) High density, high performance, low power [1]					
		EP4SE110	EP4SE230	EP4SE290	EP4SE360	EP4SE530	EP4SE680
Density and speed	Equivalent LEs	105,600	228,000	291,200	353,600	531,200	681,100
	ALMs	42,240	91,200	116,480	141,440	212,480	272,440
	Registers[2]	84,480	182,400	232,960	282,880	424,960	544,880
	M9K memory blocks	660	1,235	936	1,248	1,280	1,529
	M144K memory blocks	16	22	36	48	64	64
	Embedded memory (Mbits)	8.1	13.9	13.3	17.7	20.3	22.4
	MLAB memory (Kbits)	1,320	2,850	3,640	4,420	6,640	8,514
	Maximum 18-bit x 18-bit multipliers	512	1,288	832	1,040	1,024	1,360
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-3, -4
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others					
	Global clock networks	16	16	16	16	16	16
	Regional clock networks	64	64	88	88	88	88
	Periphery clock networks	56	88	88	88	112	112
	PLLs/unique outputs	4/34	4/34	12/96	12/96	12/96	12/96
	Design security	✓	✓	✓	✓	✓	✓
	HardCopy series device support	HC4E2	HC4E3	HC4E4	HC4E5	HC4E6	HC4E7
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)					
	Emulated LVDS channels	128	128	256	256	256	288
	Number of LVDS channels, 1.6 Gbps (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					
Configuration file sizes	Configuration file size (Mbits)	52	102	140	140	189	230

[1] All data is preliminary

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

[3] 3.3V compliant, requires a 3.0V power supply

Stratix FPGA series features

Stratix IV GX FPGAs (0.9V) up to 8.5-Gbps transceivers [1]

		EP4SGX70D	EP4SGX70H	EP4SGX110D	EP4SGX110F	EP4SGX110H	EP4SGX180D	EP4SGX180F	EP4SGX180H	EP4SGX180K	EP4SGX230D
Density and speed	Equivalent LEs	72,600	72,600	105,600	105,600	105,600	175,750	175,750	175,750	175,750	228,000
	ALMs	29,040	29,040	42,240	42,240	42,240	70,300	70,300	70,300	70,300	91,200
	Registers[2]	58,080	58,080	84,480	84,480	84,480	140,600	140,600	140,600	140,600	182,400
	M9K memory blocks	462	462	660	660	660	950	950	950	950	1,235
	M144K memory blocks	16	16	16	16	16	20	20	20	20	22
	Embedded memory (Mbits)	6.3	6.3	8.1	8.1	8.1	11.1	11.1	11.1	11.1	13.9
	MLAB memory (Kbits)	908	908	1,320	1,320	1,320	2,197	2,197	2,197	2,197	2,850
	Maximum 18-bit x 18-bit multipliers	384	384	512	512	512	920	920	920	920	1,288
	Speed grades (fastest to slowest)	-2x[3], -3, -4	-2, -3, -4	-2x[3], -3, -4	-2x[3], -3, -4	-2, -3, -4	-2x[3], -3, -4	-2x[3], -3, -4	-2, -3, -4	-2, -3, -4	-2x[3], -3, -4
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others									
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	Regional clock networks	64	64	64	64	64	64	64	64	64	64
	Periphery clock networks	56	56	56	56	56	88	88	88	88	88
	PLLs/unique outputs	3/27	4/34	4/34	4/34	4/34	3/27	6/54	6/54	8/68	3/27
	Design security	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy series device support	HC4GX1	–	HC4GX2		–	HC4GX2	HC4GX2	HC4GX2	HC4GX3	HC4GX3
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[4]									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)									
	Emulated LVDS channels	128	128	128	128	128	128	192	192	192	128
	Number of LVDS channels, 1.6 Gbps (receive/transmit)	28/28	56/56	28/28	28/28	56/56	28/28	44/44	44/44	88/88	28/28
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) channels (600 Mbps–8.5 Gbps with PCS + PMA)	8	16	8	16	16	8	16	16	24	8
	Transceiver (SERDES) channels[5] (600 Mbps–6.5 Gbps with PMA only)	–	8	–	–	8	–	–	8	12	–
	PCI Express hard IP blocks	1	2	1	2	2	1	2	2	2	1
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR									
Configuration file sizes	Configuration file size (Mbits)	52	52	52	52	52	102	102	102	102	102

[1] All data is preliminary

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

[3] Support for -2 core and -3 1/O speed-grade. Support for PCI Express Gen1 and Gen2 x8.

[4] 3.3V compliant, requires a 3.0V power supply

[5] These are additional transceivers, total transceiver count is sum of 8.5-Gbps transceivers plus 6.5-Gbps transceivers.

Stratix FPGA series features

Stratix IV GX FPGAs (0.9V) up to 8.5-Gbps transceivers [1]

EP4SGX230F	EP4SGX230H	EP4SGX230K	EP4SGX290F	EP4SGX290H	EP4SGX290K	EP4SGX290N	EP4SGX360F	EP4SGX360H	EP4SGX360K	EP4SGX360N	EP4SGX530H	EP4SGX530K	EP4SGX530N
228,000	228,000	228,000	291,200	291,200	291,200	291,200	353,600	353,600	353,600	353,600	531,200	531,200	531,200
91,200	91,200	91,200	116,480	116,480	116,480	116,480	141,440	141,440	141,440	141,440	212,480	212,480	212,480
182,400	182,400	182,400	232,960	232,960	232,960	232,960	282,880	282,880	282,880	282,880	424,960	424,960	424,960
1,235	1,235	1,235	936	936	936	936	1,248	1,248	1,248	1,248	1,280	1,280	1,280
22	22	22	36	36	36	36	48	48	48	48	64	64	64
13.9	13.9	13.9	13.3	13.3	13.3	13.3	17.7	17.7	17.7	17.7	20.3	20.3	20.3
2,850	2,850	2,850	3,640	3,640	3,640	3,640	4,420	4,420	4,420	4,420	6,640	6,640	6,640
1,288	1,288	1,288	832	832	832	832	1,040	1,040	1,040	1,024	1,024	1,024	1,024
-2x[3], -3, -4	-2, -3, -4	-2, -3, -4	-2x[3], -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2x[3], -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4
Nios II processor, as well as partner processors from ARM, Freescale, and others													
16	16	16	16	16	16	16	16	16	16	16	16	16	16
64	64	64	88	88	88	88	88	88	88	88	88	88	88
88	88	88	88	88	88	88	88	88	88	88	112	112	112
6/54	6/54	8/68	6/54	6/54	12/96	12/96	6/54	6/54	12/96	12/96	6/54	12/96	12/96
✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HC4GX3			HC4GX4	HC4GX4			HC4GX5				HC4GX6		
1.2, 1.5, 1.8, 2.5, 3.3[4]													
LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)													
192	192	192	144	192	256	256	144	192	256	256	192	256	256
44/44	44/44	88/88	0/0	44/44	88/88	98/98	0/0	44/44	88/88	98/98	44/44	88/88	98/98
✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
16	16	24	16	16	24	32	16	16	24	32	16	24	32
–	8	12	–	8	12	16	–	8	12	16	8	12	16
2	2	2	2	2	2	4	2	2	2	4	2	4	4
DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR													
102	102	102	140	140	140	189	140	140	140	189	189	189	189

[1] All data is preliminary

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

[3] Support for -2 core and -3 I/O speed grade. Support for PCI Express Gen1 and Gen2 x8

[4] 3.3V compliant, requires a 3.0V power supply

[5] These are additional transceivers, total transceiver count is sum of 8.5-Gbps transceivers plus 6.5-Gbps transceivers.

Stratix FPGA series features

		Stratix III L FPGAs Balanced logic, memory, and DSP						Stratix III E FPGAs Memory/DSP enhanced			
		EP3SL50	EP3SL70	EP3SL110	EP3SL150	EP3SL200	EP3SL340	EP3SE50	EP3SE80	EP3SE110	EP3SE260
Density and speed	Equivalent LEs	47,500	67,500	107,500	142,500	198,900	338,000	47,500	80,000	107,500	254,400
	ALMs	19,000	27,000	42,600	56,800	79,560	135,200	19,000	32,000	42,600	101,760
	Registers[1]	38,000	54,000	85,200	113,600	159,120	270,400	38,000	64,000	85,200	203,520
	M9K memory blocks	108	150	275	355	468	1,040	400	495	639	864
	M144K memory blocks	6	6	12	16	36	48	12	12	16	48
	Embedded memory (Kbits)	1,836	2,214	4,203	5,499	9,396	16,272	5,328	6,183	8,055	14,688
	MLAB memory (Kbits)[2]	297	422	672	891	1,250	2,109	297	500	672	1,594
	Maximum 18-bit x 18-bit multipliers	216	288	288	384	576	576	384	672	896	768
	Speed grades (fastest to slowest)	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4	-2, -3, -4
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others									
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	Regional clock networks	48	48	48	48	88	88	48	48	48	88
	Periphery clock networks	104	104	208	208	208	208	104	208	208	208
	PLLs/unique outputs	4/34	4/34	8/68	8/68	12/96	12/96	4/34	8/68	8/68	12/96
	Design security	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy series device support	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0									
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS									
	True-LVDS data rate (Mbps)	125–1,600									
	Number of LVDS channels (receive/transmit)	56/56	56/56	88/88	88/88	112/112	132/132	56/56	88/88	88/88	112/112
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR									
Configuration file sizes	Configuration file size (Mbits)	22	22	47	47	66	120	26	48	48	93

1 This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which can increase total register count by an additional 50 percent.
2 MLAB ROM mode values are twice those of MLAB RAM (Kbits).

Stratix FPGA series features

		Stratix II GX FPGAs (1.2V) 6.375-Gbps transceivers							
		EP2SGX30C	EP2SGX30D	EP2SGX60C	EP2SGX60D	EP2SGX60E	EP2SGX90E	EP2SGX90F	EP2SGX130G
Density and speed	Equivalent LEs	33,880	33,880	60,440	60,440	60,440	90,960	90,960	132,540
	ALMs	13,552	13,552	24,176	24,176	24,176	36,384	36,384	53,016
	ALUTs	27,104	27,104	48,352	48,352	48,352	72,768	72,768	106,032
	Total RAM (Kbits)[1]	1,338	1,338	2,485	2,485	2,485	4,415	4,415	6,590
	M512 RAM blocks (512 bits + 64 parity bits)	202	202	329	329	329	488	488	699
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	144	144	255	255	255	408	408	609
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	1	1	2	2	2	4	4	6
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	64/128	64/128	144/288	144/288	144/288	192/384	192/384	252/504
	Speed grades (fastest to slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others							
	DSP blocks	16	16	36	36	36	48	48	63
	I/O registers per I/O element	6	6	6	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	48	48	48	48	48	48	48	48
	PLLs/unique outputs	4/18	4/18	4/18	4/18	8/36	8/36	8/36	8/36
	Design security	✓	✓	✓	✓	✓	✓	✓	✓
	HardCopy series device support	–	–	–	–	–	–	–	–
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVDS, LVPECL, HyperTransport, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS							
	True-LVDS data rate (Mbps)	125–1,000							
	True-LVDS channels (receive/transmit)	31/29	31/29	31/29	31/29	42/42	47/45	59/59	73/71
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps–6.375 Gbps							
	Transceiver (SERDES) channels	4	8	4	8	12	12	16	20
External memory interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR							
Configuration file sizes	Configuration file size (Mbits)	10	10	17	17	17	28	28	40

[1] Kbits = 1,024 bits

Stratix FPGA series features

		Stratix II FPGAs (1.2V) High density, high performance					
		EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
Density and speed	Equivalent LEs	15,600	33,880	60,440	90,960	132,540	179,400
	ALMs	6,240	13,552	24,176	36,384	53,016	71,760
	ALUTs	12,480	27,104	48,352	72,768	106,032	143,520
	Total RAM (Kbits)[1]	410	1,338	2,485	4,415	6,590	9,163
	M512 RAM blocks (512 bits + 64 parity bits)	104	202	329	488	699	930
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	78	144	255	408	609	768
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	0	1	2	4	6	9
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	48/96	64/128	144/288	192/384	252/504	384/768
	Speed grades (fastest to slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others					
	DSP blocks	12	16	36	48	63	96
	I/O registers per I/O element	6	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	48	48	48	48	48	48
	PLLs/unique outputs	6/28	6/28	12/56	12/56	12/56	12/56
	Design security	✓	✓	✓	✓	✓	✓
	HardCopy series device support	–	✓	✓	✓	✓	✓
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, HyperTransport, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II),1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	True-LVDS data rate (Mbps)	125–1,000					
	True-LVDS channels (receive/transmit)	38/38	58/58	80/84	114/118	152/156	152/156
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR2, DDR, QDR II, RLDRAM II, SDR					
Configuration file sizes	Configuration file size (Mbits)	5	10	17	28	40	53

[1] Kbits = 1,024 bits

FOR MORE INFORMATION

Stratix IV FPGAs	www.altera.com/stratix4
Stratix III FPGAs	www.altera.com/stratix3
Stratix II FPGAs	www.altera.com/stratix2
Training	www.altera.com/training

HardCopy ASIC series

Altera's HardCopy® system development methodology delivers the lowest total cost, lowest risk system designs. This methodology speeds the design of deep sub-micron HardCopy ASICs by employing the ease and flexibility of FPGA-based system design. This unique flow allows true hardware/software co-design and co-verification, so you can deliver your system to market sooner—on average 9 to 12 months faster than standard-cell solutions.

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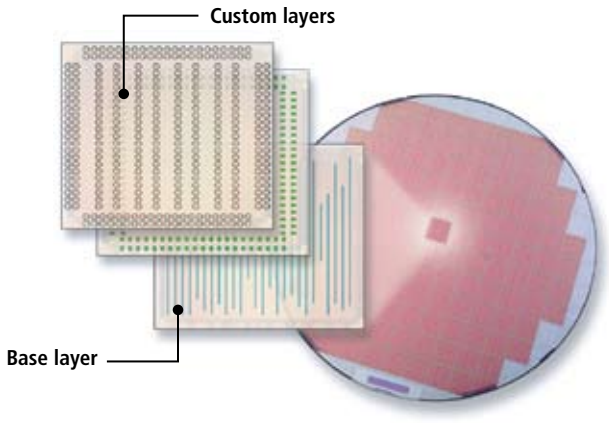
HardCopy ASIC



Key features

- System development methodology
  - Design-once seamless prototyping
  - True software/hardware co-design and co-verification
  - 9- to 12-month faster system availability
  - Fast and predictable design handoff to production HardCopy ASIC silicon
- Dramatically lower power, increased SEU immunity, increased security, and lower bill of materials (BOM) cost compared to FPGAs

HardCopy® IV

40-nm HardCopy ASICs with 6.5+ Gbps transceiver option

The HardCopy IV ASIC family offers the benefits of FPGAs and the benefits of ASICs. HardCopy IV ASICs deliver the lowest risk, lowest total cost, and fastest time to market available in leading-edge ASIC technology today, as well as risk-free, seamless prototyping on a Stratix IV family FPGA. The HardCopy IV family meets your diverse application needs in markets including wireless, wireline, high-performance computing, high-reliability computing, storage, military, and more. The HardCopy IV family has two family variants: HardCopy IV GX and HardCopy IV E devices. Both the HardCopy IV GX and HardCopy IV E variants include high-performance logic—up to 11.5M and 13.3M ASIC gates respectively, and up to 20.3 Mbits of memory. Additionally, HardCopy IV GX ASICs feature up to 36 transceiver channels with up to 6.5+ Gbps bandwidth.

HardCopy IV family features summary (GX only)

Equivalent SERDES block to Stratix IV GX FPGAs	Same transceivers, same hard IP as Stratix IV GX companion devices.
Multi-gigabit transceivers (PMA and PCS features)	Up to 24 high-speed transceiver channels (full duplex) with PLL-based CDR operating from 600 Mbps to 6.5 Gbps (6.5 Gbps industrial) and superior signal integrity.
Enhanced transceiver block	Two central CMUs per transceiver block, used for reference clock inputs and transmit PLLs. CMUs can be configured as transmit PLLs or as additional channels 5 and 6 in transceiver block. Embedded PCS pattern detector, word aligner with programmable pattern byte reordering, 8b/10b encoder/decoder, protocol-specific hardware for PCI Express (PIPE interface), XAUI, Gigabit Ethernet, and SONET.
Protocol support	Support for PCI Express Gen1 and Gen2, XAUI/HiGig-XAUI, Gigabit Ethernet, SRIO, Interlaken, CEI-6G, SONET OC-3/12/48, SDI, ASI, GPON, SATA, 3G and 6G basic modes with rule-based protocol configuration.
Plug & Play Signal Integrity	Support for adaptive equalization and hot socketing.
PCI Express hard IP	Complete protocol solution with embedded PCI Express hard IP blocks, v1.1 and v2.0, that implement PHY-MAC layer, data-link layer, and transaction layer functionality.
Dynamic transceiver reconfiguration	Provides the capability to support multiple protocols and data rates on the same transceiver channel in a single HardCopy ASIC.
Low-power transceiver	Typical PMA power consumption of 100 mW at 3.125 Gbps and 135 mW at 6.375 Gbps per channel.

HardCopy IV family features summary (E and GX)

Seamless prototyping	HardCopy IV ASIC seamless prototyping on Stratix IV FPGAs is available for both GX and E variants. Single toolset across HardCopy IV and Stratix IV devices for enhanced productivity. All of the HardCopy IV and Stratix IV devices are supported in Quartus II software.
External memory interface circuitry	HardCopy IV ASICs support external DRAM and SRAM memory interfaces, including DDR3, DDR2, QDR II, QDR, RLDRAM II, and RLDRAM. The dynamic self-calibrating PHY continuously compensates for PVT variations during operation. You can achieve higher performance, up to 800 Mbps (400 MHz), better signal integrity, increased robustness, expanded design margin, and lower power in your designs. Complete solutions including easy-to-use IP, hardware development platforms, and comprehensive timing analysis are available to minimize risk and speed time to market.
TriMatrix memory	TriMatrix memory offers three memory block sizes to suit complex design needs: 640-bit MLABs, 9-Kbit M9K blocks, and 144-Kbit M144K blocks. With up to 16.8 Mbits of memory performing at over 600 MHz and features such as dual-port RAM and integrated ECC, TriMatrix memory is more flexible and efficient, and provides higher memory bandwidth than any other memory architecture. All three configurations support parity checking.
DSP blocks	HardCopy IV ASICs support up to 1,288 multipliers. All DSP block circuitry used will be implemented in HCell logic, the basic building block used for logic implementation. DSP blocks include all associated pipelining, adders, and accumulators. They are configurable to support 9-bit x 9-bit, 12-bit x 12-bit, 18-bit x 18-bit, or 36-bit x 36-bit multipliers at up to 455 MHz and 586 GMACS, making HardCopy IV ASICs ideal for custom-built DSP replacement, as well as coprocessing for hardware acceleration.
High-speed single-ended I/O support	Up to 20 modular I/O banks with programmable slew rate, programmable drive strength, programmable output delay, OCT, and dynamic trace compensation. Maximizes I/O flexibility and performance for over 40 industry standards to optimally match your system requirements. I/O configuration will be fixed after design handoff to design center.
High-speed differential I/O support	Optimized LVDS I/O pins at between 150-MHz and 1.25-GHz performance provide high performance and excellent signal integrity with half the capacitance of competitive devices. HardCopy IV LVDS supports hard DPA and SERDES blocks with clock forwarding for CDR in high-speed chip-to-chip applications. MegaWizard plug-ins make differential I/O configuration straightforward and easy.
DPA	As a feature of the LVDS high-speed differential I/O support, DPA minimizes bit errors and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
OCT	Serial, parallel, dynamic, and differential OCT simplifies design and reduces component count. Dynamic OCT enables support for next-generation memory interface designs that must dynamically switch between serial and parallel termination. Digital calibration circuitry provides industry-leading OCT tolerance within 10 percent.
Clock management features	Up to 12 PLLs with up to 10 unique customizable outputs per PLL ranging from 5 to 720 MHz. There are also up to 16 global, 88 quadrant, and 208 periphery clocks. Advanced clock management features include PLL reconfiguration, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	Hardwired logic is very secure—no bitstream, no external programming device.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Increased SEU immunity	The connections between HCells are hardwired after via programming. The high SEU tolerance nature of HardCopy IV ASICs is due not only to the hardwiring, but also to improved architecture of sequential elements.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications.

HardCopy IV transceiver protocol support (GX only)

Protocol	Data rate
ASI	0.27
Basic (proprietary)	0.6 - 6.5
CEI-6G (SR,LR)	4.976-6.375
CPRI	0.6144, 1.2288, 2.4576, 3.072
10G Ethernet (XAUI)	3.125
Gigabit Ethernet	1.25
Fibre Channel	1.0625, 2.125, 4.25
GPON	1.244 uplink, 2.488 downlink
HiGig+	3.75
HyperTransport™ 3.0	0.4, 2.4, 2.8, 3.2
Interlaken	3.125-6.375
OBSAI	0.768, 1.536, 3.072
PCI Express Gen1, Gen2	2.5, 5
PCI Express Cable	2.5
RXAUI	6.25
SAS	1.5, 3, 6
SATA	1.5, 3, 6
3G-SDI	2.97
SDI SD/HD	0.27/1.485
SerialLite II	0.6-6.375
Serial RapidIO®	1.25, 2.5, 3.125
SFI-5.1	2.488-3.125
SONET OC-3/OC-12/OC-48/OC-192	0.155/0.622/2.488/NA

HardCopy III

HardCopy ASICs deliver high levels of integration

HardCopy III ASICs deliver low risk, low total cost, and rapid time to market and profit for your custom logic needs. The HardCopy methodology allows you to prototype your system with Stratix III FPGAs and completely prepare your system for production. Altera's HardCopy Design Center uses a fast and predictable turnkey process to implement the low-cost, low-power, functionally equivalent, pin-compatible HardCopy III device. Our methodology is the low-risk solution for rapid system development and production.

HardCopy III family features summary

Seamless prototyping	HardCopy III ASIC seamless prototyping on Stratix III FPGAs. Single toolset across HardCopy III and Stratix III devices for enhanced productivity. All of the HardCopy III and Stratix III devices supported in Quartus II software.
External memory interface circuitry	HardCopy III ASICs support external DRAM and SRAM memory interfaces, including DDR3, DDR2, QDR II, QDR, RLDRAM II, and RLDRAM. The dynamic self-calibrating PHY continuously compensates for PVT variations during operation. You can achieve higher performance, up to 800 Mbps (400 MHz), better signal integrity, increased robustness, expanded design margin, and lower power in your designs. Complete solutions including easy-to-use IP, hardware development platforms, and comprehensive timing analysis are available to minimize risk and speed time to market.
TriMatrix memory	TriMatrix memory offers three memory block sizes to suit complex design needs: 640-bit MLABs, 9-Kbit M9K blocks, and 144-Kbit M144K blocks. With up to 16.3 Mbits of memory performing at over 600 MHz and features such as dual-port RAM and integrated ECC, TriMatrix memory is more flexible and efficient, and provides higher memory bandwidth than any other memory architecture. All three configurations support parity checking.
DSP blocks	HardCopy III ASICs support up to 896 multipliers. All used DSP block circuitry is implemented in HCell logic. DSP blocks include all associated pipelining, adders, and accumulators. They are configurable to support 9-bit x 9-bit, 12-bit x 12-bit, 18-bit x 18-bit, or 36-bit x 36-bit multipliers at up to 455 MHz and 407 GMACS, making HardCopy III ASICs ideal for custom-built DSP replacement, as well as coprocessing for hardware acceleration.
High-speed single-ended I/O support	Up to 20 modular I/O banks with programmable slew rate, programmable drive strength, programmable output delay, OCT, and dynamic trace compensation. Maximizes I/O flexibility and performance for over 40 industry standards to optimally match your system requirements. I/O configuration will be fixed after Design Review 2.
High-speed differential I/O support	Optimized LVDS I/O pins at 150-MHz and 1.25-GHz performance provide high performance and excellent signal integrity with half the capacitance of competitive devices. HardCopy III LVDS supports hard DPA and SERDES blocks with clock forwarding for CDR in high-speed chip-to-chip applications. MegaWizard plug ins make differential I/O configuration straightforward and easy.
DPA	As a feature of the LVDS high-speed differential I/O support, DPA minimizes bit errors and simplifies PCB layout and timing management for high-speed data transfer. DPA eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.
OCT	Serial, parallel, dynamic, and differential OCT simplifies design and reduces component count. Dynamic OCT enables support for next-generation memory interface designs that must dynamically switch between serial and parallel termination. Digital calibration circuitry provides industry-leading OCT tolerance within 10 percent.
Clock management features	Up to 12 PLLs with up to 10 unique customizable outputs per PLL ranging from 5 to 720 MHz. There are also up to 16 global, 88 quadrant, and 208 periphery clocks. Advanced clock management features include PLL reconfiguration, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth for all on- and off-chip clocking requirements.
Design security	Hardwired logic is very secure—no bitstream and no external programming device.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence.
Increased SEU immunity	The connections between HCells are hardwired after via programming. The high SEU tolerance nature of the HardCopy III ASICs is due not only to the hardwiring, but also to improved architecture of sequential elements. HCells are the logic building blocks for HardCopy ASICs.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications.

HardCopy II

90-nm HardCopy ASICs with guaranteed success

The 1.2V, 90-nm HardCopy II family offers up to 3.6M ASIC gates, 8.8 Mbits of memory, and over 350-MHz system performance. Compared to FPGAs, HardCopy II ASICs offer over 50 percent power reduction and up to 100 percent higher core performance. For data on increased SEU immunity, contact your Altera® representative. Using Stratix II FPGAs for seamless prototyping, plus our fast and predictable back-end process, provides fast time to market with reduced risk for your HardCopy ASIC-based systems.

HardCopy II family features summary

Clock management	Up to 12 programmable PLLs, providing robust clock management and frequency synthesis capabilities for maximum system performance. The PLLs provide high-end features, including clock switchover, PLL reconfiguration, spread-spectrum clocking, frequency synthesis, programmable phase shift, programmable delay shift, external feedback, and programmable bandwidth.
Differential I/O support	Support for high-speed differential I/Os for data rates up to 1 Gbps to address the high-performance needs of emerging I/O interfaces, including support for the LVDS, LVPECL, and HyperTransport™ standards.
External memory interfaces	Advanced external memory interface support allows you to integrate external high-density SRAM and DRAM devices into complex system designs without degrading data-access performance.
OCT	Series and differential OCT support can simplify board layout by minimizing the number of external resistors needed.
Single-ended I/O standards	High-bandwidth, single-ended I/O interface standards (SSTL, HSTL, PCI, and PCI Express) supported.
Source-synchronous protocols	Support for a wide array of high-speed interface standards, including SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, and SRIO.
TriMatrix memory	Up to 8.8 Mbits of RAM—configurable M4K and M-RAM embedded RAM blocks for a wide range of features.
Nios II embedded processor support	Nios II embedded processors offer an ideal replacement for low-cost discrete microprocessors, serve as a system's primary processor, and support multi-core applications. Nios II soft processor support for HardCopy II FPGAs offers up to 230-DMIPS performance.

HardCopy ASIC series package and I/O matrix

HardCopy IV ASICs (0.9V) with 6.5+ Gbps transceivers option[1]

951 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

		HC4GX1YZ[5]	HC4GX2YZ	HC4GX3YZ	HC4GX4YZ	HC4GX5YZ	HC4GX6YZ	HC4E2YZ	HC4E3YZ	HC4E4YZ	HC4E5YZ	HC4E6YZ	HC4E7YZ
FBGA (F)	484 pin (WF[2])							296	296				
	484 pin (FF[3])							296	296				
	780 pin (WF)							392	392	392			
	780 pin (FF)	368	368	368	256/288	256/288		488	488	488			
	1,152 pin (LF[4])		560	560	560	560				744	744	744	744
	1,152 pin (FF)		560	560	560	560	560			744	744	744	744
	1,157 pin (LF)			736	736	736	736			880	880	880	880
	1,517 pin (FF)			736	736	736	736			880	880	880	880

[1] All data is preliminary
[2] WF = wire bond
[3] FF = Performance-optimized flip chip
[4] LF = Cost-optimized flip chip
[5] Y = I/O count, Z = package type

HardCopy III ASICs (0.9V)[1]

951 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

		HC31YZ[5]	HC32YZ	HC33YZ	HC35YZ	HC36YZ	HC37YZ
FBGA (F)	484 pin (WF[2])	296	296	296	296	296	296
	484 pin (FF[3])	296	296	296	296	296	296
	780 pin (WF)	392	392	392	392	392	392
	780 pin (FF)	488	488	488	488	488	488
	1,152 pin (LF[4])		744	744	744	744	744
	1,152 pin (FF)		744	744	744	744	744
	1,517 pin (LF)				880	880	880
	1,517 pin (FF)				880	880	880

[1] All data is preliminary
[2] WF = wire bond
[3] FF = Performance-optimized flip chip
[4] LF = Cost-optimized flip chip
[5] Y = I/O count, Z = package type

HardCopy II ASICs (1.2V)

951 Number indicates available user I/O pins.

All HardCopy series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

		HC210W	HC210	HC220W	HC220	HC230	HC240
FBGA (F)	484 pin (WF[1])	308					
	484 pin (FF[2])		334				
	672 pin (WF[1])			440			
	672 pin (FF[2])				492		
	780 pin (WF[1])			445			
	780 pin				494		
	1,020 pin					698	742
	1,508 pin						951

[1] WF = wire bond
[2] FF = Performance-optimized flip chip

HardCopy ASIC series features

		HardCopy IV ASICs (0.9V) with 6.5+ Gbps transceivers option[1]											
		HC4GX1YZ	HC4GX2YZ	HC4GX3YZ	HC4GX4YZ	HC4GX5YZ	HC4GX6YZ	HC4E2YZ	HC4E3YZ	HC4E4YZ	HC4E5YZ	HC4E6YZ	HC4E7YZ
Density and speed	Usable ASIC gates	2.8M	3.8M–6.7M	6.7M–9.2M	7.7M	9.4M	11.5M	3.8M	9.2M	7.7M	9.4M	11.5M	13.3M
	Embedded memory (Mbits)	6.3	8.1–11.0	8.9–13.9	9.2–13.3	9.2–17.7	13.3–20.3	8.1	10.7	12.1–13.3	17.7	18.0	18.4
	Maximum 18-bit x 18-bit multipliers	384	512	1,288	832	1,040	1,024	512	1,288	832	1,040	1,024	1,024
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others											
	PLLs	3	3/4/6	3/6/8	2/4/6/8	2/4/6/8	6/8	4	4	4/8/12	8/12	8/12	8/12
	Design security[2]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Stratix series prototyping support	EP4SGX 70	EP4SGX 110 EP4SGX 180	EP4SGX 180 EP4SGX 230	EP4SGX 290	EP4SGX 360	EP4SGX 530	EP4SE 110	EP4SE 230	EP4SE 290	EP4SE 360	EP4SE 530	EP4SE 680
I/O features	I/O voltage levels supported	1.2, 1.5, 1.8, 2.5, 3.0											
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)											
	True-LVDS maximum data rate (Mbps)	150–1,250+											
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength[3]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Transceiver (SERDES) data rate range	600 Mbps–6.5+Gbps with PCS + PMA[4]											
	6.5+ Gbps transceiver (SERDES) channels	8	8/16	8/16/24	8/16/24	8/16/24	16/24	–	–	–	–	–	–
	6.5+ Gbps transceiver (SERDES) channels (PMA Only)	0	0/8	0/8/12	0/8/12	0/8/12	0/8/12	–	–	–	–	–	–
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR											

[1] All data is preliminary

[2] Since all HardCopy ASICs contain hardwired logic, they are inherently secure.

[3] Settings are fixed post Design Review 2.

[4] Subject to increase, pending characterization.

HardCopy ASIC series features

		HardCopy III ASICs (0.9V)[1]					
		HC31YZ	HC32YZ	HC33YZ	HC35YZ	HC36YZ	HC37YZ
Density and speed	Usable ASIC gates	2.7M	3.6M	5.8M	5.3M	6.9M	7.0M
	Embedded memory (Mbits)	4.1	5.4	5.4–7.9	5.4–9.2	5.4–14.3	12.1–15.9
	Maximum 18-bit x 18-bit multipliers	288	384	896	576	768	576
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others					
	DSP blocks	Implemented in HCell macros					
	True dual-port RAM	✓	✓	✓	✓	✓	✓
	PLLs	4	4/8	4/8	4/8/12	4/8/12	4/8/12
	Design security[2]	✓	✓	✓	✓	✓	✓
	Stratix series prototyping support	EP3SL110	EP3SL150	EP3SE110	EP3SL200	EP3SE260	EP3SL340
I/O features	I/O voltage levels supported	1.2, 1.5, 1.8, 2.5, 3.0					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II)					
	True-LVDS maximum data rate (Mbps)	150–1,250+					
	Embedded DPA circuitry	✓	✓	✓	✓	✓	✓
	Series and differential OCT	✓	✓	✓	✓	✓	✓
	Programmable drive strength[3]	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM II, SDR					

[1] All data is preliminary.
[2] Since all HardCopy ASICs contain hardwired logic, they are inherently secure.
[3] Settings are fixed post Design Review 2.

HardCopy ASIC series features

		HardCopy II ASICs (1.2V)					
		HC210W	HC210	HC220W	HC220	HC230	HC240
Density and speed	Usable ASIC gates	1.0M	1.0M	1.9M	1.9M	2.9M	3.6M
	Additional gates for DSP blocks	0	0	300,000	300,000	700,000	1,400,000
	LEs	–	–	–	–	–	–
	Total RAM bits	875,520	875,520	3,059,712	3,059,712	6,368,256	8,847,360
	M512 RAM blocks (512 bits + 64 parity bits)	–	–	–	–	–	–
	M4K RAM blocks (4 Kbits[1] + 512 parity bits)	190	190	408	408	614	768
	M-RAM blocks (512 Kbits[1] + 65,536 parity bits)	0	0	2	2	6	9
	Speed grades (fastest to slowest)	–	–	–	–	–	–
Architectural features	Embedded processor	Nios II processor, as well as partner processors from ARM, Freescale, and others					
	DSP blocks	Implemented in HCell macros					
	18-bit x 18-bit/9-bit x 9-bit embedded multipliers	Implemented in HCell macros					
	I/O registers per I/O element	6	6	6	6	6	6
	True dual-port RAM	✓	✓	✓	✓	✓	✓
	Global and regional clock networks	16/32	16/32	16/32	16/32	16/32	16/32
	PLLs	4	4	4	4	8	12
I/O features	I/O voltage levels supported (V)	1.5, 1.8, 2.5, 3.3					
	I/O standards supported	LVDS, LVPECL, HyperTransport, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS					
	External memory device interfaces	QDR II, DDR2, RLDRAM II, DDR, SDR					
	True-LVDS maximum data rate (Mbps)	125–1,000					
	True-LVDS channels (receive/transmit)	13/17	19/21	29/31	29/31	42/42	118/118
	Medium-speed LVDS data rate (Mbps) (receive/transmit)	–	–	–	–	–	–
	Series and differential OCT	✓	✓	✓	✓	✓	✓
	FPGA prototype options	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90	EP2S30 EP2S60 EP2S90 EP2S130	EP2S60 EP2S90 EP2S130	EP2S90 EP2S130 EP2S180	EP2S180

[1] Kbits = 1,024 bits

FOR MORE INFORMATION

HardCopy ASIC series	www.altera.com/hardcopy
HardCopy IV ASICs	www.altera.com/hardcopy4
HardCopy III ASICs	www.altera.com/hardcopy3
HardCopy II ASICs	www.altera.com/hardcopy2
Training	www.altera.com/training

Embedded processing

How do you create the exact system you need? Altera combines the versatility of programmable logic with high-performance embedded processors for a flexible solution that scales to fit individual application needs, lowers system cost, and reduces the risk of obsolescence. You can use a processor in an FPGA as your main system controller or for offloading tasks from an external processor. Either way, you get the exact set of peripherals, memory, and I/O interfaces that fit your needs—together with FPGA flexibility, fast time to market, and system integration—all at the performance and cost points you're looking for.

Altera offers the broadest selection of soft processor cores in the industry:

- Nios® II processor (Altera)—Create an exact mix of peripherals, memory interfaces, and hardware accelerators for your application with the versatile Nios II processor, the FPGA industry's #1 soft processor.
- Cortex-M1 processor (ARM)—The ARM® Cortex-M1 processor enables OEMs to leverage their expertise with ARM architectures for FPGA- and HardCopy® ASIC-based systems.
- V1 ColdFire processor (Freescale)—The small-footprint V1 ColdFire core is designed for entry-level 32-bit applications. It enhances system utilization, resulting in low power consumption while giving more than 10 times the performance of an 8-bit MCU.
- A variety of processor cores from additional Altera partners.

These processor cores work seamlessly with Altera's SOPC Builder system design tool to give you a head start on your design.

Embedded processors

Product name	Vendor name
32-/16-bit	
Nios II embedded processor[2]	Altera Corporation
ARM Cortex-M1[2]	Arrow Electronics/ARM
V1 ColdFire[2]	Freescale
8-/4-bit	
8051X-C Microcontroller	CAST, Inc.
8051XC-B Microcontroller	CAST, Inc.
8051XC-A Microcontroller	CAST, Inc.
DR8051 8-bit RISC Microcontroller	Digital Core Design
DR8052EX 8-bit RISC Extended Microcontroller	Digital Core Design
C68000 Microprocessor	CAST, Inc.
CZ80CPU Processor	CAST, Inc.
DF6811CPU 8-bit Microcontroller CPU	Digital Core Design
DFPIC1655X RISC Microcontroller	Digital Core Design

[1] SOPC Builder component (no license required)
[2] SOPC Builder-ready licensed core

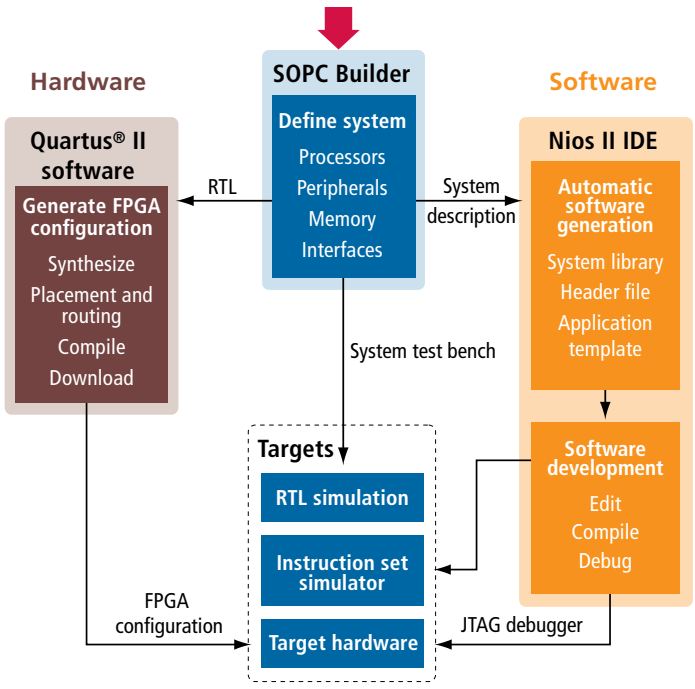
Nios II embedded processors

Nios® II

When you're poised to capture an early-to-market advantage with your novel idea, turn to Altera's Nios II embedded processor to give you a jump on the competition. By allowing you to drag and drop the precise mix of processors and peripherals needed to build your system, the versatile 32-bit Nios II processor equips you to create an exact-fit processor system in just minutes.

Compared with traditional embedded processors, the Nios II processor offers much more flexibility. It provides a customizable feature set, along with costs and performance that you can tailor to your unique system requirements. Used by each of the world's top 20 OEMs and with more than 20,000 development kits sold worldwide, the proven Nios II processor is the industry's most widely used soft processor as confirmed by the market research firm Gartner.

Nios II processor development flow



Versatility

We designed Nios II processors to meet the unique demands of new design cycles, enabling you to:

- Choose the exact set of processors, peripherals, memory, and interfaces needed for your application
- Increase system performance without changing your board design or increasing clock frequency
- Eliminate the risk of processor and ASSP obsolescence
- Lower overall system cost, complexity, and power consumption with multiple functions combined on a single chip
- Remotely upgrade your designs in the field to improve competitiveness and address changing requirements
- Target any Stratix® or Cyclone® series FPGA or HardCopy series ASIC
- Migrate designs to standard cell ASICs through the Synopsys DesignWare Star IP Program

Broad software support

The Nios II processor is backed by the Eclipse-based Nios II Integrated Development Environment (IDE) and a full range of software and operating system support provided by Altera and our partners. To boost performance, just right-click to accelerate your ANSI-C code using the Nios II C-to-Hardware Acceleration (C2H) Compiler.

Nios II C2H Compiler

An easy-to-use productivity tool, the Nios II C2H Compiler lets you boost the performance of time-critical ANSI-C functions by converting them into hardware accelerators in the FPGA. With the Nios II C2H Compiler, you can:

- **Accelerate performance of your Nios II embedded software—without increasing your clock frequency**
- **Design using the standard ANSI-C programming language and the familiar Eclipse-based Nios II IDE**
- **Boost software performance from 10X to 70X**

Traditionally, offloading software to hardware accelerators has been a manual task, benefiting only those developers with the tools, experience, and time required to create, test, and integrate RTL blocks into their processor systems. The Nios II C2H Compiler automates the creation and integration of hardware accelerators, reducing development time from weeks to minutes.

Software and operating system support

	Product name	Vendor name	Description
Operating system	MicroC/OS-II	Micrium	Real-time kernel; included in Nios II development kits
	eCos	eCosCentric	Open-source real-time operating system
	Nucleus PLUS	Mentor Graphics	Royalty-free, real-time operating system
	ThreadX	Express Logic	High-performance, real-time kernel
	µClinux	SLS	Complete µClinux distribution for the Nios II processor
	Euros	Euros RTOS	Real-time operating system
	embOS	Segger	Royalty-free real-time operating system
	OSEK/VDX-OS	Vector	Preemptive multitasking operating system
	Evidence	Erika Enterprise	Real-time operating system with microprocessor support
Debuggers/ IDEs	Nios II IDE	Altera Corporation	Full-featured IDE included in the Nios II Embedded Design Suite (EDS)
	EDGE IDE	Mentor Graphics	Eclipse-based IDE and debugger
	TRACE32-PowerView	Lauterbach	Flexible, fast debug environment
	Universe	Adveda	Hardware/software co-verification tools
	System Navigator	First Silicon Solutions	Software debug probe
	TRACE32-PowerView	Lauterbach	Software debug probe environment
Compilers	Tasking VX-Toolset	Altium	Optimizing C compiler
	GCC Compiler	GNU	Standard GNU compiler for Nios II processor

Nios II performance features and summary

High-performance processor core	Optimize performance-critical applications with the Nios II/f "fast" core, which has 6-stage pipeline, dynamic branch prediction, instruction and data cache, and over 300-DMIPS[1] performance.
Multi-processor systems	Use multi-core systems to scale a system's performance or to break up software applications into simpler tasks. The Nios II EDS includes support for creating customized multi-core systems using Nios II processors.
High-bandwidth bus structure	Automatically generate a system interconnect fabric to support any system that you build by using the SOPC Builder system generation tool, allowing you to generate high-throughput systems supporting simultaneous multiple master/slave connections, direct memory access (DMA) channels, and on-chip data buffers.
Hardware accelerators	Use logic and memory resources in the FPGA to offload and accelerate tasks that are typically implemented in application software. You can automate this process with the Nios II C2H Compiler.
Custom instructions	Accelerate time-critical software algorithms by adding custom instructions to the Nios II processor instruction set.
Fast configurable on-chip memory	Create fixed low-latency on-chip memory buffers for performance-critical applications.

[1] Performance varies by product family

Performance

With performance clocked at well over 300 DMIPS, the Nios II processor is the industry's fastest FPGA-based configurable processor. You'll uncover the true processing performance potential of your FPGAs when you offload their processing tasks from software into dedicated hardware accelerators. Unlike off-the-shelf processors, FPGAs have parallel processing capabilities that let you create very high-performance, high-throughput systems.

Designing with Nios II processors

Nios II processors come with a comprehensive tool suite that raises productivity by helping you and your team efficiently build and manage customized embedded processor systems. What's more, our software design suite was developed to accommodate the unique requirements of systems on programmable chips.

Nios II EDS

The Nios II EDS is a collection of all the tools, utilities, libraries, and drivers needed to develop embedded software for the Nios II processor. Among many other tools and utilities, the Nios II EDS includes the Nios II IDE, the primary software development environment for the Nios II processor. Within this Eclipse-based GUI, you can edit, compile, download, debug, and program flash devices.

Embedded partners

Working with Altera, you'll have the backing of more than a dozen embedded partners, offering a broad range of third-party operating systems, middleware, and embedded software development tools.

Nios II EDS contents

- Code development tool: Nios II IDE
  - New project wizards
  - Software templates
  - Source navigator and editor
  - Compiler for C and C++ (GNU)
  - Based on the Eclipse community project
- Source debugger
- Flash programmer
  - Hardware Abstraction Layer (HAL)
  - MicroC/OS-II real-time operating system[1]
  - NicheStack TCP/IP Network Stack—Nios II Edition[1]
  - Newlib ANSI-C standard library
  - Simple file system
- Other Altera® command line tools and utilities
- Design examples
- C acceleration tool: Nios II C2H Compiler[1]

[1] Production license sold separately

Hardware development tools

- Quartus II design software
- SOPC Builder, an exclusive Quartus II software tool that lets you build and evaluate systems at the block level easily and quickly
- SignalTap® II embedded logic analyzer plug-in for the Nios II processor
- FPGAView software from First Silicon Solutions for configuring and debugging Altera FPGA devices with Tektronix logic analyzers

Nios II processor family members

Feature	Nios II/f (fast) processor	Nios II/s (standard) processor	Nios II/e (economy) processor
Description	Optimized for maximum performance	Balanced cost and performance	Optimized for minimum logic usage
Pipeline	6 stage	5 stage	1 stage
Multiplier	1 cycle[1]	3 cycle	Emulated in software
Branch prediction	Dynamic	Static	None
Instruction cache	Configurable	Configurable	None
Data cache	Configurable	None	None
Custom instructions	Up to 256	Up to 256	Up to 256

[1] Using DSP blocks in Stratix or Stratix II FPGAs

Processor cores

The Nios II processor family consists of three CPU cores, each optimized for a specific price and performance range. All three CPU cores share a common 32-bit instruction set architecture, are binary code compatible, and are supported by the same software design suite. Simply choose which CPU is appropriate for each of your designs. You can also create multi-core systems with any Nios II CPU to scale a system's performance or to break up software applications into simpler tasks.

Embedded IP

SOPC Builder includes a portfolio of standard embedded peripherals that you can use to jump-start your system design. These SOPC Builder components include HAL drivers that will let you immediately begin your software development.

Altera embedded peripherals

• JTAG UART	• Tri-state bridge
• UART	• Serial flash controller (EPCS)
• DMA	• Ethernet
• Timer	• PLL core
• PIO	• Mailbox and mutex
• SPI	• LCD controller
• SDRAM controller	• System ID peripheral
• DDR SDRAM controller	• Performance counter
• Common flash interface controller	• SG-DMA

Ready to go?

Make a Nios II development kit your starting point—the kits include everything you'll need to begin designing embedded systems for FPGAs:

- Processor and peripheral IP (with perpetual use license)
- Complete software development tool suite
- FPGA development board

When you're ready to ship your product, you'll need the Nios II core license that's included with all Nios II development kits. You can also buy the license as a standalone offering. Contact your local Altera representative for details. This royalty-free license never expires and allows you to target your processor design to any Altera FPGA, so your software application is preserved even if the underlying hardware changes.

Start working with the Nios II processor today using free Altera development tools. Hardware engineers should download Quartus II Web Edition design software to create Nios II processor-based hardware systems. Software designers should download the Nios II EDS to begin programming Nios II applications right away.

FOR MORE INFORMATION

Altera embedded processing	www.altera.com/embedded
Nios II processors	www.altera.com/nios2
Nios II development kits	www.altera.com/nioskits
Nios II C2H Compiler	www.altera.com/c2h
Nios user forum	www.niosforum.org
SOPC Builder-ready IP	www.altera.com/sopcready

Digital signal processing

If your stand-alone DSP processor is running out of computational horsepower, FPGAs can solve the problem. FPGAs speed up your system with massive DSP horsepower that efficiently implements DSP algorithms in applications such as motion estimation, complex video processing, OFDM-MIMO processing in basestations, and single data rate (SDR) algorithms.

For example, motion estimation, which underlies the coding efficiency for H .264 algorithms, relies on billions of sum of absolute difference calculations per frame to make encoding decisions. Each individual operation is straightforward, but all of the operations together require huge amounts of computing power.

If you want the performance of a DSP farm, Altera's new Stratix® IV architecture offers over 700-GMAC/s DSP performance. By doing the job of tens or even hundreds of DSP processors, a signal processing system built using the Stratix IV FPGA instead of DSP processors also has significantly lower bill of material (BOM) cost and power consumption.

Altera provides the industry's most comprehensive portfolio of solutions for implementing your high-performance DSP design in our FPGAs:

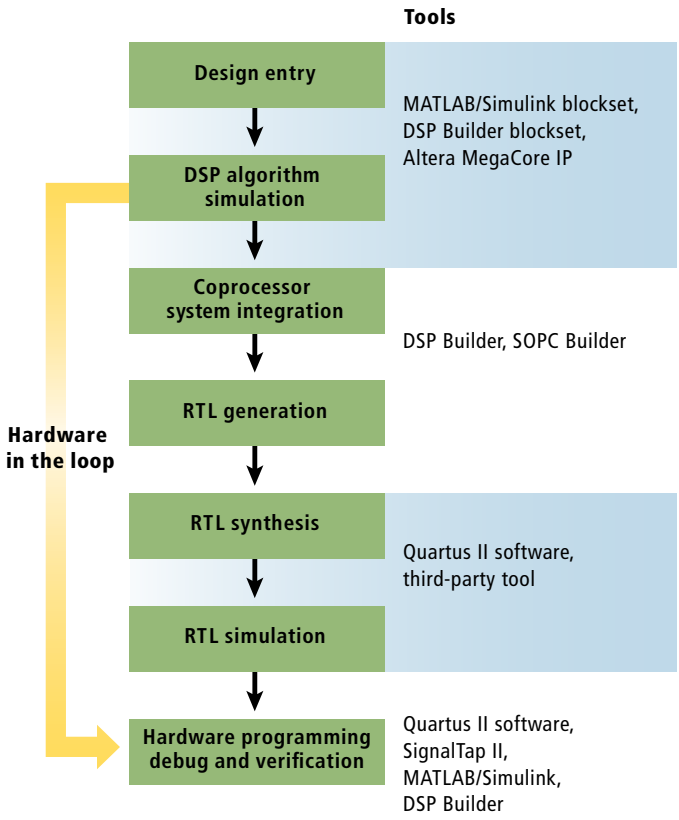
- DSP Builder—A MATLAB/Simulink-based design tool that enables system-level design
- Comprehensive collection of intellectual property (IP) functions for signal processing, including the largest suite of IP for video processing and floating-point operations
- Large portfolio of DSP reference designs for wireless, high-definition video, and other signal processing applications
- Range of DSP development kits to speed up design

DSP Builder: FPGA industry's premier DSP design tool

Designing DSP applications in FPGAs requires both high-level algorithm development and HDL development tools. Altera's DSP Builder integrates these tools by combining the algorithm development, simulation, and verification capabilities of MATLAB/Simulink system-level design tools with VHDL synthesis, simulation, and the hardware debugging capabilities of the Quartus® II development tool.

DSP Builder creates a seamless bridge between the MATLAB/Simulink tool and Altera® Quartus II software, and automatically generates timing-optimized HDL from a high-level Simulink description of the system. This capability is critical for designing multi-channel signal processing datapaths in applications such as RF processing in wireless applications and SDR in military applications. With DSP Builder, you can achieve high-performance design implementations running at near-peak FPGA performance in a matter of minutes compared to the hours, if not days, required to hand-optimize HDL code.

DSP design flow overview



DSP Builder features summary

HDL optimized for DSP applications	Optimizes HDL to meet the system f_{MAX} and latency specified in the Simulink environment. Also optimizes the synthesis of multi-channel signal processing datapaths.
Effortless device retargeting	Allows designers to easily retarget their designs to other device families from within Simulink, e.g., from Stratix series FPGAs (including the new 40-nm Stratix IV family) to Cyclone® series FPGAs.
Testbench generation	Automatically generates a VHDL testbench or Quartus II Vector File (.vec) from MATLAB and Simulink test vectors.
Hardware in the loop	Accelerates system-level co-simulation with Simulink.
Suite of reference designs	Comes with an updated suite of reference designs for digital up/down conversion and multi-channel filters.

IP functions for signal processing

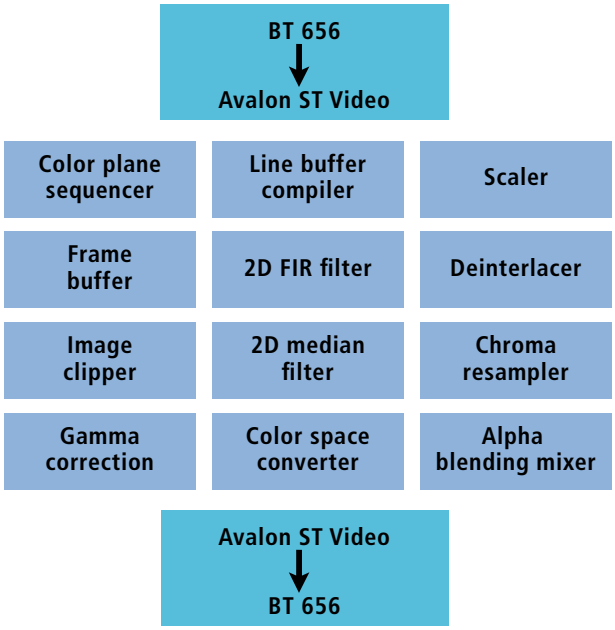
Altera provides an extensive portfolio of intellectual property (IP) MegaCore® functions to design and build DSP datapaths with our FPGAs. These functions, which can easily be integrated into your design using Altera's DSP Builder and SOPC Builder design tools, range from simple arithmetic functions to complex multirate filters, FFTs, and video processing functions. Altera also provides the video image processing IP suite, which consists of commonly used video processing functions ranging from simple color space converters to complex polyphase scalers and motion adaptive deinterlacers.

Applications such as radar, sonar, bio and molecular science, financial modeling, advanced wireless antenna processing, medical imaging, image analytics and synthesis, and precision control are creating a demand for floating-point capabilities in FPGAs. Altera provides the largest library of IEEE 754-compliant floating-point megafunctions, and they can all be used in any Altera device family. Key megafunctions include:

- Logarithm [altfp_log]
- Exponential [altfp_exp]
- Inverse [altfp_inv]
- Inverse Square Root [altfp-inv_sqrt]
- Addition/subtraction [altfp_add_sub]
- Multiplication [altfp_mult]
- Division [altfp_div]
- Square root [altfp_sqrt]
- Compare [altfp_compare]

All MegaCore Altera Megafunction Partners Program (AMPP^{SM}) functions have been rigorously tested to meet or exceed the exacting requirements of industry standards.

Video image processing suite



DSP reference designs

Speed up the development of common DSP applications by using one of our DSP reference designs. These reference designs range from video processing to wireless designs to designs for interfacing FPGAs with a DSP processor. For broadcast applications, Altera also provides 1080p reference designs that implement complex video processing of multiple high-definition video channels, and references designs that implement digital up and down conversion using the MATLAB/Simulink tool environment.

DSP development kits

Jump-start your DSP design using Altera DSP development kits. These kits—which include a development board with an Altera FPGA, software, and reference designs—help you prototype and debug your design quickly and efficiently.

DSP Stratix III board with daughtercard

FOR MORE INFORMATION

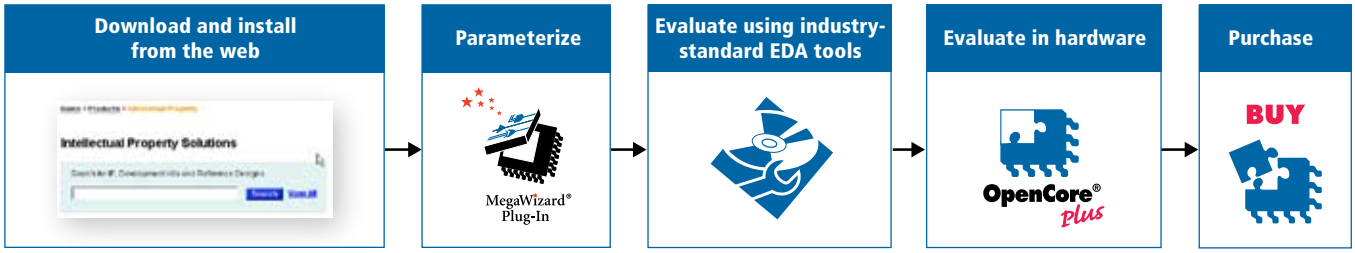
DSP information	www.altera.com/dsp
Development kits	www.altera.com/devkits
Intellectual property	www.altera.com/ipmegastore
Training	www.altera.com/training

Intellectual property solutions

Altera offers a broad portfolio of easy-to-use, flexible IP cores. These IP cores are high-quality "building blocks" that you can drop into your system designs, avoiding the time-consuming task of creating every block in your designs from scratch. Pre-verified and configurable, Altera® IP cores are optimized for the latest Altera devices and are fully supported in Quartus® II design software. Some of the IP cores listed in our catalog are offered by leading third-party IP vendors who have developed, optimized, and qualified their IP products for Altera devices, licensing them directly to our customers.

Discover how quickly you can use these cores to accelerate your system design, lower development costs, increase productivity, and speed your time to market.

Altera IP design flow



Designing with Altera IP

Install	Download and install with Quartus II software.
Parameterize	Use Altera's powerful, user-friendly MegaWizard® Plug-In tool to select the right features for your design requirements, estimate resources, set up third-party tools, and generate all files necessary for integrating parameterized IP into your design.
Simulate logic in real time	Evaluate all the features of the IP before you buy—including functionality, size, and speed in your system—with the OpenCore® simulation evaluation feature.
Evaluate in hardware	Generate time-limited FPGA programming files using the OpenCore Plus hardware evaluation feature. Then use the files to verify your complete FPGA design on your own hardware, or any other available board—all before you decide to purchase an IP license.
License	When you are completely satisfied with the IP core and are ready to take your design into production, purchase the license and generate the production device programming files. Altera MegaCore® licenses are for perpetual use, support multiple projects, and include upgrades and support for one year. Floating and node-locked licenses are available for all Altera IP. Third-party IP cores are offered under a variety of different licensing terms, conditions, and pricing models. Contact the IP partners directly for details.

Altera IP search engine

Our online IP search engine includes a portfolio of DSP and embedded system cores, interface protocols, and memory controllers as well as a broad range of development kits and application-specific reference designs. Use the search engine to find the right combination of IP and hardware solutions for your next Altera FPGA or ASIC design.

Altera megafunction library elements

Altera's IP portfolio is not limited to licensed cores. We also provide two types of IP that do not require license fees or license keys: basic megafunction library elements and SOPC Builder components. Altera offers an entire library of basic library elements, called megafunctions, that support more efficient logic synthesis and device implementation. These megafunctions are optimized for all Altera device architectures, and can be parameterized to scale in size and function. You can implement these megafunctions in Altera-based designs without license fees or keys by using the MegaWizard® plug-in tool, available in Quartus II design software. Key megafunction library elements are described below. Consult the MegaWizard plug in for the most complete listing.

SOPC Builder components

SOPC Builder components are hardware design blocks integrated in Quartus II software's SOPC Builder tool. These components consist of a variety of peripherals that are ideal for instantiation in on- and off-chip processor designs and for IP integration.

Search engine overview

DSP	IP cores and reference designs used for digital modulation, video and image processing, and wireless DSP applications. Multiple hardware development kits with optional daughtercards from Altera and partners enable faster system integration and verification.
Embedded	Versatile embedded processors with a wide range of peripherals, development kits, and software tools.
Interface protocols	Today's most common system interfaces with development kits for telecom, datacom, and storage applications.
Memory controllers	Extensive portfolio of standard and high-performance memory controllers for use with the suite of FPGA development kits.

SOPC Builder-ready certification

Altera awards the SOPC Builder-ready certification to licensed IP cores that are ready to integrate with the Nios® II embedded processor or a third-party processor or to implement the system interconnect fabric via SOPC Builder. These cores support the Avalon® Memory-Mapped interface or the Avalon Streaming interface and include applicable software drivers, low-level routines, or other software design files.

Altera megafunction library elements	Description
alt2gxb	Designed for use with Altera Stratix® GX and Arria® GX family devices. Enables set-up of one or more transceivers at multiple data rates.
altmemphy	Physical interface which comprises silicon features as well as soft logic. It is responsible for the safe transfer of data between the FPGA and the memory, including all aspects of crossing between different clock domains.
altdll / altdq_dqs	Designed for use with Stratix III and Stratix IV FPGAs. Used to support memory standards that are not supported by the altmemphy function.
Encoder and decoder error correction codes [altecc_encoder, altecc_decoder]	Detects errors in digital data transmission through the process of encoding and decoding.
Complex multiplier [altmult_complex]	Simplifies the process of multiplying complex numbers.
Shift register (RAM-based) [altshift_taps]	Implements RAM-based shift register in the device memory blocks.
Clock control block [altclkctrl]	Implements a basic clock control block.
Memory-based multiplier [altmemmult]	Implements a basic multiplier.
Remote update circuitry [altremote_update]	Enables your designs to take advantage of dedicated remote system upgrade circuitry available in Stratix series devices.
SERDES transmitter/receiver [altlvds]	Implement either an LVDS deserializer receiver or an LVDS serializer transmitter.
PLL [altpll]	Configures the PLLs in the Stratix and Cyclone® series devices.
PLL reconfiguration [altpll_reconfig]	Reconfigures the PLLs in Stratix and Cyclone series devices.
Square root [altsqrt]	Implements the basic square root.
Active serial memory interface [altasmi_parallel]	Implements a basic active serial memory interface (ASMI) block without the need to know the serial interface.
Double data rate (DDR) I/Os [altddio_out, altddio_in, and altddio_bidir]	Implements DDR interface inputs and outputs.

IP megafunctions

DSP

Product name	Vendor name
Error detection/correction	
Reed-Solomon Compiler, Decoder	Altera Corporation
Reed-Solomon Compiler, Encoder	Altera Corporation
Viterbi Compiler, High-Speed Parallel Decoder	Altera Corporation
Viterbi Compiler, Low-Speed/Hybrid Serial Decoder	Altera Corporation
Multi-Rate FEC for G.709 (OTN)	Avalon Microelectronics
G.751.1 Annex 4-compliant EFEC for OTN	Avalon Microelectronics
DVB-RCS CTC Turbo Decoder	TurboConcept
WiMAX CTC Decoder	TurboConcept
3GPP/LTE CTC Decoder	TurboConcept
Turbo Product Code Decoder	TurboConcept
Filters and transforms	
FFT/inverse FFT (IFFT)	Altera Corporation
CIC Compiler	Altera Corporation
FIR Compiler	Altera Corporation
2D DCT IDCT	Barco Silex
Forward Discrete Cosine Transform (DCT)	CAST, Inc.
Modulation/demodulation	
Numerically Controlled Oscillator Compiler	Altera Corporation
DVB-C / J.83 (QAM) Modulator	Commsonic
DVB-C / J.83 Demodulator	Commsonic
DVB/H T/H Modulator	Commsonic
DVB-S2 Modulator	Commsonic
Video and image processing	
Video and Image Processing Suite[2]	Altera Corporation
Color Space Converter	CAST, Inc.
Fast Black and White JPEG Decoder	Barco Silex
Fast Color JPEG Decoder	Barco Silex
JPEG2000 Encoder	Barco Silex
JPEG2000 Decoder	Barco Silex
JPEG CODEC	CAST, Inc.
JPEG Encoders and Decoders	CAST, Inc.
Lossless JPEG Encoder and Decoder	CAST, Inc.
Forward Discrete Wavelet Transform (FDWT)	Barco Silex
Inverse Discrete Wavelet Transform (IDWT)	Barco Silex
H.264 / MPEG-4 AVC SD Single Chip Encoder	ATEME
H.264 / MPEG-4 AVC Full HD Encoder	ATEME
CCIR-656 Encoder and Decoder	Adaptive Micro-Ware, Inc.
Video LVDS SERDES Transmitter/ Receiver	Microtronix

DSP (continued)

Product name	Vendor name
Additional functions	
Floating-Point Addition/Subtraction	Altera Corporation
Floating-Point Multiplication	Altera Corporation
Floating-Point Division	Altera Corporation
Floating-Point Square Root	Altera Corporation
Floating-Point Compare	Altera Corporation
SHA-1	CAST, Inc.
32- and 128-bit AES Encryption/Decryption Cores	CAST, Inc.
DES Cryptoprocessor	CAST, Inc.
High-Speed AES Encryption/ Decryption Cores	D'Crypt Pte. Ltd.
Accelerated Display Graphics Engine	Bitsim
Floating-Point Arithmetic Unit[2]	Digital Core Design
Floating-Point Mathematics Unit[2]	Digital Core Design
Floating-Point Pipelined Divider Unit	Digital Core Design
Floating-Point-to-Integer Pipelined Converter	Digital Core Design
Integer-to-Floating-Point Pipelined Converter	Digital Core Design
D/AVE 2D Vector Graphics	TES Electronic Solutions
D/AVE 2D Graphics Hardware Accelerator	TES Electronic Solutions
VLYNQ Full-Duplex Communications Interface	TES Electronic Solutions

Embedded processors

Product name	Vendor name
32-/16-bit	
Nios II Embedded Processor[2]	Altera Corporation
ARM® Cortex-M1[2]	Arrow Electronics/ARM
V1 ColdFire[2]	Freescale
8-/4-bit	
8051X-C Microcontroller	CAST, Inc.
8051XC-B Microcontroller	CAST, Inc.
8051XC-A Microcontroller	CAST, Inc.
DR8051 8-bit RISC Microcontroller	Digital Core Design
DR8052EX 8-bit RISC Extended Microcontroller	Digital Core Design
C68000 Microprocessor	CAST, Inc.
CZ80CPU Processor	CAST, Inc.
DF6811CPU 8-bit Microcontroller CPU	Digital Core Design
DFPIC1655X RISC Microcontroller	Digital Core Design

[1] SOPC Builder component (no license required)
[2] SOPC Builder-ready licensed core

IP megafunctions

Interfaces and protocols

Product name	Vendor name
Communication	
8B/10B Encoder/Decoder	Altera Corporation
AAL5	Modelware
Inverse Multiplexing for ATM (IMA) version 1.0/1.1	Modelware
ATM Formatter	Adaptive Micro-Ware, Inc.
ATM Deformatter	Adaptive Micro-Ware, Inc.
CRC Compiler	Altera Corporation
Frame-Mapped GFP Controller	Nuvation
GEOS-10: 10:1 Gigabit Ethernet to SONET Multiplexer	Nuvation
GEOS2+2	Nuvation
Multi-Channel HDLC	Modelware
Single-Channel HDLC[2]	Modelware
POS-PHY Level 2 and 3, Link and PHY	Altera Corporation
POS-PHY Level 4	Altera Corporation
SDLC Controller	CAST, Inc.
SONET/SDH Deframer	Aliathon
SONET/SDH Demapper	Aliathon
SONET/SDH Framer	Aliathon
SONET/SDH Mapper	Aliathon
OTN Framer/Deframer	Avalon Microelectronics
SFI 5.1	Avalon Microelectronics
FlexBUS-3 Link Layer	Modelware
SPI-4 Phase 1 (FlexBUS-4)	Modelware
SPI-4.2 Foundation and Manager	Modelware
T1 Framer[2]	Adaptive Micro-Ware, Inc.
T1 Deframer	Adaptive Micro-Ware, Inc.
UTOPIA Level 2 Master	Altera Corporation
UTOPIA Level 2 Slave	Altera Corporation
Bluetooth Baseband	Wipro-NewLogic
802.11MAC and Modem (a, b, g)	Wipro-NewLogic
Ethernet	
10 Gigabit Ethernet	Altera Corporation
Tri-Speed Ethernet (MAC and PCS)[2]	Altera Corporation
MAC-1G Gigabit Ethernet MAC	CAST, Inc.
Gigabit Ethernet MAC[2]	IFI
Advanced Gigabit Ethernet MAC[2]	IFI
10/100/1000 1588 Ethernet MAC	MorethanIP
10/100/1000 Ethernet MAC with SGMII	MorethanIP
10/100/1000 Ethernet MAC-Net[2]	MorethanIP
10/100/1000Mbps Full Duplex Ethernet MAC[2]	MorethanIP
AnySpeed Ethernet MAC[2]	MorethanIP
10/100 Ethernet MAC[2]	MorethanIP
10/100 Ethernet MAC	Microtronix

Interfaces and protocols (continued)

Product name	Vendor name
Ethernet (continued)	
10 Gigabit Ethernet MAC	MorethanIP
10 Gigabit Ethernet PCS	MorethanIP
SPAUI MAC	MorethanIP
10 Gigabit Reduced XAUI PCS	MorethanIP
40/100 Gigabit Ethernet	MorethanIP
40/100 Gigabit Ethernet	Sarance Technologies, Inc.
High Speed	
Serial RapidIO®[2]	Altera Corporation
SerialLite II	Altera Corporation
HyperTransport™ 8-bit	Altera Corporation
HyperTransport 16-bit	GDA Technologies
1394A Firewire	CAST, Inc.
1394b Firewire	Wipro-NewLogic
SATA 1.0	Intelliprop, Inc.
SATA 2.0	Intelliprop, Inc.
Serial Attached SCSI (SAS) 1.0	Intelliprop, Inc.
Serial Attached SCSI (SAS) 2.0	Intelliprop, Inc.
Interlaken	Sarance Technologies, Inc.
HyperTransport 3.0	University of Heidelberg
PCI	
PCI Express Gen1 x1, x4, x8 Controller (Soft IP)[2]	Altera Corporation
PCI Express Gen1 and Gen2 x1, x4, and x8 Lane (hard IP)	Altera Corporation
PCI Express Controller	CAST, Inc.
PCI Express Gen1 x1, x4, x8 Controller	Northwest Logic, Inc.
PCI Express Complete Core x1, x4, x8	Northwest Logic, Inc.
PCI Express, Gen1 and Gen2	PLDA
PCI-X Master/Target Core 32-/64-bit	PLDA
PCI-X Controller	Northwest Logic, Inc.
PCI Compiler, 32-bit Master/Target[2]	Altera Corporation
PCI Compiler, 32-bit Target[2]	Altera Corporation
PCI Compiler, 64-bit Master/Target[2]	Altera Corporation
PCI Compiler, 64-bit Target[2]	Altera Corporation
32-bit PCI Bus Master/Target Interface[2]	Eureka Technology Inc.
32-bit PCI Host Bridge	Eureka Technology Inc.
64-bit PCI Bus Master/Target Interface[2]	Eureka Technology Inc.
64-bit PCI Host Bridge	Eureka Technology Inc.
Integrated PCI Core	Northwest Logic, Inc.
PCI Interface	Northwest Logic, Inc.
PCI Bus Arbiter	Eureka Technology Inc.
PCI-ISA Bridge	Eureka Technology Inc.
PCI-PCI Bridge	Eureka Technology Inc.

[1] SOPC Builder component (no license required)
[2] SOPC Builder-ready licensed core

IP megafunctions

Interfaces and protocols (continued)

Product name	Vendor name
Serial	
I2C Bus Controller[2]	CAST, Inc.
I2C Bus Controller Slave	CAST, Inc.
DI2CM I2C Bus Interface-Master[2]	Digital Core Design
DI2CSB I2C Bus Interface-Slave[2]	Digital Core Design
I2C Master / Slave / PIO Controller	Microtronix Inc.
I2C Master	SLS
I2C Slave	SLS
C_CAN[2]	Bosch
CAN[2]	CAST, Inc.
Nios_CAN[2]	IFI
Nios II Advanced CAN[2]	IFI
ATA-4 Host Controller	Nuvation
ATA-5 Host Controller	Nuvation
MediaLB Device Interface[2]	IFI
PS2 Interface	SLS
USB High-Speed Function Controller[2]	SLS
USB Full/Low-Speed Function Controller[2]	SLS
CUSB USB Function Controller	CAST, Inc.
CUSB2 USB High-Speed Function Controller	CAST, Inc.
USB High Speed OTG Multi-Point	CAST, Inc.
USB High Speed OTG Single Point	CAST, Inc.
USB 1.1 Host/Device	Microtronix
CPRI 3.0	Radiocomp
OBSAI 4.0	Radiocomp
SDIO/SD Memory/Slave Controller	Eureka Technology Inc.
AHB Slave	Eureka Technology Inc.
AHB Master	Eureka Technology Inc.
AHB to SDRAM Controller	Eureka Technology Inc.
Local Interconnect Network (LIN) Controller	CAST, Inc.
SPI Master/Slave	CAST, Inc.
H16450 and H16450S UARTs	CAST, Inc.
H16550 and H16550S UARTs[2]	CAST, Inc.
D16550 UART with 16 Bytes FIFO[2]	Digital Core Design
H16750 and H16750S UARTs	CAST, Inc.
SPI[1]	Altera Corporation
SPI/Avalon Master Bridge[1]	Altera Corporation
UART[1]	Altera Corporation
JTAG UART[1]	Altera Corporation
JTAG/Avalon Master Bridge[1]	Altera Corporation
UART	Eureka Technology Inc.
H8250[2]	CAST, Inc.

Interfaces and protocols (continued)

Product name	Vendor name
Serial (continued)	
Programmable Interval Timer/ Counter, 8254	CAST, Inc.
MD5	CAST, Inc.
Smart Card Reader	CAST, Inc.
DSPI Serial Peripheral Interface Master/Slave[2]	Digital Core Design
SD Host Controller	SLS
SD/MMC SPI[2]	El Camino GmbH
SDIO/SD Memory /MMC Host Controller	Eureka Technology Inc.
PowerPC Bus Arbiter	Eureka Technology Inc.
PowerPC Bus Master[2]	Eureka Technology Inc.
PowerPC Bus Slave	Eureka Technology Inc.
AHB to PCI Host Bridge	Eureka Technology Inc.
PowerPC/SH/1960 System Controller	Eureka Technology Inc.
Audio and Video	
Character LCD[1]	Altera Corporation
Pixel Converter (BGR0 ->BGR)[1]	Altera Corporation
Video Sync Generator[1]	Altera Corporation
ASI[2]	Altera Corporation
SD/HD/3G-HD SDI	Altera Corporation
I2S Audio CODEC	SLS

[1] SOPC Builder component (no license required)
[2] SOPC Builder-ready licensed core

IP megafunctions

Memories and memory controllers

Product name	Vendor name
DMA	
Scatter Gather DMA Controller[1]	Altera Corporation
DMA Controller[1]	Altera Corporation
DMA Controller	Eureka Technology Inc.
DMA Controller for AHB[2]	Eureka Technology Inc.
Flash	
NAND Flash Memory Controller - nflashctrl	CAST, Inc.
NAND FLASH Controller	Eureka Technology Inc.
CompactFlash (True IDE)[1]	Altera Corporation
EPCS Serial Flash Controller[1]	Altera Corporation
Flash Memory[1]	Altera Corporation
Compact Flash Interface	SLS
ISA/PC Card/PCMCIA/Compact Flash Host Adapter	Eureka Technology Inc.
SDRAM	
Streaming Multi-Port SDRAM Memory Controller	Microtronix
HyperDrive Multi-Port DDR2 Memory Controller	Microtronix
DDR and DDR2 SDRAM Controllers[2]	Altera Corporation
DDR and DDR2 SDRAM High-Performance Controllers[2]	Altera Corporation
DDR3 SDRAM High-Performance Controller[2]	Altera Corporation
DDR SDRAM Controller	CAST, Inc.
DDR SDRAM Controller	Northwest Logic, Inc.
DDR2 SDRAM Controller	Northwest Logic, Inc.
Mobile DDR SDRAM Controller	Northwest Logic, Inc.
Mobile SDR SDRAM Controller	Northwest Logic, Inc.
SDR SDRAM[1]	Altera Corporation
SDR SDRAM Controller	CAST, Inc.
SDR SDRAM Controller	Northwest Logic, Inc.
Avalon Multi-Port SDRAM Memory Controller[2]	Microtronix
RLDRAM II Controller	Altera Corporation
RLDRAM II Controller	Northwest Logic, Inc.
SRAM	
SSRAM (Cypress CY7C1380C)[1]	Altera Corporation
SRAM (IDT71V416)	Altera Corporation
QDR II SRAM Controller	Altera Corporation

[1] SOPC Builder component (no license required)
[2] SOPC Builder-ready licensed core

FOR MORE INFORMATION

Online IP search engine **www.altera.com/ipmegastore**
Training **www.altera.com/training**

Quartus II design software

If you're looking for a design environment that will quickly move you from concept to creation, choose Altera's Quartus® II design software. Number one in performance and productivity for CPLD, FPGA, and HardCopy® ASIC designs, Quartus II software offers complete, automated system definition and implementation, all without requiring lower-level HDL or schematics. This capability—plus its seamless integration with leading EDA software tools and flows—will help turn your ideas into working systems in minutes.

Quartus II software

	Subscription Edition	Web Edition
Devices:	All	MAX® and Cyclone® series; Arria® GX family
Features:	100%	95%
Distribution:	Download and DVD	Download and DVD
Cost:	Paid license	Free—no license required
Operating system support:	Windows and Linux (32- and 64-bit)	Windows (32-bit only)

Quartus II design software features summary

Design flow methodology	**Incremental compilation**	Improves design timing closure and reduces design compilation times up to 70 percent. Supports team-based design.
	Up-front I/O assignment and validation	Enables PCB layout to begin earlier.
	Pin planner	Eases the process of assigning and managing pin assignments for high-density and high pin-count designs.
	SOPC Builder	Automates adding, parameterizing, and linking IP cores—including embedded processors, coprocessors, peripherals, memories, and user-defined logic.
	Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Altera's megafunction library and from Altera's third-party IP partners.
	Parallel development of FPGA prototypes and ASICs	Allows for FPGA prototypes and HardCopy ASICs to be designed in parallel using the same design software and IP.
	Scripting support	Supports command-line operation and Tcl scripting, as well as GUI design processing.
Performance and timing closure methodology	**Physical synthesis optimization**	Uses post place-and-route delay knowledge of a design to improve performance.
	Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Quartus II software settings to find optimal results.
	Extensive cross-probing	Unmatched support for cross-probing between verification tools and design source files.
	Optimization advisors	Provides design-specific advice to improve design timing performance, resource usage, and power consumption.
	Timing closure floorplan editor	Enables analysis of timing data in the floorplan.
	Chip planner	Reduces verification time (while maintaining timing closure) by enabling small, post place-and-route design changes to be implemented in minutes.
	RTL viewer and technology map viewer	Provides schematic representation that can be used to analyze a design's structure before and after its implementation.
Verification	**TimeQuest timing analyzer**	Create, manage, and analyze complex timing constraints, and quickly perform advanced timing verification with TimeQuest, an ASIC-strength timing analysis tool with native SDC support.
	SignalTap® II embedded logic analyzer	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
	PowerPlay technology	Enables you to accurately analyze and optimize both dynamic and static power consumption.
	SignalProbe routing	Routes an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer.
Third-party support	**EDA partners**	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

Free software package

Our free Quartus II Web Edition software for Windows-based PCs includes everything you need to design for Altera's latest CPLD and low-cost FPGA families, including our Arria GX FPGA family. Quartus II Web Edition software also includes support for select members of Altera's high-end FPGA families.

Free software package includes:

- Quartus II Web Edition software
  - Support for MAX series CPLDs, and Cyclone series and Arria FPGAs
  - Support for Windows (32-bit) operating system
- Nios® II Embedded Design Suite
- ModelSim®-Altera® Starter Edition simulation software
  - Optional upgrade: ModelSim-Altera Edition for faster simulation
- Evaluation of the Altera MegaCore® IP library

Altera subscription program

Altera's subscription program offers a comprehensive suite of premium software and IP products. Included in the subscription are:

- Quartus II Subscription Edition software
  - Support for all Altera devices
  - Support for Windows (32- and 64-bit), and Linux (32- and 64-bit) operating systems
- Support for enhanced productivity features
  - Incremental compilation for faster compile times
  - Multi-processor support for faster compile times
- Nios II Embedded Design Suite (EDS)
- ModelSim–Altera Starter Edition simulation software
  - Optional upgrade: ModelSim-Altera Edition for faster simulation
- Complete IP base suite, which includes full licenses to the following Altera functions:
  - FIR Compiler
  - NCO Compiler
  - FFT Compiler
  - DDR SDRAM Controller
  - DDR SDRAM High-Performance Controller
  - DDR2 SDRAM Controller
  - DDR2 SDRAM High-Performance Controller
  - DDR3 SDRAM High-Performance Controller
  - QDR II SRAM Controller
  - RLDRAM II Controller
  - SerialLite II

DSP Builder

Altera's DSP Builder creates a seamless bridge between the MATLAB/Simulink tool and Altera's Quartus II software, giving FPGA designers the algorithm development, simulation, and verification capabilities of MATLAB/Simulink system-level design tools.

Download the latest software and IP in the Altera subscription program at www.altera.com/download.

SOPC Builder

SOPC Builder is a Quartus II IP integration tool that enables you to quickly and easily build systems in minutes. Using SOPC Builder, you can focus on your custom user logic design, differentiating functions by eliminating manual system integration tasks. In addition to your custom logic, you can select common functions from the Altera or Altera partner IP core libraries to include in your system. SOPC Builder automatically generates interconnect logic to make the system work optimally and creates a testbench to verify functionality, saving valuable design time.

Peripheral expansion of stand-alone processors

SOPC Builder includes a component editor feature so you can easily interface to nearly any external processor or DSP device. If you create an SOPC Builder component interface to your processor, you can add additional I/O pins, prepackaged peripherals, or custom, self-made peripherals in just a few mouse clicks. SOPC Builder will build the system and output header files for your software development team. Your team can then access the peripherals from the external processor using their preferred integrated development environment.

Connecting to ASSPs or CPUs

Many ASSPs and processors include standard interface protocols, such as PCI, PCI Express, Serial RapidIO®, SPI, and I^2C. SOPC Builder and SOPC Builder-ready IP let you easily connect your FPGA system to popular external ASSPs and CPUs using the standard interface protocols.

SOPC Builder features summary

IP selection and parameter selection	Select and parameterize off-the-shelf IP from Altera and our partners or create your own custom components. Off-the-shelf IP includes the Nios II processor, ARM® Cortex-M1 processor, V1 ColdFire processor, memory interfaces, common embedded system peripherals, bridges and interfaces, DSP IP, and hardware accelerator peripherals.
System interconnect fabric generation	Uses an optimal interconnect fabric created specifically for the requirements of each system. Integration tasks automatically performed by SOPC Builder include: • Datapath multiplexing between design blocks • Address decoding • Wait-state generation • Dynamic bus sizing • Interrupt priority assignment • Clock domain crossing to connect peripherals or systems operating on different clock domains
Component editor	Allows you to create your own custom SOPC Builder components.
IP reuse	Reuse any custom-created IP core designed for SOPC Builder in future products.
Testbench generation	Outputs testbench suites to test-generated systems.
Header file generation	Seamlessly integrates with Altera's Nios II EDS software to automatically generate board support packages for processor-based systems.

FOR MORE INFORMATION

Quartus II software	www.altera.com/quartus2
Quartus II Web Edition and Subscription Edition download	www.altera.com/download
Purchase Quartus II software	www.altera.com/buysoftware
Quartus II literature	www.altera.com/literature
Training	www.altera.com/training

Development kits

Altera and our partners offer an array of feature-rich development kits, boards, and companion daughtercards to help you simplify your design process and reduce time to market. These board solutions speed system design by providing you with test and debug platforms for RTL generation, while also allowing you to start developing your application software. With reference designs, cables, and programming hardware, these kits and daughtercards provide an ideal FPGA or CPLD design environment.

Companion daughtercards extend the functionality of Altera's host development kits for a variety of application areas such as video and embedded design. Beginning with our Cyclone® II and Stratix® II series development kits, Altera implemented its newly developed high-speed mezzanine connector (HSMC), enabling greater extensibility and higher performance to these host development kits. The HSMC was conceived by Altera and is manufactured and sold by Samtec. The HSMC specification is available for download from Altera's website.

Our development kits were created to be easy to master, delivering detailed example designs supporting Quartus® II design software and a variety of programming options for Altera® devices. What's more, these kits provide a platform for you to use the Altera IP simulation and hardware evaluation flow.

DSP development kits

Prototype and debug DSP designs for programmable logic using Altera DSP development kits. These kits include all of the critical design resources you'll need: a DSP development board populated with an Altera FPGA, Quartus II software (one-year, time-limited license), DSP Builder (Quartus II MATLAB/Simulink interface), a 30-day evaluation copy of MATLAB/Simulink, and system reference designs. In addition, by using the hardware evaluation feature of our DSP IP, you can jump-start your designs for video and image, wireless, and other complex digital communications by implementing entire subsystems in hardware within hours.

I/O interconnect development kits

Altera and our partners offer cost-effective development kits to evaluate high-speed interfaces. Consider, as an example, the Transceiver Signal Integrity Development Kit, Stratix IV GX Edition. This kit enables you to verify our embedded transceiver for use with a wide variety of interfaces such as PCI Express, Gigabit Ethernet, XAUI, Fibre Channel, Serial RapidIO®, HD-SDI, and other major standards.

Each I/O interconnect board comes with a one-year license to Quartus II design software, a user application, and a library of reference designs. You can also use the development kits and hardware IP evaluation to assess a variety of high-speed interconnect IP cores as well as to rapidly prototype and debug in a real-time environment.

Embedded development kits

For embedded processor system development, Altera's embedded development kits provide a great starting point. The Altera Nios® II development kits include Nios II embedded processors and a perpetual license to create embedded systems, the Nios II EDS, and access to more than 60 peripheral IP cores. The kits contain Quartus II design software (one-year, time-limited license), a feature-rich FPGA-based development board (including power supply, USB-Blaster™ download cable, and LCD display), extensive reference designs, tutorials, and complete documentation. In addition, numerous partners are offering companion boards enabling application-specific embedded Nios II development.

Nios II Development Kit, Stratix Edition

DSP Cyclone III EP3C120 board with daughtercard

General-purpose development kits

Whether designing with our MAX® II CPLDs, Cyclone series FPGAs, or Stratix series FPGAs, you can get off the ground quickly with our portfolio of low-cost, easy-to-use development kits. For example, the MAX II Development Kit provides a complete design environment with all of the software, cables, and accessories needed to evaluate the MAX II feature set or begin prototyping a design before you've received custom hardware. These kits enable increased design productivity whether you're evaluating one of the devices, validating your design, prototyping, or using FPGAs as part of your ASIC prototyping strategy.

Development kits

DSP

Product name and vendor name	Device	Description
DSP Development Kit, Cyclone III Edition[1] [DK-DSP-3C120N] **Altera Corporation**	Cyclone III EP3C120N	This kit is for general DSP or wireless design engineers, regardless of whether you need pre-processing, DSP plus FPGA coprocessing, or post-processsing. Complete high-speed analog-to-digital (A/D) and (D/A) digital-to-analog conversion capability (16-bit, 200 megasamples per second) is included as well as interfaces to DM642 and DaVinci. Altera's DSP Builder GUI simplifies the information flow between the FPGA toolset and MATLAB/Simulink (30-day evaluation copy included).
Cyclone III Video and Image Processing Development Kit* **Bitec**	Cyclone III EP3C120N	This kit is designed to help you start developing complex video applications. It supports various video I/O interfaces, allowing you to get your video data in and out of the Cyclone III FPGA. Different video interfaces are supported using the different daughtercards included in this kit: cards supporting ASI/SDI, composite, component, and digital video interfaces (DVIs).
SPR Development System **Bittware**	Cyclone III FPGA	The Software Programmable Reconfiguration (SPR) development system provides a system platform to explore software reconfiguration of waveform functionality for high-end signal processing applications such as software-defined radio (SDR). The platform provides a flexible, portable, low-cost environment for SPR development in an AMC and MicroTCA environment, enabling you to quickly and cost-effectively bring your waveform designs to life.
Video Development Kit, Cyclone II Edition[1] [DK-VIDEO-2C70N] **Altera Corporation**	Cyclone II EP2C70N	Composite video input channels (NTSC/PAL), 10-bit BT.656 output, 2 x 2 14-bit, 125 million samples per second (MSPS) A/D, two 14-bit, 165 MSPS D/A, VGA DAC, stereo audio CODEC (96 KHz), EMIF connector, Mictor connector, expansion connector, 256-Mbit DDR2 DIMM, 1-Mbit synchronous SRAM, two EPCS64 devices, MATLAB/ Simulink evaluation software, DSP Builder development tool.
Tetra-PMC **Bittware**	Cyclone II FPGA	The Tetra-PMC+ (TRPM) board is a high-speed analog input board that provides data capture for four 14-bit A/D channels running at up to 105 MHz. The board streams the data directly to an Altera Cyclone II FPGA, which provides A/D control, data distribution, and front-end processing capabilities. A 32-bit, 66-MHz PCI interface and four TigerSHARC link ports make the captured data available to the host board.
DSP Development Kit, Stratix II Edition[1] [DK-DSP-2S60N] **Altera Corporation**	Stratix II EP2S60N	2-channel 12-bit, 125 MSPS A/D, 2-channel 14-bit 165 MSPS D/A, VGA DAC, stereo audio CODEC 96 KHz, connector for Texas Instuments C6000 kit, two 40-pin connectors for Analog Devices A/D boards, Mictor connector, RSD232 serial port, RJ45, 32-Mbyte SDR SDRAM, 16-Mbyte flash, 1-Mbit SRAM, 16-Mbyte compact flash, MATLAB/ Simulink evaluation software, Quartus II development kit edition (DKE) software, DSP Builder development tool, evaluation DSP IP cores, system reference designs and labs, Nios II reference designs.
DSP Development Kit, Stratix II Professional Edition[1] [DK-DSP-2S180N] **Altera Corporation**	Stratix II EP2S180N	2-channel 12-bit, 125 MSPS A/D, 2-channel 14-bit 165 MSPS D/A, VGA DAC, stereo audio CODEC 96 KHz, connector for TI C6000 kit, two 40-pin connectors for Analog Devices A/D boards, Mictor connector, RSD232 serial port, RJ45, 32-Mbyte SDR SDRAM, 16-Mbyte flash, 1-Mbit SRAM, 16-Mbyte compact flash, MATLAB/Simulink evaluation software, Quartus II DKE, DSP Builder development tool, evaluation DSP IP cores, system reference designs and labs, Nios II reference designs.
DSP Development Kit, Stratix III Edition [DK-DSP-3SL150N] **Altera Corporation**	Stratix III EP3SL150	This kit comprises a Stratix III development board with an HSMC equipped with 16-bit A/D and D/A converters (operating at up to 200 megasamples/per second). The HSMC also has interfaces to TI DSP processors (DM642 and DaVinci), allowing the designs that use Stratix III FPGAs to be created both as stand-alone devices and as companion devices. The kit also contains Altera's Quartus II DKE and DSP Builder software and a 30-day trial of MATLAB/Simulink.

[1] RoHS compliant

Development kits

	Product name and vendor name	Device	Description
DSP (continued)	Audio Video Development Kit, Stratix II GX Edition[1] [DK-VIDEO-2SGX90N] **Altera Corporation**	Stratix II EP2SGX90N	DVI I/Os, SD/HD/SDI I/Os, ASI I/Os, AES3 and S/PDIF audio interfaces, DDR2 DIMM, 2-Mbyte SRAM, HSMC expansion connector, 10/100/1000 Ethernet PHY, 1394 MAC/PHY, USB MAC/PHY, Video and Image Processing Suite evaluation IP cores, SDI reference design.
	B2-AMC Universal Baseband Processing Module **BittWare**	Stratix II FPGA	Stratix II FPGA, TigerSHARC DSP cluster, full-height, single-wide AMC, configurable to support Serial RapidIO®, PCI Express, GbE, and XAUI.
	GT-3U-cPCI CompactPCI Board **BittWare**	Stratix II GX EP2SGX90	Ruggedized hybrid signal processing, Stratix II FPGA, TigerSHARC DSP cluster, BittWare's ATLANTIS architecture providing 2 Gbps of external I/O throughput, DDR2 SRAM/QDR SDRAM, flash memory.
	GX-AMC **Bittware**	Stratix II GX FPGA	The GX-AMC (GXAM) is a mid-size, single-wide AdvancedMC that can be attached to Advanced Telecom Compute Architecture (AdvancedTCA) carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The GXAM features a high-density Altera Stratix II GX FPGA, BittWare's ATLANTIS framework (implemented in the FPGA), a front panel I/O interface, a control plane interface via BittWare's FINe interface bridge, an IPMI system management interface, and a configurable x8 SERDES interface supporting a variety of protocols. It also provides 10/100 Ethernet, Gigabit Ethernet, two banks of DDR2 SDRAM, one bank of QDR II SRAM, and flash memory for booting the FPGA and FINe.
	Video Input Daughtercard [DC-VIDEO-TVP5146] **Altera Corporation**	Daughtercard	Two composite video input channels using TI ADC, support for NTSC/PAL, 10-bit BT.656 output, compatibility with expansion connector found on most Altera development kits; included with Video Development Kit, Cyclone II Edition.
	SC DVI Output Module **Bitec**	Daughtercard	Supports all Altera development kits with Altera DVI expansion slots.
	THDB-ADA **Terasic**	Daughtercard	Dual AD channels with 14-bit resolution and data rate up to 65 MSPS. Dual DA channels with 14-bit resolution and data rate up to 125 MSPS. Supports both Altera HSMC and Terasic DE-style connectors.
I/O Interconnect	Arria® II GX FPGA Development Kit **Altera Corporation**	Arria II GX EP2AGX120F1152	Provides a full-featured hardware development platform for prototyping and testing of high-speed serial interfaces to an Arria II GX FPGA. PCI Express x4 form factor, includes one HSMC connector, 32-Mbyte DDR2 SDRAM, 512-Mbyte flash.
	Arria GX FPGA Development Kit [EP1AGX60N] **Altera Corporation**	Arria GX FPGA	Provides a hardware platform for development and testing of high-speed serial interfaces in Arria GX FPGAs. PCI Express x4 form factor; includes one HSMC connector, 32-Mbyte DDR2 SDRAM, 512-Mbyte flash, and a PCI Express x4 reference design.
	PCI Development Kit, Cyclone II Edition[1] [DK-PCI-2C35N] **Altera Corporation**	Cyclone II EP2C35N	Short-form universal PCI (3.3V or 5.0V) card (32/64 bit, 33/66 MHz), 128-Mbit DDR2 SDRAM, two EPCS64 devices, 100-MHz oscillator, SMA/PCI connector clock input, four user push-button switches, eight dual in-line package (DIP) switches, eight user LEDs.
	1-Lane PCI Express Board **HiTech Global**	Cyclone II EP2C50	One-lane, low-cost PCI Express development platform.
	4-Lane PCI Express Board **HiTech Global**	Cyclone II EP2C70	Four-lane PCI Express development board with external PHY.
	PCI Express Design Kit with Cyclone II + External PHY **PLDApplications**	Cyclone II EP2C20 to EP2C50	Designed to support low-cost Altera FPGA families, includes free board version of PLDA's IP Core for PCI Express and a Phillips PCI Express x1 PHY.
	Transceiver Signal Integrity Kit, Stratix IV GX Edition **Altera Corporation**	Stratix IV GX EP4SGX230F1517	8 full duplex transceiver channels with SMA connectors, 156.25-155.52-, 125-, 100-, and 50-MHz clock oscillators, 6 user push buttons, 8 dipswitches, 8 user LEDs, 7-segment LCD display, power and temperature measurement circuitry, Ethernet, USB, and JTAG ports.

[1] RoHS compliant

Development kits

I/O Interconnect (continued)

Product name and vendor name	Device	Description
Stratix IV GX FPGA Development Kit **Altera Corporation**	Stratix IV GX EP4SGX230F1517	Provides a full-featured hardware development platform for prototyping and testing of high-speed serial interfaces to a Stratix IV GX FPGA. PCI Express x8 form factor, 2 HSMC connectors for expandability, Ethernet, USB, SDI, and HDMI interfaces. Memory includes: 1x64 DDR3, 1x16 DDR3, 2x18 QDR+, flash, and SRAM. 5 SMA connectors for differential Tx/Rx, along with 156.25-,155.52-, 125-, 100-, and 50-MHz clock oscillators. User interfaces include: 6 user push buttons, 8 DIP switches, 8 user LEDs, 7-segment LCD display, power and temperature measurement circuitry.
S4GX-AMC **Bittware**	Stratix IV GX EP4SGX230F1517	Based on Altera's Stratix IV GX FPGA, BittWare's S4GX-AMC is a mid-size, single wide AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. This board has two banks of DDR3 SDRAM (up to 1 Gbyte each), and two banks of QDR II SRAM (up to 9 Mbytes). Includes IP support for Serial RapidIO, PCI Express, Gigabit Ethernet, XAUI (10 Gigabit Ethernet), CPRI, and OBSAI interfaces.
SF/GX-AMC **Bittware**	Stratix II GX EP2SGX130	Based on Altera's Stratix II GX FPGA, BittWare's SF/GX-AMC is a full-size, single wide AdvancedMC that can be attached to AdvancedTCA (advanced telecom compute architecture) carriers or other cards equipped with advanced mezzanine card (AMC) bays, and used in MicroTCA systems. The SF/GX-AMC has all the features of the GX-AMC card and includes four small form-factor pluggable-plus (SFP/SFP+) compact optical transceiver connectors.
PCI Express Development Kit, Stratix II GX Edition[1] [DK-PCIE-2SGX90N] **Altera Corporation**	Stratix II GX EP2SGX90N	PCI Express IP core (eval), two HSMC connectors, 10/100/1000 Ethernet PHY, two SFP interfaces, 256-Mbit DDR2 SDRAM, 2-Mbit QDR II SRAM, 64-Mbyte flash.
PCI XpressGXII Board **PLDApplications**	Stratix II GX EP2SGX90	Includes free PCI Express IP core, x1, x4, x8 configurations, FPGA-based, x8 PCI Express male connector, endpoint PCI Express designs.
8-Lane PCI Express Board **HiTech Global**	Stratix II GX EP2SGX90 and EPS2SGX130	Eight-lane PCI Express development platform (endpoint).
Transceiver Signal Integrity Development Kit, Stratix II GX Edition* [DK-SI-2SGX90N] **Altera Corporation**	Stratix II GX EP2SGX90N	Six full-duplex transceiver channels with SMA connectors, one microstrip channel, four matched stripline channels, 25-MHz and 156.25-MHz clock oscillators, SMA clock input, six user push-button switches, eight DIP switches, eight user LEDs, two 7-segment displays, USB port.
MimoKit FPGA Development Platform **Comsis**	Stratix II EP2S180	The MimoKit is designed for extensively networked embedded applications that require wireless LAN connectivity and Gigabit Ethernet. Based on two Stratix II EP2S180 FPGAs, the MimoKit permits the implementation of extremely complex digital processing blocks, such as those found in modern multi-antenna WLAN interfaces.
PCI X/PCI Development Kit (PCIXSYS2) **PLDApplications**	Stratix II EP2S60 to EP2S180	Ideally suited for ASIC/FPGA prototyping, data acquisition applications.
DN7000K10PCIS **The Dini Group**	Stratix II EP2S90, EP2S130, or EP2S180	Complete LE system providing ASIC or IP designers with a vehicle to cost-effectively prototype logic and memory design.
PCI/PCI-X Board **HiTech Global**	Stratix II EP2S90, EP2S130, or EP2S180	PCI/PCI-X development platform.
802.11b Wireless Design Kit **Microtronix Inc.**	Daughtercard	Kit includes a wireless 802.11b CompactFlash card and a Microtronix CompactFlash board.
Ethernet USB Expansion Kit **Microtronix Inc.**	Daughtercard	Kit includes a wireless 802.11b CompactFlash card and a Microtronix CompactFlash board.
I^2C Design Kit **Microtronix Inc.**	Daughtercard	Provides an easy way to design, develop, and test the Microtronix I^2C IP core.
10/100/1000 Ethernet PHY Daughter Board with Marvell PHY **MorethanIP**	Daughtercard	Provides the ability to implement high-speed Ethernet PHY solutions for prototyping and evaluation and embedded software development.
10/100/1000 Ethernet PHY Daughter Board with National Semiconductor PHY **MorethanIP**	Daughtercard	Provides the ability to implement fast Ethernet solutions for prototyping and evaluation and embedded software development.

[1] RoHS compliant

Development kits

	Product name and vendor name	Device	Description
Embedded	Nios II Embedded Evaluation Kit, Cyclone III Edition[1] [DK-N2EVAL-3C25N] **Altera Corporation**	Cyclone III EP3C25N	Beginners can check out the pre-built, eye-catching demos displayed on the LCD touch screen, or do some lightweight development. Advanced microcontroller designers can learn about the "hottest" techniques, multi-processor systems, hardware acceleration using Nios II C2H Compiler, or about designing a complete system in 30 minutes. The kit includes a complete hardware and software design environment for a 32-bit microcontroller plus FPGA evaluation.
	Cyclone III FPGA Development Kit [PK-DEV-3C120N] **Altera Corporation**	Cyclone III EP3C120N	8-Mbyte SSRAM, 256-Mbyte DDR2 SDRAM, 64-Mbyte flash, configuration via USB, 10/100/1000 Ethernet and USB ports, on-board oscillators and SMAs, graphics LCD and character LC displays, two HSMC expansion connectors, three HSMC debug cards included, on-board power measurement circuitry. Complete documentation including reference designs: *Create your first FPGA design in an hour, Measure Cyclone III FPGA power.* This kit also includes Quartus II Web Edition design software, an evaluation edition of Nios II processor plus related design suite, and the Altera IP library.
	Nios II Development Kit, Cyclone III Edition[1] [DK-N2EVAL-3C120N] **Altera Corporation**	Cyclone III EP3C120N	Altera's Nios II family of embedded processor-based development kits, the top-selling type of kit sold in the last few years, has been outfitted with the latest in cutting-edge hardware and software technology. The unique combination of high-performance embedded processor power and easy-to-use integrated design software has been updated to take advantage of Cyclone III devices, the industry's lowest cost, first-to-market 65-nm FPGA family. This development kit provides an ideal environment for developing and prototyping a wide range of price-sensitive, high-performance embedded applications.
	Nios II Development Kit, Cyclone II Edition[1] [DK-NIOS-2C35N] **Altera Corporation**	Cyclone II EP2C35N	Perpetual Nios II license, µC-OSII evaluation version, 1-Mbit SRAM, 16-Mbit SDR SDRAM, 16-Mbit flash, CompactFlash connector header, 10/100 Ethernet MAC/PHY, two RS-232, expansion headers, debug Mictor connector, four push-button switches, eight LEDs, two 7-segment LED display.
	Firefly Modules EP2C20, EP2C35, and EP2C50 editions[1] **Microtronix Inc.**	Cyclone II EP2C20, EP2C35, and EP2C50	Complete Nios II processor system on a module, up to 95 user I/Os available, functionally compatible with Firefly I modules, hardware DSP support.
	Desktop NanoBoard NB2DSK01 **Altium**	Cyclone II FPGA	A LiveDesign-enabled, FPGA-based development board allows rapid and interactive implementation and debugging of FPGA designs and supports multiple target devices in the form of swappable FPGA daughterboards, providing a reconfigurable development platform. Upgraded from the NB1, the Desktop NanoBoard supports Cyclone II devices and provides a much larger number of I/O connections from the target FPGA to the connected peripherals.
	Quicgate Controller/FPGA **Dallas Logic**	Cyclone II FPGA	Allows implementation of general logic functions and/or Altera Nios II processor operation in a small form-factor module.
	Niomite Controller/FPGA Module **Dallas Logic**	Cyclone II FPGA	Allows implementation of FPGA logic functions and/or Altera Nios II processor operation in the smallest possible form factor.
	BDK2C35 **EBV**	Cyclone II FPGA	A broadcast development kit based on Altera's Nios II embedded processor and low-cost Cyclone II FPGA family, this kit includes basic audio/visual (A/V) and IT interface building blocks required to build professional broadcast systems on an FPGA platform while offering extensive customization options via a comprehensive range of add-on cards.
	DBC2C20 **EBV**	Cyclone II FPGA	An FPGA-based development board designed specifically for Altera's Nios II embedded processors and the .NET framework in the industrial market, this board features a Cyclone II device and is equipped with several industrial I/O standards, such as CAN, RS485, RS232, and 24V I/Os, for direct connection to the industrial automation world. Several IP cores are delivered with the board, including Ethernet MAC, CAN Controller (evaluation), and USB Controller (evaluation).

[1] RoHS compliant

Development kits

	Product name and vendor name	Device	Description
Embedded (continued)	Nios II Development Kit, Stratix II Edition[1] [DK-NIOS-2S60N] **Altera Corporation**	Stratix II EP2S60N	Perpetual Nios II license, µC-OSII evaluation version, 1-Mbit SRAM, 16-Mbit SDR SDRAM, 16-Mbit flash, CompactFlash connector header, 10/100 Ethernet MAC/PHY RJ45, RS-232, 2 expansion headers, debug Mictor connector, 2 expansion/prototype headers, Quartus DKE, Nios II EDS.
	PARIS automotive development platform **TRS-STAR**	Stratix II EP2S90 or EP2S180 Optional path to HardCopy® HC210W	Microcontroller development platform to create scalable reference designs for automotive infotainment (head-end, drivers assistance, navigation, etc.); add-on modules and reference designs available. Designs can be ported to Altera's automotive-grade Cyclone III FPGAs or HardCopy ASICs.
	DIGILAB CX II **El Camino GmbH**	Stratix II EP2S90, EP2S130, or EP2S180	Stratix II development board, stackable with four SSRAM banks, serial flash, security key supported SD/MMC socket, and 56 user I/O pins.
	Lancelot VGA IP Design Kit **Microtronix Inc.**	Daughtercard	Kit includes a small hardware board with a 24-bit RAMDAC, VGA connector, stereo audio connector, and two PS/2 connectors.
	Compact Flash Expansion Kit **Microtronix Inc.**	Daughtercard	Inexpensive module allows the addition of compact flash cards to the Microtronix Product Starter Kit development board system.
ASIC prototyping	DN7020k10 **The Dini Group**	Stratix III, Stratix IV FPGA	A complete logic prototyping system that gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to 20 Stratix III or Stratix IV devices
	DN7006K10PCIe-8T **The Dini Group**	Stratix III, Stratix IV FPGA	A complete logic prototyping system with a dedicated PCI Express interface that gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to 6 Stratix III or Stratix IV devices.
	DIGILAB SX III **El Camino GmbH**	Stratix III FPGA	A universal FPGA prototyping platform based on Altera's largest Stratix III devices. Supports 2-Mbyte Flash, 2-Mbyte SRAM, 4 Samtec expansion connectors, 2 Mictor connectors, user LEDs and pushbuttons along with RS-232, SPI, and USB interfaces.
	PROC30M , PROC9M **Gidel**	Stratix III FPGA	Designed for debug and verification of SOC ASIC designs from 3 to 100+ million gates in size with the ability to run at system clock speeds up to 300 MHz.
	PROCStar II, ProcStar III **Gidel**	Stratix III, Stratix II FPGA	Provides high-capacity, high-speed, multi-FPGA-based prototyping and end system platforms.
	PROCSuperStar **Gidel**	Stratix II FPGA	An expandable, building block-type system enabling up to 21 Altera Stratix II EP2S180 FPGAs to be used on the board.
	PROCSpark II **Gidel**	Cyclone II FPGA	Provides an FPGA-based platform for reconfigurable computing.
	Hpe Midi **Gleichmann**	Stratix, Stratix II FPGA	A flexible FPGA and ASIC development system to replace the Hpe_compact. The Hpe_midi delivers a low-cost environment, enabling complete system development.
	DN7000K10PCI Stratix-based ASIC Prototyping Kit **The Dini Group**	Stratix II FPGA	A complete logic emulation system providing ASIC or IP designers with a vehicle to cost-effectively prototype logic and memory design.
	DNMEG S2GX Stratix II GX-Based ASIC Prototyping Kit **The Dini Group**	Stratix II GX FPGA	A logic emulation daughtercard enabling ASIC or IP designers to cost-effectively prototype logic and memory designs. The DNMEG_S2GX is hosted on any DN7000 or DN8000 series ASIC Dini Group product, but can also be used alone.
	Cyclone Compute Board **Iris Technologies**	Cyclone II FPGA	Designed for algorithm acceleration, ASIC prototyping, or simulation acceleration, this board has four Cyclone II FPGAs, a PCI Express x4 interface, and 2 Gbytes of DDR2. It can be used either within a system or as a stand-alone unit.
	DSP Compute Board **Iris Technologies**	Cyclone II FPGA	Designed for signal processing, hardware-in-loop simulation, or coprocessing applications, this board has two Cyclone II FPGAs, two TI 6416T DSPs running at 1 GHz, a PCI Express x4 interface, and 1 Gbyte of DDR2 memory. It can be used either within a system or as a stand-alone unit.
	DSP DPA Compute Board **Iris Technologies**	Cyclone II FPGA	Adds data acquisition to the DSP Compute Board by incorporating two 14-bit 125 msps ADC and two 14-bit 165 msps DACs.
	PROC2S Stratix II FPGA Board **GiDEL Limited**	Stratix II EP2S60 to EP2S180	Functions as ASIC replacement in customer prototyping environment.

[1] RoHS compliant

Development kits

	Product name and vendor name	Device	Description
ASIC prototyping (continued)	PROCStar II Development Kit **GiDEL Limited**	Stratix II EP2S60 to EP2S180 (1–4 devices)	Provides a high-capacity, high-speed FPGA-based platform
	MAGMA High-Speed Prototyping Board **ReFLEX CES**	Stratix II EP2S180	High-speed prototyping board featuring four high-density FPGA devices.
	HAC2 **Gleichmann Electronics Research**	Stratix II EP2S180	A hardware accelerator and cosimulator development tool with key features such as high-speed clock acceleration and hardware-in-the-loop for rapid system exploration.
	DNMEG S2GX Stratix II GX-Based ASIC Prototyping Kit **The DiNi Group**	Stratix II GX daughtercard	A logic emulation daughtercard enabling ASIC or IP designers to cost-effectively prototype logic and memory designs.
General purpose	Arria II GX FPGA Development Kit **Altera Corporation**	Arria II GX EP2AGX120F1152	Provides a full-featured hardware development platform for prototyping and testing of high-speed serial interfaces to an Arria II GX FPGA. PCIe x4 form factor, includes one HSMC connector, 32-Mbyte DDR2 SDRAM, 512-Mbyte flash.
	Cyclone III FPGA Starter Kit[1] [DK-START-3C25N] **Altera Corporation**	Cyclone III EP3C25N	1-Mbyte SSRAM, 16-Mbytes DDR SDRAM, 16-Mbytes parallel flash, configuration via USB, four user push buttons, four user LEDs, power measurement circuitry. Complete documentation including reference designs: *Create your first FPGA design in a hour*, *Measure Cyclone III FPGA power*, and *Create your first Nios II*. This kit also includes Quartus II Web Edition design software, evaluation edition of Nios II processor plus related design suite, and Altera IP library.
	Video Development Kit **Bitec**	Cyclone III FPGA	This kit contains the Cyclone III EP3C120 Development Kit and two HSMC video interface cards together with a collection of IP cores and reference designs. The kit provides a variety of video interface standards including both digital and analog up to HD resolutions.
	ViClaro III HD Video Enhancement Development Platform **Microtronix**	Cyclone III FPGA	A video enhancement development platform supporting 100/120-Hz HDTV that is 1080p bandwidth-capable and features 32-bit DDR II SDRAM memory, an HDMI transmitter, an analog/HDMI receiver, and dual LVDS links.
	Cyclone II FPGA Starter Development Kit[1] [DK-CYCII-2C20N] **Altera Corporation**	Cyclone II EP2C20N	8-Mbit SDRAM, 512-Kbit SRAM, 1/4-Mbit flash, 24-bit audio CODEC, 10 switches, four push buttons, four 7-segment displays, 10 red and eight green LEDs, VGA, RS-232, and PS/2 ports, two 40-pin expansion ports, SD/MMC socket.
	DB2C5 **EBV**	Cyclone II EP2C5	Provides an entry point into Altera's current FPGA technology. Three LVDS input channels and output channels are available for high-speed communication with other modules. Available I/O pins are connected with plugs on the underside of the board.
	DB2C20 **EBV**	Cyclone II EP2C20	FPGA-based development board designed specifically for Altera's Nios II embedded processors and the .NET Framework in the industrial market.
	DE2 Development and Education Board **Terasic Technologies Inc.**	Cyclone II EP2C35	• Development and education board • Many high-end multimedia features (USB, CD-quality audio, digital television (DTV), Ethernet, SD, and LCD) • Many reference designs with free source code
	Hpe Mini **Gleichmann Electronics Research**	Cyclone II EP2C35	An FPGA and ASIC SOC development tool with variants to create simplified or complex CPU systems.
	ViClaro II HD Video Enhancement Development Platform **Microtronix**	Cyclone II FPGA	A platform for quickly creating, testing, and deploying new picture enhancement algorithms. The HDMI transmitter and receiver support the defacto standard HDTV digital interface. The dual LVDS links are 1080p-bandwidth capable and support 50-/60-Hz HDTV display systems. When combined with IP, the board can be used to convert or enhance video quality.
	Stratix IV GX FPGA Development Kit **Altera Corporation**	Stratix IV GX EP4SGX230F1517	Provides a full-featured hardware development platform for prototyping and testing of high-speed serial interfaces to a Stratix IV GX FPGA. PCIe x8 form factor, 2 HSMC connectors for expandability, Ethernet, USB, SDI, and HDMI interfaces. On-board memory includes: 1x64 DDR3, 2x32 DDR3, 2x18 QDR+, flash, and SRAM. 5 SMA connectors for differential Tx/Rx, along with 155.52-, 156.25-, 125-, 100-, and 50-MHz clock oscillators. User interfaces include: 6 user push buttons, 8 dipswitches, 8 user LEDs, 7-segment LCD display, power and temperature measurement circuitry.

[1] RoHS compliant

Development kits

General purpose (continued)

Product name and vendor name	Device	Description
Stratix III FPGA Development Kit [DK-DEV-3SL150N] **Altera Corporation**	Stratix III EP3SL150	This kit allows rapid and early development of designs for high-performance Stratix III FPGAs. The development board provides general I/Os that connect to on-board switches and indicators, and to the included 2-line LCD and 128x64-pixel graphics display. The board also has non-volatile and volatile memories (64-Mbyte flash, 4-Mbyte pseudo-SRAM, 36-Mbit QDR II SRAM, 128-Mbyte DDR2 DIMM, and 16-Mbyte DDR2 device), HSMC, and triple-speed Ethernet interfaces. The kit is delivered with Quartus II DKE software and all of the cabling required to start using the board straight out of the box.
Hpe Compact **Gleichmann Electronics Research**	Stratix II EP2S60 to EP2S180	An FPGA and ASIC development tool providing a low-cost environment for creating complete system development.
RUBY II PMC Prototyping Board **ReFLEX CES**	Stratix II EP2S60 to EP2S180	PCI mezzanine card (PMC) prototyping board supporting Stratix II devices in 1,020-pin FPGA packages.
TREX S2 Prototyping System **Terasic Technologies Inc.**	Stratix II EP2S60 to EP2S180	700 available user I/O pins, flexible and reusable, a selection of various motherboards, high-speed connectors to enable DDR2 memory access.
Stratix II Demo Board **Galaxy**	Stratix II EP2S180	Designed for IC development and verification, compatible with Altera Stratix II FPGAs in 1,020-pin packages.
DB1270 **EBV**	MAX II EPM1270	Low-cost MAX II CPLD development board providing a hardware platform for a wide range of applications.
MAX II Starter Kit **Galaxy**	MAX II EPM1270	Kit can also be used by designers interested in simulating and synthesizing programmable logic circuits in their applications.
MAX II Development Kit[1] [DK-MAXII-1270N] **Altera Corporation**	MAX II EPM1270N	USB MAC/PHY, PCI Edge connector (3.3V and 5V tolerant), LCD module, SRAM (128K x 8 bit), temperature gauge with serial peripheral interface (SPI), onboard power meter, active I/O sense circuitry, expansion/prototype header, four switches, four LEDs.
DBMAXLED **EBV**	MAX II EPM1270	Demonstrates that a single MAX II EPM1270 device can drive a large number of PWM channels.
MAX II Micro **Terasic Technologies, Inc.**	MAX II CPLD	• Development and education board for CPLD design • MAX II micro board with MAX II EPM2210F324C3 (largest CPLD in MAX II series) and on-board USB-Blaster cable • Reference designs with source code
DIGILAB picoMAX Prototyping Board and Starter Kit **El Camino GmbH**	MAX EPM3032A to EPM7160S	MAX 3000/MAX 7000 starter kit, includes download/programming hardware.
DB3128 **EBV**	MAX EPM3128A	Low-cost MAX 3000A CPLD development board with 128 macrocells provides an easy entry point into Altera's CPLD technology.
DB3256 **EBV**	MAX EPM3256A	5.2-megapixel camera daughtercard with selectable frame rates and resolutions.
PM410 StarFabric Compact PCI Carrier Board **Parsec**	MAX EPM3256A	Two 3.3V PMC sites, 32-/64-bit 33-/66-MHz PCI busses, 2.5-Gbps StarFabric links on J3, supports full PCI bandwidth.
TRDB_DC2 1.3 Megapixel Camera Module **Terasic Technologies Inc.**	Daughtercard	Complete digital camera reference design with source code in Verilog HDL, user manual with live demo examples; supports exposure, light-control, and motion capture.
TRDB_LCM Digital Panel Daughtercard **Terasic Technologies Inc.**	Daughtercard	3.6" digital panel development kit, reference designs (TV player and color pattern generator) with source code in Verilog HDL.
HSMC DVI Input/Output Module **Bitec**	Daughtercard	DVI TX/RX module for the HSMC interface enables you to interface their FPGA projects to real-world DVI signals.
SC DVI Input Module **Bitec**	Daughtercard	DVI module for the Santa Cruz interface enables you to interface their FPGA projects to real-world DVI signals.
SC DVI Output Module **Bitec**	Daughtercard	DVI module for the Santa Cruz interface enables you to drive high-resolution displays with digital clarity.
SC Camera **Bitec**	Daughtercard	5.2-megapixel camera daughtercard with selectable frame rates and resolutions.
SC Proto **Bitec**	Daughtercard	Prototyping board for the Santa Cruz interface with convenient access points to power and ground with connector break-out.

[1] RoHS compliant

FOR MORE INFORMATION

Development kits **www.altera.com/devkits**
Training **www.altera.com/training**

Configuration devices

Altera offers two options for FPGA configuration. Serial configuration using one of our configuration devices is the simplest solution, with minimal connection and board space requirements. For a faster, more flexible solution, try parallel configuration using a common flash interface (CFI) flash memory and a MAX® II CPLD to speed power-up configuration time and expand your configuration device options.

Serial configuration devices features summary

Low-cost leadership	Serial configuration devices are designed for low cost. They are the ideal complement to the Cyclone FPGA series to create the lowest-cost system-on-a-programmable-chip (SOPC) solution. They also serve as a low-cost, small-form factor solution for the Stratix FPGA series and Arria GX FPGAs.
ISP	In-system-programmability increases design flexibility by allowing in-system design updates and reduces costs by streamlining the manufacturing process.
Flash memory access	Several interface peripherals available with the Nios® and Nios II embedded processors allow you to access the serial configuration device as a memory module connected to your embedded system. Device memory capacity not consumed storing configuration data can be used as general-purpose non-volatile memory, which is perfect for program and data storage. You can also use a Nios II processor to modify configuration data, which is useful for in-field system updates.
Small form factor	The serial configuration devices are available in space-saving 8-pin and 16-pin small-outline integrated circuit (SOIC) packages.

Serial configuration

Altera® serial configuration devices store the configuration file for Altera's SRAM-based FPGAs, including Arria®, Cyclone®, and Stratix® series FPGAs. We designed our serial configuration devices to minimize cost and board space while providing a dedicated FPGA configuration solution. Because these devices are cost-optimized, they feature fewer pins, smaller packages, and by extension lower prices and performance than parallel configuration solutions.

Key features

- Low cost
- In-system programmability
- Flash memory access
- Small form factor

Serial configuration device	Memory size (bits)
EPCS1	1,048,576
EPCS4	4,194,304
EPCS16	16,777,216
EPCS64	67,108,864
EPCS128	134,217,728

Serial configuration devices for Cyclone III FPGAs

Cyclone III device	Raw binary file size (bits) [1]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP3C5	2,949,120	–	✓	✓	✓	✓
EP3C10	2,949,120	–	✓	✓	✓	✓
EP3C16	4,087,808	–	✓	✓	✓	✓
EP3C25	5,750,784	–	–	✓	✓	✓
EP3C40	9,535,488	–	–	✓	✓	✓
EP3C55	14,893,056	–	–	✓	✓	✓
EP3C80	19,972,096	–	–	✓ [2]	✓	✓
EP3C120	28,573,696	–	–	✓ [2]	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Cyclone III compression feature enabled.

Serial configuration devices for Cyclone II FPGAs

Cyclone II device	Raw binary file size (bits) [1]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP2C5	1,265,792	✓ [2]	✓	✓	✓	✓
EP2C8	1,983,536	–	✓	✓	✓	✓
EP2C20	3,892,496	–	✓	✓	✓	✓
EP2C35	6,848,608	–	–	✓	✓	✓
EP2C50	9,535,488	–	–	✓	✓	✓
EP2C70	14,319,216	–	–	✓	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Cyclone II compression feature enabled.

Serial configuration devices for Cyclone FPGAs

Cyclone device	Raw binary file size (bits) [1]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP1C3	1,265,792	✓	✓	✓	✓	✓
EP1C4	1,983,536	✓	✓	✓	✓	✓
EP1C6	3,892,496	✓ [2]	✓	✓	✓	✓
EP1C12	6,848,608	–	✓	✓	✓	✓
EP1C20	14,319,216	–	✓	✓	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Cyclone compression feature enabled.

Serial configuration devices for Arria II GX FPGAs

Arria II GX device	Raw binary file size (bits) [1, 2]	Serial configuration device			
		EPCS4	EPCS16	EPCS64	EPCS128
EP2AGX20	10,325,712	–	✓	✓	✓
EP2AGX30	10,325,712	–	✓	✓	✓
EP2AGX45	27,834,480	–	–	✓	✓
EP2AGX65	27,834,480	–	–	✓	✓
EP2AGX95	47,441,600	–	–	✓	✓
EP2AGX125	47,441,600	–	–	✓	✓
EP2AGX190	81,656,584	–	–	–	✓
EP2AGX260	81,656,584	–	–	–	✓

[1] These are uncompressed file sizes.
[2] These values are preliminary.

Serial configuration devices for Arria GX FPGAs

Arria GX device	Raw binary file size (bits) [1]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP1AGX20C EP1AGX20D	9,640,672	–	–	✓	✓	✓
EP1AGX35C EP1AGX35D	9,640,672	–	–	✓	✓	✓
EP1AGX50C EP1AGX50D	16,951,824	–	–	✓ [2]	✓	✓
EP1AGX60C EP1AGX60D EP1AGX60E	16,951,824	–	–	✓ [2]	✓	✓
EP1AGX90E	25,699,104	–	–	✓ [2]	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Arria compression feature enabled.

Serial configuration devices for Stratix IV GT FPGAs

Stratix IV GT device	Raw binary file size (bits) [1, 3]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP4S40G2	102,000,000	–	–	–	✓ [2]	✓
EP4S40G5	189,000,000	–	–	–	–	✓ [2]
EP4S100G2	102,000,000	–	–	–	✓ [2]	✓
EP4S100G3	189,000,000	–	–	–	–	✓ [2]
EP4S100G4	189,000,000	–	–	–	–	✓ [2]
EP4S100G5	189,000,000	–	–	–	–	✓ [2]

[1] These are uncompressed file sizes.
[2] This is with the Stratix IV GT compression feature enabled.
[3] These values are preliminary.

Serial configuration devices for Stratix IV GX FPGAs

Stratix IV GX device	Raw binary file size (bits) [1, 3]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP4SGX80	51,000,000	–	–	–	✓	✓
EP4SGX100	51,000,000	–	–	–	✓	✓
EP4SGX220	102,000,000	–	–	–	✓ [2]	✓
EP4SGX290	140,000,000	–	–	–	–	✓ [2]
EP4SGX360	140,000,000	–	–	–	–	✓ [2]
EP4SGX530	189,000,000	–	–	–	–	✓ [2]

[1] These are uncompressed file sizes.
[2] This is with the Stratix IV compression feature enabled.
[3] These values are preliminary.

Serial configuration devices for Stratix IV E FPGAs

Stratix IV E device	Raw binary file size (bits) [1, 3]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP4SE100	51,000,000	–	–	–	✓	✓
EP4SE220	102,000,000	–	–	–	✓ [2]	✓
EP4SE290	140,000,000	–	–	–	–	✓ [2]
EP4SE360	140,000,000	–	–	–	–	✓ [2]
EP4SE530	189,000,000	–	–	–	–	✓ [2]
EP4SE630	229,000,000	–	–	–	–	✓ [2]

[1] These are uncompressed file sizes.
[2] This is with the Stratix IV compression feature enabled.
[3] These values are preliminary.

Serial configuration devices for Stratix III FPGAs

Stratix III device	Raw binary file size (bits) [1, 3]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP3SL50	22,000,000	–	–	✓ [2]	✓	✓
EP3SL70	22,000,000	–	–	✓ [2]	✓	✓
EP3SL110	47,000,000	–	–	–	✓	✓
EP3SL150	47,000,000	–	–	–	✓	✓
EP3SL200	66,000,000	–	–	–	✓	✓
EP3SE260	93,000,000	–	–	–	✓ [2]	✓
EP3SL340	120,000,000	–	–	–	–	✓
EP3SE50	26,000,000	–	–	–	✓	✓
EP3SE80	48,000,000	–	–	–	✓	✓
EP3SE110	48,000,000	–	–	–	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Stratix III compression feature enabled.
[3] These values are preliminary.

Serial configuration devices for Stratix II GX FPGAs

Stratix II GX device	Raw binary file size (bits) [1, 3]	Serial configuration device				
		EPCS1	EPCS4	EPCS16	EPCS64	EPCS128
EP2SGX30C EP2SGX30D	9,640,672	–	–	✓	✓	✓
EP2SGX60C EP2SGX60D EP2SGX60E	16,951,824	–	–	✓ [2]	✓	✓
EP2SGX90E EP2SGX90F	25,699,104	–	–	✓ [2]	✓	✓
EP2SGX130G	37,325,760	–	–	–	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Stratix II GX compression feature enabled.

Serial configuration devices for Stratix II FPGAs

Stratix II device	Raw binary file size (bits) [1]	Serial configuration device			
		EPCS4	EPCS16	EPCS64	EPCS128
EP2S15	4,721,544	✓ [2]	✓	✓	✓
EP2S30	9,640,672	–	✓	✓	✓
EP2S60	16,951,824	–	✓ [2]	✓	✓
EP2S90	25,699,104	–	✓ [2]	✓	✓
EP2S130	37,325,760	–	–	✓	✓
EP2S180	49,814,760	–	–	✓	✓

[1] These are uncompressed file sizes.
[2] This is with the Stratix II compression feature enabled.

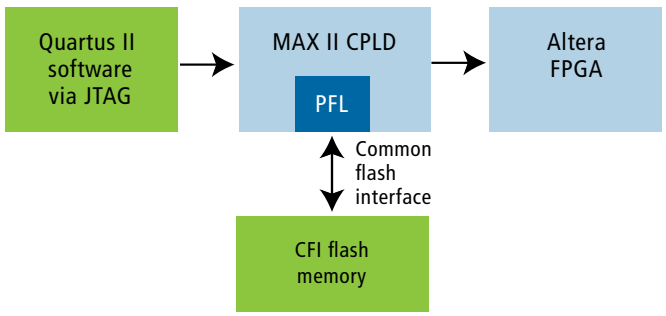
Parallel configuration

If your system already contains a CFI flash memory, you can speed power-up configuration and reduce system cost by using it together with the parallel flash loader (PFL) feature in a MAX II CPLD to configure any Altera FPGA. The MAX II device operates as a bridge between the JTAG interface and the CFI flash memory to allow programming using the Altera download cable. This option also gives you the flexibility to use a variety of industry devices to configure our FPGAs. Once configuration is complete, the PFL block releases the unused flash memory to be used by your application.

Key features

- Fast configuration
- Reduces flash-programming manufacturing costs
- Reduces cost by using flash already in system for configuration
- Does not interfere with flash operation after configuration
- Low power in standby mode
- Flexibility to work with many types of flash
- Supports remote updates

MAX II PFL feature



Parallel configuration devices

Manufacturer	Device name	Density (Mbit)
Numonyx (formerly Intel)	28F800C3	8
	28F160C3	16
	28F320C3	32
	28F640C3	64
	28F320J3	32
	28F640J3	64
	28F128J3	128
	28F640P30	64
	28F128P30	128
	28F256P30	256
	28F512P30	512
	28F640P33	64
	28F128P33	128
	28F256P33	256
	28F512P33	512
Numonyx (formerly ST Micro)	M29W32OE	32
	M29W640G	64
	M29W128G	128
Spansion	S29GL128N	128
	S29GL256N	256
	S29GL512N	512
	S29AL016D	16
	S29AL032D	32
	S29AL016M	16
	S29JL032H	32
	S29JL064H	64

FOR MORE INFORMATION

Serial configuration	www.altera.com/confighandbook
Parallel configuration	www.altera.com/parallel
Parallel configuration	www.altera.com/parallelfl
Training	www.altera.com/training

Training

Attend an Altera® technical training course to reduce your time to market and achieve optimal design results. Our courses give you the skills you need to quickly produce high-performance, small-footprint designs. Each curriculum is designed for a particular audience and provides a flowchart of recommended courses to take.

Altera instructor-led training courses *(All courses are one day in length unless otherwise noted)*

Course category	General description	Course titles
Design languages	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic.	• Introduction to VHDL • Advanced VHDL Design Techniques • Introduction to Verilog HDL • Advanced Verilog HDL Design Techniques
Software	Acquire design entry, compilation, programming, verification, and optimization skills by learning how to use both basic and advanced features of Quartus® II software.	• The Quartus II Software Design Series: Foundation • The Quartus II Software Design Series: Verification • The Quartus II Software Design Series: Timing Analysis • The Quartus II Software Design Series: Optimization
Embedded systems	Learn to design a Nios® II soft-core microprocessor system in an Altera FPGA and increase software execution speed through hardware acceleration.	• Designing with the Nios II Processor and SOPC Builder (For hardware engineers. Course length: two days.) • Developing Software for the Nios II Processor (For software engineers. Course length: two days.) • Accelerating Software Using the Nios II C2H Compiler
Memory interfaces	Implement interfaces to external memory.	• Interfacing to External Memory with Altera FPGAs
DSP	Solve DSP design challenges using Altera technology.	• Designing with DSP Builder • Designing with the DSP Builder Advanced Blockset

Online offerings

Online classes give you an overview of a variety of features and design techniques. Take advantage of these free, online training modules to preview topics covered in greater depth in our instructor-led classes, brush up on key how-to tips, or even jump-start your design.

Altera free online training courses *(Courses are approximately one hour in length)*

Course category	Course titles
General information	• Read Me First! (English only)
Design languages	• VHDL Basics (English and Chinese) • Verilog HDL Basics (English and Chinese)
Software	• Using Quartus II Software: An Introduction (English and Chinese) • The Quartus II Software Interactive Tutorial (English only) • How to Begin a Simple FPGA Design (English only) • What's New in the Quartus II Software Version 9.0 (English only) • The Quartus II Software Design Series: Foundation (Online Training) (English and Chinese) (Note: This training is equivalent to the instructor-led course of the same name) • Design Planning Guidelines for High-Density FPGAs (English only) • Using Quartus II Software: Schematic Design (English and Chinese) • Using Quartus II Software: Simulation (English and Chinese) • Overview of Mentor Graphics ModelSim Software (English only) • TimeQuest Timing Analyzer (English only) • Validating Performance with the TimeQuest Static Timing Analyzer (Chinese only) • Switching to the TimeQuest Timing Analyzer (English only) • Constraining and Analyzing Timing for Source Synchronous Circuits with TimeQuest (English only) • Introduction to Incremental Compilation (English only) • Design Partition Planner in the Quartus II Software (English only) • SignalTap® II Embedded Logic Analyzer (English only) • Design Debugging Using the SignalTap II Logic Analyzer (Chinese only) • Using Quartus II Software: Chip Planner (English only) • I/O Management (English only) • Power Analysis with the Quartus II Software (English only) • FPGA to Board Design Flow Using Mentor Graphics Tools (English only)
Embedded systems	• Designing with the Nios II Processor and SOPC Builder (Day 1) (Online Training) (English only) (Note: This training is equivalent to day 1 of the instructor-led course of the same name) • Developing Software for the Nios II Processor: Tools Overview (English and Chinese) • Developing Software for the Nios II Processor: Design Flow (English and Chinese) • Using SOPC Builder (English and Chinese) • System Console Overview (English only) • Using the Nios II Processor (English and Chinese) • System-on-a-Programmable-Chip Design Using the Nios II Embedded Processor (Japanese only) • Developing Software for the Nios II Processor: Nios II IDE (English only) • Developing Software for the Nios II Processor: Debug Primer (English and Chinese) • Developing Software for the Nios II Processor: HAL Primer (English and Chinese) • Developing Software for the Nios II Processor: Software Build Flow - Part 1 of 2 (English only) • Developing Software for the Nios II Processor: Software Build Flow - Part 2 of 2 (English only) • Developing Software for the Nios II Processor: C2H Fundamentals (English only) • Nios II C2H Compiler Fundamentals (Japanese only) • Nios II Floating-Point Custom Instructions (English only) • Developing software for the Nios II Processor: MMU and MPU (English only)

Online offerings

Altera free online training courses *(Courses are approximately one hour in length)*

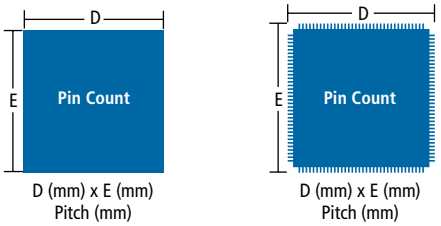
Course category	Course titles
Devices	• Basics of Programmable Logic (English and Chinese) • Arria GX Device Family Enhancements (English only) • Arria II GX Device Family Overview (English only) • Stratix III Devices: Features and Capabilities (English only) • Cyclone III Devices: Features and Capabilities (English only) • HardCopy ASIC Architecture and Design Flow (English only) • MAX IIZ CPLDs in Mobile Handsets (English and Chinese)
High speed	• Using High-Performance Memory Interfaces in Altera FPGAs (English only) • Transceiver Basics (English and Chinese) • Implementing PCI Express Solutions in Transceiver-Based FPGAs (English only) • Dynamically Reconfiguring Stratix II GX Transceivers (English only) • Serial RapidIO® Design with Altera 40-nm Devices (English and Chinese) • 10/100/1000 Mbit and 10 Gbit Ethernet Design with Altera 40-nm Devices (English and Chinese) • PCI Express Design with Altera 40-nm Devices (English and Chinese) • High-Speed Serial Protocol Design with Altera 40-nm Devices (English only) • Dynamic Signal Integrity Management with Altera 40-nm Devices (English only)
Applications	• DSP System Design with DSP Builder (English only) • DSP System Design with DSP Builder Using the Advanced Block Set (English only) • DSP Builder: Migrating from Version 6.1 to 7.1 or Later (English only) • Debugging and Communicating with an FPGA Using the Virtual JTAG Megafunction (English Only) • Viterbi Decoder (English only) • Using Cascaded-Integrator-Comb Filter in Multirate Digital Systems (English only) • Industrial Ethernet Solutions (English only) • Triple Rate SDI (English only) • Introduction to Graphics (English only) • Introduction to D/AVE GPU (English only)
Scripting	• Command Line Scripting (English only) • Introduction to Tcl Part 1 of 2 (English only) • Introduction to Tcl Part 2 of 2 (English only) • Basic Quartus II Software Tcl Scripting Part 1 of 2 (English only) • Basic Quartus II Software Tcl Scripting Part 2 of 2 (English only)

FOR MORE INFORMATION

Training www.altera.com/training

Package dimensions

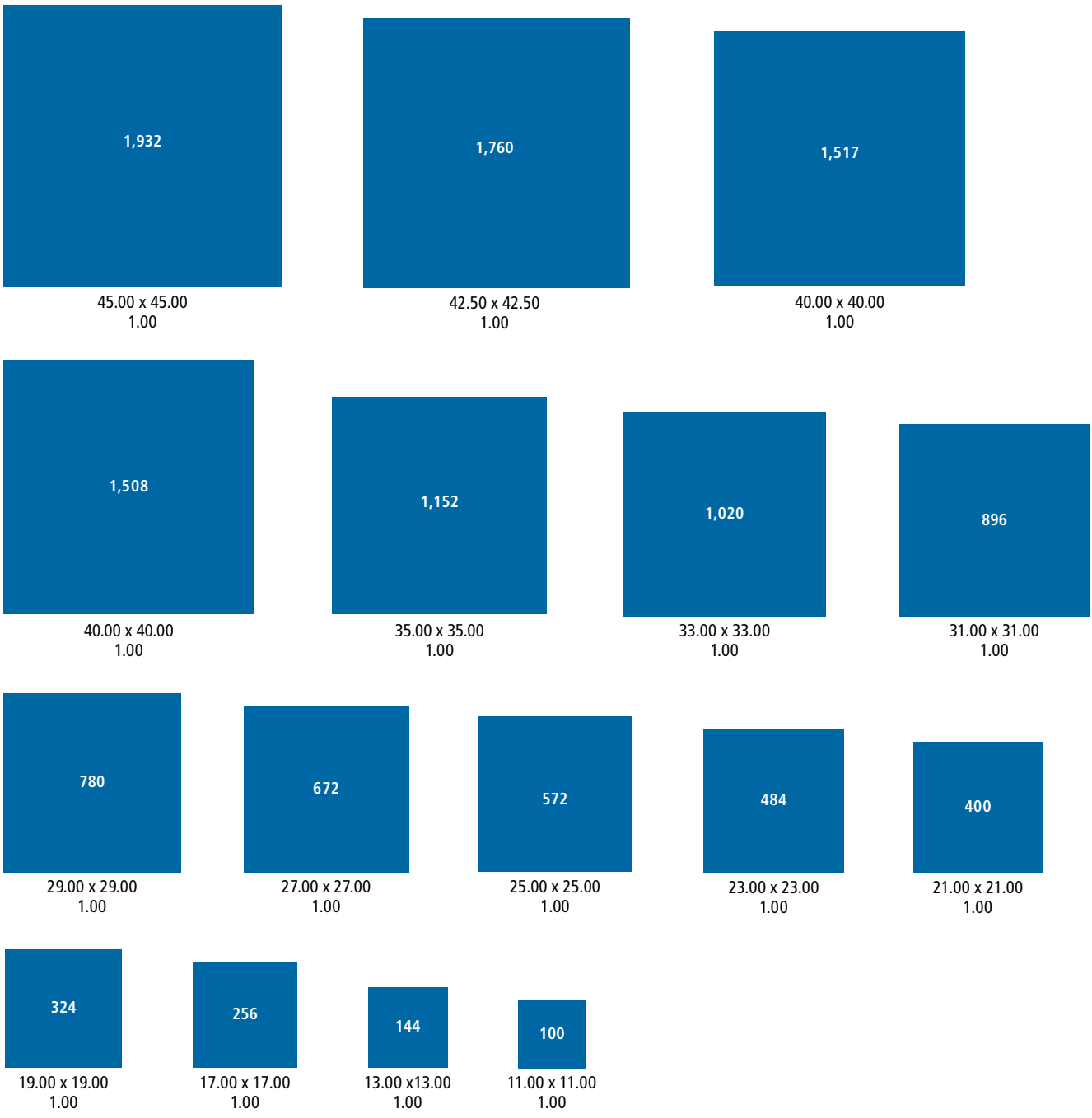
Legend



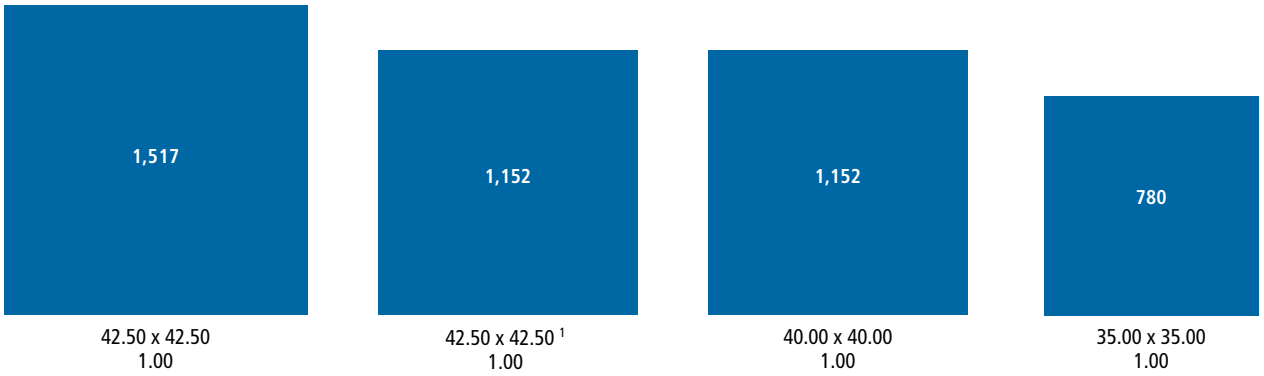
For package details, go to www.altera.com/packages

Note: Outermost dimensions are "D" and "E" for both array and peripheral package families.

FineLine BGA (FBGA)

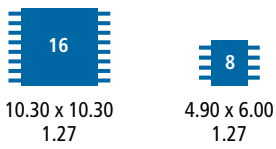


Hybrid FineLine BGA (HFBGA)

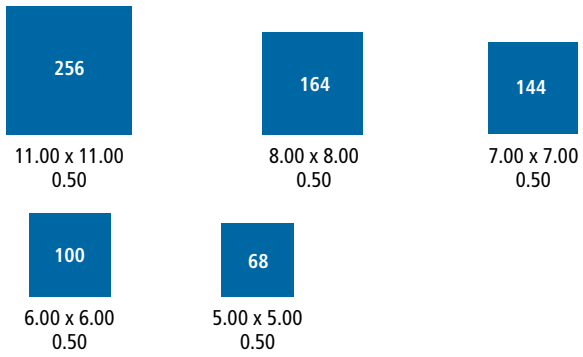


[1] Package for EP4SGX530H1152 and EP4SE530H1152 FPGAs only.

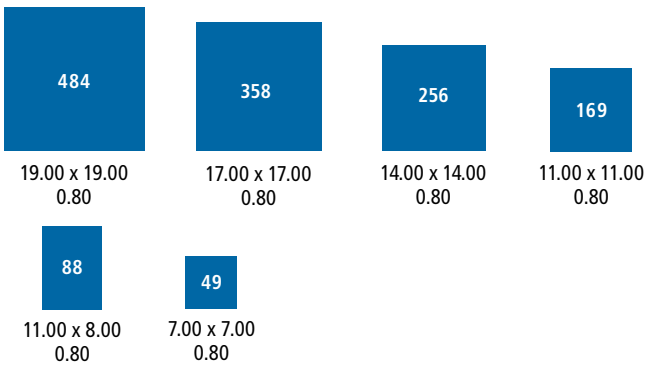
Small-Outline Integrated Circuit (SOIC)



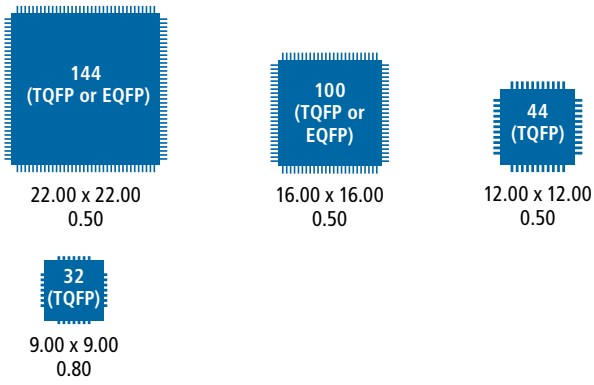
Micro FineLine BGA (MBGA)



Ultra FineLine BGA (UBGA)

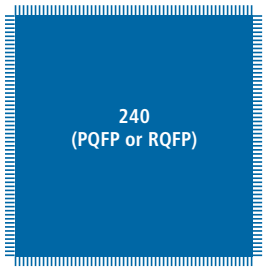


Thin Quad Flat Pack (TQFP), Enhanced Thin Quad Flat Pack (EQFP)

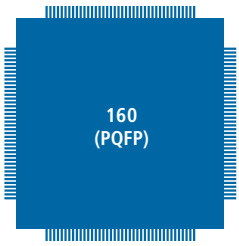


Plastic Quad Flat Pack (PQFP), Power Quad Flat Pack (RQFP)

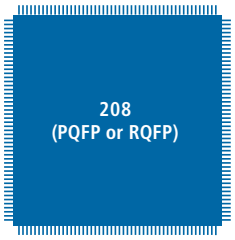
42.60 x 42.60
0.50



34.60 x 34.60
0.50



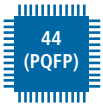
31.20 x 31.20
0.65



30.60 x 30.60
0.50

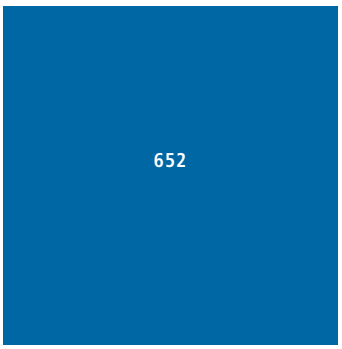
18.30 x 24.30
0.65
(EPC8 and EPC16)

17.20 x 23.20
0.65

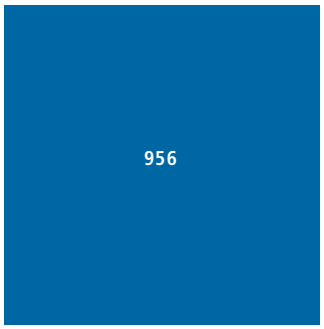


13.20 x 13.20
0.80

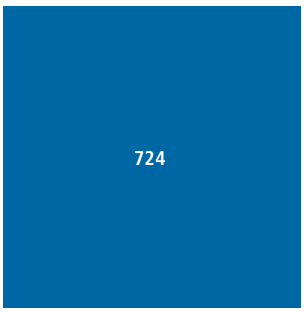
BGA



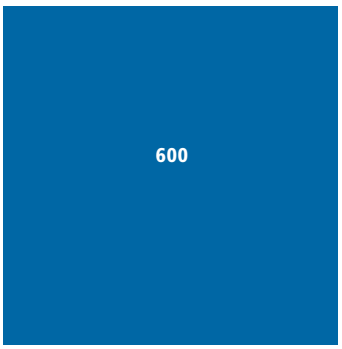
45.00 x 45.00
1.27



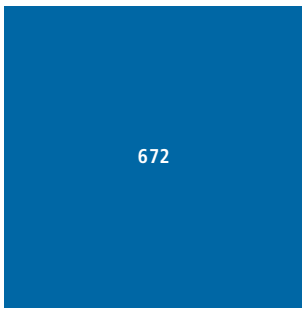
40.00 x 40.00
1.27



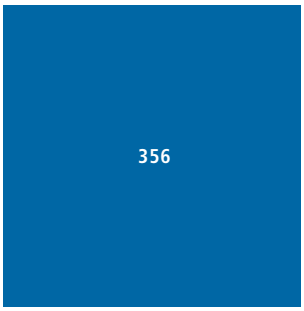
35.00 x 35.00
1.27



45.00 x 45.00
1.27



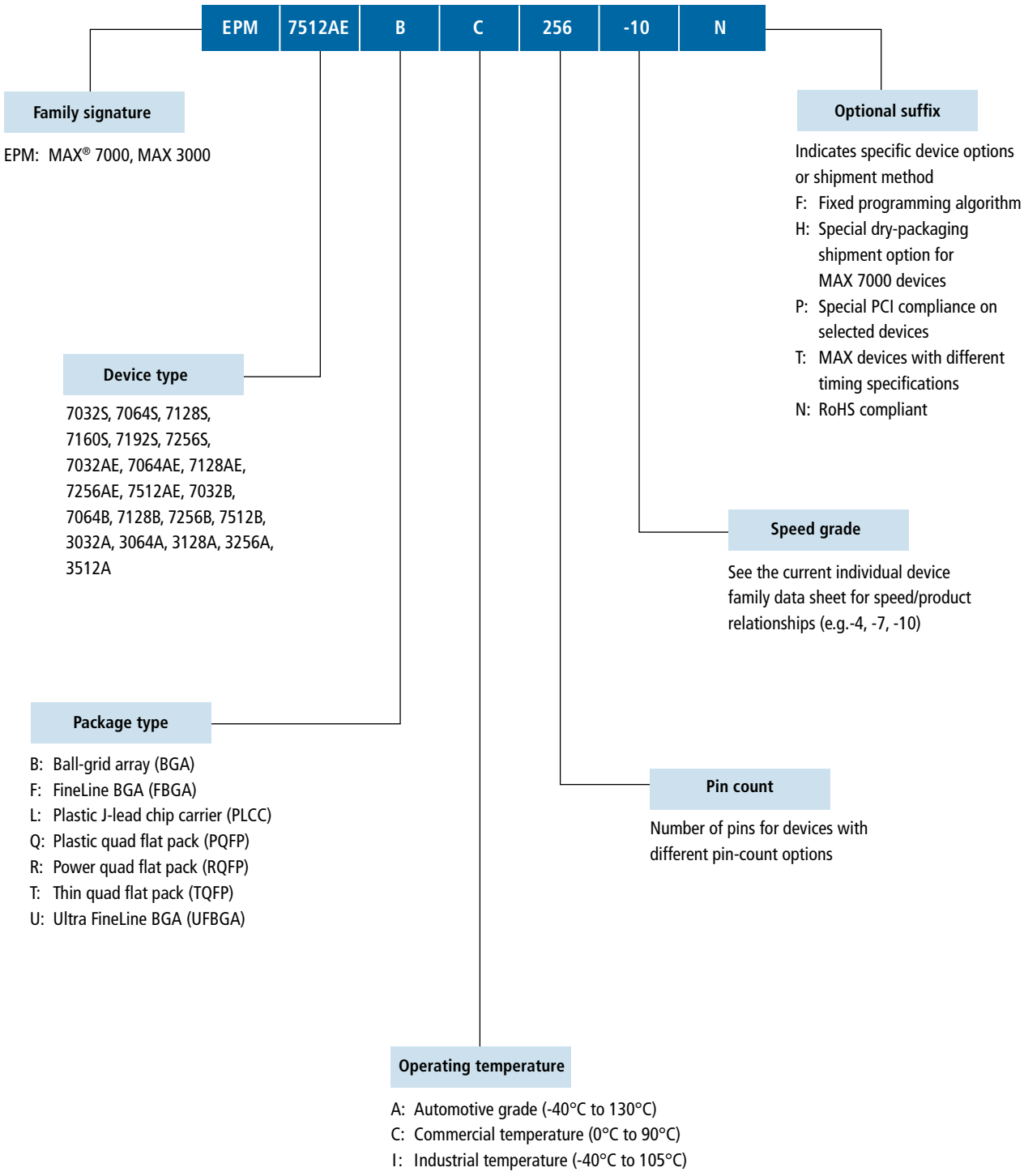
35.00 x 35.00
1.27



35.00 x 35.00
1.27

27.00 x 27.00
1.27

Ordering codes



EP1S	25	F	780	C	5	N

Family signature

EPM: MAX II
EP3C: Cyclone® III
EP2C: Cyclone II
EP1C: Cyclone
EP2AGX: Arria® II GX
EP1AGX: Arria GX
EP4SE: Stratix® IV E
EP4SGX: Stratix IV GX
EP4S: Stratix IV GT
EP3SL: Stratix III L
EP3SE: Stratix III E
EP2S: Stratix II
EP2SGX: Stratix II GX
EP1S: Stratix
EP1SGX: Stratix GX
HC4E: HardCopy® IV E
HC4GX: HardCopy IV GX
HC3: HardCopy III
HC2: HardCopy II
HC1S: HardCopy Stratix

Device type

EPM: 240, 570,1270, 2210
EP3C: 5, 10, 16, 25, 40, 55, 80, 120
EP2C: 5, 8, 8A, 15A, 20, 20A, 35, 50, 70
EP1C: 3, 4, 6,12, 20
EP2AGX: 20, 30, 45, 65, 95, 125, 190, 260
EP1AGX: 20, 35, 50, 60, 90
EP4SE: 110, 230, 290, 360, 530, 680
EP4SGX: 70, 110, 230, 290, 360, 530
EP4S: 40G, 100G
EP3SL: 50, 70, 110, 150, 200, 340
EP3SE: 50, 80, 110, 260
EP2S: 15, 30, 60, 90, 130,180
EP2SGX: 30, 60, 90, 130
EP1S: 10, 20, 25, 30, 40, 60, 80
EP1SGX: 10, 25, 40
HC4E: Consult your sales representative.
HC4GX: Consult your sales representative.
HC3: Consult your sales representative.
HC2: 10W, 10, 20, 30, 40
HC1S: 25, 30, 40, 60, 80

Transceiver channels

For transceiver-based FPGAs (GX) only

C: 4	G: 20
D: 8	H: 24
E: 12	K: 36
F: 16	N: 48

Product-line suffix

For MAX II devices only
Indicates device core voltage
G: 1.8V V_{CCINT} device
Blank: 2.5V or 3.3V V_{CCINT} device

Package type

B: Ball-grid array
E: Enhanced thin quad flat pack
F: FineLine BGA
H: Hybrid FineLine BGA
M: Micro BGA
T: Thin quad flat pack
U: Ultra FineLine BGA
Q: Plastic quad flat pack

Pin count

Number of pins for devices with different pin-count options

Note: Statix IV E, Stratix IV GX, Stratix IV GT, and Arria II GX devices use package size in place of pin counts:

Package type/size:	Package type/pin count:
F29/H29	F780/H780
F35/H35	F1152/H1152
F40/H40	F1517/H1517
F43	F1760
F45	F1932

Operating temperature

A: Automotive grade (-40°C to 125°C)
C: Commercial temperature (0°C to 85°C)
I: Industrial temperature (-40°C to 100°C)

Speed grade

	Fast ← → Slow						
Devices	2	3	4	5	6	7	8
MAX II		✓	✓	✓			
Cyclone III					✓	✓	✓
Cyclone II					✓	✓	✓
Cyclone					✓	✓	✓
Arria II GX		✓	✓	✓			
Arria GX					✓		
Stratix IV E	✓	✓	✓				
Stratix IV GX	✓	✓	✓				
Stratix IV GT	✓	✓					
Stratix III L	✓	✓	✓				
Stratix III E	✓	✓	✓				
Stratix II		✓	✓	✓			
Stratix II GX		✓	✓	✓			
Stratix				✓	✓	✓	
Stratix GX				✓	✓	✓	

Optional suffix

Indicates specific device options or shipment method
ES: Engineering sample
N: RoHS compliant

Product websites and information

- MAX® CPLD series

  MAX II CPLDs
  www.altera.com/max2

  MAX 3000A CPLDs
  www.altera.com/products/devices/max3k

  MAX 7000 CPLDs
  www.altera.com/products/devices/max7k

- Cyclone® low-cost FPGA series

  Cyclone III FPGAs
  www.altera.com/cyclone3

  Cyclone II FPGAs
  www.altera.com/cyclone2

  Cyclone FPGAs
  www.altera.com/cyclone

- Arria® FPGA series

  Arria II FPGAs
  www.altera.com/arria2gx

  Arria FPGAs
  www.altera.com/arriagx

- Stratix® high-end FPGA series

  Stratix IV FPGAs
  www.altera.com/stratix4

  Stratix III FPGAs
  www.altera.com/stratix3

  Stratix II FPGAs
  www.altera.com/stratix2

- HardCopy® ASIC series

  HardCopy ASIC series
  www.altera.com/hardcopy

  HardCopy IV ASICs
  www.altera.com/hardcopy4

  HardCopy III ASICs
  www.altera.com/hardcopy3

  HardCopy II ASICs
  www.altera.com/hardcopy2

- Embedded processing

  Altera® embedded processing
  www.altera.com/embedded

  Nios® II processors
  www.altera.com/nios2

  Nios II development kits
  www.altera.com/nioskits

  Nios II C2H Compiler
  www.altera.com/c2h

  Nios user forum
  www.niosforum.org

  SOPC Builder-ready IP
  www.altera.com/sopcready

- Digital signal processing

  DSP information
  www.altera.com/dsp

- Intellectual property solutions

  Online IP search engine
  www.altera.com/ipmegastore

- Quartus® II design software

  Quartus II software
  www.altera.com/quartus2

  Quartus II Web Edition and Subscription Edition download
  www.altera.com/download

  Purchase Quartus II software
  www.altera.com/buysoftware

- Development kits

  Altera and partner development kits
  www.altera.com/devkits

- Configuration devices

  Configuration handbook
  www.altera.con/confighandbook

  Application note 386
  www.altera.com/parallel

  Application note 478
  www.altera.com/parallelfl

- Training

  Altera technical training
  www.altera.com/training

- Package dimensions

  Altera device packages
  www.altera.com/packages

- Literature

  More details on Altera and partner offerings
  www.altera.com/literature

Have comments about this catalog?
Email us at catalog@altera.com.

Notes

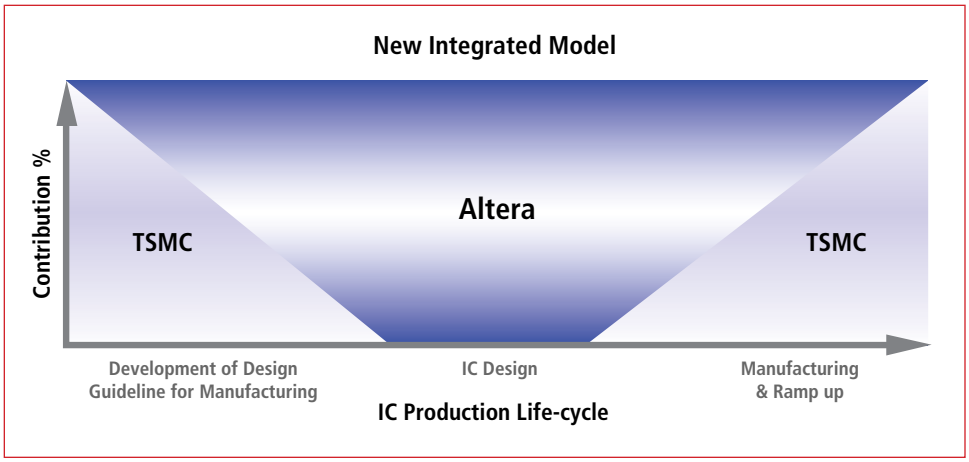
Notes

Notes

Wouldn't you like to design without worry?

Wouldn't it be nice if you could focus on your design performance objectives? Without worrying about cost or power dissipation? And without having to balance early adoption of leading-edge technology against risk?

According to Moore's Law, the more transistors we can fit onto a chip, the greater the performance. TSMC is the only foundry to deliver a 40nm process technology. The goal is to provide advanced technology options that allow designers to differentiate products in today's competitive electronic market places.



Devices fabricated on 40nm process technologies are robust, reliable, and ready for integration into an array of high-end applications. And, you'll find that they meet your power, performance, and cost expectations.

More for less

TSMC's 40G and 40LP processes offer designers up to a 2.35 times raw gate density improvement over the 65nm node. The 40G process is up to 30% faster than TSMC's 65nm GP process at the same leakage, or up to 70% lower leakage at the same speed. In addition, it provides up to 45% lower active power than the 65GP process. The 40LP process provides up to 46% lower leakage and up to 50% lower active power than TSMC's 65LP at the same speed. It also features the smallest SRAM cell size, 0.242 μm^2, and macro size in production today.

The 40nm node features strained silicon, nickel silicide, and copper interconnects. To achieve high-quality yields, we're implementing a combination of 193nm immersion photolithography and extreme low-k (ELK) materials.

Redefining the foundry model

Our longtime partnership with Altera also contributes to our success. From design through tape out, together we're constantly refining the manufacturing process, resulting in chips that are rolled out successfully from node to node.

What's more, we're also redefining the foundry model. Traditionally, foundries and their IC customers worked in their respective areas—manufacturing process development and IC design—somewhat autonomously. This resulted in longer time-to-market and higher costs. Through a new integrated model, TSMC and Altera engineers collaborate on both manufacturing process development and IC design to achieve better and faster results that ultimately benefit you.

TSMC often qualifies its manufacturing process with Altera test chips. Test chips address design issues upfront while validating circuit design and process characteristics. For Altera, a faster manufacturing ramp means a faster production cycle for their devices.

Winning through close collaboration

To fully leverage today's 40nm advanced process, you need a foundry with the proven experience to make you a winner. TSMC's deep, broad collaboration with Altera assures your success from start to finish.

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku I Tower 32F
6-5-1, Nishi Shinjuku
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
www.altera.co.jp

Altera International Ltd.
Unit 11- 18, 9/F
Millennium City 1, Tower 1
388 Kwun Tong Road
Kwun Tong
Kowloon, Hong Kong
Telephone: (852) 2 945 7000
www.altera.com.cn

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