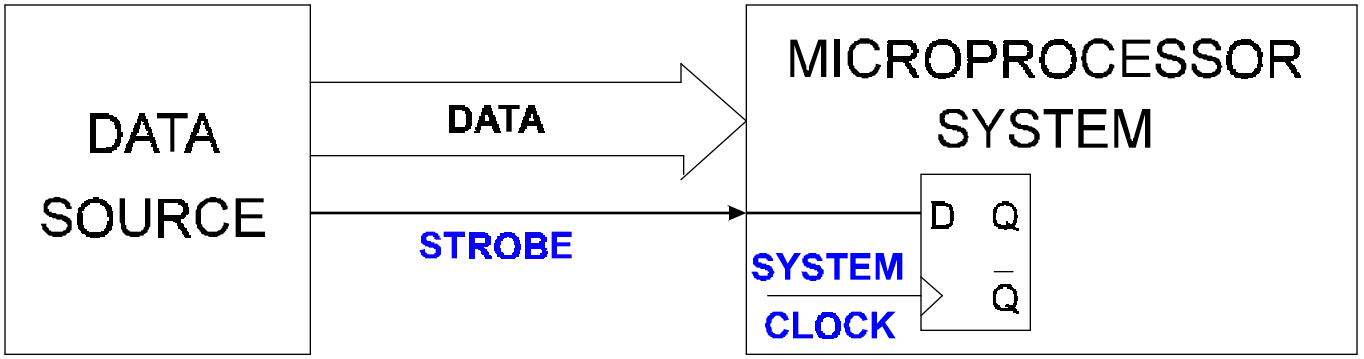
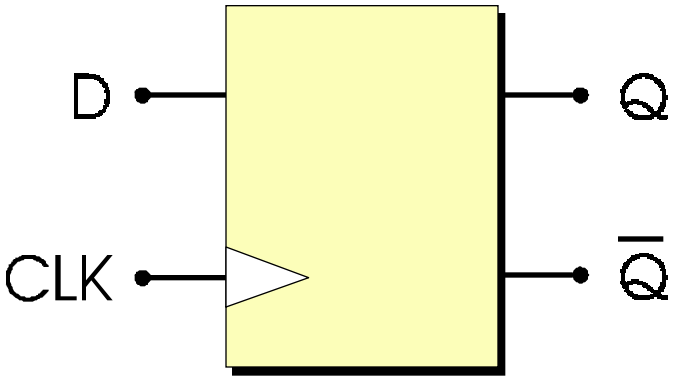
Metastability

The Synchronization Problem



- ★ **Microprocessors are synchronous systems.**
- ★ **Data sources (peripheral devices, memories, etc.) provide data mostly asynchronously with respect to the microprocessor.**
- ★ **Therefore the control signals of the data source have to be synchronized to the system clock.**
- ★ **In synchronization circuits the timing requirements of flip-flops (t_{su}, t_h) are violated.**

Metastable Behaviour

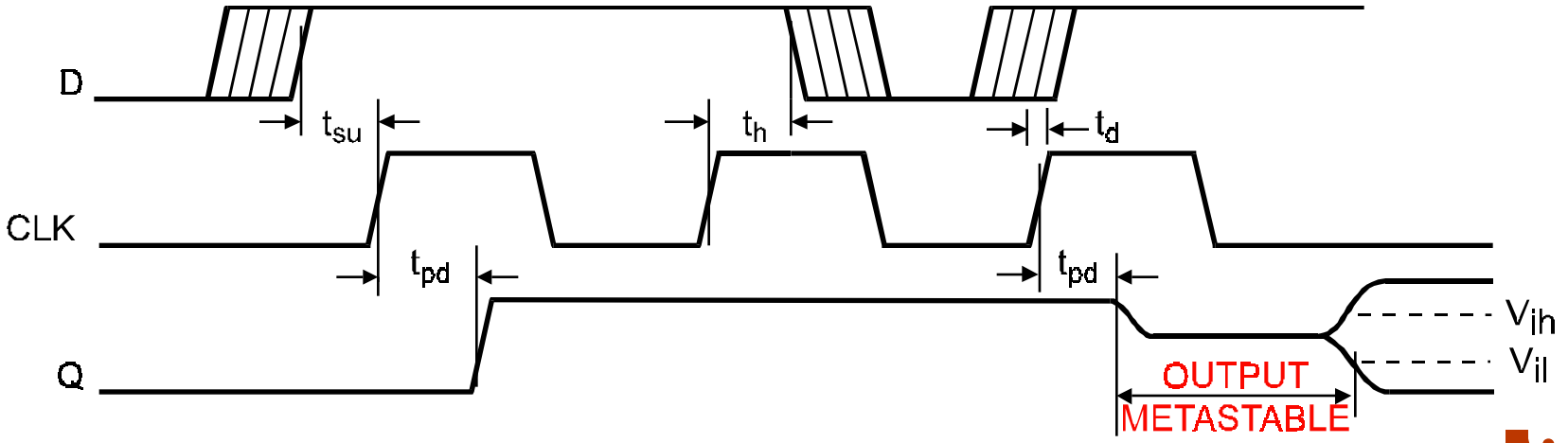


Critical time window td = 10... 150 ps

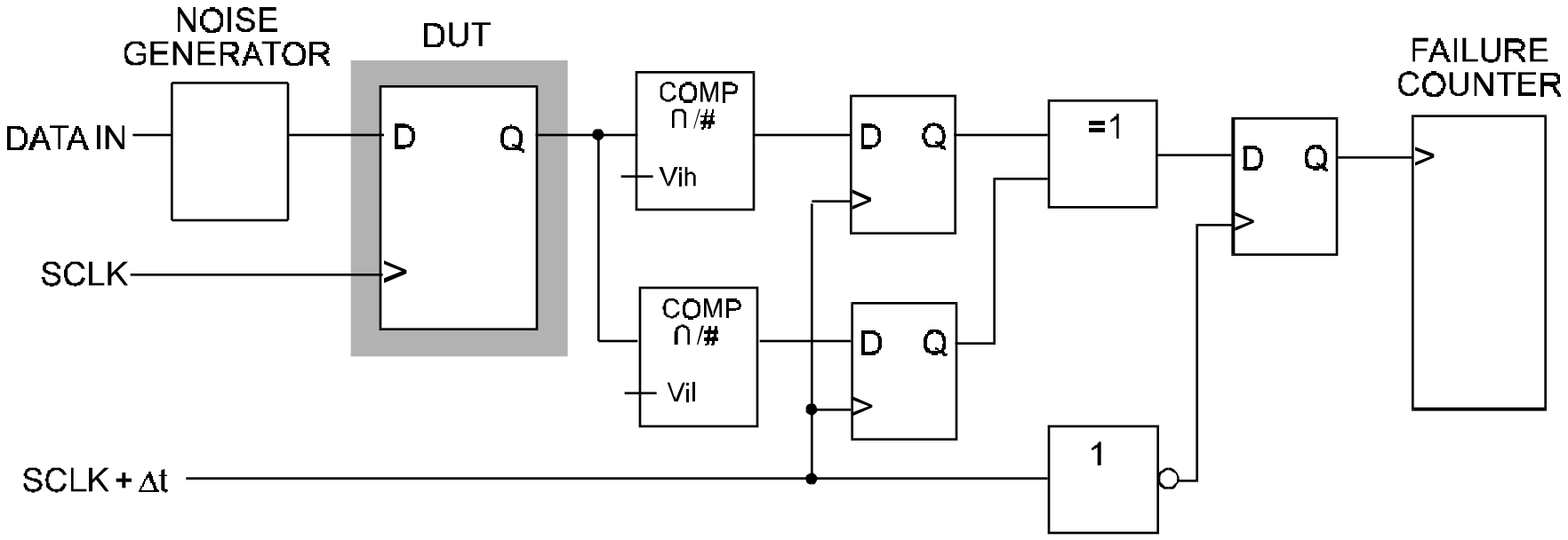
$$\text{MTBF} = \frac{1}{f_{in} \times f_{CLK} \times t_d}$$

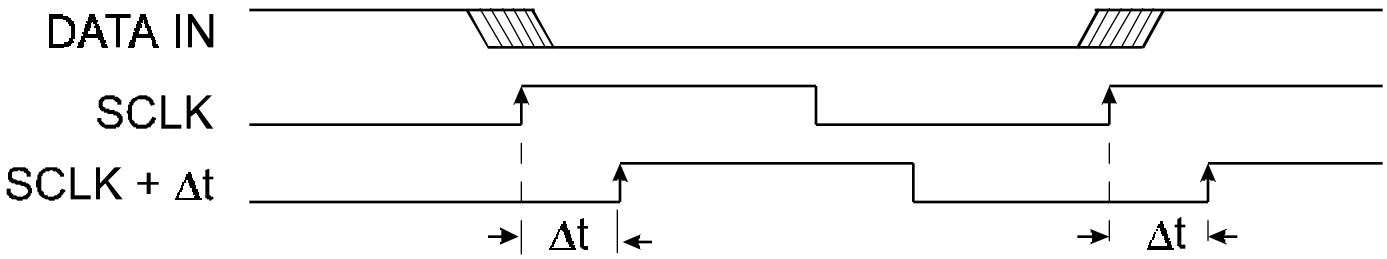
Example:

$$\text{MTBF} = \frac{1}{1\ \text{kHz} \times 1\ \text{MHz} \times 30\ \text{ps}} = 33.3\ \text{s}$$



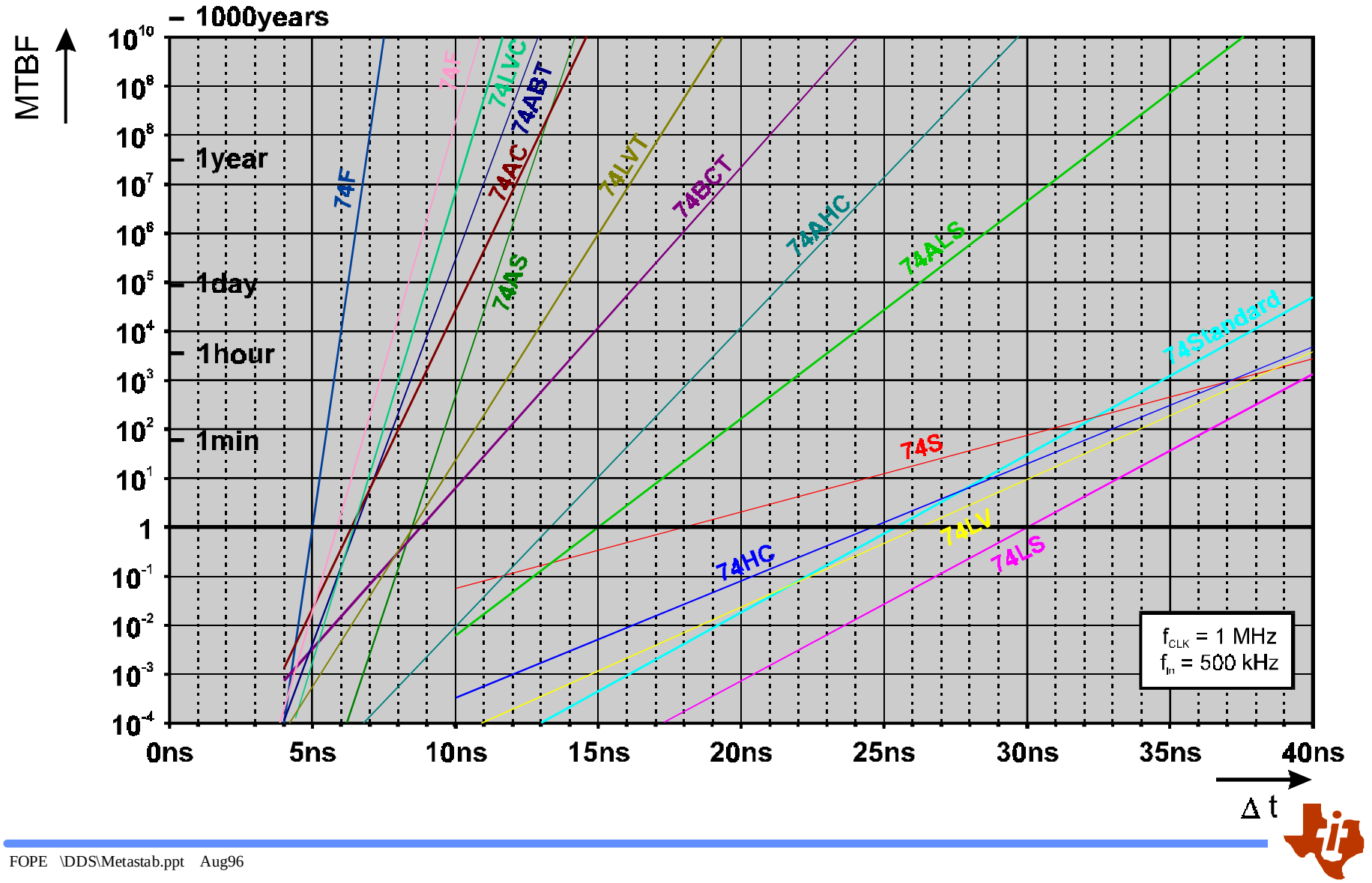
Metastable Evaluation Test Circuit





$$\text{MTBF} = \frac{\text{TIME (SEC)}}{\#\text{FAILURES}}$$

Metastable Characteristics of Logic Families



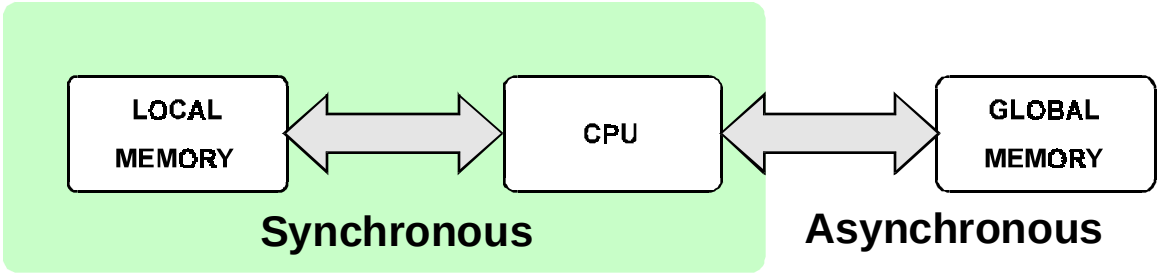
Mean Time between Failures of a Synchronizer

$$MTBF = \frac{\exp(T \times \Delta t)}{f_{in} \times f_{CLK} \times T_O}$$

- ★ There is no way to avoid metastable states in synchronization circuits.
- ★ Fast Logic Circuits return quicker from a metastable to a stable state.
- ★ The probability of system failures is greatly reduced by a delayed test of the synchronization circuit.

	$T\ [ns^{-1}]$	$T_o\ [s]$
74STD	0,74	2,9E-4
74LS	0.72	4.8E-3
74S	0.36	1.3E-9
74ALS	1.02	8.8E-6
74AS	4.03	1.4E3
74F	9.20	1.9E8
74BCT	1.51	1.14E-6
47ABT	3.61	0.033
74HC	0.55	1.48E-6
74AHC	1.41	2.9E-4
74AC	2.80	1.1E-4
74LV	0.60	1.38E-5
74LVC	4.40	4.008
74ALVC	4.60	1.047
74LVT	2.13	1.52E-4

Calculation of System Reliability



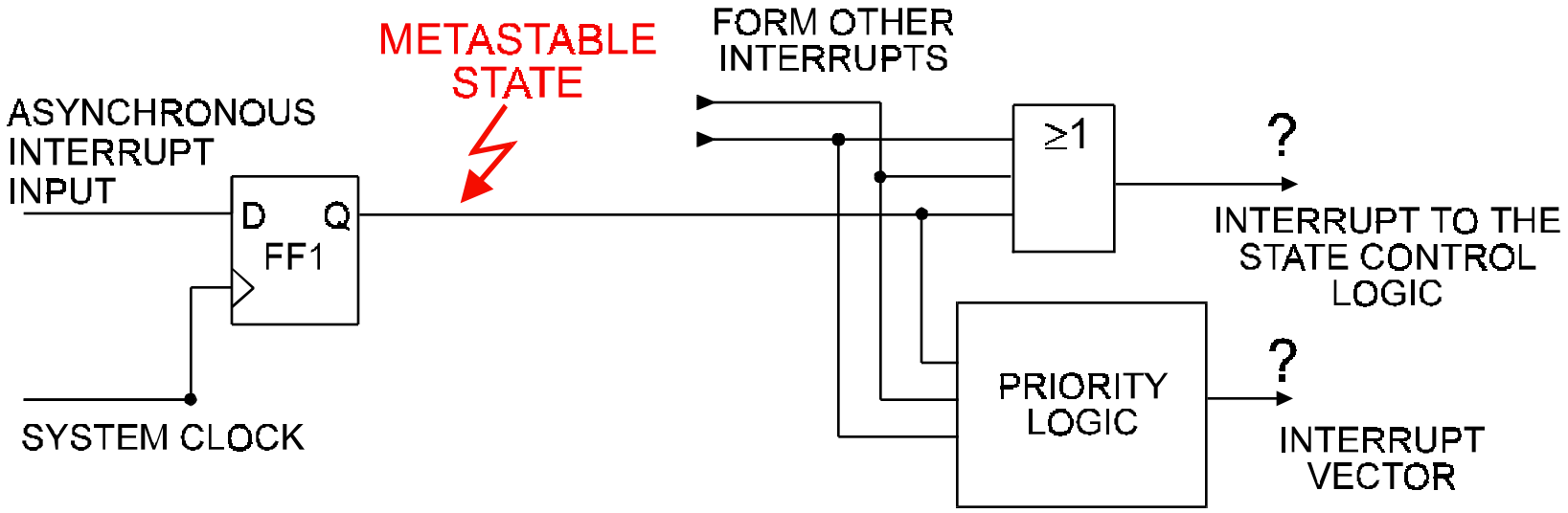
Assumptions:	System clock rate	10 MHz
	Average access rate to the global memory	100 kHz
	Logic family	SN74ALS
Required:	Mean time between failure	> 100 years

$$\textbf{100 years} = 3.2 \times 10^9 \text{ s} = \frac{\exp(1.02 \times \Delta t)}{100 \text{ kHz} \times 10 \text{ MHz} \times 8.8 \times 10^{-6}}$$

$$\Delta t = 37 \text{ ns}$$

To meet the required system reliability, the test of the synchronization circuit output signal has to be delayed by 37 ns.

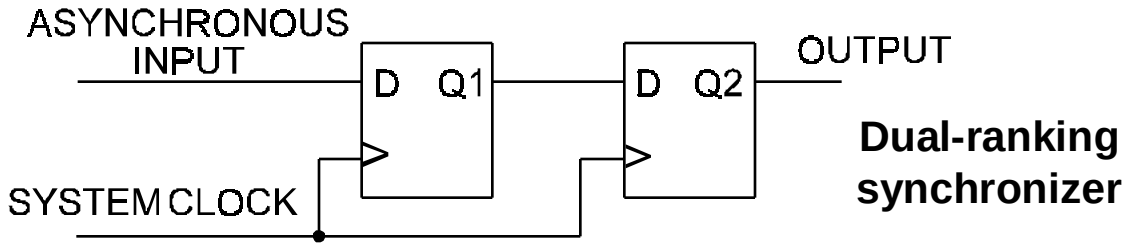
Example for Synchronization Failure

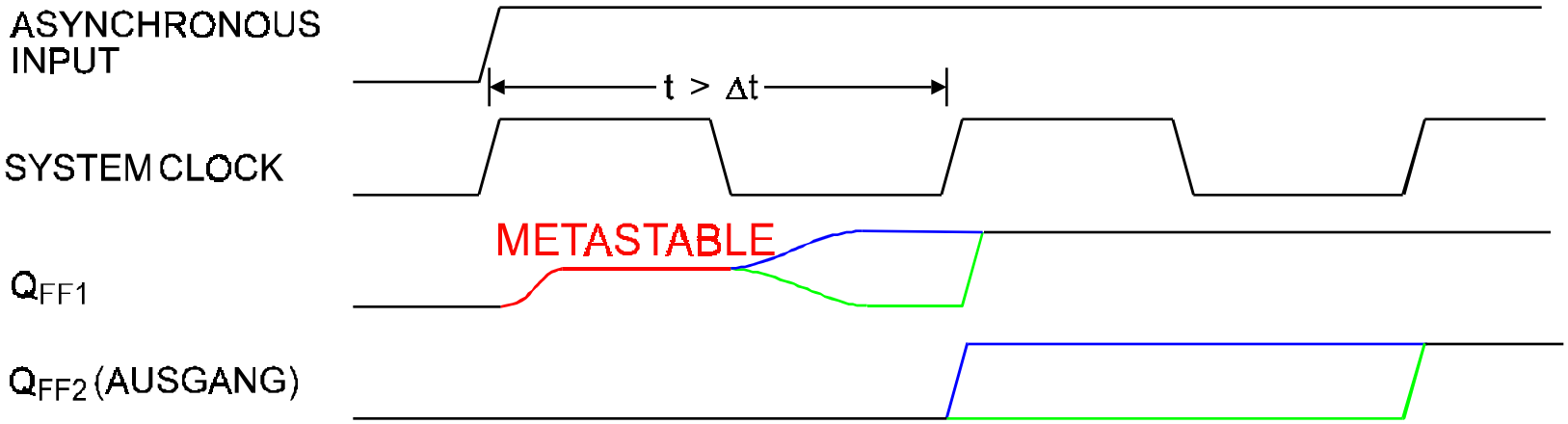


Possible failure :

Due to an undefined logic level caused by a metastable state at the output of the synchronization flip-flop, the OR gate forces an interrupt to the state control logic, while the priority logic provides a wrong interrupt vector.

Metastable-hardened Synchronization Circuit





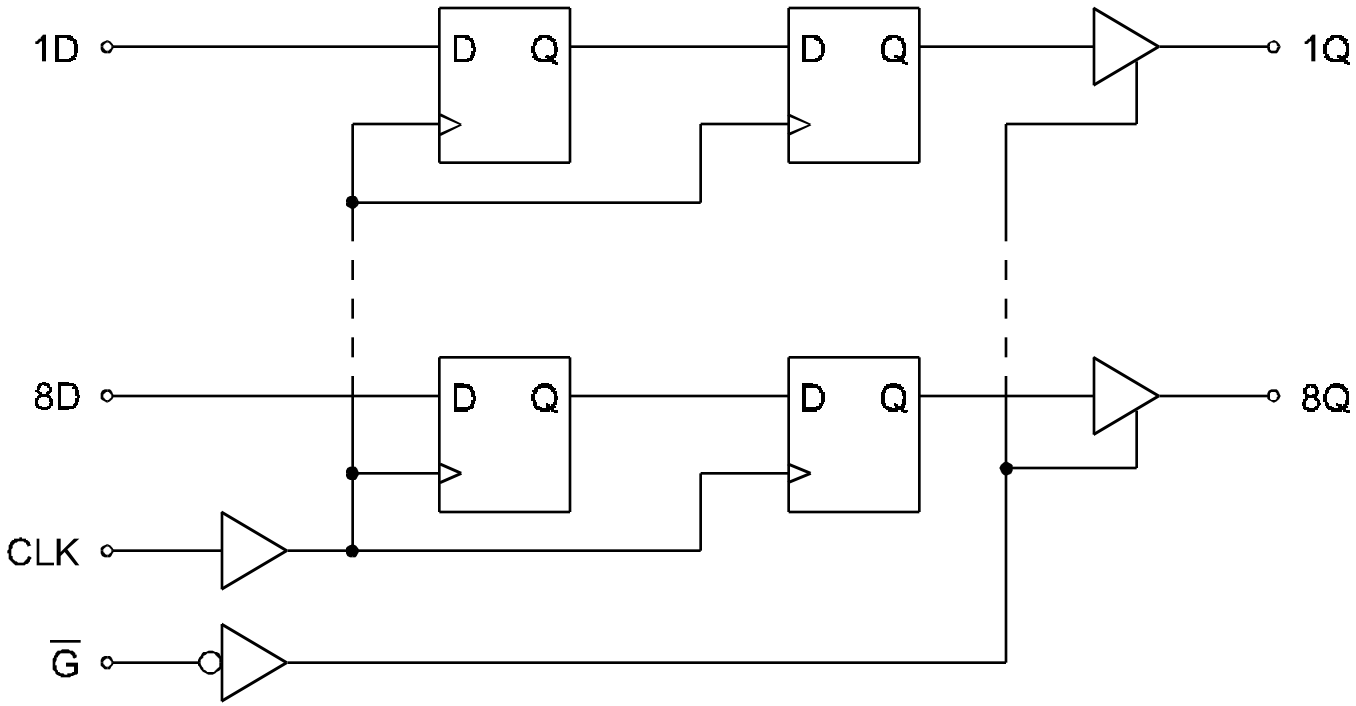
The output of a dual-rank synchronizer provides a defined (but not necessarily correct) logic level, if

$$t \geq \Delta t$$

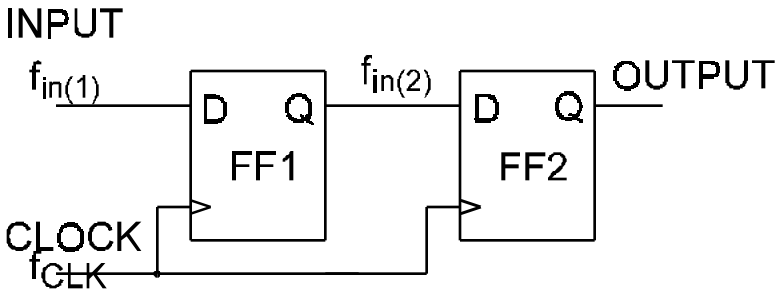
Note: The output signal response is delayed by one clock period.

Circuits for Synchronizer Applications

Improved system reliability due to dual-rank synchronizer SN74AS4374



Mean Time between Failure of a Dual-rank Synchronizer



$$MTBF(2) = \frac{\exp(T \times t)}{f_{CLK} \times f_{in(2)} \times T_o}$$

$$f_{in(2)} = \frac{1}{MTBF(1)}$$

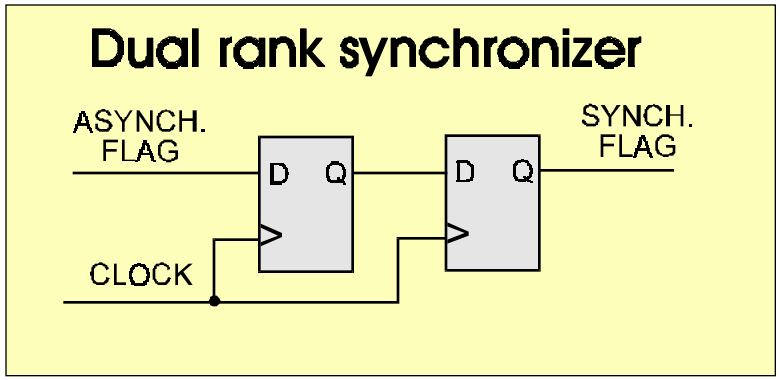
$$= \frac{f_{CLK} \times f_{in(1)} \times To}{\exp(T \times 1 / f_{CLK})}$$

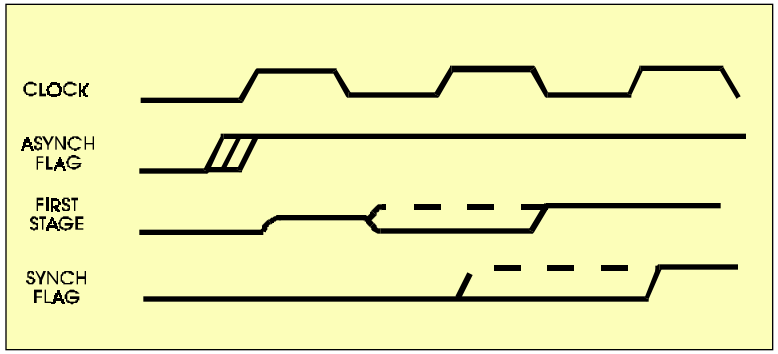
$$MTBF(2) = \frac{\exp(T \times t) \times \exp(T \times 1 / f_{CLK})}{f_{CLK}^2 \times f_{in}(1) \times T_o^2}$$

Note: The flip-flop (2) will only fall into a metastable state, if the output of flip-flop (1) violates the timing requirements at the input of flip-flop (2)

Reliability of Clocked FIFOs

Multi-Stage Flag Synchronization reduces the Probability of Metastable States





Second flip-flop stage filters metastable events from first stage, increasing the MTBF by several orders of magnitude.