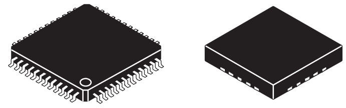


Burr-Brown Products from Texas Instruments

ADS7881

SLAS400B − SEPTEMBER 2003 − REVISED NOVEMBER 2005

12-BIT, 4-MSPS LOW POWER SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 4 MHz Sample Rate, 12-Bit Resolution
- Zero Latency
- Unipolar, Pseudo Differential Input, Range:
  - 0 V to 2.5 V
- High Speed Parallel Interface
- 71 dB SNR and −88.5 dB THD at 1 MHz I/P
- Power Dissipation 95 mW at 4 MSPS
- Nap Mode (10 mW Power Dissipation)
- Power Down (10 μW)
- Internal Reference
- Internal Reference Buffer
- 48-Pin TQFP and QFN Packages

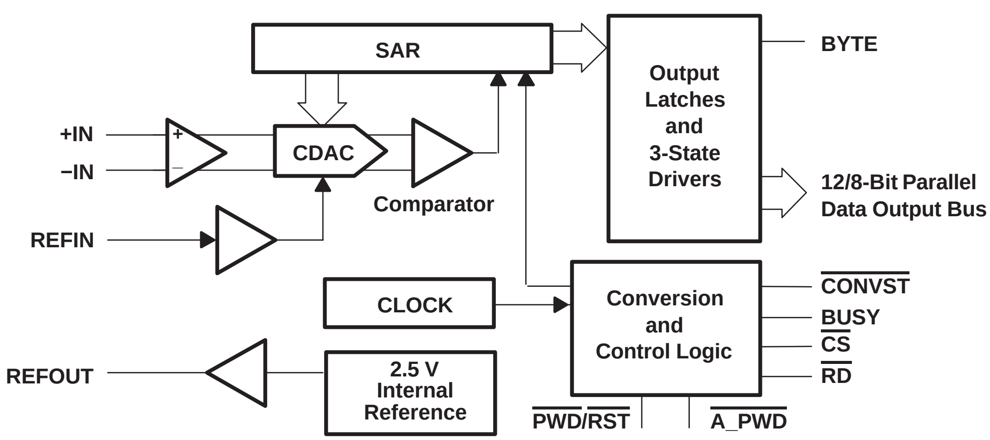
APPLICATIONS

- Optical Networking (DWDM, MEMS Based Switching)
- Spectrum Analyzers
- High Speed Data Acquisition Systems
- High Speed Close-Loop Systems
- Telecommunication
- Ultra-Sound Detection

DESCRIPTION

The ADS7881 is a 12-bit 4-MSPS A-to-D converter with 2.5-V internal reference. The device includes a capacitor based SAR A/D converter with inherent sample and hold. The device offers a 12-bit parallel interface with an additional byte mode that provides easy interface with 8-bit processors. The device has a pseudo-differential input stage.

The −IN swing of ±200 mV is useful to compensate for ground voltage mismatch between the ADC and sensor and also to cancel common-mode noise. With nap mode enabled, the device operates at lower power when used at lower conversion rates. The device is available in 48-pin TQFP and QFN packages.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS7881	±1	±1	12	48-Pin TQFP	PFB	−40°C to 85°C	ADS7881IPFBT	Tape and reel 250
							ADS7881IPFBR	Tape and reel 1000
	±1	±1	12	48-Pin QFN	RGZ	−40°C to 85°C	ADS7881IRGZT	Tape and reel 250
							ADS7881IRGZR	Tape and reel 2500

NOTE: For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range(1)

		UNIT
+IN to AGND		−0.3 V to +VA + 0.1 V
−IN to AGND		−0.3 V to 0.5 V
+VA to AGND		−0.3 V to 7 V
+VBD to BDGND		−0.3 V to 7 V
Digital input voltage to GND		−0.3 V to (+VBD + 0.3 V)
Digital output to GND		−0.3 V to (+VBD + 0.3 V)
Operating temperature range		−40°C to 85°C
Storage temperature range		−65°C to 150°C
Junction temperature ($T_J$max)		150°C
TQFP and QFN packages	Power dissipation	(T_J Max–T_A)/ θ_{JA}
	θ_{JA} Thermal impedance	86°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = −40°C to 85°C, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 2.5 V, f_{sample} = 4 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span(1)	+IN – (−IN)	0		V_{ref}	V
Absolute input range	+IN	−0.2		V_{ref} + 0.2	V
	−IN	−0.2		+0.2	
Input capacitance			27		pF
Input leakage current			500		pA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No missing codes		12			Bits
Integral linearity(2)		−1	±0.6	1	LSB(3)
Differential linearity		−1	±0.6	1	LSB(3)
Offset error(4)	External reference	−1.5	±0.25	1.5	mV
Gain error(4)	External reference	−2	±0.75	2	mV
Common-mode rejection ratio	With common mode input signal = 200 mVp−p at 1 MHz		60		dB
Power supply rejection	At FF0$_H$ output code, +VA = 4.75 V to 5.25 V , Vref = 2.50 V		80		dB
SAMPLING DYNAMICS					
Conversion time	+VDB = 5 V		185	200	nsec
	+VDB = 3 V			205	nsec
Acquisition time	+VDB = 5 V	50	65		nsec
	+VDB = 3 V	45			nsec
Maximum throughput rate				4	MHz
Aperture delay			2		nsec
Aperture jitter			20		psec
Step response			50		nsec
Over voltage recovery			50		nsec
DYNAMIC CHARACTERISTICS					
Total harmonic distortion(5)	V_{IN} = 2.496 Vp−p at 100 kHz/2.5 Vref		−91		dB
	V_{IN} = 2.496 Vp−p at 1 MHz/2.5 Vref		−88.5	−86	
	V_{IN} = 2.496 Vp−p at 1.8 MHz/2.5 Vref		74		
SNR	V_{IN} = 2.496 Vp−p at 100 kHz/2.5 Vref		71.5		dB
	V_{IN} = 2.496 Vp−p at 1 MHz/2.5 Vref	69	71		
	V_{IN} = 2.496 Vp−p at 1.8 MHz/2.5 Vref		69.7		
SINAD	V_{IN} = 2.496 Vp−p at 100 kHz/2.5 Vref		71.5		dB
	V_{IN} = 2.496 Vp−p at 1 MHz/2.5 Vref	69	71		
	V_{IN} = 2.496 Vp−p at 1.8 MHz/2.5 Vref		68.3		
SFDR	V_{IN} = 2.496 Vp−p at 1 MHz/2.5 Vref		90		dB
−3 dB Small signal bandwidth			50		MHz
EXTERNAL REFERENCE INPUT					
Input V_{REF} range		2.4	2.5	2.6	V
Resistance(6)	To internal reference voltage		500		kΩ

SPECIFICATIONS Continued

T_A = −40°C to 85°C, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 2.5 V, f_{sample} = 4 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE OUTPUT						
Start-up time		From 95% (+VA), with 1-µF storage capacitor on REFOUT to AGND			120	msec
V_{REF} Range		IOUT=0	2.47	2.5	2.53	V
Source current		Static load			10	µA
Line regulation		+VA = 4.75 V to 5.25 V		1		mV
Drift		IOUT = 0		25		PPM/C
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		
Logic level	V_{IH}	I_{IH} = 5 µA	$+V_{BD}$ −1		$+V_{BD}$ + 0.3	V
	V_{IL}	I_{IL} = 5 µA	−0.3		0.8	V
	V_{OH}	I_{OH} = 2 TTL loads	$+V_{BD}$ − 0.6		$+V_{BD}$	V
	V_{OL}	I_{OL} = 2 TTL loads	0		0.4	V
Data format				Straight Binary		
POWER SUPPLY REQUIREMENTS						
Power supply voltage	+VBD		2.7	3.3	5.25	V
	+VA		4.75	5	5.25	V
Supply current, +VA, 4 MHz sample rate				19	22	mA
Power dissipation, 4 MHz sample rate		+VA = 5 V		95	110	mW
NAP MODE						
Supply current, +VA				2	3	mA
Power-up time(7)				60		nsec
POWER DOWN						
Supply current, +VA				2	2.5	µA
Power down time(8)		From simulation results		10		µsec
Power up time		1-µF Storage capacitor on REFOUT to AGND		25		msec
Invalid conversions after power up or reset				4		Numbers
TEMPERATURE RANGE						
Operating free-air			−40		85	°C

(1) Ideal input span; does not include gain or offset error.
(2) This is endpoint INL, not best fit.
(3) LSB means least significant bit.
(4) Measured relative to actual measured reference.
(5) Calculated on the first nine harmonics of the input frequency.
(6) Can vary ±20%.
(7) Minimum acquisition time for first sampling after the end of nap state must be 60 nsec more than normal.
(8) Time required to reach level of 2.5 µA.

TIMING REQUIREMENTS

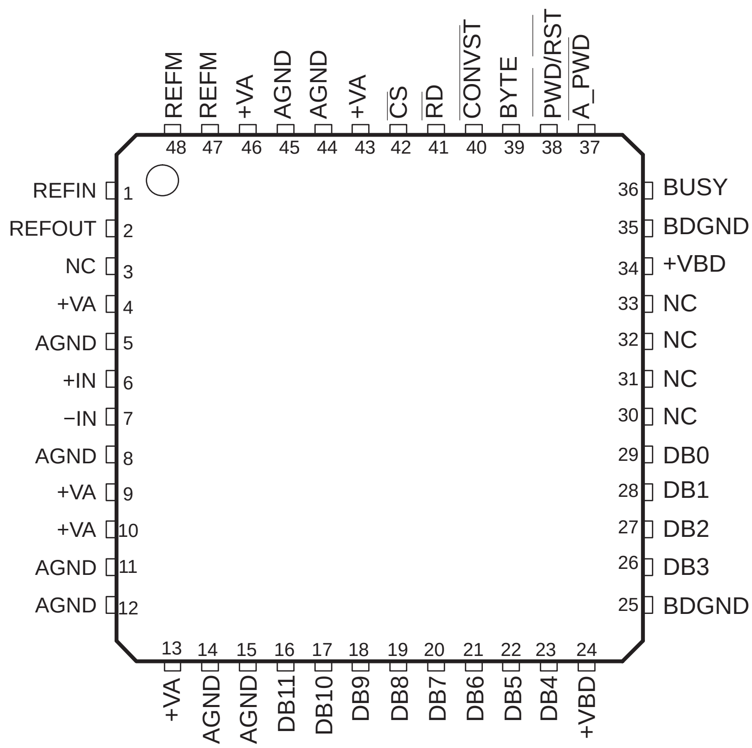
All specifications typical at −40°C to 85°C, +VA = +5 V, +VBD = +5 V (see Notes 1, 2, 3, and 4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	REF FIG.
Conversion time	$t_{(conv)}$		185	200	ns	5
Acquisition time	$t_{(acq)}$	50	65		ns	5
SAMPLING AND CONVERSION START						
Hold time $\overline{CS}$ low to $\overline{CONVST}$ high (with BUSY high)	t_{h1}	10			ns	3
Delay $\overline{CONVST}$ high to acquisition start	t_{d1}	2	4	5	ns	1
Hold time, $\overline{CONVST}$ high to $\overline{CS}$ high with BUSY low	t_{h2}	10			ns	1
Hold time, $\overline{CONVST}$ low to $\overline{CS}$ high	t_{h3}	10			ns	1
Delay $\overline{CONVST}$ low to BUSY high	t_{d2}			40	ns	1
$\overline{CS}$ width for acquisition or conversion to start	t_{w3}	20			ns	2
Delay $\overline{CS}$ low to acquisition start with $\overline{CONVST}$ high	t_{d3}	2	4	5	ns	2
Pulse width, from $\overline{CS}$ low to $\overline{CONVST}$ low for acquisition to start	t_{w1}	20			ns	2
Delay $\overline{CS}$ low to BUSY high with $\overline{CONVST}$ low	t_{d4}			40	ns	2
Quiet sampling time(3)		25			ns	
CONVERSION ABORT						
Setup time $\overline{CONVST}$ high to $\overline{CS}$ low with BUSY high	t_{s1}			15	ns	4
Delay time $\overline{CS}$ low to BUSY low with $\overline{CONVST}$ high	t_{d5}			20	ns	4
DATA READ						
Delay $\overline{RD}$ low to data valid with $\overline{CS}$ low	t_{d6}			25	ns	5
Delay BYTE high to LSB word valid with $\overline{CS}$ and $\overline{RD}$ low	t_{d7}			25	ns	5
Delay time $\overline{RD}$ high to data 3-state with $\overline{CS}$ low	t_{d9}			25	ns	5
Delay time end of conversion to BUSY low	t_{d11}			20	ns	5
Quiet sampling time $\overline{RD}$ high to $\overline{CONVST}$ low	t_1			25	ns	5
Delay $\overline{CS}$ low to data valid with $\overline{RD}$ low	t_{d8}			25	ns	6
Delay $\overline{CS}$ high to data 3-state with $\overline{RD}$ low	t_{d10}			25	ns	6
Quiet sampling time $\overline{CS}$ low to $\overline{CONVST}$ low	t_2			25	ns	6
BACK-TO-BACK CONVERSION						
Delay BUSY low to data valid	t_{d12}			10	ns	7, 8
Pulse width, $\overline{CONVST}$ high	t_{w4}	60			ns	7, 8
Pulse width, $\overline{CONVST}$ low	t_{w5}	20			ns	7
POWER DOWN/RESET						
Pulse width, low for $\overline{PWD}/\overline{RST}$ to reset the device	t_{w6}	45		6140	ns	10
Pulse width, low for $\overline{PWD}/\overline{RST}$ to power down the device	t_{w7}	7200			ns	9
Delay time, power up after $\overline{PWD}/\overline{RST}$ is high	t_{d13}			25	ms	9

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagram.
(3) Quiet period before conversion start, no data bus activity including data bus 3-state is allowed in this period.
(4) All timings are measured with 20 pF equivalent loads on all data bits and BUSY pin.

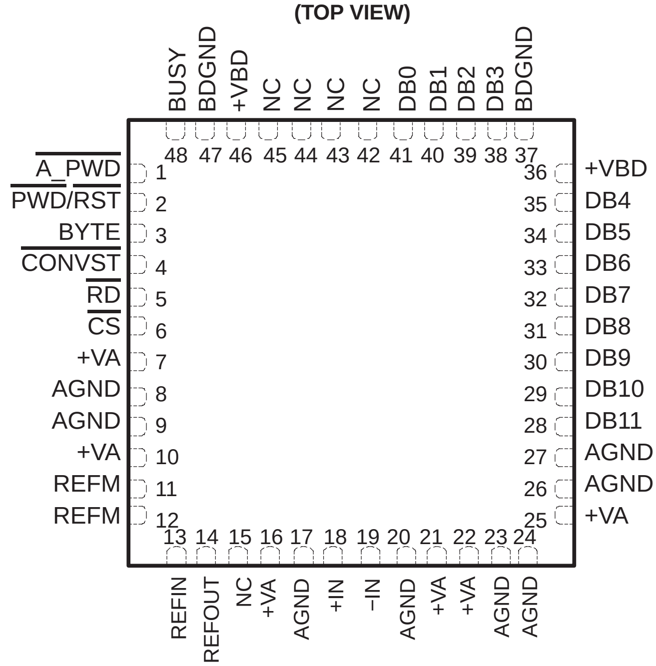
PIN ASSIGNMENTS

PFB PACKAGE
(TOP VIEW)



NC − No connection

RGZ PACKAGE
(TOP VIEW)



NC − No internal connection

NOTE: The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TERMINAL FUNCTIONS

NAME	NO. PFB	NO. RGZ	I/O	DESCRIPTION		
DATA BUS				8-Bit Bus		16-Bit Bus
				BYTE = 0	BYTE = 1	BYTE = 0
DB11	16	28	O	D11 (MSB)	D3	D11 (MSB)
DB10	17	29	O	D10	D2	D10
DB9	18	30	O	D9	D1	D9
DB8	19	31	O	D8	D0 (LSB)	D8
DB7	20	32	O	D7	0	D7
DB6	21	33	O	D6	0	D6
DB5	22	34	O	D5	0	D5
DB4	23	35	O	D4	0	D4
DB3	26	38	O	D3	0	D3
DB2	27	39	O	D2	0	D2
DB1	28	40	O	D1	0	D1
DB0	29	41	O	D0 (LSB)	0	D0 (LSB)
CONTROL PINS						
$\overline{\text{CS}}$	42	6	I	Chip select. Active low signal enables chip operation like acquisition start, conversion start, bus release from 3-state. Refer to the timing diagrams for more details.		
$\overline{\text{CONVST}}$	40	4	I	Conversion start. The rising edge starts the acquisition. The falling edge of this input ends the acquisition and starts the conversion. Refer to the timing diagrams for more details.		
$\overline{\text{RD}}$	41	5	I	Active low synchronization pulse for the parallel output. When $\overline{\text{CS}}$ is low, this serves as the output enable and puts the previous conversion results on the bus.		
$\overline{\text{A\_PWD}}$	37	1	I	Nap mode enable, active low		
$\overline{\text{PWD}}$/$\overline{\text{RST}}$	38	2	I	Active low input, acts as device power down/device reset signal.		
BYTE	39	3	I	Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Lower byte D[3:0] is folded back to high byte so D3 is available in D11 place.		
STATUS OUTPUT						
BUSY	36	48	O	Status output. High when a conversion is in progress.		
POWER SUPPLY						
+VBD	24, 34	36, 46	−	Digital power supply for all digital inputs and outputs. Refer to Table 3 for layout guidelines.		
BDGND	25, 35	37, 47	−	Digital ground for all digital inputs and outputs. Short to analog ground plane below the device.		
+VA	4, 9, 10, 13, 43, 46	7, 10, 16, 21, 22, 25	−	Analog power supplies. Refer to Table 3 for layout guidelines.		
AGND	5, 8, 11, 12, 14, 15, 44, 45	8, 9, 17, 20, 23, 24, 26, 27	−	Analog ground pins. Short to analog ground plane below the device.		
ANALOG INPUT						
+IN	6	18	I	Noninverting analog input channel		
−IN	7	19	I	Inverting analog input channel		
REFIN	1	13	I	Reference (positive) input. Needs to be decoupled with REFM pin using 0.1-µF bypass capacitor and 1-µF storage capacitor.		
REFOUT	2	14	O	Internal reference output. To be shorted to REFIN pin when internal reference is used. Do not connect to REFIN pin when external reference is used. Always needs to be decoupled with AGND using 0.1-µF bypass capacitor.		
REFM	47, 48	11, 12	I	Reference ground. Connect to analog ground plane.		
NC	3, 30, 31, 32, 33	15, 42, 43, 44, 45	−	No connection		

DESCRIPTION AND TIMING DIAGRAMS

SAMPLING AND CONVERSION START

There are three ways to start sampling. The rising edge of $\overline{\text{CONVST}}$ starts sampling with $\overline{\text{CS}}$ and BUSY being low (see Figure 1) or it can be started with the falling edge of $\overline{\text{CS}}$ when $\overline{\text{CONVST}}$ is high and BUSY is low (see Figure 2). Sampling can also be started with an internal conversion end (before BUSY falling edge) with $\overline{\text{CS}}$ being low and $\overline{\text{CONVST}}$ high before an internal conversion end (see Figure 3). Also refer to the section DEVICE OPERATION AND DATA READ IN BACK-TO-BACK CONVERSION for more details.

A conversion can be started two ways (a conversion start is the end of sampling). Either with the falling edge of $\overline{\text{CONVST}}$ when $\overline{\text{CS}}$ is low (see Figure 1) or the falling edge of $\overline{\text{CS}}$ when $\overline{\text{CONVST}}$ is low (see Figure 2). A clean and low jitter falling edge of these respective signals triggers a conversion start and is important to the performance of the converter. The BUSY pin is brought high immediately following the $\overline{\text{CONVST}}$ falling edge. BUSY stays high throughout the conversion process and returns low when the conversion has ended.

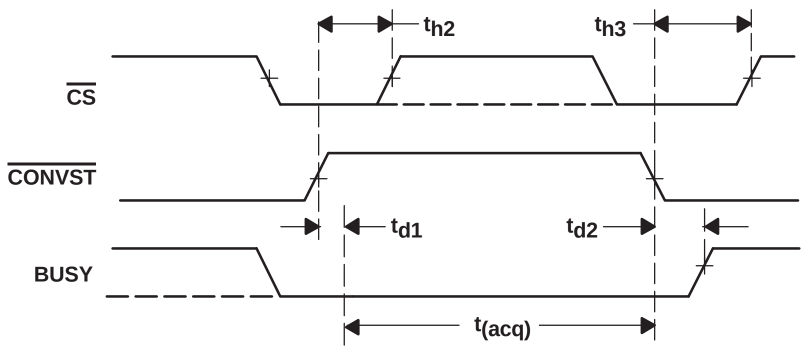


Figure 1. Sampling and Conversion Start Control With $\overline{\text{CONVST}}$ Pin

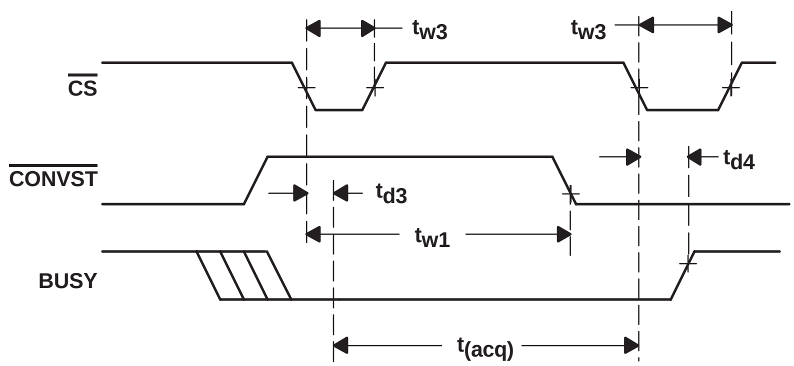


Figure 2. Sampling and Conversion Start Control With $\overline{\text{CS}}$ Pin

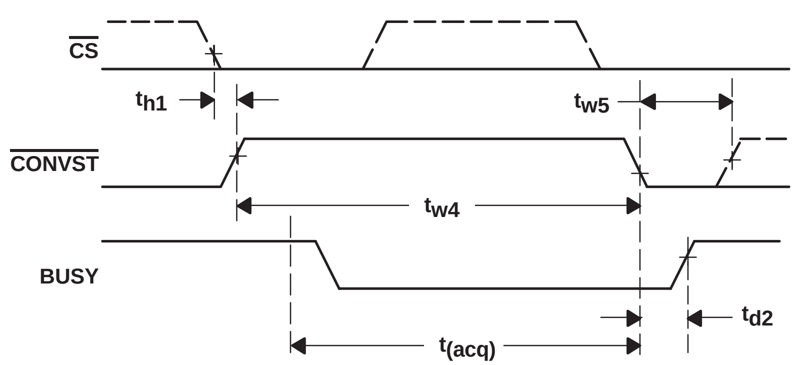


Figure 3. Sampling Start With $\overline{\text{CS}}$ Low and $\overline{\text{CONVST}}$ High (Back-to-Back)

CONVERSION ABORT

The falling edge of $\overline{\text{CS}}$ aborts the conversion while BUSY is high and $\overline{\text{CONVST}}$ is high (see Figure 4). The device outputs FE0 (hex) to indicate a conversion abort.

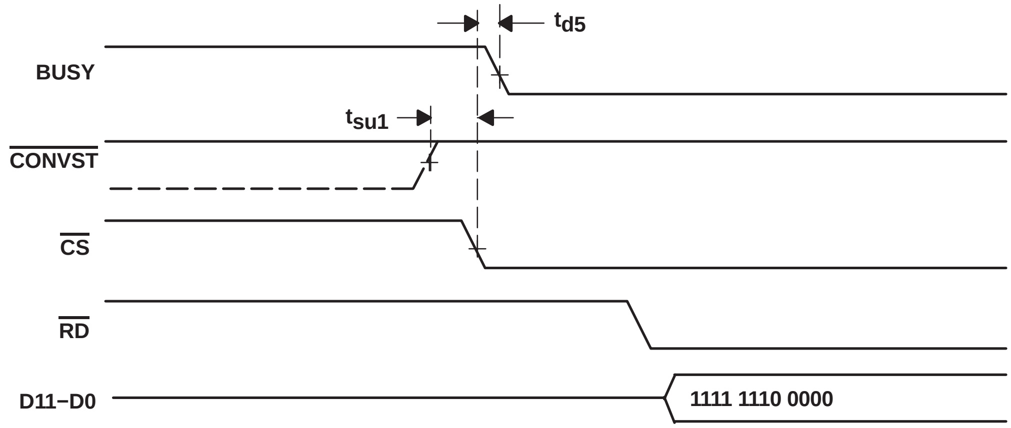


Figure 4. Conversion Abort

DATA READ

Two conditions need to be satisfied for a read operation. Data appears on the D11 through D0 pins (with D11 MSB) when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Figure 5 and Figure 6 illustrate the device read operation. The bus is three-stated if any one of the signals is high.

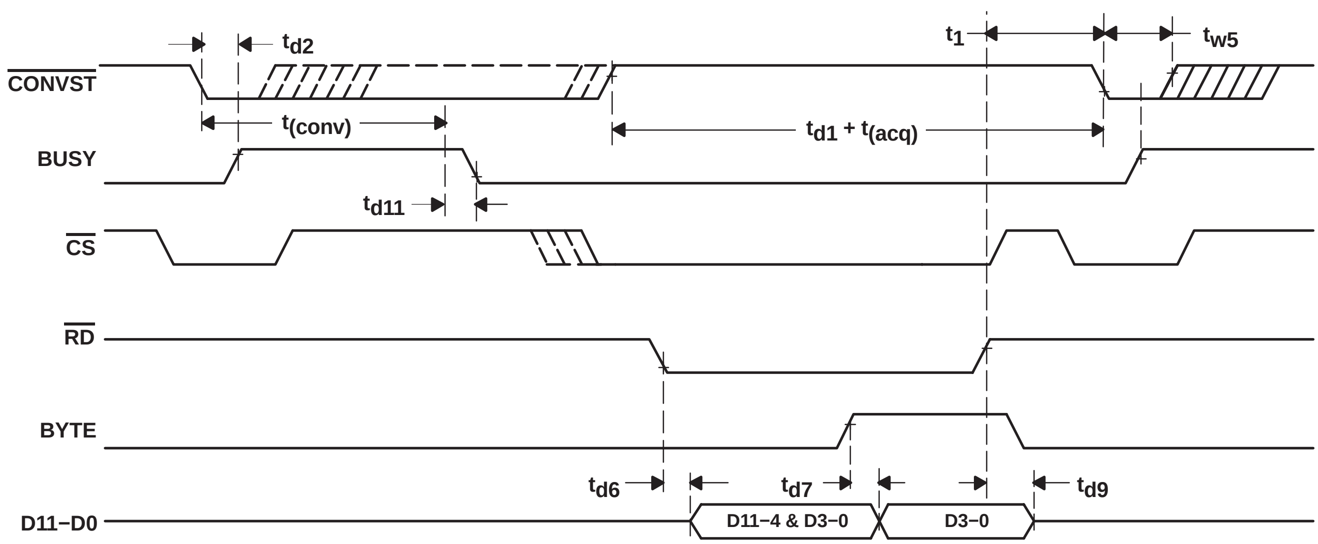


Figure 5. Read Control Via $\overline{\text{CS}}$ and $\overline{\text{RD}}$

There are two output formats available. Twelve bit data appears on the bus during a read operation while BYTE is low. When BYTE is high, the lower byte (D3 through D0 followed by all zeroes) appears on the data bus with D3 in the MSB. This feature is useful for interfacing with eight bit microprocessors and microcontrollers.

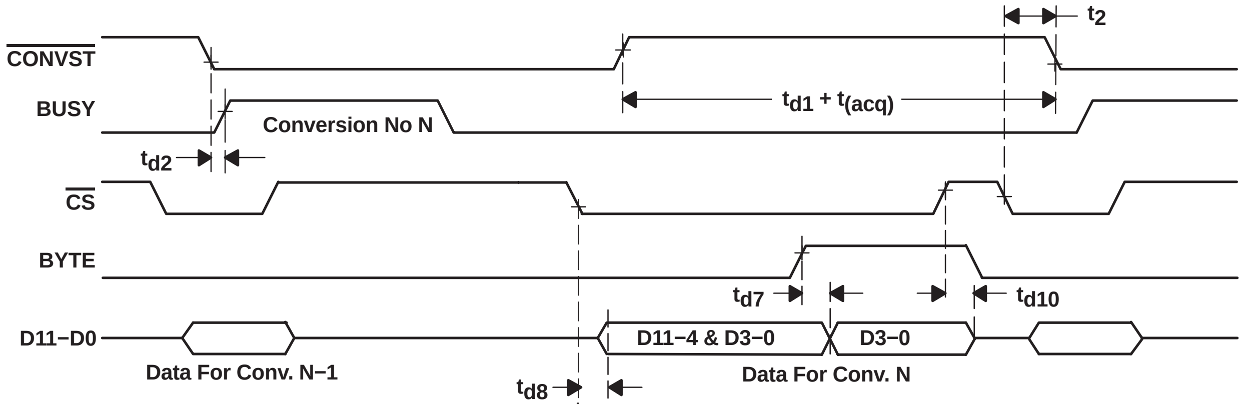


Figure 6. Read Control Via $\overline{CS}$ and $\overline{RD}$ Tied to BDGND

DEVICE OPERATION AND DATA READ IN BACK-TO-BACK CONVERSION

The following two figures illustrate device operation in back-to-back conversion mode. It is possible to operate the device at any throughput in this mode, but this is the only mode in which the device can be operated at throughputs exceeding 3.5 MSPS.

A conversion starts on the $\overline{CONVST}$ falling edge. The BUSY output goes high after a delay (t_{d2}). Note that care must be taken not to abort the conversion (see Figure 4) apart from timing restrictions shown in Figure 7 and Figure 8. The conversion ends within the conversion time, $t_{(conv)}$, after the $\overline{CONVST}$ falling edge. The new acquisition can be immediately started without waiting for the BUSY signal to go low. This can be ensured with a $\overline{CONVST}$ high pulse width that is more than or equal to ($t_0 - t_{(conv)}$ + 10 nsec) which is t_{w4} for a 4-MHz operation.

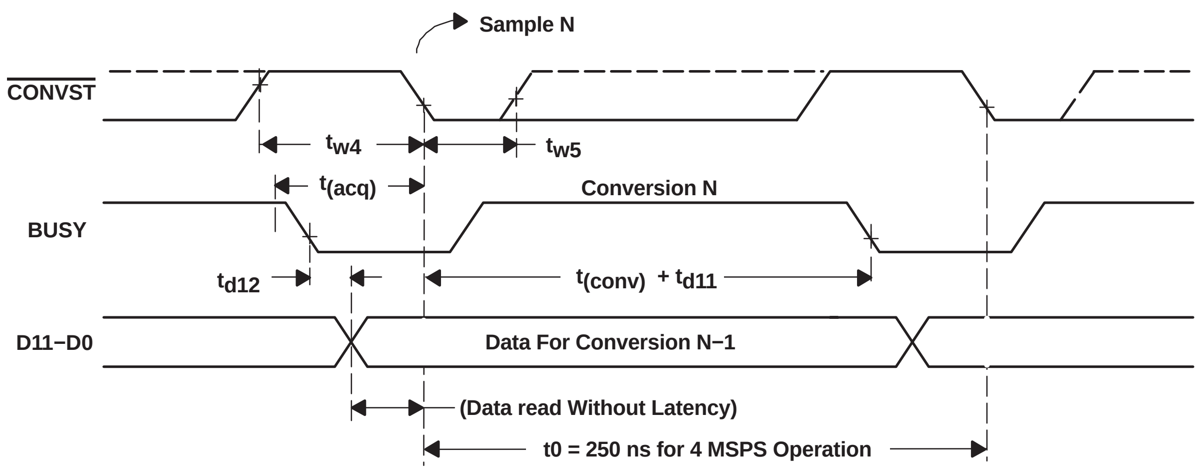


Figure 7. Back-To-Back Operation With $\overline{CS}$ and $\overline{RD}$ Low

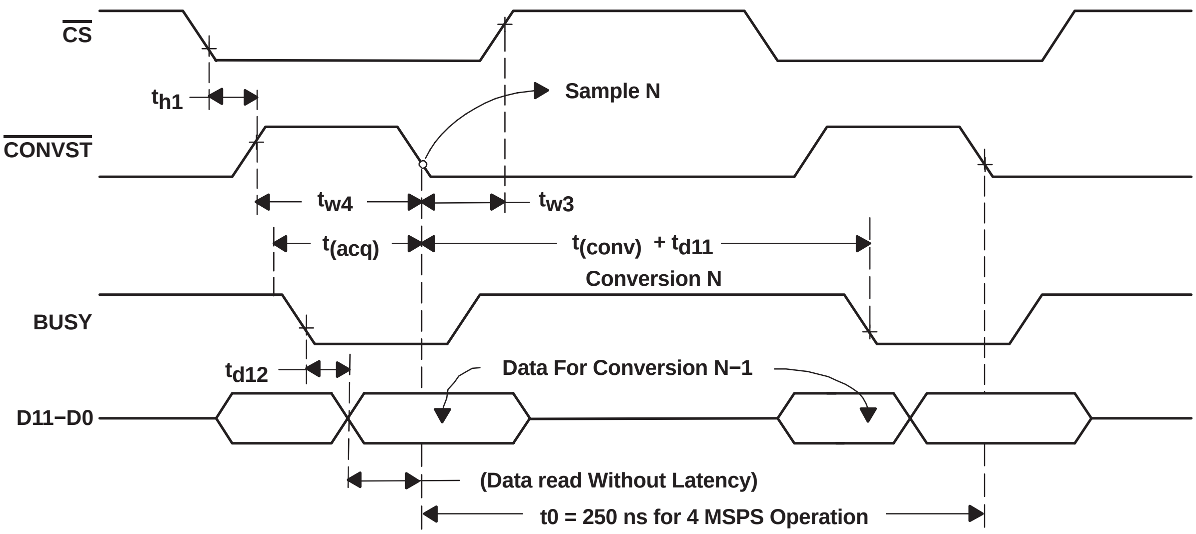


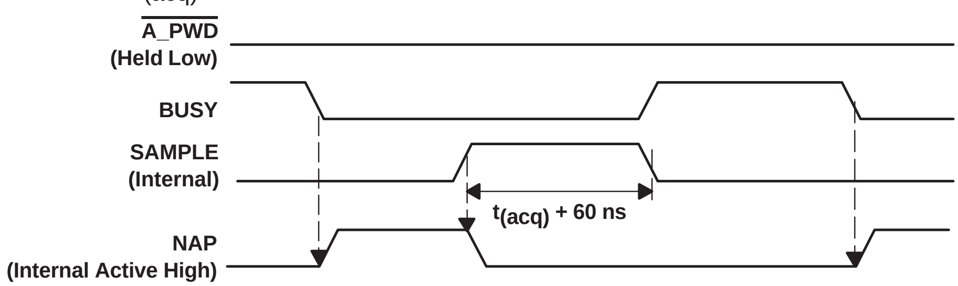
Figure 8. Back-To-Back operation With $\overline{\text{CS}}$ Toggling and $\overline{\text{RD}}$ Low

NAP MODE

The device can be put in nap mode following the sequences shown in Figure 9. This provides substantial power saving while operating at lower sampling rates.

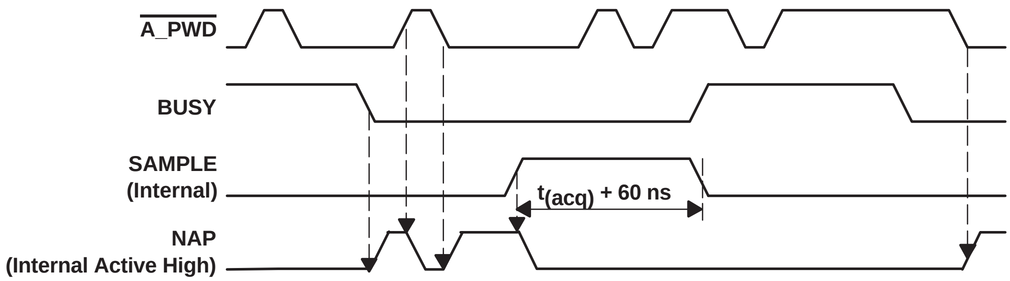
While operating the device at throughput rates lower than 3.2 MSPS, $\overline{\text{A\_PWD}}$ can be held low (see Figure 9). In this condition, the device goes into the nap state immediately after BUSY goes low and remains in that state until the next sampling starts. The minimum acquisition time is 60 nsec more than $t_{(acq)}$ as defined in the timing requirements section.

Alternately, $\overline{\text{A\_PWD}}$ can be toggled any time during operation (see Figure 10). This is useful when the system acquires data at the maximum conversion speed for some period of time (back-to-back conversion) and it does not acquire data for some time while the acquired data is being processed. During this period, the device can be put in the nap state to save power. The device remains in the nap state as long as $\overline{\text{A\_PWD}}$ is low with BUSY being low and sampling has not started. The minimum acquisition time for the first sampling after the nap state is 60 nsec more than $t_{(acq)}$ as defined in the timing requirements section.



NOTE: The SAMPLE (Internal) signal is generated as described in the Sampling and Conversion Start section.

Figure 9. Device Operation While $\overline{\text{A\_PWD}}$ is Held Low



NOTE: The SAMPLE (Internal) signal is generated as described in the Sampling and Conversion Start section.

Figure 10. Device Operation While $\overline{\text{A\_PWD}}$ is Toggling

POWERDOWN/RESET

A low level on the $\overline{\text{PWD}}$/$\overline{\text{RST}}$ pin puts the device in the powerdown phase. This is an asynchronous signal. As shown in Figure 11, the device is in the reset phase for the first t_{W6} period after a high-to-low transition of $\overline{\text{PWD}}$/$\overline{\text{RST}}$. During this period the output code is FE0 (hex) to indicate that the device is in the reset phase. The device powers down if the $\overline{\text{PWD}}$/$\overline{\text{RST}}$ pin continues to be low for a period of more than t_{W7}. Data is not valid for the first four conversions after a power-up (see Figure 11) or an end of reset (see Figure 12). The device is initialized during the first four conversions.

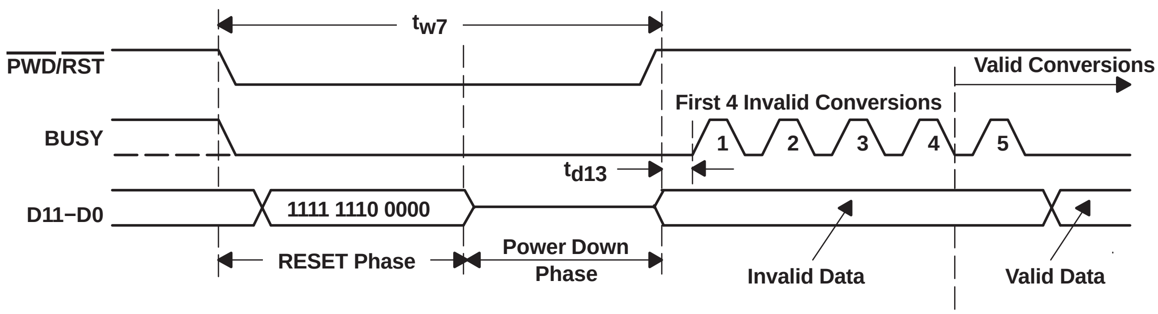


Figure 11. Device Power Down

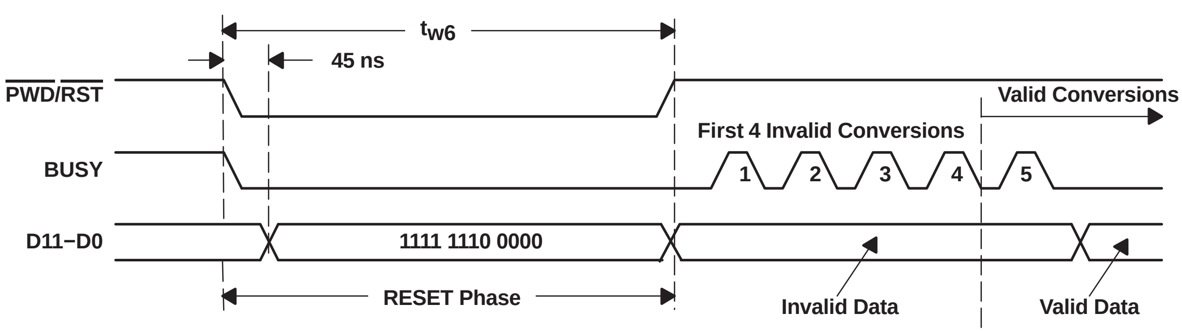


Figure 12. Device Reset

TYPICAL CHARACTERISTICS(1)

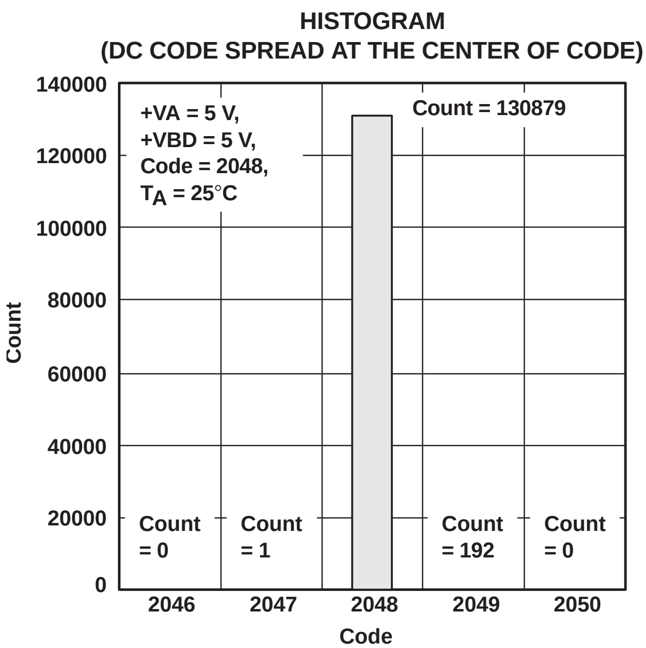


Figure 13

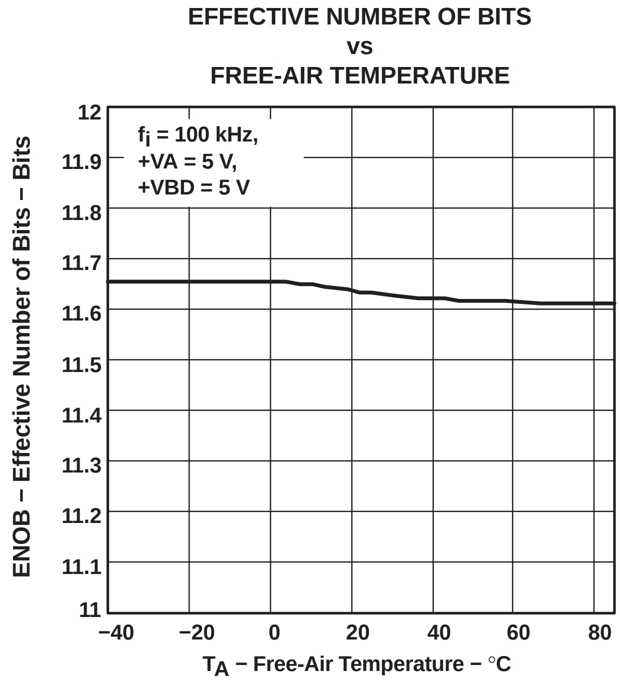


Figure 14

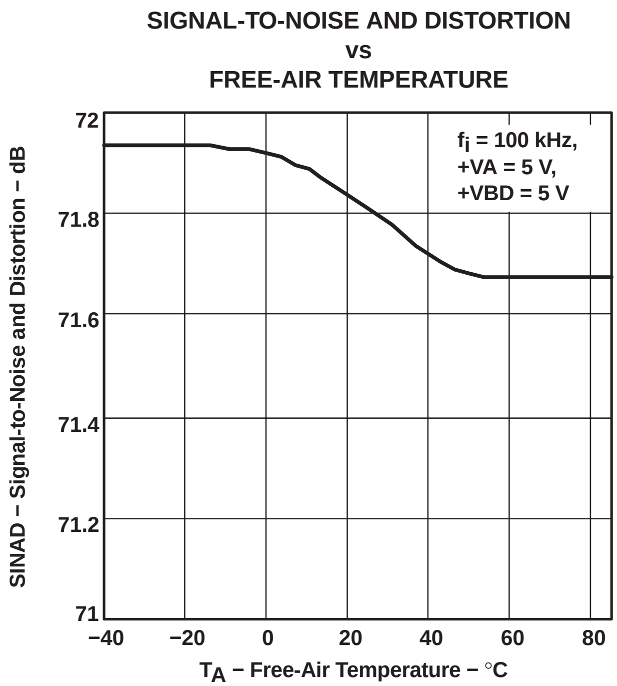


Figure 15

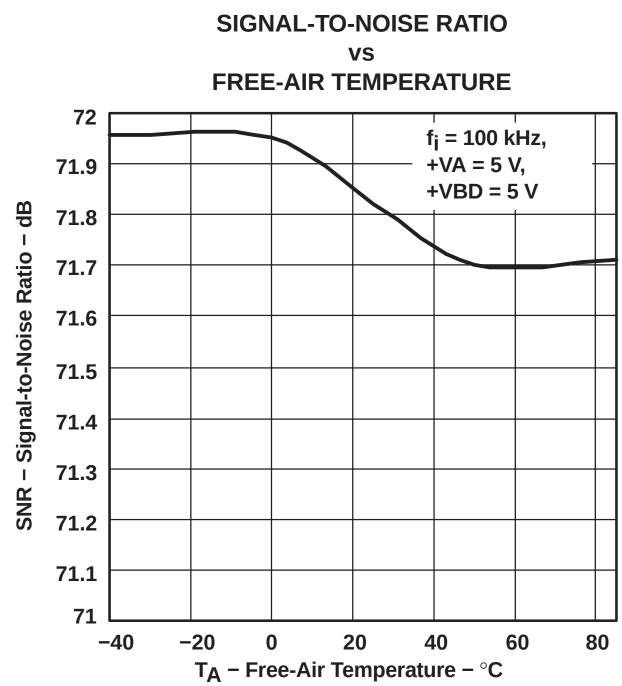


Figure 16

(1) At sample rate = 4 MSPS, V_{ref} = 2.5 V external, unless otherwise specified.

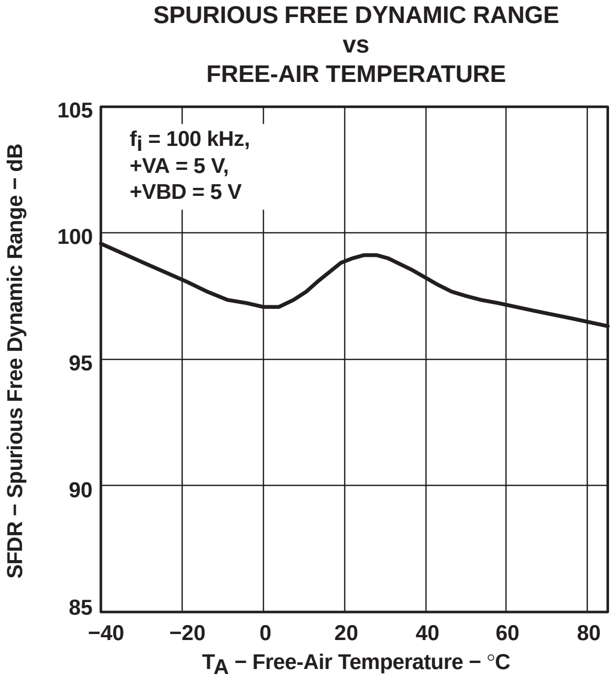


Figure 17

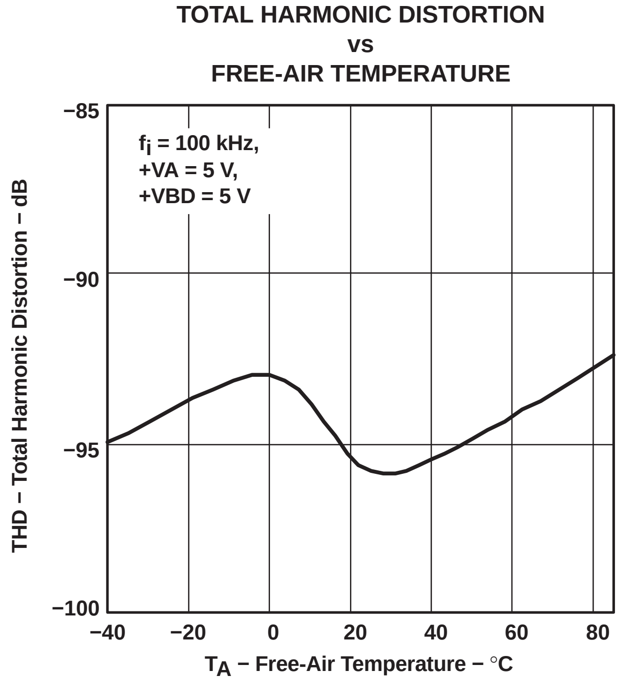


Figure 18

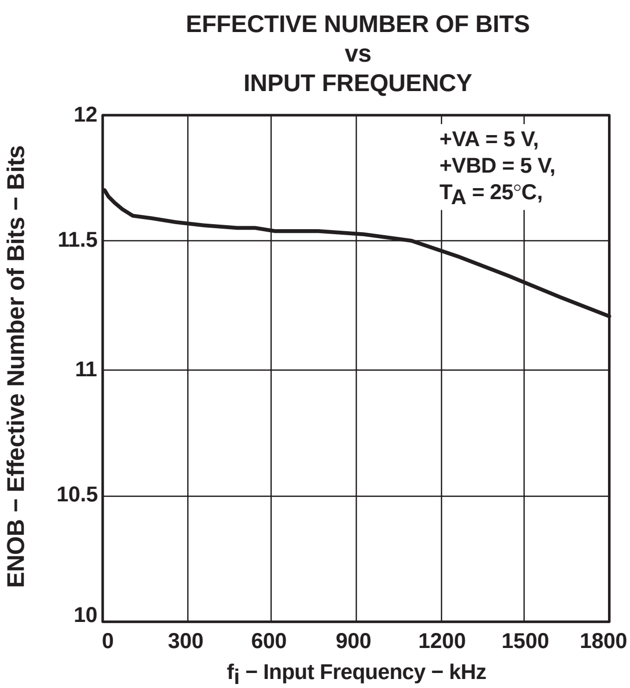


Figure 19

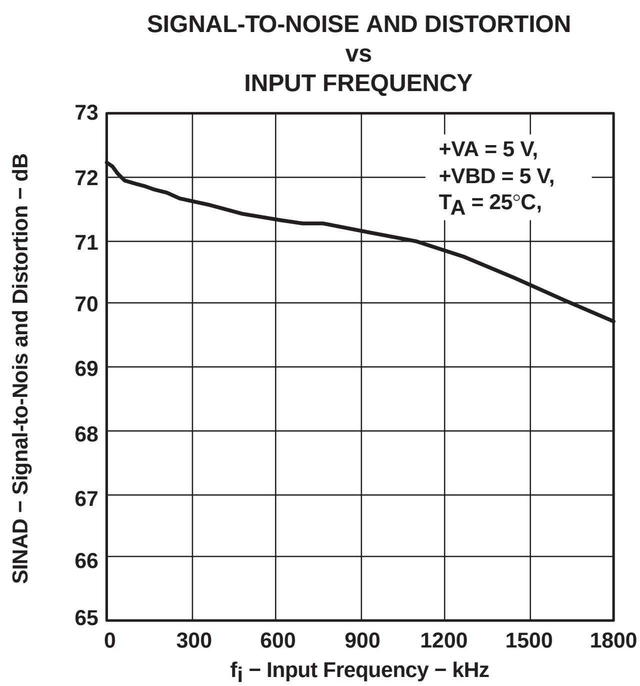


Figure 20

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

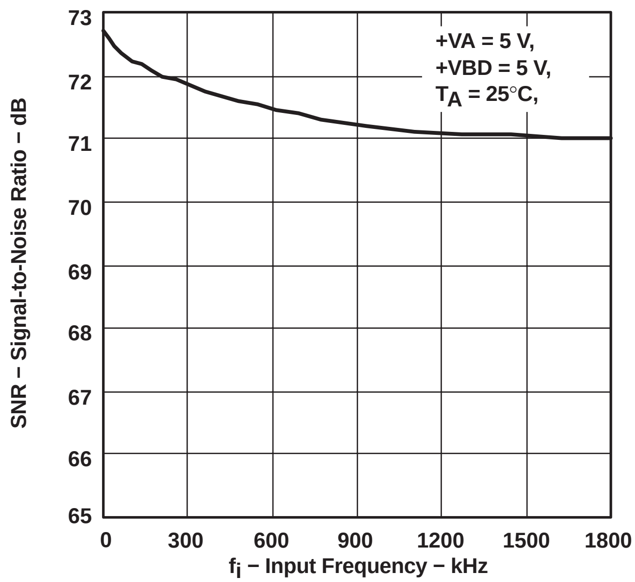


Figure 21

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

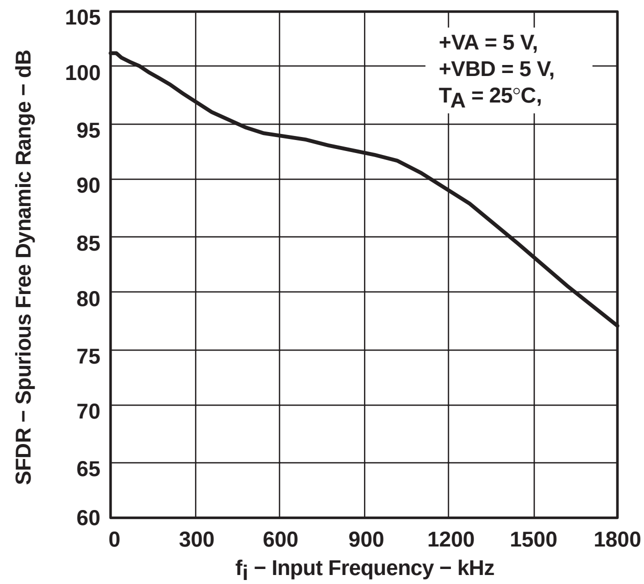


Figure 22

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

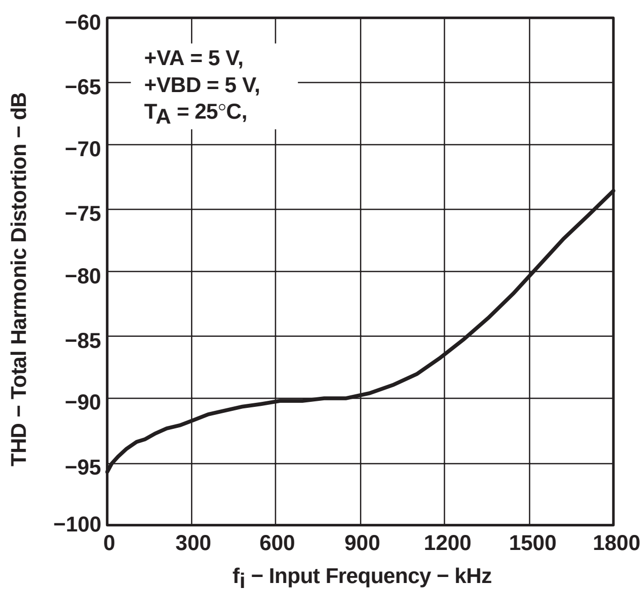


Figure 23

GAIN ERROR
vs
SUPPLY VOLTAGE

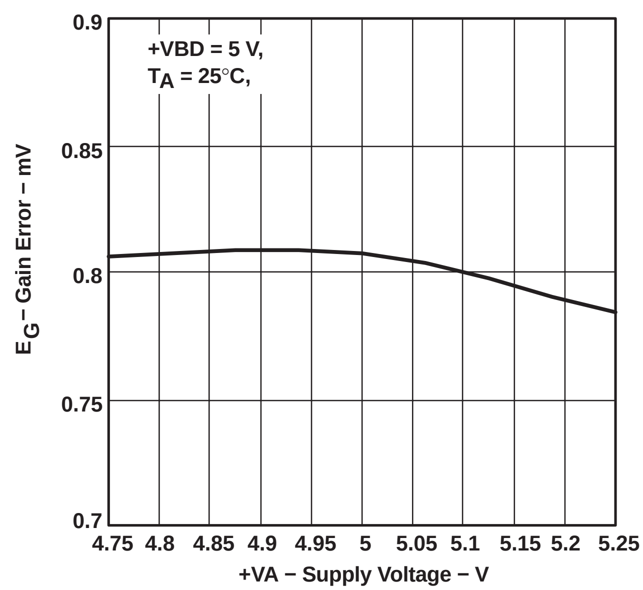


Figure 24

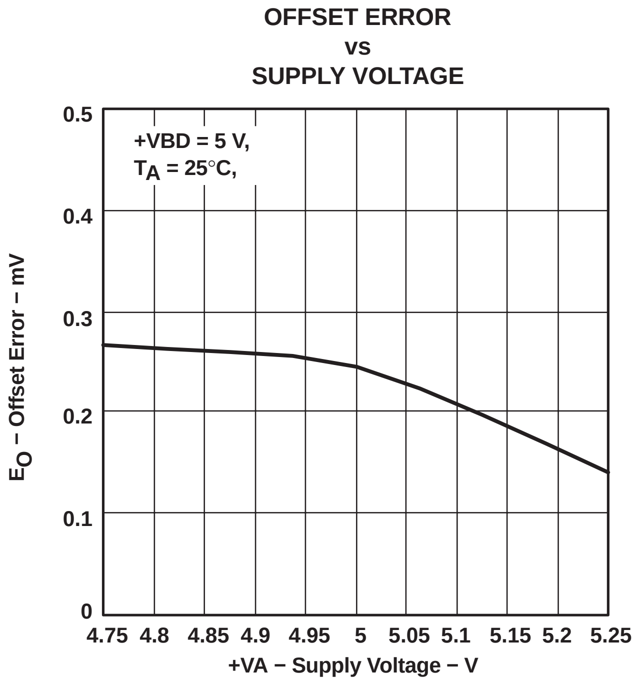


Figure 25

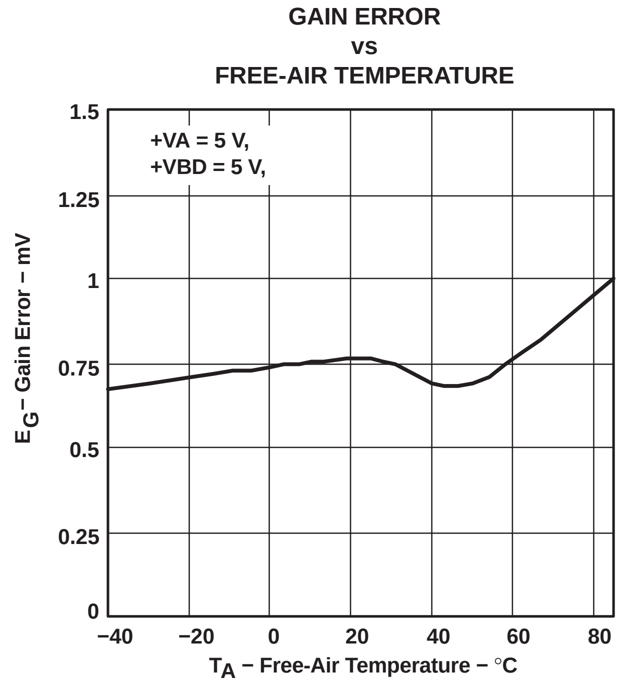


Figure 26

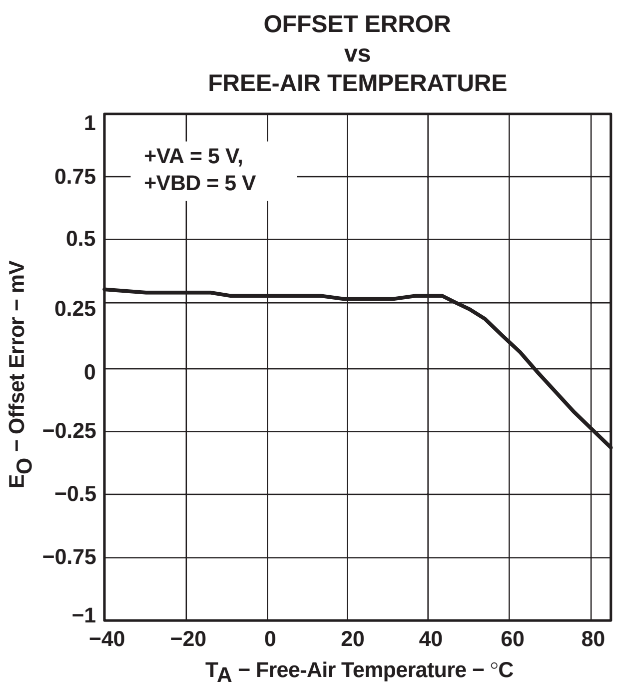


Figure 27

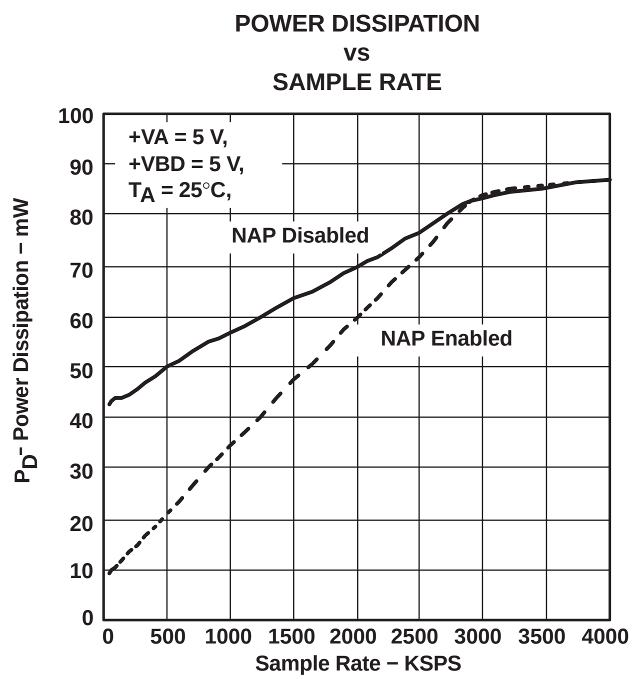


Figure 28

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

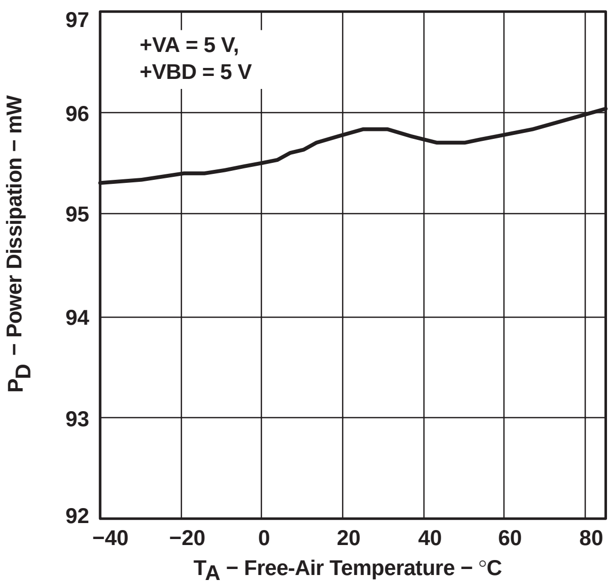


Figure 29

DIFFERENTIAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

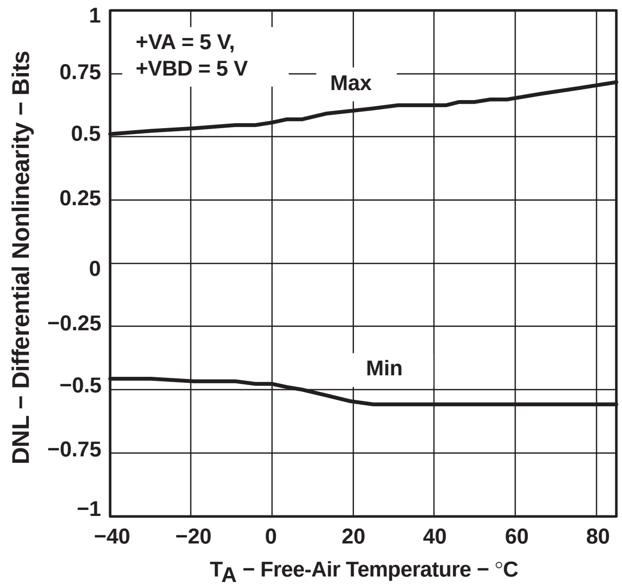


Figure 30

INTEGRAL NONLINEARITY
vs
FREE-AIR TEMPERATURE

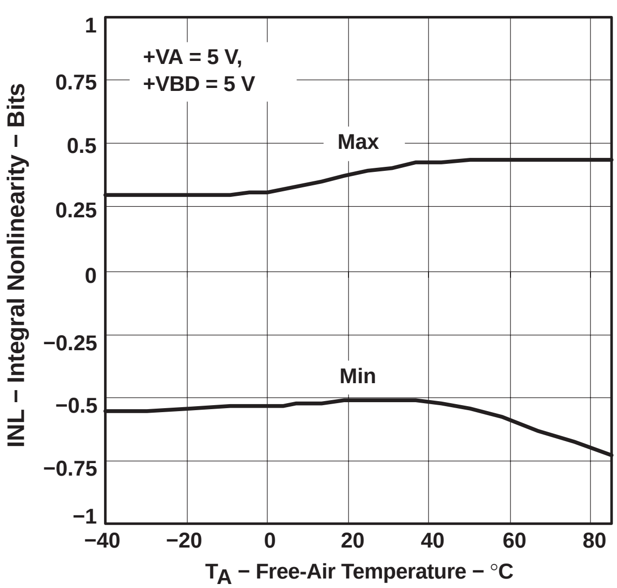


Figure 31

INTERNAL REFERENCE OUTPUT
vs
FREE-AIR TEMPERATURE

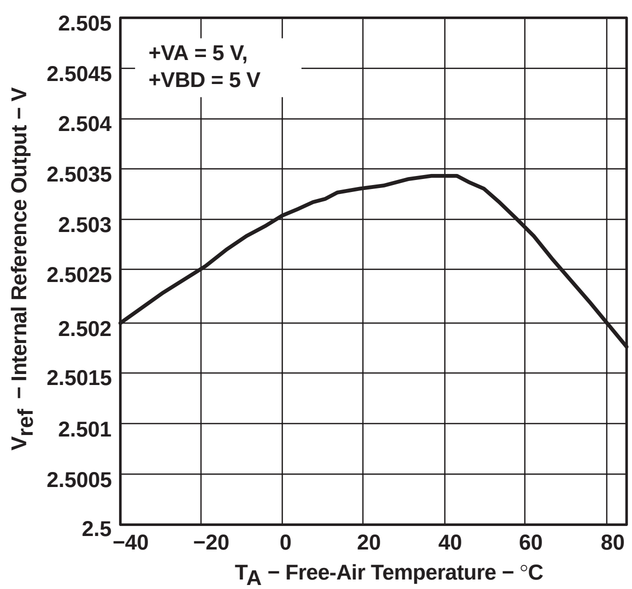


Figure 32

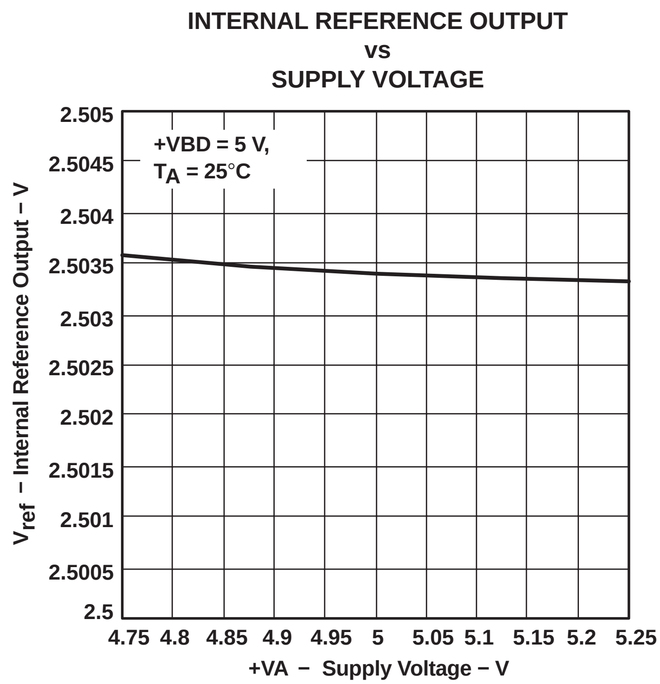


Figure 33

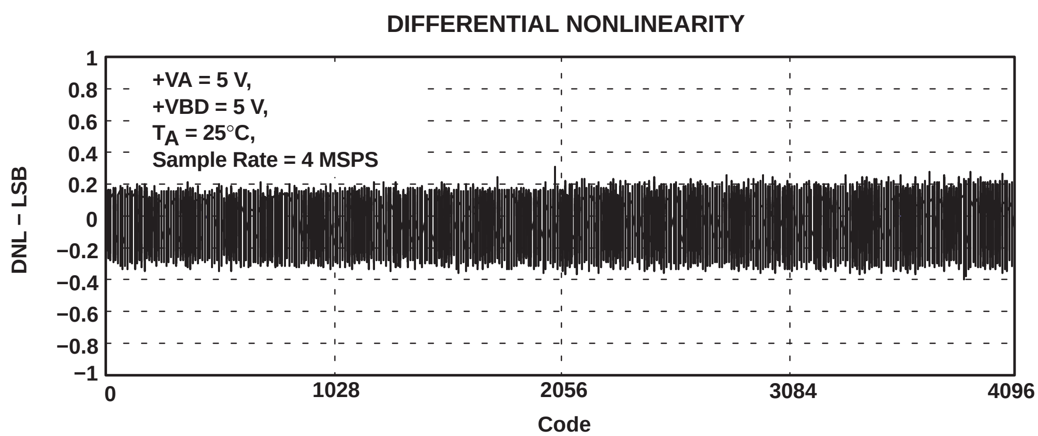


Figure 34

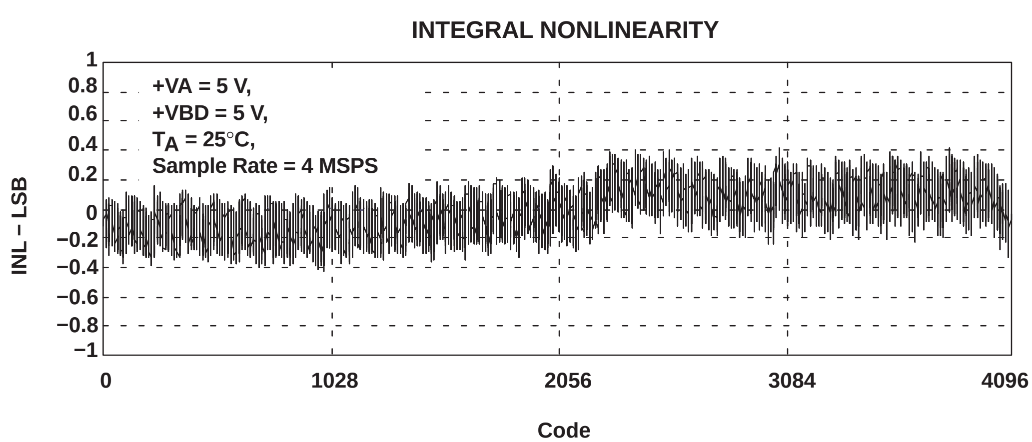


Figure 35

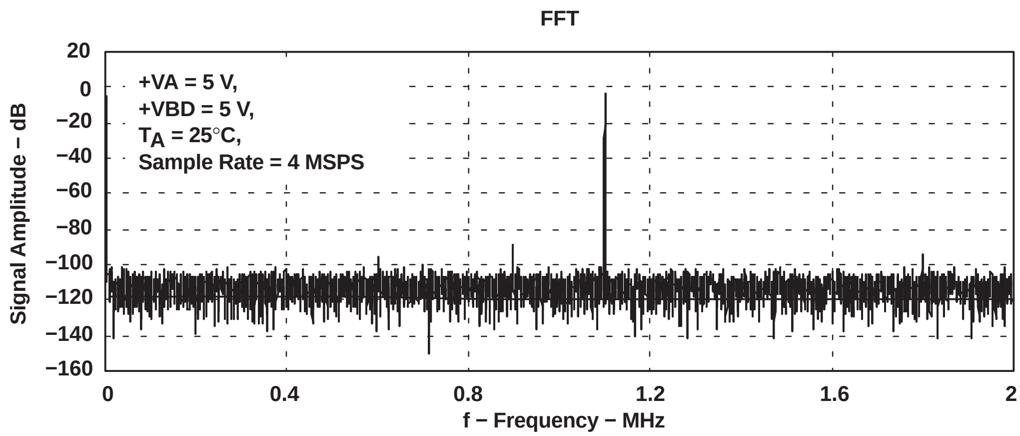

FFT
+VA = 5 V,
+VBD = 5 V,
T_A = 25°C,
Sample Rate = 4 MSPS
Signal Amplitude − dB
20
0
−20
−40
−60
−80
−100
−120
−140
−160
0
0.4
0.8
1.2
1.6
2
f − Frequency − MHz

Figure 36

PRINCIPLES OF OPERATION

The ADS7881 is a member of a family of high-speed successive approximation register (SAR) analog-to-digital converters (ADC). The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The conversion clock is generated internally. The conversion time is 200 ns max (at 5 V +VBD).

The analog input is provided to two input pins: +IN and −IN. (Note that this is pseudo differential input and there are restrictions on –IN voltage range.) When a conversion is initiated, the difference voltage between these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS7881 has a built-in 2.5-V (nominal value) reference but can operate with an external reference. When an internal reference is used, pin 2 (REFOUT) should be connected to pin 1 (REFIN) with an 0.1-µF decoupling capacitor and a 1-µF storage capacitor between pin 2 (REFOUT) and pins 47, 48 (REFM). The internal reference of the converter is buffered . There is also a buffer from REFIN to CDAC. This buffer provides isolation between the external reference and the CDAC and also recharges the CDAC during conversion. It is essential to decouple REFOUT to AGND with a 0.1-µF capacitor while the device operates with an external reference.

ANALOG INPUT

When the converter enters hold mode, the voltage difference between the +IN and −IN inputs is captured on the internal capacitor array. The voltage on the −IN input is limited to between –0.2 V and 0.2 V, thus allowing the input to reject a small signal which is common to both the +IN and −IN inputs. The +IN input has a range of –0.2 V to (+V_{ref} +0.2 V). The input span (+IN – (−IN)) is limited from 0 V to VREF.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, signal frequency, and source impedance. Essentially, the current into the ADS7881 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current (this may not happen when a signal is moving continuously). The source of the analog input voltage must be able to charge the input capacitance (27 pF) to better than a 12-bit settling level with a step input within the acquisition time of the device. The step size can be selected equal to the maximum voltage difference between two consecutive samples at the maximum signal frequency. (Refer to Figure 39 for the suggested input circuit.) When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, both −IN and +IN inputs should be within the limits specified. Outside of these ranges, the converter’s linearity may not meet specifications.

Care should be taken to ensure that +IN and −IN see the same impedance to the respective sources. (For example, both +IN and −IN are connected to a decoupling capacitor through a 21-Ω resistor as shown in Figure 39.) If this is not observed, the two inputs could have different settling times. This may result in an offset error, gain error, or linearity error which changes with temperature and input voltage.

DIGITAL INTERFACE

TIMING AND CONTROL

Refer to the SAMPLING AND CONVERSION START section and the CONVERSION ABORT section.

READING DATA

The ADS7881 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{CS}$ and $\overline{RD}$ are both low. There is a minimal quiet sampling period requirement around the falling edge of $\overline{CONVST}$ as stated in the timing requirements section. Data reads or bus three-state operations should not be attempted within this period. Any other combination of $\overline{CS}$ and $\overline{RD}$ three-states the parallel output. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes(1)

DESCRIPTION	ANALOG VALUE	BINARY CODE	HEX CODE
Full scale	V_{ref} − 1 LSB	1111 1111 1111	FFF
Midscale	$V_{ref}/2$	1000 0000 0000	800
Midscale − 1 LSB	$V_{ref}/2$ − 1 LSB	0111 1111 1111	7FF
Zero	0 V	0000 0000 0000	000

(1) Full-scale range = V_{ref} and least significant bit (LSB) = $V_{ref}/4096$

The output data appears as a full 12-bit word (D11−D0) on pins DB11 – DB0 (MSB−LSB) if BYTE is low.

READING THE DATA IN BYTE MODE

The result can also be read on an 8-bit bus for convenience by using pins DB11−DB4. In this case two reads are necessary; the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB11−DB4, and then bringing BYTE high. When BYTE is high, the lower bits (D3−D0) followed by all zeros are on pins DB11 − DB4 (refer to Table 2).

These multi-word read operations can be performed with multiple active $\overline{RD}$ signals (toggling) or with $\overline{RD}$ tied low for simplicity.

Table 2. Conversion Data Read Out

BYTE	DATA READ OUT	
	DB11 − DB4	DB3 − DB0
High	D3 − D0, 0000	All zeroes
Low	D11 − D4	D3 − D0

Also refer to the DATA READ and DEVICE OPERATION AND DATA READ IN BACK-TO-BACK CONVERSION sections for more details.

Reset

Refer to the POWERDOWN/RESET section for the device reset sequence.

It is recommended to reset the device after power on. A reset can be issued once the power has reached 95% of its final value.

$\overline{PWD}/\overline{RST}$ is an asynchronous active low input signal. A current conversion is aborted no later than 45 ns after the converter is in the reset mode. In addition, the device outputs a FE0 code to indicate a reset condition. The converter returns back to normal operation mode immediately after the $\overline{PWD}/\overline{RST}$ input is brought high.

Data is not valid for the first four conversions after a device reset.

Powerdown

Refer to the POWERDOWN/RESET section for the device powerdown sequence.

The device enters powerdown mode if a $\overline{PWD}/\overline{RST}$ low duration is extended for more than a period of t_{w7}.

The converter goes back to normal operation mode no later than a period of t_{d13} after the $\overline{PWD}/\overline{RST}$ input is brought high.

After this period, normal conversion and sampling operation can be started as discussed in previous sections. Data is not valid for the first four conversions after a device reset.

Nap Mode

Refer to the NAP MODE section in the DESCRIPTION AND TIMING DIAGRAMS section for information.

APPLICATION INFORMATION

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7881 circuitry.

As the ADS7881 offers single-supply operation, it is often used in close proximity with digital logic, micro-controllers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve acceptable performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to the end of sampling (within quiet sampling time) and just prior to latching the output of the analog comparator during the conversion phase. Thus, driving any single conversion for an n-bit SAR converter, there are n+1 windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS7881 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor and 1-µF storage capacitor are recommended from REFIN (pin 1) directly to REFM (pin 48).

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a micro-controller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane that is separate from the connection for +VBD and digital logic until they are connected at the power entry point onto the PCB. Power to the ADS7881 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of capacitor. In addition to a 0.1-µF capacitor, a 1-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors, all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 3. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE / SUPPLY PINS	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
Pairs of pins that require a shortest path to decoupling capacitors	(4,5), (9,8), (10,11), (13, 15), (43, 44) (46, 45)	(24, 25), (34, 35)
Pins that require no decoupling	14, 12	

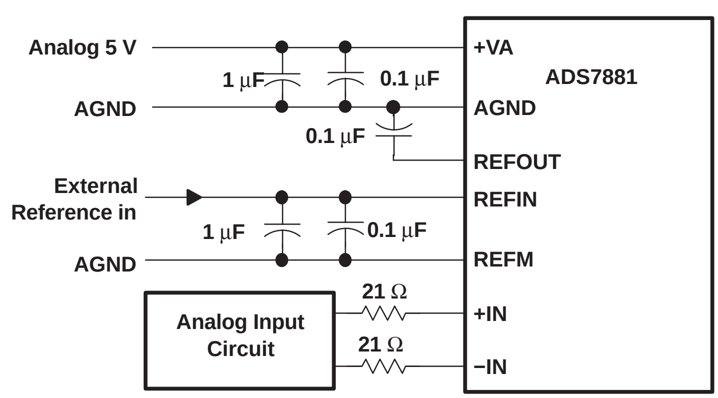


Figure 37. Using External Reference

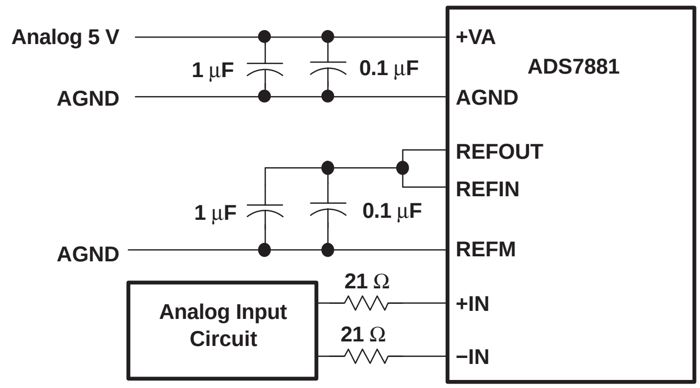


Figure 38. Using Internal Reference

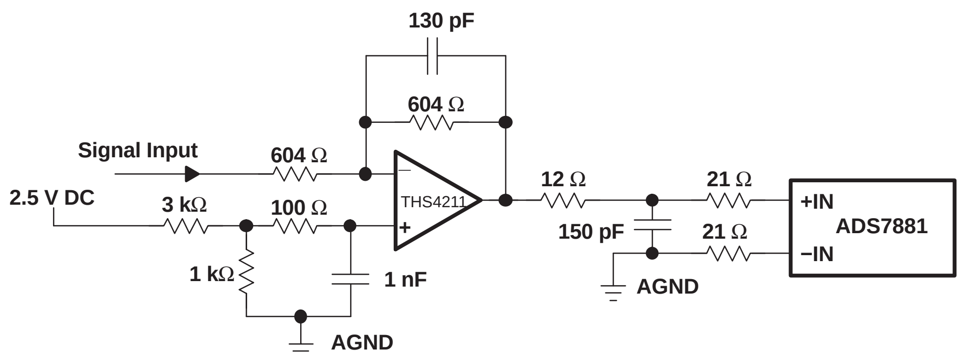


Figure 39. Typical Analog Input Circuit

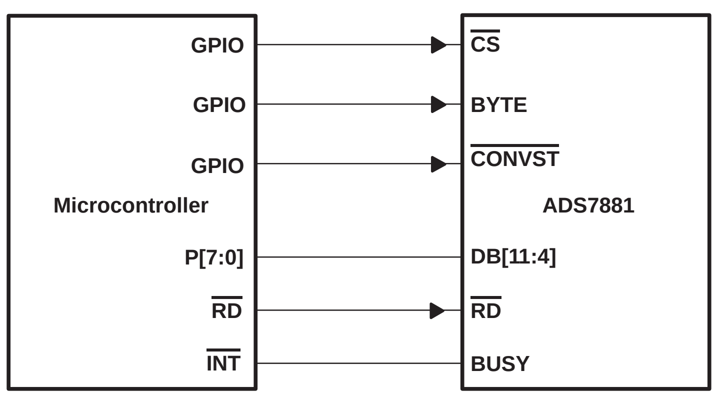
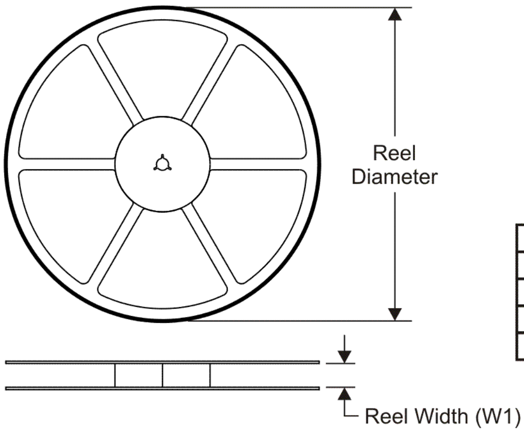


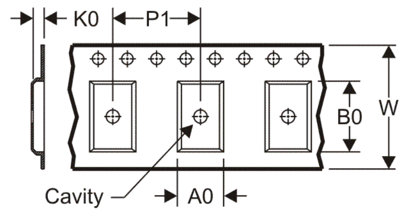
Figure 40. Interfacing With Microcontroller

TAPE AND REEL INFORMATION

REEL DIMENSIONS

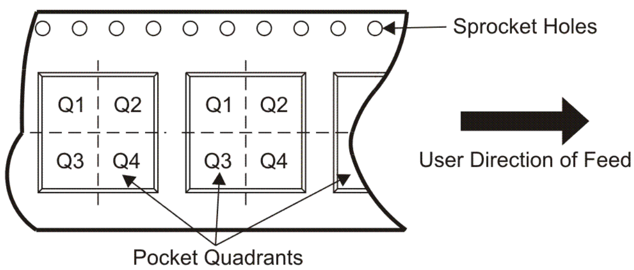


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

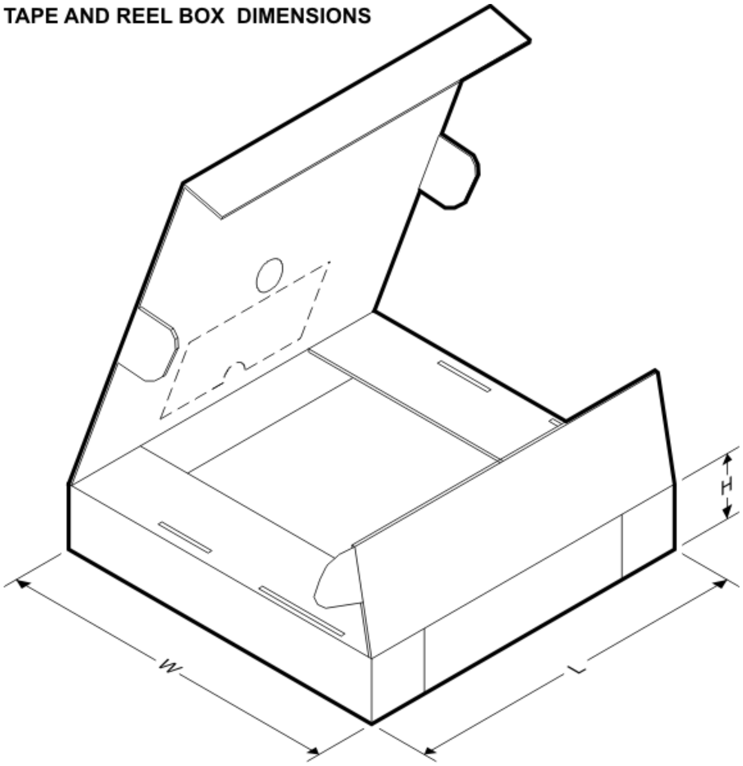
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7881IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS7881IPFBT	TQFP	PFB	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS7881IRGZR	QFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS7881IRGZT	QFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

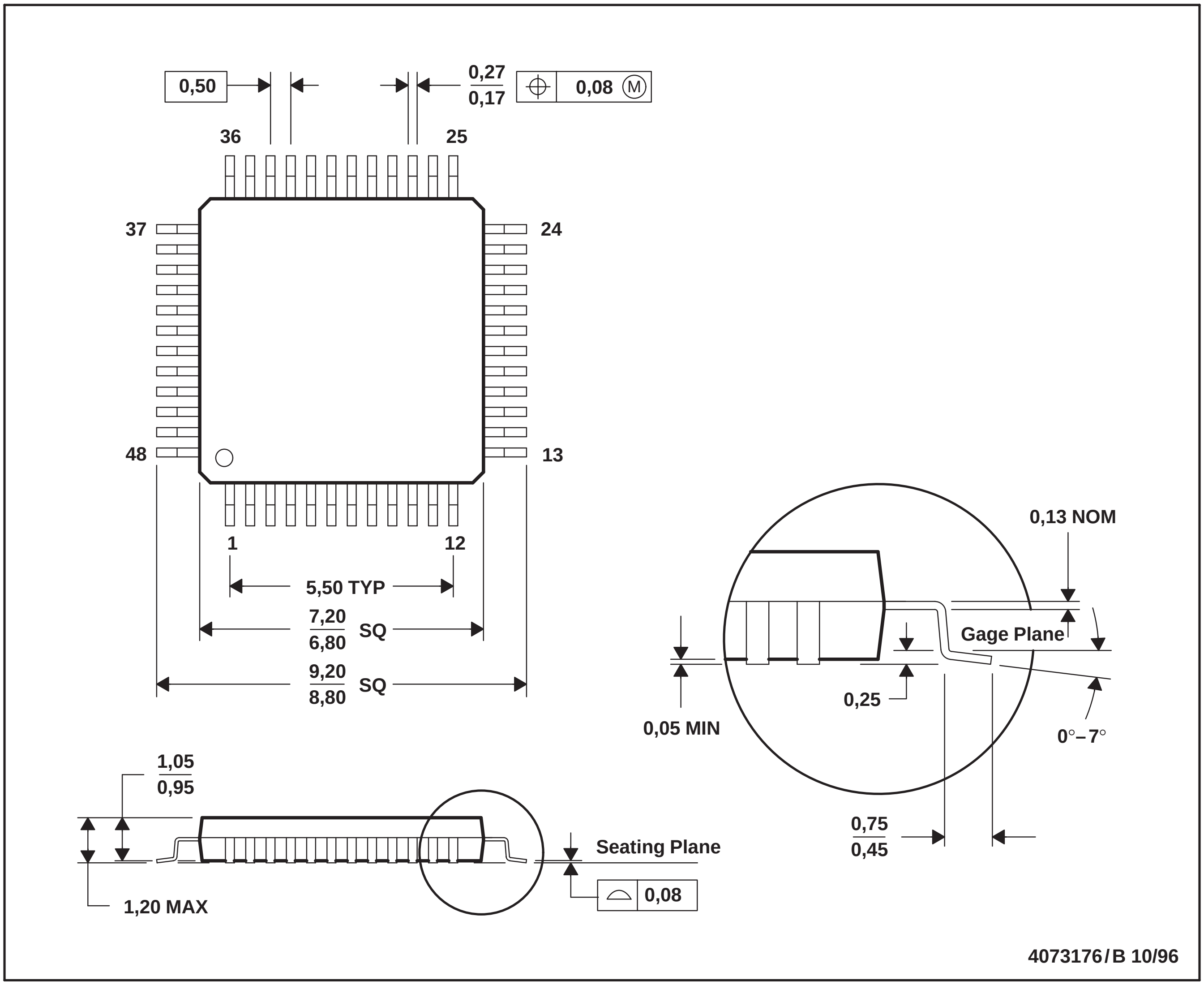
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

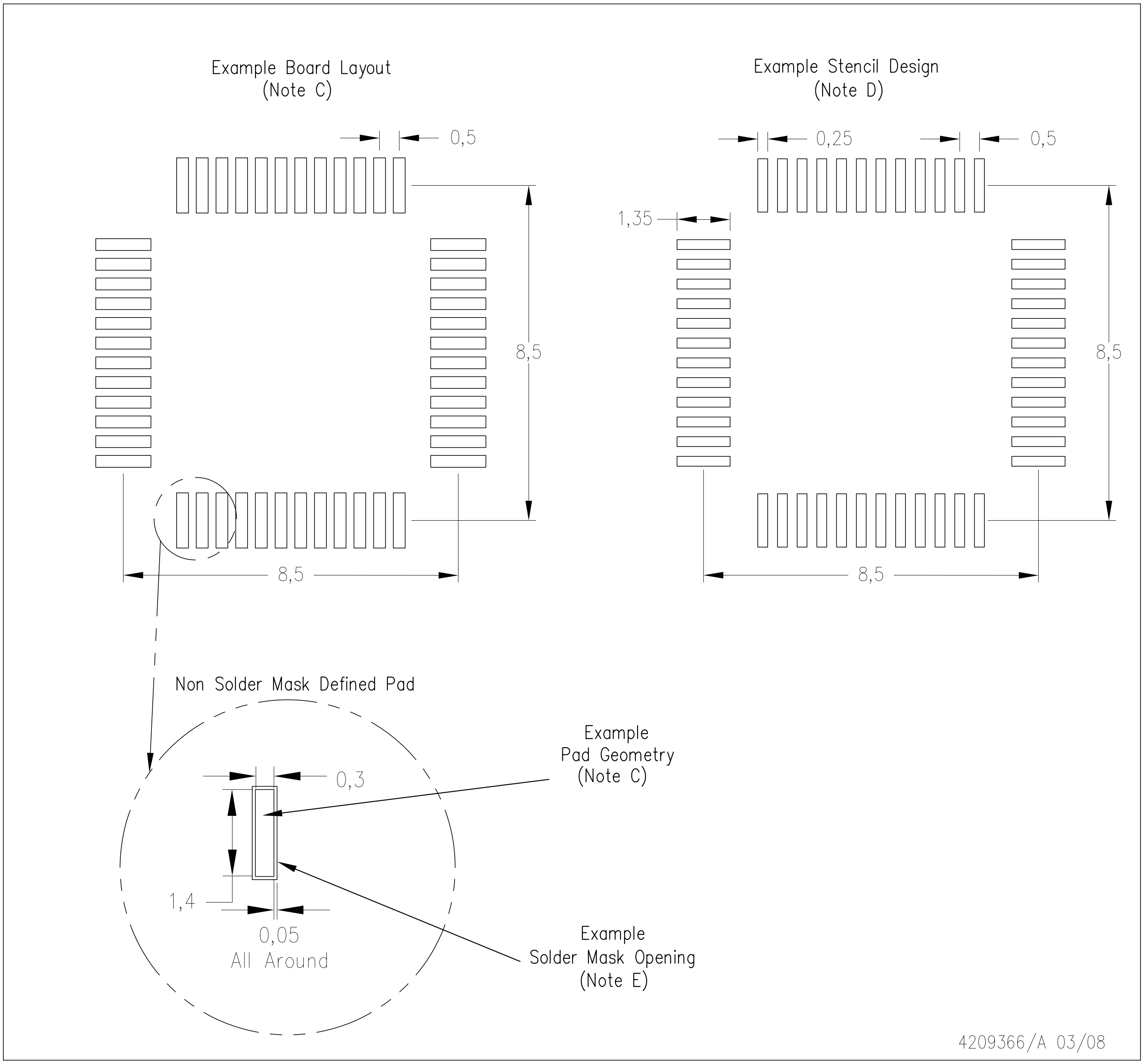
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7881IPFBR	TQFP	PFB	48	1000	346.0	346.0	33.0
ADS7881IPFBT	TQFP	PFB	48	250	346.0	346.0	33.0
ADS7881IRGZR	QFN	RGZ	48	2500	333.2	345.9	28.6
ADS7881IRGZT	QFN	RGZ	48	250	333.2	345.9	28.6

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



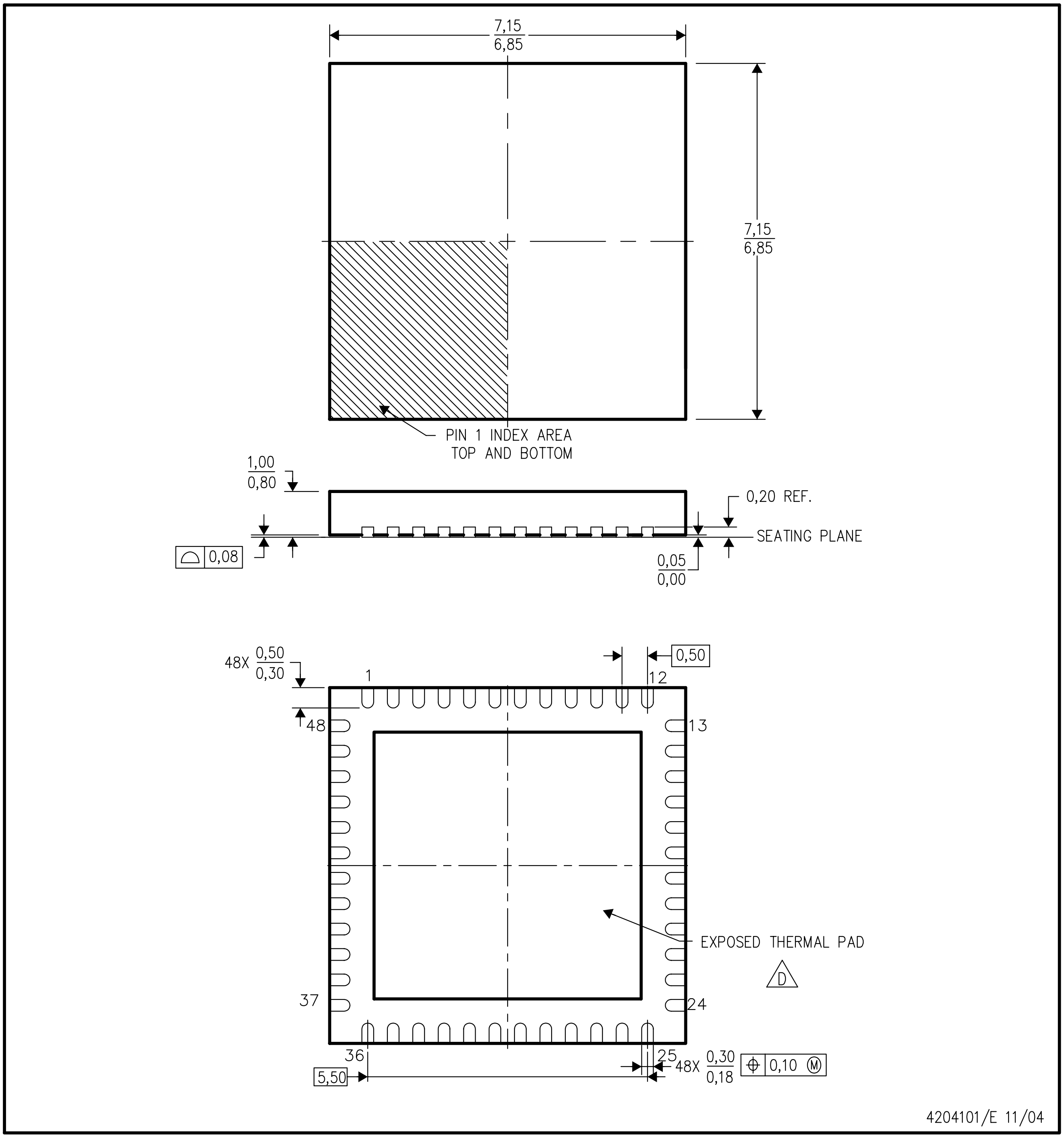
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S-PQFP-G48)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

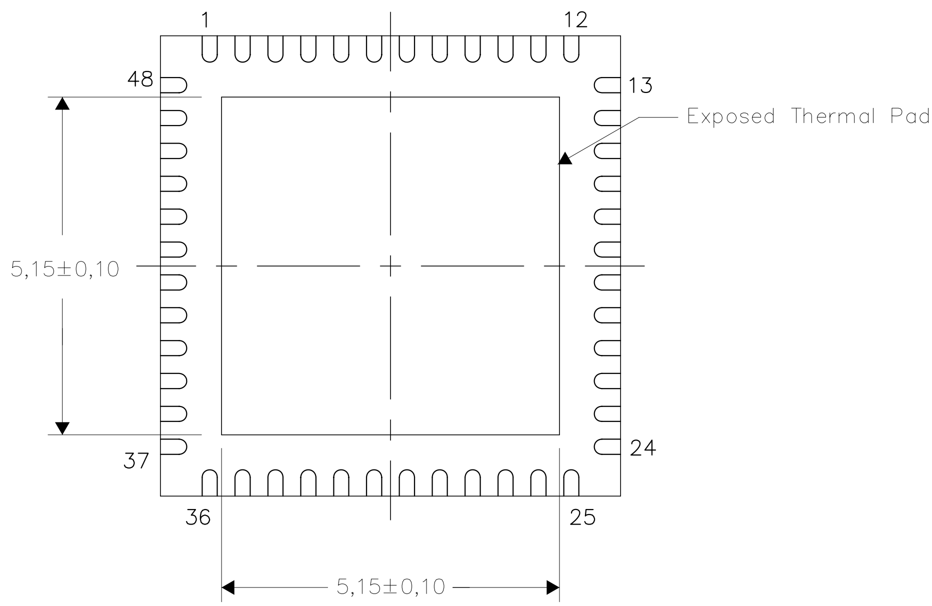
RGZ (S-PVQFN-N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

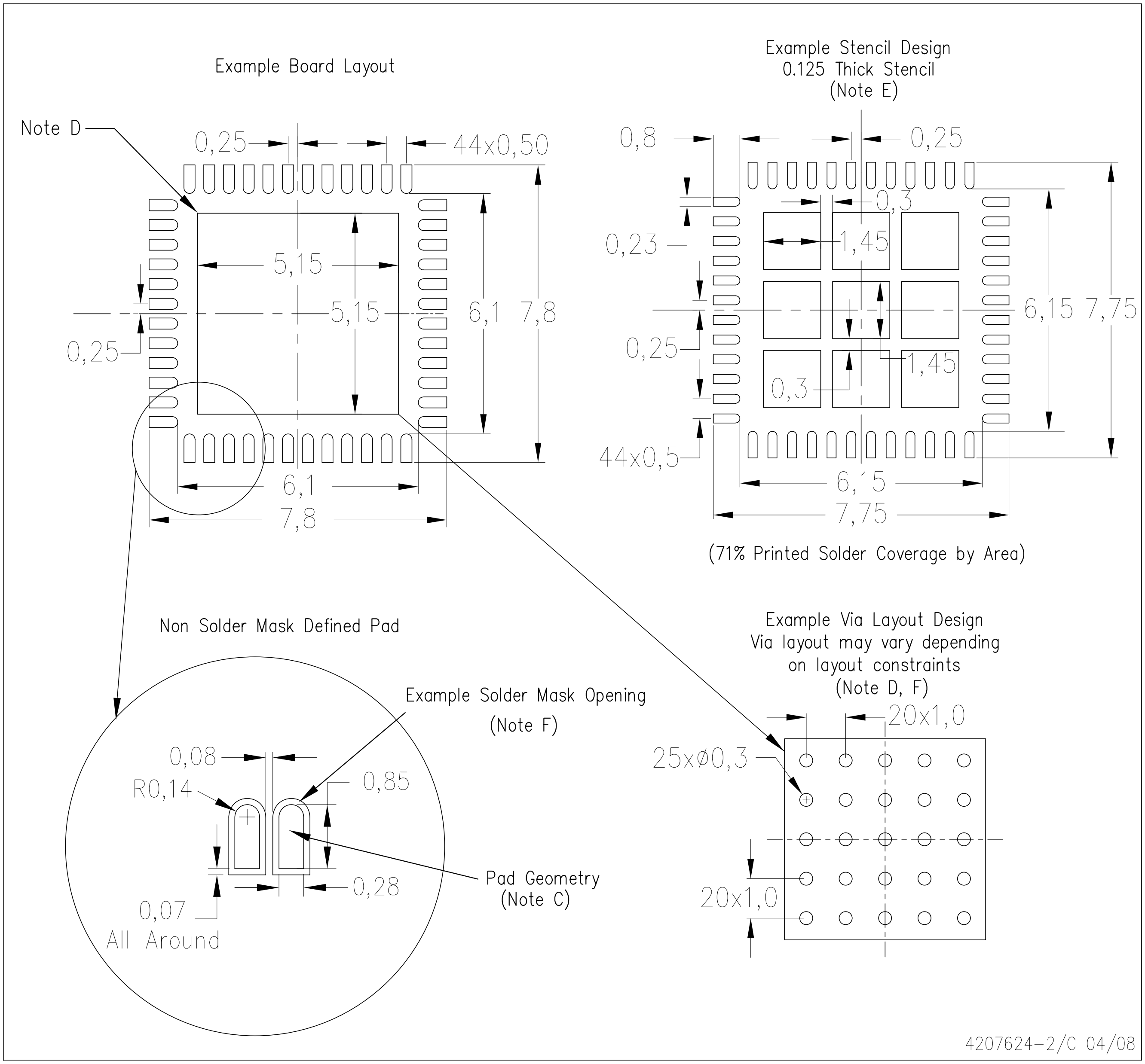


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S–PVQFN–N48)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.