FAIRCHILD SEMICONDUCTOR™

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Effects of On Resistance (R_{ON}) to an Analog Switch

There are many factors that affect R_{ON} such as temperature, input voltage, supply voltage, and gate length "W".

The following calculations derive how Gate Length "W" effects R_{ON}.

$I_D = (\mu_n C_{OX}) W/L [(V_{GS} - V_T) V_{DS} - 1/2V_{DS}^{\wedge 2}]$

Where:

μ_n = Electron mobility, (the ease with which electrons drift in the material)

C_{OX} = Oxide capacitance

W = Length of the gate (see Figure 1)

L = Width of the gate (see Figure 1)

R_{ON} = On Resistance or resistance drain-to-source

I_D = Drain current

R_{ON} can be derived by taking the partial derivative of I_D over V_{DS} where all other variables are considered constant.

$R_{ON} = 1/(\mu_n C_{OX} W/L)(V_{CC} - V_{IN} - V_T))$

Where:

$V_{DS} = 0$

Therefore:

$R_{ON} = 1/(\mu_n C_{OX} W/L)(V_{GS} - V_T)$

Where:

$V_S = V_{IN}$ and $V_G = V_{CC}$

Therefore (Equation 1):

$R_{ON} = 1/(\mu_n C_{OX} W/L)(V_{CC} - V_{IN} - V_T)$

Optimizing the performance of a MOSFET as an analog switch requires a number of trade-offs. If the Width/Length ratio is increased to reduce R_{ON} the parasitic capacitance of the gate oxide will increase proportionately resulting in lower bandwidth. The two graphs below (Figures 2, 3) show R_{ON} versus V_{IN} with a constant supply voltage V_{CC}. As the supply voltage (V_{CC}) is decreased, the value of R_{ON} gets larger; this is due to the input voltage being inversely proportional to R_{ON} (see Equation 1).

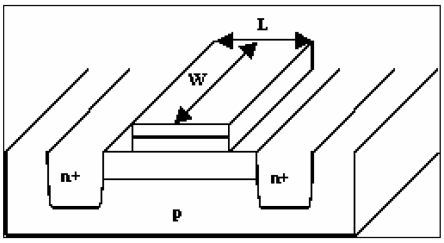

FIGURE 1. N-Channel MOSFET (NMOS)

NMOS-On Resistance vs. Input voltage (V_{CC} = 10V)

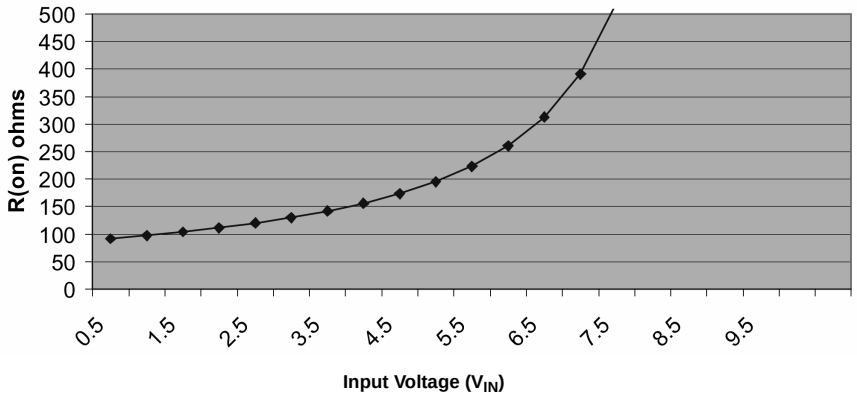

FIGURE 2. MOSFET R_{ON} Characteristics

NMOS-On Resistance vs. Input Voltage (V_{CC} = 5V)

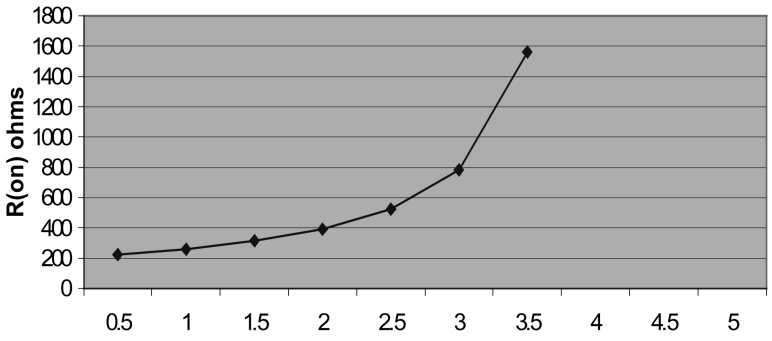

FIGURE 3. MOSFET R_{ON} Characteristics

In a pass gate configuration (see Fairchild Semiconductor Miscellaneous Document, MS-555, "Basic Analog and Digital Multiplexer Design Comparison") in order to keep R_{ON} to a minimum, the NMOS and PMOS transistors need to be matched. To match the two transistors the PMOS transistor needs to be approximately three times larger than the NMOS transistor. This is due to the PMOS's lower hole mobility (see explanation below).

Equation 2:

$\delta_n = qn\mu_n$

Equation 3:

$\delta_p = qn\mu_p$

Where:

δ_n = Electron conductivity

δ_p = Hole conductivity

q = Electron/hole change (p = q and n = –q)

n = Electrons/cm^3

p = Holes/cm^3

Assumption: Holes and electrons take up the same space.

In a matched PMOS/NMOS device there must be identical electrical behavior when discounting for the sign of the electrical currents and voltages.

Therefore:

$\delta_n = \delta_p$ and, $qn\mu_n = qp\mu_p$;

Therefore:

$p/n = \mu_n/\mu_p$

Where:

μ_p = 1350 cm^2/V-s

μ_n = 480 cm^2/V-s

p/n = 2.81 (Ratio of NMOS-to-PMOS)

With this increase in the PMOS gate region, an increase in the parasitic capacitance is a concern at high frequencies. In this situation, the gate oxide becomes an issue especially at high frequencies.

On Resistance Versus Input Voltage (V_{CC} = 10V)

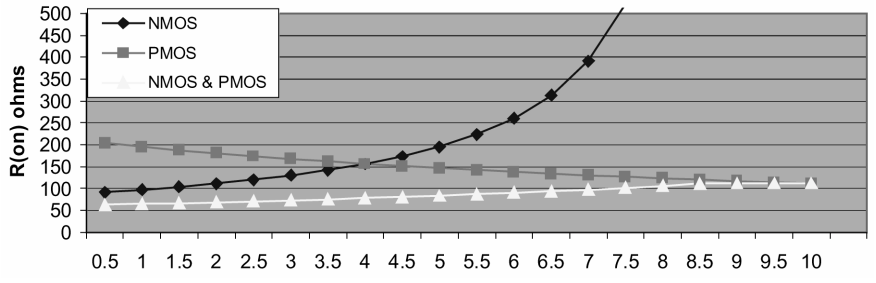

FIGURE 4. Pass Gate R_{ON} Characteristics

On Resistance Versus Input Voltage (V_{CC} = 5V)

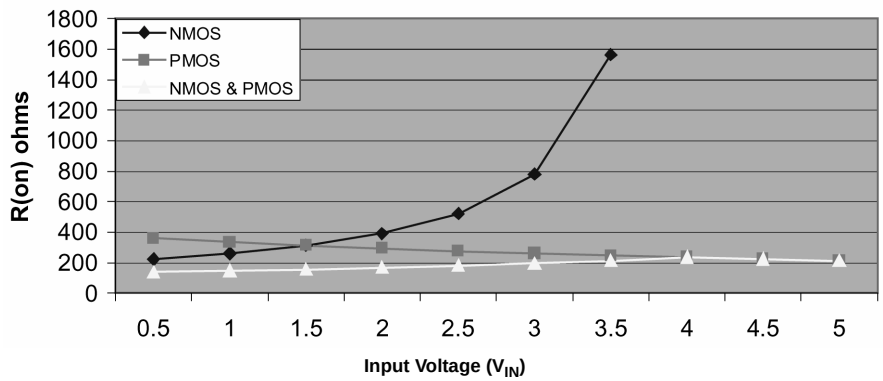

FIGURE 5. Pass Gate R_{ON} Characteristics

Figures 4, 5 show that the combination of the NMOS and PMOS yields a lower and a more constant R_{ON} value than either an NMOS or PMOS on its own (see Figures 2, 3).

R_{ON} is application specific. For low signal, high-speed applications, small R_{ON} is required to maintain the integrity of the input signal throughout the device. If the use is for audio, a low R_{ON} may not be as important due to the lower frequencies and power of the signal.

The source to substrate capacitance, the drain to substrate capacitance, and the source-to-drain Miller capacitance all have an effect on R_{ON}. As the frequency of the input signal increases, these capacitances can increase insertion loss and decrease off isolation. With R_{ON} being non-linear and a strong function of voltage and temperature; an analog switch should not be used in any critical resistive voltage divider path in a circuit.

If a MOSFET is being used for a power application as the source-to-drain voltage increases a larger source-to-drain breakdown voltage is required, therefore increasing the value of R_{ON}.

There are applications where R_{ON} is not a large concern, but there are others when it is. In order to design in a switch or any type of MOSFET device, a full understanding of the application is required.

Questions that need to be asked are:

- What frequency or frequencies will the device be operating at?
- What is the maximum amount of current the device will see?
- How important is termination?

As long as the designer understands his/her design requirements, the specifications given on the different FET devices will lead them to select the most appropriate device.