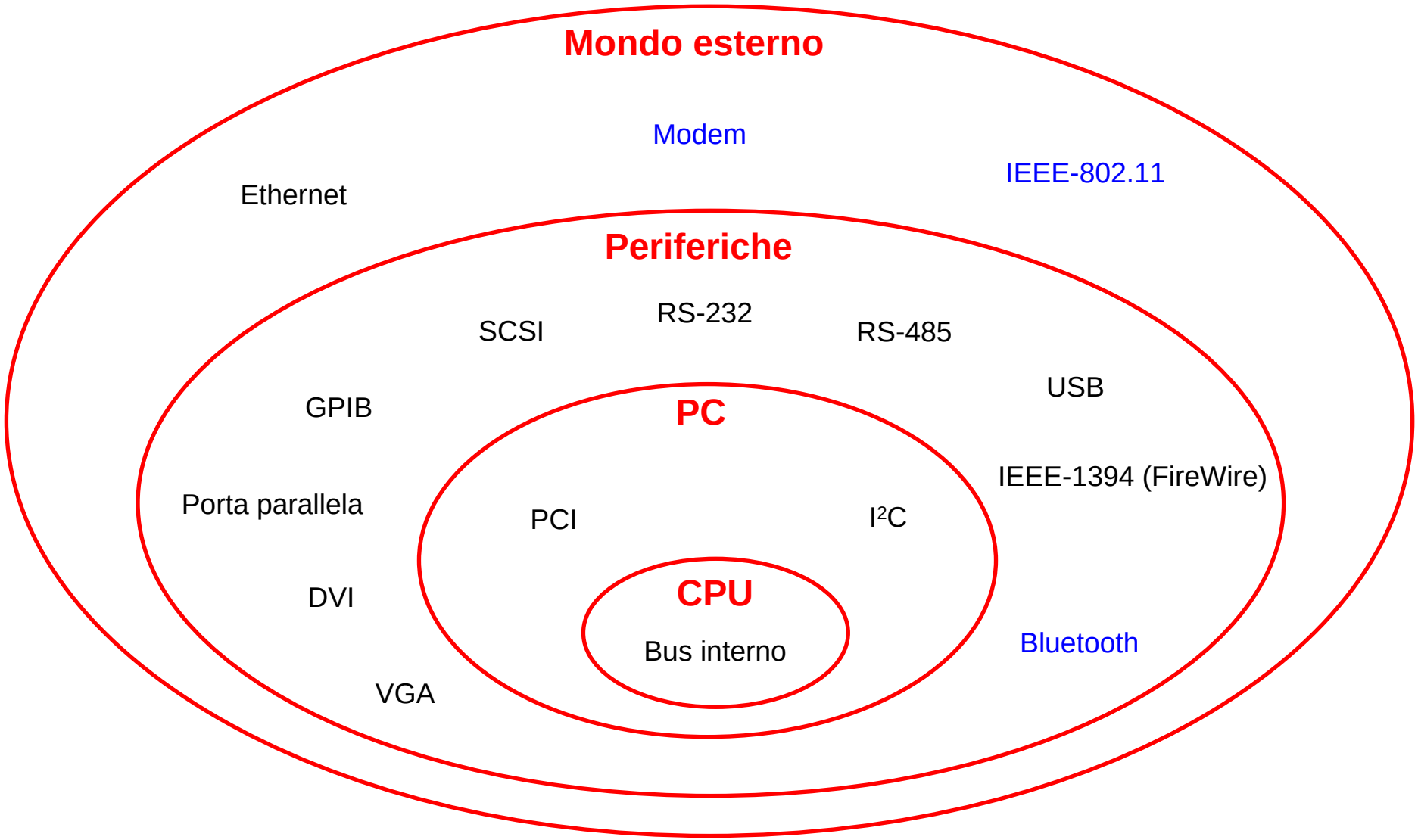
Facoltà d' Ingegneria
Dipartimento di Elettronica e Telecomunicazioni

Tecniche di interconnessione digitali

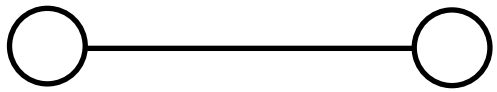
Massimiliano Pieraccini

Interconnessioni

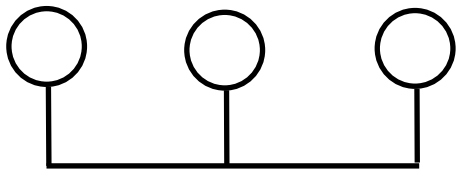


Topologie

- Punto-Punto

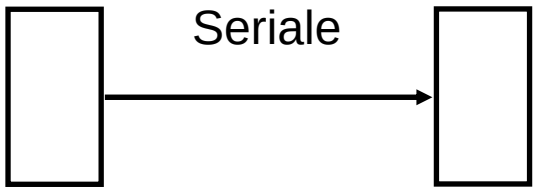


- Bus

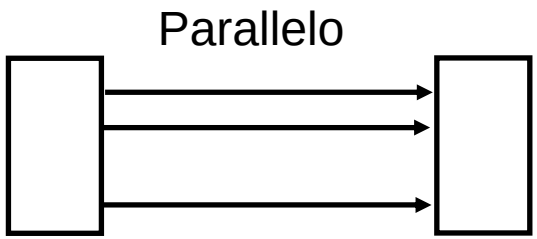


Le topologie ad **anello** o a **stella** si ottengono combinando più connessioni punto-punto

Seriale-parallelo

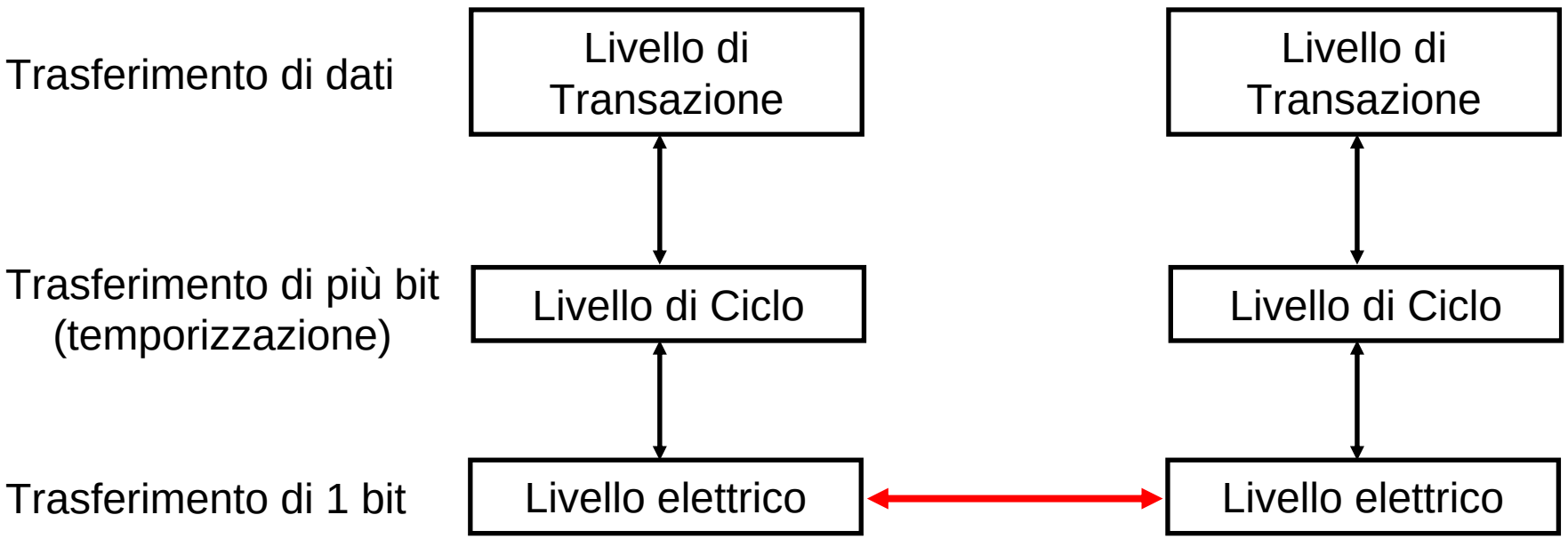


1 canale di informazioni

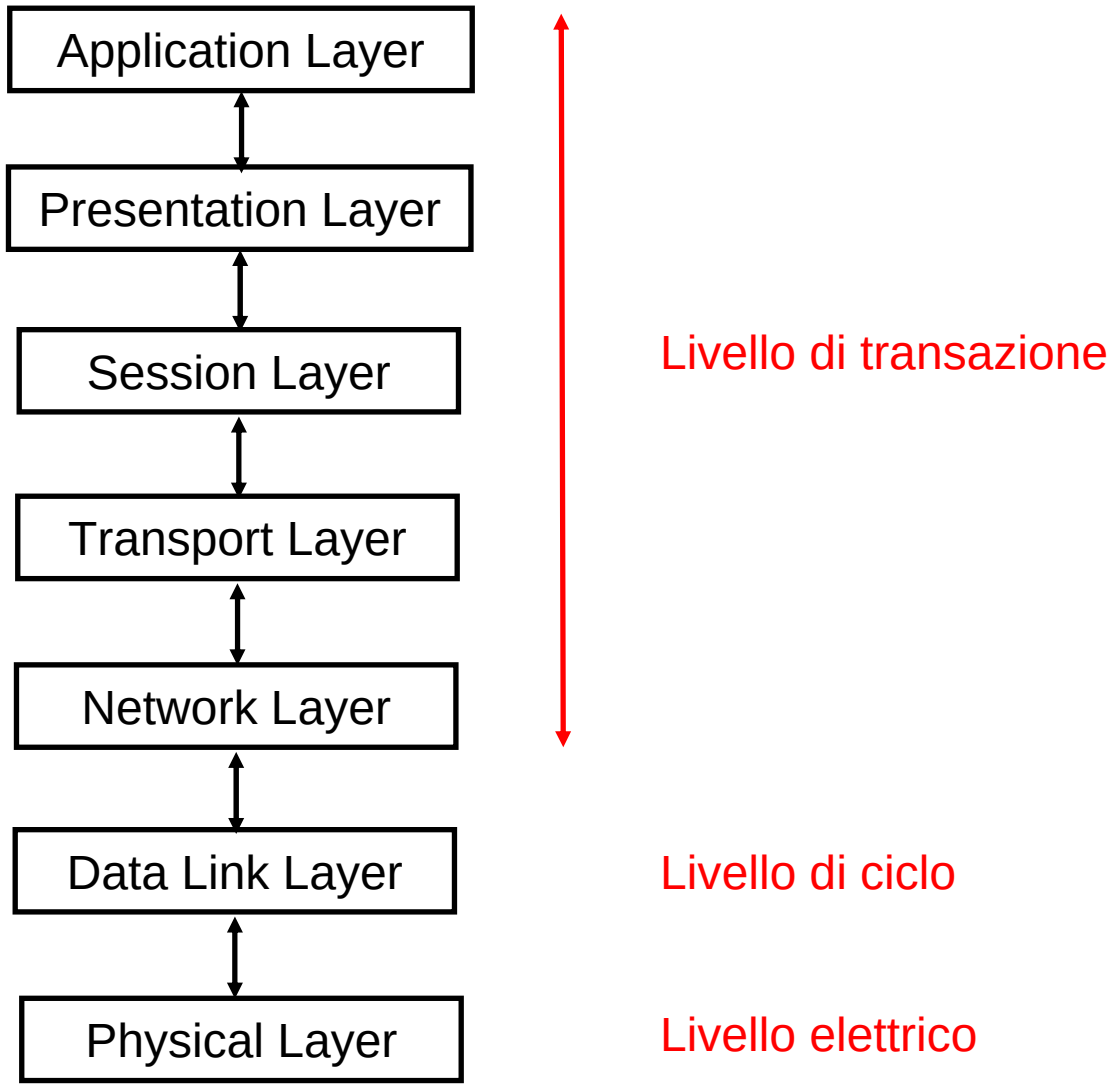


più di un canale di informazioni

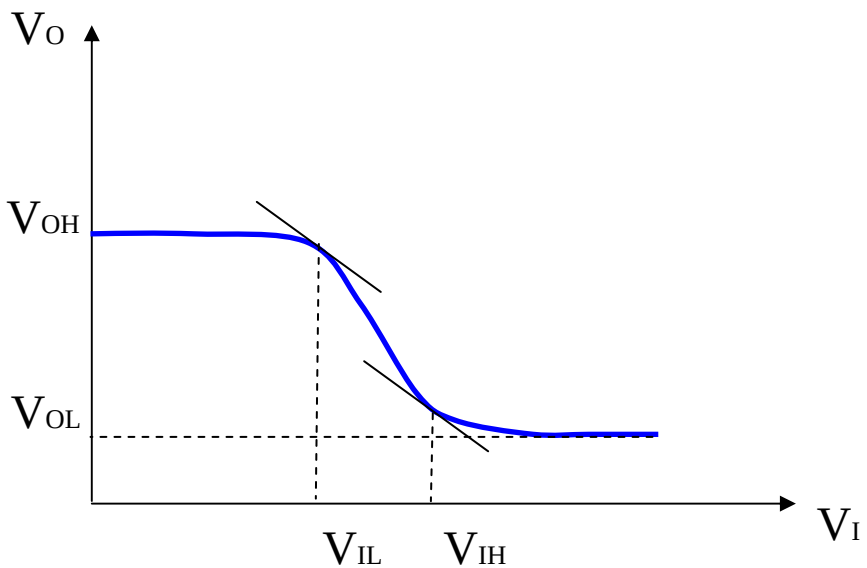
Modello a Strati



Modello OSI (Open System Interconnession)



Problema:
Se il trasmettitore trasmette un dato livello (ad esempio alto o basso) il ricevitore deve riconoscerlo

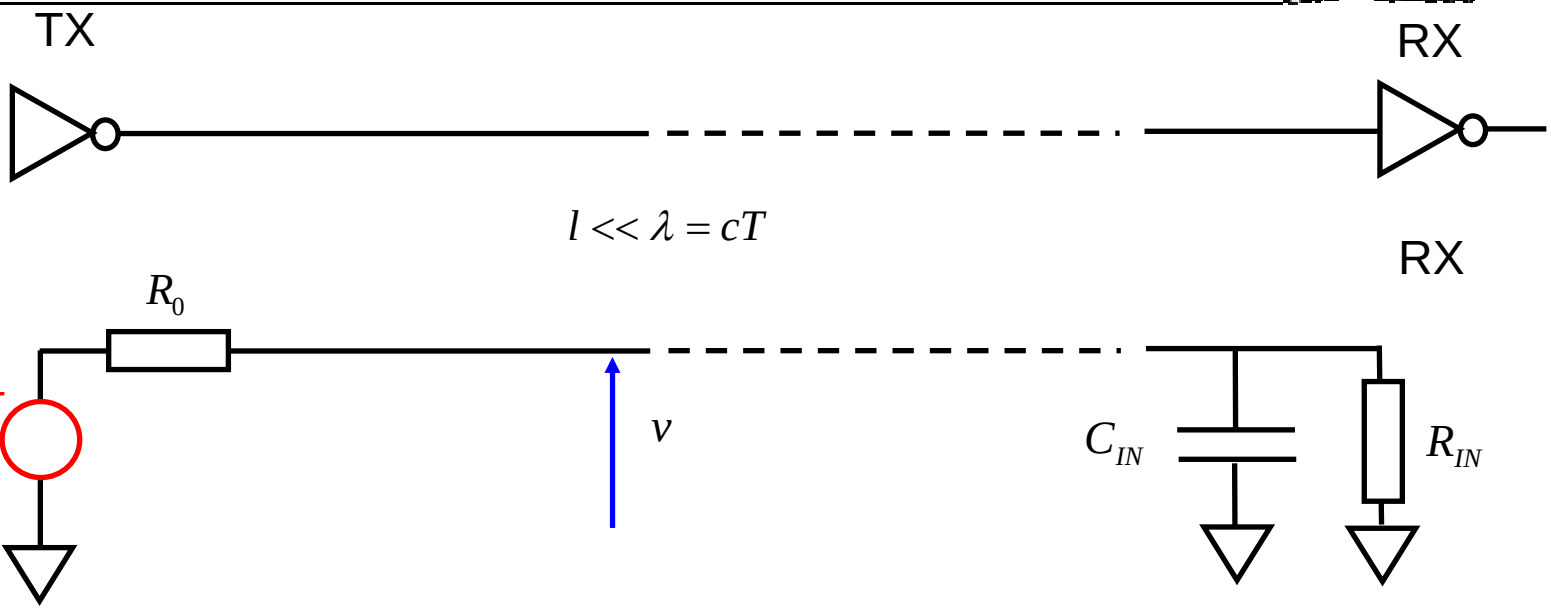


$$V_{OH} > V_{IH} \qquad NM_H = V_{OH} - V_{IH}$$

$$V_{OL} < V_{IL} \qquad NM_L = V_{IL} - V_{OL}$$

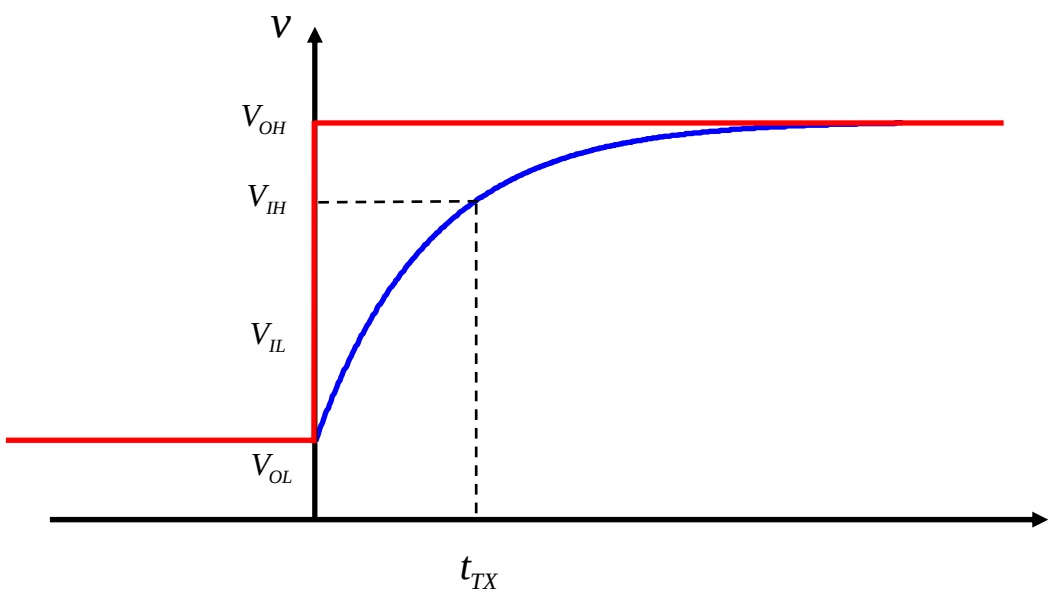
Margini di rumore

Livello elettrico

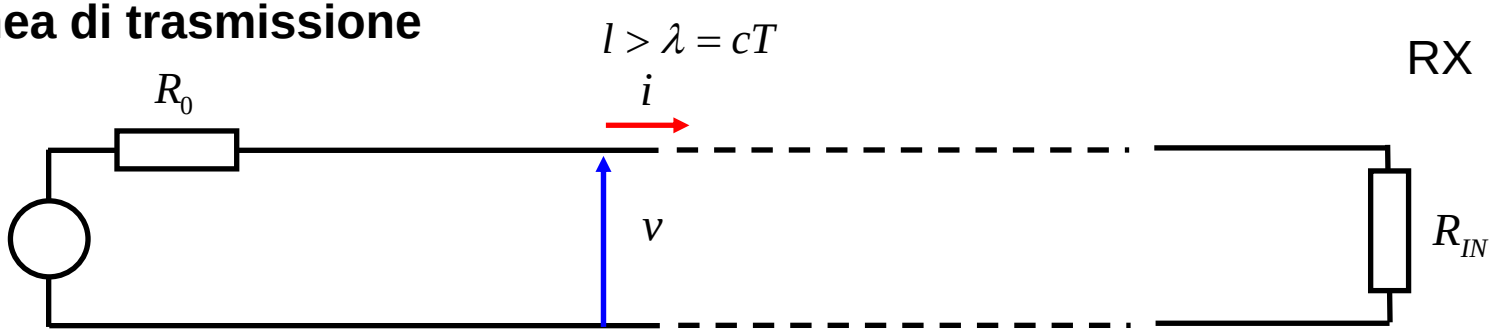


$$v = V_{OH} + (V_{OL} - V_{OH})e^{-\frac{t}{\tau}}$$

$$\tau = (R_0 \| R_{IN})C_{IN}$$



Linea di trasmissione



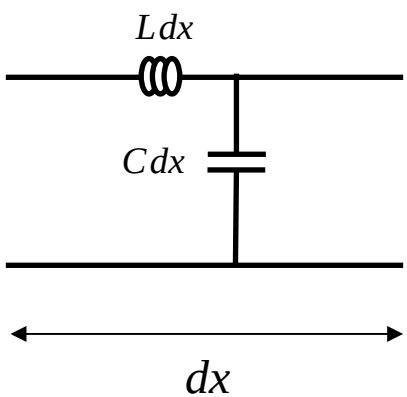
$$v = v_1\left(t - \frac{x}{c}\right) + v_2\left(t + \frac{x}{c}\right)$$

$$i = \frac{v_1\left(t - \frac{x}{c}\right) + v_2\left(t + \frac{x}{c}\right)}{Z_0}$$

$$c = \frac{1}{\sqrt{LC}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

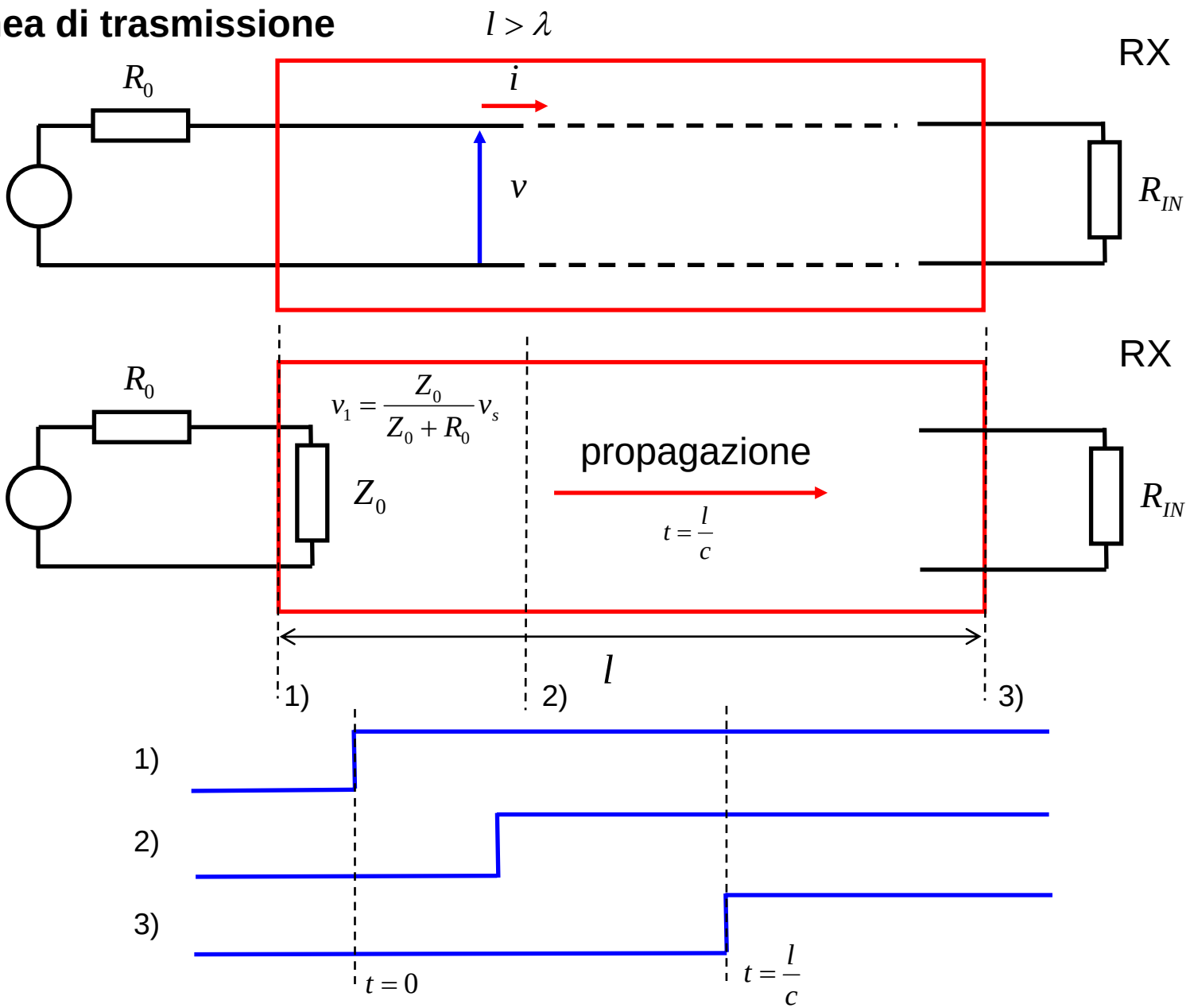
$$Z_0 = 20 - 200\Omega$$



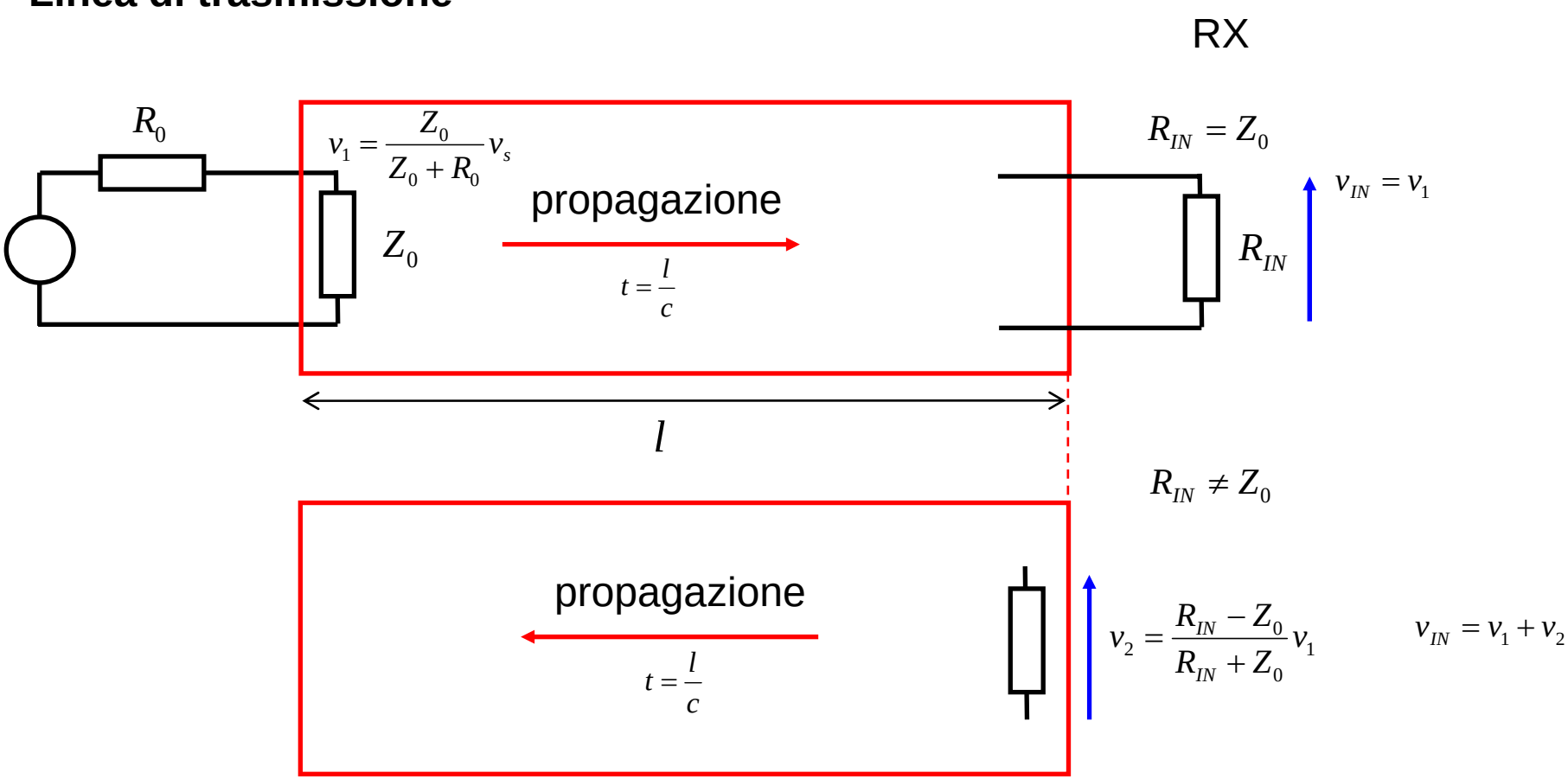
Lunghezza critica

Famiglia	Tempo di transizione (ns)	Lunghezza critica (mm)
CMOS	15	100
HCMOS	6	40
ACMOS	4	27
TTL-LS/ALS/S	3	20
TTL-AS	1.2	10
BiCMOS	0.7	5
ECL 100K	0.5	3
Logiche GaAs	0.15	1

Linea di trasmissione



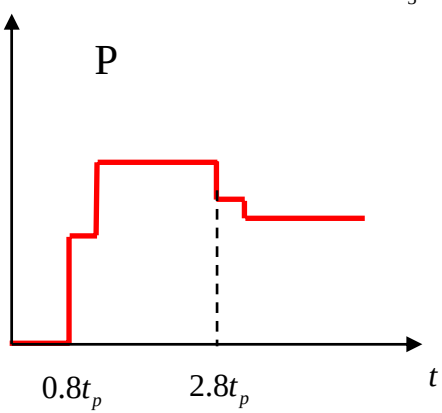
Linea di trasmissione



$$\Gamma = \frac{R_{IN} - Z_0}{R_{IN} + Z_0}$$

Linea di trasmissione

$$t_p = \frac{l}{c}$$



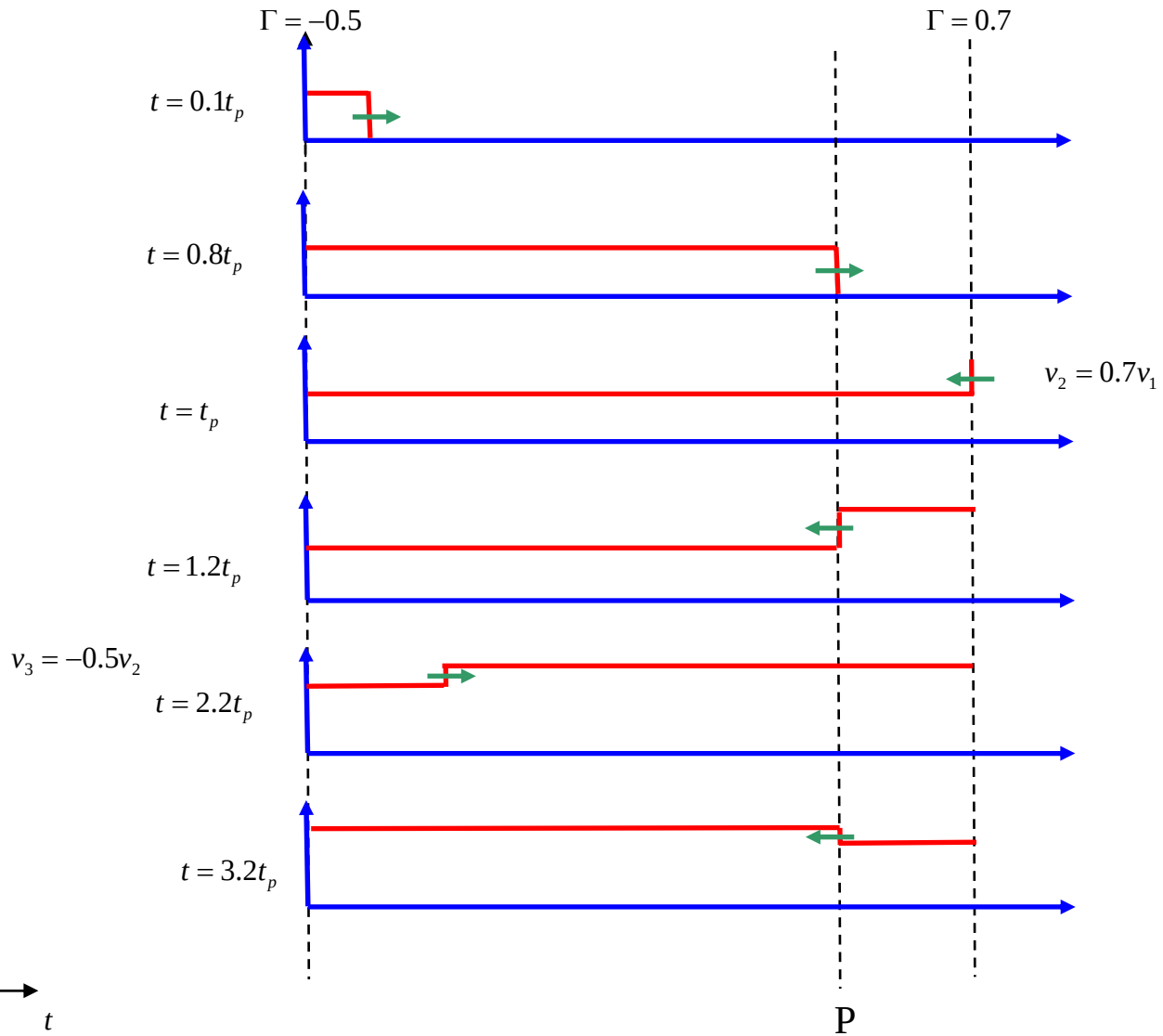


Diagramma di Bergeron

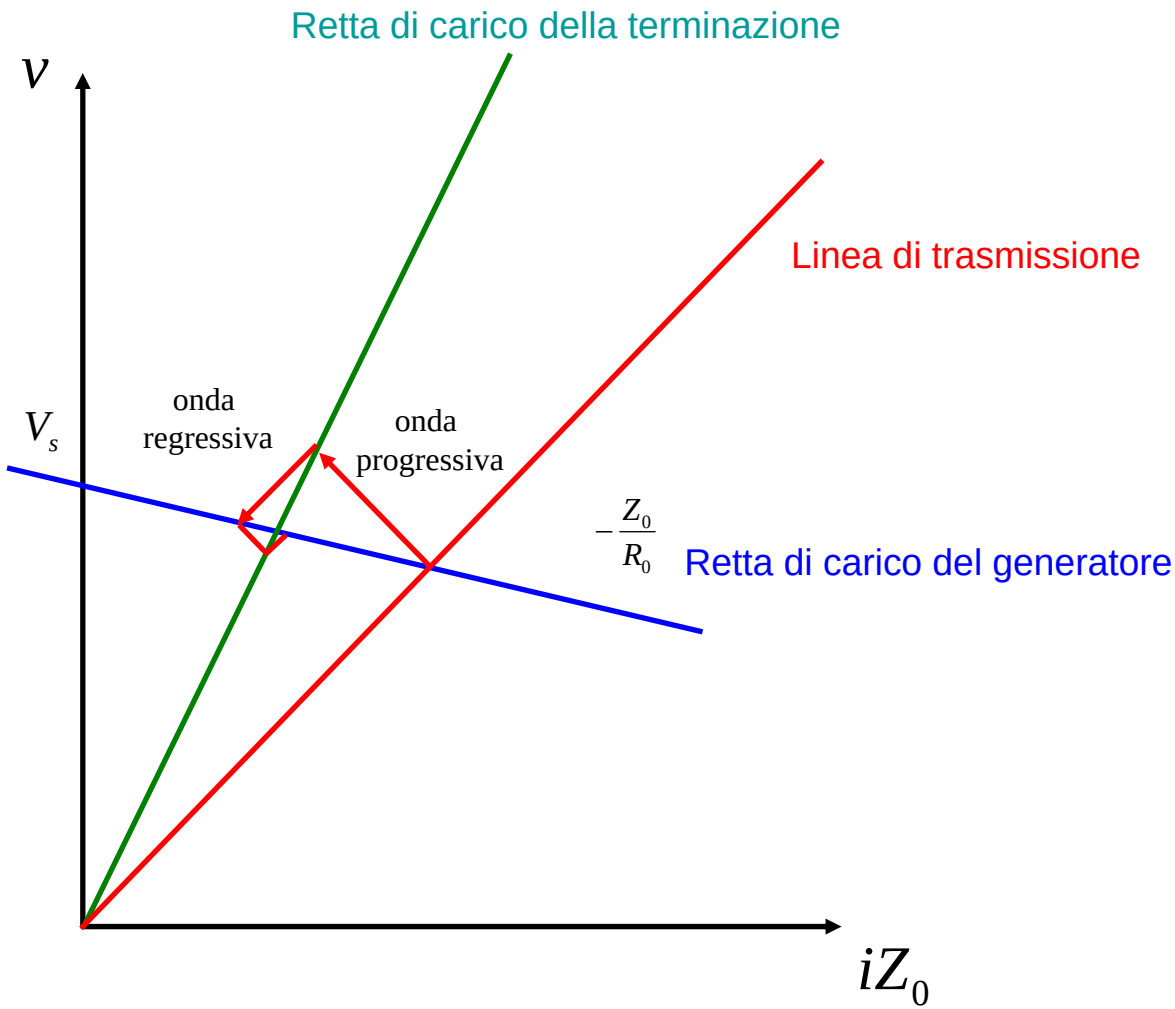


Diagramma di Bergeron

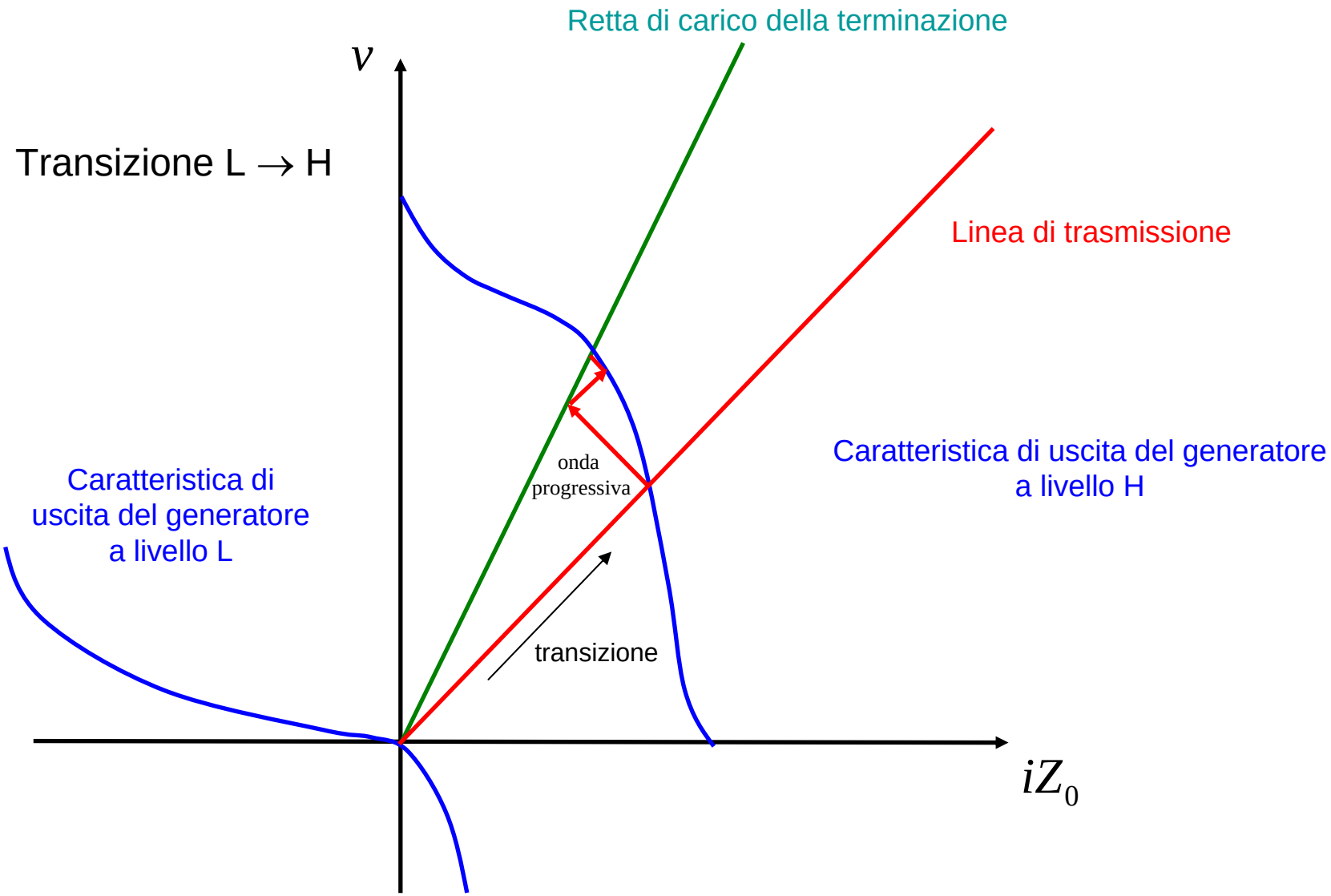
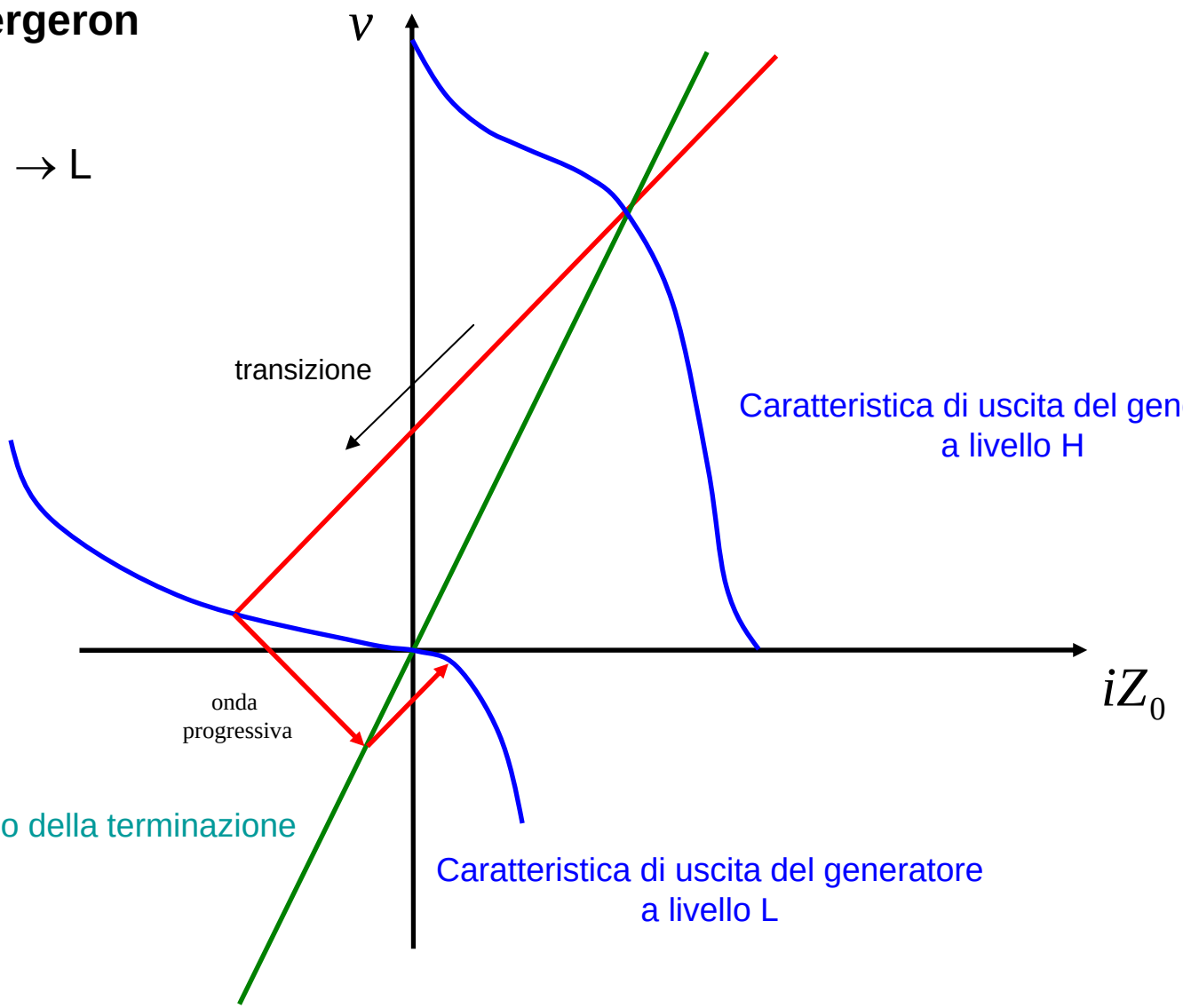
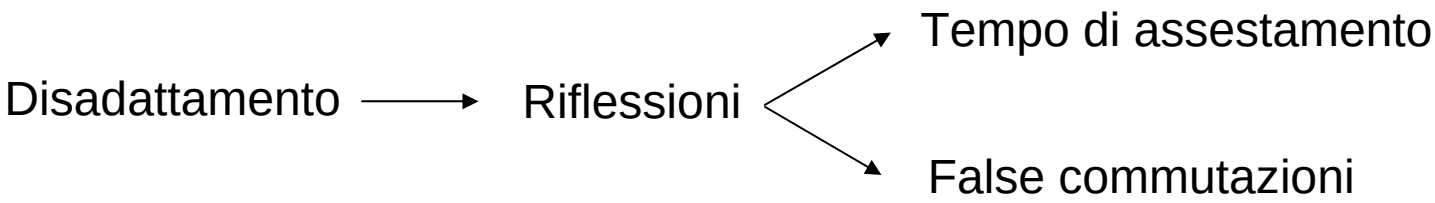


Diagramma di Bergeron

Transizione H $\rightarrow$ L



Diodi clamp in RX



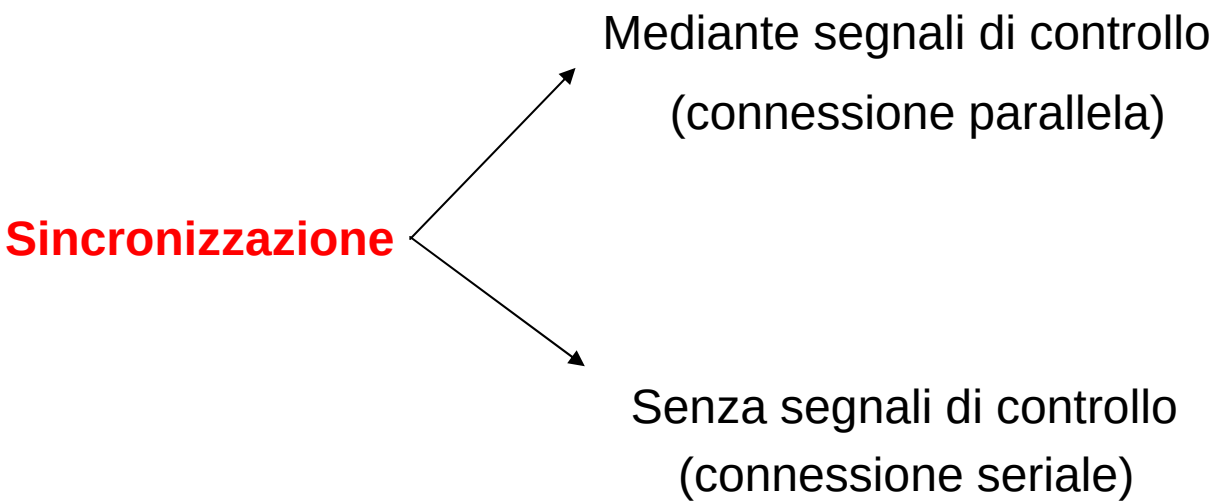
Terminazione adatattata:
- Nessun problema di riflessioni
- Consumo (anche in condizioni statiche)

Terminazione ad alta impedenza:
- Riflessioni
- Basso consumo (nullo in condizioni statiche)

Problema:
Se il ricevitore deve leggere il segnale, quando il segnale è valido e NON durante le transizioni

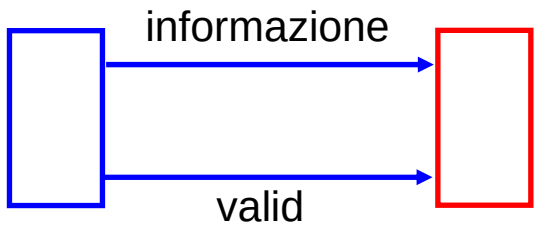
↓

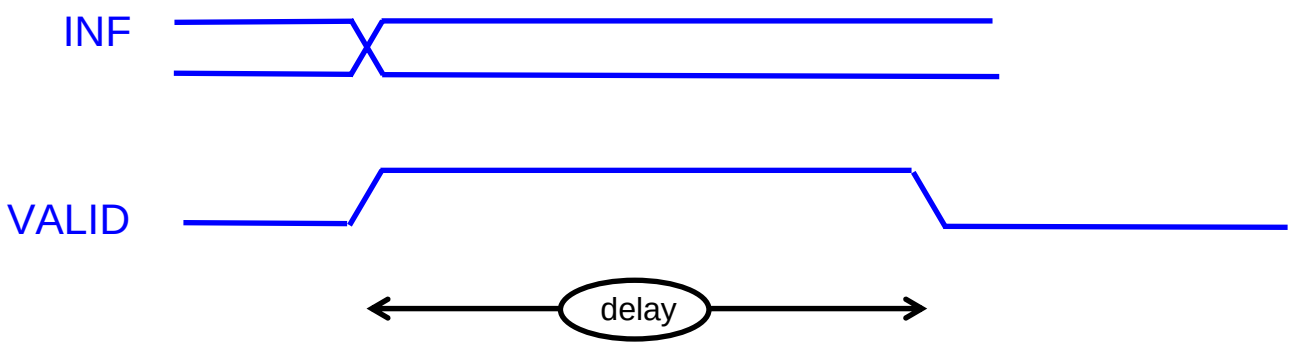
Sincronizzazione



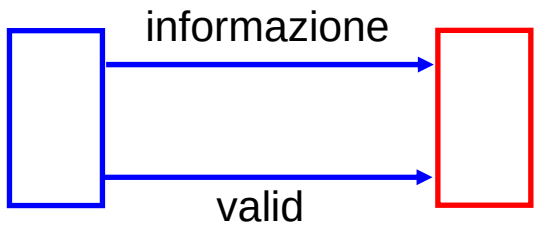
Nota: la connessione può essere parallela ma la comunicazione seriale (protocollo seriale)

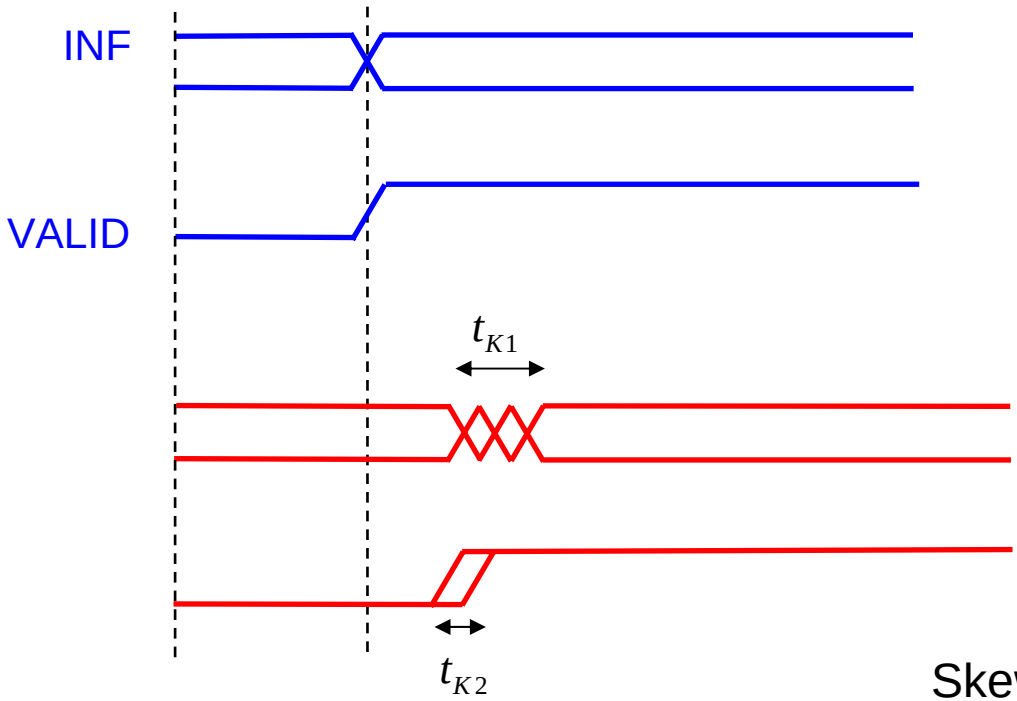
Punto-Punto





Punto-Punto



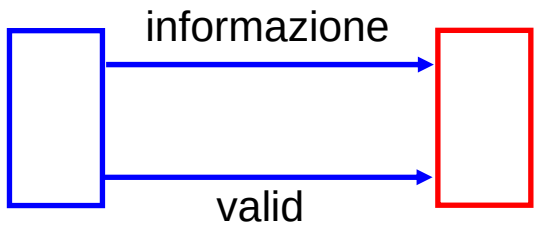


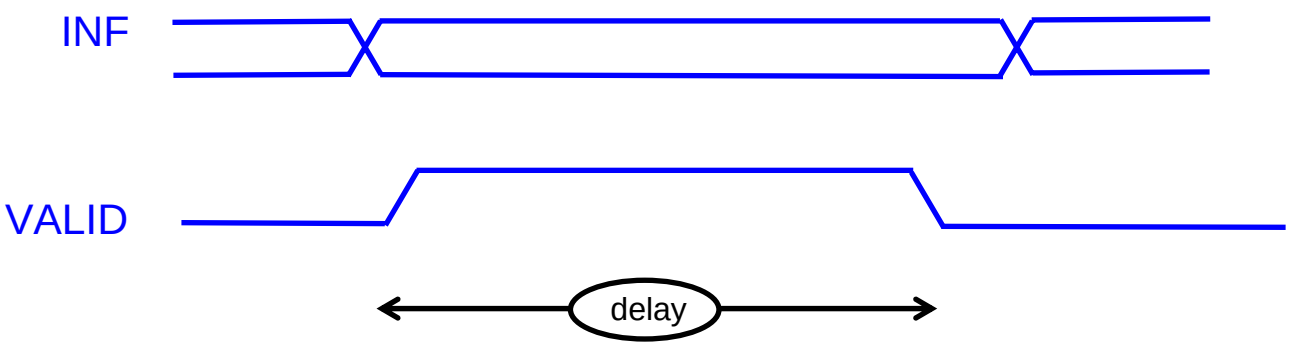
Skew: $\frac{t_{K1}}{2} + \frac{t_{K2}}{2}$

Deskew al TX: inserire un ritardo tra INF e VALID
Deskew al RX: inserire un ritardo dopo il segnale di VALID prima di acquisire

Punto-Punto

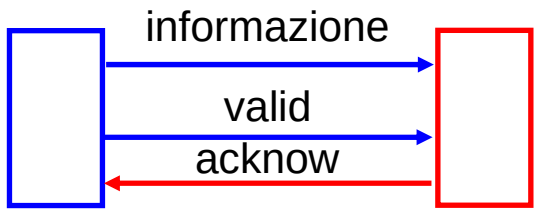
SINCRONO

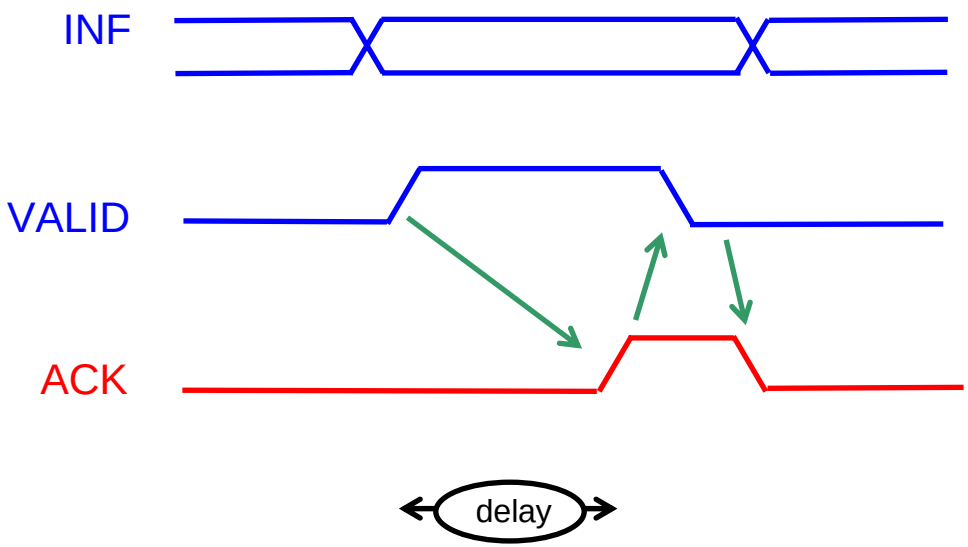




Punto-Punto

ASINCRONO

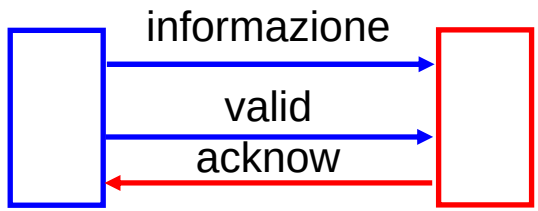


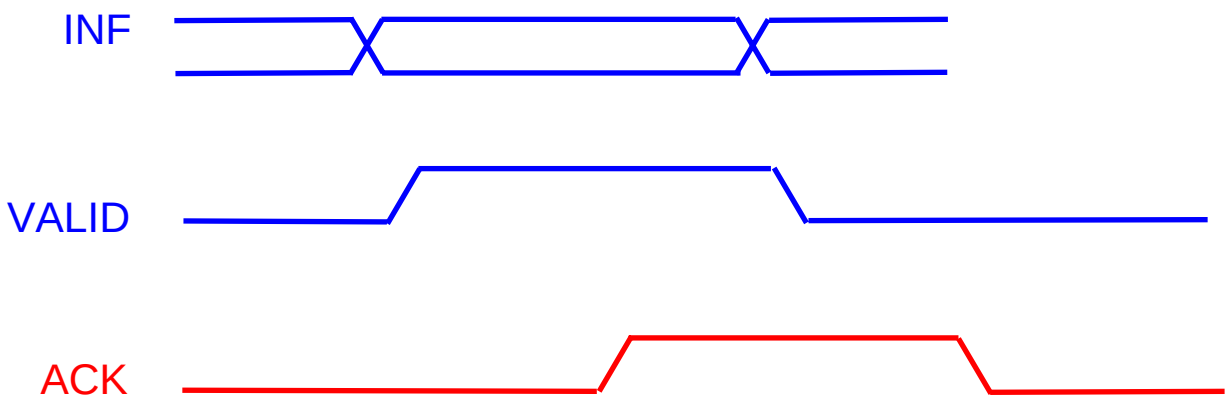


Punto-Punto

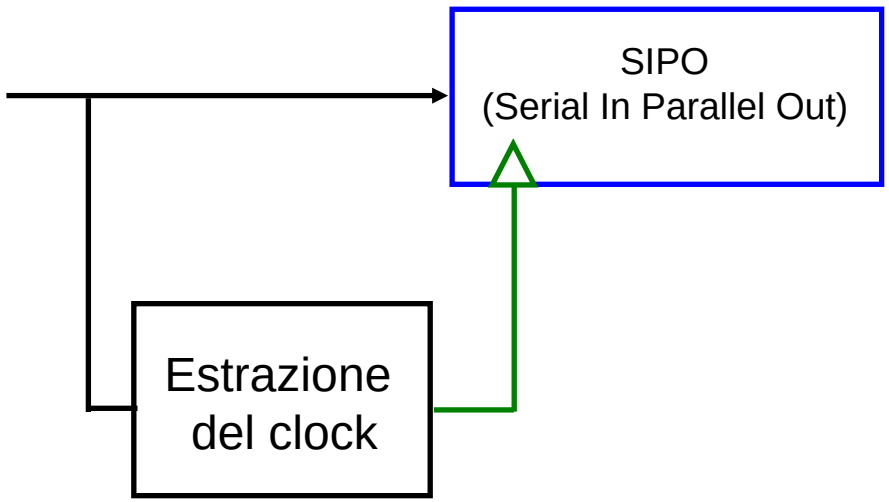
ASINCRONO

DDR: Double Data Rate

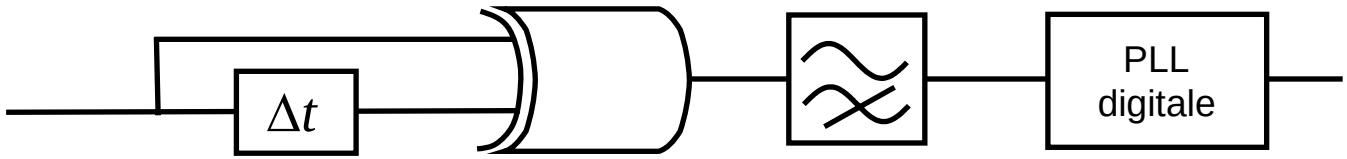


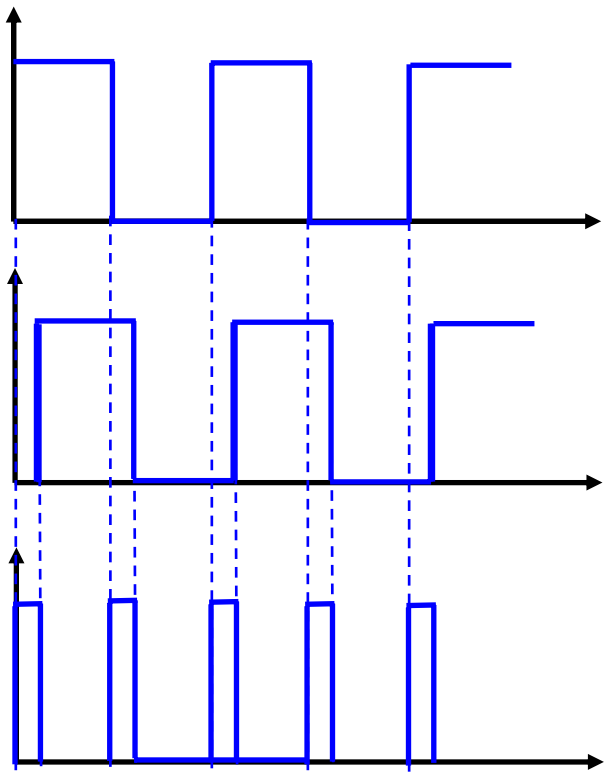


Protocolli seriali sincroni



Ricostruzione del clock





0 1 0 1 0 1 Massima frequenza

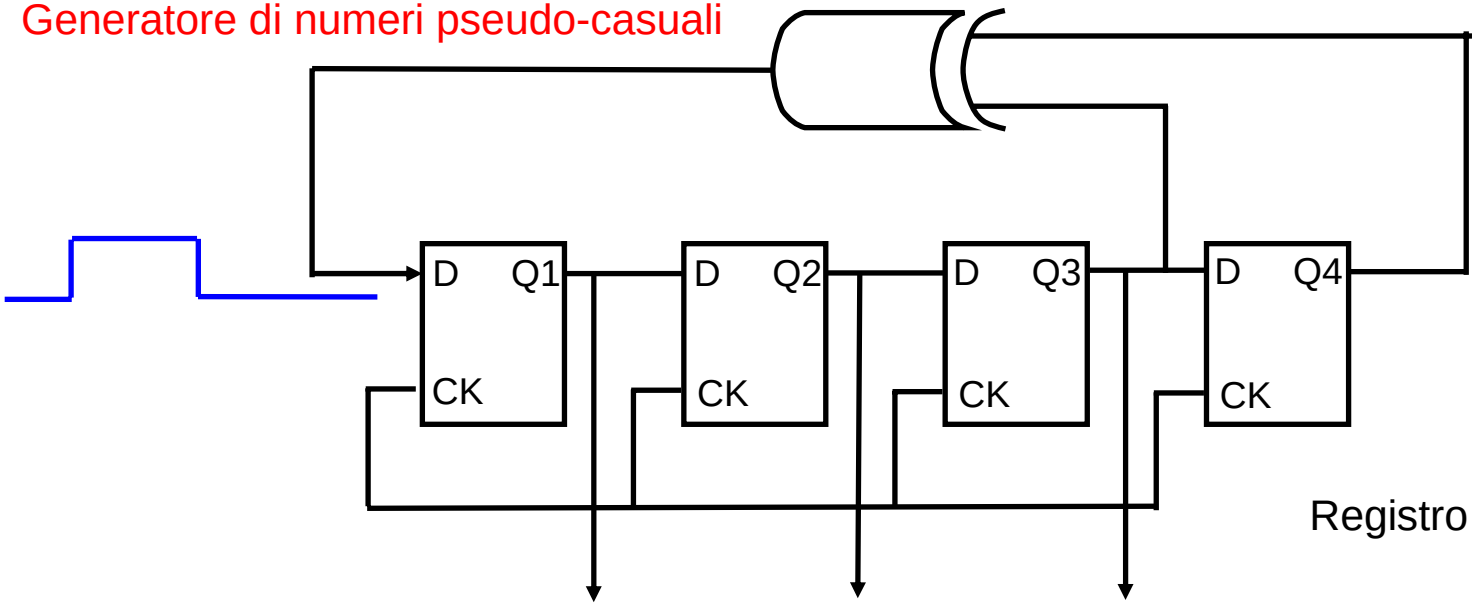
0 1 0 0 0 1 Componenti a più bassa frequenza

Bit stuffing

Ogni cinque “1” è inserito un “0”
(Il RX è programmato per ignorare il bit dopo 5 “1” consecutivi)

Bit scrambling

Generatore di numeri pseudo-casuali

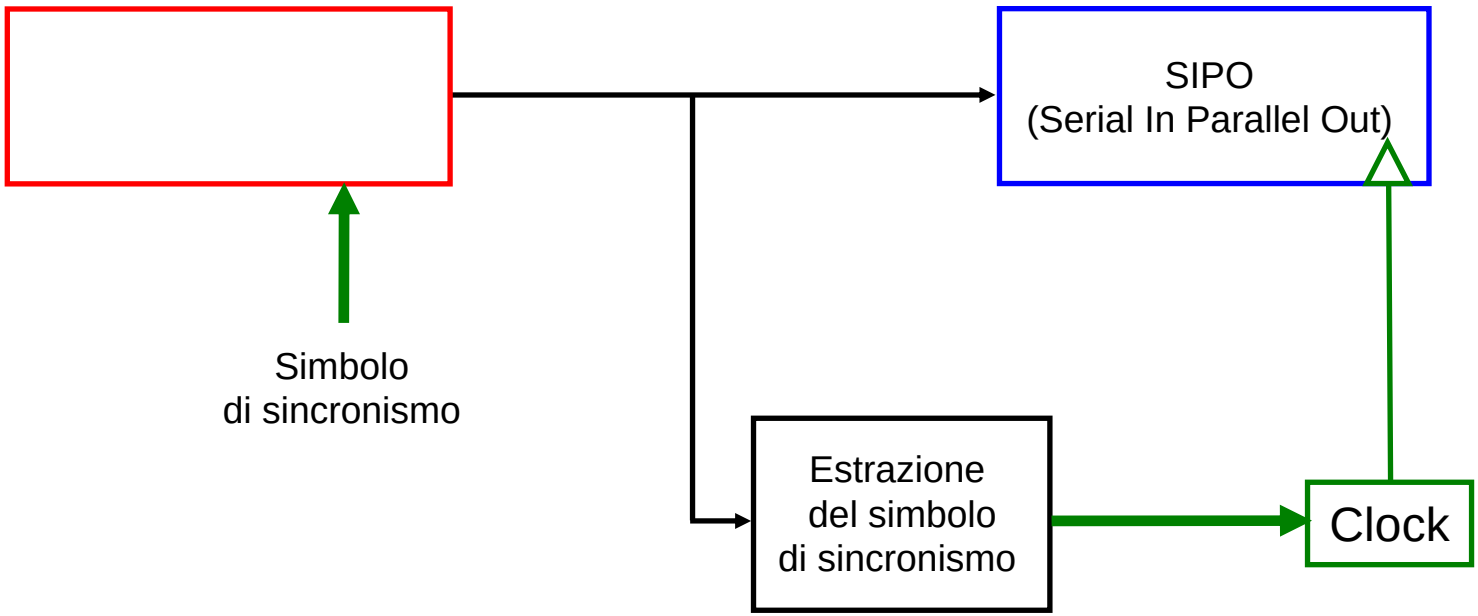


Registro a scorrimento

MLS (Maximum Lenght Sequence) = $2^N - 1$

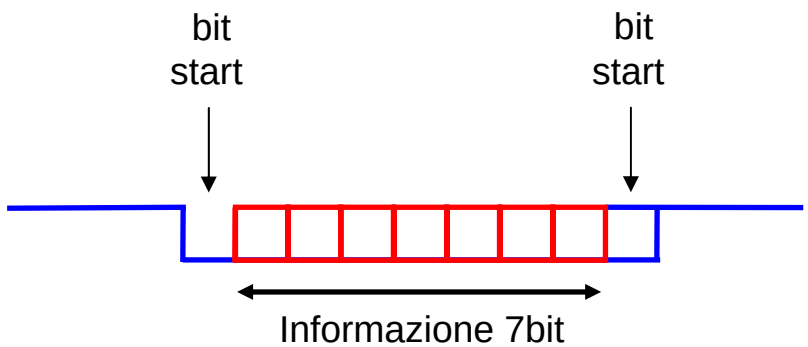
Nota: la funzione logica della rete di reazione dipende dal numero di bit

Protocolli seriali asincroni



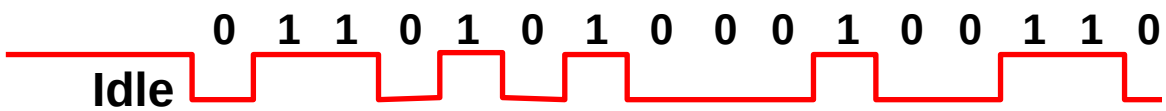
Protocolli seriali asincroni

Esempio: RS-232

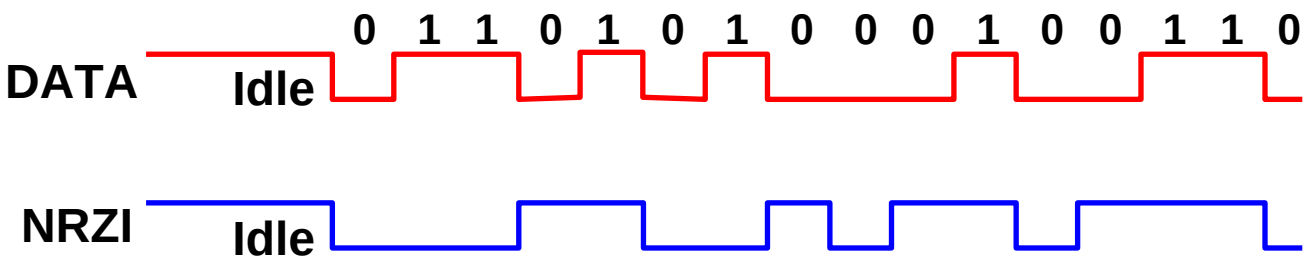


Codici

NRZ-L (Non Return Zero – Level)



NRZI = Non Return to Zero Invert

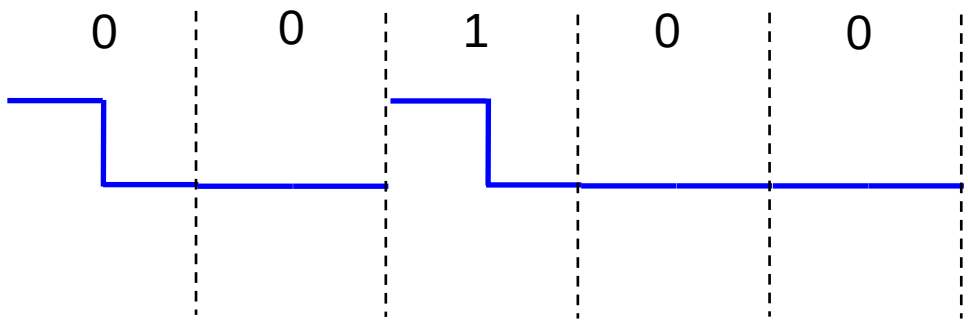


Cambia ogni volta che trova uno zero

Bit stuffing

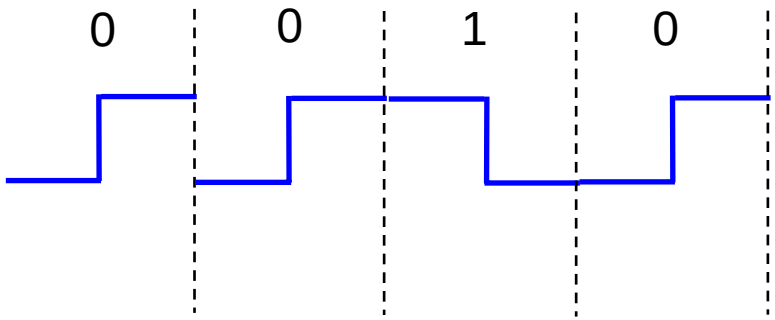
Codici

RZ (Return Zero)

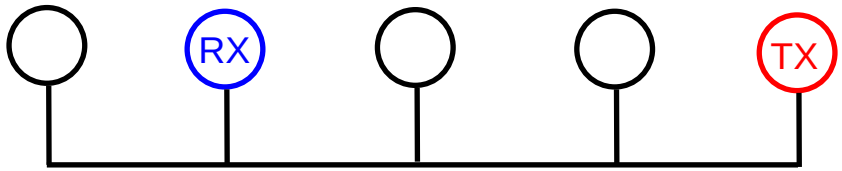


Codici

Codici autosincronizzanti



Manchester



TX

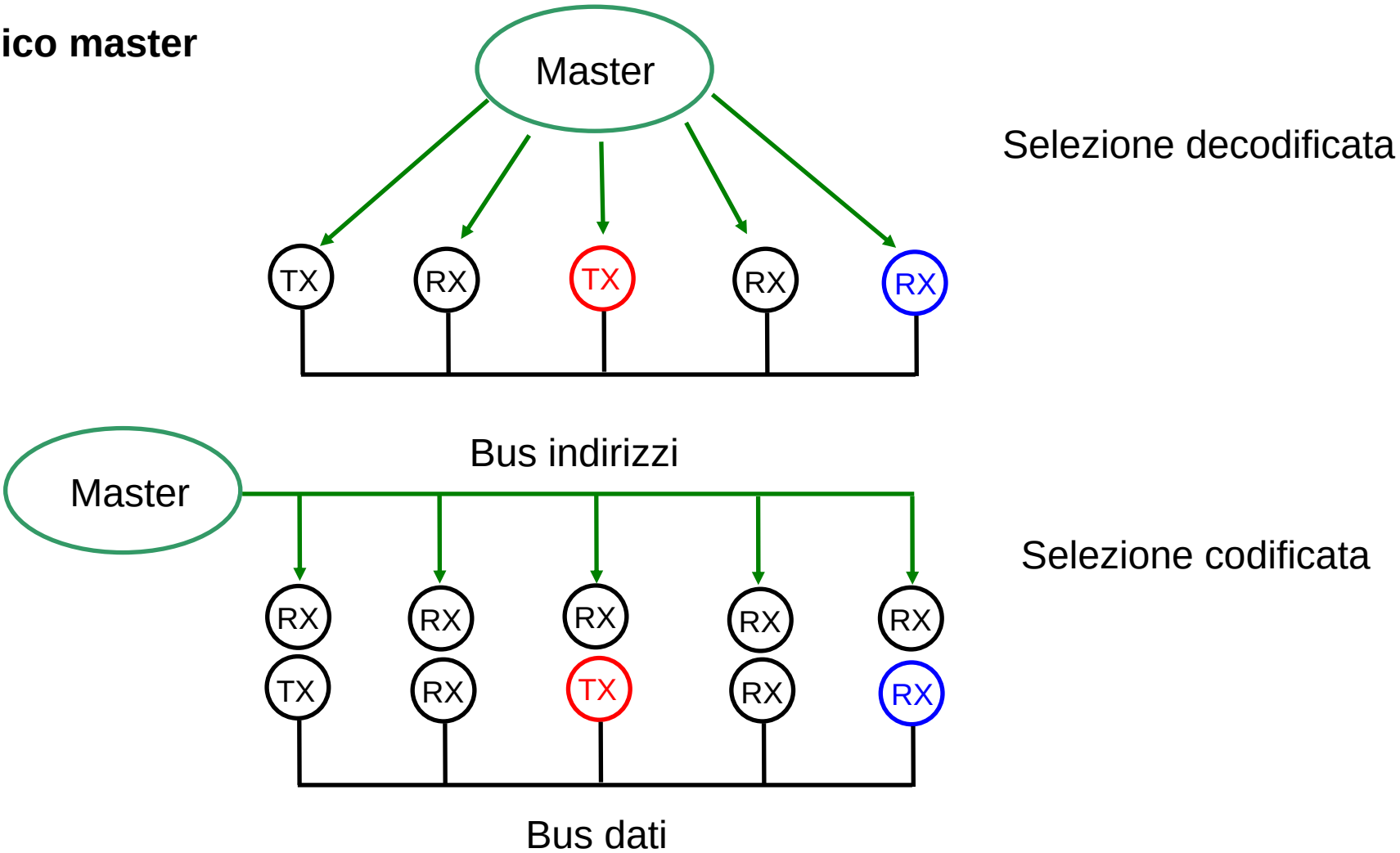
RX

Master

Slave

1) Unico master
2) Più master (arbitraggio)

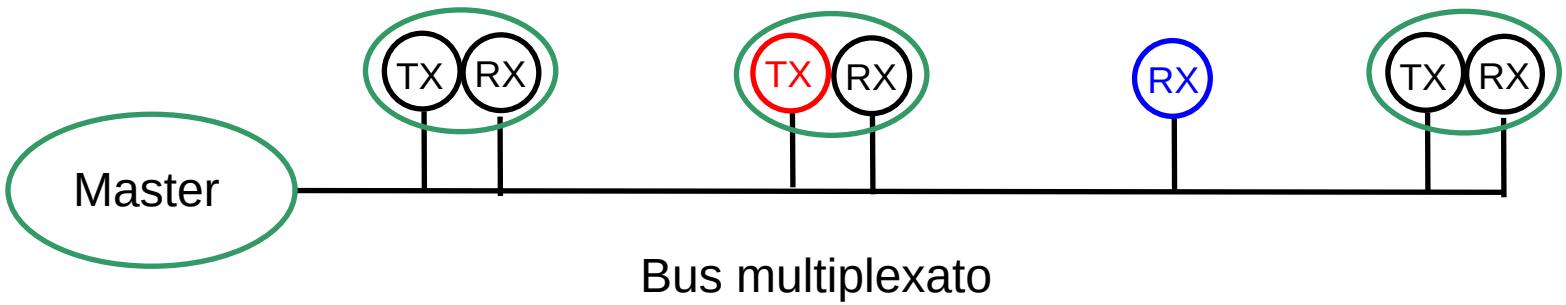
Unico master



Nota: ogni transazione è costituita da 2 indirizzi in rapida successione e quindi la transazione nel bus dati

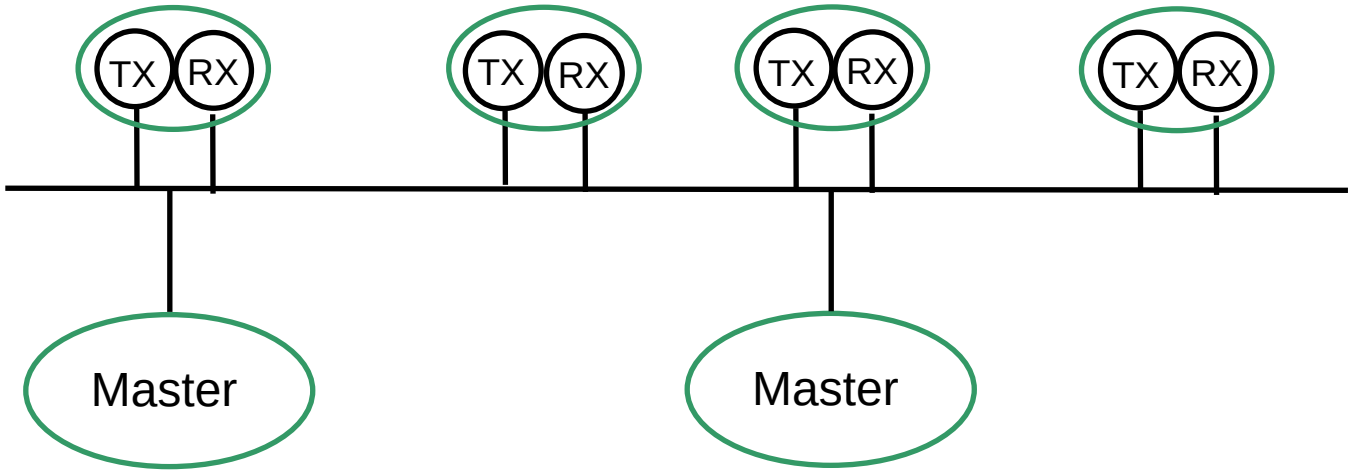
Transazione a burst: 2 indirizzi, incrementi

Unico master

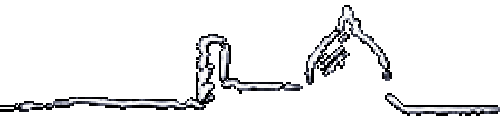


Bus multiplexato

Più master



Protocollo di arbitraggio



PCI	comunicazione parallela	bus
Porta parallela	comunicazione parallela	porta
GPIB	comunicazione parallela	bus
VGA-DVI	comunicazione parallela	porta
SCSI	comunicazione parallela	bus
RS232	comunicazione seriale	porta
I2C	comunicazione seriale	bus
USB	comunicazione seriale	bus
FireWire	comunicazione seriale	bus
Ethernet	comunicazione seriale	bus