MINIATURE PAGER WITH NOVEL RECEIVER ON-A-CHIP

Ian A.W. Vance
Standard Telecommunication Labs. Ltd.
London Road, Harlow, Essex, England.

Abstract

A new miniature pager is described which employs a completely integrated vhf receiver. The radio system is described together with the other component parts of the pager. It is shown that a substantial size reduction has been made whilst keeping full wide-area specifications.

Introduction

In recent years great advances have been made in mobile voice communications but wide-area paging remains today the lowest cost way of communicating with a mobile person. It thus brings the benefits of such communication in terms of efficient use of time and resources to a wide population and for many is the first contact with the radio communication business. Furthermore it utilises the scarce resource of the radio spectrum in a very efficient manner. For this reason, demand for paging is high resulting in operating companies and administrations seeking ways to achieve more users per channel available to them. Digital codes have replaced tone systems and high capacity central controllers with combined simul-cast and sequential transmitters are commonplace. In this environment the market for pagers is one characterised by increasing volume, reducing prices and greater attention to technical performance.

This paper describes a new radiopager which utilises the latest technology to meet the challenge of this market: the first pager to use the new 'POCSAG' code (now CCIR radiopaging code No. 1) and the first pager to have the entire radio receiver made on a single silicon chip.

An overall description of the pager is given followed by a detailed consideration of the new receiver circuit and its characteristics.

Figure 1 Miniature Radiopager

Overall Pager Design

The most important feature of the new pager overall is its small size, as shown in figure one. At 97 by 42 by 14 mm it is truly a miniature device and in particular the slimness makes it more attractive to the end-user. This small physical volume is achieved by the use of large scale integration; two custom designed chips comprise almost all the active electronics. Figure 2 shows the configuration of the circuitry. A loop antenna provides the input signal to the first integrated circuit which is a bipolar chip containing the receiver functions. The output of this chip is the demodulated data signal after filtering and slicing, which is input to the second chip. This low threshold CMOS circuit contains the data decoder for all four addresses which are available, together with circuitry to generate the output 'bleep' cadences. All addresses can be stored in memory mode and are programmed into each unit with a fusible-link diode matrix PROM. All timing functions associated with the data at 512 bit/s are controlled by a 32768 Hz watch crystal.

The low component count made possible with this integrated approach allows a conventional single printed board assembly to be used.

RF Circuitry

Radio receiver design is, in electronic engineering terms, an old established art and so it is particularly interesting that the receiver for this pager uses a new demodulation circuit.

Figure 3 shows the internal circuit blocks of the radio chip. A direct conversion principle is used (Ref. 1, 2) and the input signals from the antenna, after amplification are split into two quadrature paths with an off-chip 90° hybrid as shown. The local oscillator is on the same frequency as the channel to be received and is derived for the two metre band by tripling from a crystal oscillator in the 50 MHz region. This enables a ruggedised crystal to be employed capable of surviving the multiple drop-testing performed by the average

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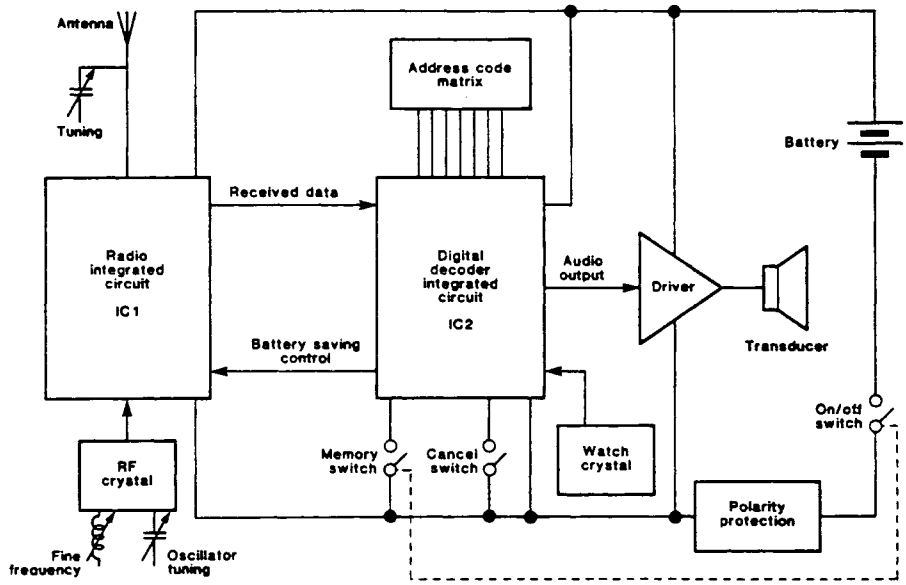

Figure 2 Pager block diagram

pager user! The frequency shift keyed r.f. signal in its two paths is mixed with this local oscillator in two balanced mixers and the output low-pass filtered. In a 25 kHz channel spacing system using plus and minus 4.5 kHz deviation the low pass filters have a corner at about 7 kHz to allow for oscillator drift and transmitter tolerances.

The filtered i.f. signal, which is the difference between the input and the oscillator, is limited in both channels and the demodulation consists of recognising the relative sign of the quadrature phase shift. Since the signal moves from one side of the oscillator frequency to the other as it changes from mark to space this lead or lag condition signifies a data one or zero. In its simplest form the demodulator can be made with D-type flip-flops as shown. This type of discriminator has a noise spectrum which falls rapidly with post detection frequency due to the 'sample and hold' nature of the flip-flop. Hence a simple data filter suffices and the chip is completed with a slicing circuit as indicated. The current to the chip is switchable externally.

This new type of receiver has numerous advantages over the conventional double superheterodyne. Most obviously the image response associated with each conversion is eliminated thus removing any need for sharply tuned high frequency circuits. Secondly, the main gain is at audio frequencies which makes it feasible from a stability point of view to have the entire receiver, with inputs and outputs only one tenth of an inch apart, on one chip. With an input sensitivity below 0.1 μV there is more than 150 dB of gain between these points. The low-frequency operation required of most of the circuit also minimises power consumption.

Another useful benefit is that the pre-detection noise bandwidth can be reduced by tailoring the filter to match the spectrum of the signal. Adding a high-pass section to the low-pass channel filters creates a notch in the centre of the equivalent r.f. channel; this matches the wide deviation fsk spectrum and eliminates unnecessary noise.

Also of direct relevance is the fact that the next channel rejection is infinite. Correctly modulated signals are not demodulated since they fail to cross the local oscillator frequency. The channel filters ensure good blocking performance for the adjacent channel.

All of these features make it possible to meet the necessary performance criteria for wide-area radiopagers using the approach outlined above and to do so with the other benefits of small size and greater reliability.

Data Decoding

The digital decoder is also fully integrated and uses the 'POCSAG' code. This has been described in detail elsewhere (Ref. 3) and is being widely adopted for new systems and as a capacity update for existing networks.

Briefly, the code achieves a calling rate of some 16 a second at a 512 bit/second transmission rate. The total capacity is in excess of two million subscribers. A particularly useful feature is that the transmissions are divided into 8 time slots and any individual pager's code defines one of these, as well as the transmitted addresses. Hence even on a heavily loaded system battery saving can be employed to good effect.

In the implementation used here the address code and the system synchronisation word are stored external to the chip in a diode matrix fusible-link PROM. The chip generates the check bits required for the BCH error correction code and performs a comparison with the incoming data for four addresses, allowing two errors per received address word.

A digital bit synchronisation circuit is used to time the decoding and, to allow battery saving of the radio receiver a data detection circuit is

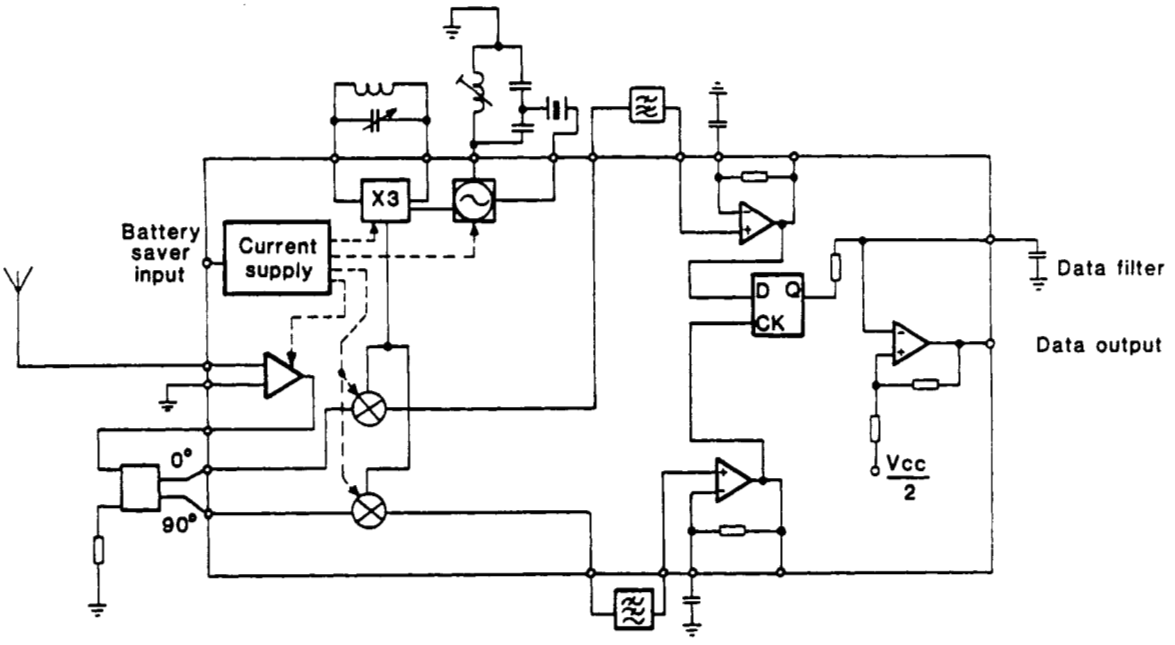

Figure 3 Receiver 1si configuration

employed. The design of these two items is a critical compromise such as to give maximum battery life whilst not impairing the overall sensitivity and at the same time achieving a probability of not correctly decoding on solid radio signals of better than one attempt in one million.

Successful decodes may be stored in memory mode and used to output an appropriate audio cadence. The audio output is also crystal controlled at 2048 Hz.

Miniature Pager Design

The totally integrated approach offers new possibilities in the ever-present trade-off between performance, cost, size and so on. In the present design it has been possible to substantially reduce the size over previous models whilst improving manufacturability. The small size, as well as enhancing the appeal of the product, makes the casework more rugged and this aspect is further improved by using a tubular one piece main case.

It is interesting to consider how far one can continue to reduce the size. The limiting factors are all the external interfaces - battery, antenna and acoustic output device. In each of these components a direct relationship exists between physical size and performance. It is to be expected that some slow progress will be made in batteries and possibly in new ferrites and ceramics such that a halving of dimensions might be seen. This would almost allow a 'credit-card' pager to be made, however until such advances in new materials become available, the unit presented here represents the current state of the art.

Conclusions

A new miniature pager has been described based on the application of 1si to radio via a new receiver architecture. This technique can be extended to other areas and we expect to find new applications for the technology.

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