MCM Technology
A Discussion Document

Brian Andrews
VeriBest International Limited

Contents

1. Introduction

There is a gradual and continuing technology move within the traditional PCB domain towards faster, lighter, denser designs that can deliver both improved performance and lower overall cost of end products. Multi Chip Modules (MCM's) were heralded as the technology vehicle that would realise the potential offered by new materials, advanced packaging and fine line production methods. The growth of MCM and the acceptance within global markets was predicted to boom over the course of the early 1990's, the reality was a somewhat more restrained growth curve. The investment required in new design techniques and manufacturing tooling has restricted many companies plans to implement new products within an MCM package. However, the underlying technological reasons for developing an MCM have not diminished. What has changed is that the huge leap required to convert from standard technology to MCM's has been broken down into more manageable steps that may be gradually introduced in a phased implementation plan.

The purpose of this paper is to explore some of the basics of MCM technology in order to help understand the markets that can benefit by implementing their products within an MCM package. Once a basic level of understanding has been reached, the fit of VeriBest CAD design tools for MCM design, and the markets that we address, will become apparent.

2. MCM Technology

2.1 What is an MCM?

An MCM can simply be described as a package containing two or more devices that need to be attached to a common substrate, are connected together with interconnect material and have some means for connection to an external circuit or assembly. MCM's utilise various traditional and new component attach methods that are discussed in **Section 3**.

Companies investing in MCM technology are doing so because they have recognised that their products need to reach new levels of performance. Simply stated, the shortest distance possible between device pins will result in less signal delay and higher performance from the system. However, as the speed increases the power requirements also rise. Given that the aim is to produce an assembly where the devices maintain very close proximity to each other in order to facilitate short interconnection, the designer is presented with problems that will require the use of analysis tools to help resolve the continual conflict between optimum performance and thermal management. The investment required for a solid, integrated EDA system is not trivial. Additionally, it is vital to have trained Engineers who understand the implications of correct MCM design.

2.2 Types of MCM

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) officially recognises three styles of MCM structures;

2.2.1 MCM Laminates (MCM-L)

Laminate MCM's are based on the traditional method of PCB manufacture. A sandwich of copper conductors and dielectric insulating material is built, etched, drilled and plated in order to provide the necessary layers of interconnect. The manufacturing process is primarily subtractive, i.e. the copper conducting material is etched away to leave the interconnect where necessary.

Recent advances allow for buried components to be incorporated within the laminate structure. Fixed value resistors, plate capacitors and inductors may be included by laminating and etching various materials during the fabrication process.

2.2.2 MCM Ceramics (MCM-C)

Ceramic MCM's have been traditionally known as co-fired ceramic hybrids. In contrast to an MCM-L, a ceramic MCM uses an additive manufacturing process. The procedure involves thick film printing techniques that lay down a conductor pattern onto dielectric sheet material. Many layers are used in order to provide the necessary interconnect as well as maintaining the mechanical strength of the completed substrate. Typical designs may employ in excess of eighty (80) layers. Dielectric layers will have via holes punched through the sheet material. These vias are subsequently filled with a conductor paste in order to provide electrical connections between adjacent layers.

In addition to conductive and dielectric material, resistive paste may be screened onto the ceramic allowing various resistor values to be built. The resistors are sometimes trimmed in order to get more accurate values.

Each layer is dried in an oven prior to additional layers being added. Once the final layers have been printed, the entire structure is fired within a high temperature oven to complete the ceramic base, hence the term 'co-fired'. The firing process causes the entire structure to shrink by a pre-determined factor, therefore the output generated by a CAD system must be oversized in order to compensate.

2.2.3 MCM Deposited (MCM-D)

The D classification relates to an MCM that is produced using deposited metals onto a deposited dielectric substrate, more typically this technology is now referred to as 'Silicon substrates'. The dielectric material is usually either inorganic or a polymer-based material. Advances in material research has resulted in dielectric material that possesses a very low dielectric constant, an important asset when we start to discuss high-speed properties inherent within an MCM substrate.

Typically these designs will use a flip chip method of component attach (**Section 3.2.3**). In order to provide accurate pad alignment the passivation layer of a die can be used as the basis of the footprint definition. Currently this data is available in GDSII stream format, the same format used for the majority of output, therefore the CAD system needs to have the ability to read and write GDSII.

3. Component attach methods

Forming the optimum connection path between the substrate interconnect pattern and the device pins is extremely important if companies are to fully capitalise on the benefits of employing MCM's. There are effectively six general types of components and each component type requires a different attach method which has unique advantages and disadvantages;

- Dual in line packages
- Pin grid array
- Surface mounted
- Ball grid array
- Chip on board
- Flip chip

3.1 Attach comparisons

The following table highlights the methods in ascending order of complexity;

Attach method / Component Type	Area	Handling	Testability	Rework	Device availability
Dual in line packages	Poor	Excellent	Good	Good	Excellent
Pin grid array	Fair	Good	Good	Poor	Average
Surface mounted	Fair	Excellent	Good	Good	Good
Ball grid array	Good	Difficult	Poor	Poor	Average
Chip on board	Very good	Average	Average	Poor	Good
Flip chip	Excellent	Difficult	Poor	Poor	Average

As can be seen from the previous table, the traditional DIP and SMD components are by far the easiest to handle and test and the devices are also readily available. As the complexity of the attach method increases, the increased area and performance benefits that are introduced are very significant. However, the problems of handling and test really dictate that these methods are only used when performance is paramount and price is not the driving factor.

3.2 Chip on board (COB)

The option that offers a compromise between simple handling and high complexity is that of COB. This method is actually a grouping of three slightly different component attach options that can be used within the high volume MCM-L style of fabrication;

- Wire bonding
- Tape automated bonding
- Flip chip solder bumping

3.2.1 Wire bonding

This technique involves gluing or soldering a bare die face up onto the substrate. The connections are subsequently built using fine wires that are bonded to the chip surface and a suitable pad on the substrate. The wire is normally bonded by either thermocompression ball bonding or ultrasonic wedge bonding

Thermocompression ball bonding is preferred due to the fact that the wire may be fed in and retracted vertically, this allows for the greatest density of devices to be achieved. Ultrasonic wedge bonding requires a clear area around the device in order to tear the wire once the wedge bond has been completed. As with virtually all areas of MCM design, there are problems and advantages with both methods. The problem with thermocompression is that the substrate surface needs to be held at a constant temperature in order to 'weld' the wire to the pad. If an MCM laminate is held at the required temperature for a long period damage will occur to the surface, pads will lift and the base laminate will distort due to the plastic nature of the material. The end result is that wire bonding is normally used on laminates when the device pin count is low and all the bonds may be completed within a short time.

3.2.2 Tape Automated Bonding (TAB)

TAB devices are supplied pre-loaded on a reel of tape. The advantage over bonded devices is that a hot metal bar (gang bonder) may be used to make a row of connections to the surface in one pass. The devices may also be tested prior to mounting, the device legs making ideal test points for passive test. The disadvantage is that the surface area required for an equivalent device is considerably more when TAB mounting, also the availability of devices packaged into TAB form is very restricted.

3.2.3 Flip Chip (Bump bonding)

The most effective mounting method for a device is when a flip chip methodology is employed. The bare die has a metal layer built onto the I/O pins, an equivalent conductor pattern is prepared on the substrate surface with a layer of solder paste screened into position. The chip is then inverted and a reflow process allows the connection to be made between the I/O pin and the conductor surface. It can be seen that the maximum packing density is achievable using this method. The disadvantage is that high density and face down devices present enormous thermal management issues. The tooling costs and process control required dictates that flip chips are only used on very high performance modules.

3.3 Device protection

Whenever a bare device is placed onto a substrate it will need protection from mechanical stress and contamination. The normal procedure is to apply a plastic coating over the entire device, effectively sealing the device from the atmosphere. The process is known as 'glob top' and it is another task that needs to be performed within the manufacturing cycle.

3.4 Thermal issues

A final point to bear in mind when utilising COB techniques with an MCM-L structure is that of thermal mismatch between the device and the laminate surface. Typically the coefficient of thermal expansion (CTE) of the device will differ from that of the laminate substrate. As the devices are intended to be high performance they tend to run at a high temperature, the mismatch of CTE between the two surfaces can lead to fracturing problems at the bond site. This effect may be minimised to some extent by using thermal adhesives in an attempt to buffer the differences of CTE, the best results are obtained when using bonding methods on silicon substrates (MCM-D).

4. Applications for MCM's

4.1 MCM-L

Features
- High volume
- Low cost
- Proven technology

Markets
- Automotive
- Consumer
- Telecommunications

4.2 MCM-C

Features
- High frequency
- Low weight
- Reliable

Markets
- Aerospace
- Medical
- Military

4.3 MCM-D

Features
- Expensive
- Extremely high performance
- Low volume

Markets
- Computing
- Research
- Telecommunications

4.4 General MCM Trends

- The volume sales and usage of MCM technology continues to be within the general framework of MCM Laminates
- Growth and development is primarily focused upon new materials and improved feature handling
- Silicon substrates represent a fundamental shift in technology that will be required as the physical limit of laminate technology is approached

5. VeriBest MCM handling

5.1 Chip on Board utility

VeriBest International Consulting Services (VBICS) has developed a utility to handle wire bonded components. The utility is fully compatible with VBPCB V14.0 and V14.1 and employs standard pads that are recognised by the Advanced Editor. Additional tools have been added to allow for pad location modification, wire modification, dynamic rule checking and data extraction. The utility is referred to below as VBICS-COB.

5.2 Table of current/future VBPCB functionality

The following table indicates the classification of MCM technology that we support with the existing release of VBPCB as well as the enhancements that will be required in order to maintain full MCM support in future releases.

Function	V14.1	V14.5	V15
MCM-L			
- SMD	✓	✓	✓
- TAB	✓	✓	✓
- Wire bonding	VBICS-COB	VBICS-COB	Scheduled
- Buried components		✓	✓
- Blind/buried vias	✓	✓	✓
- Vias under SMD pads		✓	✓
- User defined layer pairs		✓	✓
MCM-C			
- SMD	✓	✓	✓
- TAB	✓	✓	✓
- Wire bonding	VBICS-COB	VBICS-COB	Scheduled
- Screened resistors			Scheduled
- Mask operations			Scheduled
- Dielectric screens			Scheduled
- Scaled output			Scheduled
MCM-D			
- Flip chip	✓	✓	✓
- GDSII in/out		Not Scheduled	Scheduled

6. Conclusions

It should be clear that enabling MCM technology is not a simple task. There are many considerations to be taken into account both from the design side and also from the manufacturing aspect. This document has only given a brief insight into some of the areas that need to be addressed by companies endeavouring to ramp up MCM production.

It is vital that VeriBest, Inc. field employees gain some knowledge of the basic issues in order to understand the prospect's requirements and why he perceives the need to use MCM's. A simple question on a wish list such as 'Do you support MCM's yes/no' shows that we really should talk with the company in order to further investigate the possibilities.

The table described in **Section 5.2** shows that we can fully support MCM-L in V14.5, the addition of a GDSII reader/writer would allow us to also support MCM-D.

We should not claim to support MCM-C or thick film hybrids until the proposed V15.x functionality is available.