MCM-D Implementation of Passive RF Components: Chip/Package Tradeoffs

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Abstract

MCM-D technology offers the capability to integrate passive components with ICs. Currently, most application volume is in a frequency range between 800MHz and 2GHz. On-chip integration of inductors in this range poses particular problems because of the conflicting needs of small size and high quality factor. MCM technology offers a way to tightly integrate inductors and capacitors in a more cost-effective fashion. To use this approach to its best advantage requires closely coupled design of ICs and substrate and will call for new design methodologies that can work across different technologies.

1. The Evolution of MCM-D Technology for RF Applications

MCM technology originated in and has been driven by high performance digital applications. For the broader class of more mainstream low-end applications, widespread use of MCMs has been held back by the emergence of highly integrated, low cost single-chip solutions and a slowly developing infrastructure for known-good die. In digital MCMs, this has led to the dominance of few-chip modules in applications with modest interconnection demands that can be met with lower cost laminate-based technologies. These factors have impeded the widespread growth of thin-film MCM technologies in digital applications, despite their performance and miniaturization advantages.

RF wireless applications pose an entirely different set of problems. The first, and most obvious, is high frequency performance. Table 1 lists the operating frequencies of many of the most commercially significant high volume RF applications. Future applications will undoubtedly emerge at still higher frequenies, most notably in the 5 to 6GHz range, but currently most of the product volume is concentrated between 800MHz and 2GHz.

In addition to high frequency performance, RF circuits make extensive use of reactive passive components (capacitors and inductors) for filtering and biasing. Currently, these are implemented either on the IC itself, or externally on the circuit board. The inability to successfully integrate all of the needed passive components on the IC has led to a proliferation of "left over" components on the board, leading to considerable system level complexity and compromised performance. Thin film MCMs with integrated passive components have been investigated as an alternative to board-level implementation. Several technological approaches to solve this problem have emerged from different sources [1, 2, 3, 4] that are remarkably similar in overall structure and characteristics.

Another important factor in the use on MCM-D technology for RF applications is the rapid growth in popularity and availability of flip-chip attachment. It offers low parasitic attachment that has some performance advantage at very high frequencies of RF applications, although it is not strictly needed for most current designs, since the ICs have been designed to tolerate a conventional package. Perhaps more importantly, however, it can be a significant benefit in the design of systems requiring tightly integrated passives and ICs. Flip-chip attachment offers high density area-array interconnection along with a nearly seamless electrical coupling between the IC and the substrate. This combination is especially advantageous for RF applications, but demands new approaches to IC and system design.

Table 1: Operating frequencies of major portable RF telecommunications applications.

Application	Frequency (MHz)
Cellular phones	824-849
Mobil data	896-935
GSM	880-925
ISM and Digital cordless phones	900
Pagers	931
Digital cellular	1700-1800
Personal communications (PCN, DCT, PHS)	1800-1900

2. Component Integration and Performance

On-chip passives offer the tightest integration and have the most direct access to available infrastructure, both for design and fabrication. Consequently, whenever practical, they are the favored approach. Capacitors are well-suited to thin-film technologies in general and IC fabrication processes in particular. For RF applications, however, on-chip implementation of inductors poses some unique problems.

Reactive passive components in RF applications need a large vertical offset from ground. For capacitors, this offset should be large compared to the device's dielectric thickness to ensure that the parasitic capacitance to ground is a small fraction of the overall capacitnce. This is practical in most IC fabrication schemes. For inductors, the offset is ideally comparable to the inductor radius, and realistically greater than the inter-winding spacing. This ensures that image currents in the ground plane introduce a mutual inductance that is small compared to the overall device inductance. The use of semi-insulating GaAs as a semiconductor solves this problem, but has high costs per unit area that is a problem for large passives. In silicon RF integrated circuits, which are more cost effective, semi-insulating material is not available. This degrades the quality factor of the inductors.

Figure 1 shows an example [5] of a highly-integrated RF IC. It illustrates some of the basic problems inherent in on-chip passive component implementation. A region of the chip containing some key passive components has been outlined in the figure. One key feature to note is that the area consumed by a relatively small number of passive components, more than one-quarter of the chip's core, is out of proportion to the rest of the circuit. In this example, the diameter of a typical inductor is about 300μm, which is typical for on-chip inductors [6, 7, 8].

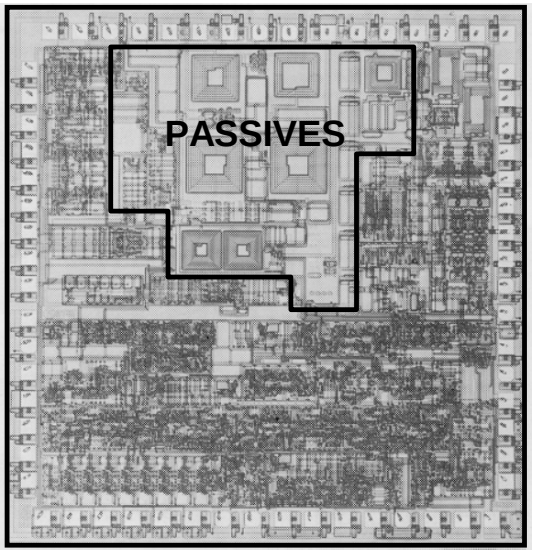

Figure 1: A GSM transceiver IC.

Despite the fact that they occupy a significant fraction of the chip area, inductors like those in this example are far from optimum. Typical quality factors for this kind of on-chip inductor are around 3 to 8 at 1GHz. Consequently, their use is restricted to relatively undemanding applications. For circuits that require better performance, the current alternative is to use off-chip, discrete components, where quality factors can about one order of magnitude larger.

Discrete implementation on a circuit board has a different set of performance compromises. While it does allow the use of individually optimized passive components, these components are not intimately connected to the IC, Instead, there are inescapable parasitics associated with the connections between chip and passives that are mainly associated with the physical separation distance between them. This physical separation translates primarily into series parasitic inductance. Chip-scale packaging offers little help in this regard [9] since most of the separation is not a result of IC package size. It arises from the fact that a large number of passive components that are left out of the IC compete for the space near the chip..

3. The Effects of Inductor Size

Capacitor design is reasonably simple. Capacitor size is dictated by the achievable capacitance density, which, in turn, is limited by breakdown voltage and defect densities. Within the limitations of a particular fabrication technology, there is little or no freedom to change the area of a capacitor.

Inductor design is more difficult. Figure 2 shows a sketch of the typical behavior characteristics of a spiral inductor. The effective inductance, L_{EFF}, is defined by

$$L_{EFF} \equiv \mathrm{Im}[Z]/(2\pi f) \qquad (1)$$

and the quality factor, Q, by

$$Q \equiv \mathrm{Im}[Z]/\mathrm{Re}[Z]\,. \qquad (2)$$

where Z is the device impedance. An important characteristic of the device is that it has a self-resonant frequency, f_{SR}, above which its behavior is no lot inductive. At the self-resonant frequency, its quality factor is zero. The quality factor is highest at some frequency, $f_{Q\text{-}MAX}$, which typically occurs at about one-fourth of the self-resonant frequency [3]. A simple, commonly used circuit model that captures the key elements of this behavior is shown in Figure 3.

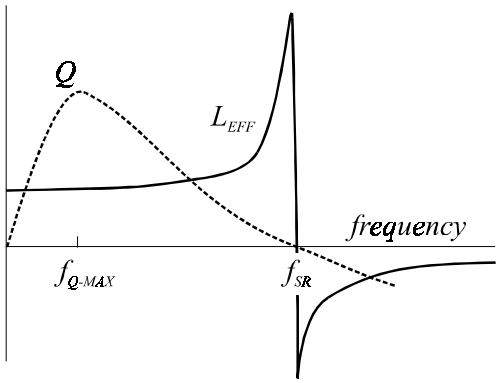

Figure 2: Typical inductor characteristics.

Unlike capacitors, for which the only design parameter is area, basic round spiral inductors can be characterized by four independent design parameters: their inner radius, number of turns, line width and spacing between the turns. One consequence of this is that a particular value of inductance can be designed in a bewildering variety of forms. The differences in these forms are manifested in the other parameters of the model.

Reasonably accurate calculations of inductance for complex geometric structures can be obtained by dividing them into short, straight segments and summing up the inductance coupling them. The inductance between the any two segments can be found from the integral

$$L_{ik} = \frac{\mu}{4\pi I_i I_k} \int d^3r \int d^3r' \frac{\boldsymbol{j}_i(r) \cdot \boldsymbol{j}_k(r')}{|r - r'|} . \qquad (3)$$

This generally requires numerical evaluation for realistic inductor design, but the calculation is straightforward and rapid [10]. Accurate calculation of the capacitive elements in the model requires more elaborate and time-consuming methods.

Empirical formulae for the inductance, self-capacitance and resistance of circular spiral inductors [11] are less accurate, but are more useful for analytical design

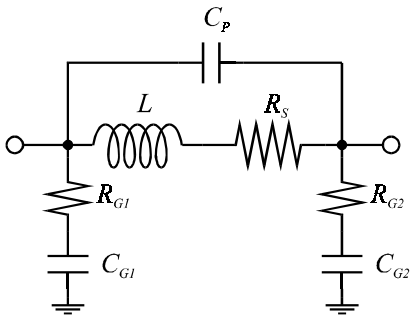

Figure 3: Inductor model.

estimates. In particular, for round spiral inductors with diameters ranging from 1 to 5mm, it has been found that the inductance is approximately given by

$$L(nH) \approx 0.0394 \frac{n^2 a^2}{8a + 11c} , \qquad (4)$$

where n is the number of turns, a is the average radius of the turns (μm) and c is the difference between the inner and outer radii (μm). The inter-winding shunt capacitance, C_P, can be approximated by

$$C_P(pF) \approx 3.5x10^{-5} D_0 + 0.06 . \qquad (5)$$

where D_0 is the outer diameter of the spiral. (This relationship was derived for alumina substrates. Silicon is a reasonably close match in dielectric constant.)

These empirical relationships illustrate two important features: the first is that the self-capacitance is roughly proportional to outer diameter. This simply reflects the fact that physically larger inductors have an inherently lower self-resonant frequency. The second is that for a particular inductor diameter, D_0, we can generally choose values of line width, spacing and number of turns that result (via Equation 4) in a desired value of inductance. The trade-off, as we are required to use more turns and smaller line dimensions, is that the series resistance, R_S, grows and the quality factor is degraded.

Generally, increasing the size of an inductor will improve Q at low frequency, but will also lower both f_{SR} and $f_{Q\text{-}MAX}$. Optimum inductor performance can be obtained by choosing the outer diameter of the inductor so that $f_{Q\text{-}MAX}$ (which is typically about one-quarter of f_{SR}) is equal to the frequency of operation.

4. Constant Impedance Scaling

As a practical matter, we find that higher frequency applications use smaller values of inductors and capacitors. This is because we usually seek to implement a particular value of impedance. In examining component size and technology trade-offs over a range of application frequencies, it is more useful to consider the area needed to implement a particular impedance than to consider a particular value of inductor.

To achieve an impedance Z at frequency f requires an inductor of value

$$L = Z/(2\pi f) . \qquad (6)$$

Since it is roughly optimal to operate this component at one-fourth of its self resonant frequency, the capacitance and inductance are related to the frequency of operation by

$$f = \frac{f_{SR}}{4} = \frac{1}{8\pi\sqrt{LC_{OPT}}}, \quad (7)$$

so

$$C_{OPT} = \frac{1}{32\pi fZ}. \quad (8)$$

Equation 8 can be used with Equation 5 to find the optimum diameter of an inductor needed to implement a particular impedance as a function of operating frequency. Figure 4 shows a plot of this relationship for some commonly used circuit impedances.

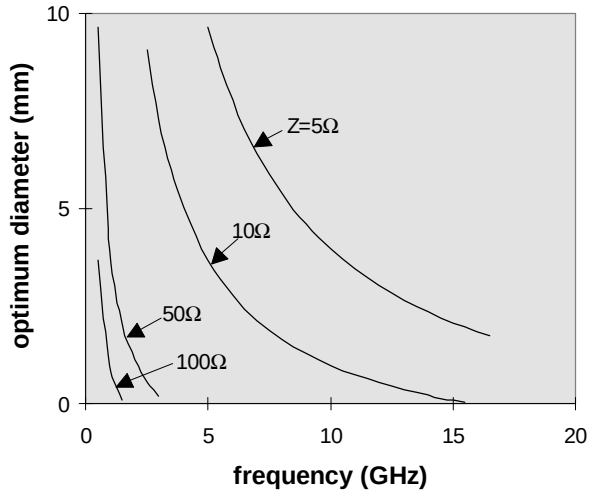

Figure 4: Optimum inductor diameter as a function of operating frequency for various values of impedance.

A key feature of interest in Figure 4 is that most of the optimal device sizes for these impedances are too large to be practical in IC technologies. The purchase prices of silicon semiconductor devices, depending primarily on their volume and complexity, range from $0.10 to $1.00 per square millimeter. (Compound semiconductors, like GaAs, are higher.) This can be compared to the cost of off-chip discrete implementation of inductors, which ranges from $0.05 to $0.50 per inductor. It is seldom cost effective to make on-chip inductors that are larger than one millimeter in diameter. The sizes of the integrated inductors shown in the example in Figure 1 reflect these cost factors. Consequently, the inductors that are feasible for on-chip integration are those with modest requirements for *Q*, since they are almost always suboptimally sized.

A second feature to note in Figure 4 is that optimal integration of reactive impedances in small sizes is easier at higher frequencies. Other factors in the structure of ICs, such as the use of conductive (*i.e.* lossy) substrates can also degrade device properties. Assuming these limitations can be overcome by appropriate changes in processing, however, it appears that higher frequencies are better suited to single-chip integration of reactive components. Unfortunately, most of the commercially significant RF wireless applications are clustered in the lower end of the range shown in Figure 4, where it is especially difficult to make small inductors.

5. The Role of MCM-D Technology in RF Wireless Applications

The main advantage offered by MCM-D technology for RF wireless applications is its ability to integrate passive components into the MCM substrate. This advantage is only practical to the extent that it improves performance without significantly raising costs.

At low operating frequencies, the optimum size for inductors becomes too large to be cost effective for both ICs and for MCMs. In such cases, other technologies like wire-wound inductors with permeable cores offer a better, more cost-effective alternative. At sufficiently high frequencies, on the other hand, it may be most cost effective to implement all of the inductors on the chip itself. This avoids the costs and parasitic impedances associated with extra pins and eliminates the need for added components on the board.

As we discussed above, most RF wireless applications are currently operating in the frequency range from 800 to 2000 MHz. At these frequencies, it is practical to make good spiral inductors in a reasonable size for MCM substrates, but impractical to implement many of these same inductors on the IC. Figure 5 shows an example of an MCM substrate designed for a GSM (1GHz) application. This example clearly shows the relationship between the sizes of the inductors and capacitors in the MCM and the chip. Overall, this module substrate reduces board area requirements by more than a factor of three compared with conventional, discrete component implementation. At the same time, however, it is obvious that these same passive components are too large for on-chip integration.

Figure 5 also helps to illustrate the fact that the extent to which MCM technology is useful for integrating passive components will be determined by the extent to which its per-unit-area substrate cost is less than that of the IC. A lower cost extends the range of inductor values that are cost effective to integrate, reducing the number of discrete components outside the module. At the same time, with low cost substrates the optimum design may be to also move components from the IC to the module for cost reasons alone. This offers the potential to further reduce cost by minimizing IC size.

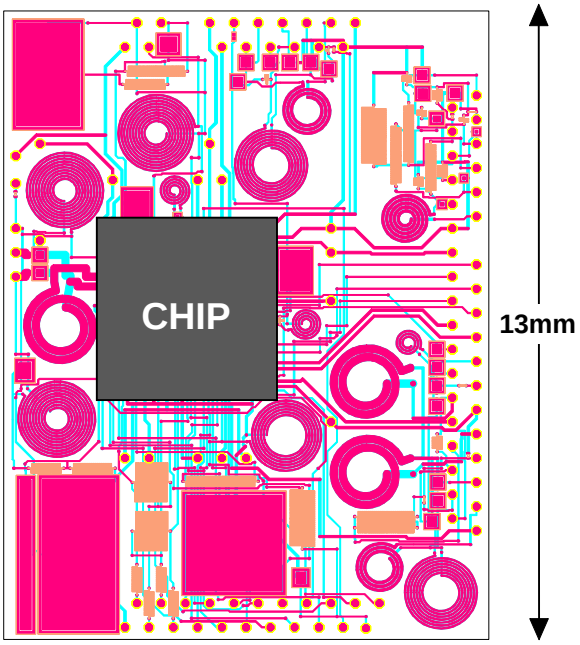

Figure 5: RF module design using MCM-D substrate technology and flip-chip assembly.

6. Challenges

The current trade-offs between on-chip integration versus discrete, off-chip implementation of passive components is reasonably well understood. Defining new trade-offs between on-chip, on-module and on-board options is more complex, and our experience with is this is currently very limited. It is clear, however, that designing modules with integrated passive components that take best advantage of the features of the various technologies involved will require new ways of designing chips and modules.

Design tools that seamlessly cross technology boundaries are today non-existent. Physical design tools depend on technology files that define a single structure – chip, MCM substrate or board. This means that designs are most conveniently accomplished within a single technology, and cross-technology designs are done by hand for lack of any alternative methods or tools. RF modules have an advantage over other analog and mixed-signal MCM applications, however, since the design is mainly done at the component (as opposed to product) level. This offers better opportunities for close design coordination among the IC, substrate and final package.

The costs of module-level implementation are poorly understood and hard to manage. A merchant infrastructure for MCM-D with embedded passive components has yet to emerge. As with all MCMs, the lack of a known good die infrastructure remains a problem, as well. RF modules pose less of a problem in this regard, since they may have as few as one chip, like the example in Figure 5.

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