RF Power Amplifier Simulation with Microwave Office

Visual System



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Simulation Methods

- A simulator is an equation solver. The models are the equations. Accurate results require accurate models and the skill to apply them.
- Large signal models of power transistors are not very accurate. Simulation should be used for verifying concepts and statistical analysis.
- Several types of simulators are used for PA design. Most all include layout for PCBs and some have RFIC process kits:

Linear – Simulation of passive networks and linear controlled sources. Prediction of power output using "Cripps Contours".

Harmonic Balance – Nonlinear frequency domain analysis. <u>Periodic sources</u> decomposed into harmonics. KVL and KCL solved for user specified number of harmonics and order of products. Good for soft to medium nonlinearities. Fast runtimes for closely spaced tones.

Spice - Nonlinear time domain analysis. Good for strong nonlinearities. Long runtimes for closely spaced tones. Must handle distributed elements and s-parameters via equivalent circuits or convolution.

Envelope – Represents modulated waveforms with complex envelope. Nonlinear circuits may be behaviorally modeled, or envelope source sliced into time steps and circuit solved with HB. Amplifiers and mixers may be incorporated into high level systems such as digital communication links, AGC loops, and linearization schemes.

2.5D EM – Microstrip, stripline, RFICs, multilayer PCBs, thin printed antennas. Primary EM coupling in XY plane.

3D EM – Packages, wirebonds, waveguide, antennas. Not a substitute for 2.5D (ex. Lange couplers).

HB Simulation

Distributed components and s-parameters pose some problems:

DC is the zero harmonic.

Closely spaced tones produce low frequency products.

! Coilcraft 0402CS-10N Chip Inductor 1 29 May 2002 # MHZ S MA R 50 MagS11 0.0007713331 54.474609 0.999552003 -0.0359838749 0.000771333108 54.474609 0.0137349967 81.4213296 0.9980436 -0.779702275 0.9980436 -0.779702275 82.9323629 0.997068075 82.9323629 0.997068075

S-parameter data should have a 0 Hz line or else the simulator will extrapolate a low frequency response or model it as a short,

likewise for EM simulations.

High order products appear at high frequencies. Simulator may extrapolate data.

Hard nonlinearities cause convergence problems. Tricks to achieve convergence:

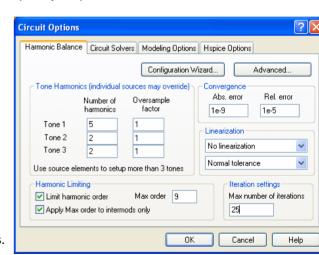
Back off power

Adjust oversample factor.

Reduce error tolerance.

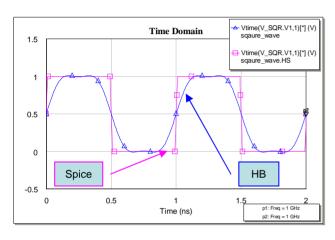
Turn off breakdown diodes in model or linearize them. Same for nonlinear capacitors.

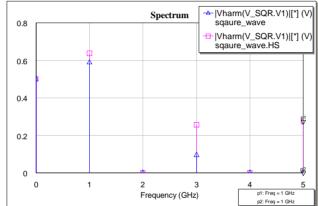
Good model should be "continuously derivable" meaning there should be a solution (no matter how small) for every harmonic.

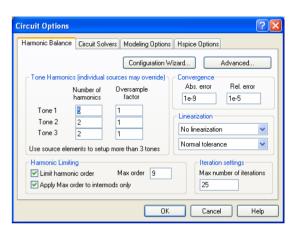


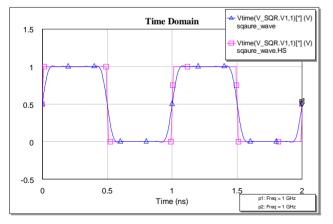
HB Waveforms

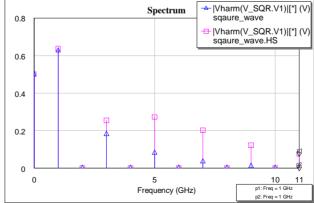
Sharp transitions difficult to model











Circuit Options	?፟፟፟፟፟፟፟፟፟፟፟፟	
Harmonic Balance Circuit Solvers Modeling Options Configuration Wi Tone Harmonics (individual sources may override) Number of harmonics Tone 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
OK Cancel Help		

Example Amplifier

Freescale MRF5S21150H reference design:

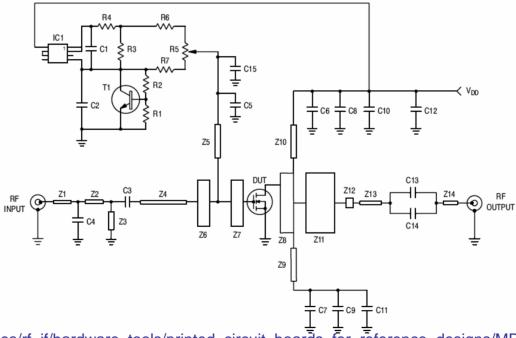
Pout=33 Watts at 2140 MHz, 2 carrier CDMA

Gain=12.5 dB

Eff=25 %

IM3=-37 dBc at 10 MHz offset

VCC=28 V, IDQ=1300 mA



http://www.freescale.com/files/rf_if/hardware_tools/printed_circuit_boards_for_reference_designs/MRF5S21150H_UMTS_RD.pdf

Launching Microwave Office

MWO-228, VSS-100 :

Linear

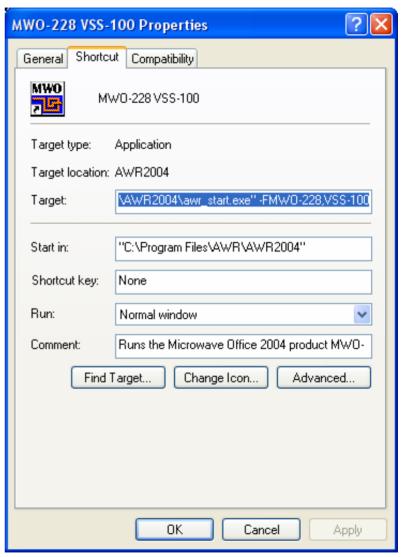
Harmonic Balance

EM

Layout

System

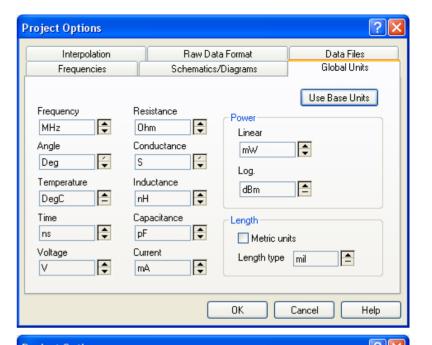
 May need to edit desktop icon and modify start parameters. May also use MWO-225

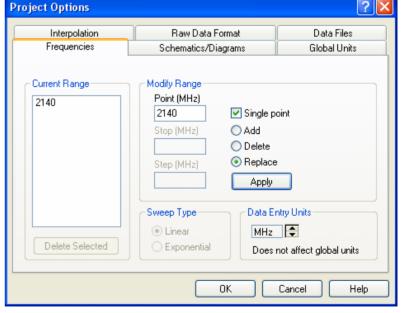


Project Setup

- Set Project Options, Global Units to:
 - MHz
 - mils

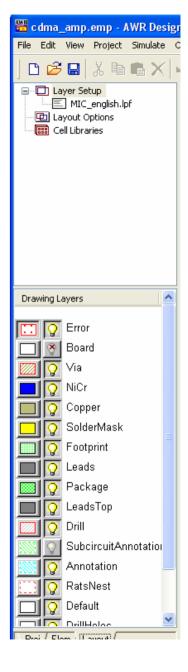
- Set Project Options, Frequencies to:
 - MHz units
 - 2140 MHz single point





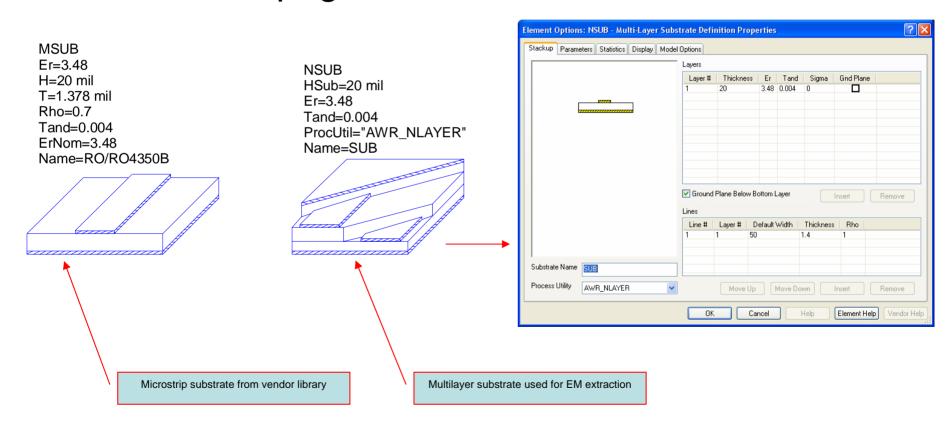
Layout Setup

- Setup drawing layers by importing pre-defined Layout Process File "MIC_english.lpf"
- Project, Process Library, Import LPF
- Example process files located in:
 - C:\Program Files\AWR\AWR2004



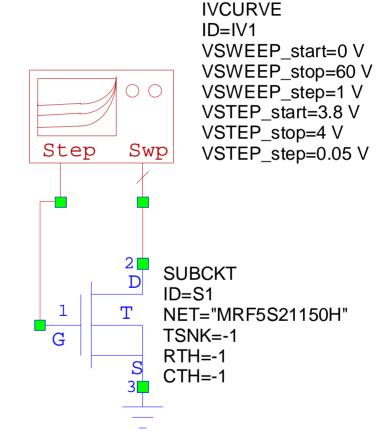
Global Definitions

 Substrate information may be placed on Global Definitions page



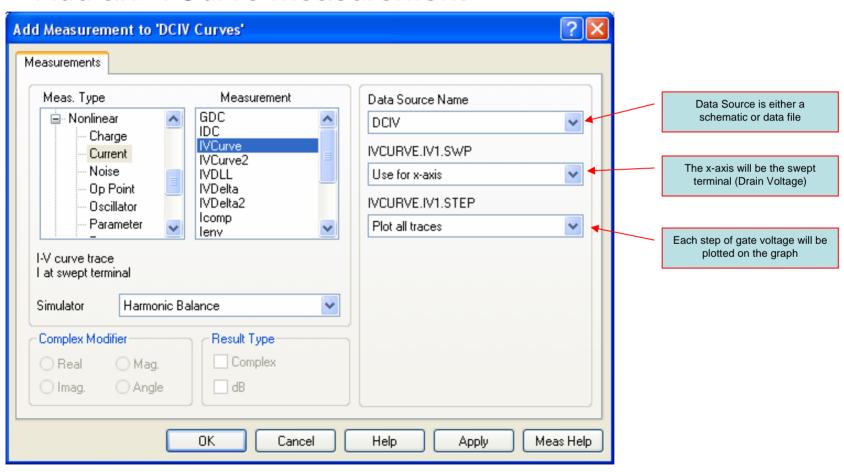
DCIV Schematic

- Create a circuit schematic named "DCIV" consisting of the non-linear model and IVCURVE measurement device
- Use a curve tracer measurement to find VGS that establishes IDQ=1300 mA at VDD=28 V



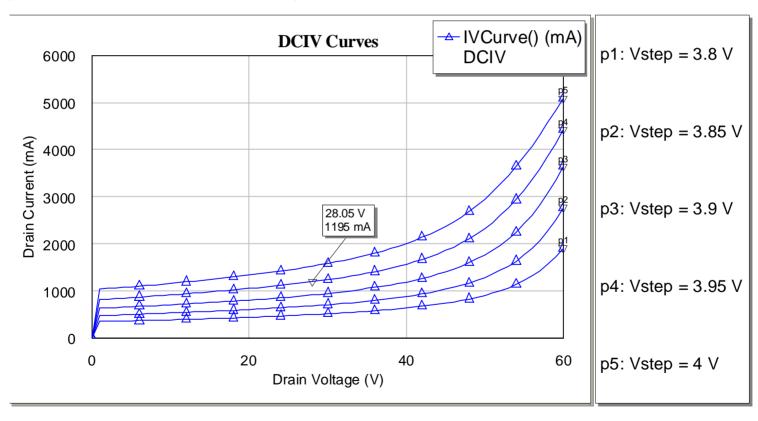
DCIV Measurement

- Create a rectangular graph named "DCIV Curves"
- Add an IVCurve measurement



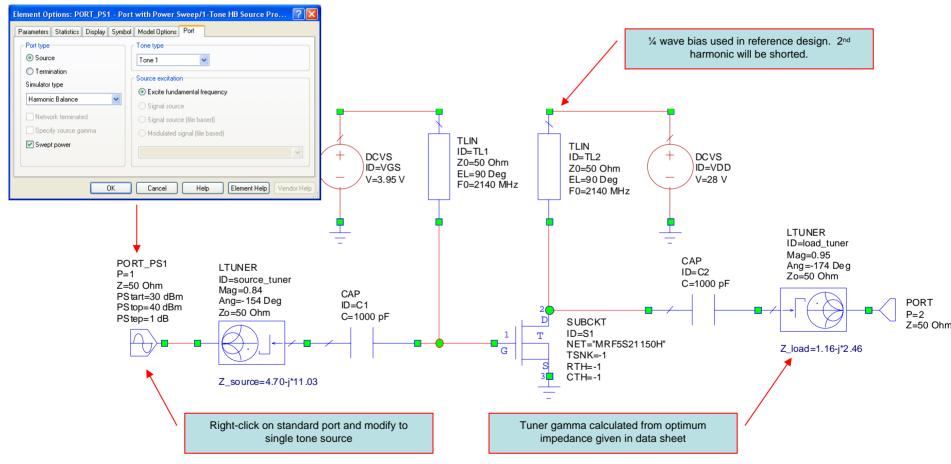
Finding the Bias Point

Simulate then place a marker showing VGS=3.95 V yields (approximately) IDQ=1300 mA at VDD=28 V



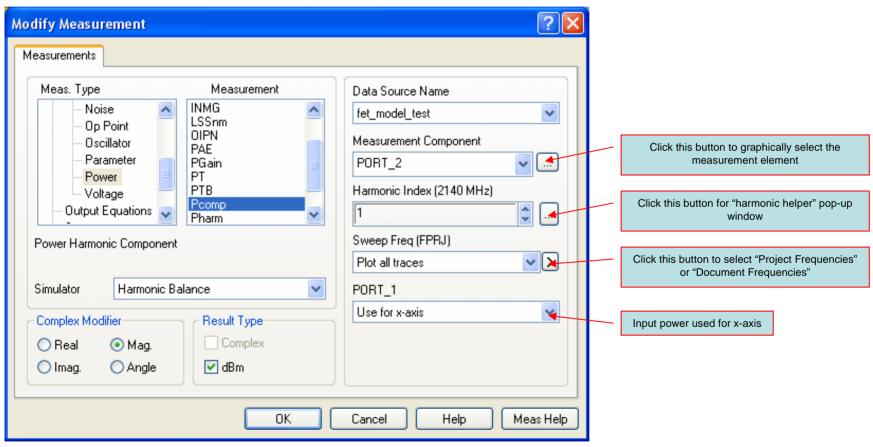
Model Verification Schematic

 Create a new schematic named "model_test" to verify performance using impedance tuners.



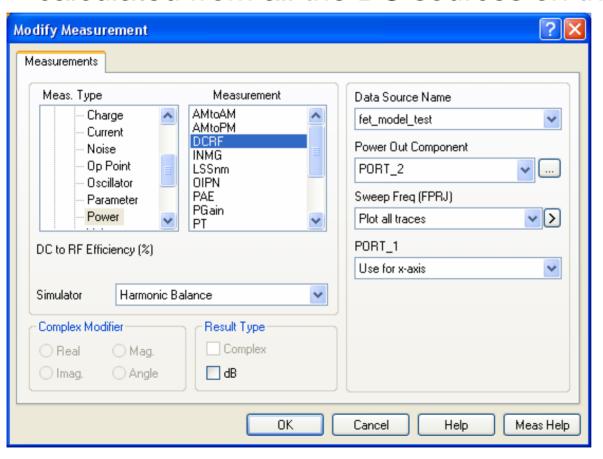
Model Verification Measurements

 Create a rectangular graph named "FET Model Output Power and Efficiency" and add an Pcomp measurement



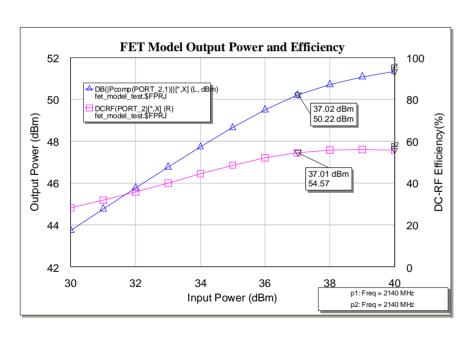
Model Verification Measurements

 Add a DCRF measurement. The DC input power is calculated from all the DC sources on the schematic.



Model Verification Results

- Comparison at Pin=5 W (37.0 dBm)
 - Model: Pout=105 W (50.2 dBm), G=13.2 dB, Eff=55 %
 - Measured: Pout=102 W, G=13.1 dB, Eff=42 %



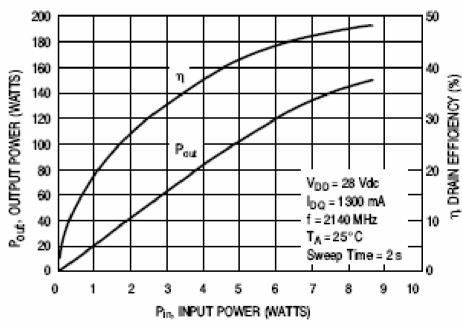


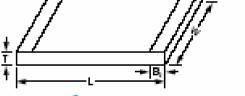
Figure 9. Output Power and Drain Efficiency versus Input Power

Layout Cell Creation

- Create a new GDS cell library named "RF_footprints".
 Create a new cell named "0805_AVX".
- Use a 10 mil snap grid to draw the footprint and leads on their respective layers.

Add cell ports (reference planes) at the inside of the pads.
 Hold down CTRL to snap to geometry.



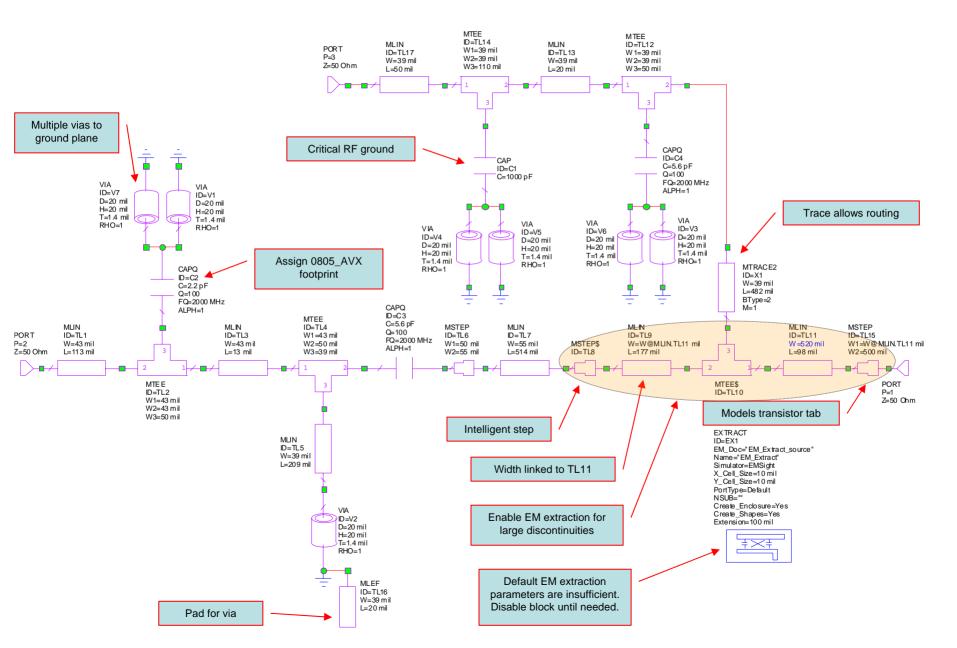


ACCU-F[®] *(Signal Type Capacitors)

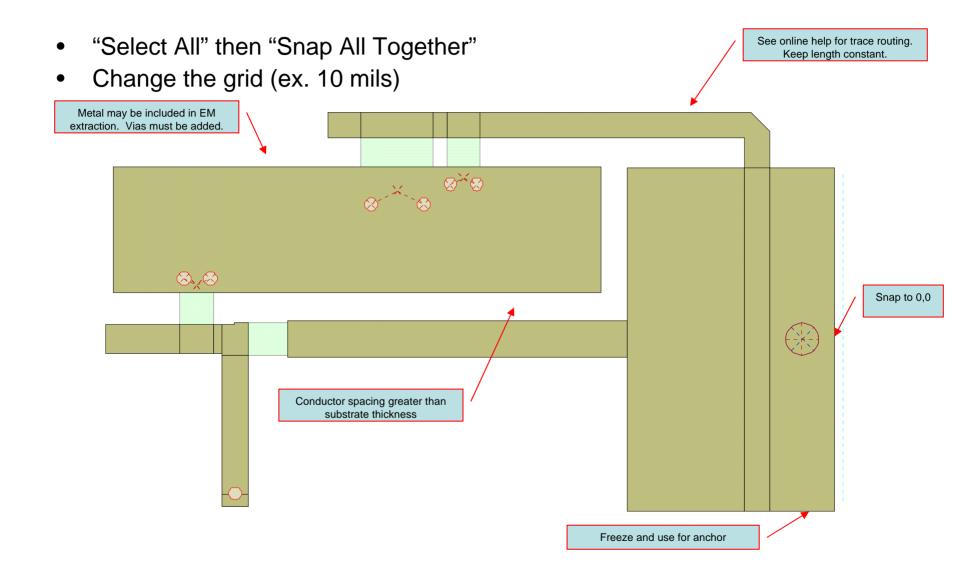
	0603	0905
L	1.60±0.1 (0.063±0.004)	2.01±0.1 (0.070±0.004)
W	0.81±0.1 (0.032±0.004)	1.27±0.1 (0.050±0.004)
Т	0.63±0.1 (0.025±0.004)	0.63±0.1 (0.025±0.004)
В	0.30±0.1 (0.012±0.004)	0.30±0.1 (0.012±0.004)

⊩not recommended for new design Accu-P's are recommended. :BIMENSIONS (Inches) milimeters

Source Match Schematic



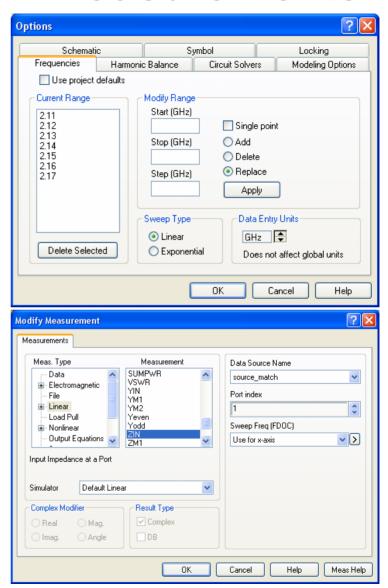
Source Match Layout



Source Match Measurements

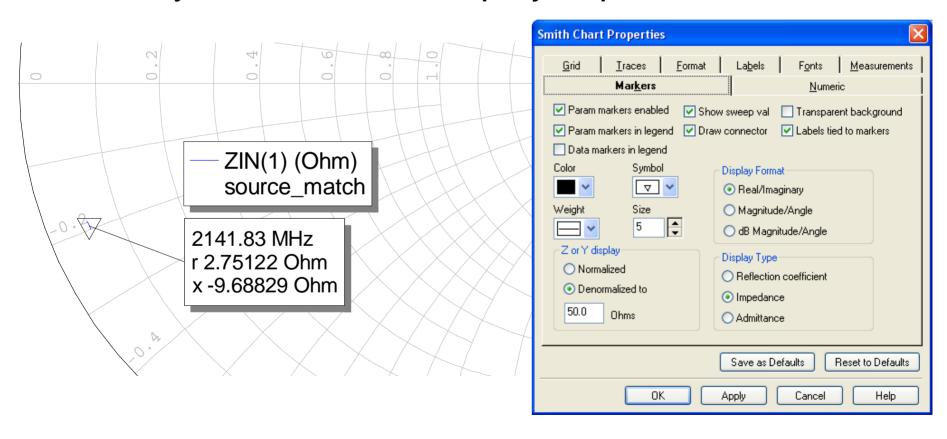
 Modify the frequency points of "source_match" by right clicking the options in the tree view.

 Create a new Smith Chart graph named "Matching Network Impedances".
 Add a Zin measurement for Port 1.



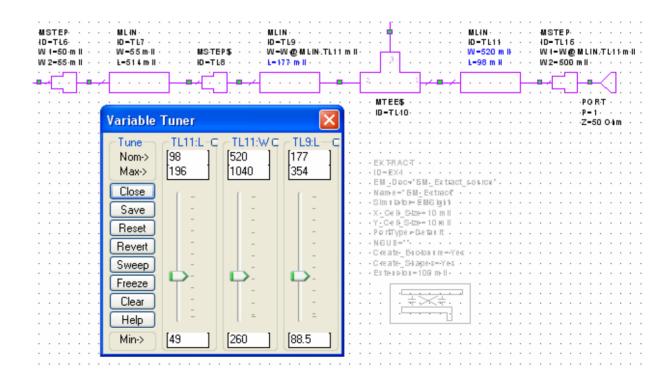
Source Match Results

- Simulate then place a marker at 2140 MHz.
- Modify the marker to display impedance

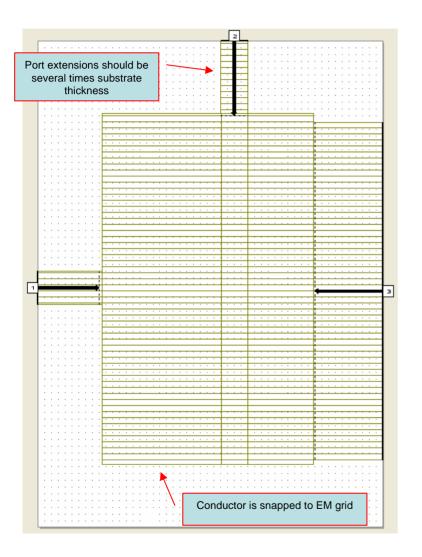


Source Match Tuning

- Is the source impedance close the 4.70—j*11.03 ohms recommended in the data sheet?
- Tune the circuit to improve the result.
- Enable the EM Extraction element and observe the result.



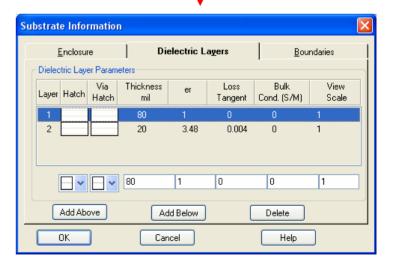
EM Extraction



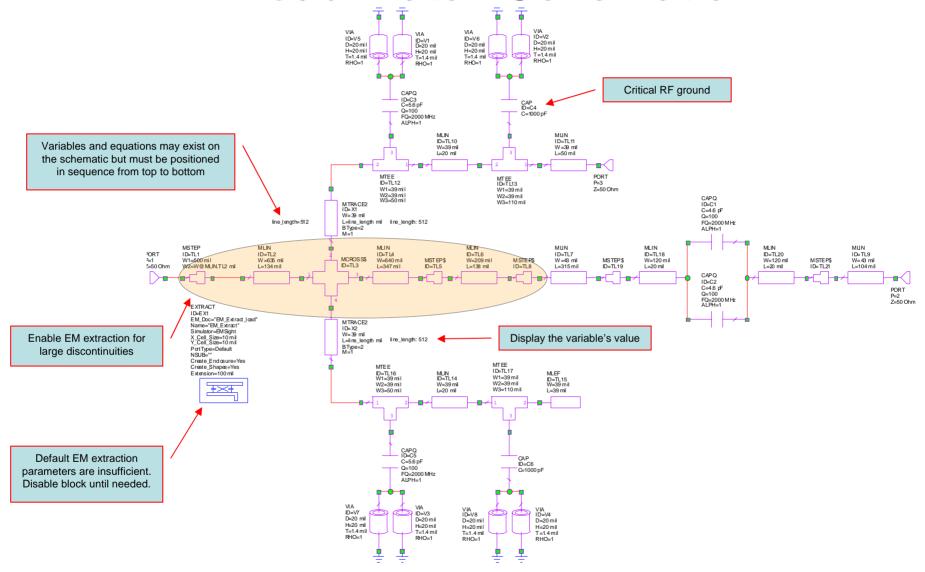
EXTRACT
ID=EX1
EM_Doc="EM_Extract_source"
Name="EM_Extract"
Simulator=EMSight
X_Cell_Size=10 mil
Y_Cell_Size=10 mil
PortType=Default
NSUB=""
Create_Enclosure=Yes
Create_Shapes=Yes
Extension=100 mil



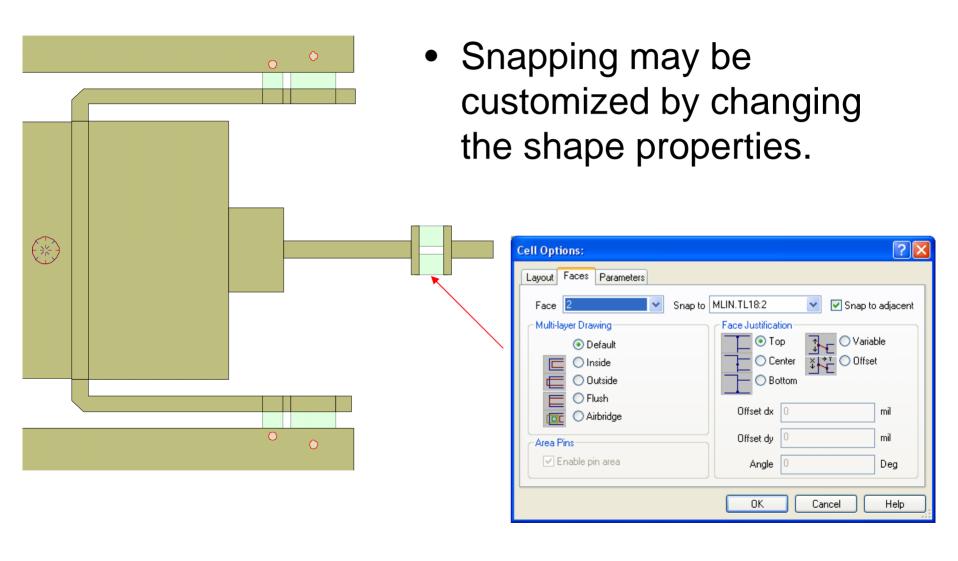
NSUB
HSub=20 mil
Er=3.48
Tand=0.004
ProcUtil="AWR_NLAYER"
Name=SUB



Load Match Schematic

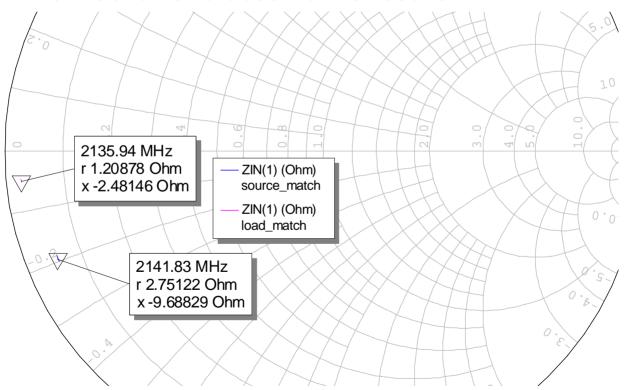


Load Match Layout

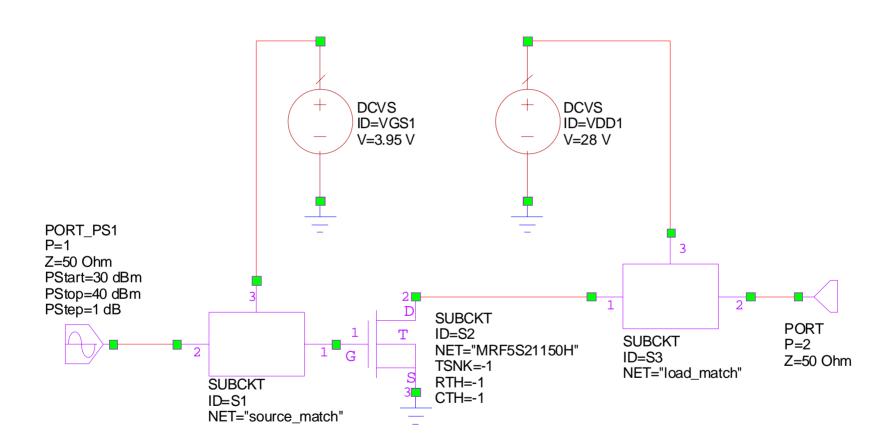


Load Match Results

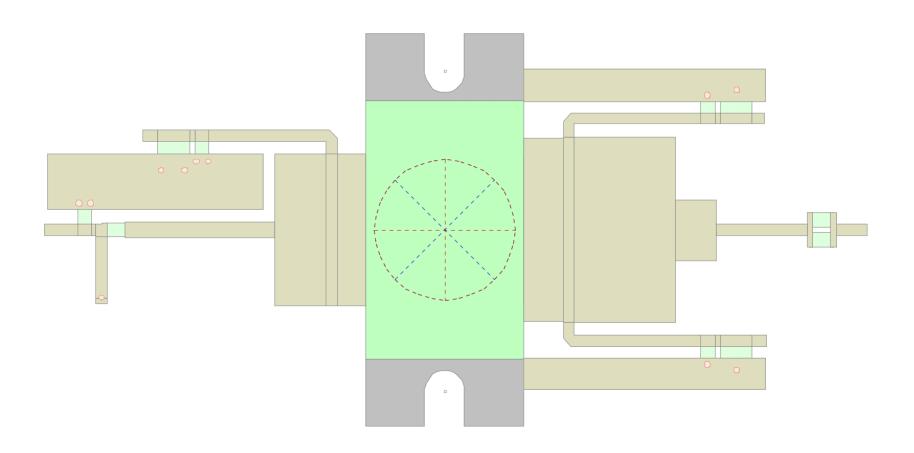
- Is the load impedance close the 1.16–j*2.46 ohms recommended in the data sheet?
- Tune the circuit to improve the result.
- Enable EM extraction and observe the results.



Amplifier Schematic

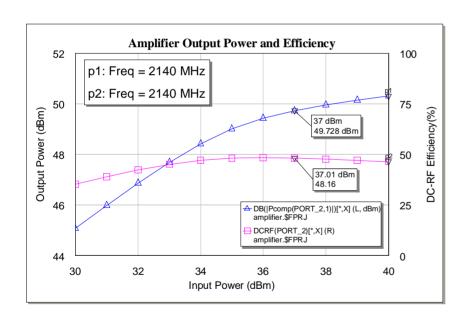


Amplifier Layout



Amplifier Pout and Eff

- Comparison at Pin=5 W (37.0 dBm)
 - Model: Pout=93 W (49.7 dBm), G=12.7 dB, Eff=48 %
 - Measured: Pout=102 W, G=13.1 dB, Eff=42 %



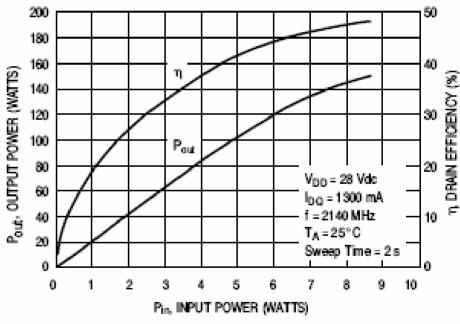
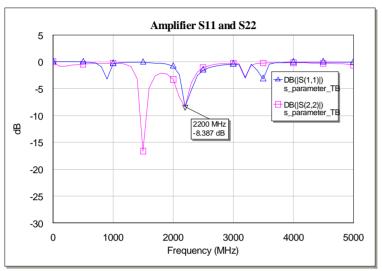
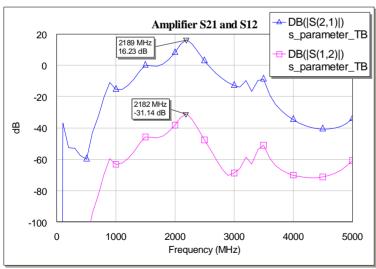
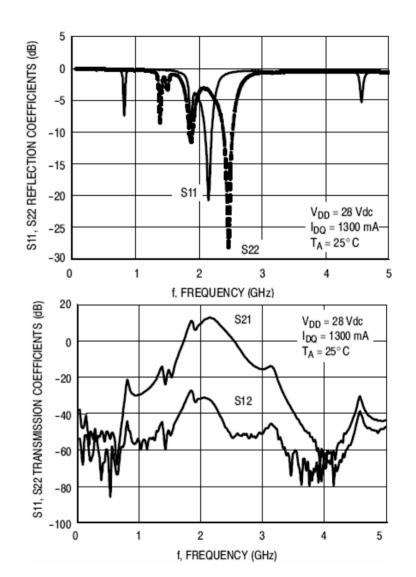


Figure 9. Output Power and Drain Efficiency versus Input Power

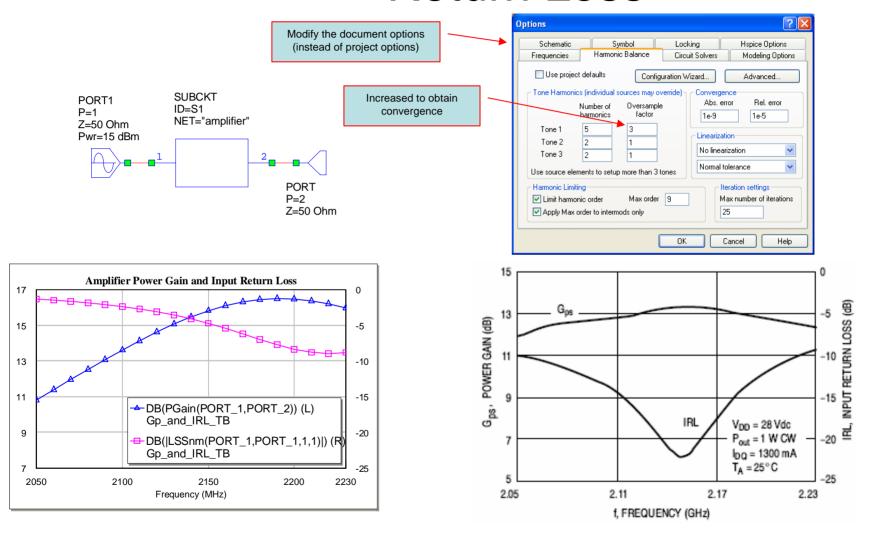
Amplifier S-Parameters





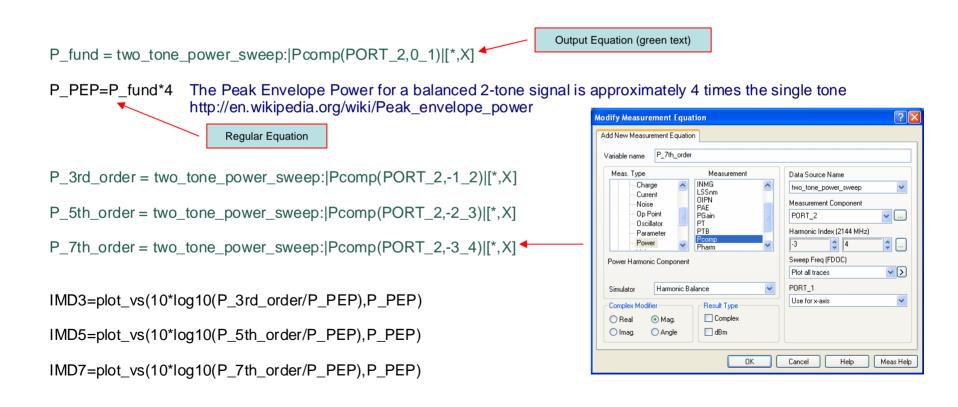


Amplifier Power Gain and Input Return Loss

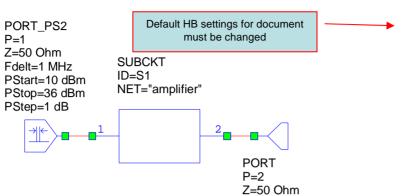


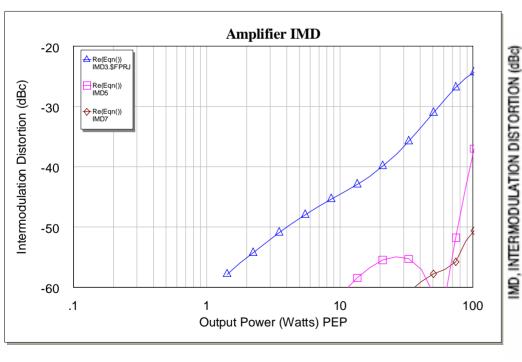
Output Equations

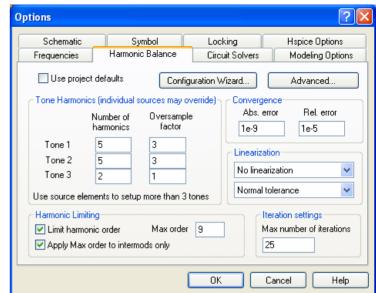
- Use output equations to assign measurements to variables.
- Output equations are always in base units
- Data may then be manipulated using a regular equation.

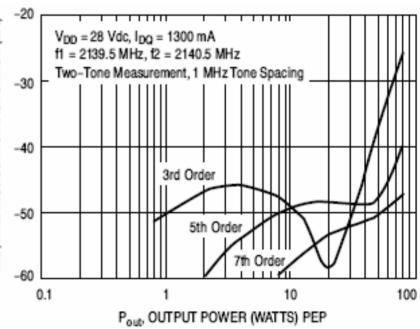


Amplifier IMD



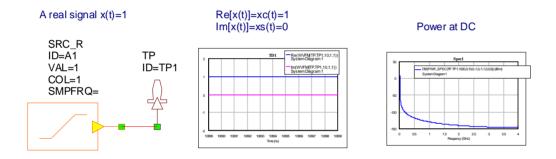


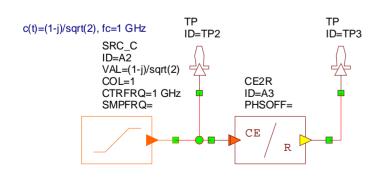


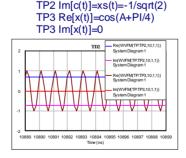


Visual System Simulator

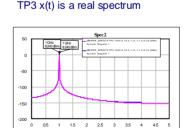
- VSS is a time domain simulator that uses both real samples and complex envelope representation.
- Complex envelope representation allows baseband waveforms to be up-converted and simulated at RF.
- VSS is very powerful however the manual should be read to fully understand it.
- See example vss_data.emp for examples of sources.







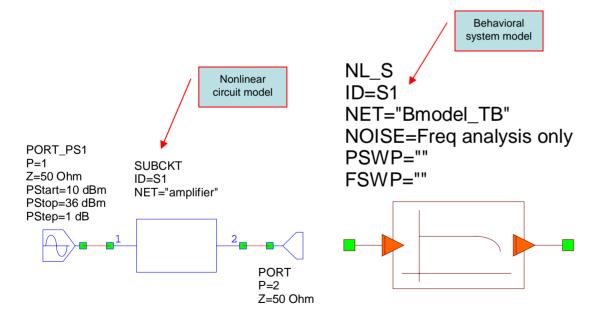
TP2 Re[c(t)]=xc(t)=1/sqrt(2)

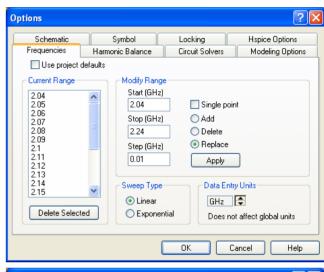


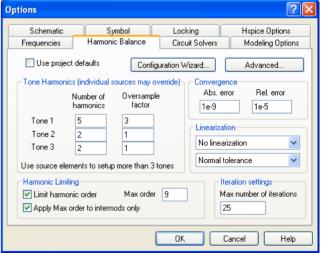
TP2 c(t) is shifted by Fc

Behavioral Modeling

- VSS uses AM-AM and AM-PM results from HB analysis to obtain a behavioral model.
- Strong nonlinearities may not model well.
- HB simulation document "Bmodel_TB" must be configured for power ranges and frequencies desired in system simulation.



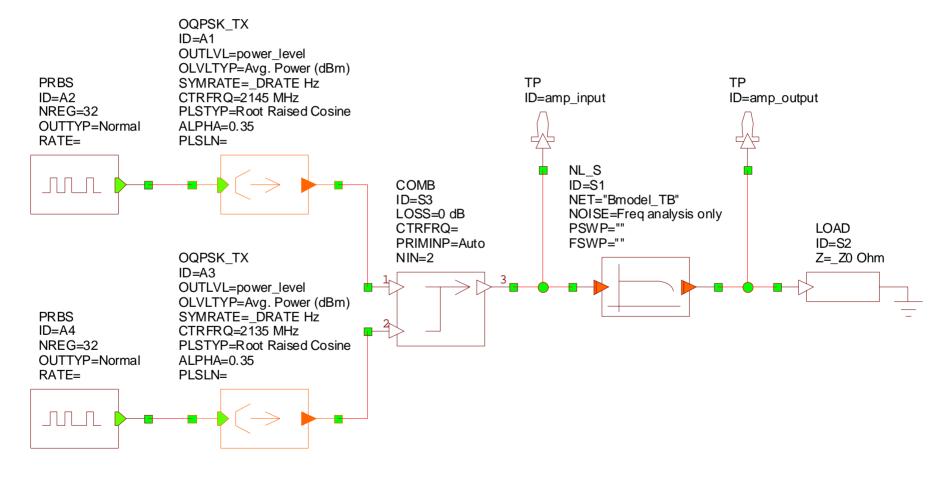




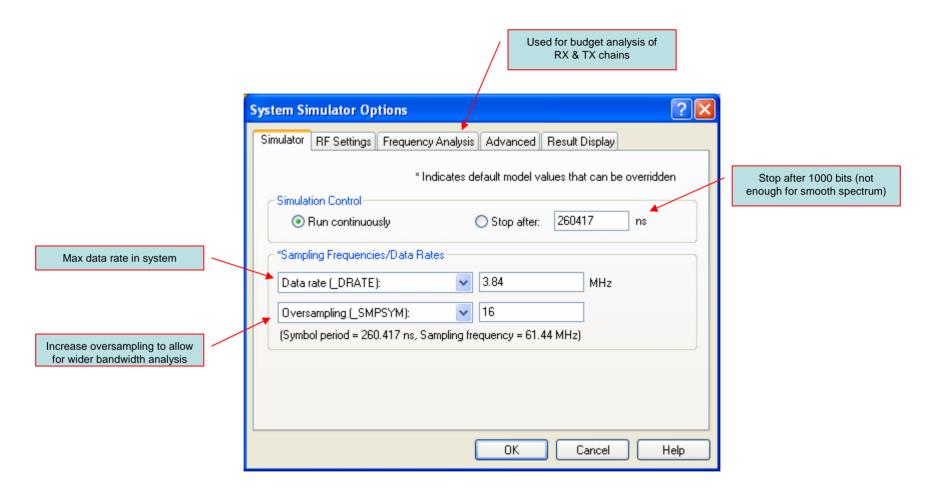
OQPSK Transmitter

power_level=0 +12 dBm power_level yields +30 dBm out of amplifier

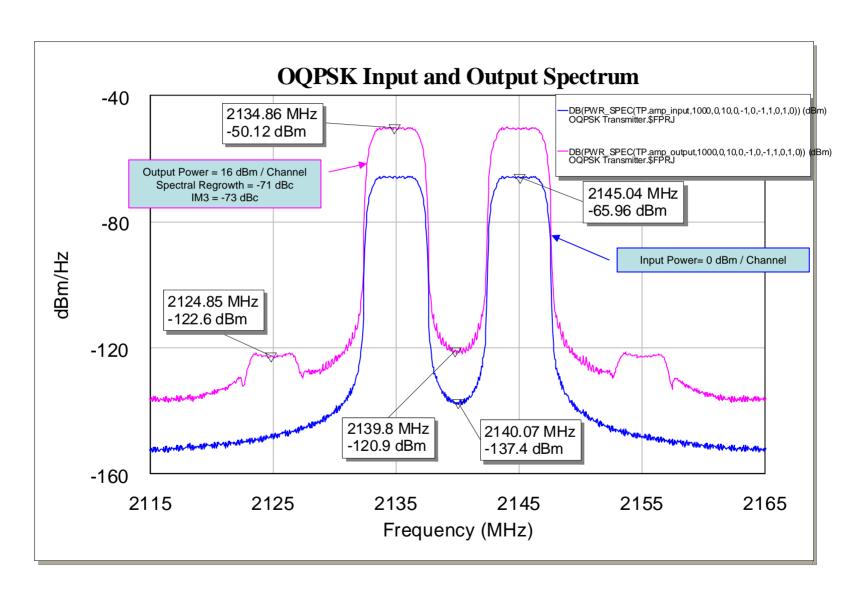
Add 10*log(3.84 MHz)=65.8 dBHz to power spectral density graph for total power



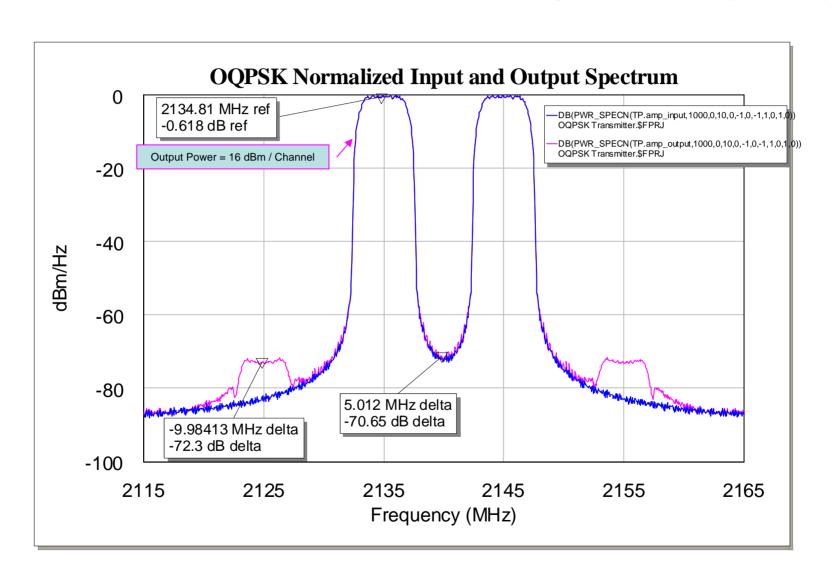
Default System Options



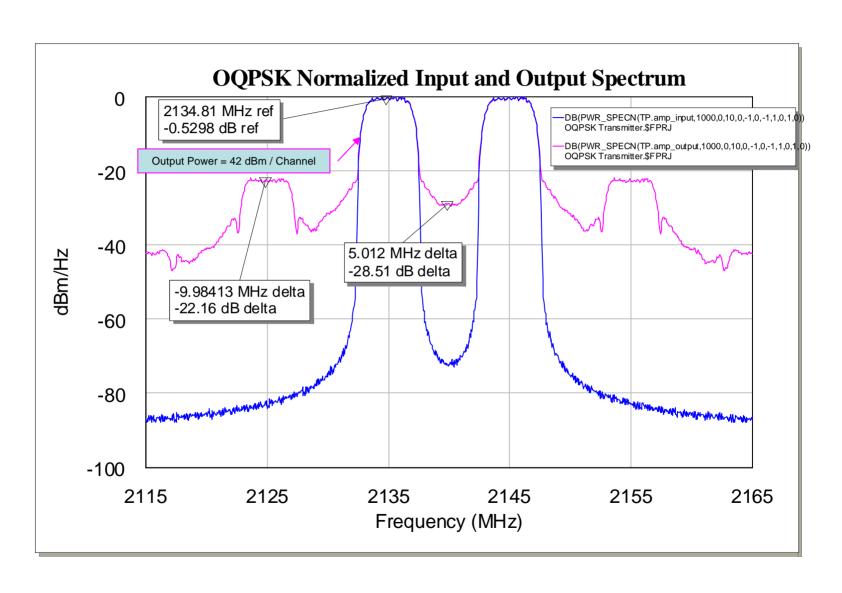
OQPSK Spectrum (PSD)



OQPSK Normalized Spectrum (PSD)



OQPSK Normalized Spectrum (PSD)



References

MRF5S21150H Reference Design http://www.freescale.com/files/rf_if/hardware_tools/printed_circuit_boards_for_reference_designs/MRF5S_21150H_UMTS_RD.pdf

MRF5S21150H Data Sheet

http://www.freescale.com/files/rf if/doc/data sheet/MRF5S21150H.pdf

Applied Wave Research's Microwave Office & Visual System Simulator

http://www.appwave.com/