

Advancing the
wireless revolution™

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What's New in Microwave Office 2008

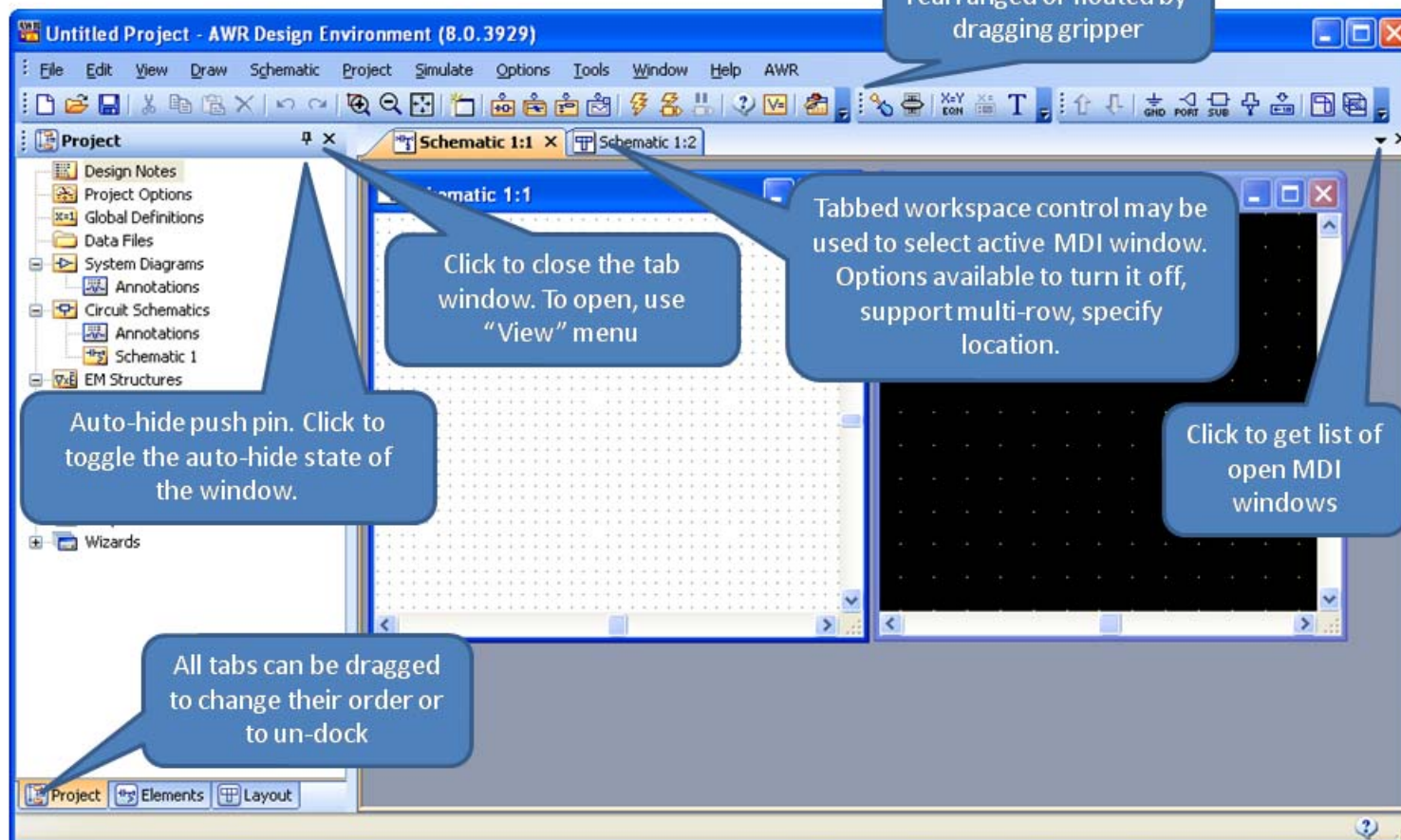
Power and Precision



- Productivity
 - New enhanced GUI for added ease-of-use and maximizing desktop
- Technology
 - APLAC® HB within Microwave Office® – Nokia-hardened for more than a decade
 - AXIEM™ part of the EM Socket™ for fast, accurate EM of large designs
 - ACE™ enhanced for use with microstrip & stripline elements
 - iNets™ – shape-based traces in addition to paths
 - EXTRACT and Layout enhancements for greater design concurrency
 - Multi-technology Module design flow - from system to verification
 - Open architecture environment
 - EM Socket – even more solvers, features, and robustness
 - DRC/LVS – ICED join Calibre and Assura
- Process Design Kits
 - MMIC – featuring AWR® industry-leading technologies

Productivity – New GUI

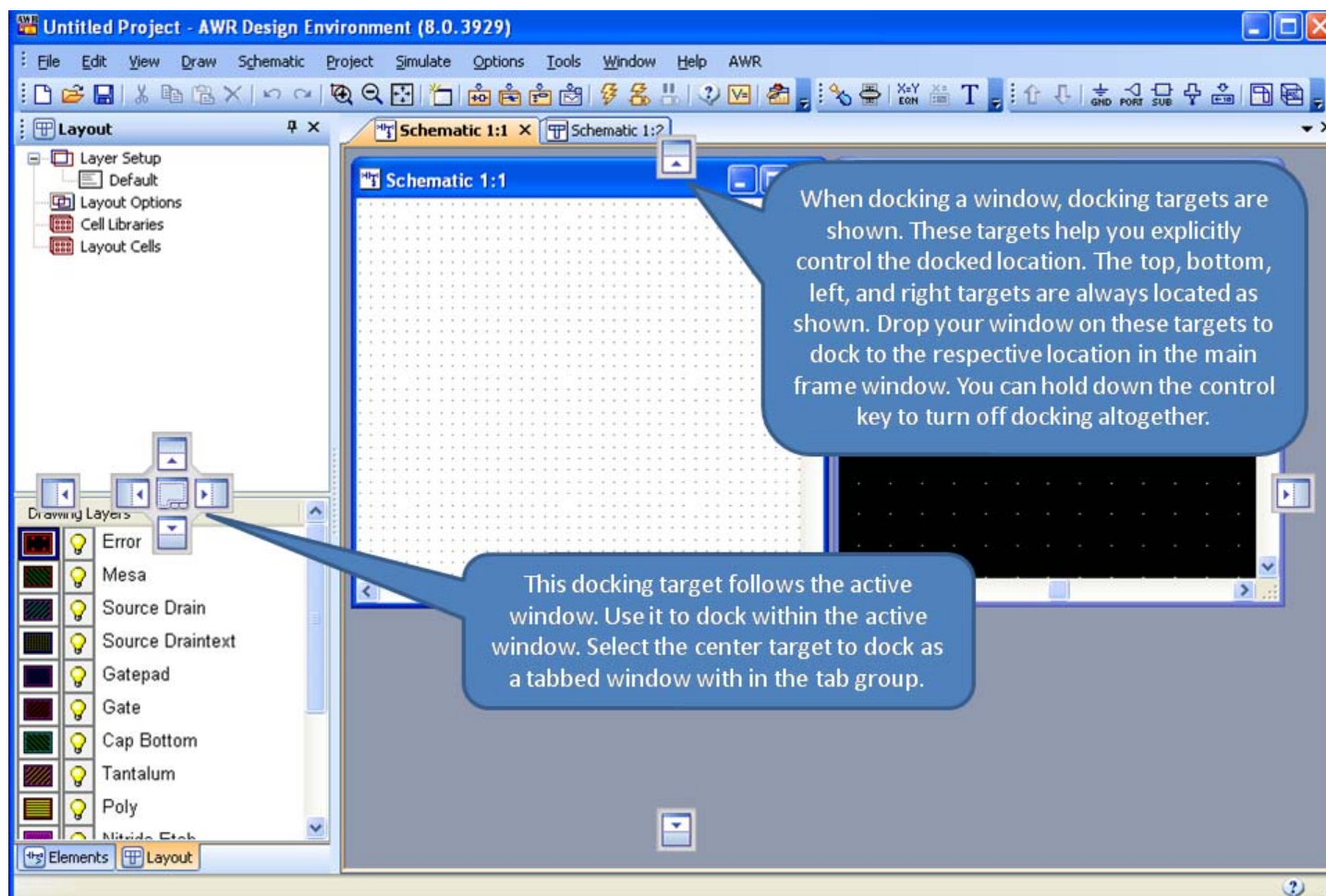
Easy to use just got EASIER!!!



Maximize your useable screen space

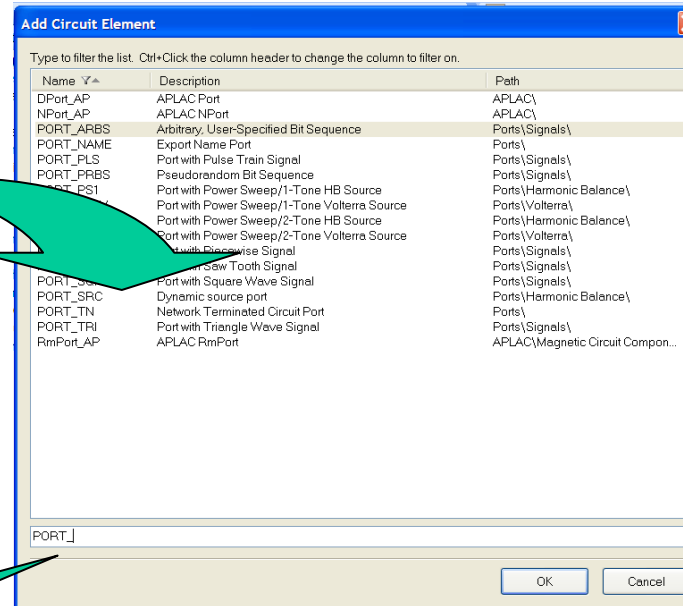
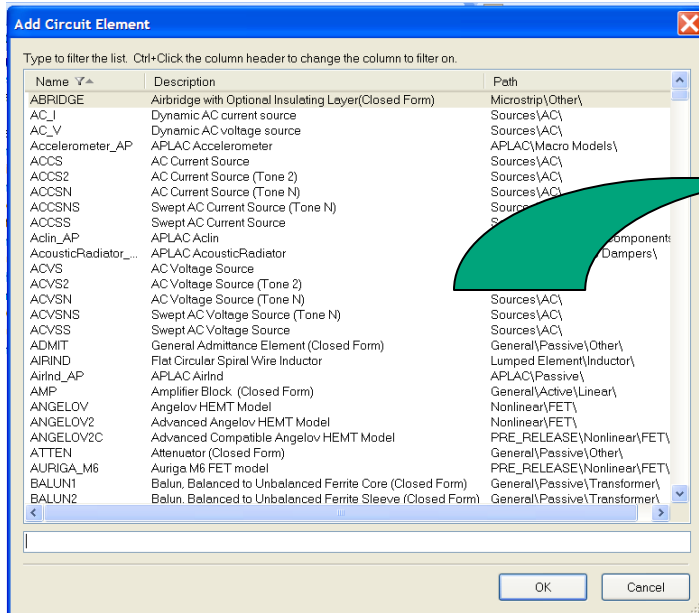
Productivity – New GUI

...packed with customer-generated suggestions & input



5 Quick tips

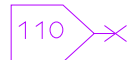
Tip 1: Add Element Dialog



Type in element name
or keyword(s)

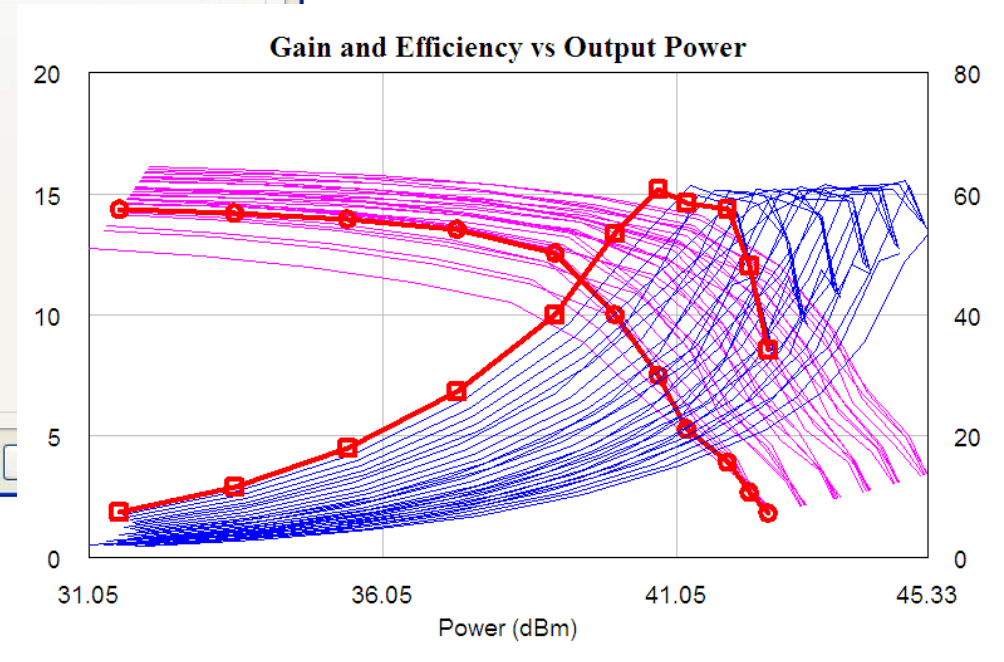
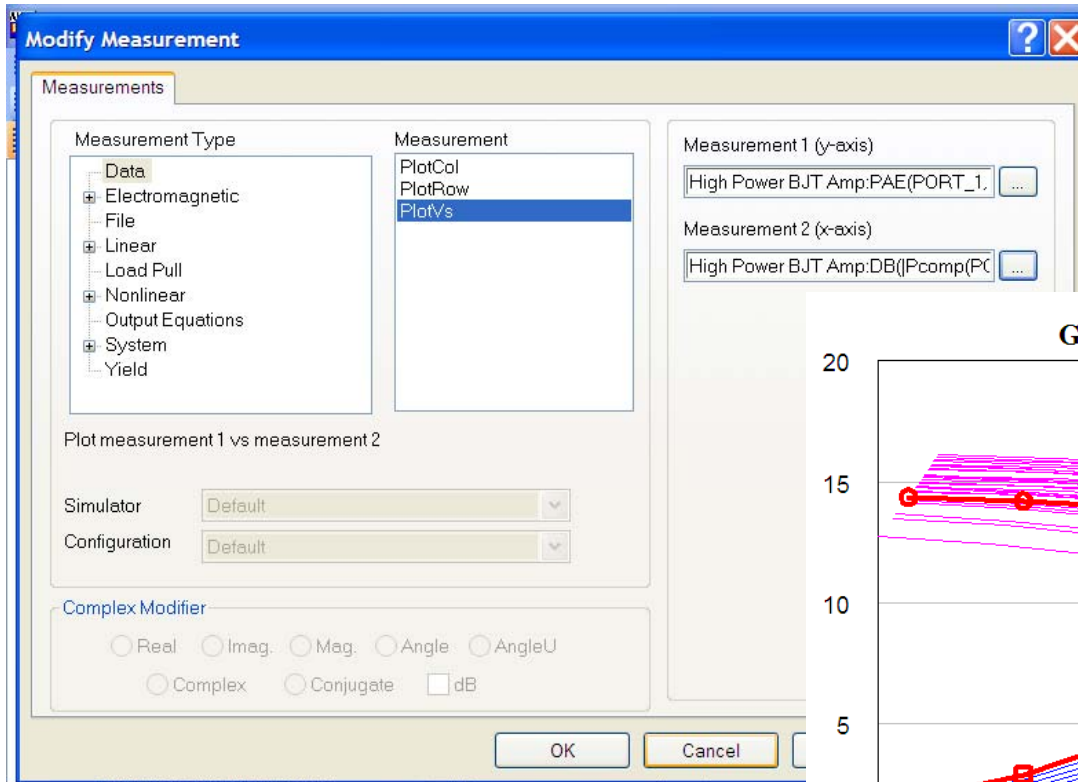
- From Schematic, CTRL+L to open
- CTRL-click on column header to change filter

PORT_ARBS
P = 1
Z = 50 Ohm
RATE = 1 GHz
SEQ = {1,0,1,0}
SAMP = 8
HI = 1 V
LO = 0 V
TR = 0 ns
TF = 0 ns
TYPE = NRZ
WINDOW = DEFAULT



5 Quick tips

Tip 2: Plot Measurements



- Plot a measurement vs. another
- Works across simulators

5 Quick tips

Tip 3: Finding Example Projects

Open Example Project

Type to filter the list. Ctrl+Click the column header to change the column to filter on.

Name	Keywords
128QAM_ADJ_channel_B...	VSS.Install,128QAM_ADJ_channel_BER,Interferers,Jammers,PWR_SPEC,IQ,BER,QAM_BERREF
16_Way_Power_Divider.e...	MWO.Install,16_Way_Power_Divider,Couplers,Layout,Tuning,S
16QAM_BER_SER.emp	VSS.Install,16QAM_BER_SER,BER,BER,QAM_BERREF,PWR_SPEC
16QAM_EVM_IQ_Imbalan...	VSS.Install,16QAM_EVM_IQ_Imbalance,EVM,RF_Impairments,Circuit_CoSimulation,IQ,PWR_vsT,S,EVM
16QAM_IQ_Imbalance.emp	VSS.Install,16QAM_IQ_Imbalance,Getting_Started,IQ,PWR_SPEC,EVM,PS
16QAM_with_Amp_and_B...	VSS.Install,16QAM_with_Amp_and_BER,Amplifier,Circuit_CoSimulation,IQ,E
18Ghz_LPF.emp	MWO.Install,18Ghz_LPF,Filters,EMSightX_Models,S
2_QPSK_Signals_BER.emp	VSS.Install,2_QPSK_Signals_BER,Interferers,Jammers,PWR_vsT,WVFM,F
3_StageCMOS_Opamp.e...	AO.Web,3_StageCMOS_Opamp,Hspice,Simulation,Vtime,VTG,Eqn,VDC
32_Carrier_QPSK_CCDF.e...	VSS.Install,32_Carrier_QPSK_CCDF,CCDF,PWR_SPEC,PWR_vsT,CCDF
3Bit_Programmable_Coun...	AO.Install,3Bit_Programmable_Counter,Layout,Simulation,Vtime
3D_Plot.emp	MWO.Web,3D_Plot,Graphs,IVCurve,PAE
4400MHz_Interdigital_Filter...	MWO.Install,4400MHz_Interdigital_Filter,F
50_ohm_s_z_EM.emp	MWO.Web,50_ohm_s_z_EM,Measurement
64bit_Laser_Driver.emp	MWO.Web,64bit_Laser_Driver,Harmonic,Balun,Integrity,Vtime,V
64QAM_OFDM_BER.emp	VSS.Install,64QAM_OFDM_BER,Coding,BER,QAM_BERREF,BER,PWR,S
7Ghz_Amplifier.emp	MWO.Install,7Ghz_Amplifier,Amplifier,PCB,Layout,E
802_11a_RX_Sensitivity.e...	VSS.Install,802_11a_RX_Sensitivity,WLAN,IQ,SPECMA,PWR_SPEC,N,BI
802_11a_TX.emp	VSS.Install,802_11a_TX,WLAN,WVFM,PWR_SPEC

Open Example Project

Type to filter the list. Ctrl+Click the column header to change the column to filter on.

Name	Keywords
CPW_Layout.emp	MWO.Install,CPW_Layout,MMIC,Layout
Distributed_Amplifier.emp	MWO.Install,Distributed_Amplifier,Amplifier,MMIC,Layout,S,LSSnm
MMIC_Two_Stage_Amp.emp	MWO.Install,MMIC_Two_Stage_Amp,MMIC,Layout,Linear,Tuning,DRC,S,NF

mmic layout

OK Cancel

Type in key words for example

- Same as Add Element, but for File->Open Example

5 Quick tips

Tip 4: Auto Hide Status Window

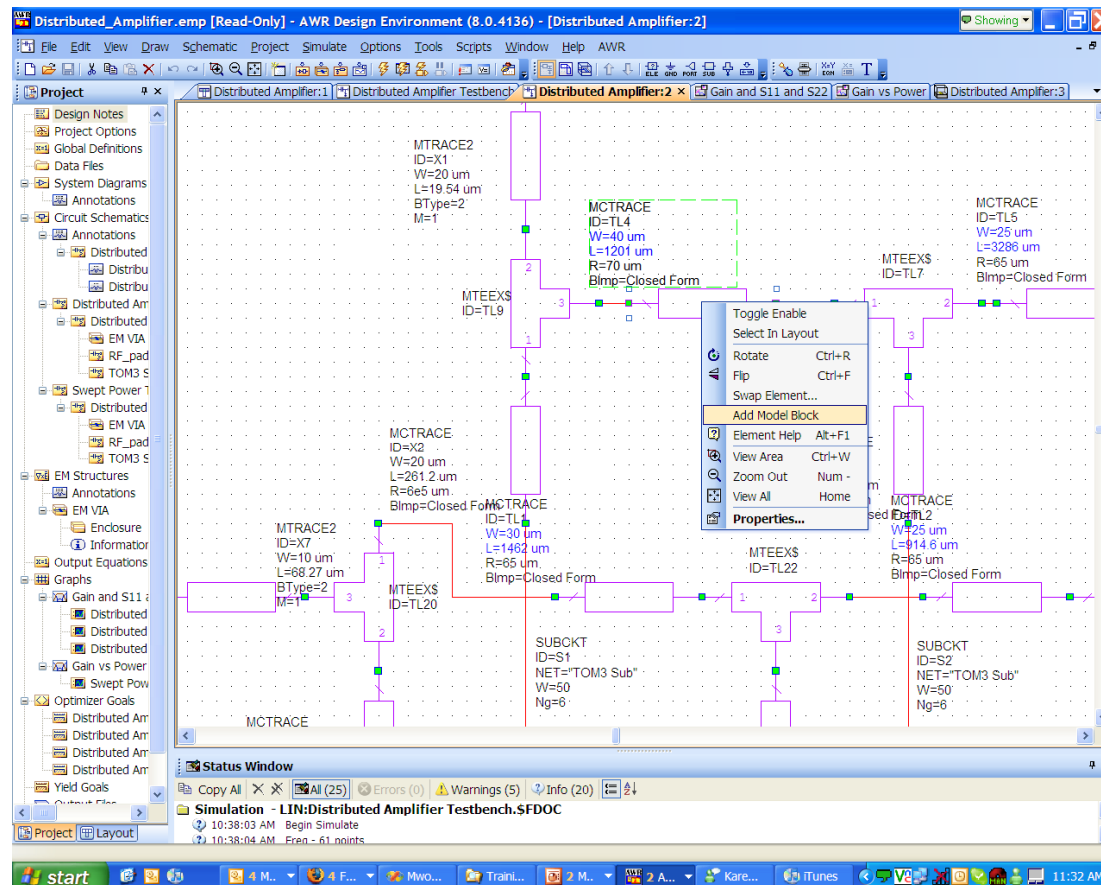
1. Click push-pin to enable

2. Put mouse pointer Over "Status"

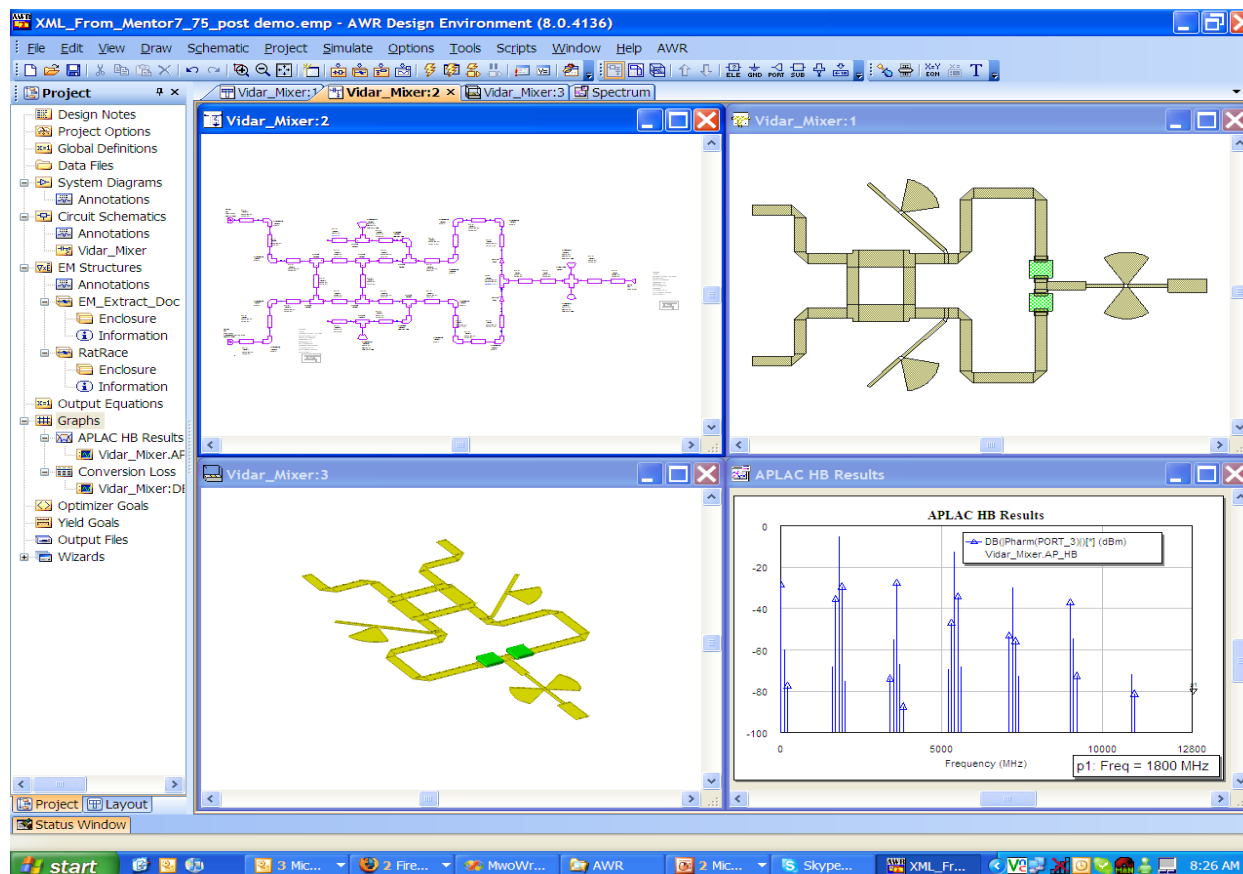
5 Quick tips

Tip 5: Add Model Dialog

- Eliminates error in substrate selection
- Speeds up getting to simulation



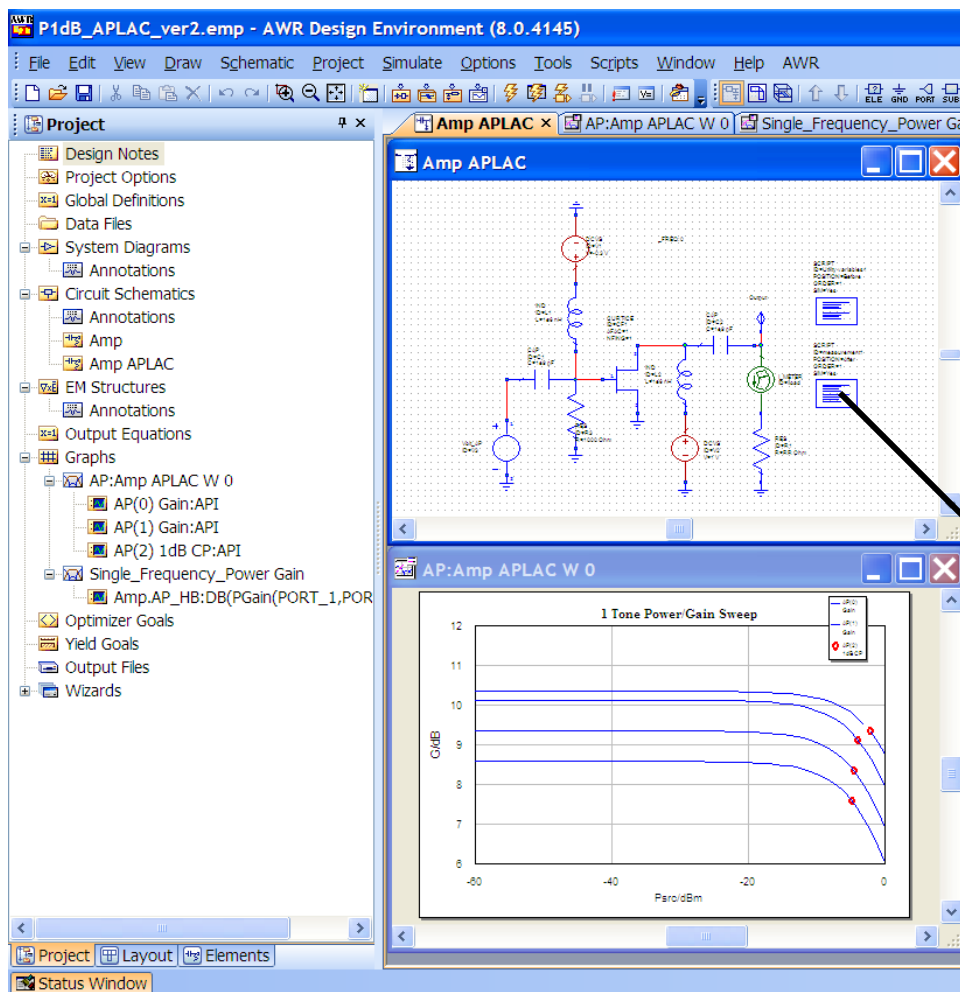
...now included as standard with all MWO nonlinear analysis



Improved Performance: Up to 100x faster nonlinear noise analysis and 90% less memory

...including *powerful* scripting technology!!!

- Scripts for Pre- and Post-simulation control

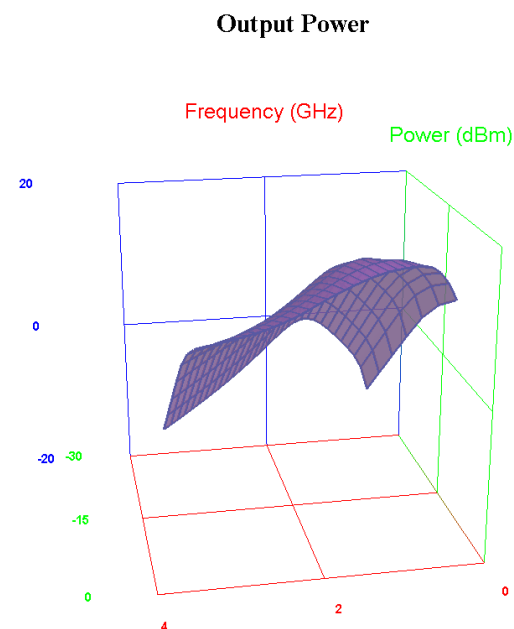


The screenshot shows the 'Element Options: SCRIPT - Script block for Aplac simulations Properties' dialog box. The 'Editor' tab is selected, showing a script for a 1 Tone Power/Gain Sweep. The script includes functions for calculating source power, load power, gain, and gain in dB, and a sweep loop. An arrow points from the 'Amp APLAC' schematic in the previous figure to the 'SCRIPT' block in this dialog box.

```
Function PsrcW $ available source power in Watts  
+ 1m*1010*(PsrcBm/10)  
  
Function PloadW $ load power in Watts  
+ Re(SpectralLine(Output.1)*Conj(SpectralLine(load.1)))/2  
  
Function Gain $ Gain  
+ PloadW/PsrcW  
  
Function GaindB $ Gain in dB  
+ 10*log10(Gain)  
  
Sweep "1 Tone Power/Gain Sweep"  
+ HB FC=fmeas ERR=1u  
+ LOOP 4 Var RR LIN 25 100  
+ LOOP PsrcSteps VAR PsrcdBm LIN PsrcStart PsrcStop  
+ WINDOW 0 GRID  
+ X "Psrc" "dBm" PsrcStart PsrcStop  
+ Y "G" "dB" -20 60 AUTOSCALEY  
  
Show  
+ WINDOW=0 Y GaindB PEN=1 NAME="Gain"  
  
If NewLoop  
  Call Gain1dB=GaindB-1.0; flag1dB=1  
EndIf  
If ((GaindB<Gain1dB) AND flag1dB)  
  Call flag1dB=0; P2=PsrcdBm; G2=GaindB  
Repeat
```

- **Speed** – solves your nonlinear simulations faster

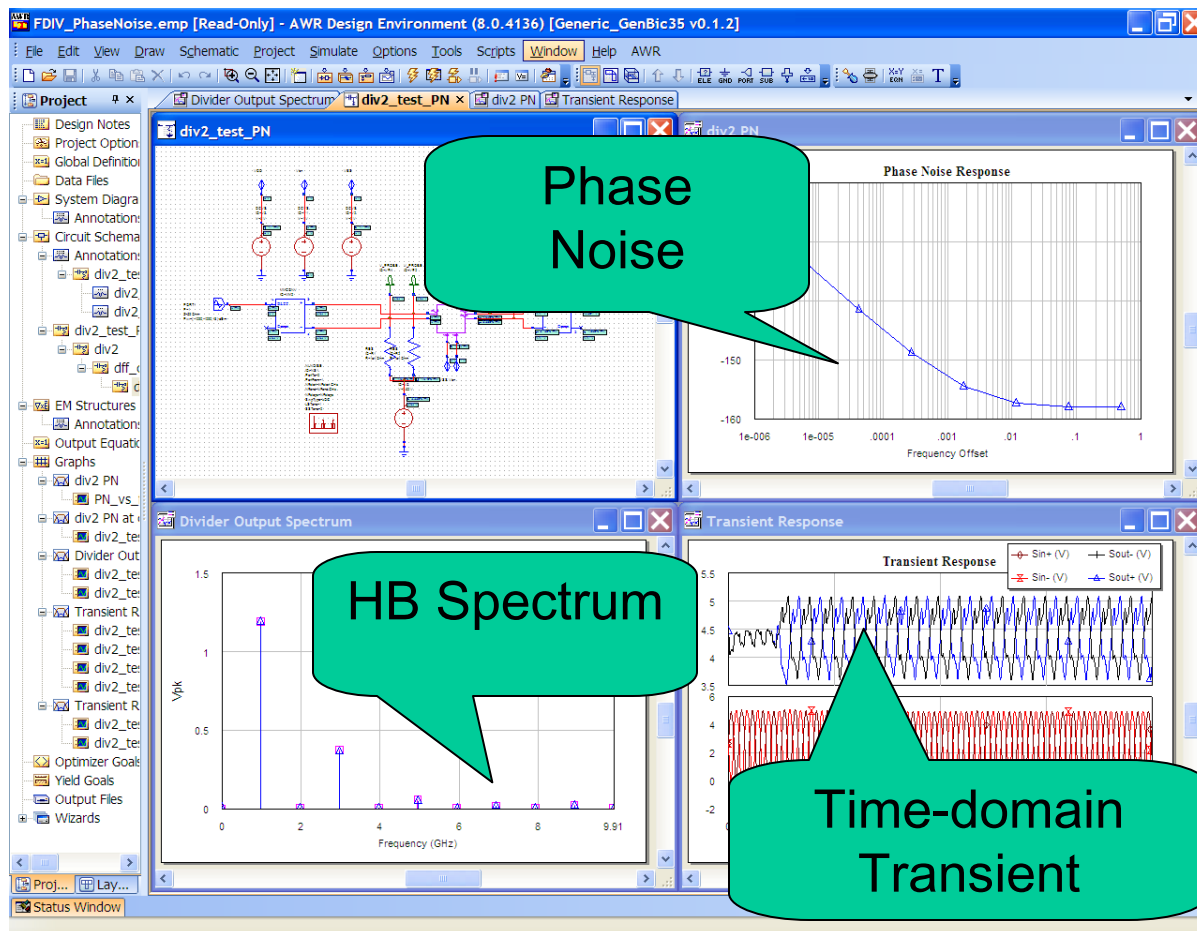
Simulator	Speed*
MWO+APLAC	8.7 sec
MWO	43.4 sec
competitor A	327.7 sec



- **Capacity** – developed for thousands of devices
- **Productivity** – Microwave Office ease-of-use

*high-density HBT MMIC circuit

Innovation – APLAC HB/TRAN



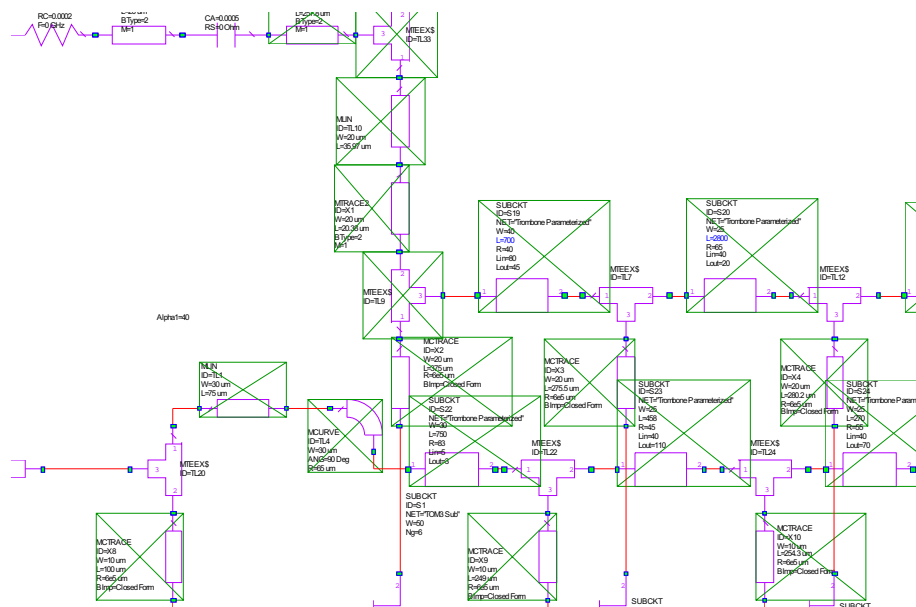
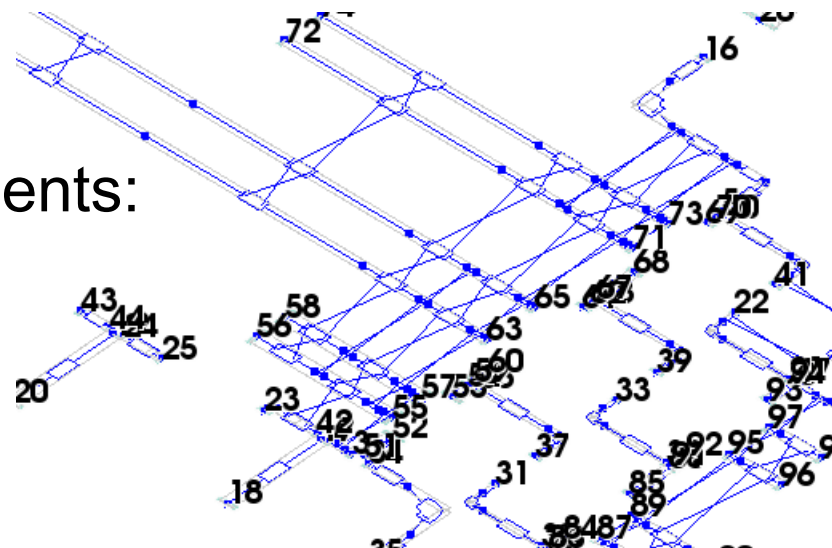
For
RF/microwave
transient
simulations

All from 1 schematic!

DC
HB
Nonlinear Noise
TRAN
AC

- Available as an option to Microwave Office

- Enhanced models
- Now supports schematic elements:
 - Microstrip lines & discontinuities
 - Stripline lines & discontinuities
- All coupled...even with iNets

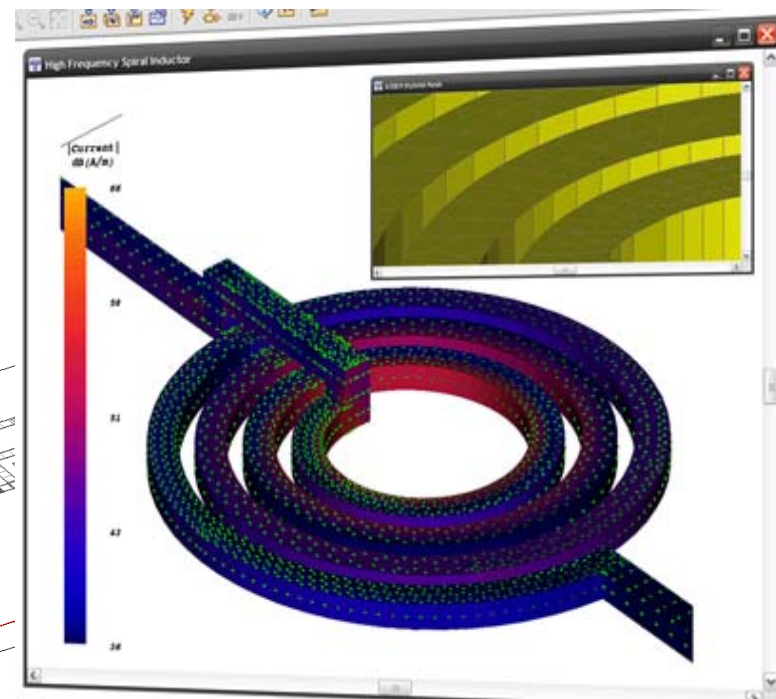
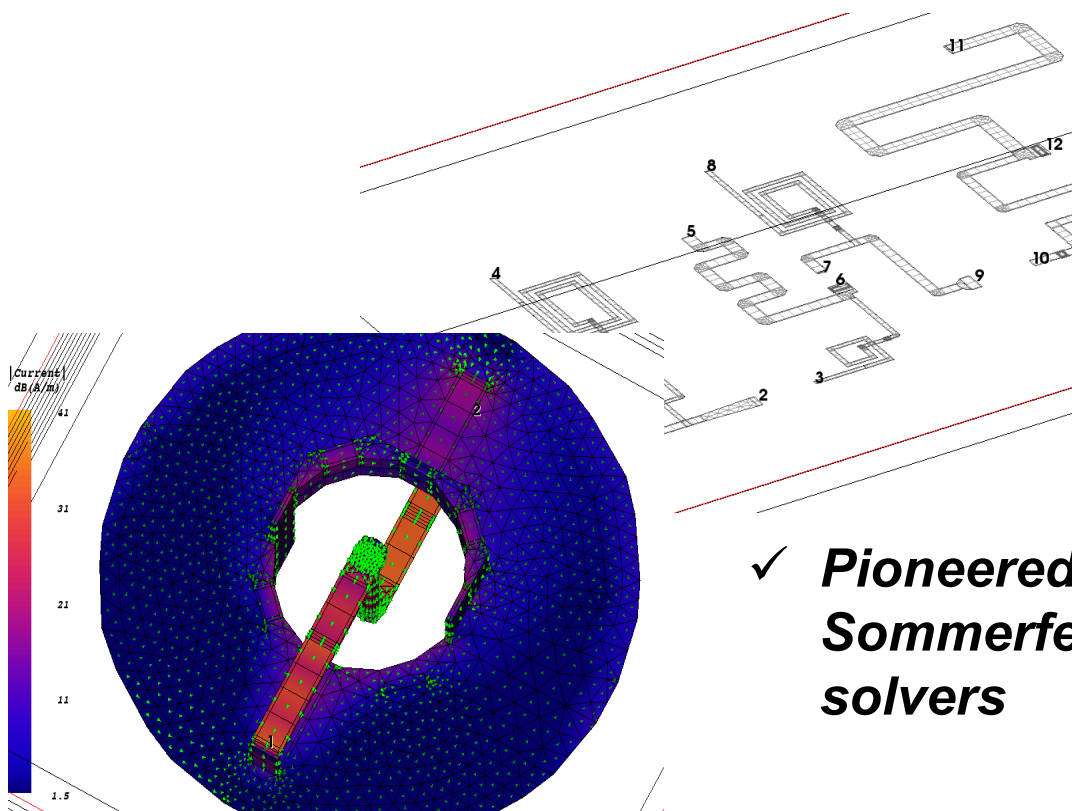


EM_Extract_Doc_extract_netlist.txt [read-only]

MLIN	165	9	ID="194"	W=1.e-005	L=1.2225e-005	MSU
M2CLIN	164	13	165	139	ID="195"	W1=1.e-005 W2=
MLIN	138	16	ID="196"	W=2.e-005	L=9.45e-005	MSUB="SUE
MLIN	146	164	ID="197"	W=1.e-005	L=9.9625e-005	MSU
MLIN	77	78	ID="198"	W=3.e-005	L=3.e-006	MSUB="SUE
MCURVE2	127	128	ID="199"	W=1.e-005	ANG=1.5708	R=3
MLIN	163	143	ID="200"	W=1.e-005	L=3.7125e-005	MSU
MLIN	5	111	ID="201"	W=2.e-005	L=1.1799e-004	MSU
MCURVE2	117	118	ID="202"	W=1.e-005	ANG=1.5708	R=1
MLIN	69	70	ID="203"	W=2.5e-005	L=2.5e-005	MSUB="SUE
M2CLIN	161	162	117	163	ID="204"	W1=1.e-005 W2=
MCURVE2	135	136	ID="205"	W=1.e-005	ANG=1.5708	R=3
GMCLIN	41	159	160	119	161	ID="207"
M2CLIN	158	141	159	160	ID="208"	W1=1.e-005 W2=
MLIN	75	76	ID="209"	W=3.e-005	L=5.e-006	MSUB="SUE
MLIN	133	23	ID="210"	W=2.e-005	L=1.e-005	MSUB="SUE
MBENDR	133	134	ID="211"	W=2.e-005	MSUB="SUB16"	
DEF98P	1	2	3	4	5	6 7 8 9

Innovation - AXIEM

- 3D Planar EM technology
- An option to Microwave Office
 - Available thru the EM Socket



✓ ***Pioneered to overcome limitations in Sommerfeld Integral-based 3D planar solvers***

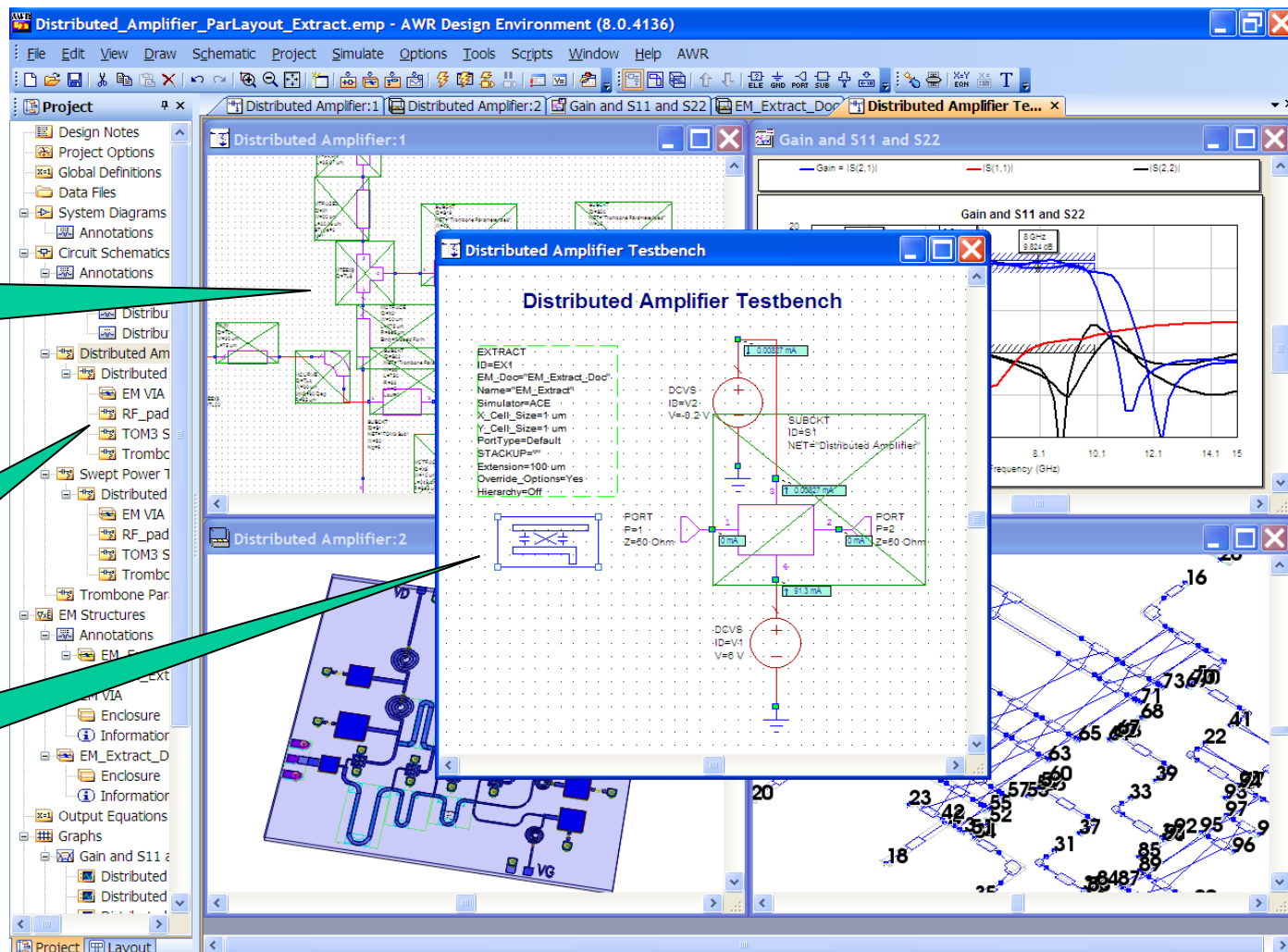
For more info: www.axiem3D.com

EXTRACT - Hierarchy

Extraction
at lower levels

Hierarchical
design

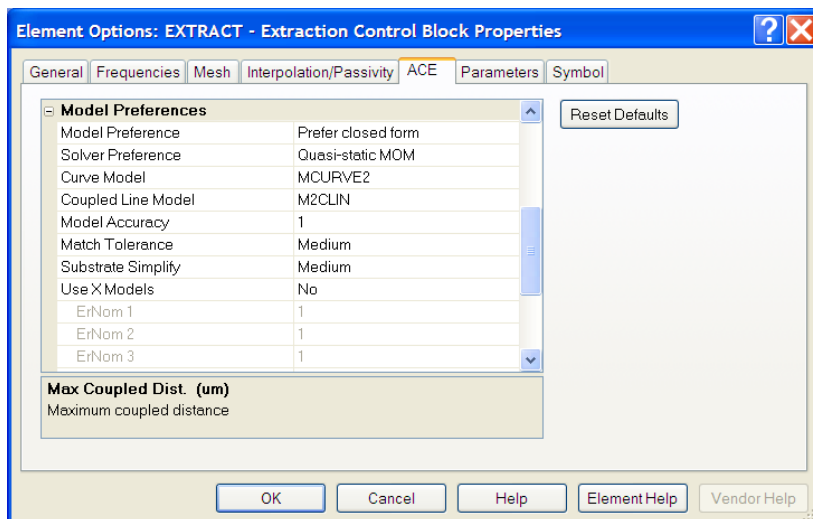
EXTRACT at
upper level



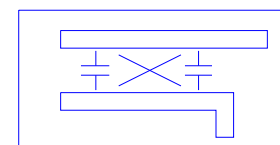
- Supports multiple EXTRACT blocks thru hierarchy

EXTRACT - Hierarchy

- New Options and dialog



```
EXTRACT
ID=EX1
EM_Doc="EM_Extract_Doc"
Name="EM_Extract"
Simulator=ACE
X_Cell_Size=1 um
Y_Cell_Size=1 um
PortType=Default
STACKUP=""
Extension=100 um
Override_Options=Yes
Hierarchy=Off
```

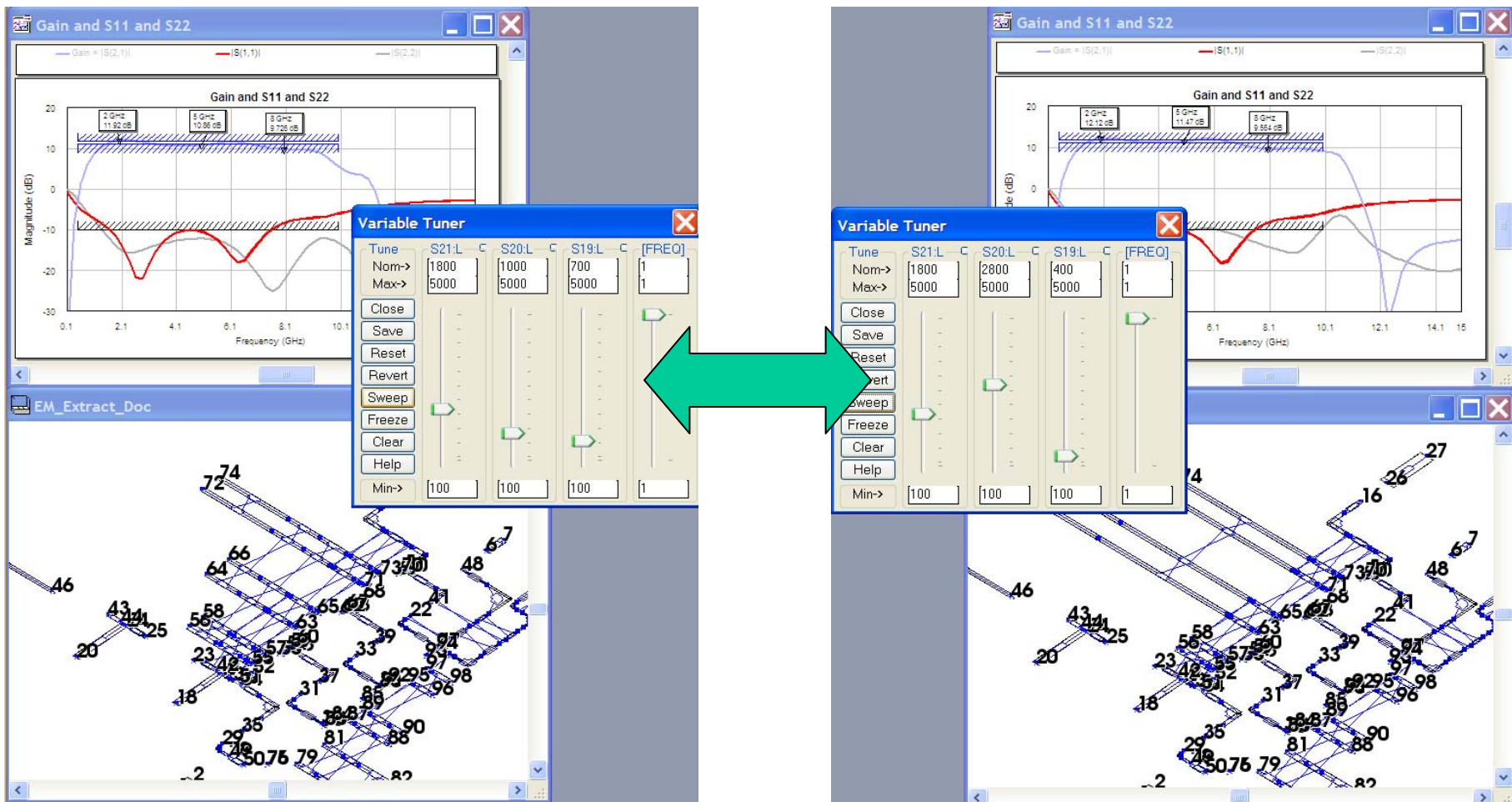


Options control
from block itself

Control for this level in
a hierarchical
EXTRACT

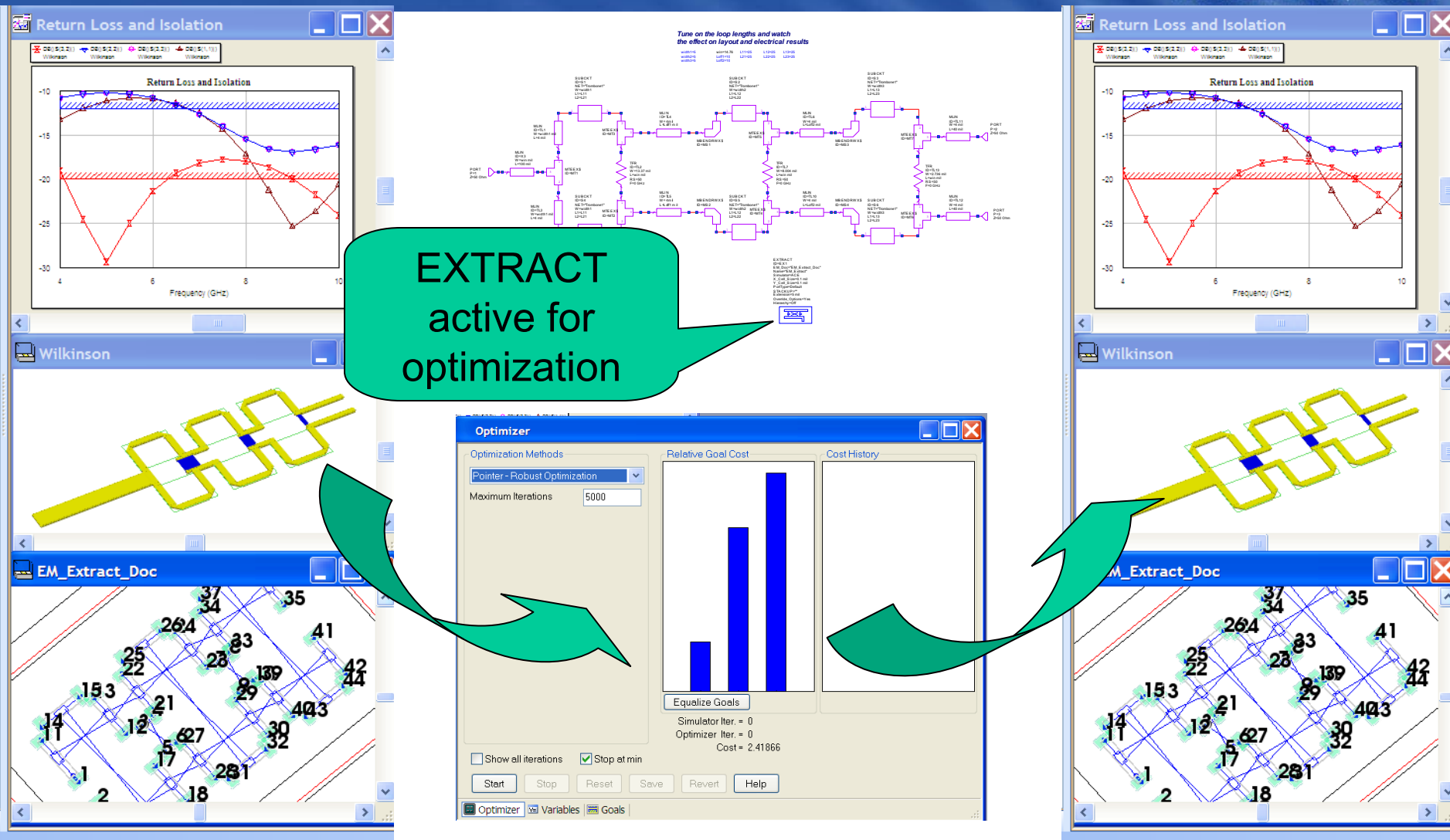
- Better support for transient simulation

EXTRACT - Tune



- EXTRACT executes under control of Tune
- Works with any solver in EM Socket

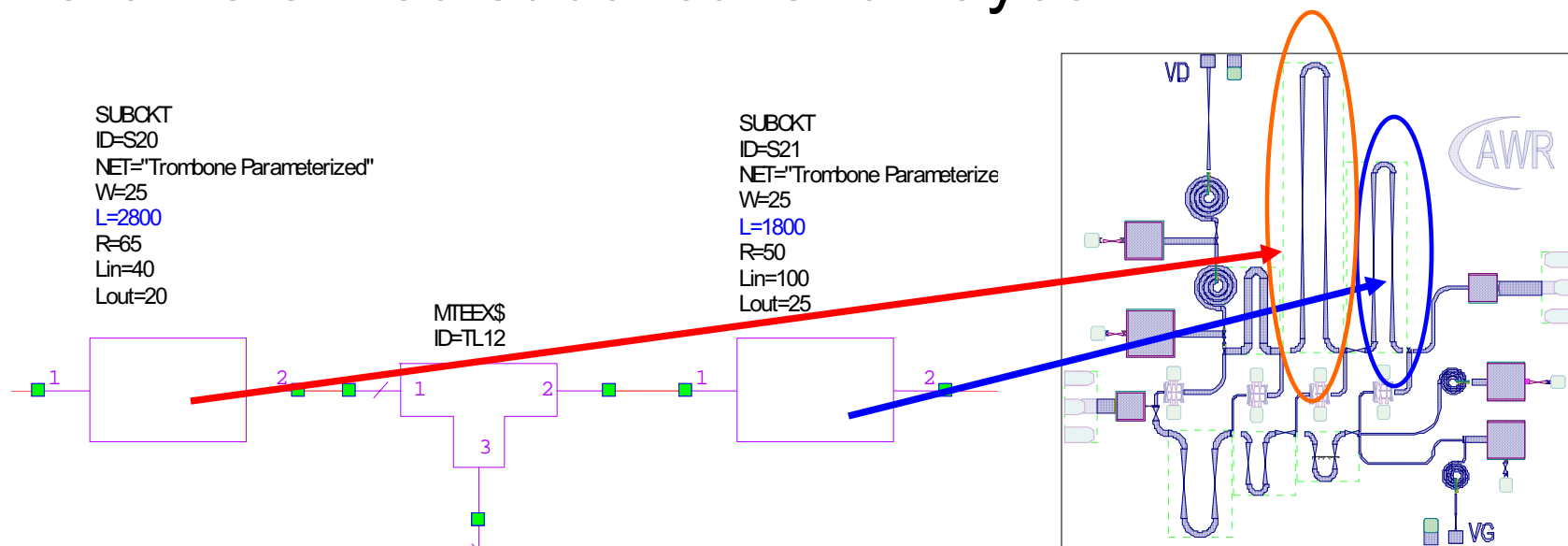
EXTRACT – Optimization & Yield



66 iterations with ACE in less than 2 minutes

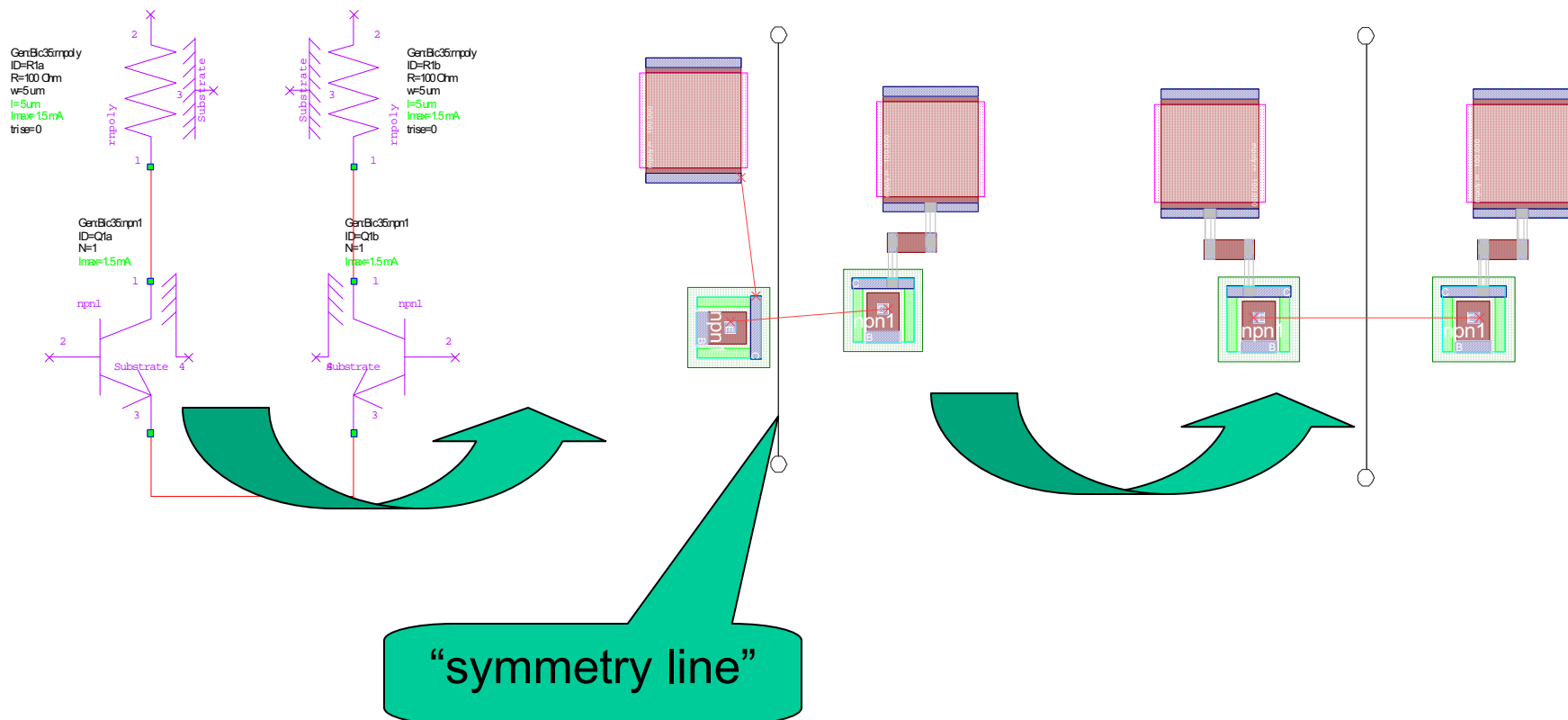
Layout – Parameterized Subcircuits

- Parameterized subcircuits for layout



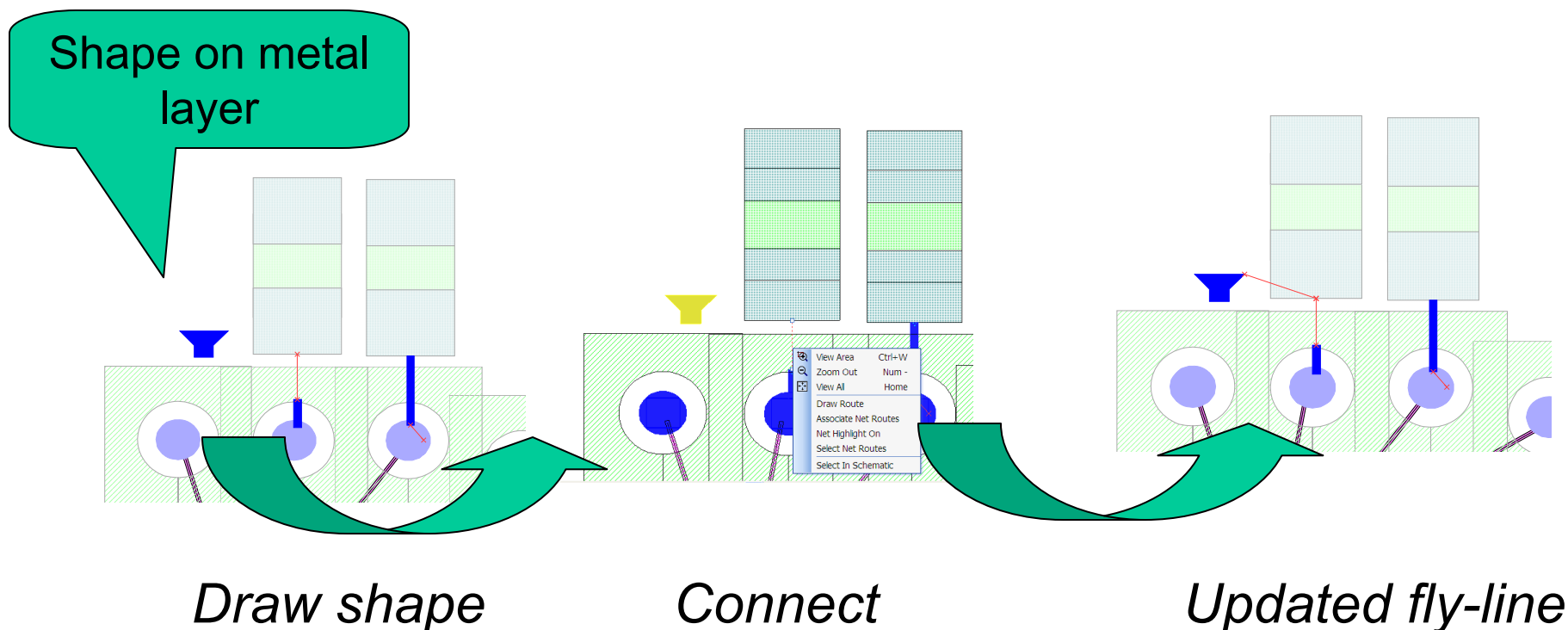
- Now the layout for parameterized subcircuits will show up.
- The subcircuit layout will automatically snap together after any change.

Layout – Placement Mirroring



- Allows quick placement of repeated structures
- Symmetry line (from Draw menu)
- IDs must correspond to each other (Q1a & Q1b)

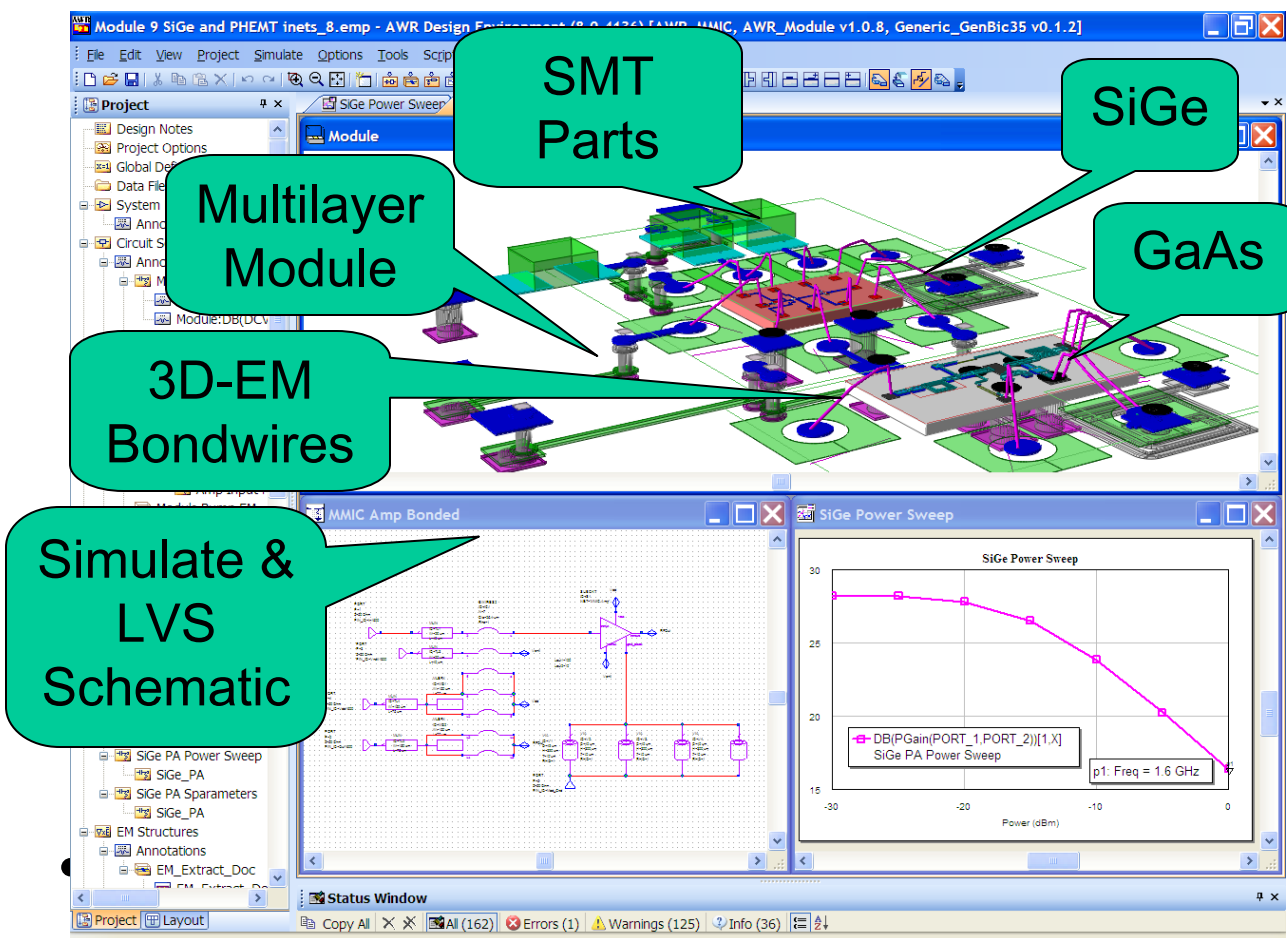
Layout – Shape-Based iNets



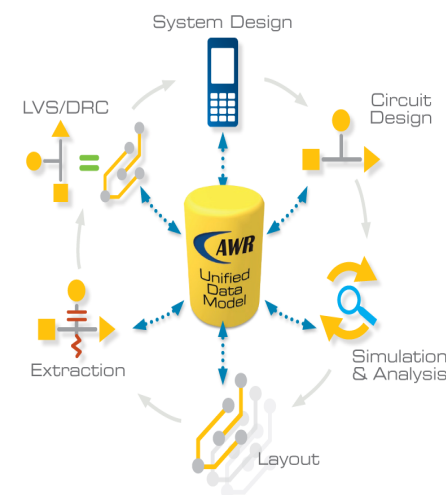
- New connectivity engine recognizes metal shape
- Allows shape to be added to net
- “Recalculates” connectivity fly-line
- Can be EXTRACTed to shape-based solvers

Multi-Technology Flow

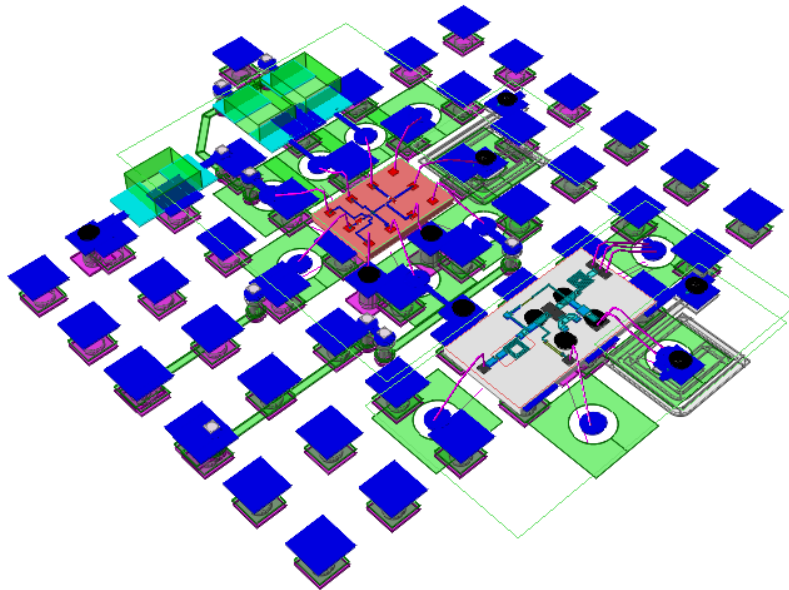
1 project with all your processes for maximum design visibility



**Power,
Precision,
&
Concurrency**



- BGA - Ball Grid Array Model

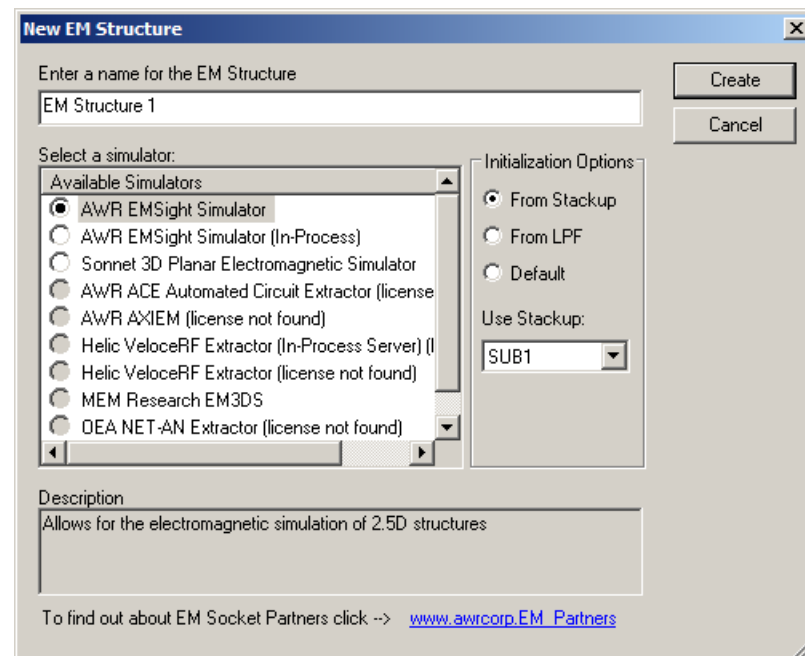
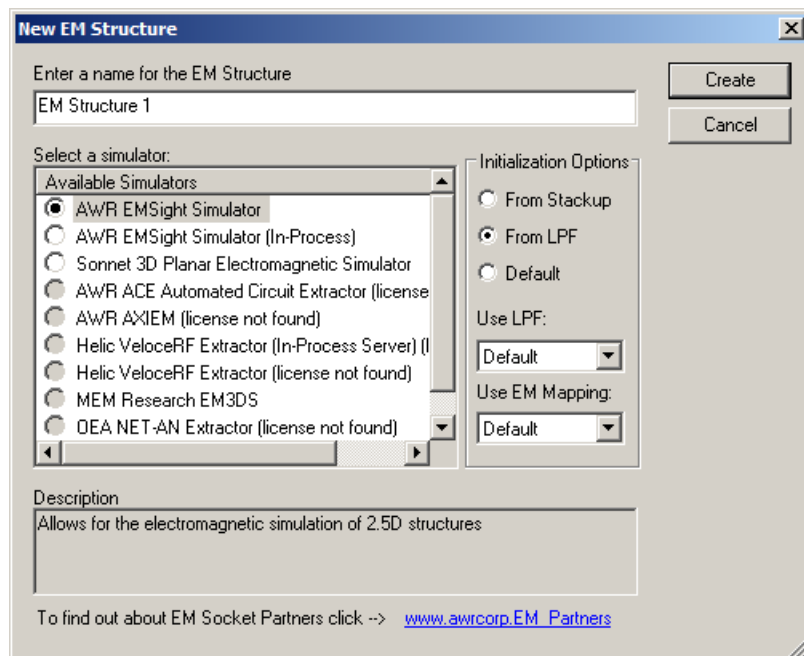


Ideal for modules-on-PCB

Based on internal 3D FEM

- VIAM - Single Via in Multilayer Board
- VIAMD - Pair of Coupled (Differential) vias in Multilayer Board

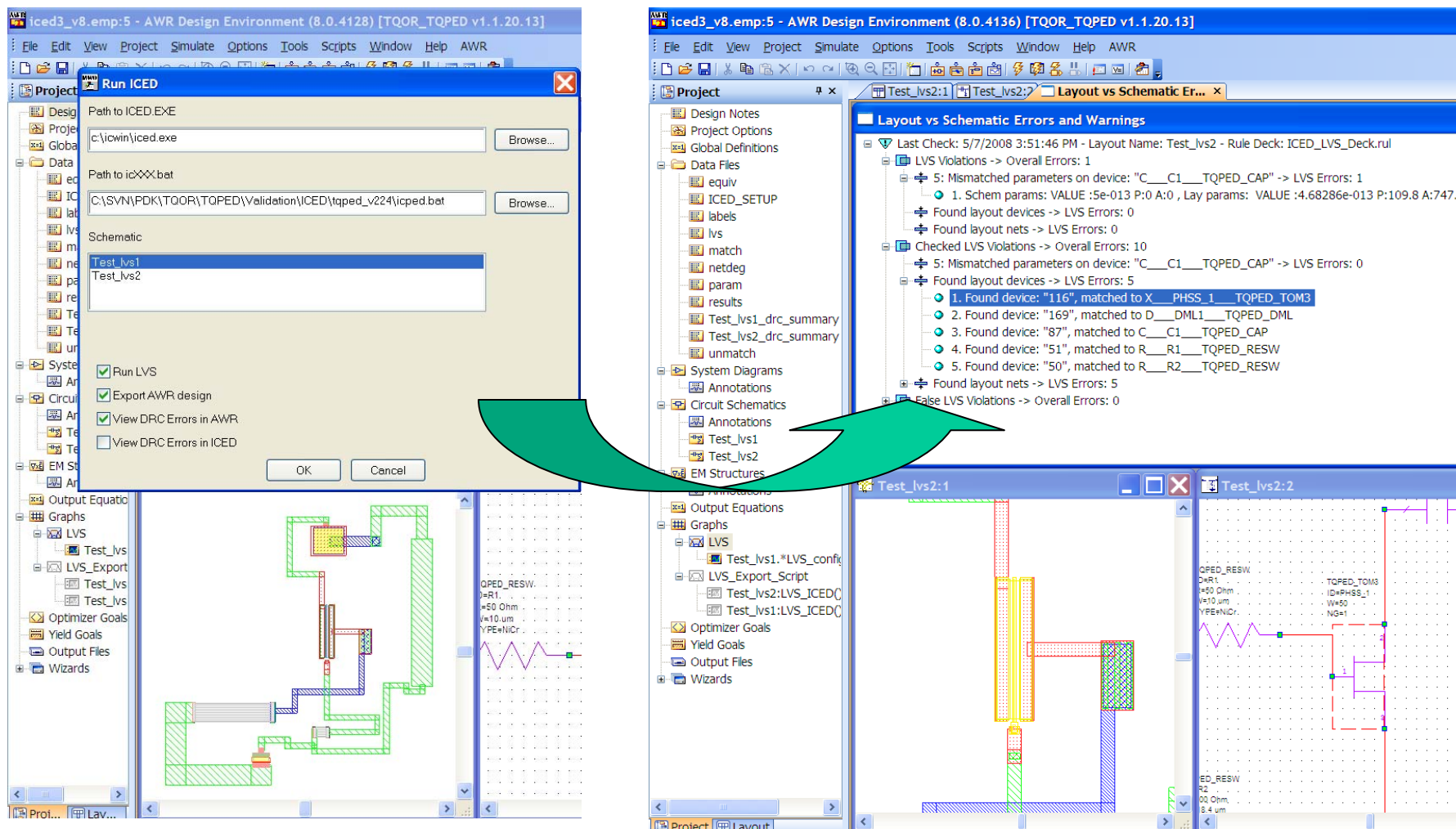
Open Architecture – EM Socket



- Pre-defined EM options from LPF or STACKUP
- DXF or GDSII can now be imported directly into EM

- CST
 - Improved EM Socket robustness and useability
- MEMS Research EM3DS
 - New internal ports with improved calibration
 - Tunable macro-models
- Sonnet
 - Co-calibrated ports directly from AWR EXTRACT ports
- Vector Fields
 - Enhanced 3D modeler
 - 3D periodic structures
- Zeland IE3D
 - Advanced thick metal capability
 - Multi-CPU support

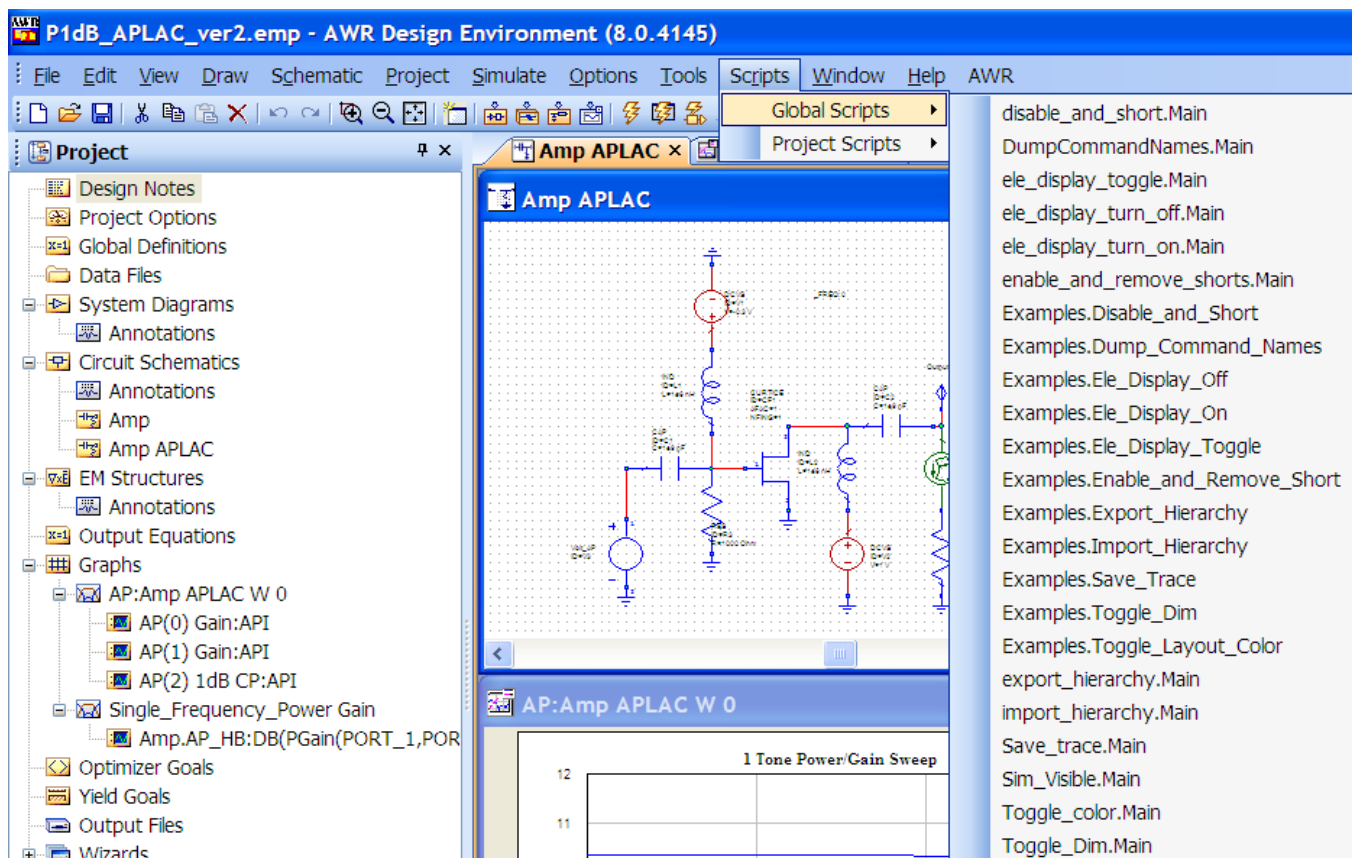
Open Architecture - ICED DRC/LVS



- Access to DRC and LVS
- Cross-probing within AWR Schematic/Layout

Open Architecture – VB Scripting

- Run scripts directly from project



- UDM data and message access for power users

Process Design Kits

- New Foundry Initiative

- ICED support
- APLAC HB and TRAN
- iNets
- ACE



- Initial Participants...

- TriQuint
- WIN
- UMS



- ...and more coming

Microwave Office Version 2008

- Available Now
- Contact your local sales office to learn more
 - <http://web.awrcorp.com/Usa/Contact/Find-a-Sales-Rep>