lem area exists in the need for active devices capable of operation at extremely low current levels.

This paper consists largely of an attack upon these problems. The relative merits of various resistor structures, including the MOS resistor, are discussed, and their electrical characteristics are compared. Active device design for low-power circuit operation is also discussed, and the design of a bipolar transistor structure is described which optimizes the current gain at low current levels. Next, a process technology is described which allows MOS resistors, double-diffused planar epitaxial NPN transistors, and diffused junction isolations to be realized within the same integrated cricuit structure.

Finally, a low-power digital circuit is described which is fabricated using the process technology mentioned previously. It is shown that the use of MOS resistors in the circuit allows the system designer an extra degree of freedom, in that the resistor values, and hence the circuit power dissipation, can be varied by changing the control voltage on the gates of the MOS resistors, so that it is possible to optimize the power-speed trade-off of the circuit, according to the requirements of the overall system.

9.4 LARGE SCALE INTEGRATED BIOPOLAR ARRAYS, Thomas B. Tansil and John L. Bohan, Texas Instruments, Inc., Dallas, Texas.

This paper discusses some of the major factors that should be taken into consideration in the design and fabrication of a large-scale digital integrated circuit array. It is assumed that the type of arrays to be considered are those which have three levels of metalized leads on a slice of silicon. The first level interconnects components to form circuits such as NAND gates. The second and third levels interconnect the gates to generate complex logic functions. The "discretionary" technique is used to interconnect the gates.

The discussion of the gate (unit cell) design will place emphasis on factors which are peculiar to gates in large arrays. For example, the computer program which performs the discretionary wiring places certain constraints on the gate design.

Discussion of the design of the array as a whole will include such subjects as distribution of power and ground within the array, the number of gates that can be obtained on a slice and the geometrical pattern formed by these gates, and techniques being used to package an array on a silicon slice. Also included will be a description of techniques used to obtain gates and flip-flops on a single slice.

Slides will be presented showing how the subjects discussed are being implemented on the LSI contract for the Air Force.[1]

[1] AF33(615)-3546.

9.5 MESA ISOLATION — AN ISOLATION TECHNIQUE FOR INTEGRATED CIRCUITS, Bert L. Frescura, Roger Rusert, and Jon Schroeder, Fairchild Semiconductor, Palo Alto, Calif.

The electrical components of an integrated circuit are presently isolated, using one of the various forms of P-N junction or dielectric isolation. In these techniques, the isolation step is performed prior to the fabrication of the active and passive components such as transistors, diodes, resistors, etc. The objective of this paper is to discuss an isolation technique in which the isolation process steps are performed after the components have been fabricated. These are two major advantages derived from isolating the components after fabrication. First, an ideal wafer surface is available for small geometry photoresist masking. Second, the mesa isolation process requires no process temperature above the silicon-aluminum eutectic temperature and thus the isolation process does not alter diffusion profiles or epitaxial films used for thickness control of transistor collector layers. Another property of the structure is that the device surfaces are buried and this may be useful in low cost packaging. Therefore after the active and passive components have been fabricated (i.e. diffused, deposited, etc.) and interconnected they are ready to begin mesa isolation processing. The wafer is first coated with a dielectric material such as glass and then it is bonded to a substrate. At this point the metal interconnection and device surfaces are buried between the substrate and the wafer. The backside of the wafer is

then thinned to the desired thickness, an isolation mask is applied, and the silicon which connects the electrical components is removed by mesa etching. The feasibility of this structure has been demonstrated using a silicon planar DTμL gate with NiCr thin film resistors.

9.6 A PROCESS FOR CERAMIC DIELECTRIC ISOLATION FOR INTEGRATED CIRCUITS, Thomas H. Ramsey and Tim Smith, Texas Instruments, Inc., Dallas, Texas.

A process for dielectric isolation has been developed which is capable of providing integrated circuits with operational characteristics similar to those of discrete components. The technique makes use of a backside etch with a ceramic filled isolation medium. Life, thermal and shock tests have indicated no detrimental effects from the isolating cement. A total of 1035 logic block and gated latch devices have been supplied for Redman (NSA) and have given very successful results. The yield based on the present process is about 9% and cost studies have indicated that the Redman type device should cost about $2.66 to manufacture.

9.7 A GLASS DIELECTRIC ISOLATION TECHNIQUE, W. L. Price and J. N. Fordemwalt, Motorola Inc., Phoenix, Ariz.

A new approach to dielectric isolation for integrated circuits utilizes a thick layer of a glass (approximately 25 microns) to replace the thin (approximately 1 micron) layer of silicon dioxide which is commonly used as the dielectric medium. This glass layer reduces the inter-device coupling capacitance, increases the dielectric breakdown voltage, and lessens the likelihood of inter-device shorting.

The structure consists of islands of N-type (or N-N+) single crystalline silicon imbedded in a layer of glass which is bonded to a supporting member.

Diffused p-n junction devices are fabricated using deposited oxides and non-oxidizing diffusion ambients. The D. C. parameters for NPN devices are as desired; however, gettering of the lifetime killing impurities by the glass-silicon inter-facial region causes some difficulty in controlling minority carrier lifetime.

The process steps required to fabricate this structure will be described. Data characterizing the properties of the structure and of the glass isolated devices will be presented.

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