The CHIP

CMOS PLL Calibration Techniques

Adem Aktas and Mohammed Ismail

Welcome to The Chip! The article in this column discusses auto calibration of phase lock loops (PLLs), particularly when used as frequency synthesizers in fully integrated radios targeting future generations of broadband wireless applications. These PLLs use wideband voltage-controlled oscillators (VCOs) covering a wide tuning range. A calibration technique is discussed and used in a wireless LAN radio. We hope you find the article of interest.

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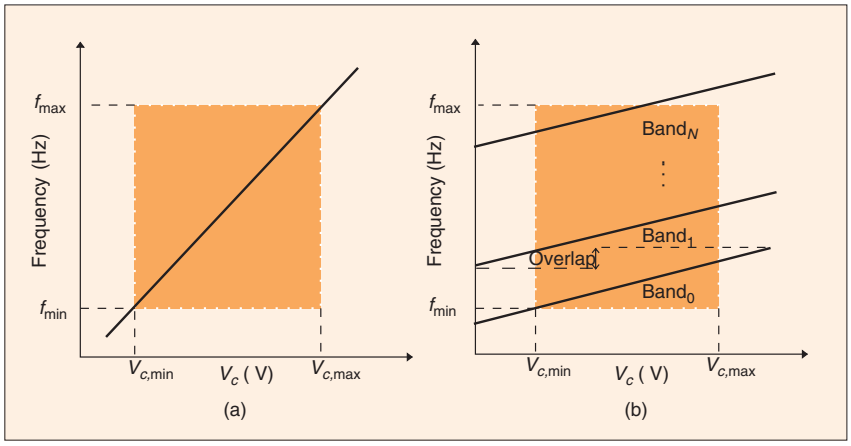
Mohammed Ismail

Modern mobile radios, used in the third (3G) and fourth generations (4G) of wireless standards, are required to support multistandard and multiband operation for backward compatibility between various generations of standards and increased capacity [1], [2]. This, in turn, requires operation in a wide range of frequency bands and channel bandwidths for the fully integrated PLL frequency synthesizers under process variations and operating conditions. In submicron complementary metal-oxide semiconductor (CMOS) technologies, the supply voltage is scaled with channel length; this has led to a smaller tuning voltage range. Smaller tuning voltage and wide tuning requirement lead to a large VCO gain, which increases the phase noise at the VCO, and, hence, PLL output. Instead, we propose that a wide tuning range is realized by digital and continuous (analog) tuning circuits to reduce the VCO gain. The digital tuning scheme divides a wideband tuning range into smaller bands. The continuous tuning control is a control line for the PLL. A PLL calibration circuit is used to assign the proper subband for a given channel frequency so that PLL can lock within tuning voltage range. PLL calibration techniques are described and a new auto-calibration circuit is presented.



1. (a) Single tuning curve. (b) Tuning range divided into subbands for a wideband VCO operation.

BACKGROUND

A wideband VCO with a continuous tuning range, as shown in Figure 1(a), results in a large VCO gain, especially in submicron CMOS technologies which have scaled supply voltage due to smaller gate breakdown voltages. A large VCO gain is not suited for fully integrated VCO solutions in a transceiver environment because a large VCO gain causes increased translation of noise on the tuning line into phase noise around oscillation frequency. Furthermore, the VCO gain significantly varies over the wide tuning range, this, in turn, degrades the PLL performance. One solution is to divide the tuning range into discrete smaller bands, as shown in Figure 1(b) [3]. An example of wideband VCO employing both discrete and continuous controls is shown in Figure 2. The PLL tune line is connected to V_{CNT} for continuous control and discrete control is provided externally by digital control word $T(0:N)$ as shown in Figure 3.

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One of the major implementation issues with this type of wideband VCO is the selection of a proper trim code for desired channel frequency such that the continuous control voltage V_{CNT} in Figure 4 should fall into the range of desired charge pump (CP) output voltage range, i.e., $V_{CP\_out,min} \leq V_{CNT} \leq V_{CP\_out,max}$, when the PLL is locked. Unfortunately, the tuning curves in the subbands move up or down due to process, temperature, bias, and supply variation (PTB). The supply and bias variations usually have less impact on the tuning range variation since an offchip voltage regulator and onchip bandgap bias reference current are used. The temperature variation has considerably less impact on the tuning curves compared to the process variations. The most important contribution to tuning variation comes from the process variation. Here, design and implementation of PLL calibration architectures and circuits to assign a proper trim code for a given channel frequency are presented.

First, process variation effect on the tuning range is discussed. Next, PLL calibration techniques are described. A new PLL auto-calibration technique is presented. Also, timing issues for PLL lock time due to calibration operation is also discussed. Finally, an implementation of the proposed calibration circuit is presented.

PROCESS VARIATION EFFECT ON A VCO'S TUNING RANGE

The temperature and bias variations effect on the tuning range depends on the circuit topology and device characteristics, and can be extracted from simulations as absolute maximum and minimum variations of the oscillation frequency in percentage. However, the process variation has a direct impact on the absolute oscillation frequency since the oscillation frequency is equal to $1/\sqrt{LC}$. The tuning range of the VCO in terms of the tank capacitance can be expressed as (assuming typical values):

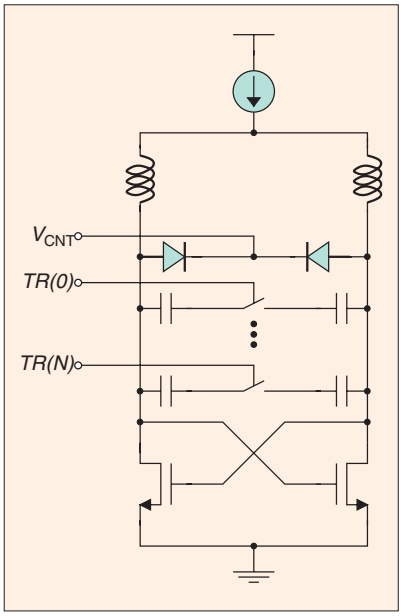
$$TR = \frac{f_{max}}{f_{min}} = \sqrt{\frac{C_{var,max} + C_{SW,max} + C_{par}}{C_{var,min} + C_{SW,min} + C_{par}}}, \quad (1)$$

where $C_{var,max/min}$ is the capacitance variation of the continuous tuning varactor. $C_{SW,max}$ is the maximum capacitance of switched cap for $TR(0:N) = 111\ldots1$. $C_{SW,min}$ is the minimum capacitance of switched cap for $TR(0:N) = 000\ldots0$. C_{par} is the fixed parasitic capacitance from the inductor, interconnects, and active device.

If we consider only the ith subband of the VCO's entire tuning range, then the ith subband tuning range and the tank capacitance relations can be written as for typical process parameters:

$$TR_i = \frac{f_{i,max}}{f_{i,min}} = \sqrt{\frac{C_{var,max} + C_{i,SW} + C_{par}}{C_{var,min} + C_{i,SW} + C_{par}}}. \quad (2)$$

The total tank capacitance is formed by the variable capacitance and the fixed capacitances due to parasitics and switching. The process variation shifts the each subband tuning curve up or down depending on the change in the fixed tank capacitance. If we want to find the absolute frequency shift for the ith subband tuning range due to process variation in capacitances, (2) can be written as

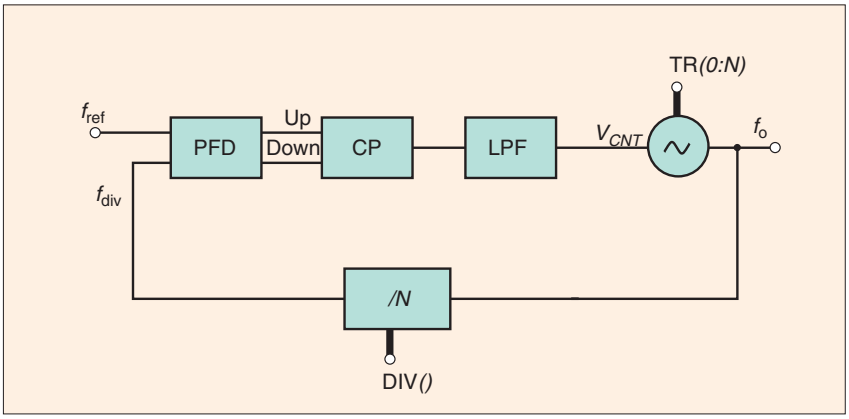


2. Wideband VCO with discrete and continuous controls.

$$TR_{i,up} = \frac{f_{i,max,up}}{f_{i,min,up}} = \sqrt{\frac{C_{var,max} + C_{i,SW,min} + C_{par,min}}{C_{var,min} + C_{i,SW,min} + C_{par,min}}} \quad (3)$$

$$TR_{i,down} = \frac{f_{i,max,down}}{f_{i,min,down}} = \sqrt{\frac{C_{var,max} + C_{i,SW,max} + C_{par,max}}{C_{var,min} + C_{i,SW,max} + C_{par,max}}}. \quad (4)$$

For each subband, the absolute values of maximum and minimum shifts can be calculated by using (3) and (4)



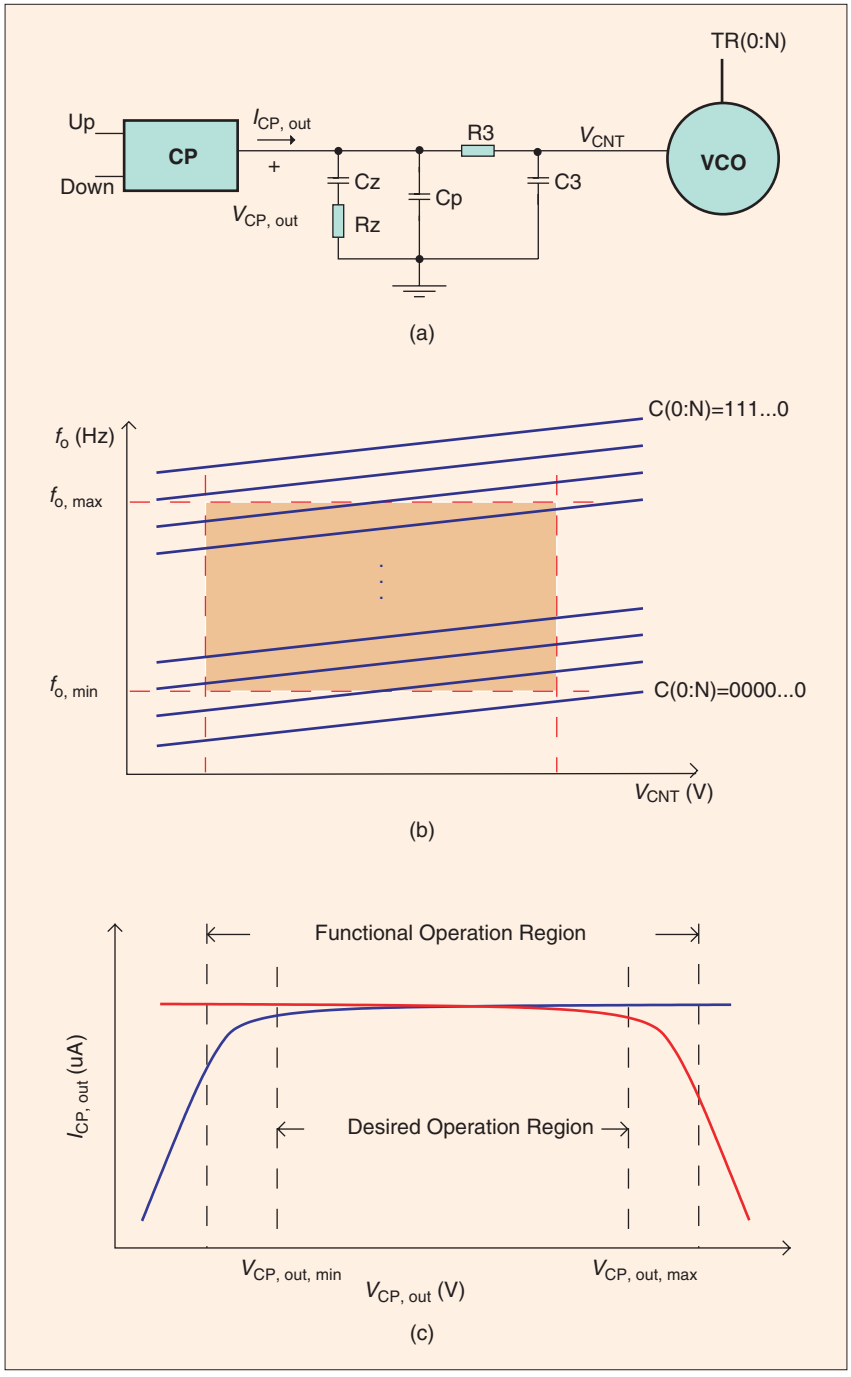
3. An integer-N PLL frequency synthesizer with a VCO having discrete and continuous tuning controls.

along with process variation parameters. Typical component variations for a CMOS process are listed below.

- onchip spiral inductor value variation ±1% <
- gate capacitance variation ±5%
- MIM capacitance variation ±15%
- parasitic capacitances (inductor and interconnects) ±15%.

PLL CALIBRATION TECHNIQUES

There are two approaches to calibrate the tuning range of a wideband VCO in a PLL operation. One approach is to apply the digital control word externally. The other approach is the auto calibration of the digital control word with a PLL calibration circuit. These techniques are presented next.



4. (a) VCO with control inputs. (b) VCO tuning curves divided into subbands. (c) CP output current as a function of output voltage.

External Trimming

External trimming requires the knowledge or the best estimate of trim() code from simulation or measurement. The basic steps for external trimming can be listed as;

- Determine the best trim word TR() for desired operation region from simulation (Monte Carlo simulation) or measurement (measure several chips).
- Write the determined trim word TR() from baseband at the power up.

Since external trimming doesn't correct the process variation, therefore, the continuous tuning curve must take into account the process variation, thus limiting the minimum VCO gain.

Auto Calibration

By PLL auto calibration, the process variation effect to the VCO tuning range can be eliminated, hence, only effects to tuning range are to be considered: temperature and bias variation after trimming. A marginal value of ±1% can be taken for absolute VCO frequency variation due to temperature and bias variation. A conventional PLL calibration algorithm should complete the following steps when performing calibration:

- Open PLL loop from VCO control voltage line.
- Set TR() code minimum or given initial estimated code.
- Measure VCO output frequency for V_{min}.
- Measure VCO output frequency for V_{max}.
- If the measured VCO output frequency $f_{min} < f_o$ for V_{min} and $f_{max} > f_o$ for V_{max}, go to the next line; or else go to next step, else TR() = TR() –1, and go back to line 3.
- Keep the TR() code and close PLL loop.

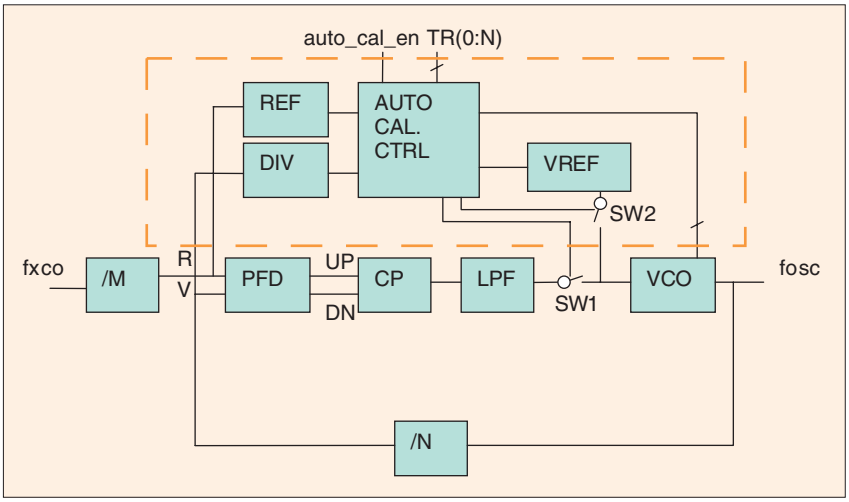
Implementations of the above algorithm or similar ones do exist in the literature [4], [5]. Figure 5 shows a typical implementation of this algorithm. The PLL loop is open with SW1, and V_{ref} (V_{min}, V_{max}) is enforced by closing the switch SW2. PLL divider /*N* is set to the lower end value of f_{min} for

$V_{ref} = V_{min}$ and f_{max} for $V_{ref} = V_{max}$. Counters, REF and DIV, will count the reference R and divided VCO output frequencies V, respectively. Counters will count long enough so that any possible error due to inital phases of R and V signals will be avoided. REF and DIV, will race until one of the counters finishes. If *REF* finishes first, then, the trim code satisfies the lower edge of the tuning range, i.e., $f_o < f_{ref} \times C_{REF}$.

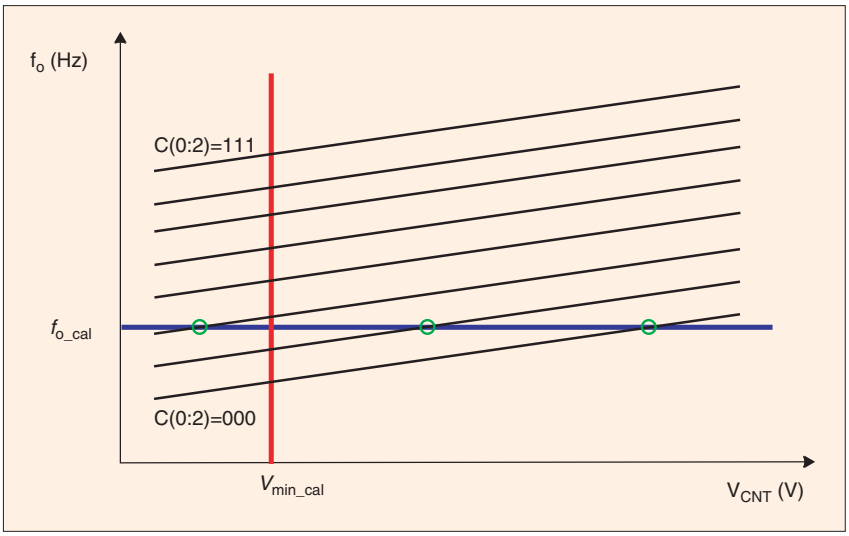
PROPOSED PLL CALIBRATION TECHNIQUE

We want to find the TRIM() code for a given VCO frequency, so that the VCO control voltage $V_{CP\_out,min} \leq V_{CNT} \leq V_{CP\_out,max}$ when the PLL is locked. The proposed PLL calibration method searches TRIM codes from starting from the highest TRIM code toward to find desired code which satisfies $V_{CNT} > V_{min}$, as shown in Figure 6. There is no need to check maximum value of the control voltage, i.e. the $V_{CNT} < V_{max}$ since the TRIM code search starts from the highest value. The search algorithm also can be started from the lowest TRIM code toward the highest one, and checked for $V_{CNT} < V_{max}$.

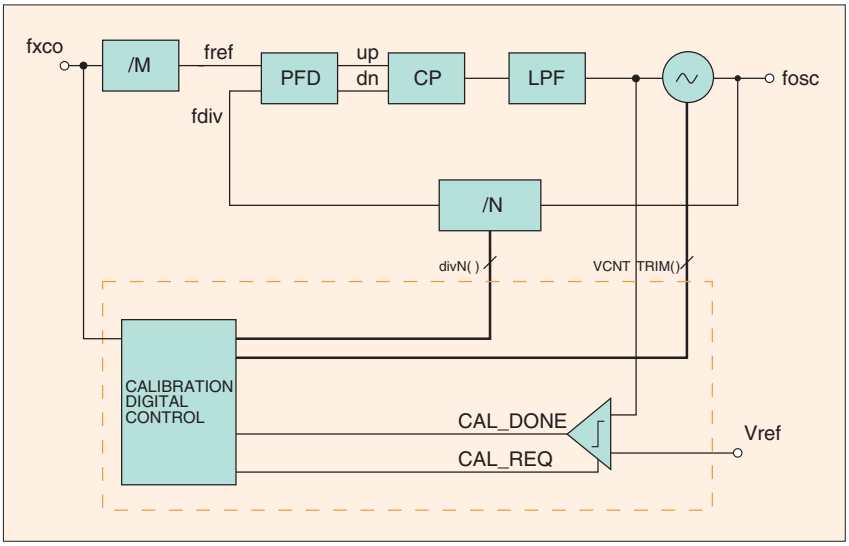
An implementation architecture of the proposed calibration method is shown in Figure 7. The operations flow chart of this architecture is shown in Figure 8. The CALIBRATION DIGITAL CONTROL block controls the calibration operation. The TRIM code is set to maximum, CAL_REQ control signal is set to 1, and the PLL divider coefficient, div$N$(), is set to the calibrated frequency at the start-up of calibration. After setting initial values, CALIBRATION DIGITAL CONTROL waits to allow the PLL to lock and the comparator to settle. Here, the wait time is set to a worst case value of 250 μs (200 μs for PLL to lock and 50 μs to comparator to settle). During wait time, the PLL tries to lock to the calibration frequency with a given TRIM code. If the TRIM code is too high, the charge-pump sends *DN* pulses continuously, which lowers the loop filter voltage (VCO control voltage) to close to 0 V. Also, the comparator compares the VCO control voltage with the



5. Conventional PLL auto calibration architecture.

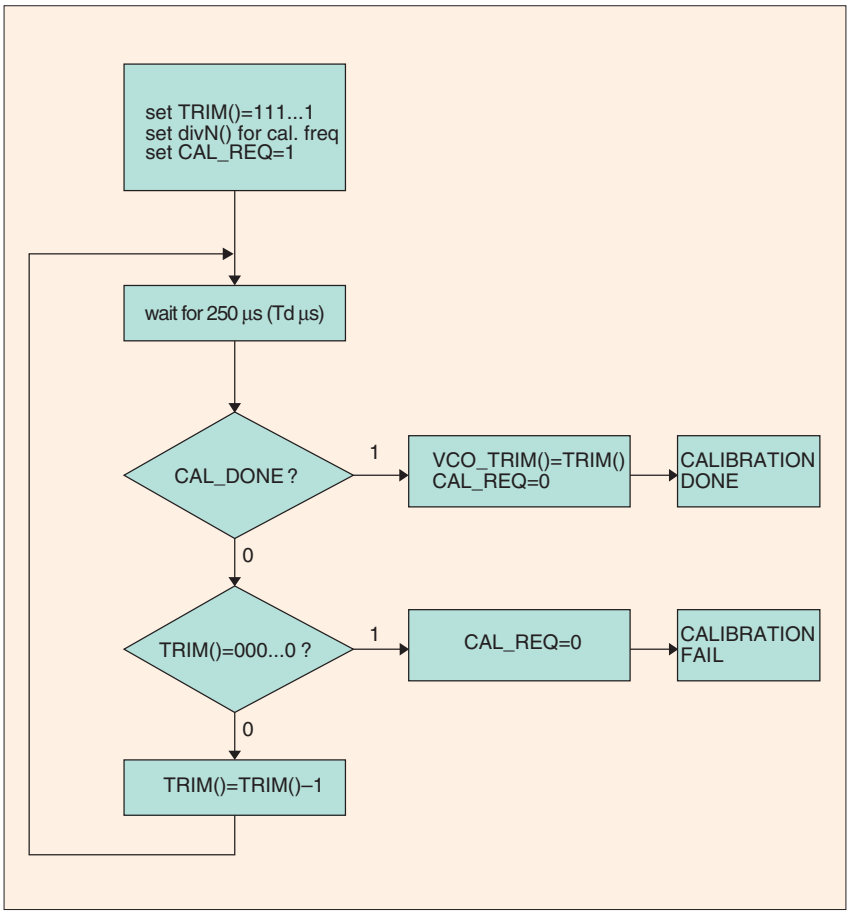


6. The calibration frequency and control voltage.

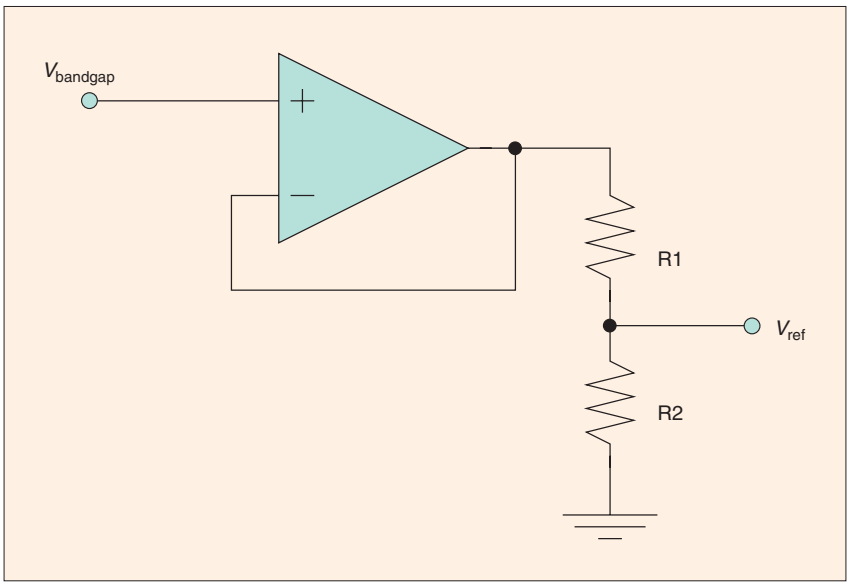


7. Proposed auto calibration architecture.

reference voltage during the wait time, and reaches a final value by the end of the wait time. After wait time, CALIBRATION DIGITAL CONTROL checks the CAL_DONE signal. If it is 1, the TRIM code is set as VCO_TRIM code, and CAL_REQ control signal is set back to 0. If the CAL_DONE signal is 0, the CALIBRATION DIGITAL CONTROL checks the TRIM() code. If the TRIM() code has reached 000..00, the the calibration failed to find an appropriate TRIM code. If the TRIM() code has not reached the 000..0, the TRIM() code is decreased and goes back to wait period.



8. Flowchart of operation in the proposed calibration architecture.



9. The reference voltage circuit.

The comparator has relaxed requirements for speed (50 μs). The input offset voltage of the comparator should be as small as possible to minimize the comparison error between V_{CNT} and V_{MIN}. The required reference voltage (Figure 9) is obtained from the bandgap voltage available onchip.

TIMING ISSUE

One important consideration is the total PLL calibration time. For PLL calibration operation, there are two approaches: 1) calibrate at the power-up or during the reset time or 2) calibrate when changing channels. The time to change from one channel to the other is determined by the standard. There may not be enough time for auto calibration when changing channels depending on the calibration circuit and PLL architecture, therefore, auto calibration must be done at the power-up. The loop bandwidth and lock time of a PLL are inversely proportional. The loop bandwidth of a PLL is determined by the channel bandwidth for integer-N PLL architecture.

The first approach is employed here. The maximum total calibration time of the proposed architecture is equal to $2^N \times W_{time}$. N is the number of the control bits. W_{time} is the wait time (250 μs is used here), which depends on the worst-case PLL lock time and the comparator settling time. The maximum total calibration time is 2 ms (8 $\times$ 250 μs) in the worst-case, 4-GHz VCO case. The calibration time of the proposed architecture is intended to use power-up calibration, and it may not satisfy the lock time of many standards if the calibration is performed during channel change. The same architecture can be modified to reduce the wait time so that it can also be used during channel switching:

- Change the PLL loop bandwidth during calibration in order to

make PLL bandwidth large so that PLL will acquire lock quickly (the PLL lock time is inversely related to the PLL loop bandwidth).

- Use fractional-*N* PLL architecture to decouple the PLL loop bandwidth and channel spacing (the PLL bandwidth is determined by the channel spacing for integer-*N* PLL architecture).

MEASURED RESULTS AND CONCLUSIONS

The proposed tuning range calibration circuit is implemented in a WLAN frequency synthesizer [6]. Figure 10(a) shows simulated tuning curves for typical process corners for the 4-GHz VCO. Figure 10(b) shows measured 4-GHz VCO control voltage behavior during calibration. The die photo of VCO and PLL is shown in Figure 11.

ACKNOWLEDGMENT

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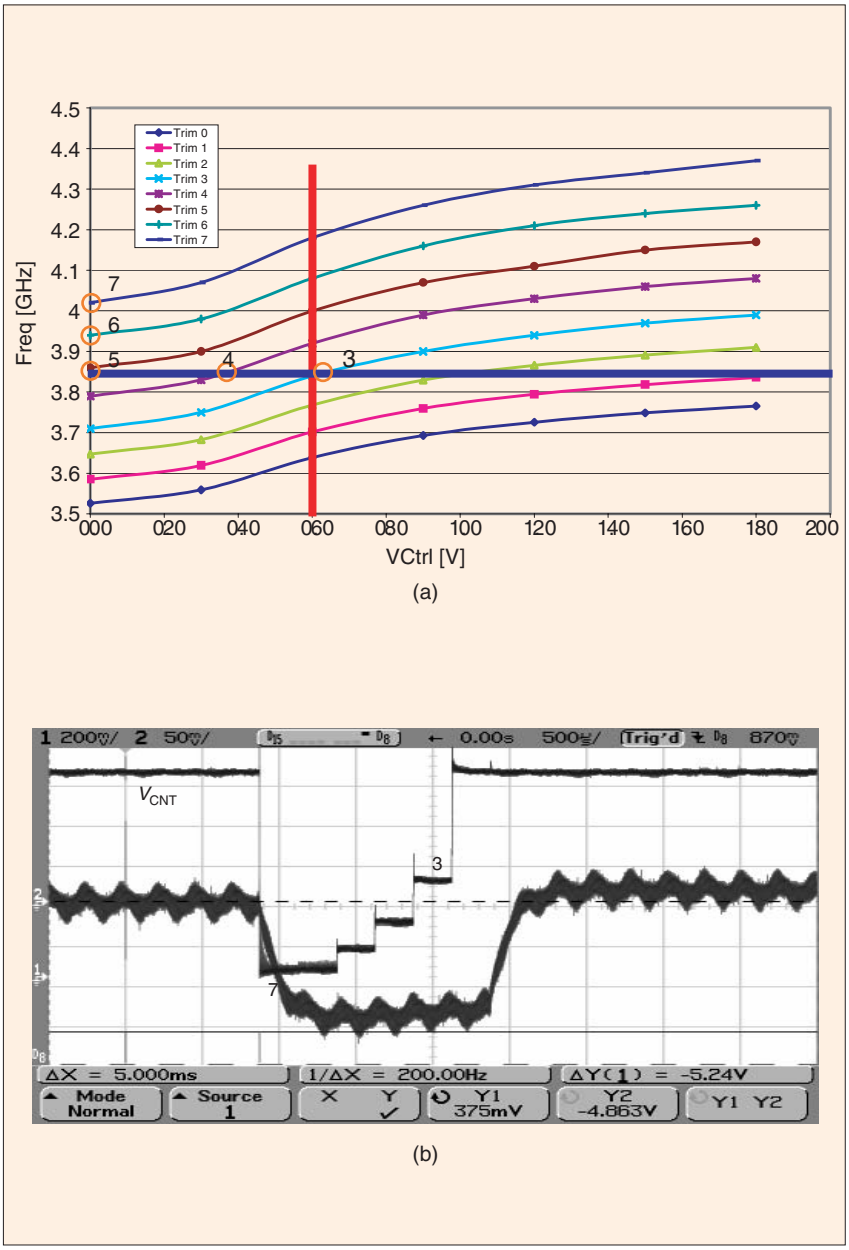
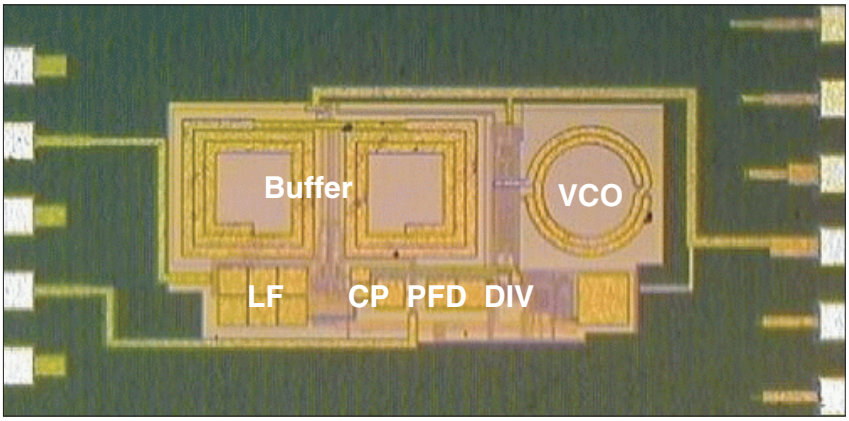


10. (a) VCO 4-GHz simulated tuning curves for typical process corners. (b) Measured VCO control voltage behavior.



11. Die photo of the test PLL.