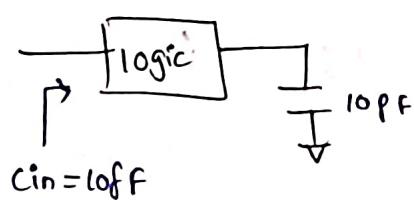


#



$$y = x$$

\* We want to design a buffer

↳ even no. of inverters in CASCADE

Can possible



We know  $\frac{K\tau}{C}$  is const  $\Rightarrow$  To reduce  $\tau$ , we need to ↑se K for const Cout.

$\Rightarrow T \propto \frac{C_{out}}{C_{in}} + \frac{C_{self}}{C_{in}}$  as we ↑ing K  $\Rightarrow$  ↑se  $C_{in}$  & ↑se  $C_{self}$ .

$\frac{L}{C} \uparrow se$ , I ↑se, charge timing's ↓se

→ keep on ↑ing  $\omega_L$ ,  $C_{self}$ .

as  $C_{eff} \gg C_{out}$  when  $\tau \approx \frac{C_{self}}{C_{in}} = \text{const}$

problem

→ prev stage loading

→

\* Waveforms in input become low

↳ makes output low.

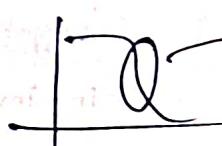
\* different modes  
show diff C values

→ approximate: We gate capacitance as  $WLcon$ ,  
(Good)

from  
output  
side

$$C_{gd} + C_{db}$$

We take  
overlap

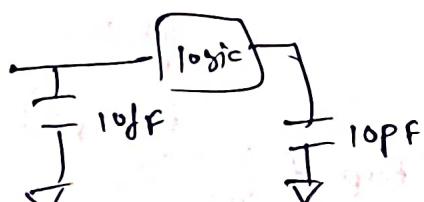


miller effect  
capacitance  
effective

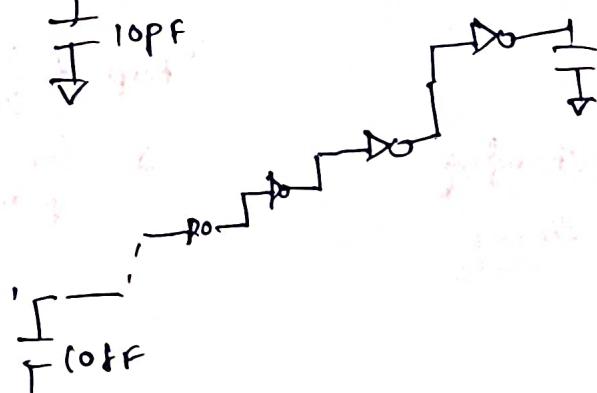
A presents

$C_{ox}$  can't see  
from drain side

miller  
effect  
only



→ How this problem to be solved?



drive cout with small  
delay by ↑ing ( $\omega_L$ )

we need another inverter  
to drive cin

- ① How to identify no. of stages? } To get min delay?  
 ② How to get stage?

Soln: Tapered Buffer chain.

$$n_{ops} = 2 \times n_{ops}$$

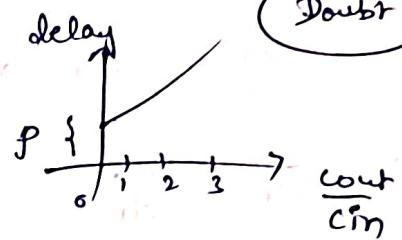
$$\downarrow \\ 2g \times T_{real}$$

$$\text{Delay} = g \frac{C_{out}}{C_{in}} + P$$

$$g = \frac{C_{eff}}{C_{in}} \quad (a)$$

$$P = g \frac{C_{eff}}{C_{in}}$$

Doubt



delay (ext)

$$\boxed{23 \text{ ps}}$$

$$= PR$$

$P=1$  driving nothing  
 $\therefore R_f = 23 \text{ ps. } k$

(load)

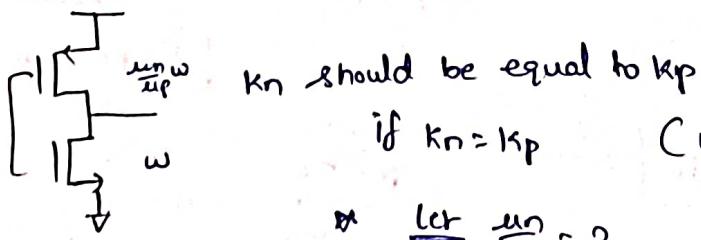
g:  $\rightarrow$  logical effort (LE)

$C_{out}/C_{in}$ :  $\rightarrow$  electric effort (h)

logical Effort: defined as input cap of that gate / input cap of inverter

When both can deliver same output current.

$$LE = \frac{C_{in-gate}}{C_{in-inverter}} \quad | \begin{array}{l} \text{if } k_n = k_p \\ \text{Delivers same op current.} \end{array}$$



$k_n$  should be equal to  $k_p$

if  $k_n = k_p$  (W-size inverter)

$$\star \quad \underline{\text{Let}} \quad \frac{w_n}{w_p} = 2$$

$$\therefore P \rightarrow 2w \quad N \rightarrow w$$

PUN  $\rightarrow$  on

cap  $\rightarrow$  charged up

when  $2w$  size transistor is on

showing us sum resistance of charging

$$\Rightarrow R_d \frac{1}{w(v_{gs}-V_T)} \quad \text{in linear mode}$$

$$\boxed{R_d \frac{1}{w}}$$

$$R_{up} \propto \frac{1}{2w}$$

sat, line

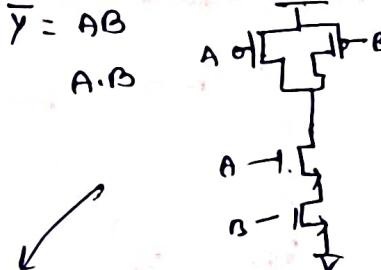
Assump'n

# for entire charging period

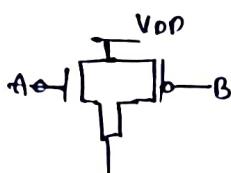
$$\overline{PDN}$$

$$R \propto \frac{1}{W}$$

$$Y = \bar{A}B + \bar{A}\bar{B}$$

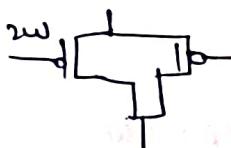


We should do equivalent to inverter



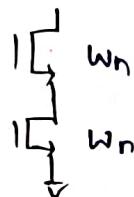
best case  $\rightarrow$  both on  
worst case  $\rightarrow$  one is on

with worst case delay  
high current  $\rightarrow$  fast changing



$2W$   $\rightarrow$  To match worst case delay of PUN & PDN with inverter's PUN & PDN

Why:



$\rightarrow$  we want to find  $W_n$

We will compare working times with PDN of networks

Works only  $\rightarrow$  (both are on)

$$R \propto \frac{1}{W} + R \propto \frac{1}{W}$$

$$R \propto \frac{2}{W_n}$$

Series in Nandgate

$$R \propto \frac{1}{W}$$

XOR

$$\frac{1}{W} = \frac{2}{W_n}$$

$$W_n = 2W$$

found  $W_n$

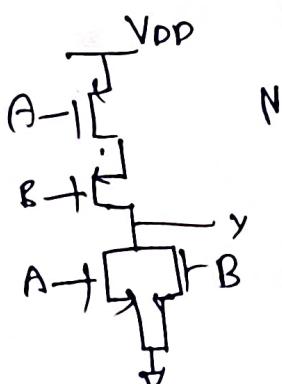
$$LF_A = \frac{\text{Cin-gate}}{\text{Cin-Inverter}}$$

$$= \frac{4W}{3W} = \frac{4}{3}$$

Input goes to 4 W's transistors

gate  $\left\{ \begin{array}{l} 2W + 2W \text{ (parallel)} \\ W + W \rightarrow \text{series} \end{array} \right.$

inver  $\left\{ \begin{array}{l} 2W \text{ parallel} \\ 2W \text{ series} \end{array} \right.$



NOR  
gate

$$W_P = 4W$$

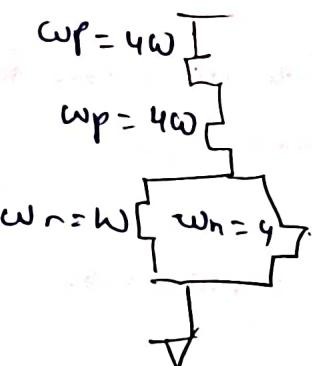
$$W_N = W$$

PDN  $\rightarrow$  worst case only one is on

best: both on  $\rightarrow$  discharge fast

$\rightarrow$  more current

$$W_N = W$$



PMOS: PUN  $\rightarrow$  conducts both on on

$$\frac{1}{w_p} + \frac{1}{w_p} = \frac{2}{w_p}$$

$$\frac{1}{2W}$$

$$\frac{1}{2W} \approx \frac{1}{w_p}$$

PMOS width in inverter  $\approx 2W$

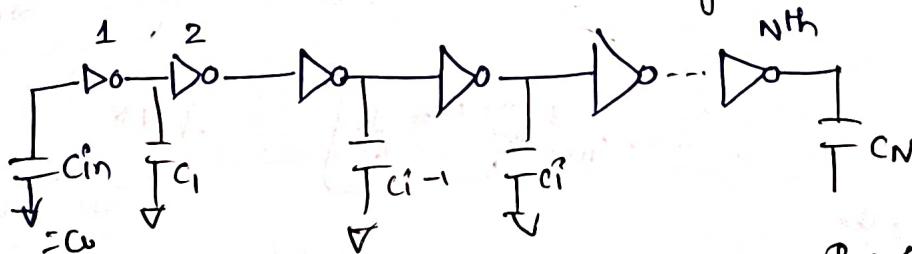
LE  
logical

$$\text{effort} = \frac{5}{3}$$

in Nor-gate

TAPERED BUFFER: (logic)

↳ How to design to get delay min?



$$\Rightarrow (\text{Delay})_{\text{overall}} = (h_1 + \rho) + (h_2 + \rho) + (h_3 + \rho) + \dots + (h_N + \rho)$$

$$(\text{Delay})_{\text{overall}} = D = \sum_{i=1}^N h_i + N\rho$$

$$= \sum_{i=1}^N \frac{c_i}{c_{i-1}} + N\rho$$

To minimize this,  
deriv wrt  $c_i$

$$\rho_1 = \rho_2 = \dots = \rho_N$$

$$\rho = p$$

$\Rightarrow$  same  
 $\Rightarrow 1$

$\rho = 1$  for inverter  
why? depth

$$\frac{\partial D}{\partial C_i} = 0 \quad \text{minimum}$$

$i \rightarrow$  specific ... ?? (doubt)

$$= \frac{\partial}{\partial C_i} \left[ \frac{C_i}{C_{i-1}} + \frac{C_{i+1}}{C_i} \right] = 0$$

$$\frac{C_i}{C_{i-1}} = \frac{C_{i+1}}{C_i}$$

$$\Leftrightarrow \frac{\text{Current stage}}{\text{C-present stage}} = \text{const}$$

$$h_1 = h_2 = \dots = h_n = h$$

$$H = \frac{C_{out}}{C_{in}} = h_1 \cdot h_2 \cdot h_3 \cdots h_n$$

$$\frac{C_1}{C_{in}} \times \frac{C_2}{C_1} \times \frac{C_3}{C_2} \cdots \frac{C_{out}}{C_{N-1}} = \frac{C_{out}}{C_{in}}$$

= product of each individual blocks

$$H = \prod_{i=1}^N h_i$$

overall

Electrical effort

$$\text{Delay} = \sum h_i + Np$$

summation

$$H = h^N$$

$$N = \frac{\ln H}{\ln h}$$

$$D = Nh + Np$$

$$= N(h+p) = N(h)^{1/N} + Np \quad \text{2 deriv wrt dN}$$

$$\frac{\partial D}{\partial N} = 0 = -1(H)^{1/N} + N \cdot \frac{1}{N}(h)^{1/N-1} + p$$

doubt

$$= (H)^{1/N} + (H)^{(1/N-1)} + p = H^{1/N} \left[ 1 - \frac{\ln H}{N} \right] + p$$

$$H^{1/N} \left[ 1 - \frac{\ln N}{N} \right] + p = 0$$

$$N = \ln H$$

$$N = \ln H \quad \checkmark \text{ let } p \text{ limits } p \rightarrow 0$$

for our  
CN

$$N = \ln \left( \frac{10PF}{10FF} \right)$$

$$D = Nh + Np$$

$$= (h+p) \frac{\ln h}{dh}$$

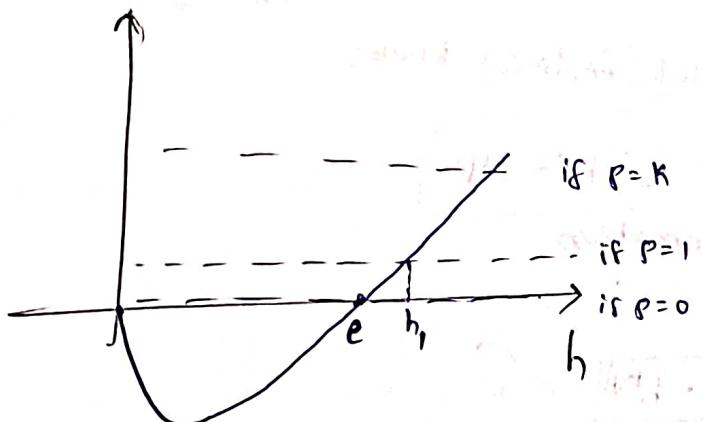
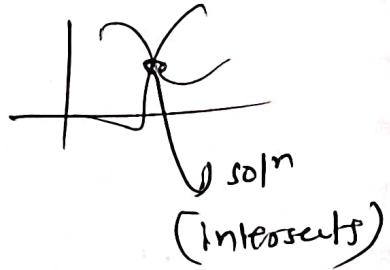
$$\frac{\partial D(h)}{\partial h} = 0 \rightarrow \frac{1}{\ln h} \left[ 1 - \frac{h+p}{h \ln h} \right]$$

$$h \ln h - (h+p) = 0 \Rightarrow h(\ln h - 1) - p = 0$$

~~h~~  $\Rightarrow h(\ln h - 1) = p$

$f_1(x)$        $f_2(x)$

draw  $f_1(x)$



wherever it intersects that the soln,

$h \rightarrow$  value

then we can know  
N value  $\cdot h$

\* Let  $p=1$  (Assume)  
(for inverter)

$P_{\text{Treal}} = P_{\text{red}}$

$P=1$  (for inverter)

$$h_1 = 3.59 \quad \text{for } p=1$$

# Let  $p=0 \Rightarrow h=e=2.73$   
(Assuming)

$p=1 \Rightarrow h=3.59 \approx 4$

Acc to Abhishek

$$3.59 \approx 4$$



$$N = \frac{\ln 10^3}{\ln 4} = 4.98$$

only even number  
4      6

\* Find delay for both cases

$$D = 4h + 4p$$

$$= 4(H)^{1/4} + 4p$$

$$= 4(10^3)^{1/4} + 4p$$

$$\approx 22.49 + 4p$$

$$(22.49 + 4p)_{\text{real}}$$

ref  $p=1$

$$N=4 \approx 26 T_{\text{real}}$$

$$N=6 = 25 T_{\text{real}}$$

$$H = \frac{C_{\text{out}}}{C_{\text{in}}} = 10^3$$

for  $N=6$

$$D = 6(H)^{1/6} + 6p$$

$$= 6 \cdot (10)^{3/8} + 6p$$

$$= 6\sqrt[3]{10} + 6p$$

$$= \underline{\underline{18.97 + 6p}}$$

~~for~~  $N=6 \rightarrow$  stage giving less delay.

How??

↳ implement

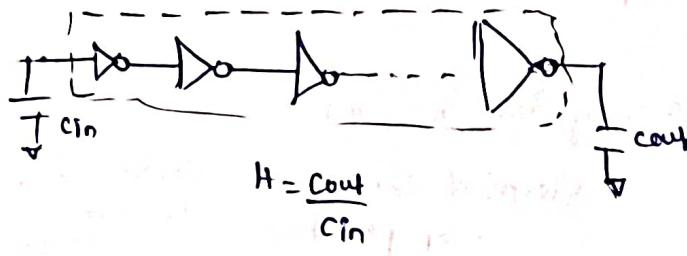
$\Rightarrow$  sizes are different

Always having less  $N$   
 $\frac{C_{\text{out}}}{C_{\text{in}}}$  are different for each

$\therefore$  getting good for  $N=6$ .

↳ book  
 → shiva

4-9-24



$$H = \frac{C_{\text{out}}}{C_{\text{in}}}$$

Tapped Inverter Chain for min delay.

$L_{\min}$



Hypothetical



$$\text{Delay} \propto \frac{C_{\text{out}}}{C_{\text{in}}} = \frac{C_{\text{self}}}{C_{\text{in}}} \cdot p_{\text{inv}}$$



$$D \propto \frac{C_{\text{out}}}{C_{\text{in}}} = \frac{C_{\text{in}} + C_{\text{self}}}{C_{\text{in}}}$$

This inverter driving

2 inverters.

~~2+P~~

$$D \propto 2+p$$

Min size inverter driving min size inverter

& consider  $C_{\text{parasitic}} = 0$

$$\therefore \beta = 0 \quad \frac{C_{\text{self}}}{C_{\text{in}}} = 0 \quad , \text{ then Here } d = \gamma$$

$$D = (gh + \beta) \tau$$

$\downarrow$   
 $g=1$  (for inverter)

$$\therefore D = (h + \beta) \tau$$

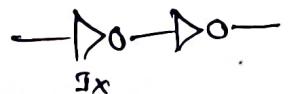
$\downarrow$  min size - driving  
min  $\tau$  &  
then  $h = 1$

& we considered  $C_{\text{self}} = 0$

$\beta = 0$

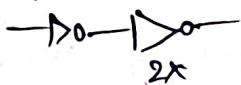
$$\therefore D = (1 + 0) \tau$$

$\therefore D = \tau$



$$D = (1 \cdot 1 + \beta) \tau$$

let driving 2 inverters,



$$D_2 = (1 \cdot 2 + \beta) \tau$$

$$= (2 + \beta) \tau$$

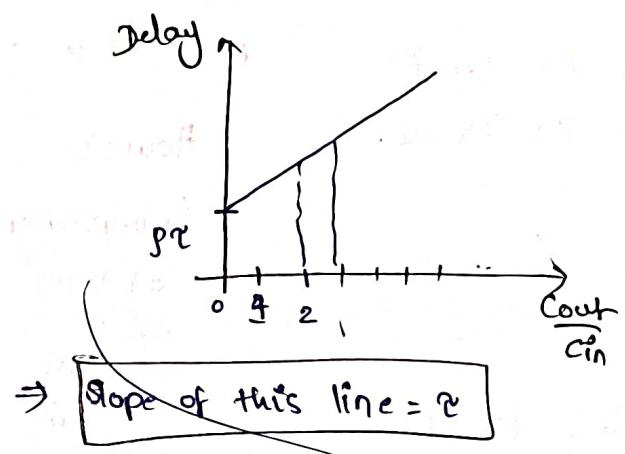
In simulation,

1 min-size inverter

measure delay

2 inv to get two points

We can get  $\beta$  &  $\gamma$  (slope)



They might deviate slightly

$$D = \sum_{i=1}^n \frac{c_i}{c_{i-1}} + \beta \tau \quad \rightarrow \frac{c_i}{c_{i-1}} = C_i H \quad \text{for every inv, } h = \text{const}$$

Electrical effort  $\rightarrow$  electric effort of prestage  $\times$  that stage

$$h_1 = \frac{c_1}{c_0} = h_2 = \frac{c_2}{c_1} \dots h_n = \frac{c_{\text{out}}}{c_{n-1}} = h$$

$$\therefore D = N \cdot h + N \cdot \beta$$

$$H = \frac{c_{\text{out}}}{c_{\text{in}}} = \frac{c_N}{c_0}$$

$$= h_1 \cdot h_2 \cdot h_3 \dots h_n$$

(product)

$$D = (h + \beta) \frac{\ln H}{\ln h}$$

$$D(x) = (x + \beta) \frac{\ln H}{\ln x}$$

$$D(h) = (h + \beta) \frac{\ln H}{\ln h}$$

$$N = \frac{\ln H}{\ln x} = \frac{\ln H}{\ln x}, \quad x = h$$

$$D'(x) = 0 \rightarrow \text{get minimum}$$

for min delay

$$D'(x) = 0$$

$$\therefore 1 = \frac{x+p}{x \ln x}$$

$$x - x \ln x + p = 0 \rightarrow \text{Let it is } f(x) \rightarrow \text{solve } f(x)$$

Newton Raphson:

Initial guess :

(let  $p=1$  (given))

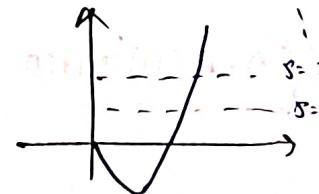
Assume

$$x_{\text{initial}} = 3$$

$$x_{\text{next}} = x_{\text{initial}} - \frac{f(x)}{f'(x)} \quad |_{x=x_{\text{initial}}}$$

$$\therefore x_{\text{next}} = x + \frac{x - x \ln x + p}{\ln x}$$

$$= \frac{x+p}{\ln x}$$



Newton Raphson

Here,

$$f(x) = 1 - x - \ln x \\ = -\ln x$$

$$x_{\text{next}} (\text{Here}) = \frac{3+1}{\ln 3} = \frac{4}{\ln 3}$$

Mfd  
exam

$$= 3.641$$

$$x_{\text{next}} = \frac{3.641 + 1}{\ln 3.641} = 3.59142$$

$$x_{\text{next}} = \frac{3.59142 + 1}{\ln(3.59142)} = 3.591$$

$$\text{Eg: } p = 0.6$$

$$x_{\text{next}} = \frac{x+p}{\ln x} = \frac{x+0.6}{\ln x} \quad x_{\text{in}} = 3$$

2-3 iteration

$$x_{\text{next}} = 3.2664$$

$$P=2 \rightarrow n_{\text{initial}} = 3$$

2-3-inverter

$$\lambda = 4.31937$$



$$Q: H = \frac{c_{\text{out}}}{c_{\text{in}}} = 10^3 \left( \frac{10^3}{10^3} \right) \rightarrow n = 3.59 \dots = h \\ \text{and also given } p=1 \\ \approx 4$$

$$D_4 = 4(10^3)^{\frac{1}{4}} + 4$$

$$D_6 = 6(10^3)^{\frac{1}{6}} + 6$$

$$D_4 \approx 26.5 \text{ ns}$$

$$D_6 \approx 25 \text{ ns}$$

$$D = N(H)^{\frac{1}{N}} + NP$$

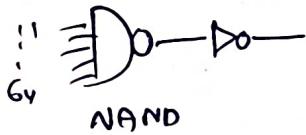
$$N = \frac{\ln H}{\ln n} = 4.98$$

$\approx 5$

$y = x$  we want,  
even no. of inverters  
we want  $\cdot h$   
4 stages      6 stages.

∴ For  $N=6$ , we are getting less delay //

64-input AND gate /

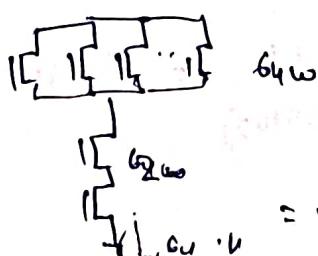
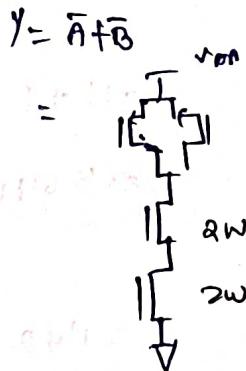


3 input NAND

$$y = \bar{A} + \bar{B} + \bar{C}$$



64 input



Parasitic cap  $\approx 192$

driving inverter

$$D = gh + P$$

gh: effort delay  $= 6 \text{ ns}$

$$\lambda = h \cdot g_{\text{in}} = h \cdot 1$$

↳ stage effort

Effort

delay

capacitance

current

power

area

frequency

temperature

noise

radiation

stress

etc

AND: uses

more

area

power

current

effort

delay

capacitance

frequency

temperature

noise

radiation

stress

etc

64 - input AND gate  
Can drive load  
 $C_{in} = \text{core values}$



case-2:

\* Method of Logical effort:

↳ Normalized delay

$\tau \rightarrow$  specific for technology, b

\* unit of time:

$\tau$ : min inverter driving min inverter without any parasitic element.

\* Dependence of technology over delay:

\* n dependence of size  $\Rightarrow h$

\* Dependence of logic time  $\Rightarrow g$

\*  $\rho \rightarrow$  parasitic delay [Independent of size]

Eg:

$$LE = \frac{C_{in\text{-gate}}}{C_{in\text{-inv}}}$$

(providing same have same current capability)

$$\text{Let } \frac{w_n}{w_p} = 2$$

2 i/p NAND

$$LE = 4/3$$

2 i/p NOR

$$LE = 5/3$$

N i/p NAND

$$= \frac{(N+2)w}{3w} = \frac{N+2}{3}$$

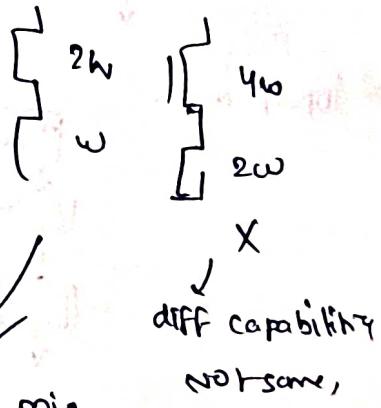


N - input NOR gate:

w - from PDN

$q_N$

For Absolute value of delay, we need to find by multiplying with  $\tau$



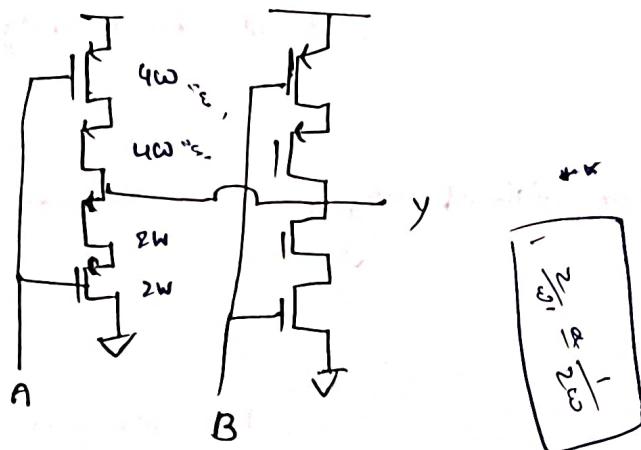
take min

2 i/p NOR  $\rightarrow$

2 i/p NOR:



$$N\text{-i/p NOR} = \frac{W + 2NW}{3W} = \frac{2N+1}{3}$$

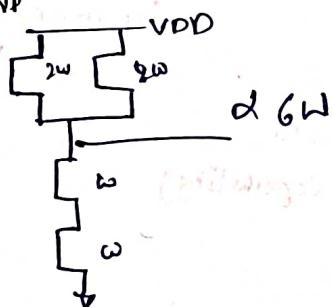


$$LE = \frac{4+2}{3} = 2$$

N-input MUX

$$LE = 2$$

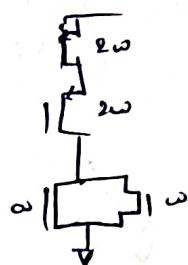
2-i/p NAND



$$P_{NAND} = \frac{6W}{3} = 2P_{INV}$$



2-i/p NOR:



$$P_{NOR} = \frac{6W}{3} = 2P_{INV}$$

N-input-NAND:

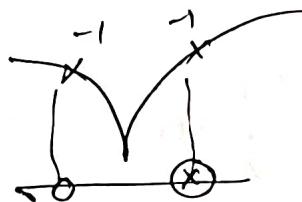
$$P_{UN - 2NW} = \frac{2NW + NW}{3} = N P_{INV}$$

$$P_{DN} = NW$$

Gate Exam  
LE, P  
min delay

6-9-24 (Tut)

DC analysis



11-9-24

② → simulation

↳ find  $\mu_n, \mu_p$

③ → 'W' size inverter     $W_n = W = 1.8 \mu m$   
                                 $W_p = 2.5 \times W$

Netlist → subcircuit  
2 times. II

(u)

Param  $k_n = 4$

$k_2 = 1.5$

$k_3 = 1$

$N_p = K_p$

DC simulation → plot  $V_{DD}$   
 $d\left(\frac{V_{DD}}{V_{in}}\right) = (-1)$  slope     $x$  coordinates,  $y$  coordinates,  
↓  
NMN, NMH

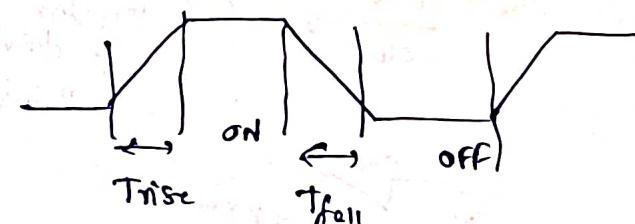
→ DO

$t_r \ t_f$   
 $t_{PLH} \ t_{PHL}$   
 $0 \rightarrow 1 \rightarrow 0$

if  $t_r = t_f$

\* might happen both are not equal

$$t_{PD} = \frac{T_{PLH} + T_{PHL}}{2}$$



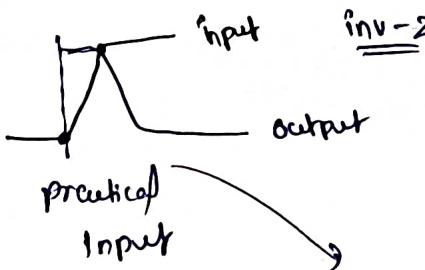
→ DO

practical input

practical output.

→ Similar to ideal input

if  $t_r \ t_f \ll$



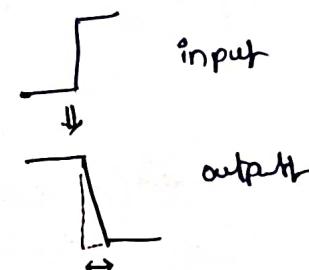
Take 50% transition

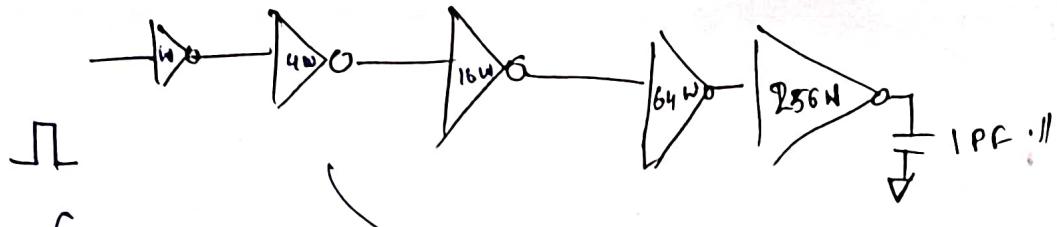
for delay 1/1

what is delay  
of inverter

Take  $t_r, t_f$

and take avg  $\Rightarrow$  delay of inverter 1/1



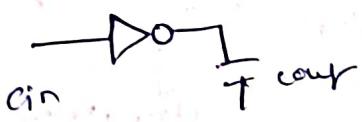


→ can choose  
very low  
tr, tf waveform  
& get that waveform

input for this inverter  
also coming from digital circuit

∴ We can characterize well. 😊

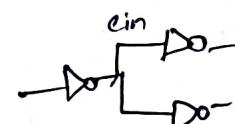
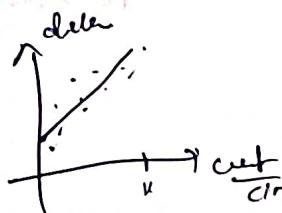
⑤



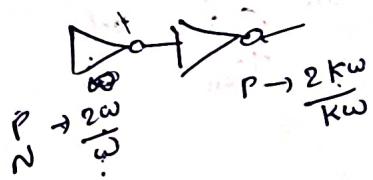
$$\frac{C_{load}}{C_{in}} = 2$$

inverter  
is driving

2 inverters of its size. //



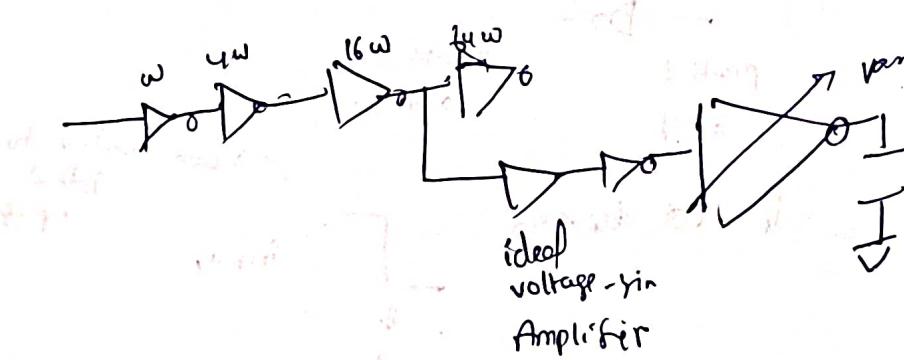
$$\frac{2C_{in}}{C_{in}} = 2$$



-D → D

$$cout = 1$$

$$cout_{in} = 2$$



positive feedback

negative feedback

no feedback

positive feedback & negative feedback

$$\overline{I}_{NM} = \text{Tolerance}$$

$g=1 \rightarrow$  Inverter (chain)

Chain  $\Rightarrow$

not only Inverters

Mux's, gates, e.t.c. //

$\Rightarrow$  2 input AND gate  
by 2 stages

delay of entire chain

In terms of each stage //

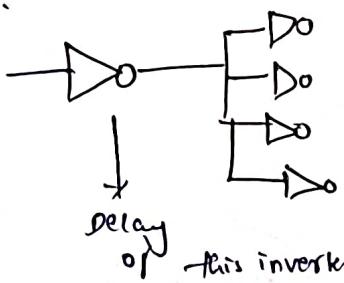
Can minimize delay by maintaining

$$\frac{C_L}{C_{in}}$$



$$D = (gh + p) T$$

Q:



Delay of this inverter

$$P_{inv} = 1$$

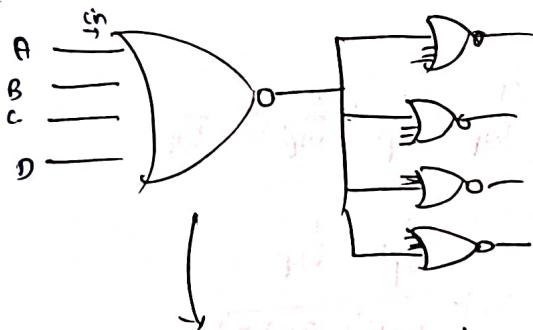
$$D = (gh + p) T$$

$$(1 \cdot 4 + 1)$$

= 5 Delay units //

$$h = \frac{4 C_{in}}{C_L} = 4$$

Q:



Delay of this  
NOR gate

\*\*\*

Delay

It is wrt to one-point / input

if we have 10 such gates //

then ~~2 kates~~  
 $h = 10$

then  $3 \cdot 10 + 4$

$$= 34 T //$$

each input  
can be cin

$$g_{NOR_4} \cdot h + g_{NOR_4}$$

$$\left(2N + \frac{1}{3}\right) \cdot 4 + 4$$

$$g_{NOR_4} = N P_{inv}$$

$$g_{NOR_4} = 2N + \frac{1}{3} = 3$$

$$f = \overline{A(B+C) + DE}$$

$f_A = ?$  Are both equal...??

$$f' = A(B+C) + DE$$

$$f_B = ?$$

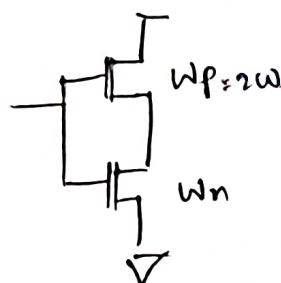
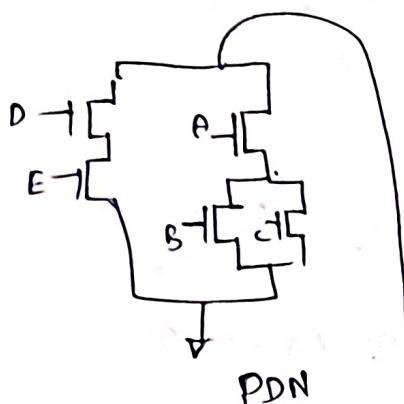
$$f = \overline{A(B+C) + DC}$$

$$= \overline{A(B+C)} \cdot \overline{DE}$$

$$= \overline{A(B+C)} \cdot (\overline{D} + \overline{E})$$

$$\overline{A} + (\overline{B} + \overline{C})$$

$$y = (\overline{A} + (\overline{B} \cdot \overline{C})) \cdot (\overline{D} + \overline{E})$$



worst case

$D, B, C$  also corr form

$$\therefore D \approx w = 3w_p$$

$B, C$  and  $A$  are in parallel

$$\frac{1}{3w_p} + \frac{1}{3w_p} = \frac{1}{w_{PA}}$$

$$\frac{2}{3w_p} \parallel \frac{1}{w_{PA}}$$

$$\therefore w'_{PA} = \frac{3w_p}{2} = \frac{3w}{2} = 3w \cdot 6$$

$$\frac{1}{w_p} + \frac{1}{w_p} + \frac{1}{w_p} \approx \frac{1}{w_p}$$

$$\frac{3}{w_p} = \frac{1}{w_p}$$

$$w'_{PA} = 3w_p = 6w = 3w \cdot 6$$

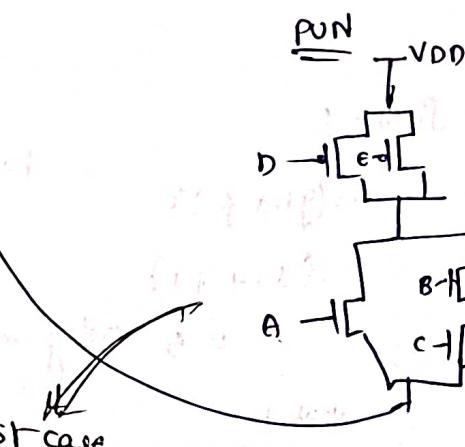
$$\therefore w'_{PA} = \frac{3w_p}{2} = \frac{3w}{2} = 3w \cdot 6$$

~~w' = w~~

$$\frac{1}{w_n} + \frac{1}{w_n} = \frac{1}{w}$$

$$\frac{2}{w_n} = \frac{1}{w}$$

$$\therefore w_n = 2w$$



$$\frac{w_n}{w_p} = 2$$

PDN:

$$2w_n = w_n$$

$$w_n = \frac{w_n}{2} = w/2$$

~~w' = w~~

$$\frac{1}{w_n} + \frac{1}{w_n} = \frac{1}{w}$$

$$\frac{2}{w_n} = \frac{1}{w}$$

$$\therefore w_n = 2w$$

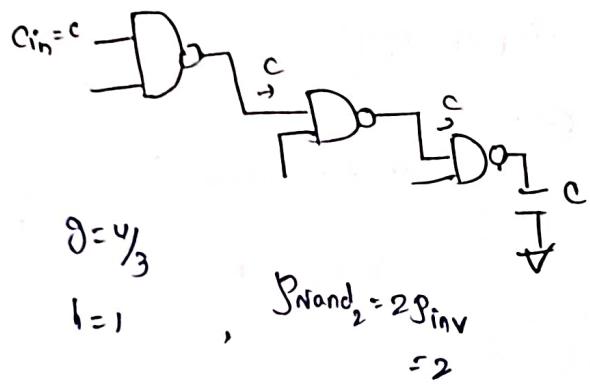
$$g_A = 2\omega + \frac{3\omega p}{\frac{3\omega}{2}} \Rightarrow 3 \frac{54}{4} = 51 \checkmark \quad g_B = 8/3 - g_C = g_E = g_D$$

$\frac{3\omega}{3\omega}$

$\nwarrow$  If inverter  
Input is A' h

$A \rightarrow \text{output}$   $\nearrow$  doesn't give worst case delay.

$\alpha:$



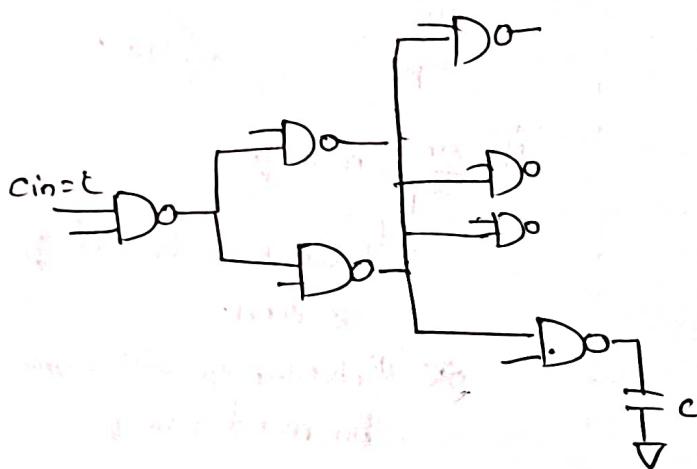
$$\theta = \psi_3$$

$$l=1 \quad , \quad g_{\text{rand}} = 2g_{\text{inv}} = 2$$

Overall delay = ?? (in  $\tau$  units)

g, h, g

$$\left[ \frac{4x}{3} + 1 + 2 \right] \times 3 = 4 + 6 = 10 \text{ units}$$

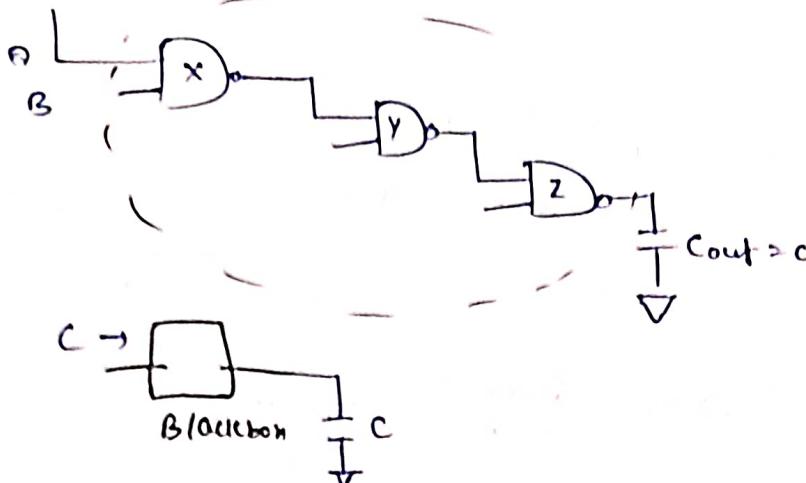


$$\rightarrow g_{bh} + p \cdot 11$$

$b = 2$   
Branching effort,

14-9-24

Eg:  $C_{in} = C$



① path Logical effort

② (from A → output) Ex:

∴ Path logical effort (G):

$$G = \prod g_i$$

Here in example,

for nand gates,  $g_i = \frac{4}{3}$   $\forall i$

$$\therefore G = \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} = \left(\frac{4}{3}\right)^3$$

considering  $\frac{m}{n_p} = 2$

$$\frac{m}{n_p} = 2$$

(mid)

$$\text{if } \frac{m}{n_p} = m \cdot \frac{1}{p}$$

we have to find  $g_i$  first.

\* different  $g_i$  will come for nand gate.

MUX design, NOR, NAND, Inverter.

H:  $\frac{C_{out}}{C_{in}}$  = electrical effort (overall)  
↳ EE of blackbox.

\* B: Branching effort

Branching effort (B):  $= \frac{\text{Con-path} + \text{Coff-path}}{\text{Con-path}}$

Now, we will see

Branching effort of X gate.

Here, Coff-path  $\rightarrow$  FAN-OUT effects



we want min from A to output  
but we have branch.

Coff path will be =  $c_1 + c_2$

$$A^{\text{Coff-path}} = c_1 + c_2$$

Now in our example

$$\text{Coff-path} = 0$$

$$\because B_X = 1 \therefore \frac{\text{Con-path}}{\text{Con-path}}$$

$$\therefore B = \prod b_i$$

Branching effort.

$$\text{We know, } F = GBH$$

$$Q = \prod g_i$$

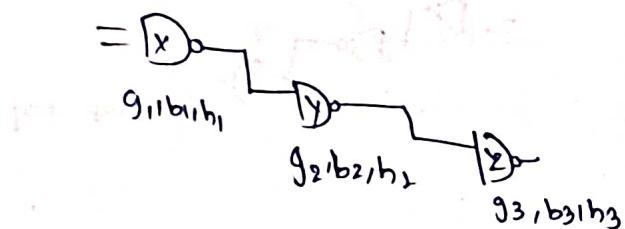
$$B = \prod b_i$$

$$H = \prod h_i$$

if there are N-stages:

(like Inv design)

our concern Inv:



For min delay,

Stage efforts of all stages are equal

Delay of N-stage logic

$$D = N(\hat{f}) + p \quad \text{each stage delay}$$

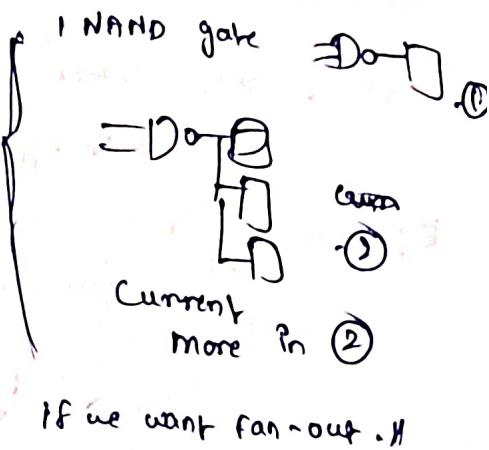
$$= N(F)^{1/N} + p$$

$$(bgh)_i = \hat{f} = (F)^{1/N} \rightarrow \text{for min delay, if}$$

let that i-th stage,  $b_i = 1$

↳ can I find  $g_i \Rightarrow$  (from there) tech

$$\text{can find } h_i \Rightarrow \frac{f^1}{\dots^L}$$



Stage effort =  $g_i b_i h_i$   
(j)

$$\hat{f} = (F)^{1/N}$$

if all are equal //

$$(bgh)_i = (bgh)_{i+1}$$

for min delay //

→ prove this. ?? (j)

$$\therefore h_i^o = \frac{g}{\sum j_i b_i^o}$$

from Henry, we know  $\eta = \frac{c_{out}}{c_{in}}$   
 (i.e. from here)

→ our desired  
(already known)

& we found each stage

Therefore, we can built our circuit.

→ Method to design multistage logic with min delay.

equilibrium stage effort ( $\hat{g}$ ) =  $r y_N$

Path effort  $r = \text{GBIA}$

$\hat{y} \rightarrow$  value we want

from topology we can get  $g_i$ 's.

If this found  $\rightarrow$  we can built circuit

$$\underline{\underline{Eg}}: N=3, F=GBII$$

$$G = \left(\frac{4}{3}\right)^3 \oplus, \quad B = 1 \quad , \quad H = \frac{\text{count}}{C_{\text{IP}}} = 1$$

$$\therefore \hat{f} = 9 \left( \left(\frac{4}{3}\right)^5\right)^{\frac{1}{10}} = \frac{4}{3}$$

$$\therefore f = k_3$$

A circuit diagram showing three parallel plate capacitors connected in parallel. The left capacitor has a fixed top plate and a variable bottom plate labeled 'D'. The middle capacitor has a fixed top plate and a variable bottom plate labeled 'D'. The right capacitor has a fixed top plate and a variable bottom plate labeled 'D'. The common connection between the three capacitors is labeled 'out = cap'.

$$(gbh)_z = \hat{g}$$

$$\frac{y_0}{4\beta} = 1$$

$$h = 1$$

$$bz = 1$$

$$g z = \frac{4}{3} \quad (\text{if } \frac{u_1}{u_0} = 2)$$

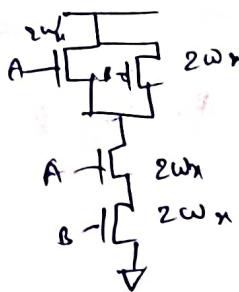
$$h_2 =$$

$$b(gbh)_y = j = \frac{1}{\sqrt{3}} \Rightarrow hy = \frac{1}{\sqrt{3}} \cdot \frac{1}{\sqrt{3}} = 1$$

$$\boxed{\therefore hy = 1} = \frac{(cout)y}{(cin)y} = \frac{1 \cdot \frac{(cin)z}{(cpn)}y}{y} = 1$$

$$\therefore \langle c_{in} \rangle_Z = \langle c_{in} \rangle_{\bar{Z}} = \Theta(c)$$

∴ all are same size.



$$(C_{in})_{\text{for 2 input}} \propto 4w_n$$

NAND

$$Y = \bar{A}\bar{B}$$

$$Y = \bar{A} + \bar{B}$$

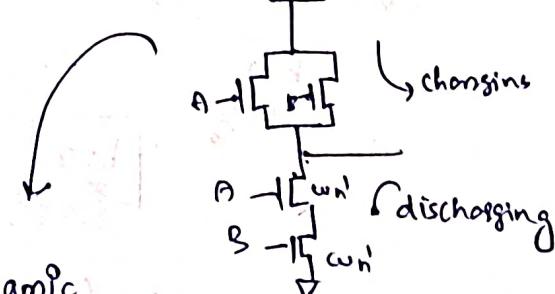
$$\bar{Y} = AB - Y$$

PDN, //

PUN



$$\frac{w_n}{w_p} = m \quad \text{if } m=2 \\ m w_n = w_p = 2w_n //$$



Dynamic performance:

(matching inv. in transient) doubt.

assump<sup>n</sup>:

acting like resistors

(linear)

$$R \propto \frac{1}{w}$$

Worst case:

PDN:

both on

$$\frac{1}{w_n} + \frac{1}{w_n'} \propto \frac{1}{w_n}$$

$$\frac{2}{w_n} = \frac{1}{w_n} \Rightarrow w_n' = 2w_n \text{ ***}$$

PUN:

only one is on → worst case

$$\frac{1}{w_p} \propto \frac{1}{m w_n} \Rightarrow \boxed{w_p' = m w_p} //$$

2

(LE)

$$(S) \text{ one input (or } A \Rightarrow) = \frac{C_{in}-\text{gate}}{C_{in}-\text{inv}} \Rightarrow \frac{(m+2)w_n}{(m+1)w_n} = \frac{m+2}{m+1}$$

If  $m=2$

$$y = \frac{2+2}{2+1} = \frac{4}{3}, b$$

$$Q9: C_{out} = 8C$$

$$H = 8 \cdot 1/1$$

$$\oplus F = G_B H$$

$$= (4/3)^3 \times 8 = (8/3)^3$$

$$F = (8/3)^3$$

$$J = (F)^{1/3} = (F)^{1/N} = 8/3$$

$$\therefore g_i = 4/3$$

$$(gbh) \frac{a}{2} = 8/3 \quad b=1$$

$$\begin{matrix} b=1 \\ g=4/3 \end{matrix}$$

$$\therefore h = 2$$

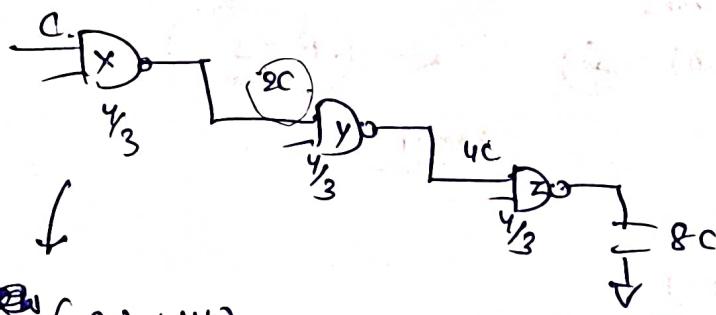
$$(gbh)_y = 8/3$$

$$hy = 8/2$$

$$\therefore (c_{in})_z = (c_{out})_y \cdot 4$$

$$(c_{in})_z = 80/2 = 4C$$

$$\frac{c}{c_{in} z} = 2$$



$$(c_{in})_n \propto 4\omega_n = C$$

$$(c_{in})_y = 2C \propto 8\omega_n$$

$$4\omega_y = 8\omega_n$$

$$\therefore \omega_y = 2\omega_n$$

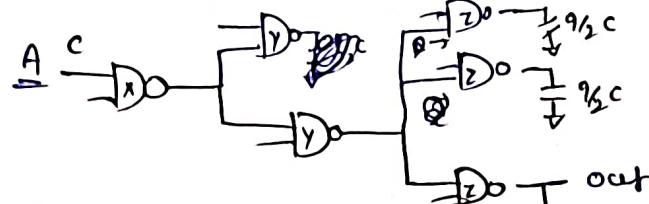
$$2\omega_y = 4\omega_n$$

$$2\omega_y = 4\omega_n$$

$$2\omega_y = 4\omega_n \cdot 4$$

④ samuris. oal hoit kare  
 \* verilog . I·B has bagh  
 Verilog 4

Eg:



$$N = 3$$

3 NAND gates

Design path-delay from

A-output is minimized

$$\Leftrightarrow F = GBH$$

$$G = \left(\frac{1}{3}\right)^3$$

G: Independent of nodes, 4

$$H = \frac{9}{2} = 4.5$$

$$B = \prod b_i$$

$$= b_1 \cdot b_2 \cdot b_3 = 1$$

$$b_x \cdot b_y \cdot b_z^{\cancel{1}} = b_x \cdot b_y$$

$\rightarrow$  non FAN out

$$\therefore b_z = 1$$

$$b_y = \text{Con}_y = c_{in}(z)$$

$$\text{coff}_y = 2 c_{in}(z)$$

$$= \frac{\text{con}_x + \text{coff}_z}{\text{con}_z} = \frac{3 c_{in} z}{(c_{in}) z} = 3 \cdot 1$$

$$\therefore b_y = 3$$

$$b_n = \text{con}_n = (c_{in})_y$$

$$\text{coff}_n = (c_{in})_y$$

$$2 c_{in} y = 2 \quad \therefore b_n = 2$$

$$\therefore B = 2 \times 3 \times 1 = 6$$

$$\therefore B = 6$$

$$F = GBH$$

$$= \frac{\frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} \times 2 \times 3 \times 9}{2} = 4 \times 4 \times 4 = 64$$

$$\therefore F = 64$$

$$f = (64)^{1/3} = 4 \quad \therefore f = 4$$

$$(gbh)_z = f$$

$$h_z = \frac{4}{\frac{4}{3}} = 3 \quad \boxed{h_z = 3}$$

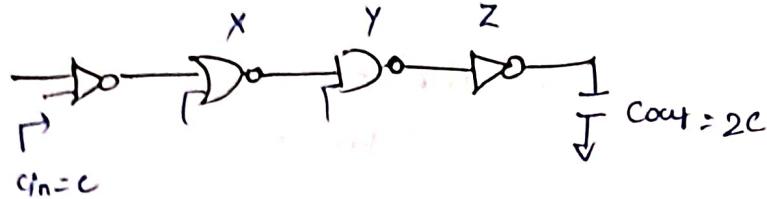
$$(gbh)_y = f$$

$$h_y = \frac{1}{\frac{1}{3} \cdot 2} = \frac{1}{\frac{2}{3} \times 2} = 1 \quad \therefore h_y = 1$$

$$(gbh)_n = f$$

$$h_n = \frac{1}{2} = \frac{1}{2} \quad \boxed{h_n = \frac{1}{2}}$$

Eg:



$$N = 4$$

$$F = GBH$$

$$G = 1 \times \frac{5}{3} \times \frac{4}{3} \times 1 = \frac{20}{9} = 2.22$$

$$B = 1 \times 1 \times 1 \times 1 = 1$$

$$H = \frac{2c}{c} = 2$$

$$\therefore F = \frac{40}{9}$$

$$\hat{f} = \left(\frac{40}{9}\right)^{1/N} = 1.45$$

$$(gbh)_x = \hat{f} = 1.45$$

$$\hat{f} = (F)^{1/N}$$

↳ prof 1/4  
MID

$$h_2 = \frac{1.45}{1 \times 1} = 1.45 \quad \text{∴ } h_2 = 1.45$$

$$f_{in}(z) = \frac{2c}{(c_{in})_2} = 1.45$$

Size of z

$$3w \alpha (c_{in})_2 = 3w \alpha c$$
$$= 1.4c$$

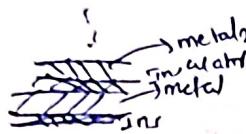
$$(c_{in})_2 = \frac{2c}{1.45} = 1.4c$$

$$\begin{aligned} \therefore \quad & 2\omega_2 = 2\omega x + 4 \\ & \omega_2 = \omega x + 2 \end{aligned}$$

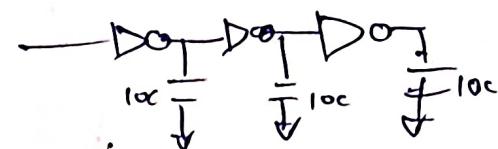
Final (CE19)



we can use 6 metals //



via contact  $M_2$   $D_x$



$$D_y = h + p$$

$$= \frac{100 + Z}{xy} + \cancel{\frac{h}{y}}$$

$$D = \frac{100 + y}{10} + \frac{100 + Z}{xy} + \frac{100}{Z} + 5p$$

why no  $y + 10c$ ?

mid  
enam

if we have  $y + 10c$

$$\frac{Z}{y} = t$$

$$10 + \frac{y}{10} + \frac{100}{y} + t + \frac{100}{yt}$$

$$\frac{\partial D}{\partial y} = 0$$

find  $y$  & min of  $t$ . //

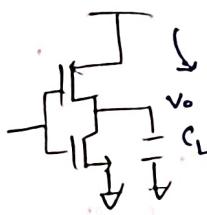
substitute  $y(t)$  in delay funcn in terms of  $t$

$$\frac{\partial D}{\partial t} = 0$$

find value of  $t$  //

18-9-24

Recap: MLE



$$I = c_L \frac{dV_o}{dt} \Rightarrow \int dt = c_L \int \frac{dV_o}{I}$$

(saturation + linear) current

$$\text{Q} = CV = IT \Rightarrow t = \frac{CV}{I} \quad (\therefore t \propto C)$$

$$\therefore \int dt = c_L \left[ \int \frac{dV_o}{I_{sat}} + \int \frac{dV_o}{I_{lin}} \right]$$

Note:

$$C_L = C_{ext} + C_{par}$$

$$T = c_L [\text{const} + \ln(1)]$$

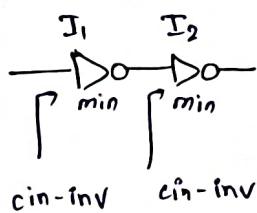
equivalent Resistance  $R_{inv}$

~ similar to  $R_{C_L}$



$$T \propto \frac{C_L}{K} = \frac{C_L}{\mu p \text{const} \frac{W}{L}}$$

$$T = C R_{inv} = C_L \frac{\alpha}{K}$$

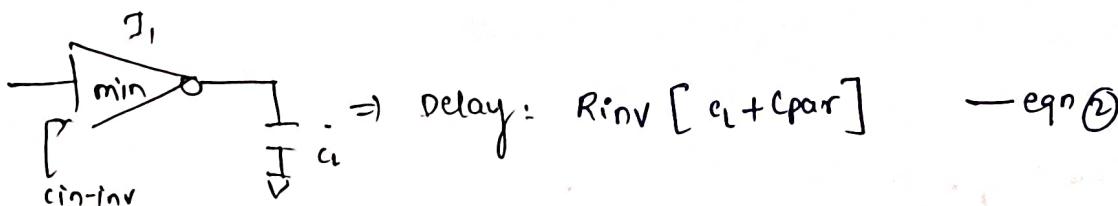


(min size inv drawing min-size  $P_{inv}$ )

Let  $C_{parasitic}$  of Inv = 0 (Hypo)

Then, Delay =  $R_{inv} \cdot C_{ext}$

$$= R_{inv} \cdot C_{in-cininv} = \tau \quad \text{--- eqn ①}$$



⇒ Delay:  $R_{inv} [c_L + C_{par}] \quad \text{--- eqn ②}$

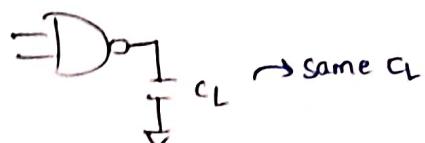
$$\frac{\text{eqn ②}}{\text{eqn ①}}$$

$$\frac{D}{\tau} : \frac{\alpha \cdot c_L}{C_{in-inv}} + \frac{C_{par}}{C_{in-inv}} \xrightarrow{C_{in-inv} \sim \omega} \frac{\alpha \omega}{\beta}$$

$\therefore \beta = \text{const}$

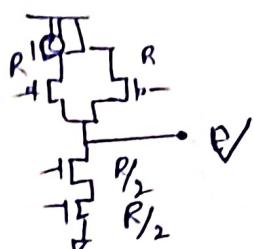
$$\therefore D = [n + p] \tau_{inv} \quad \text{Absolute delay of inverter}$$

↑ used to capture Absolute delay.



Let const current flowing (assuming)

$$t = \frac{CV}{I}$$



worst case Analysis

equating currents

∴ equating resistances

for same current carrying capability

Cpar-Nand  $\propto 6W$

at note "W"

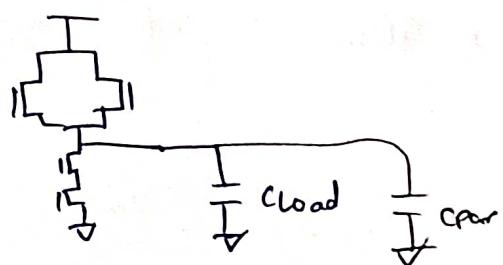
∴ time should be less than inverter

$$D_{\text{logic}} = R_{\text{logic}} [C_{\text{load}} + C_{\text{par}}] \quad \text{--- (3)}$$

$$R = R_{\text{inv}} \cdot C_{\text{in-inv}} \quad \text{--- (1) (from ?)}$$

$$\frac{\text{eqn } (3)}{\text{eqn } (1)} \Rightarrow$$

$$\frac{D_{\text{logic}}}{2} = \frac{R_{\text{logic}}}{R_{\text{in}}} \left[ \frac{C_L}{C_{\text{in-inv}}} + \frac{C_{\text{par}}}{C_{\text{in-inv}}} \right]$$



We are making  $R_{\text{in}}$  resistance equivalent to logic gate resistance

by making different sizes

$R \propto \frac{1}{W} \rightarrow \text{Scaling change}$

$\therefore \frac{R_{\text{logic}}}{R_{\text{in}}} = 1$

$$\begin{aligned}
 \frac{D_{\text{logic}}}{t} &= \frac{\text{cin-logic}}{\text{cin-inv}} \otimes \frac{c_L}{\text{cin-logic}} + P_{\text{logic}} \\
 &= \frac{\text{cin-logic}}{\text{cin-inv}} \times \frac{c_L}{\text{cin-logic}} + P_{\text{logic}} \\
 &\quad \swarrow \quad \curvearrowright \\
 g & \quad h \\
 &= gh + P_{\text{logic}}
 \end{aligned}$$

$\therefore D_{\text{logic}} = [gh + P_{\text{logic}}] t$

Mid Exam

- ① logic given - NAND, NOR, 2, 3, 4, 5, X inp

$t$  - given . find Delay  
 optimise this logic to min delay

- ② Sizing of gates

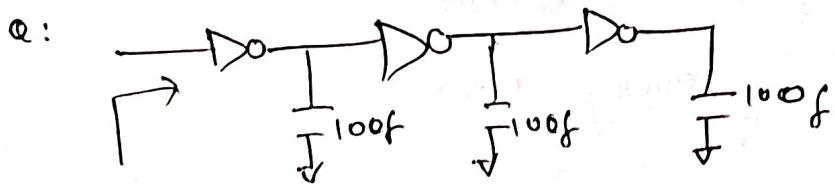
$$F = GBH \quad \text{find } f \rightarrow \text{no. ofhet}$$

$$f = \sum f_i = (F)^{1/N}$$

output side Starr  $\rightarrow$  & size each gate.

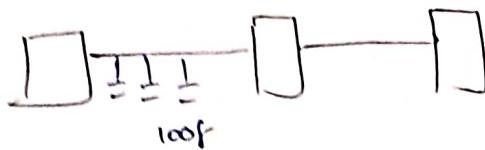
- ③ Few que's related to Assignment

2 pages - A4 (Allowed)

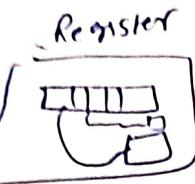


$$\text{cin} = 10f$$

Magiz

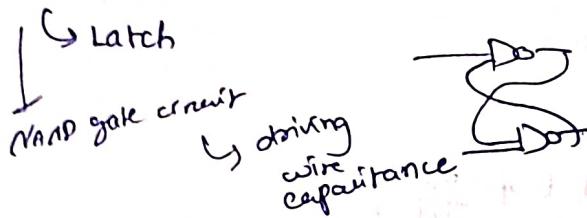


Shift register



long range in travel in chip  
(10-100 micrometers)

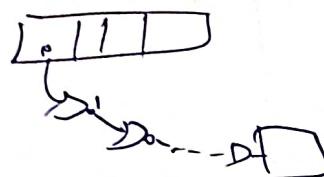
D-flip flop



Shift register  
to drive Inverted

& say  
loop

Buffers  
Inversion



↳ if we want electrical efforts.

We will estimate parasitic  
capacitance  
after post layout

10f -  
50f -  
100f -  
↳ half of area → buffers etc.  
to get our requirements

↓ if doesn't need our requirements  
then we will make buffers. //

$$F = GBH$$

$$G_i = \pi g_i$$

$$B = \pi b_i = \frac{\text{compath} + \text{off path}}{\text{cm-path}}$$

$$H = \pi h_i^2 = \frac{\text{comf}}{\text{cm}}$$



AK =  
Delay  $\min \Rightarrow$  each stage / stage effort is same

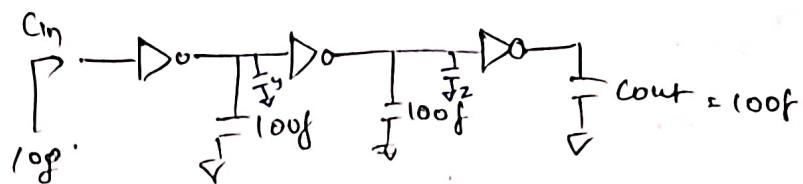
$$f = (r2)^{1/N}$$

$$f_i = (gbb)_1$$

(A)  $D = h + p_{inv}$

$$D = D_1 + D_2 + D_3$$

$$= (h_x + h_y + h_z) + 3p_{inv}$$



$p_{inv} \rightarrow$  indep of size

↳ depends on structure  
layout

$$D = \frac{100+y}{10} + \underbrace{\frac{100+z}{y}}_{\text{minimize this}} + \frac{100}{z} + 3p_{inv}$$

↳ already const  $\parallel \Theta$

$$\frac{z}{y} = t$$

$$D = \left( 10 + \frac{y}{10} + \frac{100}{y} + t + \frac{100}{yt} \right)$$

$$\frac{\partial D}{\partial y} = 0 + \frac{1}{10} + \left( -\frac{100}{y^2} \right) + 0 + \left( -\frac{100}{ty^2} \right)$$

$$D = 10 + \frac{y}{10} + \frac{100 + \frac{100}{t}}{y} + t$$

$$t = 1.6 \parallel$$

$$\frac{\partial D}{\partial y} = 0$$

$$y = 31.7 \sqrt{1 + \frac{1}{t}} \quad \text{--- (5)}$$

$$y = 40$$

$$z = 64$$

~~$$D_{min}(t) = 10 + t + 2\sqrt{10 + \frac{10}{t}}$$~~

$$\frac{\partial D_{min}}{\partial t} = 0$$

$$\downarrow \\ t = 1.6$$

Substitute in eqn (5)

$$y \approx 40 \Rightarrow z = 64 \parallel$$

$$h_x \approx 14 \quad h_y = \frac{100+z}{y} \quad h_z = \frac{100}{z}$$

$$= \frac{100+40}{40}$$

Stage efforts come are NOT equal

Now

Modify probm s.t stage effort of each stage are equal //

$$\beta_x = f^y + f^z \\ 14 \quad 4 \quad 16$$

Hint:

Can add More  
inverters. //



$$F = GBH = 2^N$$

If  $N =$  this (certain no)

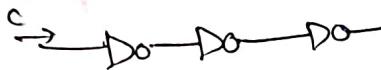
stage effort what?



Q:



$$Cout = 25C$$



$$H = \frac{25C}{3} = 25$$



All are same inverters

$$D_1 = (25 + p_{inv})^2$$

$$D_2 = ((25)^{1/3} + p_{inv})^2 \times 3$$

$$F = GBH = 1 \times 1 \times 25$$

$$D_1 = 25 + p_{inv} = 26$$

$$D_5 = ((25)^{1/5} + p_{inv})^2 \times 5$$

$$F = 25$$

$$D_2 = 3(25)^{1/3} + 3p_{inv}$$

$$\beta = (F)^{1/3} = (25)^{1/3} = 2.92$$

$$D_3 = 5(25)^{1/5} + 5p_{inv} = 11$$

$$p_{inv} = 1$$

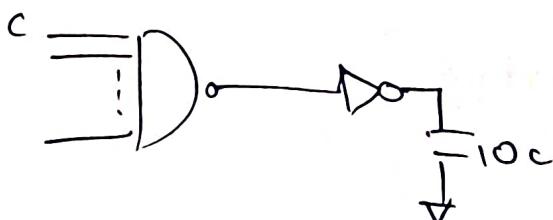
$$\begin{array}{l} \diagdown \qquad \diagup \\ \beta = (25)^{1/5} = 9.5 + 5 = 14.5 \end{array}$$

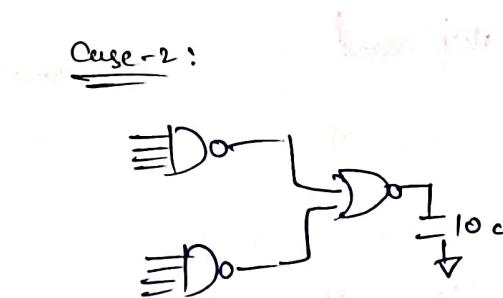
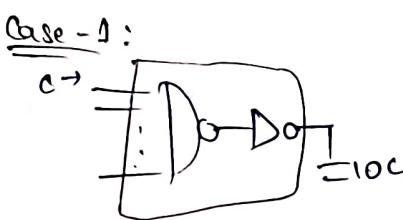
$D_2 \rightarrow$  min delay ✓ ☺

⇒ If we change 'H' our choice can change for getting min delay.

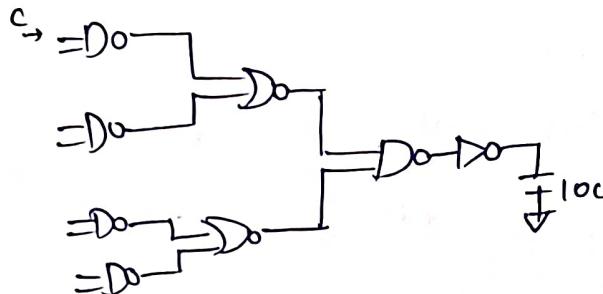
Eg: 8 9/p AND., H = 10

each input capacitance seen = C //





Case - 3:



From one input to out we will go

& write delay in  $\tau$  units

& find delay

which is min? Your answer

Delays

Case 1:

$$D = N(F)^{1/2} + P_{par}$$

$| N=2$

$$F = 10 \times 1 \times G = G = 5/3 \times 6$$

$$= \frac{10}{3} \times 1 \times 100$$

$$G = \frac{Nf_2}{3}$$

$$P_{par} = \frac{100}{3} f = \frac{100}{3}$$

$$\therefore D = 2 \times \left(\frac{100}{3}\right)^{1/2} + P_{par}$$

$\underbrace{P_{par}}_{\substack{\text{8-imp} \\ \text{Nand}}} + \underbrace{P_{inv}}_{\substack{\text{8-imp} \\ \text{Nand}}} + \underbrace{P_{inv}}_{\substack{\text{8-imp} \\ \text{Nand}}}$

$$= 2 \times \left(\frac{100}{3}\right)^{1/2} + 8P_{inv}$$

$N_{input} \Rightarrow N P_{inv}$

$$= 2 \times \left(\frac{100}{3}\right)^{1/2} + 9P_{inv} = 2 \times \left(\frac{100}{3}\right)^{1/2} + 9 = 20.55 \approx \text{units}$$

Case - 2:

$$N = 2$$

$$F = GBH$$

$$= g_{1g_2} \times 1 \times 10$$

$$g_{NAND-4} = \frac{4+2}{3} = \frac{6}{3} = 2$$

$$= \frac{5}{3} \times 2 \times 10$$

$$g_{NOR-2} = \frac{5}{3}$$

$$= \frac{100}{3}$$

$$P_{par} = \left(\frac{100}{3}\right)^{1/2}$$

$$D = 2 \times \left(\frac{100}{3}\right)^{1/2} + 4P_{inv} + 2P_{inv}$$

$\underbrace{P_{par}}_{\substack{\text{nand} \\ \text{nand}}} + \underbrace{P_{par}}_{\substack{\text{nand} \\ \text{nand}}}$

$$D_2 = 17.55 \text{ T units}$$

Case-3:  $\boxed{N=4}$

$$F = GBH$$

$$= 9_{1-4} \times 1 \times 10$$

$$\frac{4}{3} \times \frac{5}{3} \times \frac{4}{3} \times 1 \\ =$$

$$= \frac{4}{3} \times \frac{5}{3} \times \frac{4}{3} \times 10 = 800/9$$

$$\hat{\delta} = (F)^{1/4} = \left(\frac{800}{9}\right)^{1/4} \approx 2.33$$

$$D = 4 \times 2.33 + \underbrace{2+2+2+1}_{\text{Pars}} = \cancel{4+8+6+1} = 16.3 \quad \checkmark \text{ Best topology}$$



Now sizing of best  $\rightarrow$

$\stackrel{\circ}{\text{inv}}$

$$gbh = 2.33$$

$$1 \times 1 \times h = \frac{10}{2.33}$$

$$h = \frac{10}{2.33} = 2.33$$

$$h = \frac{10}{2.33} = 2.33$$

$\rightarrow$  Analyse - delay  $\delta$   
size it  $\odot$

If  $H=1$

$$D_1 = 2 \times \left(\frac{10}{3}\right)^{1/2} + 8 = 12.65$$

$$D_2 = 2 \times \left(\frac{10}{3}\right)^{1/3} + 6 = 9.65 \quad \checkmark \text{ Best topology} \Rightarrow D_2$$

$$D_3 = 4 \times \left(\frac{800}{27}\right)^{1/4} + 7 = 4 \times 1.3 + 7 = 12.24$$

Now size this //

From output to input