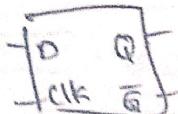


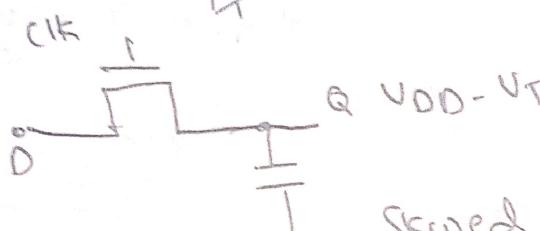
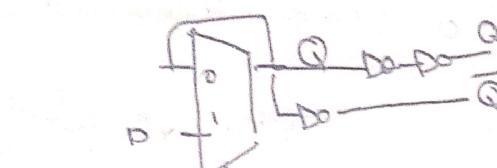
291

latch



if $CLK = 1$ if $CLK = 0$
 $Q = D$ $Q = 0$
else $Q = Q$ $Q = Q$

levelsensitivity latch



can't hold for long time

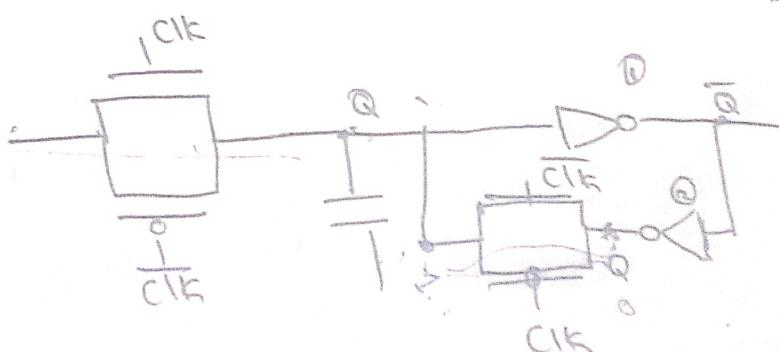
reverse saturation current

decays

before discharging again apply $CLK = 0$ so
charges again or else $CLK = \text{high}$



not need

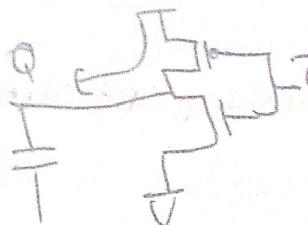


$CLK = 1$
 $Q = 0$

$\bar{Q} = \bar{0}$

$CLK = 0$

so Q will not get decay



Mos
Principles of
Semiconductors

Differential
amplifiers

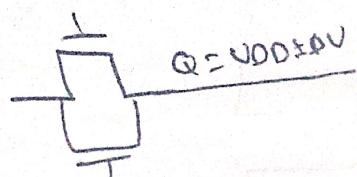
sense

adders

time constraining
SPICE
layout

Vhdl

fpga

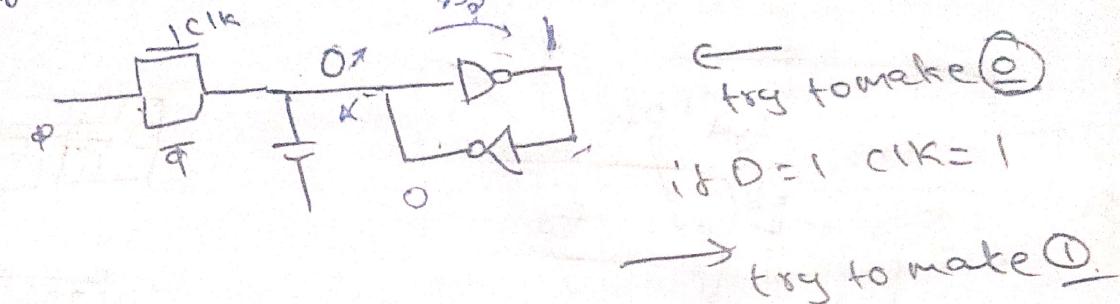


$$Q = 0$$

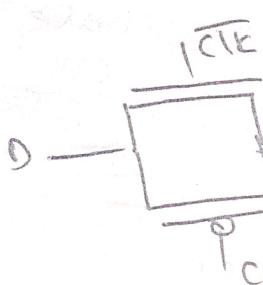
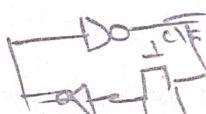
$$Q = 1$$

$$D = 1, \text{C} \bar{\text{K}} = 1$$

if transmission gate is not there

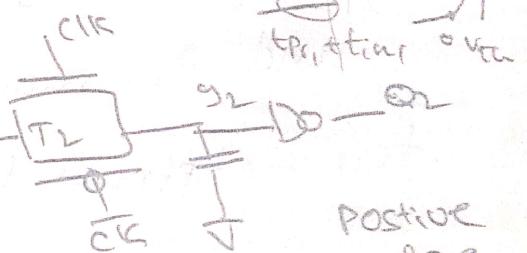
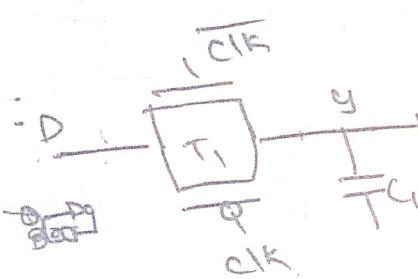


if



$$\text{if } CK = 0 \quad Q = 0$$

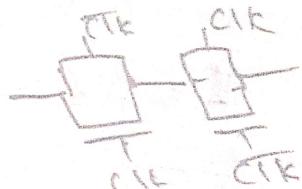
$$\text{else } CK = 1 \quad Q = Q$$



positive edge
Hi-P-Hop

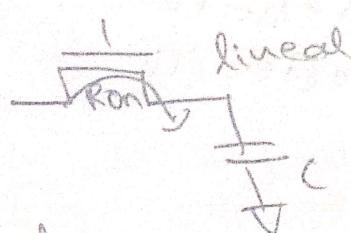
Without not gates we can't get \bar{Q}_2

now we will get \bar{Q}_2, Q_2

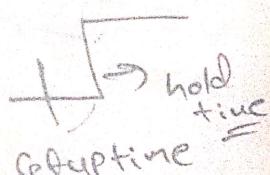


this is negative edge

now setup time / hold time

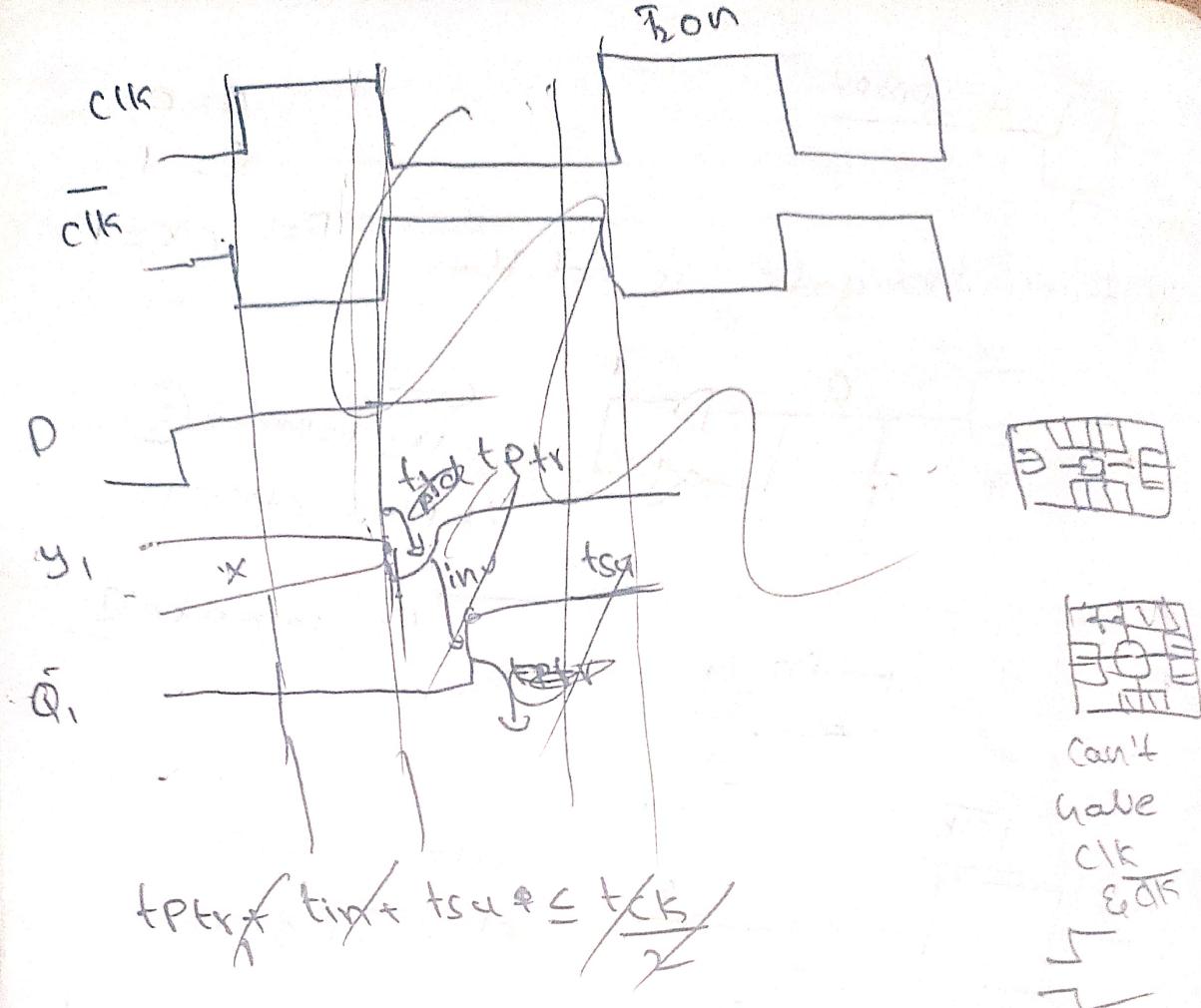


delay in transition also



R higher negar

RC so delay int'



before owing T_2 y_1 should stable else
and Q_1 should stable else

$$t_{\text{su}} = t_{\text{ptr}} + t_{\text{in}}, \text{ for getting}$$

$$\underline{t_{\text{hold}}} = 0 \Rightarrow 1 \text{ after}$$

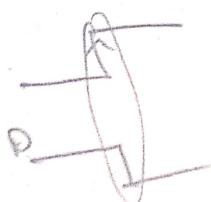
$$t_{\text{hold}} = t_{\text{ptr}} + t_{\text{in}}$$

$$\underline{t_{\text{hold}}} = 0$$

$$\begin{aligned} t_{\text{PCQ}} \\ = t_{\text{ptr}} + t_{\text{in}} \end{aligned}$$



input
should
hold
~~input~~
 $t_{\text{hold}} = 1 \text{ ms}$

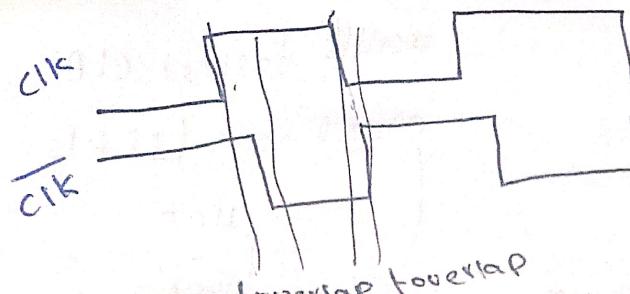


anyway T_1 off

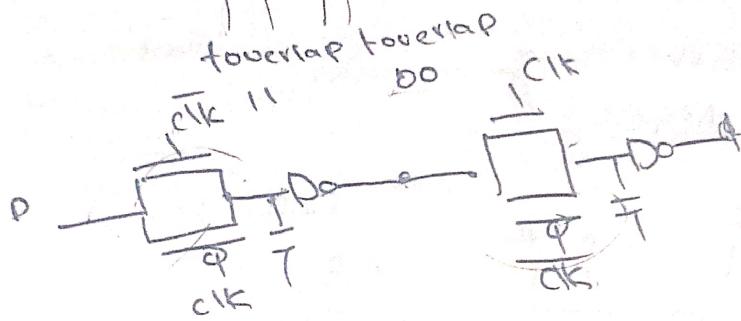
T_2 will not get effected

need not hold after Clk

$t_{\text{hold}} = 0$



$t_{00} \sim -1$
 $T_1 = \text{on}$
 $T_2 = \underline{\text{on}}$



it changes in t_{01} & changes

Q changes

$t_n \rightarrow t_{n+1}$

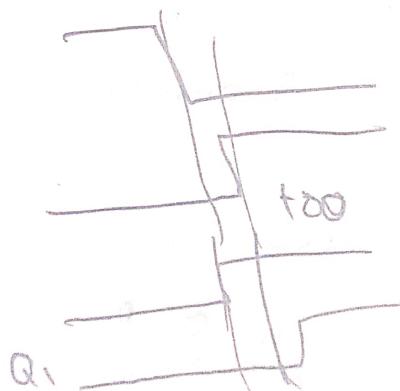
$t_{00} \underline{00} \rightarrow \text{neg edge}$

pmos on in both T_1 & T_2

then also $t_n > t_{00} \underline{00}$

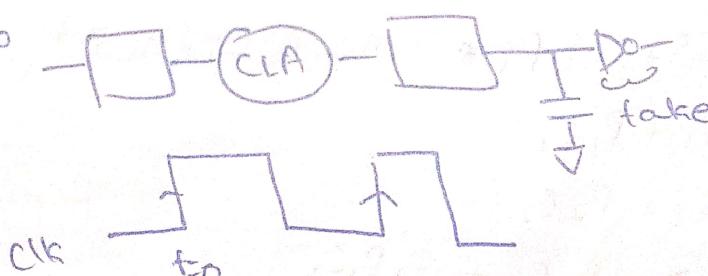
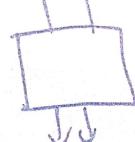
input not shielded
change in neg edge

t_{CK}



4/11/24

Project
 $A_2 \dots A_0$ $B_2 \dots B_0$



changes
& then overall
out changes
charge
tovil



$$t = t_{T_1} + t_{T_2} + t_{\text{off}} + t_I =$$

$$t_{T_1} + t_{I_1} > t_{00} \underline{00}$$

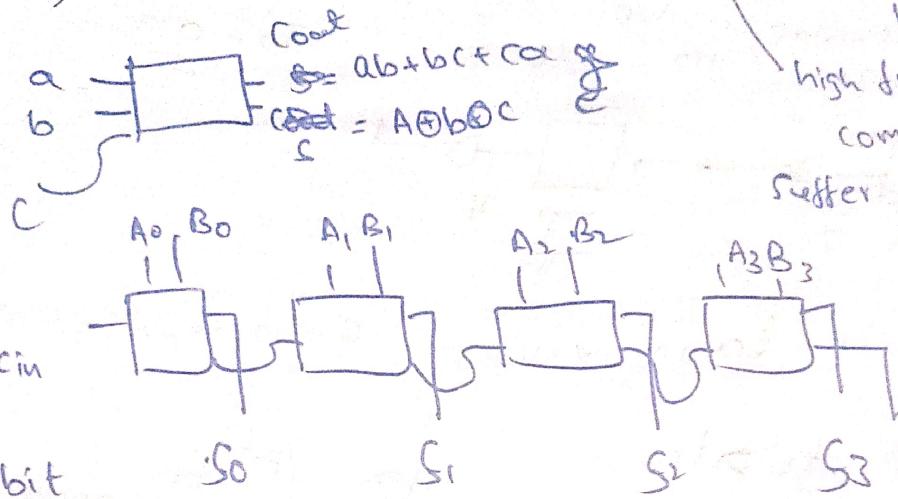
??

OSREG
clocked bands
 C^2 MOS
TSPC

1 CLK cycle
to compute
try to fpd less

$$A = \begin{smallmatrix} 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 \end{smallmatrix}$$

$$\frac{}{B = \begin{smallmatrix} 1 & 0 & 1 & 0 & 0 \end{smallmatrix}}$$



world's fastest CLA

max linear $|I| + B$

HFT
- within
Hardware

high frequency
components
suffer better

$d_1 + d_2 + d_3 + d_4 = \text{Ripple carry adder}$
large delay

to speed up RCA

Pre compute all terms don't depend on C_{in}

$$A_i^0 = 0, B_i^0 = 0, C_{out} = 0$$

$$\oplus \quad A \quad C_{in} = X$$

Kill condition.

$$\ominus \quad \otimes$$

$$K = \bar{A}_0 \bar{B}$$

$$A_i^0 = 1, B_i^0 = 1, C_{in} = X, C_{out} = 1$$

Generate

$$Q = A \cdot B$$

$$\begin{array}{c} A \\ B \\ \hline A \oplus B \end{array}$$

iii) $A_i^0 = 0, B_i^0 = 1$
 $A_i^1 = 1, B_i^1 = 0$

$$C_{out} = C_{in}$$

$$\begin{array}{ccccc} C_{in} & 0 & 1 & 1 & 1 \\ A & 0 & 0 & 1 & 1 \\ B & 1 & 1 & 1 & 1 \\ \hline C_{out} & 0 & 1 & 1 & 1 \end{array}$$

Propagate

$$P = A \oplus B$$

$$(i+1) = Q_i + (i) P_i + = A \cdot B + C_i \cdot (A \oplus B)$$

$$C_2 = Q_1 + P_1 C_1$$

$$C_3 = Q_2 + P_2 C_2$$

$$C_3 = Q_3 + P_2 Q_1 + P_2 P_1 C_1$$

$$C_{i+1} = C_i + P_i G_{i+1} + P_i P_{i-1} G_{i-1} G_i$$

all charges are got at a time

power delay product

later - IEEE conference template



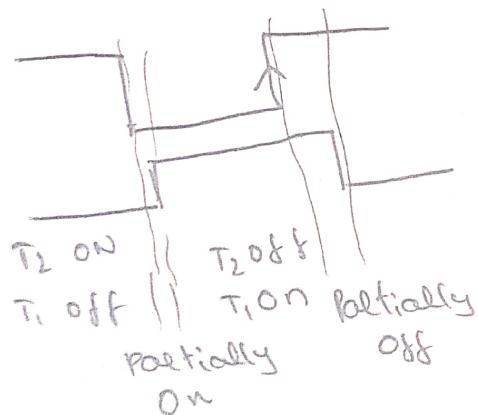
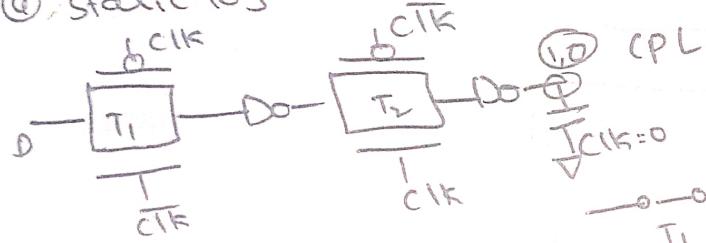
latches & flipflops

① CPL based (dynamic)

② CMOS (II)

③ TSPC (II)

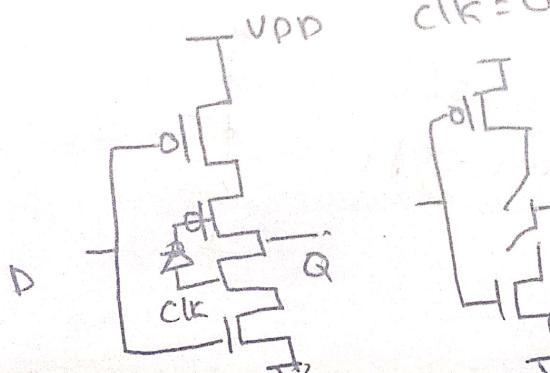
④ static logic gate based



threshold too high
Dynamic latch

to replenish

CMOS clocked CMOS



CLK=0

Q=0

High level sensitivity



[31]
ultra papers

ISSCC

top notch

conference

2 page

JSSC

IEEE

classic papers

Razavi:

Circuits for all seasons

articles

first TB

& scanning

& reading

RFIC

CICC 9

Measured chip results

ISCA 95

Simulation results

VLSI D

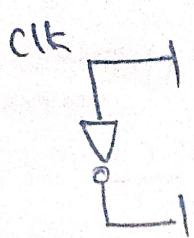
new cas

new cas

little thin

to make fast

low level sensitive flip flop

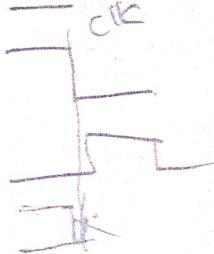
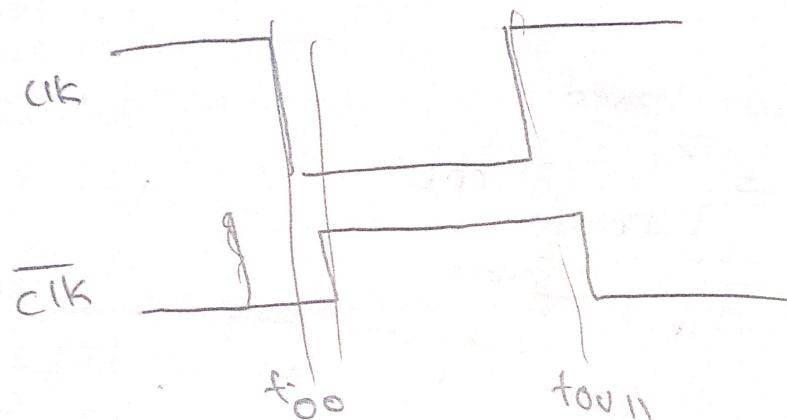
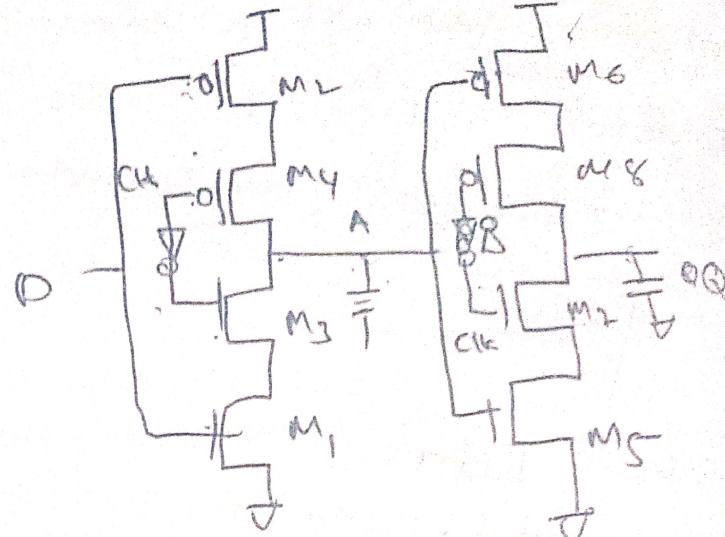


$$Ck = 0$$

$$A = \bar{D} \quad Q = Q$$

CK = 1

$$A = A \quad Q = \bar{A} = D$$



touco

D₂ 1 → 0 Mg - OH Mn - OH

A-Charges \rightarrow m_{g-on}, m_{f-off}

① holds
Previously

Mg - off

$D^o: O \rightarrow I$

A \Rightarrow B holds if A is satisfied & holds

tood

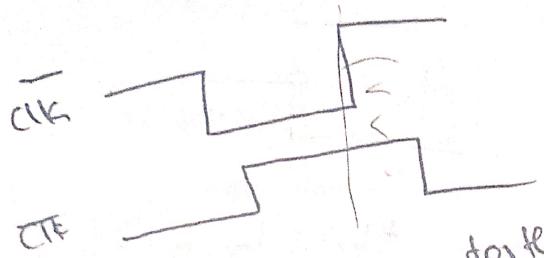
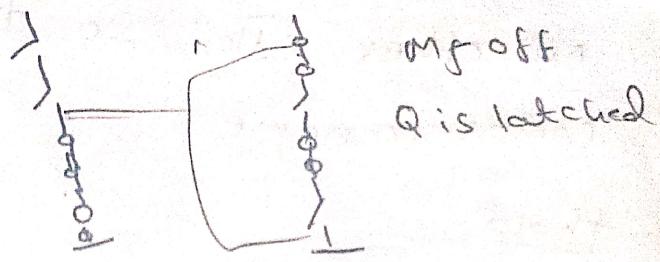
D₀ t → 0 M₃ - on M₄ - off
M₂ - on M₁ - off

A° holds

so Q holds

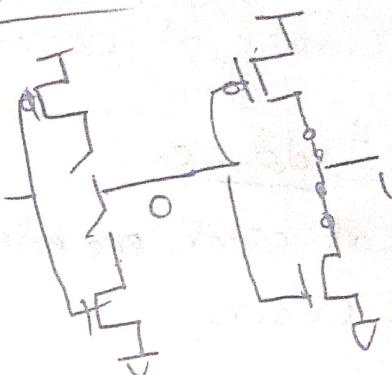
D: 0 → 1

A: discharges
Q: holds



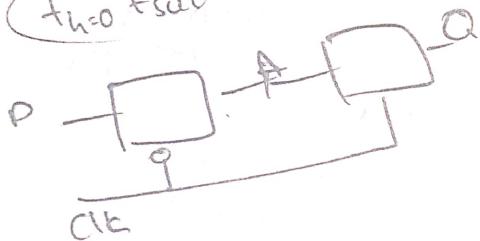
After t₁₁

for this
t_{hold} > t_{over} = 0



overall forbidden window constant

(two t_{set} sideways?)

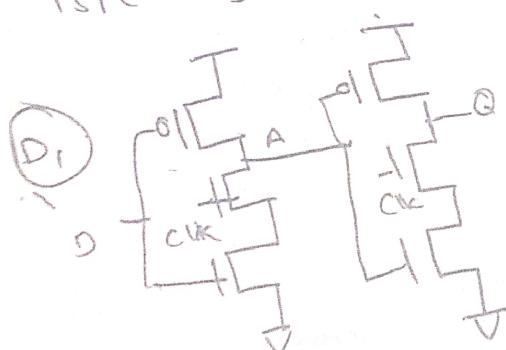


as A = 0
so Q = 1

before edge A should
be at reached state.

t_{su} = t delay 0 → A - t₁₁ ?

true single phase
clocked latch II FF
TSPC register



CK = 0

A = 0
D = 0 A = 1 Q = latch
D = 1 A = latch Q = latch

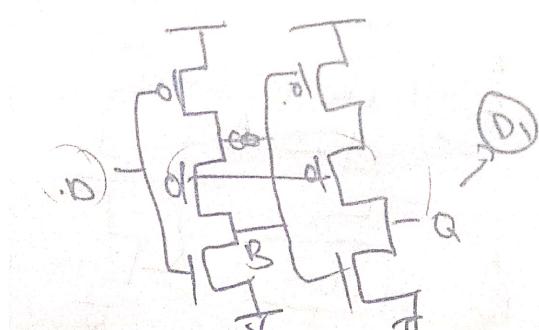
CK = 1

A = 0 Q = A = D

CK = 0

B = 0 Q = B = 0

CK = 1
D = 0 B = latch Q = latch
D = 1 B = 0 Q = latch
lowlevel Sistive latch



no other C_{IK} so true single phased
comes to name

hold

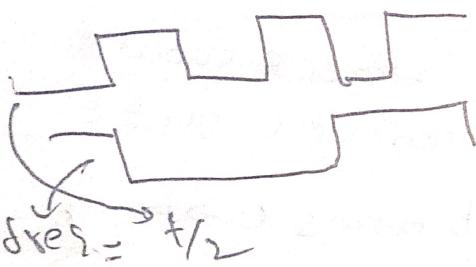
after clock edge

change at clocked edge

t_{hold} = 0

at clock edge at data

or change



Static nand gate ff

can't ~~be~~ met

TSPC can work loops +
hundreds

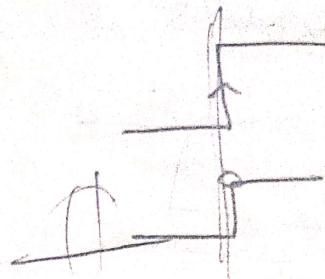
fails for OPs

TSPC - no C_{IK}, single phased

Razavi - TSPC circuit fail all sessions

NAND(ff) > TSPC
area

Add logic to latch



hold for latch!

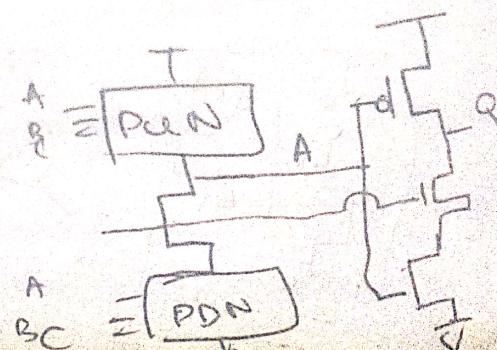
evenedge

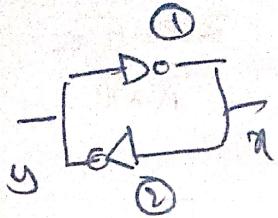
D -
evenedge setup held
want respond
as PS

Paper
(Xuan
Svensson)

D→JK
JK→D
T→JK

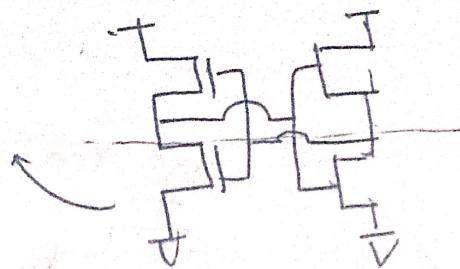
current
mode
levelieu
dividers
(ctrl)



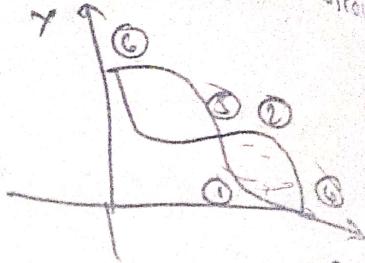


Small diff

$$0 \cdot \infty, 1 \cdot \infty, 0$$



interview question



battery graph

Slight difference
in goes to ①, ②

⑤ - metastable

⑥ bi stable

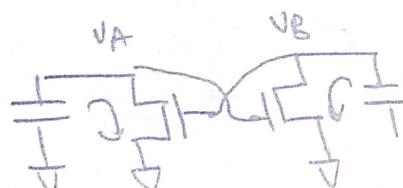
$$I_1 = -C \frac{dV_1}{dt}$$

$$I_2 = -C \frac{dV_2}{dt}$$

$$I_1 - I_2 = -C \frac{d}{dt} (V_1 - V_2) = -2C \frac{dV}{dt}$$

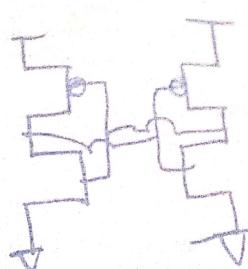
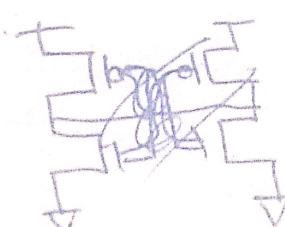
$$\left. \begin{array}{l} B(V_1 - V_T)^2 \\ B(V_{0m} - V_T)^2 \\ B(V_{0r} + V_T)^2 \end{array} \right\} \quad \left. \begin{array}{l} n(t) = n(0) e^{\alpha t} \\ (\alpha > 0) \end{array} \right.$$

do for each PMOS & NMOS

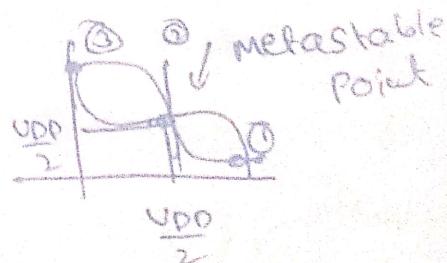


$$\text{if } V_A = V_B + \alpha \Delta$$

Property can be used to



\rightarrow $e^{(\beta) e^{\alpha t}}$
amplification

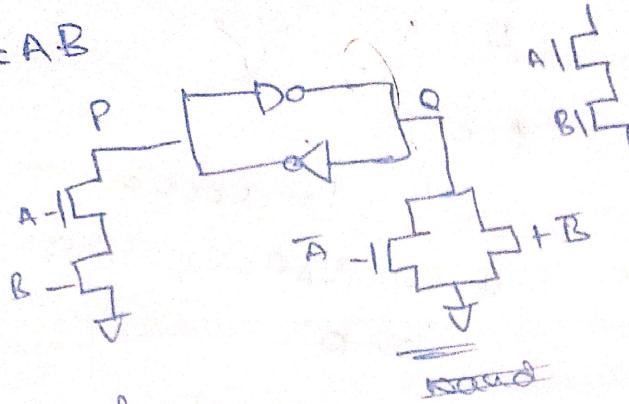


gain is too large
small perturbation at ①
then goes to ① or ②



How to do simulation of \rightarrow ?

$$f = AB$$



how to get noise
in simulation

$$A=1, B=1 \quad P=0 \quad Q=1$$

1	0	1	0
0	1	1	0
0	0	1	0

$$P = \bar{A} \cdot \bar{B} \quad Q = AB$$

$$A=1, B=1 \quad Q=0 \quad P=1$$

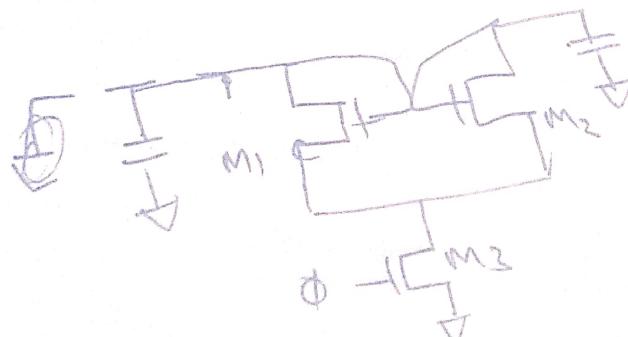
1	0	0	1
0	1	0	1
0	0	0	0

$$P = A + B \quad Q = \bar{A} + \bar{B}$$

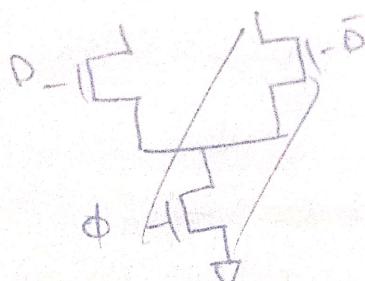
$$A+B$$

$$f = A+B \quad S = a \oplus b \oplus c$$

$$f = A + \bar{B} \quad \text{try this} \quad \text{and see}$$



Clock sense amplifier



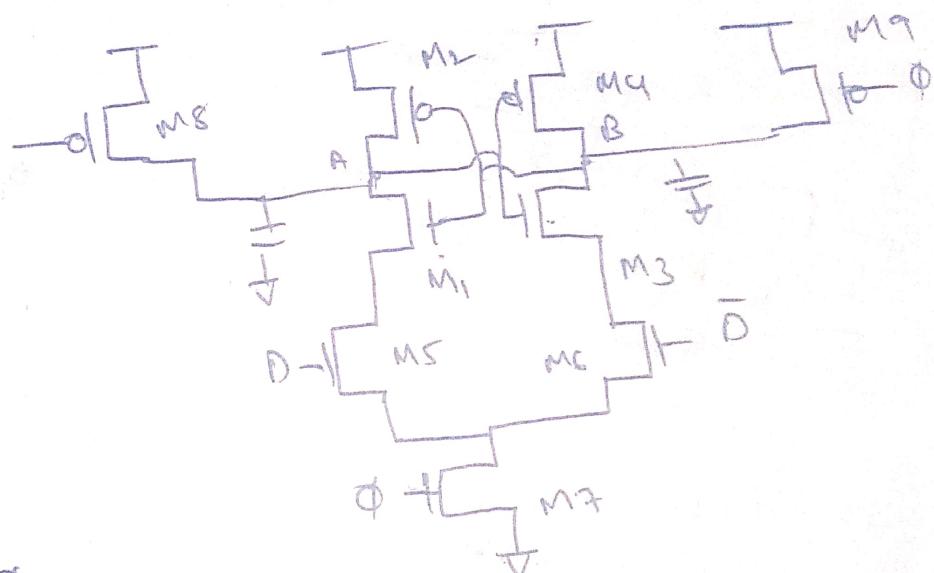
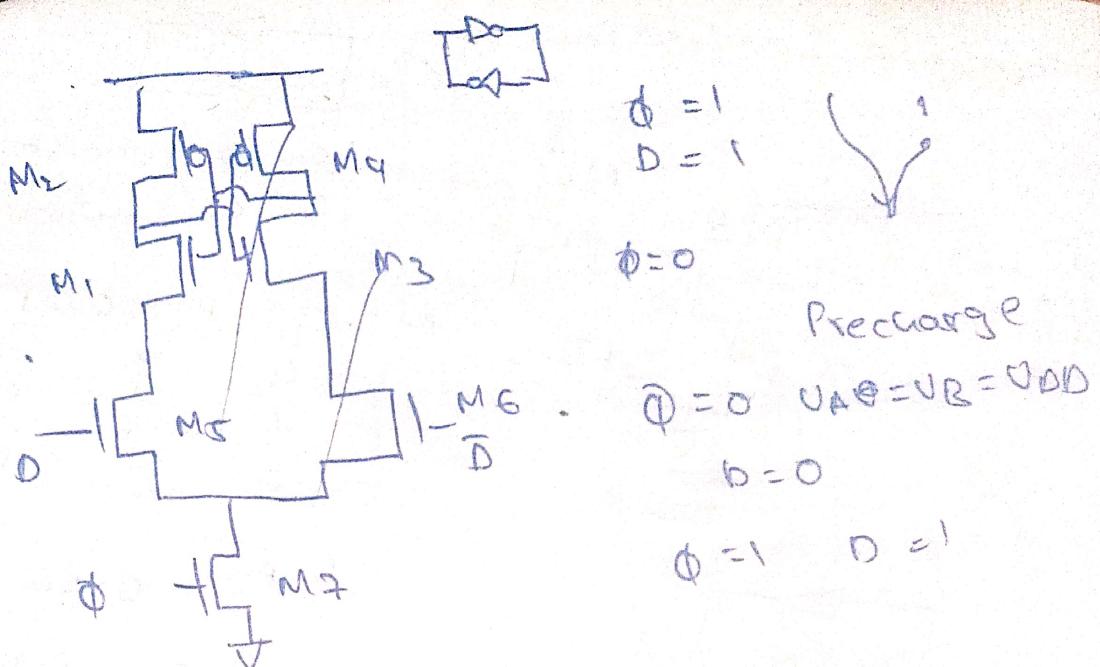
$$\Phi = 0 \quad (\text{idle state})$$

$$A = \text{wout} \uparrow \text{change}$$

$$B = \text{wout} \quad "$$

$$\Phi = 1$$

like an amplifier
both di.e.
 M_3 - deep triode



$$\emptyset = \emptyset \Rightarrow 1 = 0$$

$$VA = ? \quad VB = ?$$

stockage → leakage
as VA holds ms off

clf
50 M₃ gate
washiger voltage
no more current in

13

as $V_A = V_B \Rightarrow$
 B rechar

↳ more careful

W16.00

$$V_A = 1 \quad V_B = 0$$

25

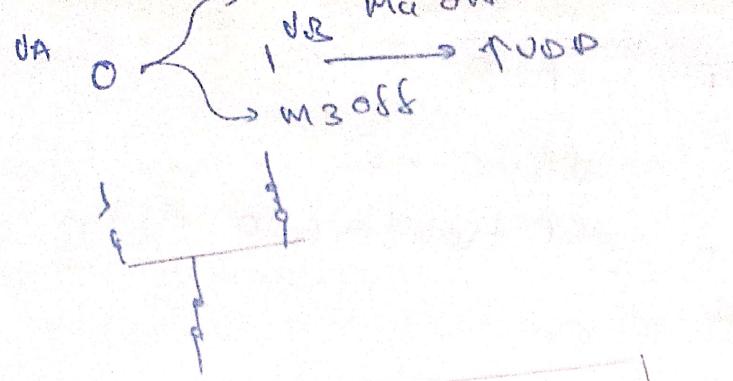
$$v_A = 0 \quad v_B = 1$$

$$\phi = 0.91$$

6

$$D=1 \Rightarrow 0$$

Now $\overline{AB} = 3$



$$Q = 0 \Rightarrow 1$$

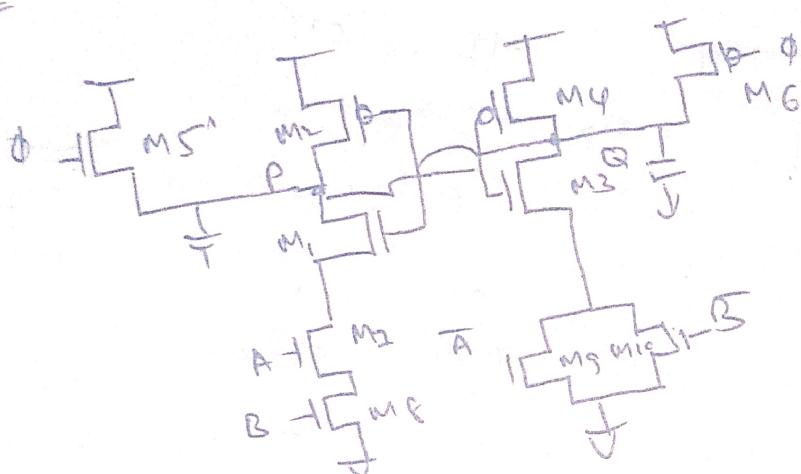
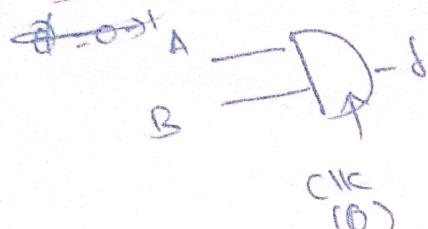
$$D = 0$$

$$V_A = 1 \quad V_B = 0$$

$$\text{then } D = 0 \Rightarrow 1$$

$$V_A = 1 \quad V_B = 1$$

this shows
edge triggered
differential
logic



$$D = 0$$

$$\text{forcing } V_P = V_Q = 1$$

If M_1, M_3 on

$D = 0$ after precharge

$$\begin{array}{cc} 0 & 1 \\ 1 & 1 \end{array} \quad V_P = 0 \quad V_Q = 1$$

$$\begin{array}{cc} 0 & 1 \\ 0 & 0 \end{array} \quad V_P = 1 \quad V_Q = 0$$

$$\begin{array}{cc} 1 & 0 \\ 0 & 0 \end{array} \quad P = \bar{A}B$$

$$Q = A \cdot B$$

and

word edge triggering

clock cycle should be long

more fanouting

less discharge

light load

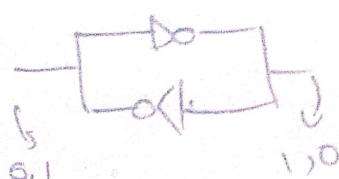
analog

for OR NOR

switch

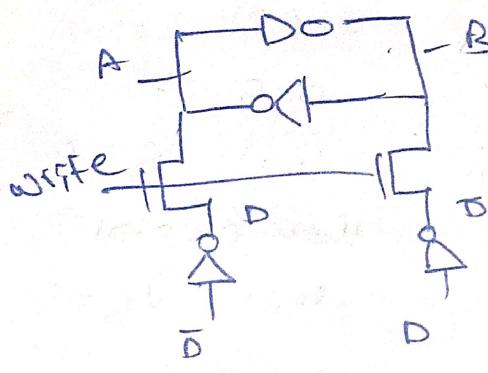
examination

some values



now to write voltage
on nodes

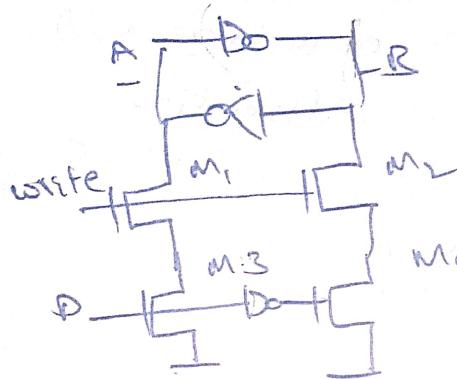




$$A = \bar{B}$$

write ω

D transfers to A & B



write = 1

$$D = 0$$

ON

ON

off

ON

$$VA = 1 \& VB = 0$$

out's stored in $\exists B$

$$B = D$$

write = 1

$$D = 1$$

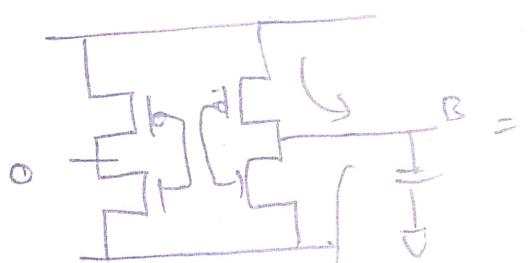
ON

ON

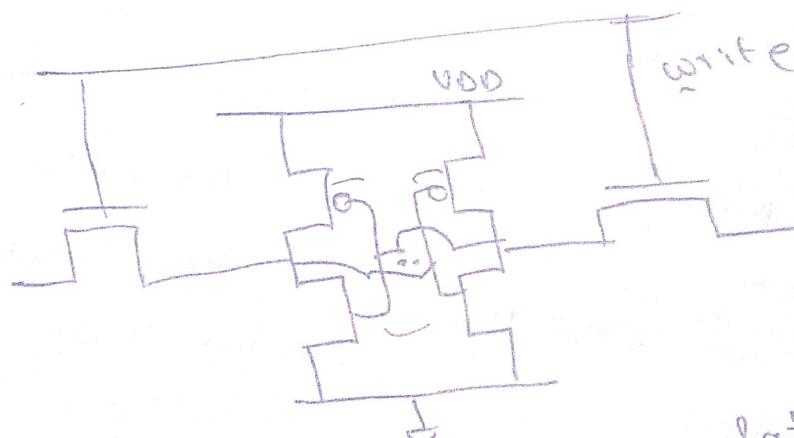
OFF

ON

$$VA = 0 \quad \exists B, VB = 1$$



should dominate
bottom



GT-cell

most basic

memory cell

latch

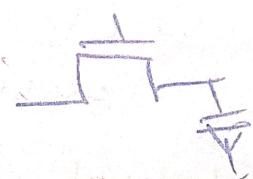
used in RAM

SRAM GTcell

volatile

Read Error

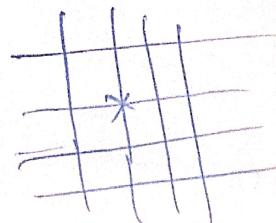
Dram cell



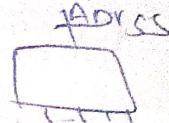
can't store
indefinitely
so charge
again.



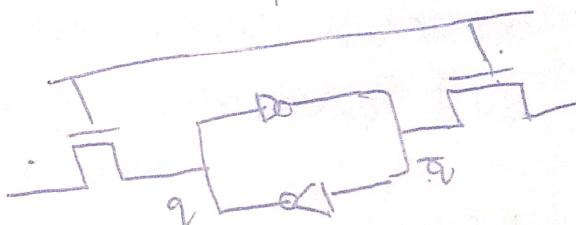
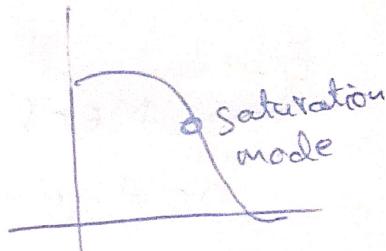
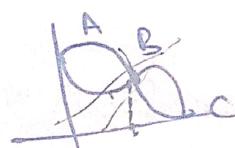
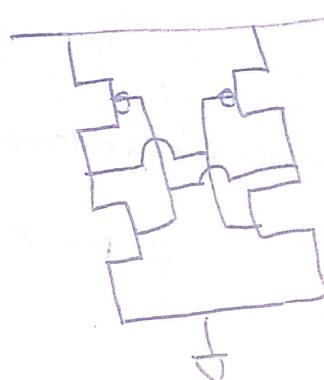
D-Ram
small area high memory density



row column
read write in next class



decoders
encoders

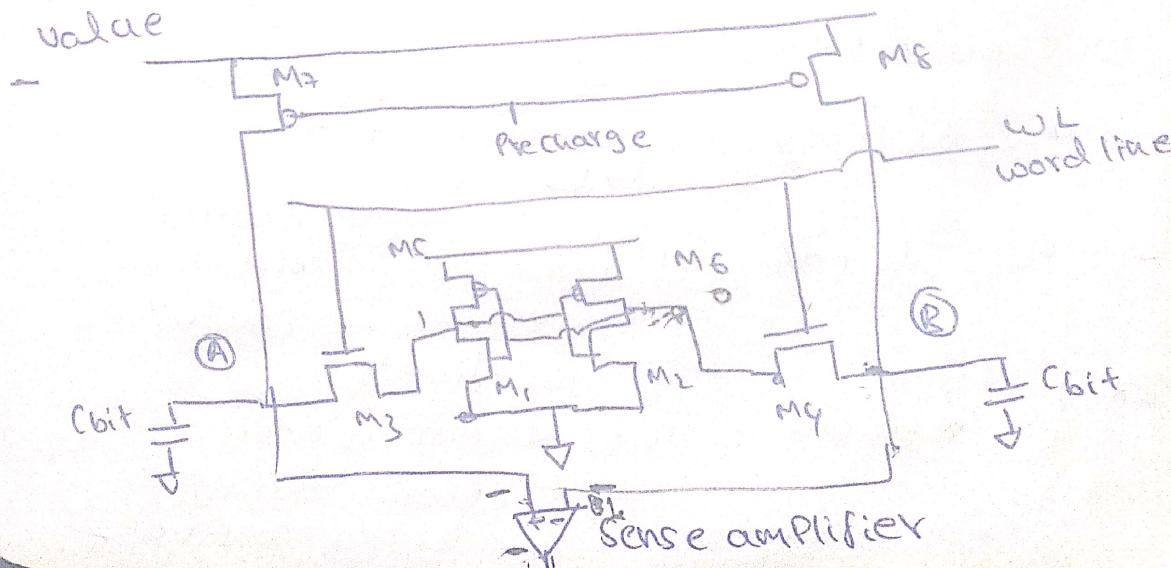


want to read what is stored
in cell CT memory cell

read operation

Idea is to the node voltages q, \bar{q} should be
only in ~~small~~ perturbation should not
cross the B as it changes value of
what stored

write should cross B voltage to change
value



$PC = 0$ $V_A = V_B = V_{DD}$ $q = 0 \bar{q} = 1$

$PC = 1$ M_3, M_4 turn on

$WL = 1$ $\bar{q} = 0$ $M_1 = ON$

$M_2 = OFF \quad q = 0$

Ⓐ V_{DD}

M_3 ON M_1 ON so A M_3M_1 gnd
discharges

$\bar{q} = 1$ M_6 off

no discharge from M_6

as Cbit high as long metal (more cells)
and parasitics from pass tr & PMOS
More time to read

No

as it is A & B are feded to sense amplifier
now small difference in ~~voltage~~ voltage if amplifies
the $V_A - V_B$ gives read operation in no
time

— $V_q > 0$ as current flowing from

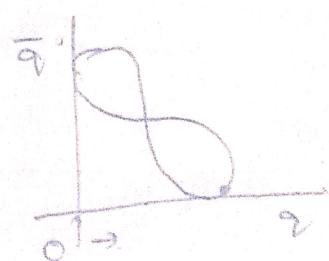
Ⓐ $V_q \uparrow \uparrow$

we should do $V_q < V_R$

as if change is
data

→ this happens if read
time

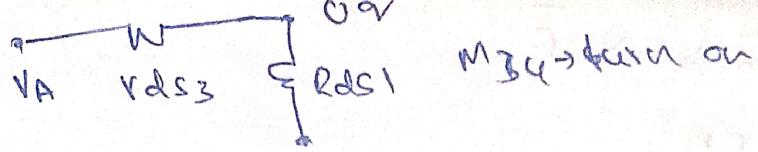
→ So memory control design is need
to know timing
constraints



read/write
operation
controls

indefinite
constrains





$$VQ = \frac{VDS_1}{VDS_3 + VDS_1}$$

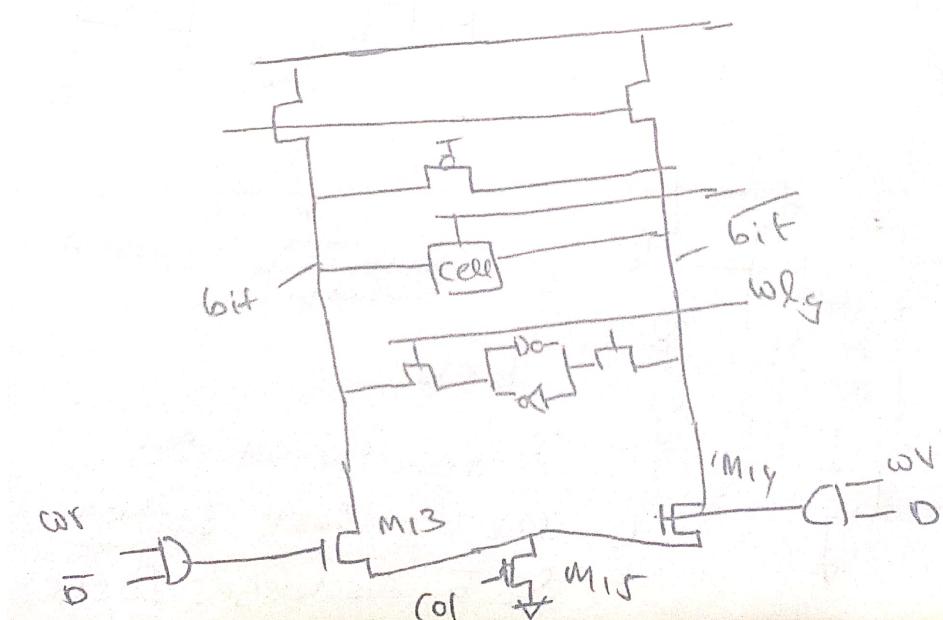
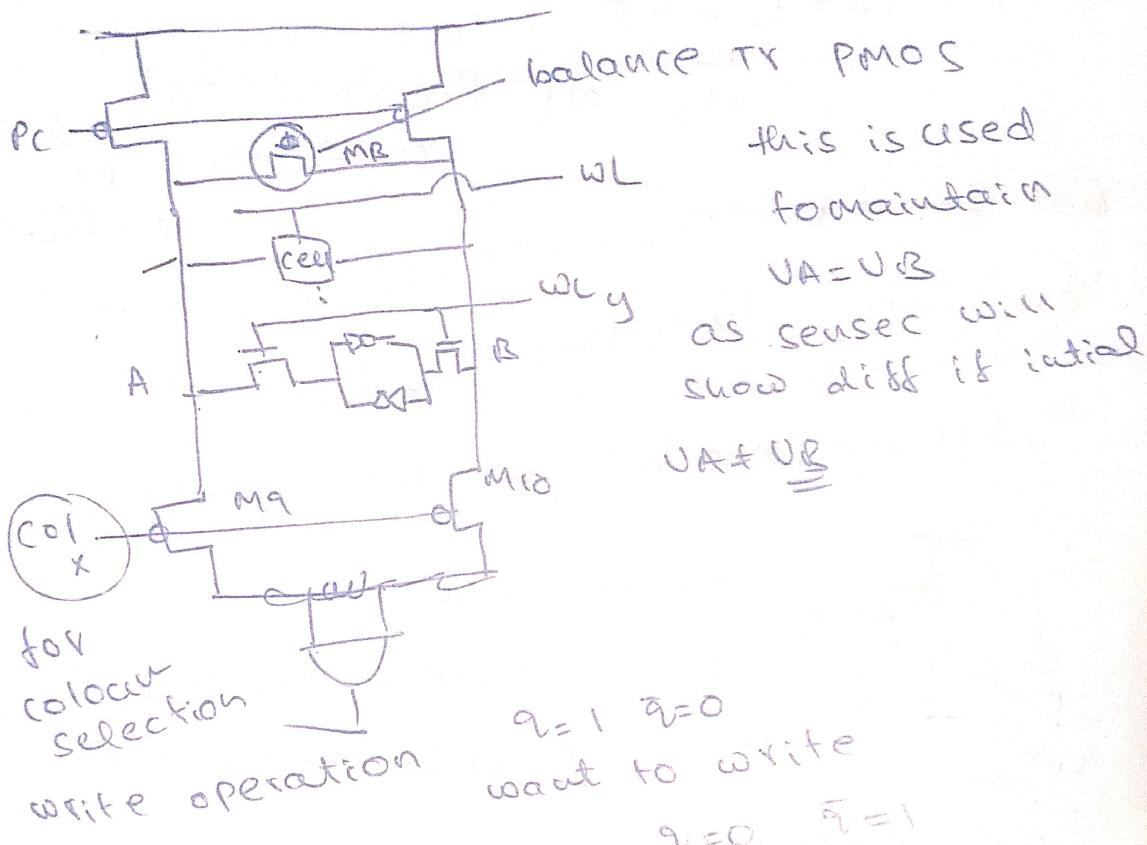
$$VQ = \frac{1}{S} UA$$

$$\text{if } VDS_1 = VDS_3 \frac{VDS_3}{W-S}$$

$$g_{DS_1} = g_{DS_3}$$

we can size them such

that this holds



$$PC=0 \quad \{b_6, \bar{b}_6\} = VDD$$

M_{15} ON

apply D & W M_{13} ON $\underline{M_{14}}$ OFF

M_{13} ON M_{15} ON bit ~~to~~ discharge S

why ON q starts to discharge

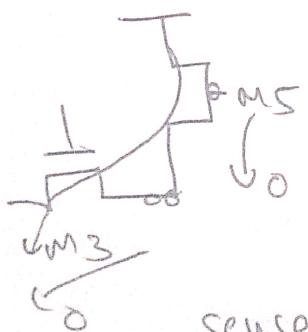
\bar{q} will get charged by $\overline{\text{bit}}$

as $q = 1 \rightarrow V_f \rightarrow 0$

M_2 off then \bar{q} will get charged by M_F PC

but for discharge will whole bit or need to discharge long time ??

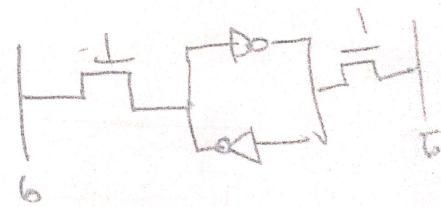
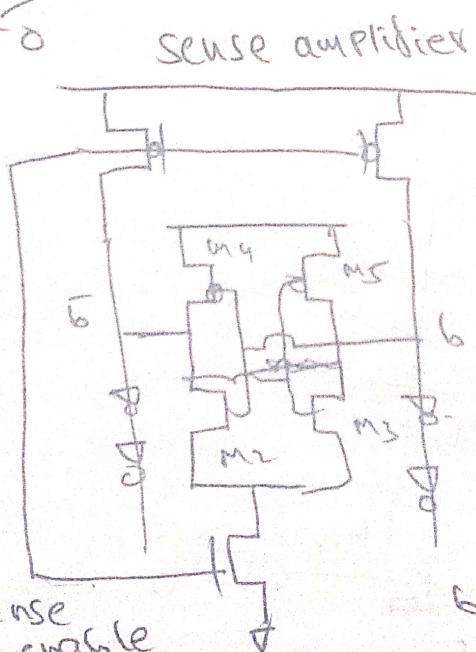
so for M_{13}, M_{15} big size for fast discharge



$M_3 > M_F$ width

so M_3 more conductance

than M_F ($R_F = R_M$ resistance)



$b < b'$

sense enable

b to b' through M_3

$b - M_2$ conduct faster
so b discharges faster

