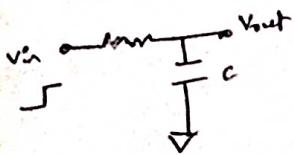
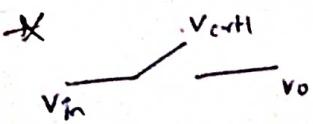


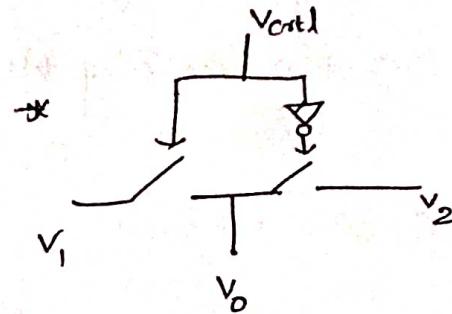
Lec-1:



$$V_{out} = V_0(1 - e^{-t/RC})$$



V_{Cout}	V_0
0	X
1	V_{in}

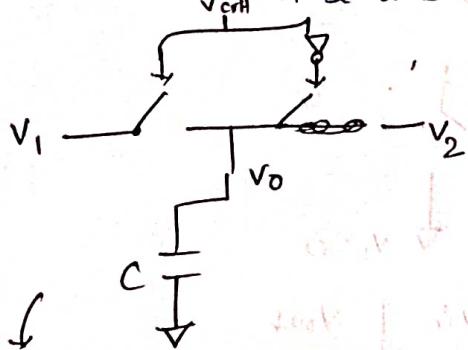


V_{Cout}	V_0
0	V_2
1	V_1

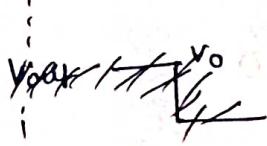
if $V_2 > V_1$

(H) (L)

then the overall circuit will be like NOT GATE (INVERTER)



Let $V_1 = 0, V_2 = V_0$



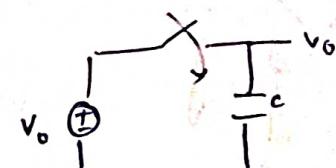
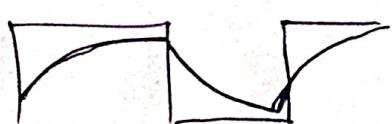
(Inverter)

Let V_{Cout}

if RC is very very small than time period



if RC is very very high



$$V_o(0^-) = 0$$

$$V_o(0^+) = V_0$$

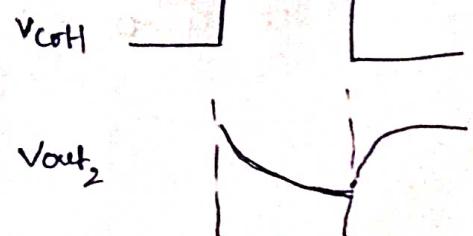
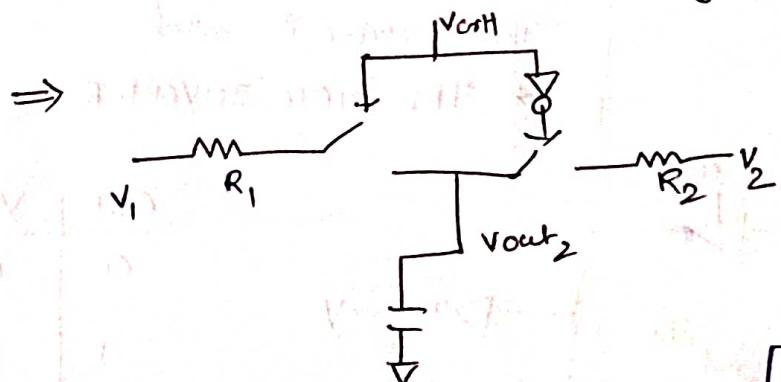
why?

KVL always ✓

We need to have an Impulse current.

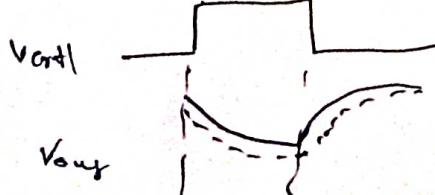
* If impulse current not provided get happen then it won't change

* if impulse current very high, it may break



if R_2 is 1sec

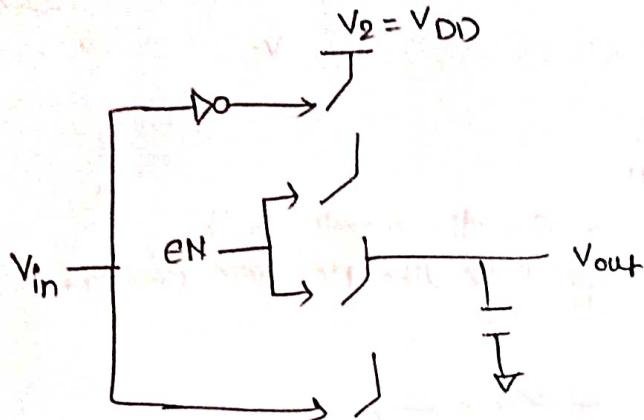
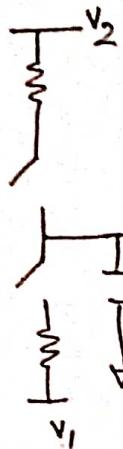
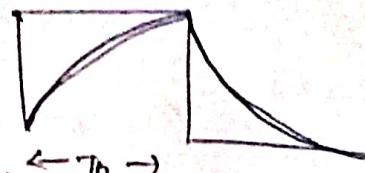
$RC \approx 1\text{ sec}$, $\approx 1\text{ sec}$, delay will 1 sec



For high RC we want complete cycle like

then we need more time period

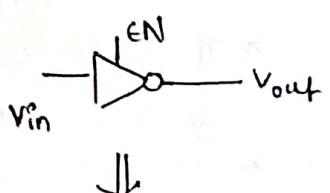
↓
low frequency we need,



overall circuit symbol



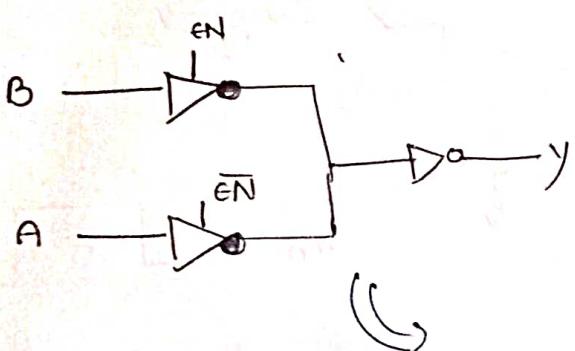
overall circuit symbol



EN	v_{in}	v_{out}
0	X	Z (High impedance state)
1	0	1 (V_{DD})
1	1	0

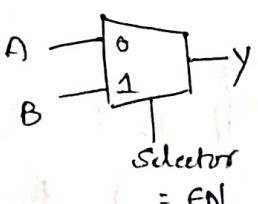
This inverter is called

* TRI-STATE INVERTER *

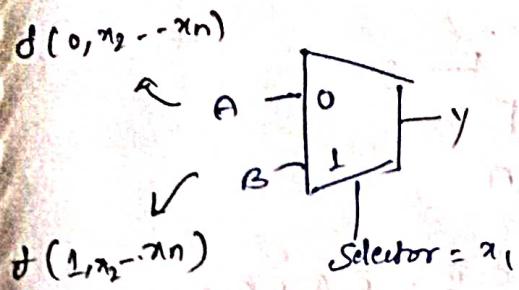


EN	y
0	A
1	B

↳ This is Working of 2-Mux



Shanon's expansion: $f(x_1, x_2, \dots, x_n) = \bar{x}_1 f(0, x_2, \dots, x_n) + x_1 f(1, x_2, \dots, x_n)$



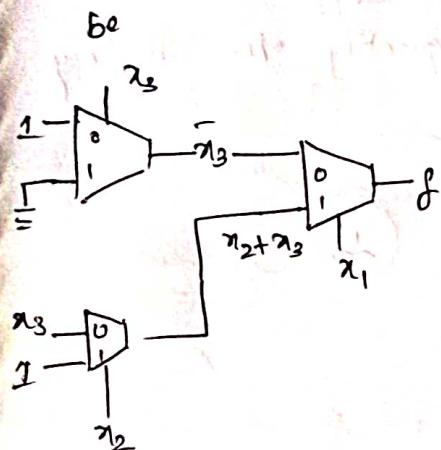
Q: Realise this funcn with 2-Mux's only ??

$$f = \bar{x}_1 \bar{x}_3 + x_1 x_2 + x_1 x_3$$

A) Let x_1 = selector

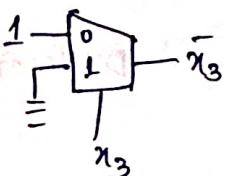
$$\bar{x}_1 \bar{x}_3 + x_1 (x_2 + x_3)$$

therefore overall circuit will

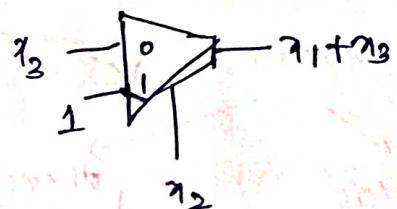


We need to implement
Not gate

We need to implement
or gate with 2 mux



$$x_2 + x_3 = x_2 + \bar{x}_2 x_3$$

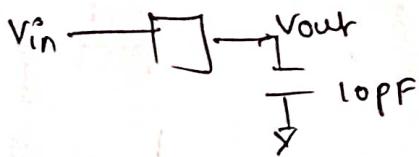


Rc should be low

to realise Higher frequency circuits

Electrical specification ... ?

Problem:



it should drive 10 pF - ??

drive - ??

3-8-24

Saturday.

Lec-2

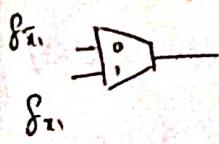
Recap:



using Multiplexer, we can realise any combinational logic.

with
from
Tri-State-Inverter

$$f(x_1, x_2, \dots, x_n) = \bar{x}_1 f(0, x_2, \dots, x_n) + x_1 f(1, x_2, \dots, x_n)$$

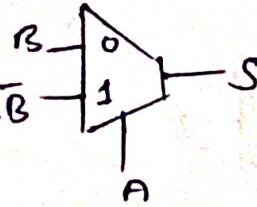


Pivot Variable \rightarrow (here it is x_1)

$$\rightarrow S = A \oplus B \quad C = AB$$

$$G = \bar{A}B + A\bar{B}$$

$$AB + \bar{A}\bar{B}$$

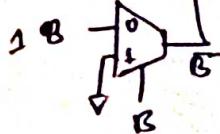


$$f = \bar{B} = \bar{B} \cdot 1 + B \cdot 0$$

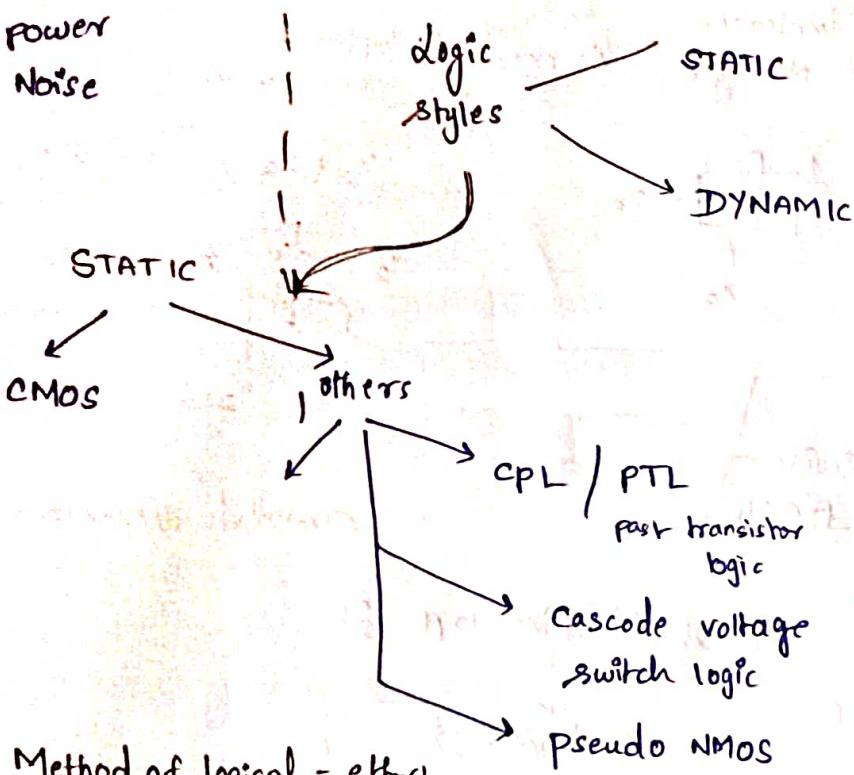
Efficient - Digital circuit

How we will quantify
in digital?

- Speed
- Delay
- Power
- Noise



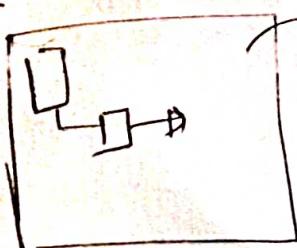
In analog, bandwidth, fan-out etc.
we will quantify our efficiency.



→ Method of logical effort

↳ Multistage logic design for delay optimisation.

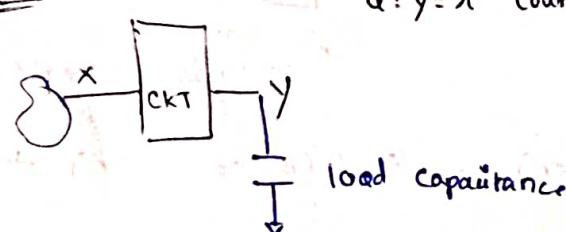
Syllabus



different
combinational
of circuits

Q_i

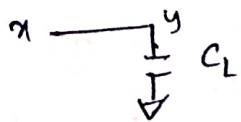
$Q_i : y = x$ (our requirement)



How we will get $y = x$?

SPICE
&
MAGIC

(A) one of soln:



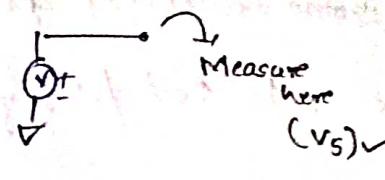
is it a soln always.

What is probm? →

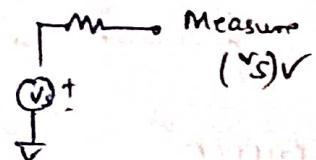
$$\begin{array}{lll} \text{If } x \text{ is H} & C_L \text{ H} \\ x \text{ is L} & C_L \rightarrow L \end{array}$$

✓
Not a problem

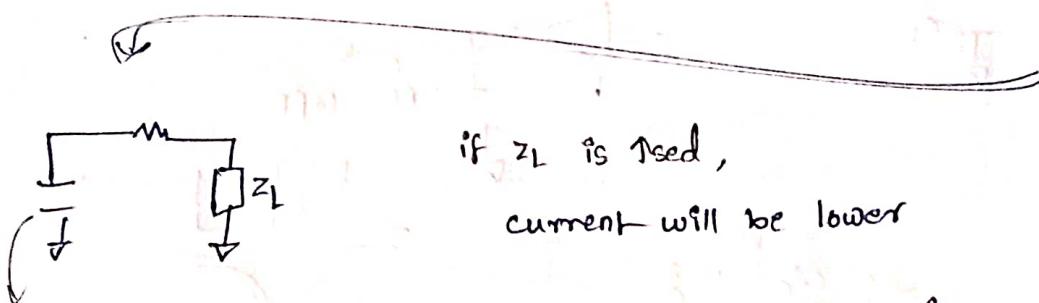
Impulse current



Measure here
(VS) ✓



Measure
(VS) ✓



if Z_L is used,
current will be lower

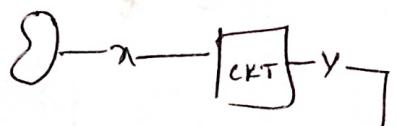
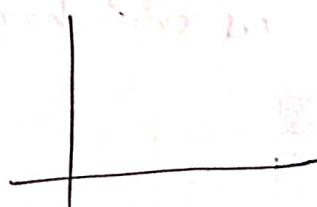
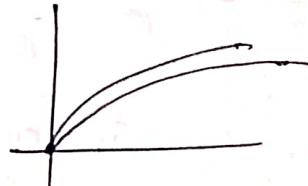
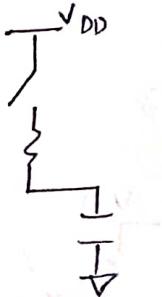
⇒ let Z_L be a capacitor

same amount of V_S
stored in capacitor

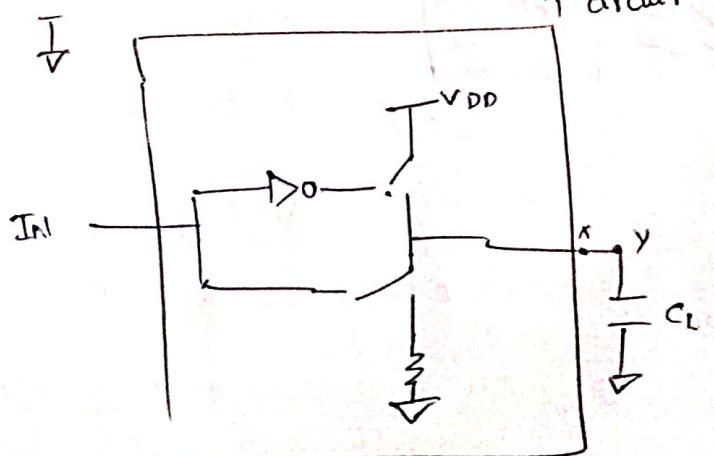
$$\frac{1}{T}$$

the amount of time
taken to charge the
two capacitors is
different

∴ delay of capacitors is
different.



we will design



We choose a certain R & C such that our delay is minimized ✓

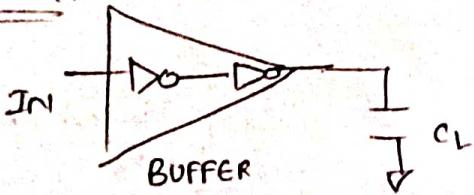
But if C_L is used / changed

our delay will change

charging & discharging time will be different.

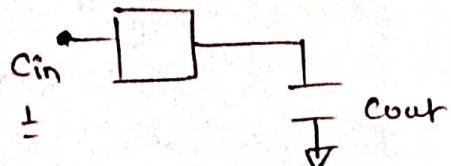
$y \Rightarrow$ it is Not a good soln.

∴ BUFFER:



20 PF
100 PP

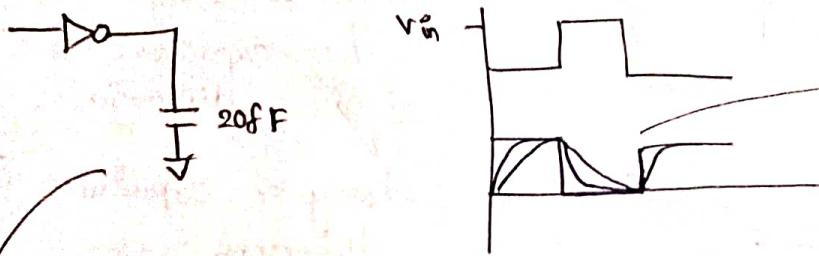
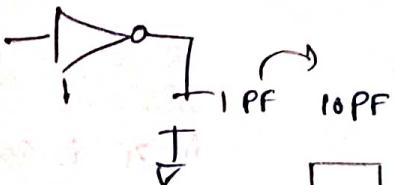
charging &
discharging
time \approx 1 sec.



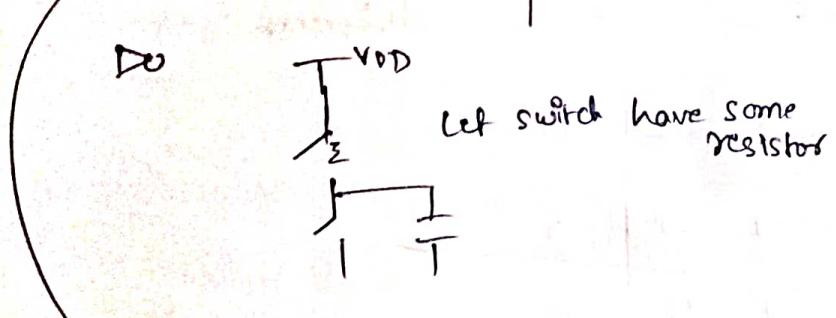
Ex: $C_{in} = 10f$ (capacitive load)

$C_{out} = 10p$

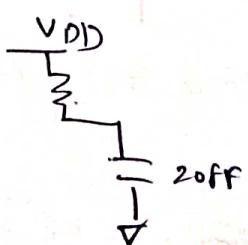
design a min-delay circuit.



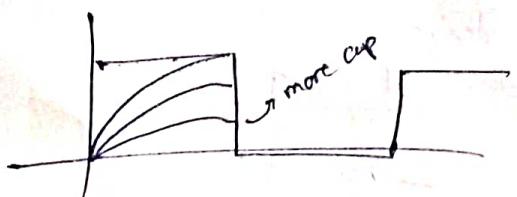
Black more capacitance
blue less " (ideal output)



It will be as



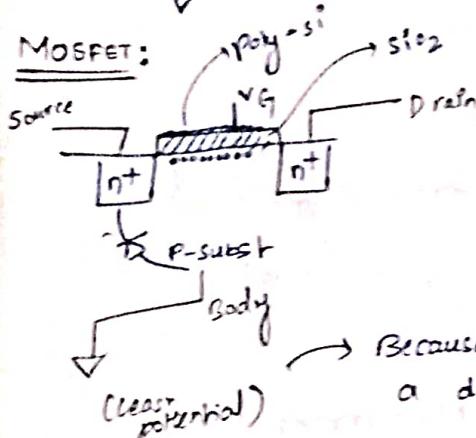
as capacitance
 $\propto C$



Prerequisites

- RC Analysis
- MOS Transistor
- DSM

T_{SiO_2} we want Si + SiO_2 (Gr) sum on for low & High

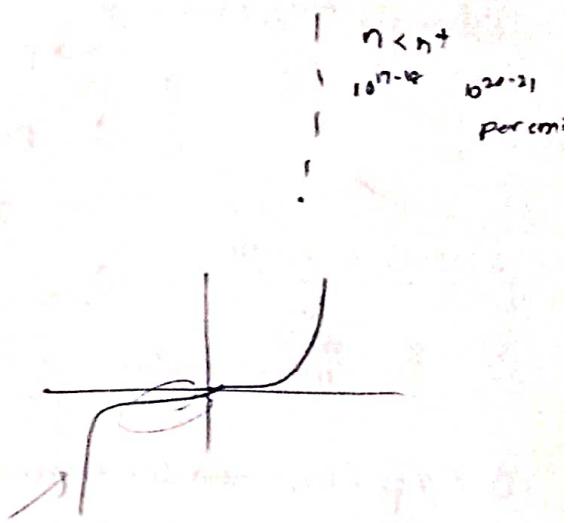


Because n-p zone making
a diode

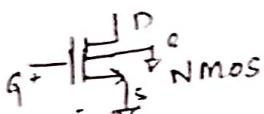
↙ ✓ ∵ We don't want any current
in diodes

∴ should be Reverse Bias

∴ p side should be low potential.



$V_{GS} < 0$



↙ ↘ we will take Source as Reference Voltage.

$V_{GS} < 0$ → Accumulation mode

Accumulation Mode. ↘ Holes will accumulate near gate

↙ ↘ No current will flow (Reverse bias with n^+ & P-subst) ⚡

$V_{GS} > 0$

↙ Holes near region pushed away. Depletion mode.

↙ if we keep rising V_{GS} , holes away

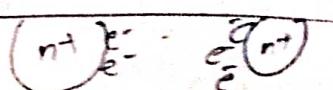
↙ we supply a force, pushed away.

↙ Depletion region forms

↙ Drain to source current NO current

↙ If rise V_{GS} , keep on rising V_{GS} , the e^- from n^+ will experience some force & pulled to region.

↙ e^- from n^+ starts coming out



$V_{GS} > V_{th}$ (threshold)

The minority carriers in p-substrate is Tsing.

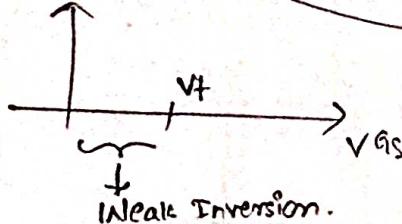
Strongly INVERTED ZONE

e⁻ coming in region

p-type is changing to n-type

Both minority & majority carriers will get equal

Created a channel. (for passing current)

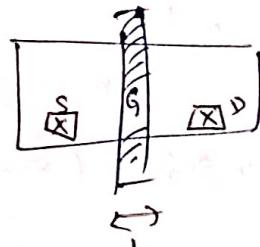
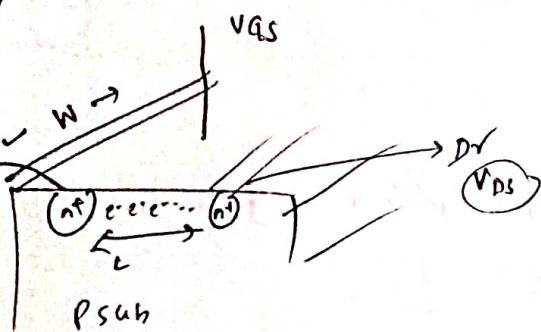
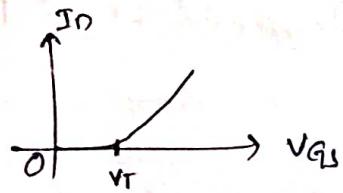
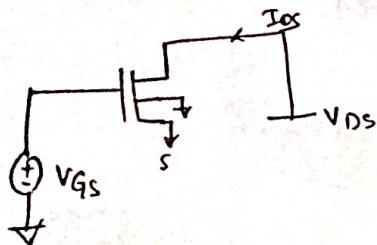


$V_{GS} \leq 0 \Rightarrow$ No current
cutoff region

$0 < V_{GS} < V_{th} \Rightarrow$ Sub-threshold region

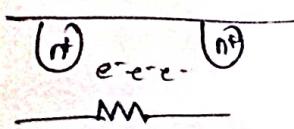
$V_{GS} > V_{th} \Rightarrow$ Strong inversion

⇒



as L↑se, Resistance ↑se

if w↑se, Resistance ↓se (by const L)



$$R \propto L, \quad R \propto \frac{1}{W} \quad \Rightarrow \quad R \propto \left(\frac{1}{W} \right) L$$

⇒ $V_{GS} > V_t$

Now we Tsing V_{DS} ,

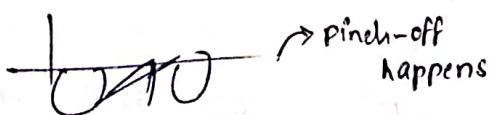
keep on Tsing V_{DS} → What happen →

$$V_{GS} - V_{DS}$$

$$= V_{GD}$$

as V_D Tsing, $V_{GD} \downarrow se$

\therefore channel length decreases from Drain side.



Cutoff

Saturation $V_{GS} \geq V_T$ & $V_{DS} \geq V_{GS} - V_{th}$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

Linear $V_{GS} \geq V_T$ & $V_{DS} \leq V_{GS} - V_{th}$

$$I_D = \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}$$

2nd order effects: (for short channel)

CLM

Mobility degradation

$$\tau_0 = \frac{1}{\lambda} I_D$$

$$\xrightarrow[V_{GS}]{V_{DS}}$$

applying V_{GS} & V_{DS}

e⁻ field existing in both hori & vert dirn

E field
charge carriers

charge carrier experience

some force

leads to scattering

$\rightarrow G$

charge carriers

overall drift velocity reduced



we can see significant reduction in current. g:

\therefore mobility is reduced

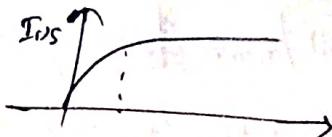
(50% or more)
for long-length

feature
min size drawn /
fabricated
in a particular foundry

Technology

most of time it
is equal to

L-channel. Its not
always channel
length



$\tau_0 \rightarrow$ Not very useful for digital case

why current gets saturation..?
Doubt.

V_{DS} true
so subtraction
going

$Tc/A \propto e \rightarrow cost/transistor$

Area of transistor $\propto A \rightarrow$ fabrication cost

so because cost/Area is rising

Velocity saturation

Doubt...?

DIBL

$$V_T' = V_T - \eta V_{DS}$$

Body effect:

(if $V_B = 0$)

V_{DS} In short channel

V_T is not independent of V_{DS} .

$$V_T = V_{TO} + \gamma \left[\sqrt{2\phi_c + V_B} - \sqrt{2\phi_c} \right]$$

Sub-threshold:

$$V_{GS} < V_T \quad I_{DS} = I_{DS_0} e^{\frac{V_{GS}-V_{th}}{nV_{th}}} \left[1 - e^{-V_{DS}/V_T} \right]$$

if $V_{DS} = 0 \rightarrow I_{DS} = 0$

if $V_{DS} \gg 2V_T \Rightarrow$ if we \uparrow V_{GS} slightly current will \uparrow exponentially

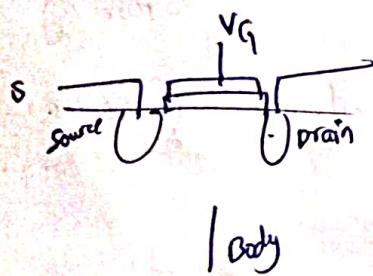
7-8-24
Wednesday

⇒ Skywater 130 nm || get parasitic capacitance etc.
due to metal connection's
leaving a design technique

⇒ Weiste & Harris
& Cisbrowinger

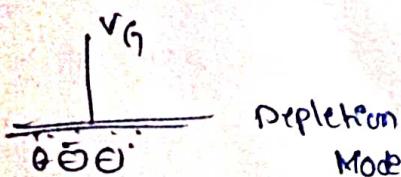
Razavi/Sedra

MOSFET:



We want current from D to S with no leakage.

∴ our Body voltage should be very low.
→ to not get leakage



if we keep on \uparrow V_G
the drain & source will



Sat: Carriers always move from S to drain : (either e⁻ & holes both)

$$I_{DS} = \frac{1}{2} \mu n C_o x \frac{W}{L} (V_{GS} - V_{Th})^2$$

Linear.

$$V_{GS} < V_{DS} < V_{GS} - V_{Th} \quad (\text{acts like resistor})$$

$$I_{DS} = \mu n C_o x \frac{W}{L} (V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2}$$

$$V_{GS} < V_T, I_{DS} = 0$$

Sub-Threshold condn $\rightarrow I_{DS} = I_{DS0} e^{\frac{V_{GS}-V_{Th}}{V_{thermal}}} \left[1 - \frac{V_{DS}}{V_{thermal}} \right]$

$$V_{thermal} = \frac{kT}{q}$$

$$\approx 26mV @ 300K$$

$$\frac{1}{e^{\frac{V_{DS}}{V_{thermal}}}}$$

if $V_{DS} = 2 \text{ times } V_{thermal}$

3 times

we will ignore $\frac{1}{e^x}$, wrt to 1.

$$\therefore I_{DS} \approx I_{DS0} e^{-x} \quad \Rightarrow x = V_{Th} - \frac{V_{GS}}{V_{thermal}}$$

$$\boxed{\therefore I_{DS} = \frac{I_{DS0}}{e^x}}$$

for a given V_{GS} & V_{Th}

$$\text{let } V_{GS} = 0.5$$

$$V_{GS} = 0.3V$$

$$I_{DS0} = \mu n C_o x \frac{W}{L} (V_{thermal})^2 e^{1.8}$$

$$V_{GS} = 0.3V$$

$$V_T = 0.5V$$

case-1:

$$\frac{I_{DS0}}{e^{0.2/V_{thermal}}}$$

$$\frac{I_{DS0}}{e^{0.1/V_{thermal}}}$$

$$\frac{I_{DS0}}{e^{0.1/V_{thermal}}}$$

* lower tech \rightarrow more no. of trans

\rightarrow each's leakage \rightarrow so more leakage. h

lower tech - less
lot of power
wasting as
leakage. h

For our analysis, For $V_{GS} < 0$, we can say our current is very small
(ignoring current)

V_{TP} is Negative

If we have +ve V_{TP}

$$V_{TP} < 0$$

n-well attract more e⁻
more.

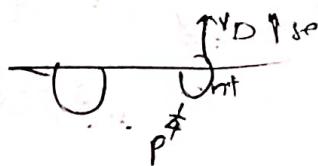
$$\Rightarrow V_{SGP} > |V_{TP}| \quad (\text{or}) \quad V_{SGP} < V_{TP} \quad (\text{since } -V_0)$$

-0.6 < -0.5 : Ex:

$$I_{SDP} = \frac{1}{2} \mu p C_o \omega \frac{W}{L} [V_{SGP} - |V_{TP}|]^2 \Leftrightarrow \text{SATURATION}$$

$$I_{SDP} = \frac{1}{2} \mu p C_o \omega \frac{W}{L} [(V_{SGP} - |V_{TP}|) V_{SDP} - \frac{V_{SD}^2}{2}]$$

\Rightarrow as $V_D \uparrow se$, Depletion region of n-p-nodiode will $\uparrow se$.



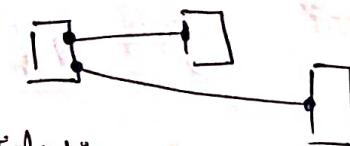
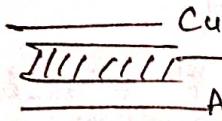
DIBL

2

$$V_T = V_{TO} - \eta V_{DS}$$



very low area

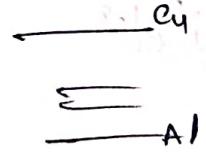


to nor get short

TSMC - 180nm \rightarrow 6 metal layers

metal 1
nearest
substrate

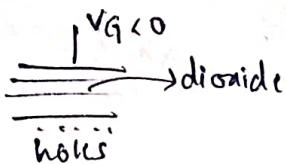
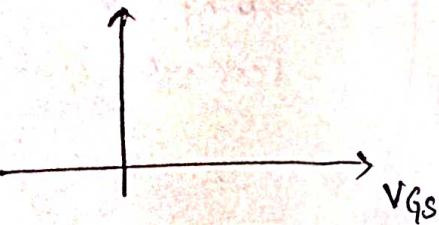
metal 6
highest
subst



These two metals
shows some
capacitance

\therefore parasitics will
be there.

(Gate)² cap



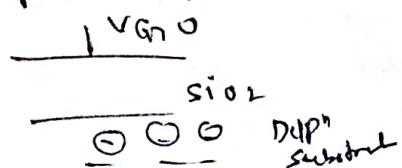
Accumulation

\therefore acts like capacitor

Cox.(WL)

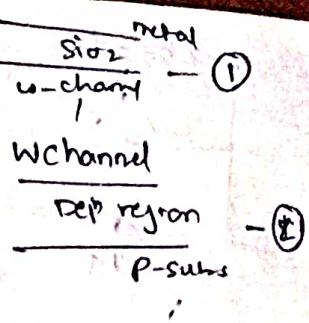
Cox \Rightarrow gate/Area

as $V_G \uparrow 0 \rightarrow$ Depletion happens



if $V_{GS} > V_{th}$ → some ϵ from the region will flow

Weak channel forms



L_{Cox}

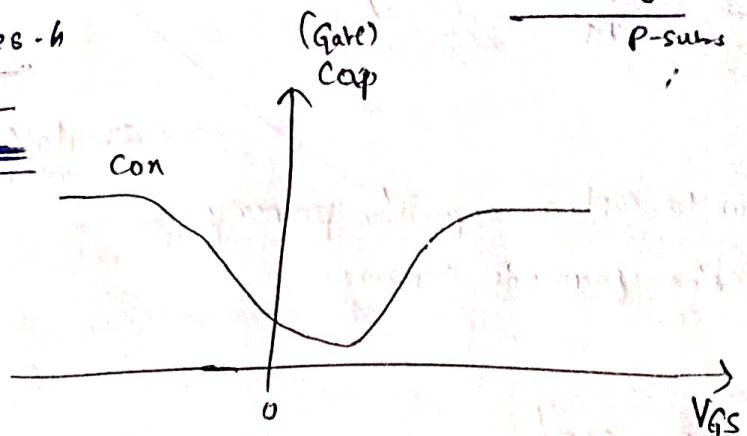
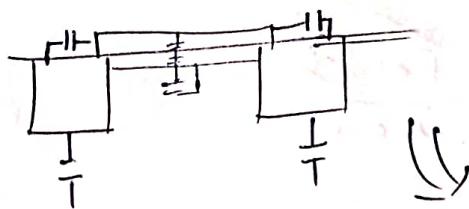
T_{cdep}

Both will be in series-h



Con

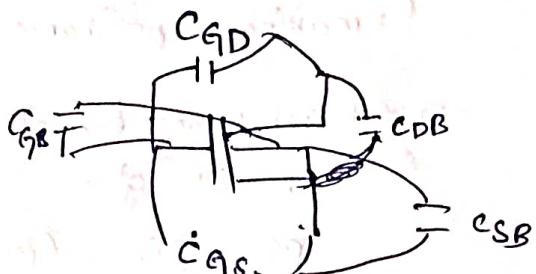
(Gate) Cap



* Again I_{DS} because of Strong Inversion.

other:

Based on region of open:



→ cutoff → channel Not formed ($V_{GS} < V_{th}$)

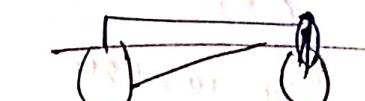
$$C_{GB} = \frac{1}{w} C_{ov}$$

$$C_{GS} = C_{GD} \\ \downarrow \quad \downarrow \\ W \cdot C_{ov} \quad W \cdot C_{ov}$$

$C_{ov} = \frac{\text{Capacitance}}{\text{Length}}$

ON:

$(V_{GS} > V_{th})$ Saturation →



↪ pinch off will happen

Near Drain due to pinchoff no capacitance

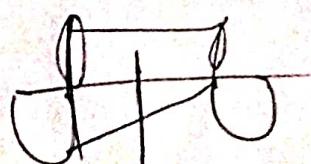
& only cap is from overlap

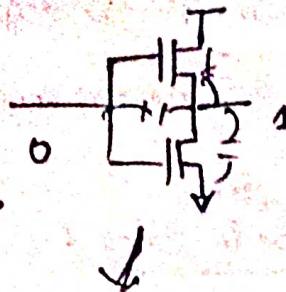
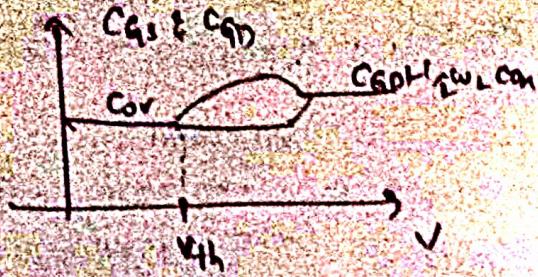
$$C_{GD} = w C_{ov}$$

$$C_{GS} = w C_{ov} + \frac{1}{2} w L \cdot C_{ov}$$

Linear Mode

$$C_{GS} = C_{GD} = w C_{ov} + \frac{1}{2} w L C_{ov}$$

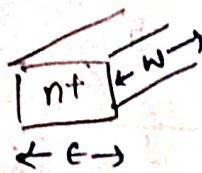




all capacitances
→ they will charge
the capacitor will
take time to
charge/discharge.

How to capture capacitor property:
→ Define parasitic capacitors

Simulation results



$$C_{jsw} = \text{cap/length}$$

side wall
Capacitor

→ All walls,

↳ making capacitance with p-substrates.

To not get wrong from all this

we will give

PS, PD

(perimeter of source, perimeter of drain)

$$\Rightarrow 2(\epsilon + W)$$

TSMC - 180nm

✓

Scale factor = λ

they design circuits with
dimensions of multiples of

this λ .

like: $L=2\lambda$

① Get current Area

$$AS, AD = EW$$

$$\Rightarrow EW$$

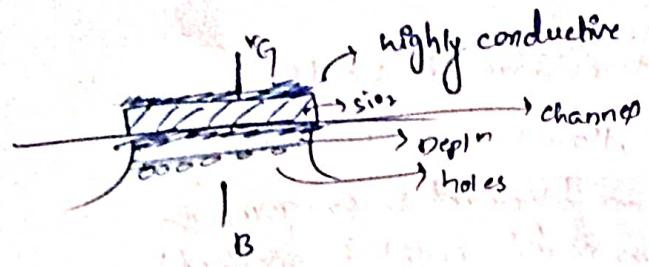
Design Rule
Checker.n

$$\epsilon = 5\lambda$$

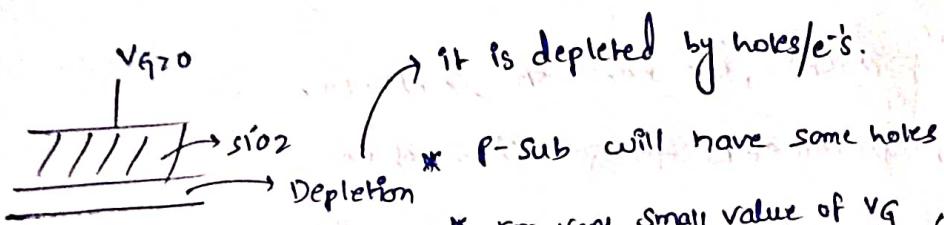
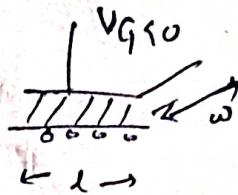
$$PD = 10\lambda + 2W$$

Recap:

10-8-24

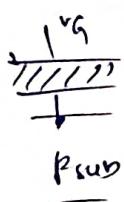


(i) $V_G < 0$

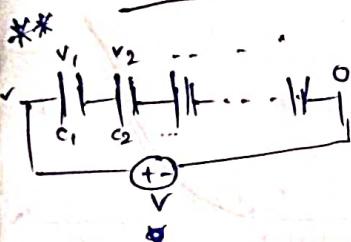


* P-sub will have some holes

* for very small value of V_G , we have very few e's coming from source to drain.



$\frac{1}{T} \text{ Con}$ \Rightarrow if we keep fixing V_G , the channel will form.
 $\frac{1}{T} C_{\text{dep}}$



$$\rightarrow Q = C(V - V_1)$$

$$\Rightarrow V - V_1 = \frac{Q}{C_1}$$

$$V_1 - V_2 = \frac{Q}{C_2}$$

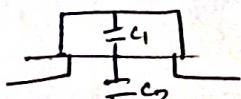
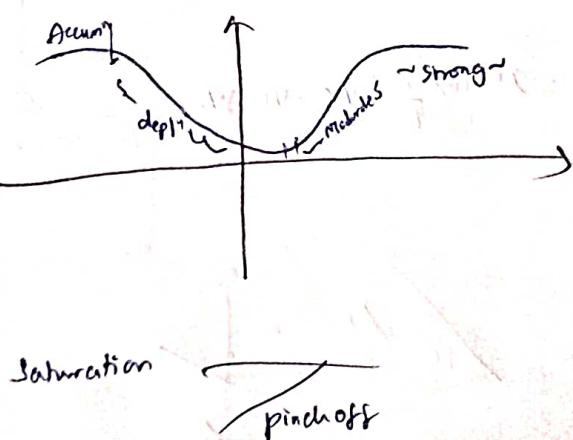
$$V_{n-1} - V_n = \frac{Q}{C_n}$$

$$\frac{Q}{\theta} = C \cdot \frac{\theta}{V} \quad Q = CV$$

$$\therefore \frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \dots + \frac{1}{C_n}$$

if you have higher V_G , channel

No C_{dep} \times acts as Insulator

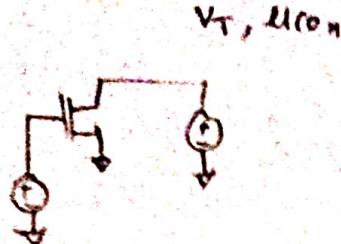


	cutoff	linear	saturation
C_{GB}	(WL) Con	0	0
C_{GS}	\rightarrow WL.Cov	\rightarrow WL.Cov	\rightarrow WL.Cov + $\frac{1}{2}$ WL.Cov
C_{GD}	\rightarrow WL.Cov	"	\rightarrow WL.Cov

entire channel
charge on it
acts as a plate of cap



Parameter Extraction for Mosfet:



TSMC
180nm → 05 nm

→ Behavior of transistors will be diff.

How our simulator, How its different to standard?

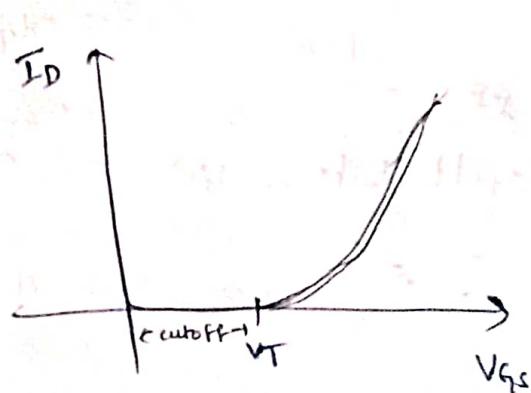
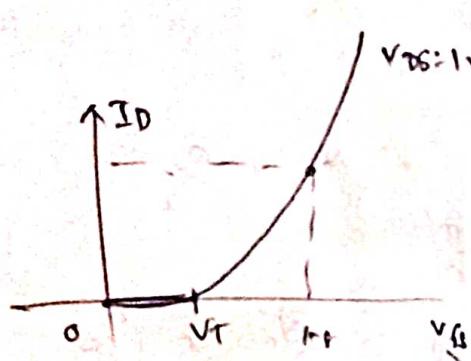
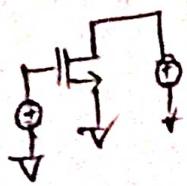
* Mosfet parameters are determined in 2x: TSMC 180
we will get some model (which is specified)

→ To explain physical behaviour of mosfet, we need V_T , λ , μC_m ...

* TSMC-180 gives lots of parameters to get idea of mosfet

PDK - process Design Kit

↳ which includes, All models & BJT model files, mosfet etc.



$$I_{DS} = \frac{1}{2} \mu C_m \frac{W}{L} (V_{GS} - V_T)^2$$

(SATURATION)

$$I_{DS} = \mu C_m \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

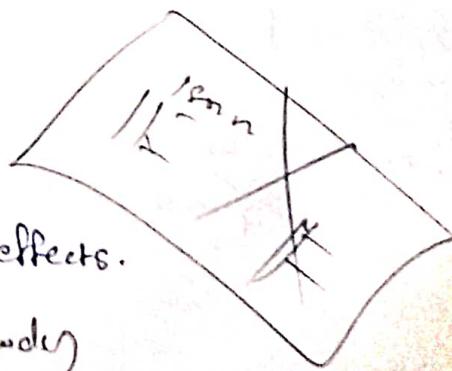
(LINEAR)

In satn:

↳ lot of 2nd order effects will have

- ✓ CLM
- ✓ pinch
- ✓ velocity saturation

$$I_{DS} = \mu C_m \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

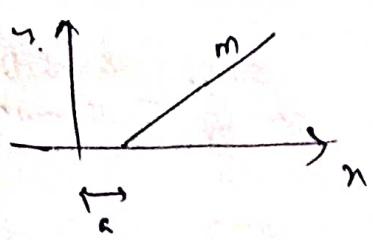


→ ~~for extracting~~

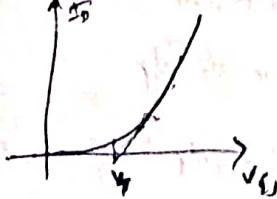
→ ∴ We take In the linear Mode, less 2nd order effects.

∴ we will use this I_{DS} eqn (only of linear mode)

$$Y = m(X - a)$$



$$\therefore a = v_T$$



$$\uparrow \frac{\partial I_D}{\partial V_{GS}} = \mu_{ON} \left(\frac{W}{L} V_{DS} \right)$$

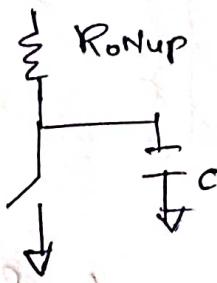
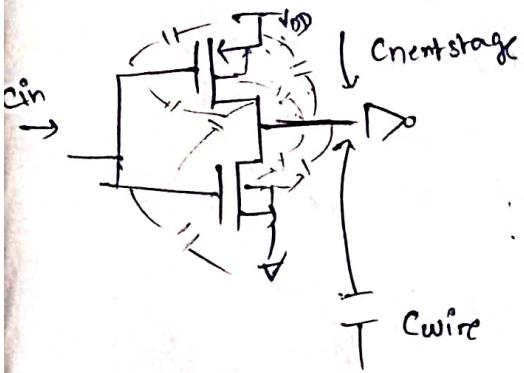
When mobility is high..?

∴

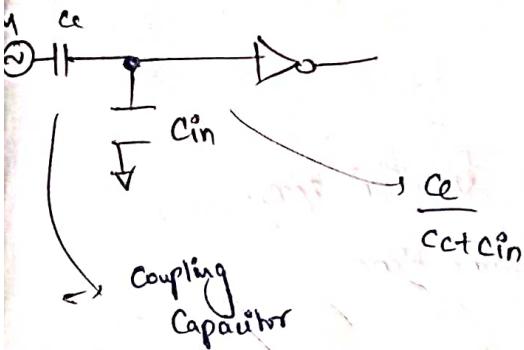
as $\frac{\partial I_D}{\partial V_{GS}}$ is high, mobility is higher.

↳ When 2nd order effects are low
↳ Means: Linear Mode ✓

CMOS Static Logic:

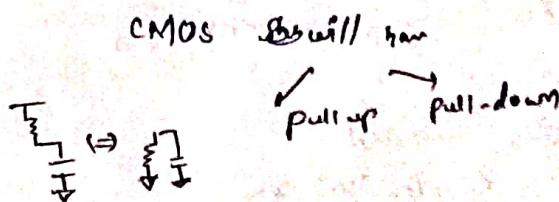
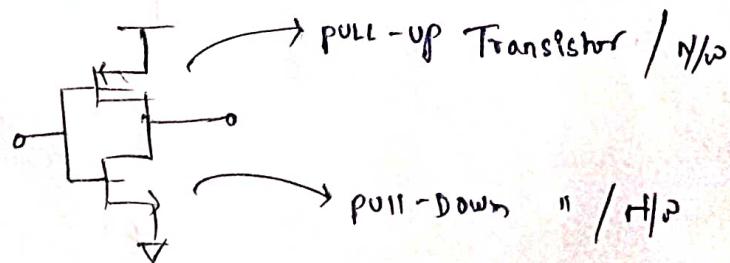


$$* \text{Centstage} = C_{GSNT} + C_{GSP} + C_{GDP} + \dots$$



if $C_C = C_{in}$
our signal will become
 $\frac{1}{2}$ of V_{DD}

→ For AC signal, supply acts as an AC ground,
 V_{DD}



CMOS will have

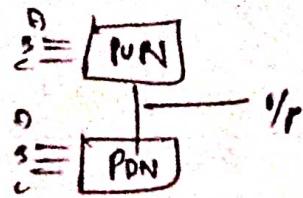
- pull up + down
- Evaluation of o/p

→ Drive the o/p is '0' or '1'.

→ Efficacy - How far

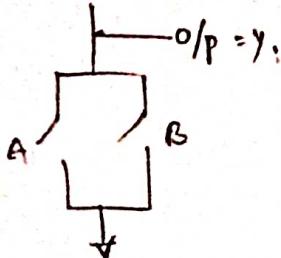
[Ability to get desired output]

Deion — Greenish brown



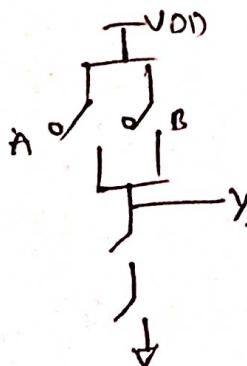
V_{DD}

B_2



A	B	y_1
0	0	1
0	1	0
1	0	0
1	1	0

$\overline{A+B} \Rightarrow \text{NOR gate}$



A	B	y_2
0	0	1
0	1	1
1	0	1
1	1	0

$\overline{AB} \Rightarrow \text{NAND gate}$

* CMOS logic will have a direct connect either with V_{DD} (or) zero.

* pull-up & pull-down network doesn't on at the same time.

Q i.e., either V_{DD} (or) "Gnd" will get on,

Static power consumption = 0

Static current = 0

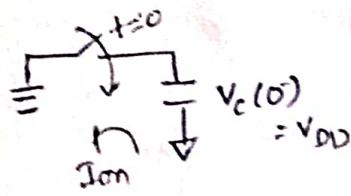
when either connected

to V_{DD} (or) gnd

(only to one,

deriv () → takes derivative w.r.t time.

Inty 10 μ ?
Faster vs slow

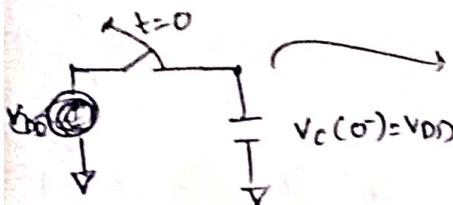


$$Q = CV$$

$$I_{ON} \cdot t = CV$$

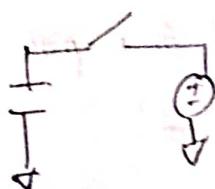
$$t = \frac{CV}{I_{ON}}$$

* Tsiividis



This node should hold voltage (Ideally)

↳ but due to some leakage

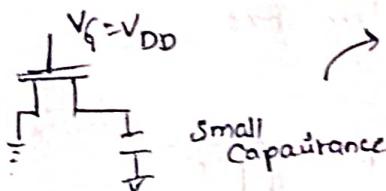


$$Q = CV$$

$$\frac{Q}{2} = \frac{CV}{2}$$

$$I_{OFF} \cdot t_{hold} = \frac{CV}{2}$$

$$t_{hold} = \frac{CV}{2I_{OFF}}$$



if Mosfer = ON,

the voltage on in capacitor will decrease due to loss, eventually to zero.



$$\text{at } t=0 \quad V_c(0) = 0$$

if switch is on

↳ current will flow & capacitor will charge

if capacitor charges to $V_{DD} - V_T$

↳ what will happen?

if happens after this ~~process will stop~~
NMOS will turn off. II

When we are trying to pass high voltage logic using n-mos then our out will only charge until

$$V_{DD} - V_T . II$$

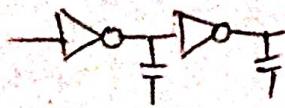
∴ NMOS is not good logic

for passing high logic

∴ our inverter



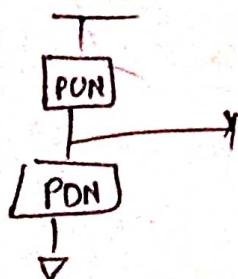
\Rightarrow if we T_{SR} width, C_{SR} , current also T_{SR}



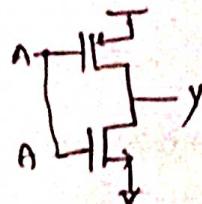
\Rightarrow if T_{SR} in current dominates T_{SR} in cap \Rightarrow then delay will reduced.

Both cap \propto current T_{SR} equally / nearly. \hookrightarrow No use now

* CMOS static logic:



Simple ex:



PUN \rightarrow made up of PMOS PDN \rightarrow made of NMOS

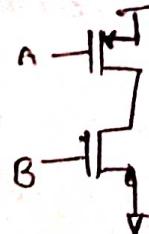
Ex: $y = f(\bar{A}, \bar{B}, \dots)$

Ex: $\bar{A} \cdot \bar{B}$

"•" \rightarrow series combn of transistors

Ex: $y = \bar{A} + \bar{B}$

$= \bar{A} \cdot \bar{B}$



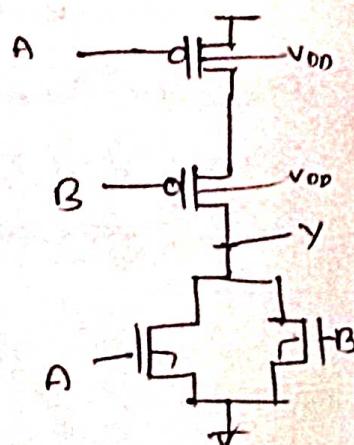
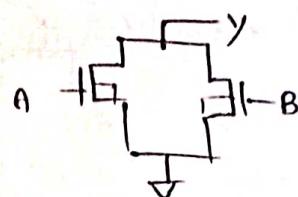
PUN

$\bar{A} + \bar{B}$

"+" \rightarrow parallel combn of transistors

Ex: $\bar{Y} = A + B$

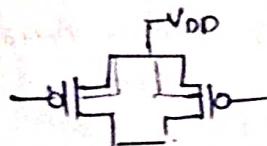
PDN



NOR funcn:

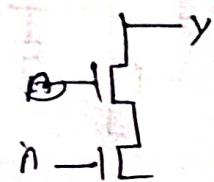
$$\text{Ex: } Y = \bar{A}B$$

$$\text{PUN} \Rightarrow Y = \bar{A} + \bar{B}$$



\Rightarrow Overall

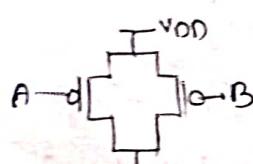
$$\text{PDN} \Rightarrow \bar{Y} = AB$$



$$\text{Ex: } Y = \overline{AB + CD}$$

$$\text{PUN} \Rightarrow Y = f(\bar{A}, \bar{B}, \dots)$$

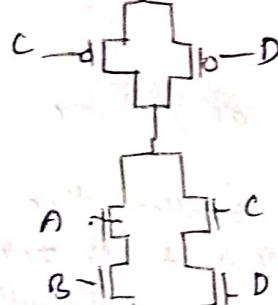
$$Y = (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D})$$



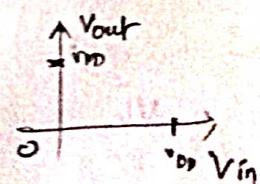
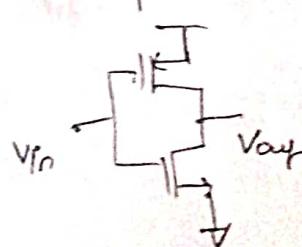
\Rightarrow CMOS Inverter (Rabueys)

$$\text{PDN} = \bar{Y} = f(A, B, \dots)$$

$$\bar{Y} = AB + CD$$



- Transfer characteristics
- Noise Margin
- Dynamic char (Rise/Fall/Delay)
- Design flow
- Trade-offs (P, A, speed)



How is the path??

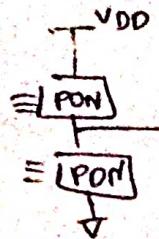
↳ find current mode of Mosfet

↳ find current eqns & equate them

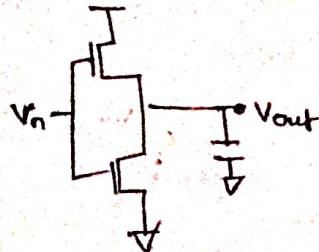
↳ solve for V_{out}

17-8-24

Recap:



e.g. CMOS Inverter



Static characteristic

Also called voltage-Transfer characteristic (VTC)

Sweep V_{in} from 0 to V_{DD}
(all we can)

$$V_{DS} > V_{GS} - V_{th} \text{ (for NMOS)}$$

\therefore After V_{th}
NMOS turns on



* NMOS \rightarrow into Saturation Mode

After some time

After the decreasing in value
PMOS also goes to saturation.

\therefore both saturation.

\therefore the direct path from V_{DD} & V .

When
 $V_{in} = V_{DD} - |V_{tp}|$

\swarrow
Then it turns off
(PMOS)

if we further give V_{in} ,

Mn will try to move towards
Linear/Throne region

as $V_{in} \uparrow$

$$V_{GS} - V_{th} > V_{DS} \text{ (becoming)}$$

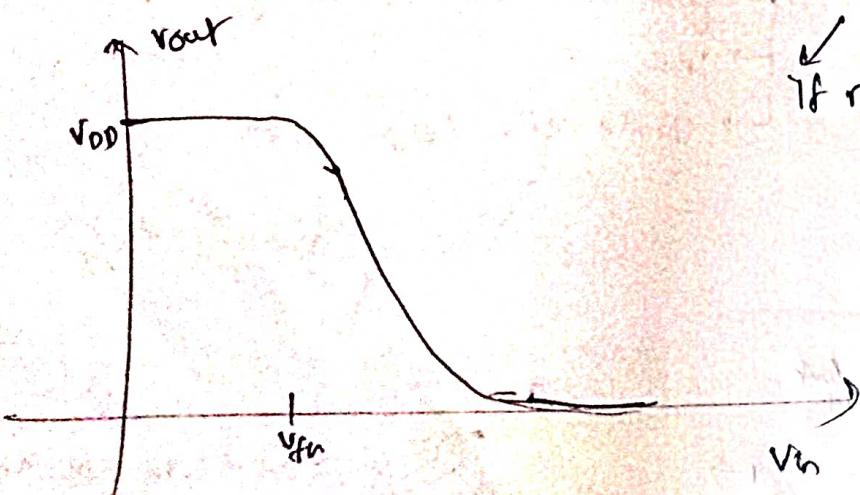
(prob is higher)

\swarrow
as it goes to linear

It will act as resistor.

\swarrow
If resistance R is smaller, then
 V_{out} to get zero

$$\text{as } R \rightarrow \infty \quad IR = 0 \quad \therefore$$



whenever transistors are in ON mode, the current flowing through both of them is same.
but V_{GS} is different in pmos & nmos.

as your $V_{GS} \propto I_{DS}$ with V_{DS} , I_{DS} also $\propto I_{DS}$

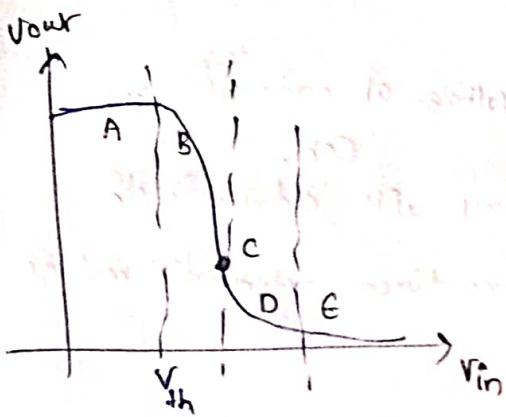
for cmos inverter

if input is very small, let = 0

$$\text{For } V_{in} = 0, \quad V_{SGP} = V_{DD} - 0 \\ = V_{DD}$$

$$V_{SDP} = 0$$

$$V_{DD} - V_{SDP} = V_{DSN}$$



A-zone:

pmos will be in linear mode,
nmos in cutoff mode

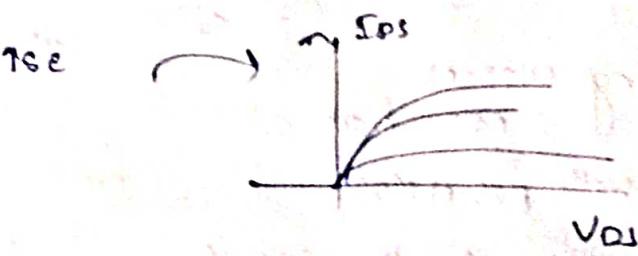
$$0 < V_{in} < V_{th}$$

$$V_{out} = V_{DD}$$

C-point:

$$V_{in} = V_{DD}/2 \quad \& \quad V_{out} = V_{DD}/2$$

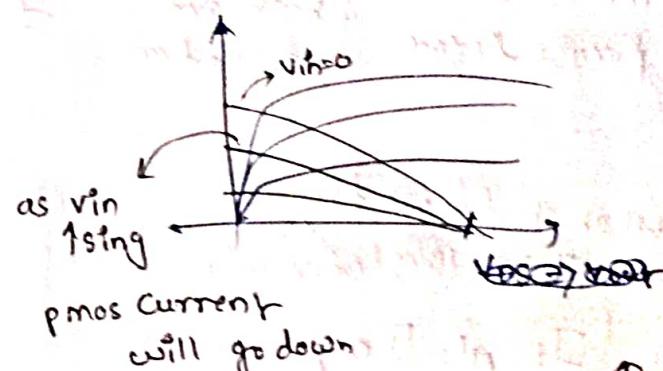
Both are in saturation mode



for linear region \rightarrow $I_{DS} \propto V_{DS}$

\therefore Hence it will be in linear mode

Good amount of current
will flow.



as V_{in} rising
pmos current
will go down

at Nmos current will go up. \uparrow

Intersecting point

$$\Rightarrow V_{DS} = V_{out}$$

B-zone

Np is in linear mode.

Mn is in saturation mode

$$V_{in} > V_{th}$$

$$V_{out} > V_{DD}/2$$

D-zone:

pmos remains in saturation

$V_{SG} \propto I_{DS}$ a lot

nmos in linear mode

$$V_{in} > V_{DD}/2$$

$$V_{in} < V_{DD}/2$$

$$V_{out} < \frac{V_{DD}}{2}$$

E zone:

$M_P \rightarrow$ cutoff

$M_N \rightarrow$ linear

~~$V_{DD} - |V_{TP}| < V_{in} < V_{DD}$~~

* Equating current eqn from both p & n mos

$$V_{out} \rightarrow 0$$

will give the curve of transfer characteristics

* E & A zone \Rightarrow current flowing is zero, $I=0$

B \rightarrow N mos saturation
P mos linear } both are turned on } a path b/w V_{DD} & ground

if we applied V_{in} for some time

the current will set to some value

\therefore The voltage at node also get set.

V_{out} will adjust itself

where these currents will matched

$$|I_{DSN}| = |I_{DSP}|$$

(in saturation) (linear)

$$\frac{k_n}{2} (V_I - V_{TN})^2 = k_p [(V_I - V_{TP})] V$$

$$k_p \left[(V_{DD} - V_I - |V_{TP}|)(V_{DD} - V_O) - \frac{1}{2} (V_{DD} - V_O)^2 \right]$$

→ Ignoring channel length Modulation (Here)

V_I is such that it is in B-zone.

$$V_O = (V_I + |V_{TP}|) \mp \sqrt{(V_{DD} - V_I - |V_{TP}|)(V_{DD} - 2V_I + V_{TN} - |V_{TP}|)}$$

-ve sign discarded

↳ reason..?

Here +ve only

$$V_{DD} - |V_{Tn}| - |V_{Tp}| > 0 \Rightarrow V_{DD} > V_{Tn} + |V_{Tp}|$$

$$V_{DD} - 2V_{In} + V_{Tn} - |V_{Tp}| > 0$$

Assumed

$$V_{Tn} = |V_{Tp}|$$

$$\therefore V_{In} < \frac{V_{DD}}{2}$$

why cancelled..?

cond'n satisfies

only for
both () ()

root under always true

\therefore both () () should be +ve. h

* If we take -ve () ()

then $V_{In} > \frac{V_{DD}}{2}$ will come

\therefore But our graph says wrong. h

\therefore taking -ve is X

$$\Rightarrow \mu_n k_N \left(\frac{W}{L} \right)_N = \mu_p k_P \left(\frac{W}{L} \right)_P$$

Assumed **

for all these calculations. h

Both in Saturation:

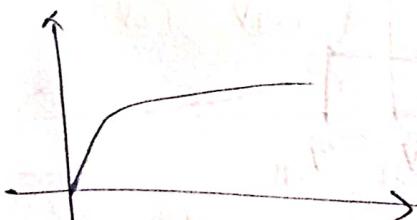
$$\text{then, } (I_{DS})_p = (I_{DS})_n \\ (\text{sat}) \quad (\text{sat})$$

$$k_n (V_I - V_{Tn})^2 = k_p (V_{DD} - V_I - |V_{Tp}|)^2$$

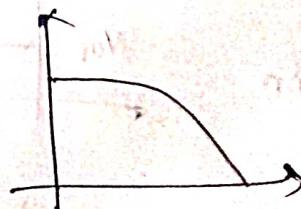
$$V_I = V_{DD} + \sqrt{\frac{k_n}{k_p} |V_{Tn} - |V_{Tp}||} \\ \left(1 + \sqrt{\frac{k_n}{k_p}} \right)$$

$$\text{if } \frac{k_n}{k_p} = 1, \quad ** \\ V_I = \left(\frac{V_{DD}}{2} \right)$$

zone our input should be bounded b/w two points. h

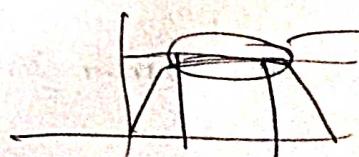


NMOS



PMOS

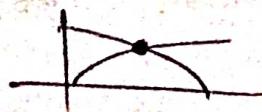
Drain current characteristic



output will like in b/w

both are in saturation. h
(overlapping)

In reality, the current will not be const / Some slope will be there,
for given voltage, we have defined (specific) V_{out} .



single point (slope is there)

$$V_{DSN} \geq V_{GSN} - V_{TN}$$

PMOS

$$V_{SDP} \geq V_{GSP} - |V_{TP}|$$

$$\boxed{V_{out} \geq V_{IN} - V_{TN}}$$

$$V_{DD} - V_{out} \geq V_{DD} - V_{IN} - |V_{TP}|$$

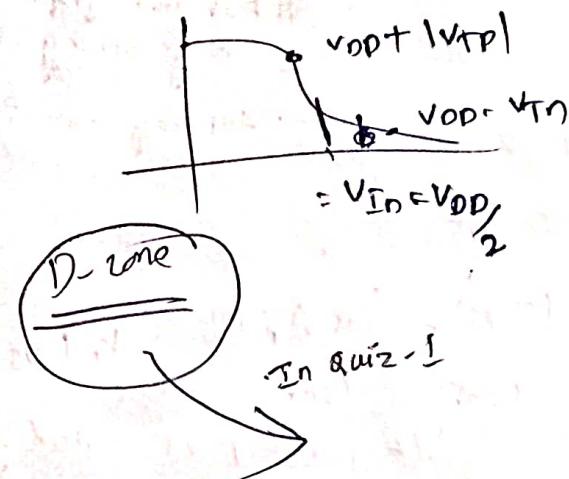
↓

$$\boxed{V_{out} \leq V_{IN} + |V_{TP}|}$$

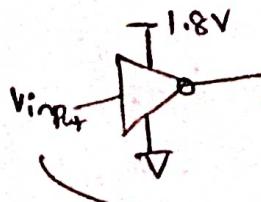
* Both transistors are in saturation;

For $k_n = k_p$, $V_{GIn} \approx V_{DD}/2$

$$V_{DD} + |V_{TP}| \leq V_{out} \leq V_{DD} - V_{TN}$$



Noise Margin:



$$\boxed{V_{out} = \overline{V_{in}}}$$

$V_{IN} = 0V$

$$[0, 1.6]$$

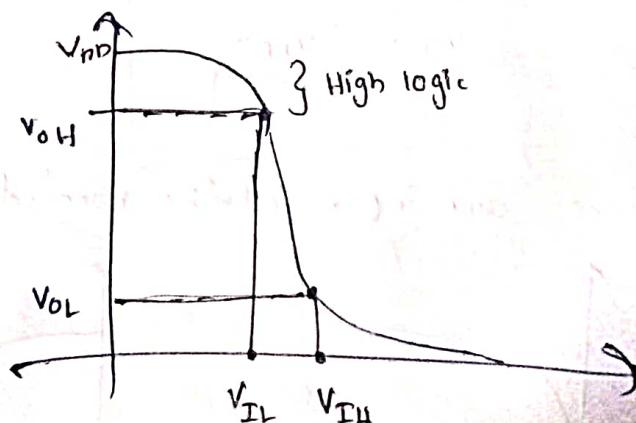
V_{in} : 0 → low 1.6 → high

$$V_{out} \quad 1.8V \quad 0V$$

V_{out} depends upon V_{DD}

$$\Rightarrow V_{in} = 1.2V$$

we don't know
∴ we need characteristic



V_{OH} = min output as high

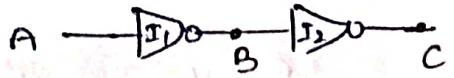
V_{OL} = max input as low

V_{IH} = max value of input (low)

to get output high

$V_{IH} \rightarrow \min$ (high input) to get low output.

V_{OH} V_{IH}
 ~~\oplus~~ V_{OL} V_{IL}



I_1 Low High
 $V_{In} < V_{IL}$ $V_B > \ominus V_{OH}$

$V_B > V_{OH}$

If some V_{OH} phase due to
Some noise

I_2 :

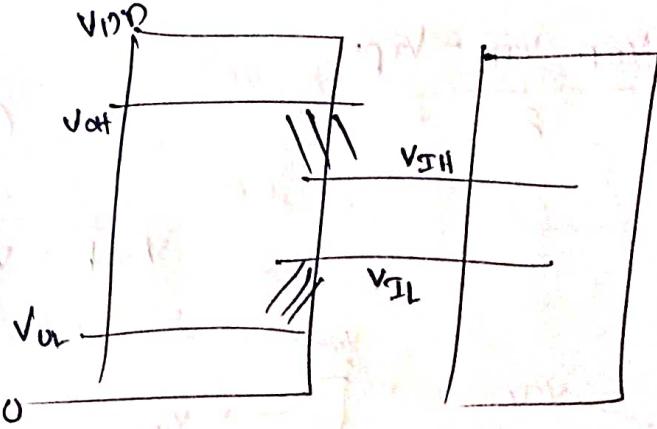
V_B will be
high

$V_B \gg V_{IH}$

Let $V_{OH} = 1.5$

then it becomes 1.45

$V_{IH} = 1.3$ Something
~~Something~~



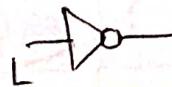
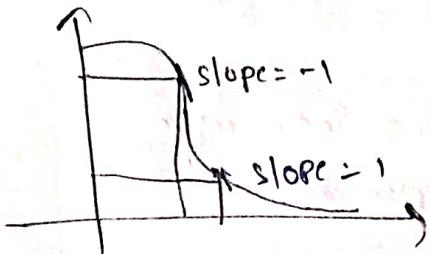
NM_L NM_H



$V_{IL} - V_{OL}$

$V_{O^P} - V_{IH}$

How to find ~~\oplus~~ NM_L & NM_H ?



$0 - 0.3V$

$$\left| \frac{\partial V_O}{\partial V_{IN}} \right| > 1$$

Where our gain ≤ 1 ?

from V_O vs V_I^P curve

where Slope = 1 (magnitude)

beyond it has high slope

before slope = 1 and after we need to operate digital system

P (V_{I1}, V_{OH}) mode of opamp at these two points we need to know -

Q (V_{I2}, V_{OL})

P (V_{IL}, V_{OH}) \Rightarrow Mn saturation

Mp linear mode

Q (point)

Equate current

$$\frac{k_n}{2}(V_I - V_{Tn})^2 = k_p [(V_{DD} - V_I + V_{Tp})(V_{DD} - V_O)]$$

$$V_{TH} = \frac{5V_{DD} + 3V_{Tn} - 8|V_{Tp}|}{8}$$

$$\frac{\partial V_O}{\partial V_{in}} = -1$$

$$V_{OL} = \frac{V_{DD} - |V_{Tn}| - |V_{Tp}|}{8}$$

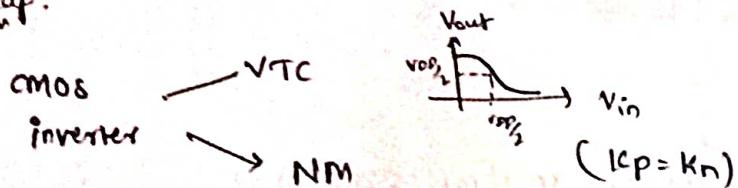
if we do this,

$$V_I = V_{I1} = \frac{3V_{DD} + 5V_{Tn} - 3|V_{Tp}|}{8}$$

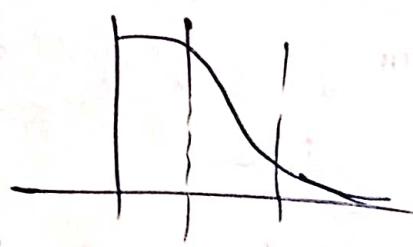
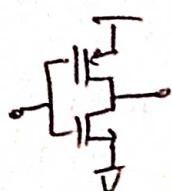
(our assumption $\Rightarrow k_n = k_p$)

21-08-24

Recap:



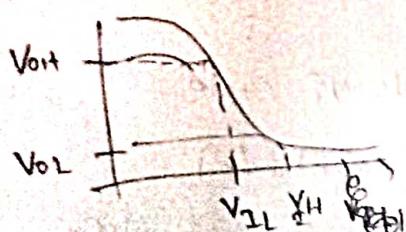
$$V_{out} = V_{OH} = \frac{7V_{DD} + V_{TN} + |V_{Tp}|}{8}$$



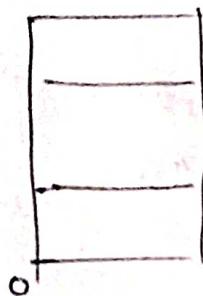
$$\therefore \left| \frac{\partial V_O}{\partial V_{in}} \right| < 1$$

we don't want to get in this region
of amplification

we will like one working
to work.



$$V_{DD} = 1.8 \text{ V}$$



V_{OH} → min output level
considered as high

V_{OL} → max voltage level
considered as low



⇒ we want high at B. &

∴ we are expecting low at C.

$$\textcircled{2} \rightarrow V_{IH} = 1.5$$

Our $V_{OH(1)} > V_{IH(2)}$

$$B = 1.6 \text{ V} = V_{DH} (\text{A}(1))$$

$$NM_{H1} = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

→ Ideally, We Want Higher Noise Margin.

Ideal characteristic

(1) boundaries defined by slopes ±1

At these two points.

We know state of condition

P ✓

Q ↘

$N_{MOS} \rightarrow lin$
 $P_{MOS} \rightarrow sat$

V_o funcn of V_{in}

$$I_{dsat} = I_{dp} I_{in}$$

$$\frac{\partial V_o}{\partial V_{in}} = -1$$

V_o as funcn of

$$\frac{\partial V_o}{\partial V_{in}} = -1$$

Q point,

what (V_{in} , V_{out})

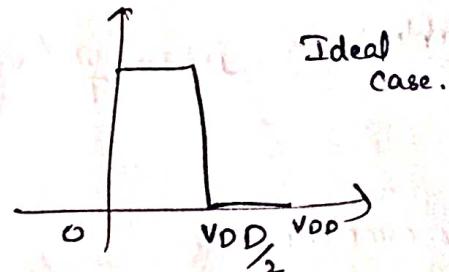
⇒ P-point

After doing this:

$$NM_H = \frac{V_{DD} - V_{th,n} + 3|V_{TP}|}{4}$$

$$NM_L = \frac{V_{DD} + 3V_{th,n} - |V_{TP}|}{4}$$

$$\text{if } V_{th,n} = |V_{TP}| \quad \Rightarrow \quad \approx \frac{V_{DD} + 2V_T}{4}$$



$$\frac{V_{DD} + 2V_T}{4}$$

$\rightarrow V_{DD}$

\rightarrow more power consumption

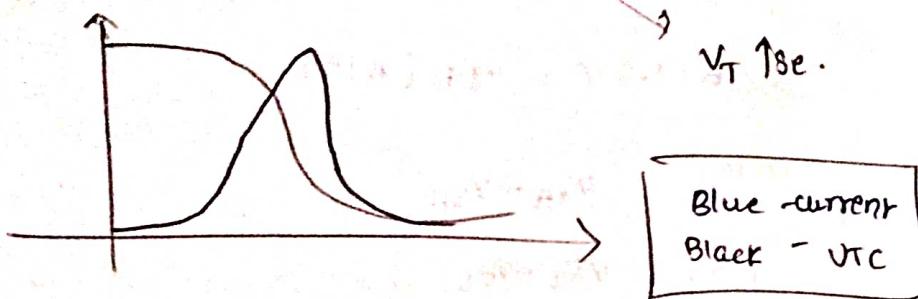
Which type of power is

1 PUN & 1 PDN

\Rightarrow Both turn on
in characteristic.
Then only at that interval
current flows.

Prblm: \Rightarrow Dynamic / switching power will \uparrow sc

What is static power?



$\Rightarrow V_T \uparrow$ sc
Use Higher V_T devices

Prblm:

$$I = \mu n C_o \omega \frac{W}{L} (V_{GS} - V_{Th})^2$$

Current will \downarrow sc

*** \Rightarrow Due to decrease in current
slower time to charge and discharge
Speed \downarrow sc

Can u comment

what happening \uparrow if scaling
technology?

\rightarrow fabricate more no. of transis

\rightarrow size of trans \downarrow sc

How noise margin trading off with technology?

- \hookrightarrow supply reducing using as tech \downarrow sc
- \hookrightarrow $V_T \downarrow$ sc (also)
- \hookrightarrow Noise margin \downarrow sc (also)

More trans in chip

\hookrightarrow more switching \rightarrow more switching noise \rightarrow noise margin

\Rightarrow

~~comes from~~ Dynamic characteristics
will use proper engineering approximations.

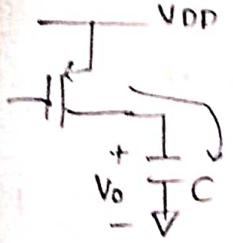


Assumption:

Either time of charging or discharging only happens

→ only one of Mosfet is ON at a time. //

Rise-time: $M_P \rightarrow \text{ON}$; $M_N \rightarrow \text{OFF}$



$t_r \Rightarrow$ time taken to charge output from 0 to V_{OH}

(And input given = V_{IL})

* Why not 0 to V_{DD} ?

* Takes time ∞ to charge from V_{DD}

→ reach steady state after ∞ time (RC circuit)

I_D of pmos is flowing in capacitor.

↳ (source to drain)

If no external load

= Cgd of pmos & Cgd of nmos



If given some Load

C_L

$C_L + \text{parasitic capacitors}$

Now, nmos is off and pmos is on.

* initial voltage of Cap = 0 V. //

∴ PMOS will be in

↳ SATURATION MODE

$$V_{SDP} > V_{SGP} - |V_{tp}|$$

$$V_{DD} > V_{SL} - |V_{tp}|$$

↳ SATURATION MODE. //

→ When it will be off of SATURATION

(goes to linear)

$$V_{SPP} \leq V_{SGP} - |V_{TP}| \quad , \quad \therefore \text{Till } (V_{IL} = V_{in})$$

$$-V_{DP} \leq -V_{GP} - V_{th}$$

$$\boxed{V_{DP} \geq V_G + V_T}$$

$$= V_m + V_P$$

Now

$$\overbrace{V_{DD} - V_0}^{\text{sr}} > V_{DD} + V_{IL} + |V_{TP}|$$

$$\boxed{V_0 \leq V_D + V_{TP}}$$

* Till $\boxed{V_{IL} + V_{TP}} = V_D$, the pmos will

be in saturation mode

after, $V_D > V_{IL} + V_{TP} \rightarrow$ Then turns into linear mode.

dynamic + static min

$$\int_0^{t_r} \frac{dt}{C} = \int_0^{V_{out}} \frac{C \cdot dv_o}{I_{DP}}$$

$$= C \cdot \left[\int_0^{V_{IL} + |V_{TP}|} \frac{dv_o}{I_{DP, \text{sat}}} + \int_{V_{IL} + |V_{TP}|}^{V_{DH}} \frac{dv_o}{I_{DP, \text{lin}}} \right]$$

Similar in saturation



$$\text{Voltage } c = v = \frac{1}{C} \int idt$$

$$= \frac{it}{C} \rightarrow \text{linearly rising}$$

Linear mode:

as v_o rising, I_d rising (in linear)

(similar to exponential (non-linear) discharging.)

$$I_{DP, \text{sat}} = \frac{1}{2} \mu_p \text{const}_L \left((V_{DD} - V_{IL} - |V_{TP}|) \right)^2 = \text{const wrt to } v_o$$

$$I_{DP, \text{lin}} = \mu_p \text{const}_L \left[(V_{DD} - V_{IL} - |V_{TP}|)(V_{DP} - v_o) - \frac{(V_{DD} - v_o)^2}{2} \right]$$

~~K [sp (a-p)]~~

$$\tau_{rise} = \frac{2(V_{IL} + |V_{TP}|)}{(V_{DD} - V_{IL} - |V_{TP}|)^2}$$

$$+ \frac{1}{(V_{DD} - V_{IL} - |V_{TP}|)} \ln \left[\frac{V_{DD} + V_{OH} - 2V_{IL} - 2|V_{TP}|}{V_{DD} - V_{OH}} \right]$$

$\tau = \frac{Cdv}{dr} = \frac{dt}{C} = \frac{dv}{\frac{dt}{C}}$

$V_{DS} > V_{GS} + V_T$ (nmos)

$V_{SP} > V_{SG} + V_{TP}$ (pmos)

$V_{DD} - V_D > V_{DD} - V_{IL} - |V_{TP}|$

or a Given Technology,

\hookrightarrow $k_p \cdot \gamma_{rise}$ is a const

$$k_p = \mu_p \cos \omega_L$$

$$k = \mu \cos \omega_L$$

C = Total capacitance at nos
inverter output.

$$\gamma = \tau_{rise}$$

$\rightarrow D_O$

\hookrightarrow nothing connected
it has C_{self}

$$= C_{DBP} + C_{DBN} + C_{gdp} + C_{gdN} = C_1$$

rise time

$$of inverter . \quad T_{\tau_1} = \frac{\text{const}}{k} \cdot C_1$$

if add extra load capacitance $C_{external}$

$$C_2 = C_{self} + C_{external}$$

$$C_2 > C_1$$

$$T_{\tau_2} = \frac{\text{const}}{k} \cdot C_2$$

$T_{\tau_2} > T_{\tau_1}$

\hookrightarrow more cap need to charge

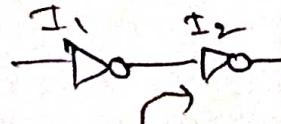
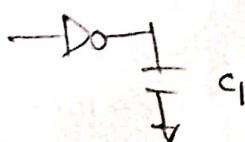
\hookrightarrow more time

If we want γ also be const then if C_{load} , k should \uparrow se,

$$= \mu \cos \frac{\omega}{L}$$

$\therefore \omega_L$ should \uparrow se.

Vocabulary
(Drift)



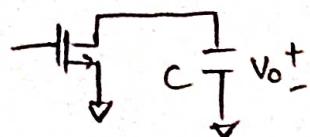
$C_{external} = \text{Load capacitance for } I_1$

$$C_{ext} = \underbrace{C_{gsn} + C_{gsp} + C_{gdn} + C_{gdp}}_{\text{from } T_2} + C_{self \text{ of } I_1}$$

$$= C_{gdp} + C_{gdn} + C_{gbp} + C_{bsn}$$

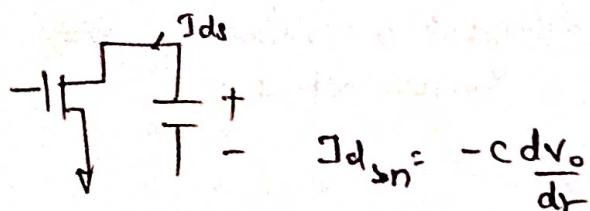
$$C_{ext} = \Sigma \text{ terms}$$

Fall-Time: $M_N \rightarrow ON$; $M_p \rightarrow OFF$



I_p is High = V_{IH}

Output: V_{DD} to V_{IL}



$\underline{\underline{T_m}}$: rise time from 0 to 0.9 V_H

derive ?
rise time eqn. n

$$\int \frac{dt}{C} = - \int_{V_{DD}}^{V_{OL}} \frac{dv_o}{I_{dsn}}$$

$$V_o > V_{IH} - V_T$$

(for saturation)

$$= - \left[\int_{V_{DD}}^{V_{IH}-V_{Tn}} \frac{dv_o}{I_{dsat}} + \int_{V_{IH}-V_{Tn}}^{V_{OL}} \frac{dv_o}{I_{dlinear}} \right]$$

$$\frac{k \cdot T_{fall}}{C} = \frac{2(V_{DD} - V_{IH} - V_{Tn})}{(V_{TH} - V_{Tn})^2} + \frac{1}{V_{IH} - V_{Tn}} \ln \left[\frac{2(V_{IH} - V_{Tn}) - V_{OL}}{V_{OL}} \right]$$

$\frac{T_{fall} \cdot k}{C}$ is also const [for specific technology]

$$\Rightarrow \frac{\tau \cdot k}{C} = \text{const} \Rightarrow \boxed{\tau \propto \frac{C}{k}} \Rightarrow \tau \propto \frac{C_{ext} + C_{self}}{k}$$

We know $K \propto \frac{W}{L}$, $C \propto W$

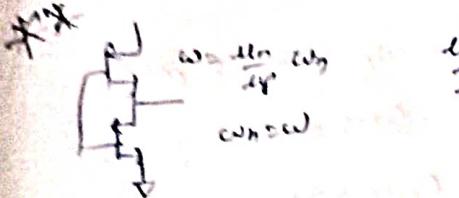
if $L = \text{const}$

$$K \propto W, C \propto W, \tau \propto \frac{C_{ext} + C_{self}}{C_{in}}$$

$$\gamma \propto \frac{c_{\text{ext}} + c_{\text{self}}}{C_{\text{in}}} = \frac{c_{\text{ext}}}{C_{\text{in}}} + \frac{c_{\text{self}}}{C_{\text{in}}} \quad \left\{ \begin{array}{l} C_{\text{ext}} \propto W \\ C_{\text{self}} \propto W \end{array} \right\} \text{Proportionality}$$

becomes const.

$$= \frac{c_{\text{ext}}}{C_{\text{in}}} + \text{const}$$



$$\frac{w}{C_{\text{in}}} + 2$$

$$W_n = W$$

$$W_p = \frac{w}{W_p} W_n \approx 2W$$

L is same $\propto H$

$$L = L_{\text{min}}$$

$$180 \text{ nm}$$

$618 \text{ nm} \propto H$
in 180 nm Tech

No extra load

applied input,
($2w, 2w$)

measure rise & fall
no driving load
same γ

Now $2w$ -sized inverter
($2w, 4w$)

Driving no load.

Same γ

c_{self} can be cancelled

\Rightarrow if c^{ext} rising, current also rising

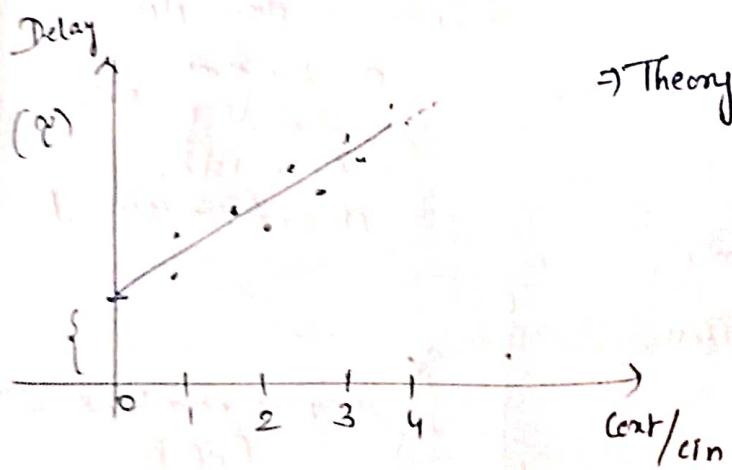
current \therefore remains const

[Intuitive]

\Rightarrow Theory suggest this

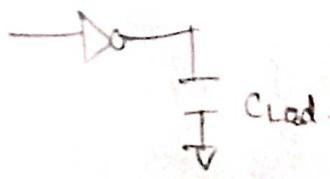
\hookrightarrow may not happen

\because practical. \hookrightarrow



$$\gamma = g \cdot \frac{c_{\text{ext}}}{C_{\text{in}}} + \beta \quad (\text{practical})$$

plotting



design inverter with this CL so that next achievable delays are small?

$$\gamma = g \cdot \frac{C_{\text{load}}}{C_{\text{in}}} + \beta = \frac{c_{\text{self}}}{C_{\text{in}}}$$

② γ should decrease.

$$\tau_L \uparrow = g_{\text{out}} \frac{C_{\text{ext}}}{C_{\text{in}} T_{\text{se}}} + \left(\frac{C_{\text{self}}}{C_{\text{in}}} \right) P$$

$\omega_L \uparrow \text{se} \Rightarrow I \uparrow \text{se} \Rightarrow \tau \uparrow \text{se}$

Here $\downarrow C_{\text{in}}$ will also $\uparrow \text{se} \Rightarrow$ as ω_L rises, C_{self} also $\uparrow \text{se}$

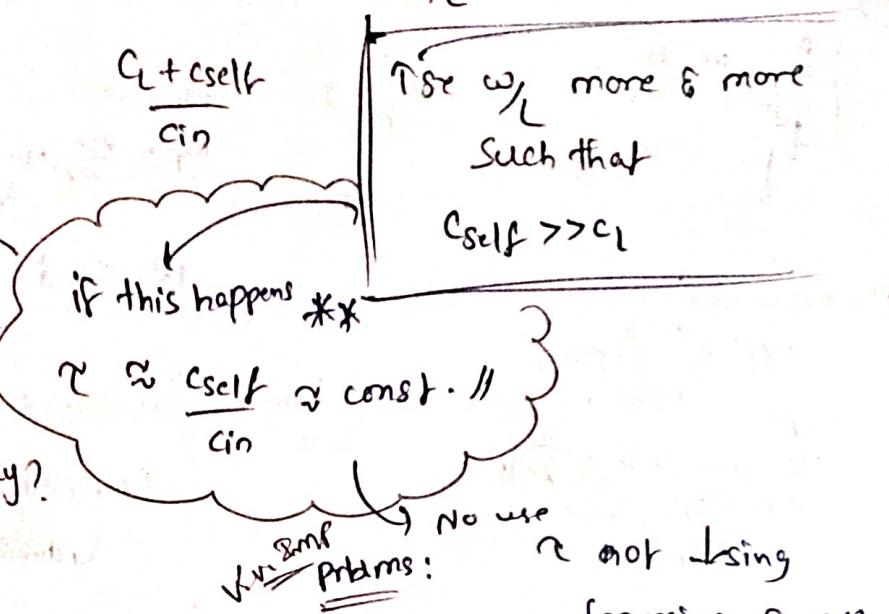
Delay will become
const. !!

Q. if we have very large $C_{\text{ext}} = C_L$

And want to have lower delay?

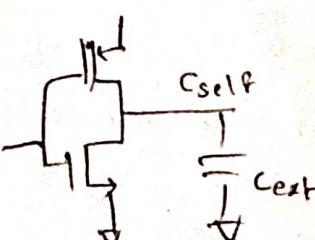
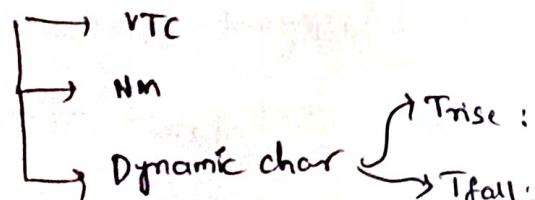
Cheat approach:

1 - big inverter
big load
n-Inverters stacked

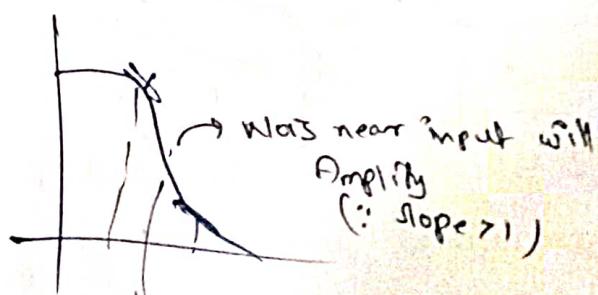


24-8-24

CMOS Inverter



1 - Ay cheat sheet
No simulation ques. !





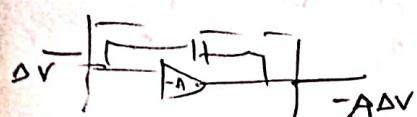
what is the relation
b/w cir 1 and
cir 2

$$c_1 \& c_2 \text{ with } c_1 \downarrow \text{ or } c_2 \downarrow$$



$$\Delta V_c = \Delta V - (-A\Delta V)$$

$$= \Delta V(1+A)$$



$$\Delta Q = C \cdot \Delta V(1+A)$$

if it considered as Black block
it drawing Charge $\Delta Q - h$

$$\therefore \text{Now } \frac{\Delta Q}{\Delta V} = C(1+A)$$

Showing equivalent capacitance of
 $C(1+A)$

* Miller Capacitance *

$$\therefore C_1 = C(1+A)$$

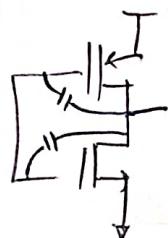
$$C_1 = (1+A)(C)$$

$$= \Delta V_c = \Delta V$$

$$\Delta Q_B = \Delta V_c C$$

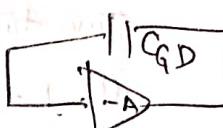
$$\frac{\Delta Q}{\Delta V} = C$$

$$\therefore C_2 = C$$



$\rightarrow C_{gdp}$ & C_{gdN} makes path
from input to output

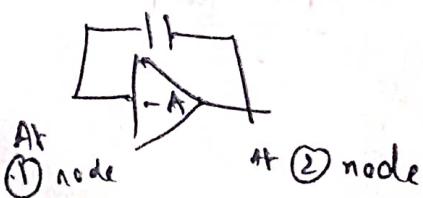
what is C_{gd} eff from C_{gdN} & C_{gdp}



$$C = (1+A) C_{GD}$$

if $A < 1$ $C \approx C_{GD}$

no gain from output to input



$$A > 1$$

At node ① $\Rightarrow C(1+A)$

At node ② $\approx C$

if $A_{ce} \approx 1$ then \therefore from node 0 $\approx (1+\alpha)C \approx C$

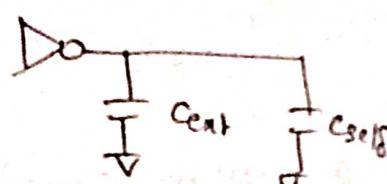
α is low loss 

From output side,

C_{self} of inverter?

$$C_{gdN} + C_{gdP} = W \cdot C_{OP}$$

$$\rightarrow \frac{KT}{C_{load}} \approx \text{const}$$



$$\tau \propto \frac{C_{out}}{K}$$

$$\therefore \tau \propto \frac{C_{out}}{C_{in}} = \frac{C_L + C_{self}}{C_{in}}$$

$$\tau \propto \frac{C_L}{C_{in}} + \frac{C_{self}}{C_{in}} \approx \text{const}$$

$$\boxed{\tau \propto \frac{C_L}{C_{in}} + C}$$

$$K = \alpha C_{in} W$$

also we know

$$C_{self} \propto W$$

$$C_{in} \propto W$$

$$DB_{N,P}$$

$$ED_{N,P}$$

$$K \propto C_{in} \\ (\text{as } C_{in} \propto W)$$

$$\therefore \frac{C_{self}}{C_{in}} = \text{const}$$

$$\boxed{\tau = g \frac{C_{load}}{C_{in}} + \text{const}}$$

$\Delta t = \text{prop delay}$



$$-D_o \frac{1}{\tau}$$

let delay = 50 pico sec

to reduce delay.

to reduce delay

$$\frac{KT}{C} \approx \text{const}$$

$T_D + t_{fse} \propto K t_{fse}$ (as $C = \text{const}$ external load)

$K t_{fse} \approx W / t_{fse}$ large value

Two types of delays

① L-H

② H-L

$$\overline{T}_{PH+HL}$$

overall delay

= Average of these two

$$\frac{T_{PH} + T_{HL}}{2}$$

due to $w \uparrow s_e$ C_{self} also $\uparrow s_e$

$$\gamma_{delay} = \text{const.} (\text{const low number})$$

\therefore We can't $\uparrow s_e$ transistor size (as we current)

(\hookrightarrow) this may get problem to previous stage loading effect & delays.

further scaling doesn't making delay \downarrow

(\hookrightarrow) Can achieve min delay

~~Prblm:~~ We are also \uparrow using C_{in}

previous stage driving present C_{in} experience more load.

may can't load \uparrow ed C_{in}

delay of previous stage can change

/ Increase

\Rightarrow CMOS inverter design flow:

\hookrightarrow symmetric behavior

$$\therefore T_{rise} = T_{fall}$$

$$N_{M_L} = N_{M_H}$$

If $k_n = k_p$ and $V_{Tn} = |V_{Tp}| \rightarrow$ we can achieve these conditions

For given C_L , $\frac{k_p n}{C} = \text{const}$

C_L -given

design inverter \downarrow PF with delay of 25ps

find K . Can find α

As we keep $\uparrow s_e$ w/

problems \hookrightarrow becoming const Independent of par

\hookrightarrow also causing loading prblm to prev stage \uparrow

Ex:

$$C_{ov} = 8355 \text{ aF}/\mu\text{m}^2 \quad ; \quad C_{ov} = 973 \text{ aF}/\mu\text{m}$$

$$L = 0.18 \mu\text{m} \quad W = 1000 \mu\text{m} \quad \text{and} \quad \frac{W_n}{W_p} = 2$$

($W \uparrow s_e$ inverter)

W - size inverter

$$W_n = W$$

$$W_p = \frac{W_n}{2}$$

$$Q: C_{self} = ? , C_{in} = ?$$

$$W_n = 1000 \mu\text{m} \quad ; \quad W_p = 2000 \mu\text{m}$$

$$1000 \times 973 \text{ aF}/\mu\text{m}$$

$$C_{gdN} \quad C_{gdP} \quad C_{dBn} \quad C_{dBP}$$

$$\underbrace{w \cdot C_{ov}}$$

\downarrow diodes rev bias

cap \rightarrow com. 18 more

$$C_{GPN} \approx C_{GDP} = W \cdot COV \times$$

$$C_{GPP} = (W) COV$$

$$C_{GPN} = W \cdot COV$$

$$C_{GDP} = 2 \times 1000 \times 973 \times 10^{-18} \times 10^{-9}$$

$$= 2.973 \times 10^9 F$$

$$= 1946 \times 1946 nF$$

$$C_{GPN} = 973 nF$$

Both are in parallel

$$\begin{matrix} 1946 \\ 1973 \\ 2.919 \end{matrix}$$

$$= 2.919 \times 10^{10} F \quad C_{self} = 2.919 nF$$

$$2.919 \times 1000 \times 10^{-18} F \parallel$$

$$= 2.919 \times 10^{-15} F = 2.919 \times 10^{10} F$$

$$CL = 1 pF$$

$$W = \frac{1000 \mu m}{5 \mu m - 500 \mu m + 1000 \mu m}$$

C_{self} now becomes greater than CL

$$T = \frac{C_{in}}{C_{self}} + \frac{C_{self}}{C_{in}} \quad : \text{no longer limit of } T \text{ using } w$$

Ising C_{in}

which mode considered
to calculate C_{in} ? Linear/saturation

$$C_{in} = C_{gen} + C_{gdp} + C_{sdn} + C_{gd}$$

\overbrace{wLCOV} for n_m

$wLCOV \quad wCOV \quad w_{COV} \quad w_{COV}$

$$= w_n LCOV + w_p LCOV + w_n COV + w_p COV$$

$$wLCOV \quad wLCOV$$

$$w_{COV} \quad w_{COV} \quad w_{COV}$$

$$w_n COV \quad w_p COV$$

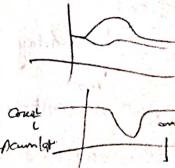
rewrite

$$C_{in} = (WLCOV + wCOV)_n$$

$$+ (WLCOV + wCOV)_p$$

$$(w \cdot COV)_n + (W \cdot COV)_p$$

Overlap
at low also.



$$C_{out} = (W \cdot COV)_n + (W \cdot COV)_p$$

$$+ C_{PBN} + C_{OBF}$$

If these parameters
given calculate

otherwise ignore

Because they are

other capacitances \Rightarrow Not dominant \approx

$$W = 0.27 \mu m \quad (\text{very min in specific technology})$$

$$= 3 \times 0.27 \times 10^{-6} \times 0.18 \times 10^{-18} \times 10^{18} F$$

$$= 3 \times 0.27 \times 10^{-6} \times 973 \times 10^{-18} \times 10^{18} F$$

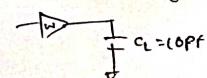
$$+ 6 \times 0.27 \times 10^{-6} \times 973 \times 10^{-18} \times 10^{18} F$$

$$\approx 2.83 fF$$

min size of $w = 0.27 \mu m$ for tech giving
2.83 fento of capacitance

$$* CL = 10 pF \quad (\text{given})$$

design inverter delay should be minimum & should drive CL ?



$$w = w_{min}$$

$$L = L_{min} = 0.18 \mu m$$

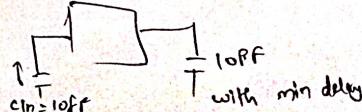
wmin use

C_{self} becomes more than
10 pF

but C_{in} also reqd
due to w_{Tie}

$$.. \text{let } C_{in} \text{ also given}$$

$$C_{in} = 10 pF$$

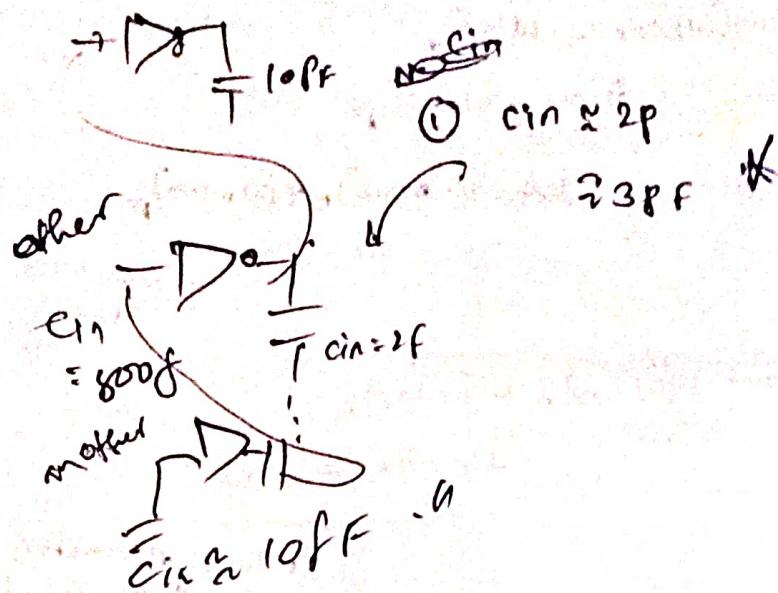


$$CL = 10 pF$$

with min delay

Soln to this - this,

$$\left[\frac{C_{out}}{C_{in}} \right] = \frac{1}{M_0} \cdot \frac{1}{\min \text{ delay}}$$



we will use multiple inverters

How many, no. of stages?

What all sizes we have to use
for inverters?

If same inverter size (min size)



small \rightarrow bigger

called
TAPERED BUFFER CHAIN

we need,

Formal method to find

Size & no. of inverters.

Quiz 1