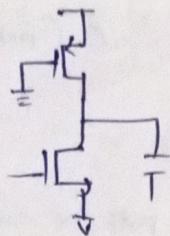


In pseudo NMOS,



(the always on PMOS)

charging \Rightarrow PMOS \uparrow

- * but here speed only depends upon NMOS upto $VDD - V_{TN}$ then PMOS will come into picture

by CVSL

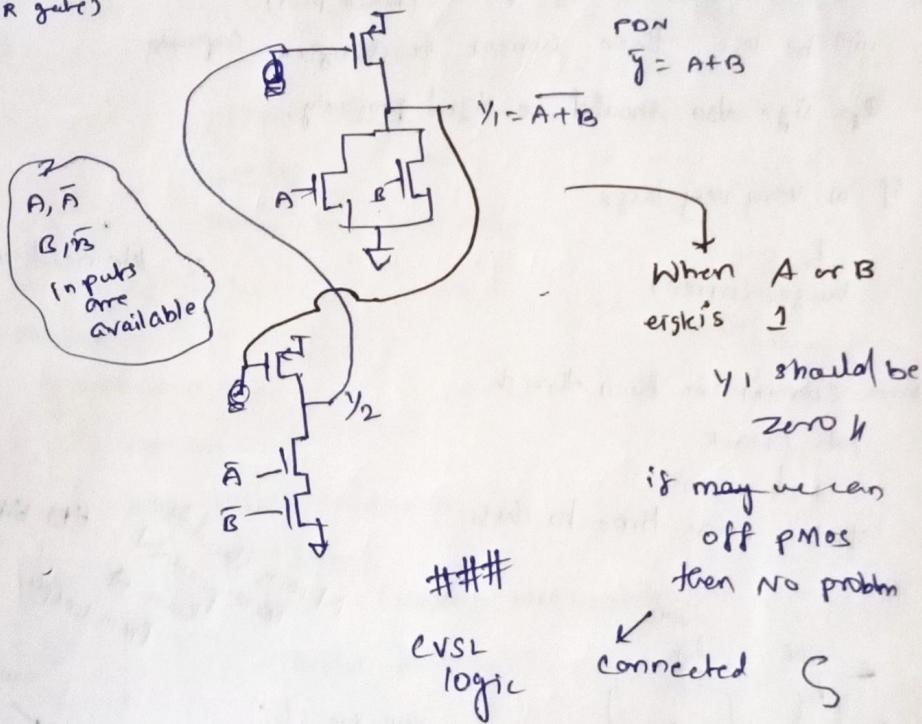
Cascade voltage switch logic

$$Y = \overline{A+B} \quad (\text{NOR gate})$$

$$Y_2 = \overline{\overline{A} \cdot \overline{B}}$$

=
NAND of
 \overline{A} & \overline{B}

$$\overline{Y}_2 = \overline{\overline{A}} \cdot \overline{\overline{B}}$$



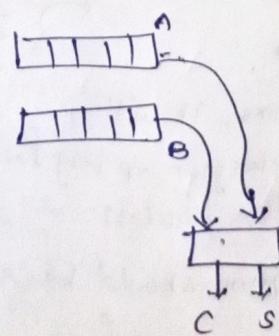
9-10-24

Static
→ CMOS
→ PTL
Pseudo-NMOS
CVSL

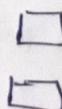
→ used to design seq / combil circuit

e.g. serial adder - n bit

$$\begin{array}{r} 12 \\ \times 11 \\ \hline 12 \\ \times 12 \\ \hline 132 \end{array} \rightarrow \text{develop architecture}$$



let 'n=1'



S: sum
C: carry

Pseudo-NMOS

problem
Static p

if PD

A-

pMOS

\Rightarrow pMOS 1

at here
speed only depends
upon NMOS
upto $VDD - VTN$
then pmos will
come into picm
 r_{on}
 $y = A + B$

$A + B$

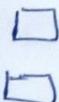
When A or B
is 1
 y_1 should be
zero 1

if may we can
off pMOS
then no problem

connected S

final circuit

let $n=1$



S: sum
C: carry

5 6 6 3

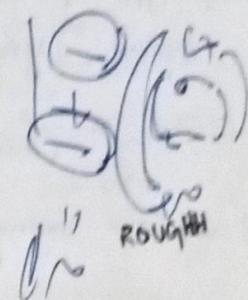
3 2 8 6

3 8 2 6

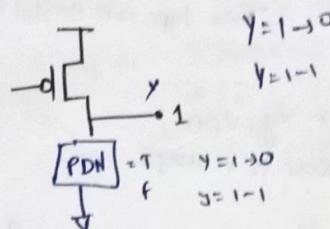
1' 3 8 2 6

100 110 12

100 5 7 3 6 = 6
6 7 8 5 6 Y



Pseudo-NMOS:



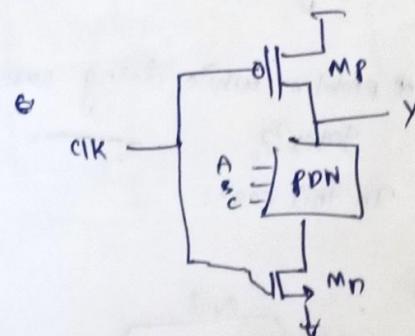
if PDN on \rightarrow then both on 1

\rightarrow we saw soln via CVEL 11

* No. of Transistors reduced (very).

Problem here:

Static power Dissipation



$CLK \Rightarrow 0$

$M_N = \text{off}$

$M_P = \text{ON}$

$y \Rightarrow \text{charge to high}$

$V_y = VDD$

$CLK \Rightarrow 1$

$M_P = \text{off}$

if PDN logic is true

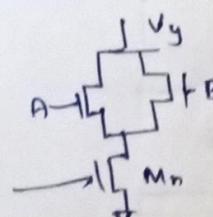
$\hookrightarrow V_y = 0$

if PDN logic false

$\hookrightarrow \text{No path}$

$V_y = VDD$

if PDN = 1

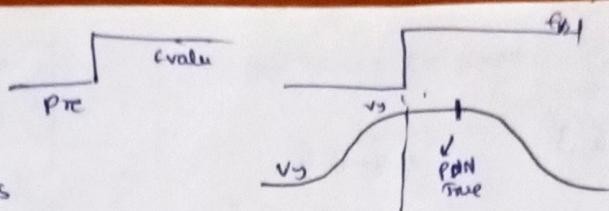


if A & B such that
is 1 is true
means \exists a path

$CLK = 1 \rightarrow$ Evaluation phase

$CLK = 0 \& V_y = VDD \rightarrow$ precharge phase

For this circuit work properly



This type of circuit is called Dynamic circuit
(due to clock)

If we are storing a logic on capacitor, there will always be a leakage

charge will decay $\propto t$
as time passes

$Clk \Rightarrow$ Making dynamic

* because there is a constraint
on Clk frequency ω

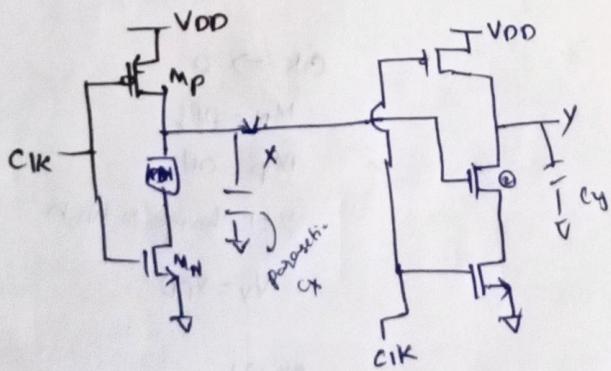
Ex: If 10 ns charge decays by 20% .

We need to recharge periodically
to maintain/stores

(2) These types are helpful then

We want $v_y = V_{DD}$
but there is leakage

Clk have to go to precharge phase again.



$A \rightarrow \square \square$ changing with frequency

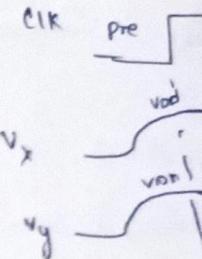
* changing of frequency A $0 \rightarrow 1$, ✓
 $0 \rightarrow 1 \rightarrow 0$
not allowed

* Input shouldn't

Change fast i.e. ~~a transition~~ has more than
one time.

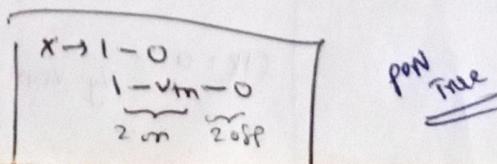
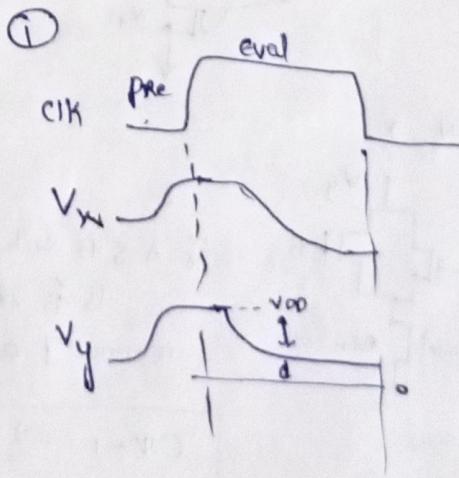
min freq constraint

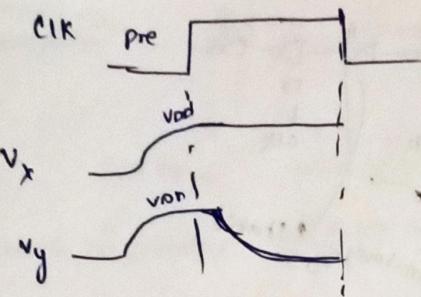
max freq constraint \Rightarrow $f_{max} = Clk$



① for some period
 $v_x <$

then after





PDN is false

$\Rightarrow v_y$ will discharge

discharges

for some period $v_x \rightarrow$ discharge (will not instantaneously)

$$v_x < v_t \Rightarrow \text{fill here}$$

~~NMOS ②~~ is ON

$\therefore v_y$ also discharge.

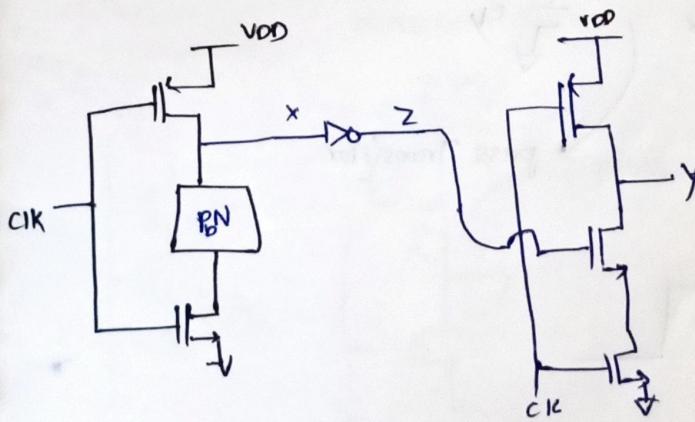
gating size of NMOS ②
fast k_{on}

drop of VDD ~~is~~ problem
problem of dynamic circuit.

then after $v_x \geq v_t \rightarrow$ NMOS ② will off

then v_y will be const

keeper circuit



Non-inverting structure

CLK = 0 (pre)

X = 1

Z = 0

Y = 1

CLK = 1 (eval)

X = 1 \rightarrow 0

PDN on

Z = 0 \rightarrow 1

NMOS ② will not be
ON instantaneously

but off

Y = 1 \rightarrow 0

PDN set (False)

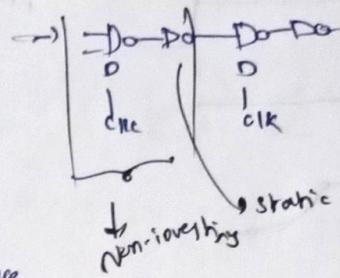
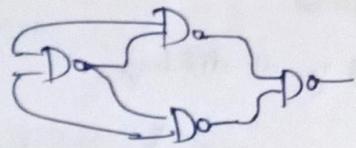
X = 1 (remains)

Z = 0

NMOS ② (off)

Y = 1

$$S = A \oplus b$$



Applications requiring,

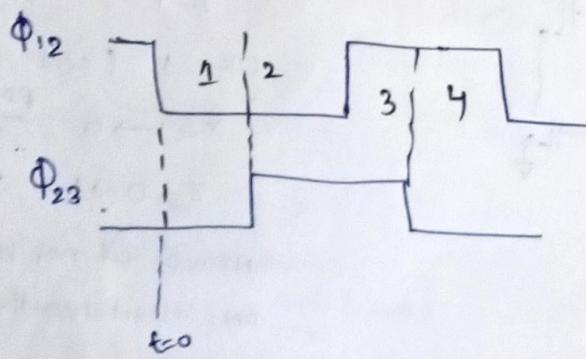
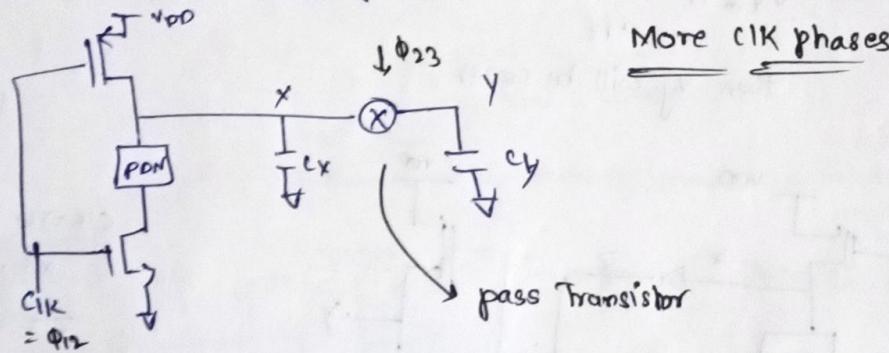
\Rightarrow logic to be stored in parasitic capacitance

\Rightarrow Dynamic circuit \rightarrow CLK \Rightarrow CLK \rightarrow max freq
logic \Rightarrow min fop

\Rightarrow cascading \rightarrow Adding CMOS inverter \rightarrow but making another problem \rightarrow Tradeoff
making Non-inverting.

One soln possible is:

IDE utilizes more phases of CLK.



Phase - 1:

$$\phi_{12} = 0, \phi_{23} = 0$$

switched

$$V_x = V_{DD}, V_y = X \quad ??$$

$$\underline{\text{Phase - 2:}} \quad \phi_{12} = 0, \phi_{23} = 1$$

$$V_x = V_{DD}, V_y = V_{DD}$$

Phase - 3:

$$\phi_{12} = 1$$

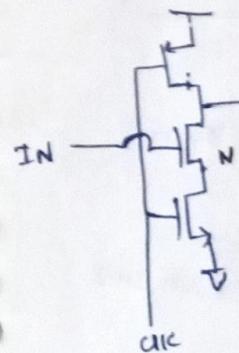
PDN true

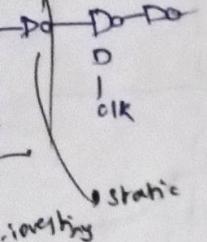
both discharge

Phase - 4: $\phi_{12} = 1$,

PDN true
 \downarrow
PDN false
 \downarrow
 $V_x = 0$

Another way (app)





Tradeoff
problem
making Non-inverting.

More CLK phases

nsistor

Phase -3: $\Phi_{12} = 1, \Phi_{23} = 1$

PDN true PDN false
both discharge Both will remain same

True	False
$V_x = 0$	$V_x = 1$
$V_y = 0$	$V_y = 1$

Phase -4: $\Phi_{12} = 1, \Phi_{23} = 0$

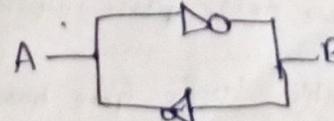
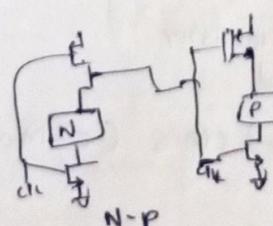
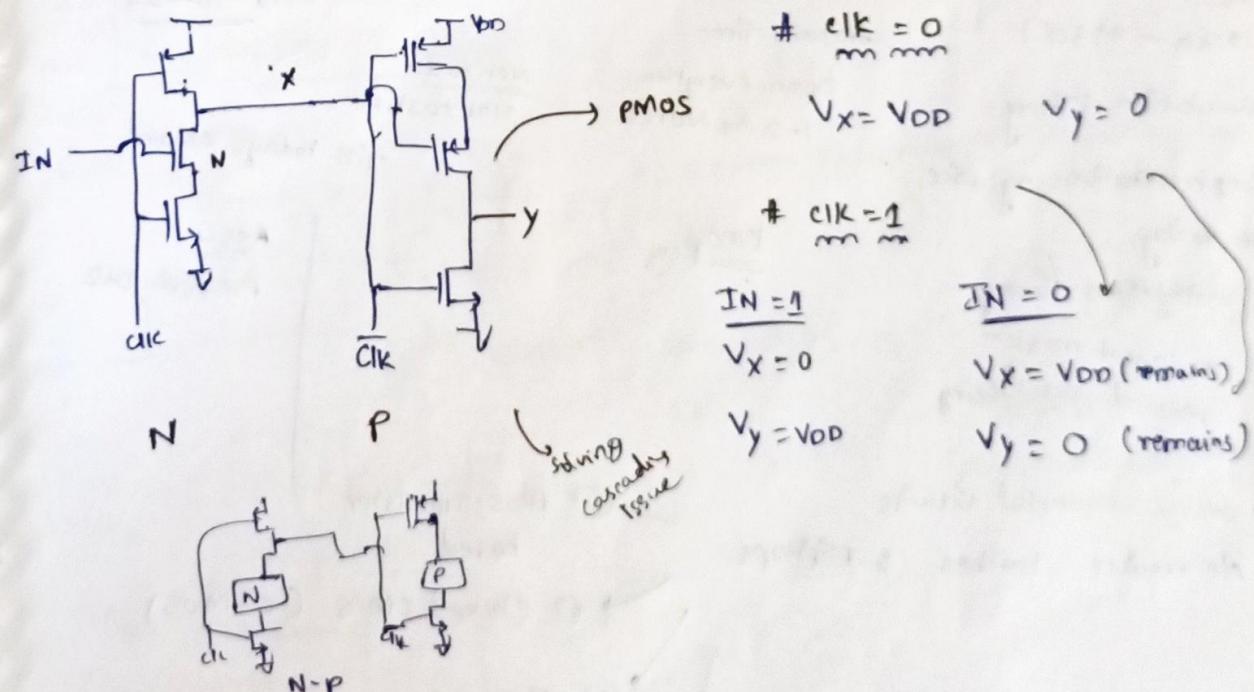
No connection
PDN true PDN false
 $V_x = 0$ $V_x = 1$ & $V_x \text{ where } \geq \Phi_3(n)$
 $V_y \rightarrow \text{stays (holds)}$

This type of gate
is called

TYPE -3 Dynamic Gate/ Circuit

Helps in doing fair design
etc.

Another way (approach): Domino logic
zipper logic
Nop-Domino
Norace (NORA logic)



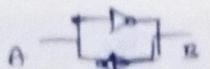
How A & B are related? $A = 0 \rightarrow B = 1$

$$B = \bar{A}$$

$$A = \bar{B}$$

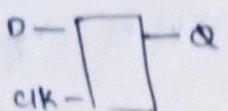
$A = 0$

$A=0 \rightarrow B=1$



Latches & Flipflops 1

D-latch:



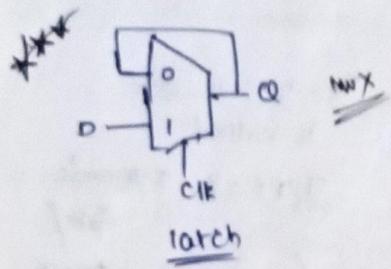
If $CLK \Rightarrow \text{High}$

then, $Q=D$;

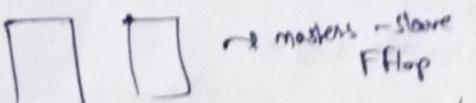
else, $CLK = 0$

$Q = \text{holds}$;

= \bar{Q} holds



MUX
↳ Tristate Inv
↳ pass-transistor ;



→ master-slave
FF flop

edge trig

{ Reasonably
Fast
FF topology
IMPACTFUL
Reason
paper layout
(Project
Refers)

16-10-24

STA
Static Time
Analysis

Ihr Quiz

(10:30 - 11:30)

sufficient time

Open-Everything
1-2 A4 Notes

Not to do
Not to share

Till today's Lecture

Implementation: ngSpice

No Verilog

verilog differs theory

No layout magic
related ques & theory

Kmap

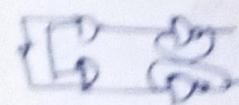
Assy
Before Wk

To design sequential circuits

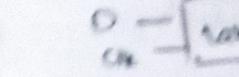
We require Latches & Flipflops

- ① Pass transistor based
- ② Clocked CMOS (C2MOS)
- ③ TSPC
- True single phase clocked
- ④ Static logic gate based

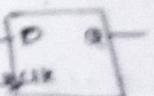
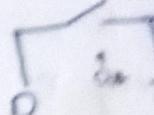
⑤ static logic gate



D-latch :



see simple implementation



M.S (base)

CLK

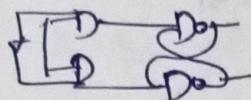
$CLK = CLK_A$

CLK_B

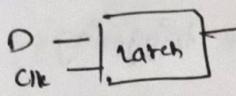
IN

X1

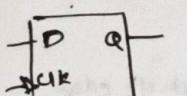
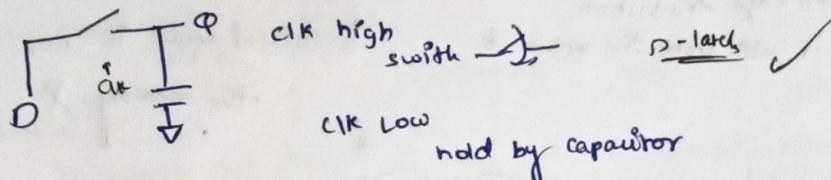
⑨ static logic, gate based



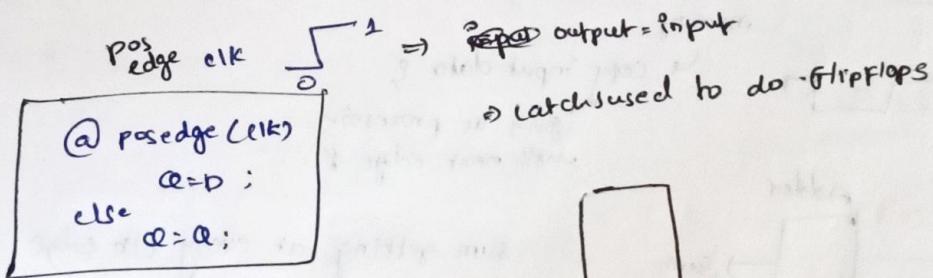
D-latch:



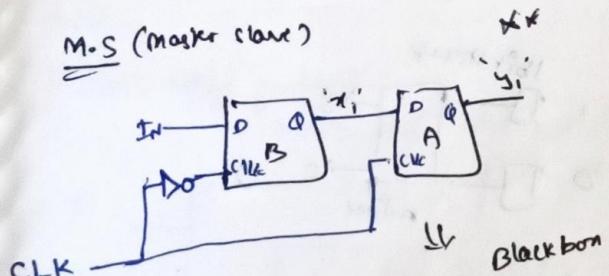
2m simple implementation



⇒ My F.F is positive edge triggered.
clk → ref point (what we are discussing)



M-S (Master slave)

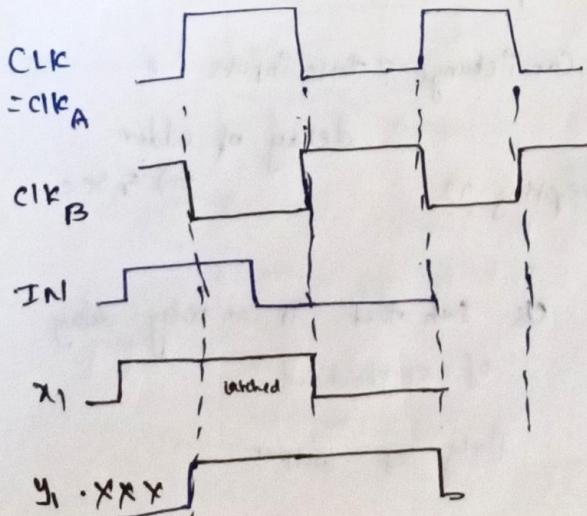


$x_i \rightarrow$ pName of variable (NOT dont care)



Latches -
↳ level sensitive

FLIPFLOP
↳ Edge sensitive
↳ Edge sensitive



Why do we need 'they latches & flipflops?

FF Memory element

FF's → Registers
Counters
FSM's

What means
Memory element?

Until edge transition
it will store the value.

-ve edge triggering

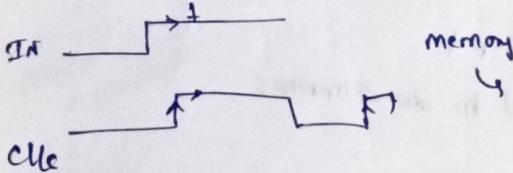
→ Show

3-bit shift register:

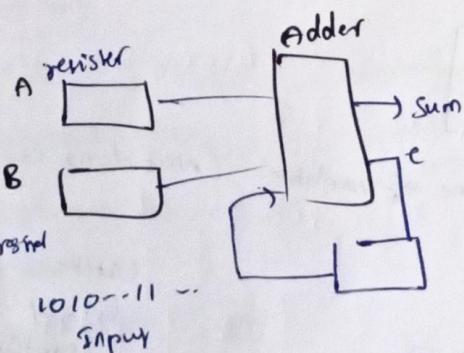
↳ Give serial
input data



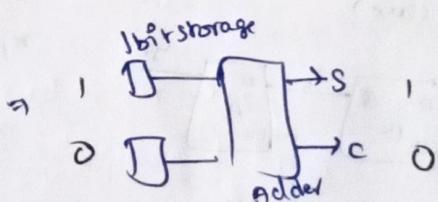
↳ This happens at each clk edge



↳ copy input data &
giving as processing
until next edge //



sum getting at every clk edge

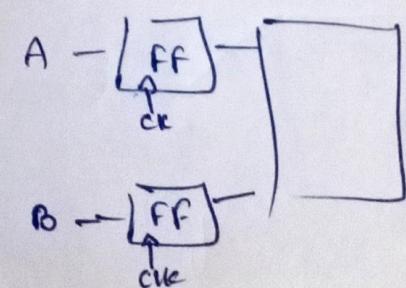


1 1
1 0
+
1 1
1 0
1 1

How fast can I change? These inputs?

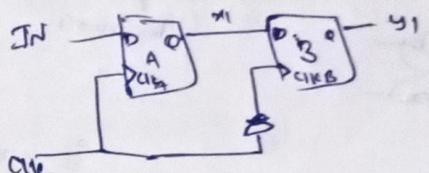
How
Correpting??

delay of adder
⇒ 5 ns



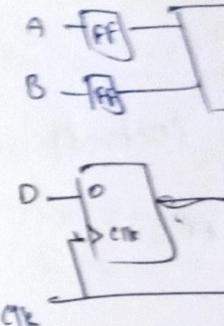
clk such that it can relay delay
of combinational

Urity of output



-ve edge triggering

→ Show



control
↳ work

let it...

tpd ce

clock

D

clk

ce



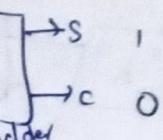
Edge triggering

→ Show

actual value is not
use
the memory X

at every clk edge

at every clk edge



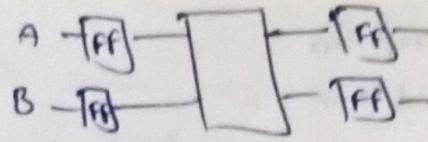
here inputs?

delay of adder

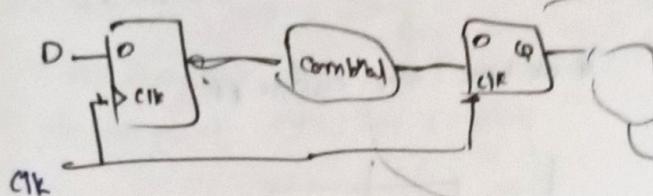
$$\Rightarrow 5 \text{ nsec}$$

- It can relay delay

input
output



how to sequence the data
to get reliable outputs?



functionally

$$\text{Design } Y = (A+B)C + DC$$

at some freq
reliable output not?

combinational

↳ worst case delay

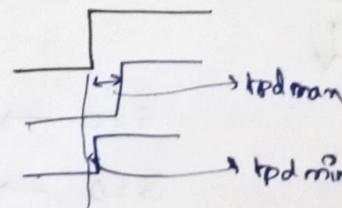
\Rightarrow sized
for best case:

combinational
circuit have propⁿ delay ↳

* $t_{pd\max}$

* $t_{pd\min}$

let it a buffer

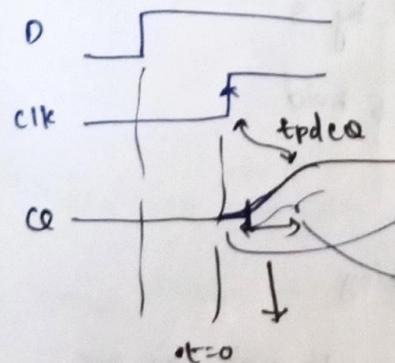


$t_{pd\ co}$

$t_{pd\ co}$:

clock edge arrived

↳ after this del is how much time it takes to set Q updated

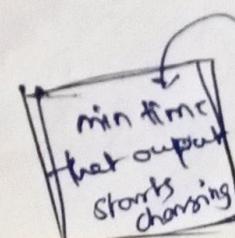


after clock edge

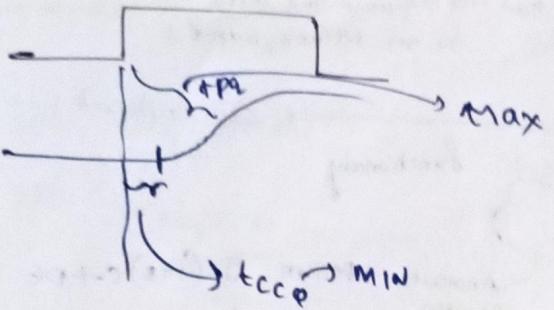
↳ some time silent
no transition

↓
no change starts
till then
contamination
delay

t_{co}



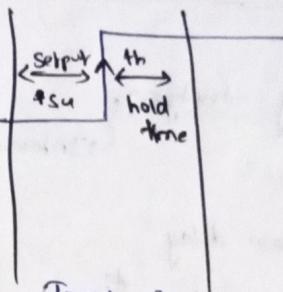
we can consider as
min delay of FF flop



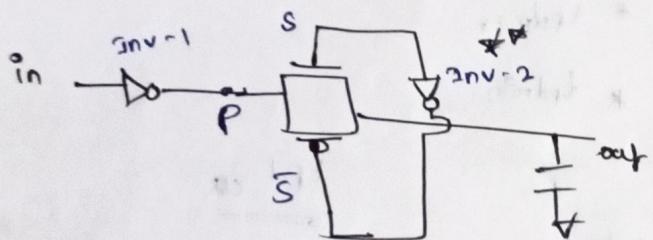
→ Setup time
→ Hold time

(Defined)

If we have two edge FF



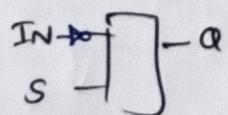
input should be kept const



If $S=0$, $out = ?$

$$out = out_{prev}$$

if $S=1$, $out = \bar{i}_{in}$



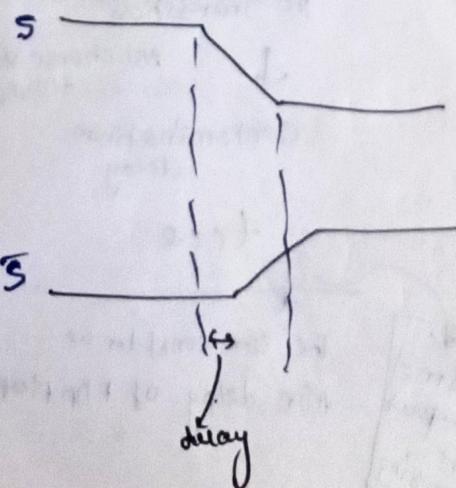
$$S=1 \Rightarrow Q=\bar{i}_{in}$$

$$S=0 \Rightarrow Q=Q_{prev}$$

kind of inverting latch

controlled by S

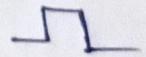
▷ Sample & hold



due to inv delay

In the region, we can't say our switch is off or on.

if we changed input
in that region



for reliable →
the segmen
the time is
→ We shoul
to change
Inv-2 de
→ S TR
durin
ce

Input

V_P

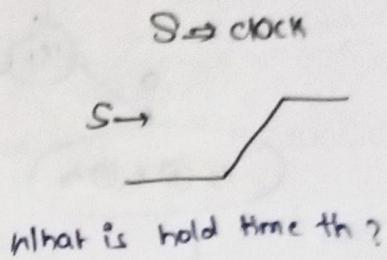
(Defined)
gr FF
Inverted latch
nmos off
pmos off
th
can't say our
n.6
ut

for reliable "open", we don't want any change of input signal during the setup region.

The time is INV-2 delay

⇒ We shouldn't allow the Input to change at time Inv-2 delay.

Inv-2 delay will govern our hold time delay

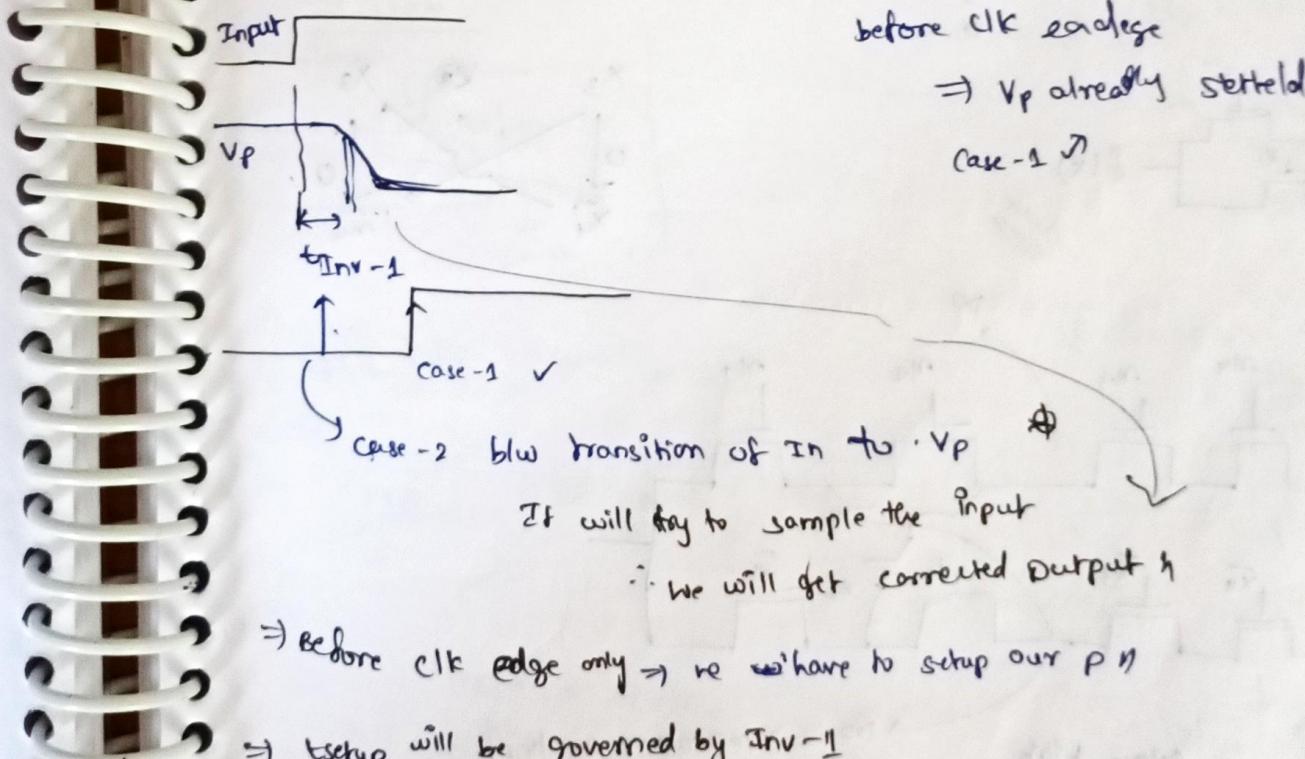


Once clock edge arrived,

P₁ charging
charge

→ S Transition happening

during delay of Inv-2 if we change input we can get corrupted.



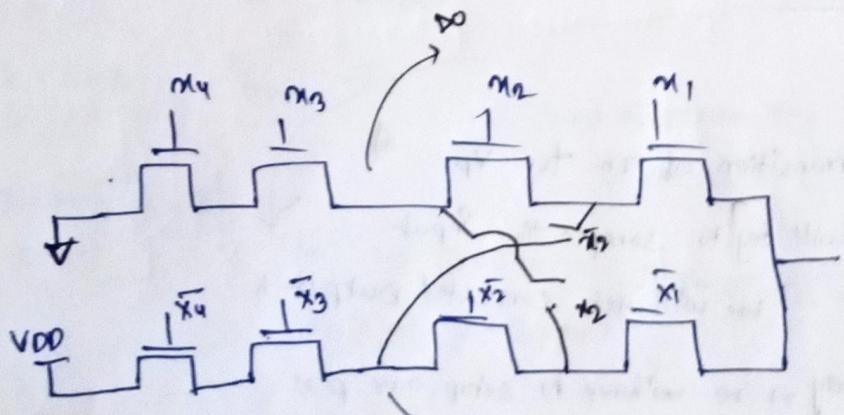
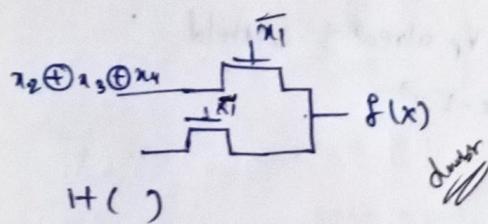
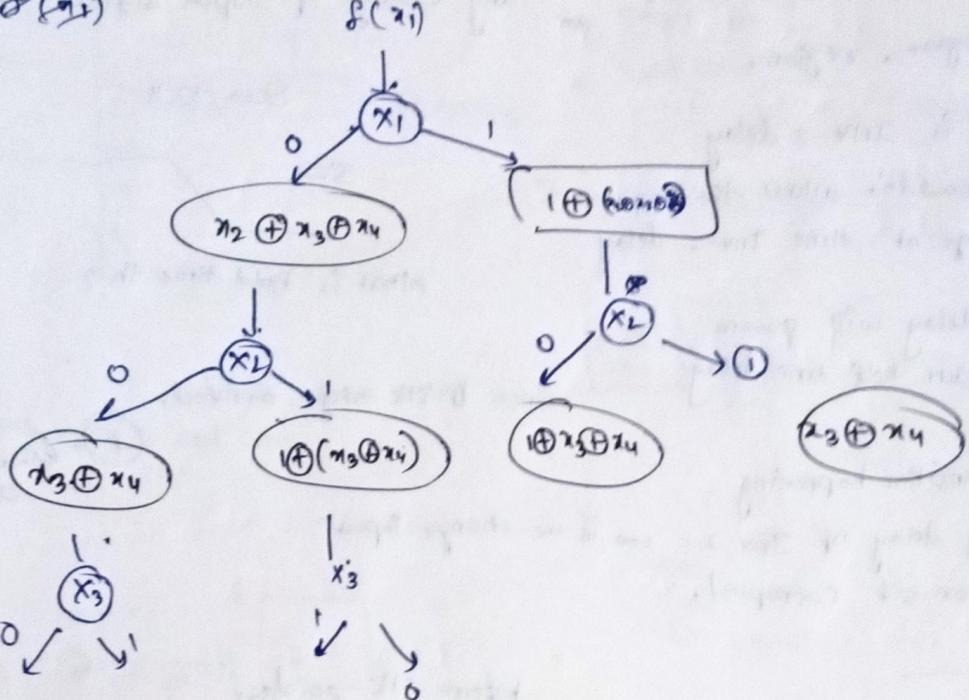
Bayant expansion:

$$\text{ex: } f(x_1, x_2, x_3, x_4) = x_1 \oplus x_2 \oplus x_3 \oplus x_4$$

but, we have to pass register logic

to implement this how??

$f(x)$



① Problems

↳ delay high

↳ loss of logic levels via due to \oplus travelling of large chain

∴ repeaters are added such that

if charge or discharge it will not reach

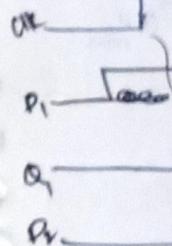
repeater

→ buffers

Setup time = t

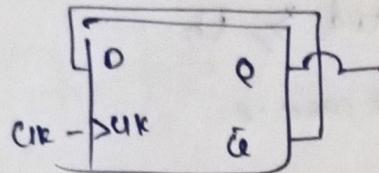
find. what
is circuit

Circuit



EPC

Constraints on
clock frequency



$$t_{PLH} = 25 \text{ ns}$$

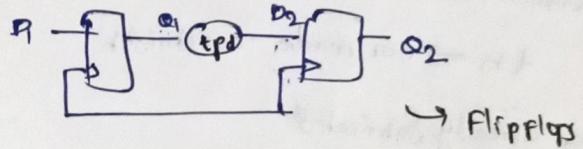
$$t_{PHL} = 40 \text{ ns}$$

$$\text{Setup time} = t_{SU} = 20 \text{ ns}$$

Find. What is the max clock frequency f_{clk_max} for which it will work?

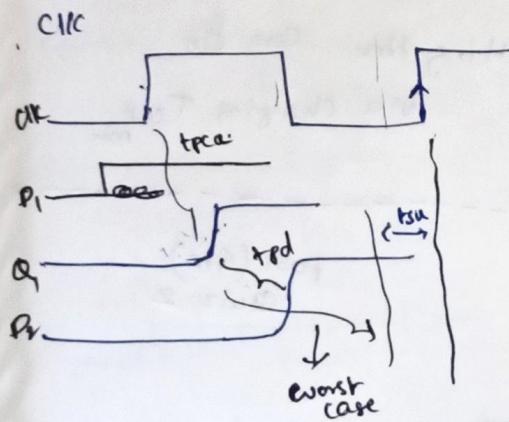
Q output $0 \rightarrow 1$ (Low to High)
 $\downarrow 25 \text{ ns}$

$1 \rightarrow 0$ (High to Low)
 $\downarrow 40 \text{ ns}$
Given



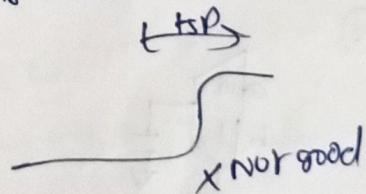
$t_{SU} \Rightarrow$ didn't change

P_2 shouldn't change at t_{SU}



$$t_{PCQ} + t_{PD} + t_{SU} = T_{clk}$$

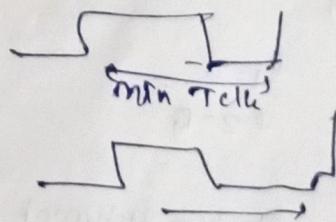
if changes



$$t_{PCQ_{max}} + t_{PD_{max}} + t_{SU_{UK}}$$

$$= T_{clk}$$

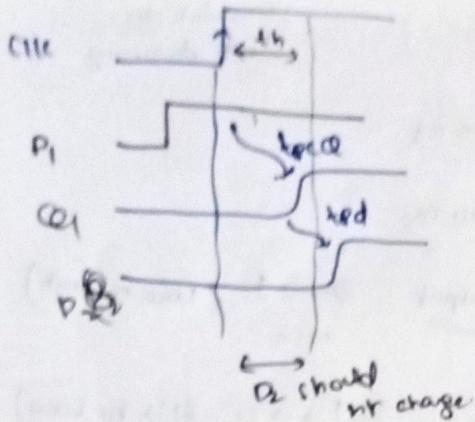
min. T_{clk}



$$\therefore T_{clk} \geq t_{PCQ_{max}} + t_{PD_{max}} + t_{SU}$$

will give $f_{max_{clk}}$

after clock clean



designed circuit

t_{th} → not made constraint

→ already fabricated

t_{th} → can't fined correct
after fabrication

$$t_{PCQ} + t_{PD} \geq t_{th}$$

for worst case \rightarrow

$$8 > t_{th}$$

$$6 > t_{th} \checkmark$$

$$t_{PCQ\min} + t_{PD\min} \geq t_{th}$$

t_{th} min delay constraint for FF

Setting time com bin

via changing $T_{cst\min}$

~~Quiz 2~~

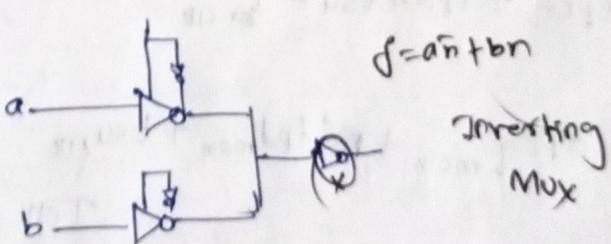
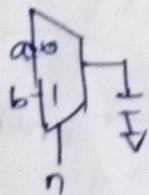
① CPLL (PLL)

No static power consumption

② $f = nB$

Differential pass Transistor logic

③



5 3 7 10 10

④

$$Q_1 = D$$

$$Q_2 = Q_1$$

Blocking statement

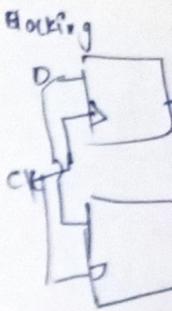
Q_1 assigned D

Q_2 assign Q_1

$$\therefore Q_2 = Q_1$$

$$Q_1 \leftarrow D$$

$$Q_2 = Q_1 \text{ fast}$$



Assignment

- ① A →
- B →

* purpose

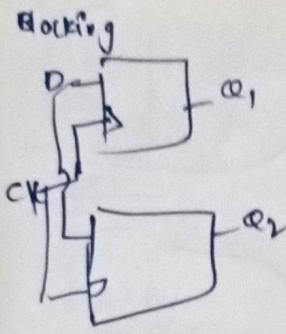
Switching

NSV

idle

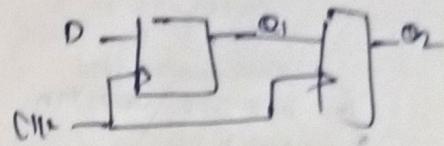
2x1

P

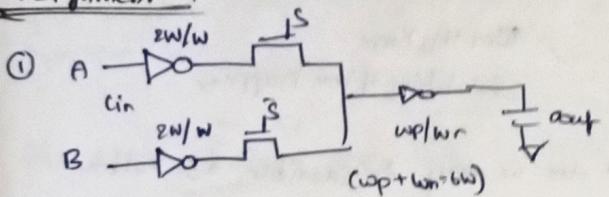


$$\begin{aligned} \textcircled{1} \quad & Q_1 = Q_2 \\ \textcircled{2} \quad & Q_1 = D \\ & Q_2 = Q_1 \text{, posy} \end{aligned}$$

Expecting both circuits?



Assignment - 4

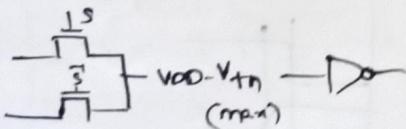


metastable
↓
vary W

* purpose of inverters
↳ to get logic 1 to VDD

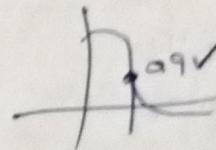
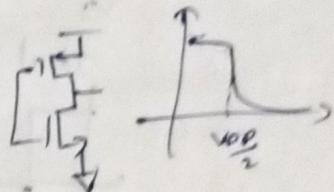
Switching threshold of
inverter ?? $V_{DD}/2$

less than $V_{DD}/2$
input
output = 1



$$\begin{aligned} \text{let } V_{DD} = 1.8V \\ V_m = 0.5 \end{aligned}$$

$$(V_{DD} - V_{TH})_{\text{max}} = 1.3V$$



1.3V → feeding to
try to switch
threshold 0.9V

We are trying to size '1' can

If 0.9 what the
signal reach 0.9 then my switch

2x1 MUX

Prob: Not going pure VDD

Let 0.65

Stop at $V_{DD} - V_{TH}$

Switch inv at 0.69

put inv set logic levels to be stored

regarding
Matched
W

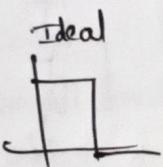
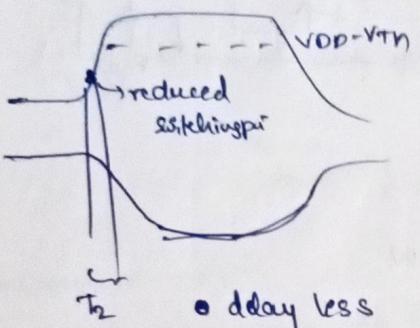
↳ delay is main
concern

$V_{DD}/2 \rightarrow$ switched

→ whenever it read $V_{DD}/2$ it will switch
then it will give correct output

If we make $VDD_2 \ominus = 0.9$ to 0.65 Recharging point

then takes



$$1.8 \rightarrow 0 \quad T_1$$

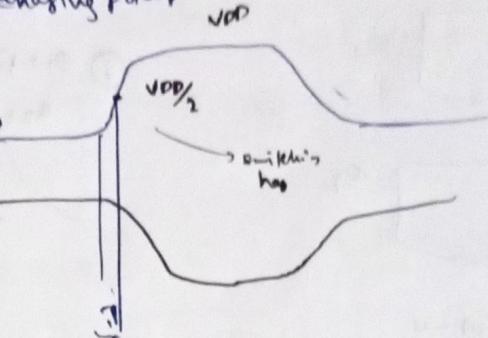
$$1.3 \rightarrow 0 \quad T_2$$

$$T_2 < T_1$$

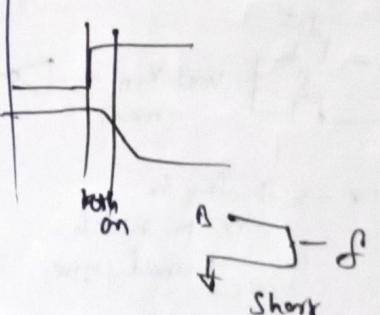
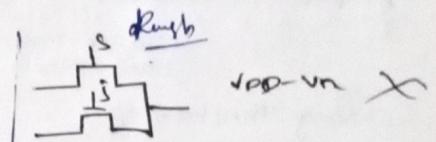
because of lowering
settling advantage

skewed Inverted
Beneficial

→ Are we okay to sacrifice 0.3 Volt
To improve delay



After this time
switching of inv happens



① Ques.

$$W_{P1} + W_{N1} \overset{\text{Req}}{=} 6W$$

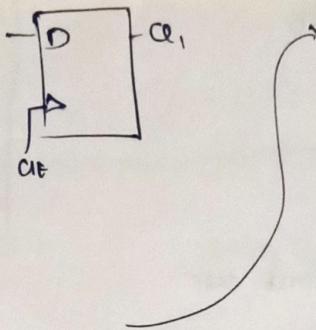
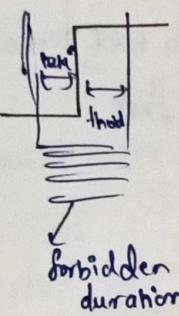
TABLE

② Inverters Not Allowed

ONLY MUX

All controlled by

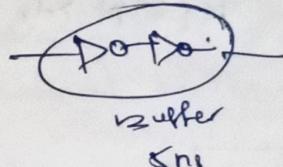
Answer



Flip flop acts like a sequential

⇒ Have a combinational effect
if it has delay

Let delay 5ns



Input shouldn't change in this duration

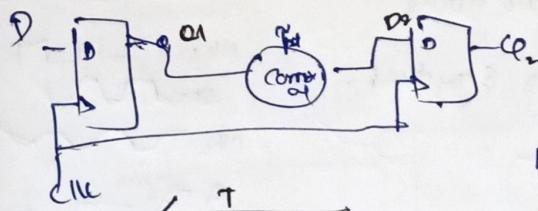
We put a keeper here
controlled by clock

If we give input also then after
clock it will give to combinational circuit

$t_{cq} \ t=0 \text{ ns}$ Input

$\checkmark \ t=2 \text{ ns}$ Input changed
NOT to be done

Internal gates will complete
not get reliable output



We are doing Timing Analysis.
Not functional Analysis

In order to not violate setup time
What to do?

⇒ MAXIMUM prop delay (We can afford)

$$t_{qk} \geq t_{pcq} + t_{pd} + t_{setup}$$

for worst case

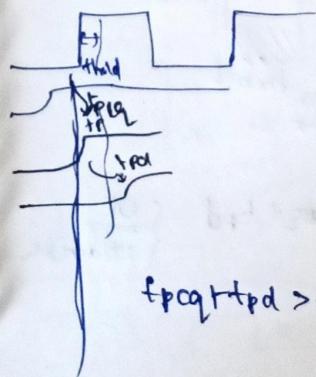
$$t_{qk} = t_{pcq} + t_{pdmax} + t_{setup}$$

$$+ t_{pdmax} = T_{clk} - t_{cq} - t_{setup}$$

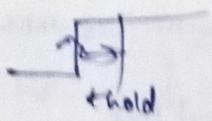
Maximum delay constraint

To avoid setup time violation,

To avoid hold time violation



$$t_{pcq} + t_{pd} > th$$

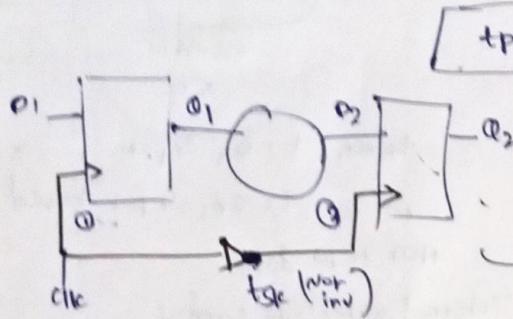


$$t_{pq} + t_{pd} > th$$

D₁ also shouldn't charge it

$$t_{pq} + t_{pd} > th$$

worst case

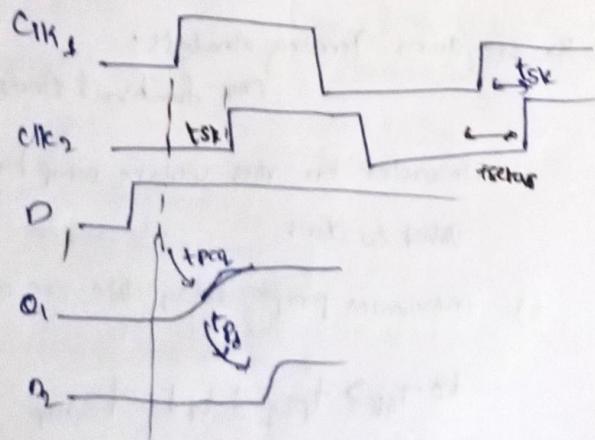


$$t_{pq, \min} \triangleq th - t_{pq}$$

Ideal
→ zero hold time
fast

Derive max & min delay constraints? Two cases

→ timing analysis & my that.

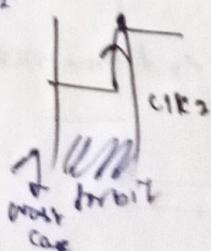


B. $t_{pq,1} + t_{pd} \leq T_{Clk} + t_{sk}$
+ t_{setup}

$$t_{pq,1} + t_{pd} + t_{setup} \leq T_{Clk} + t_{sk}$$

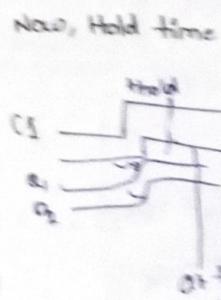
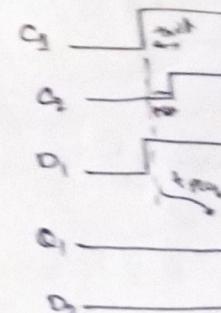
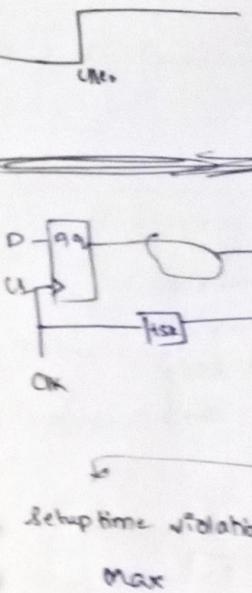
O₁ change after t_{pqa}
O₂ T₁₁ " t_{pqa} + t_{pd}
D₂ shouldn't change
before flip flop 2 clk

Flip flop 2:



✓

$t_{sk} + t_{pd}$ { Ok
Hold time

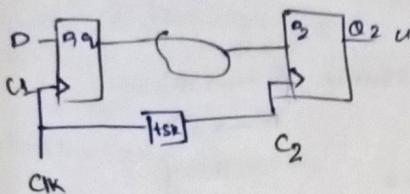


Toys H/W

threshold

26-10-24

light green — Biscuit
dark



Timing issue:

↳ constraints?...

Any combinational circuit will be surrounded by FF's for not to overwrite data. !!

↳
Setup time violations
Max

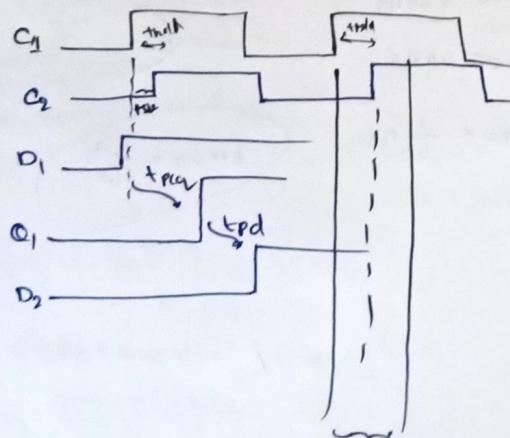
t_{pd} & t_{hold}:
Hold time violations
Min d_u

a — b — c
S — F — FF
how fast can change a & b ??
t_{combinational}

present



Why/How
related??



$$*(t_{pcq} + t_{pdg} + t_{setup}) \leq T_{clk} + t_{sk}$$

If $t_{sk} = 0$

Let $T_{clk} = 10 \text{ ns}$

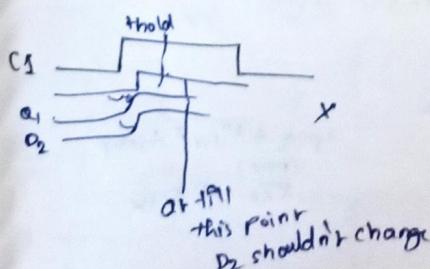
$t_{ons} \leq T_{clk}$

$\Rightarrow T_{clk} > t_{ons}$ must

If some $t_{sk} \neq 0$

$T_{clk} \geq t_{ons} - t_{sk}$

Now, Hold time violation:



$$\therefore t_{pcq} + t_{pd} \geq t_h + t_{skew}$$

Q: $t_{pcq} = 5 \text{ (max)}$

3 (min)

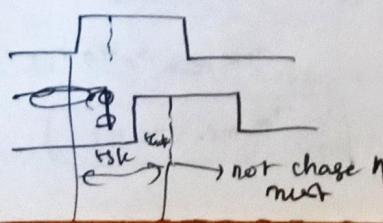
$t_{sk} = 5 \text{ n}$

$t_{su} = 4$

$t_{sk} = 5 \text{ n}$

$t_h = 2$

Find $t_{pd \text{ max}}$ and $t_{pd \text{ min}}$??

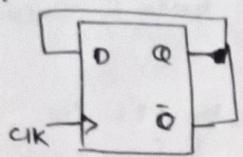


Holdtimes gives min constraint or propagation delay.

$$t_{pd} \text{ max} = 6$$

$$\text{min} = 4$$

Q:



$$t_{PLH} = 25$$

$$t_{PHL} = 40$$

$$; t_{SU} = 20 \text{ ns}$$

Assume

$$t_{CK \text{ to } Q}$$

$$t_{CK \text{ to } \bar{Q}}$$

delay
same

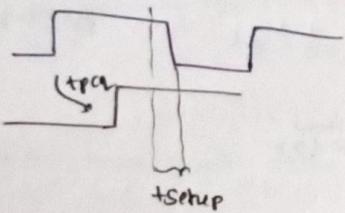
Q_1 can go $0 \rightarrow 1$ or $1 \rightarrow 0$

" "

\therefore These usage there are going to be

Q: Find Max clock freq?

$$f_{\text{max}} = \frac{1}{(T_{CK \text{ min}})}$$



$$T_{CK} \geq t_{PCQ} + t_{\text{setup}}$$

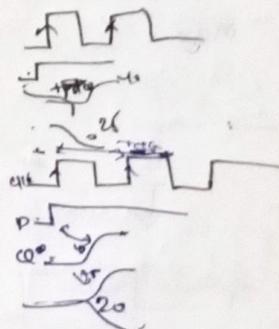
$$\geq 40 + 20 = 60 \text{ ns}$$

Take MAXIMUM

$$T_{CK} \geq \text{max } 60 \text{ ns}$$

Since both
Constraints Should
Satisfy

$$f_{\text{max}} \leq \frac{1}{60} \text{ Hz}$$



$$\therefore f_{\text{max}} = \frac{1}{60} \text{ Hz}$$

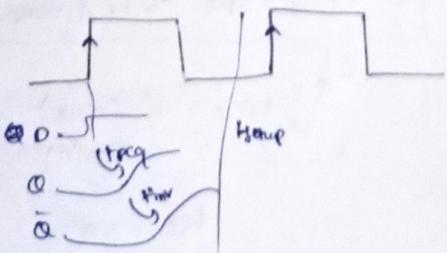
if $h \rightarrow L$

$L \rightarrow H$ are not equal

$$t_{INV} = 10 \text{ ns}$$

Same values as above ques

$T_{CK \text{ min}} ?$ s.t it should work?

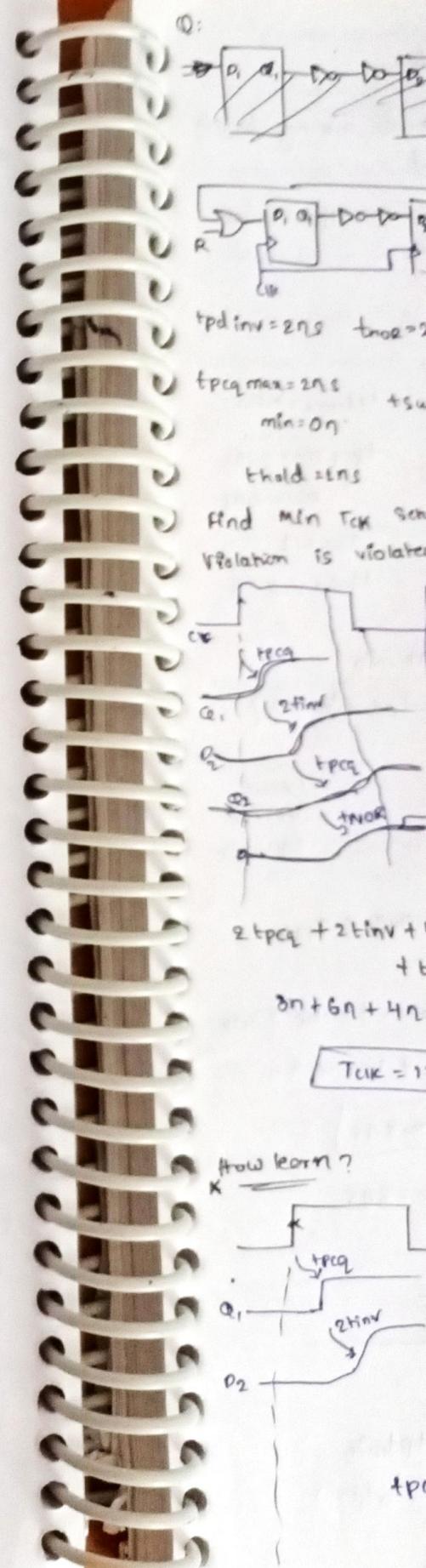


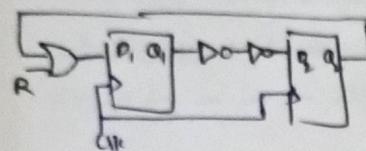
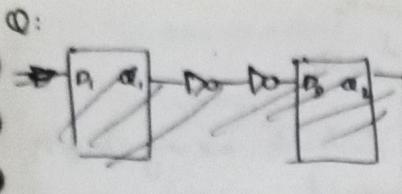
$$t_{PCQ} + t_{INV} + t_{\text{setup}} \\ (\text{max}) \\ \leq T_{CK}$$

$$40 + 10 + 20 \leq T_{CK}$$

$$T_{CK \text{ min}} \geq 70 \text{ ns}$$

$$\therefore T_{CK \text{ min}} = 70 \text{ ns}$$





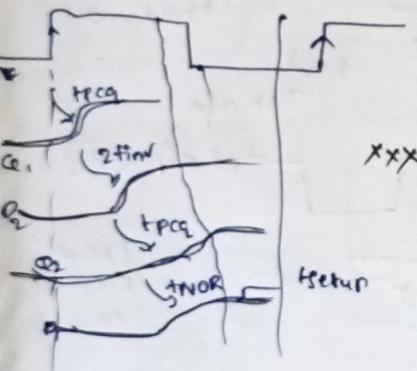
$$tpd_{inv} = 2\tau_2 \quad t_{NOE} = 2\tau_2$$

$$tpcq_{max} = 2\tau_2 \quad min = 0\tau_2 \quad t_{SU} = 3\tau_2$$

$$t_{hold} = 1\tau_2$$

Find Min TCK setup time

Violation is violated?



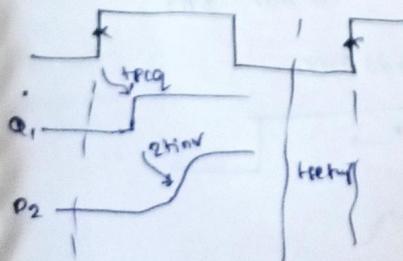
$$2tpcq + 2t_{INV} + t_{NOE} \leq TCK \\ + t_{setup}$$

$$3\tau_2 + 6\tau_2 + 4\tau_2 = 13\tau_2 \leq TCK$$

$$TCK = 13\tau_2 \rightarrow \text{NOKU}$$

??

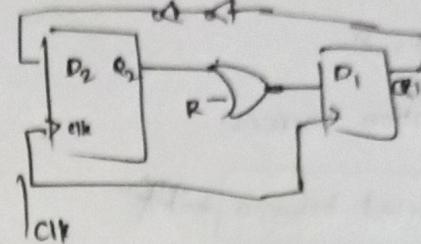
How to run?



$$tpcq + 2t_{INV} + t_{setup} \leq TCK$$

$$TCK > 9\tau_2 \quad ??$$

Same circuit



$$tpcq + tpd_{NOE} + t_{setup} \leq TCK$$

$$TCK \geq 7\tau_2$$

We will take max of both

$$\therefore TCK \text{ of both max} = \max(9, 7)$$

$$= 9\tau_2$$

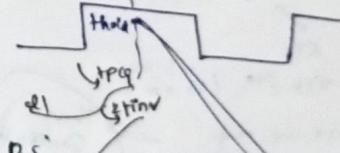
doubt

$$\therefore TCK = 9\tau_2$$

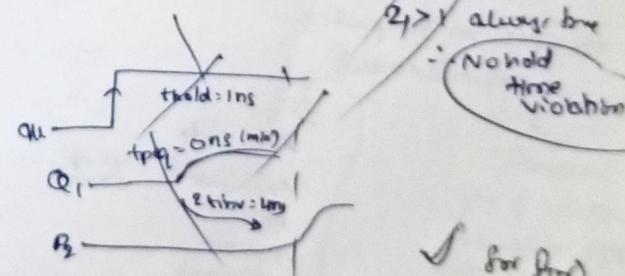
To satisfy both

Analyse for hold time violation?
For ① kind off.

② should it change till Hold time

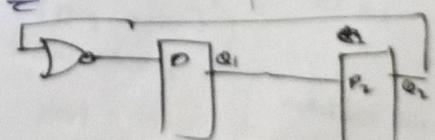


~~②~~ + 2\tau_2 > t_{hold} ✓
or always
2\tau_2 > 1 always true

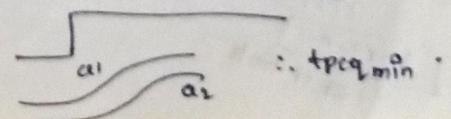


✓ for first
that circuit

if not



For this same values



$$\therefore tpcq_{min} =$$

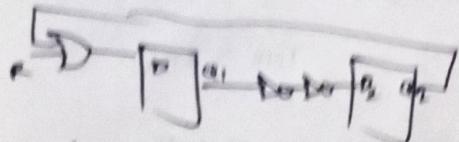
th < one

~~th < 200 ns~~

→ hold violation happens:

↳ Buffer inserted between ~~hold~~

that circuit is



✓ For this same value AD hold time violation.

(For this, check prev page) XXX

Design compiler ??

CPU processor → verilog

↳ we want chip

✓ RTL
Tech file (130 nm)

* These are my constraints

Then
Generated
chip

Scripts on Companies' Fundamentals

✓ LinkedIn

Skills & req:

RTL designer

⇒ skill set

industry aware

skill set → Tung team

mentor

10/11/15 N

Cadence

Schematic simulation

else add version of
LT SPICE

Vorturino

Toolset tools

RTL side
Encounter (one of tools)

Mentor
Graphviz

Learning Tools
(Easier part)
fundamentals

Learn X tools
Y tool knows
make easier

1 week, monthly
each idea
(if shared)

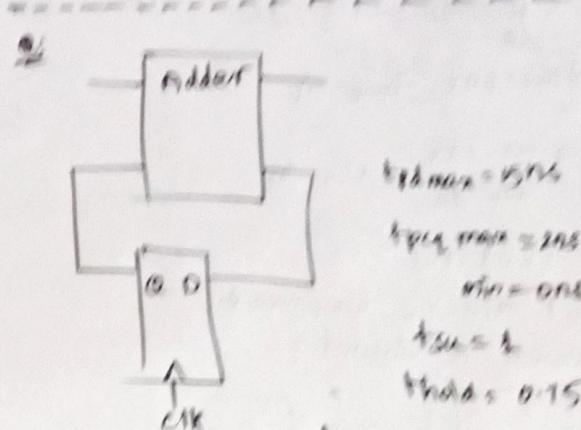
If No Idea
undergrad → facilitates our way though
shouldn't be confused
FOCUS on THAT

→ 100% shared

tpd min 2, 4
1/4 hold min 2

It's very fast else
often hold time
missed.

We can make a
Inserting buffer



tpd max = 15 ns

treq max = 2 ns

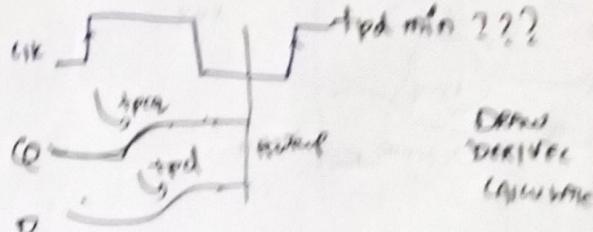
th = one

tuse = 2

thdd = 0.15

Find Tck min tuse

tpd min ???



treq + tpd + tsetup < Tck

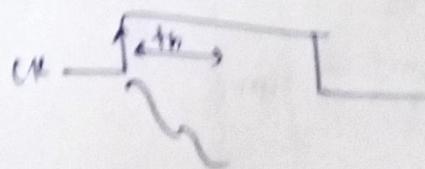
=> treq max + tpd max + tsetup < Tck

2 ns + 5 ns + 1 ns < 9 ns

$$\therefore Tck \geq 8 ns$$

∴ Tck min = 8 ns

Tools for hold time



th < treq min + tpd min

2 = 0 (tpd)

tadmin > th

guru
D1 max
min
D2 max
min
Q1 —
Tck min
worst case
delay

older
elements are very strong
used

so no hold time

$t_{pd\ max} = 15\ ns$
 $t_{pcq\ max} = 2ns$
 $\min = 0ns$
 $t_{su} = 1$
 $t_{hold} = 0.15$
 $T_{clk\ min} = T_{clk}$
 $t_{pd\ min} ??$

Draw
Derive
Calculate

$t_{pd} + t_{setup} \leq T_{clk}$

$t_{pd\ max} + t_{setup} \leq T_{clk}$

$+ 5ns + 1ns \leq T_{clk}$

$\therefore T_{clk} \geq 8ns$

Time

$c_q\ min + t_{pd\ min}$
 $\geq 0\ (\text{given})$

$t_{min} \geq t_h$

$t_{pd\ min} > 0.75ns$

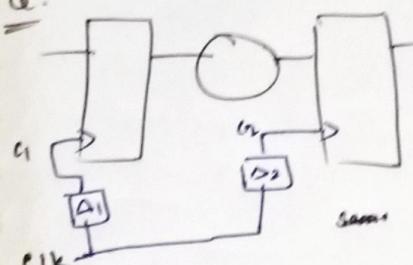
$\therefore t_{pd\ min} \geq 0.75ns$

If very fast circuit created

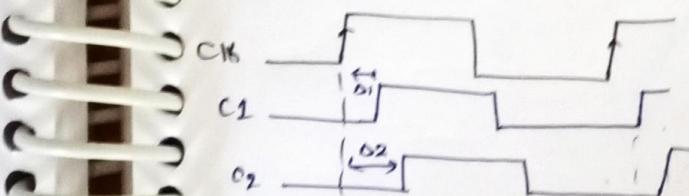
then hold time constraint
violated.

We can make use of
Inserting buffers ~~xxx~~ ✓ (?)

a:



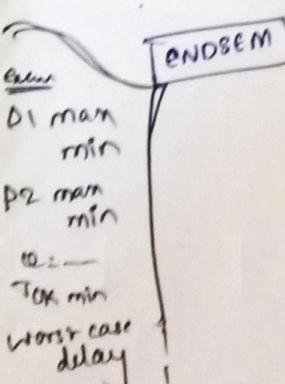
Derive constraint eqns for this ??



Individual
project

20%

VIVT



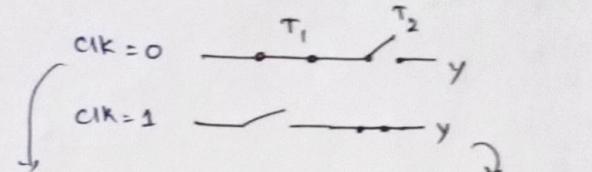
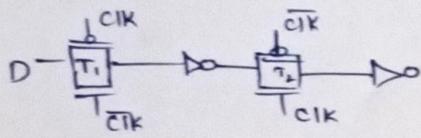
$C1\ min$
 $P1\ min$
 $P2\ min$
 $t_{clk\ min}$
worst case delay

6-11-24

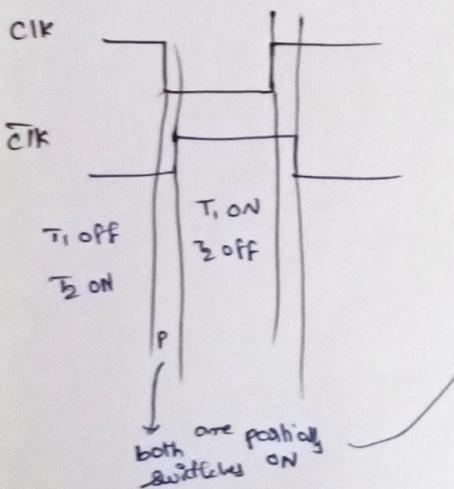
Latches & flipflops:

- ① CPL based (Dynamic)
- ② C²MOS (Dynamic)
- ③ TSPC (Dynamic)
- ④ Static logic gate based

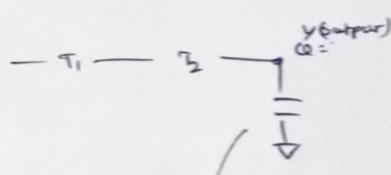
CPL based:



Here y not changing
∴ (Latching)
↳ to Master-Slave FF.

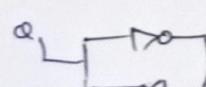


There is a path from input to output.
* if we change input, output will change



Charging & discharging

Soln:



will solve the problem.

PTL ??
another

↳ If use it gets reduced to desired value
& also uses less power.

clk=0

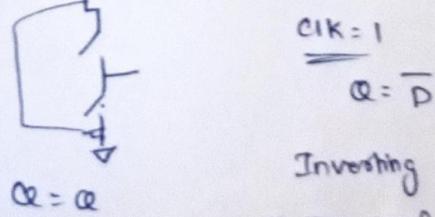
⇒ M₄ & M₃ will be off

kind of Tri-state Inverter

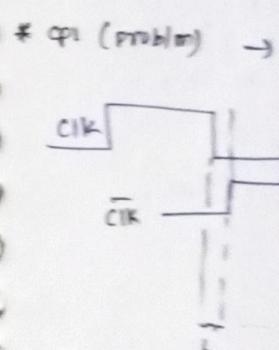
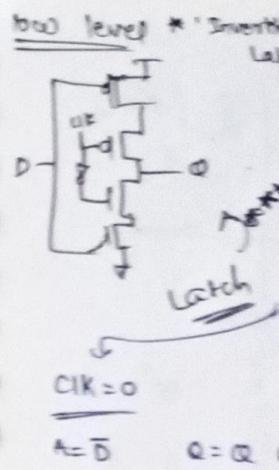


Inverting latch

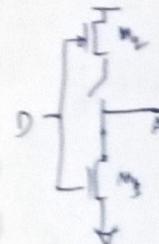
If we want normal (non-inverting)
Put inverter before Q
output



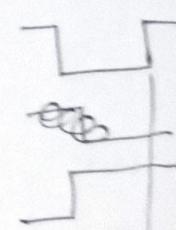
Inverting Latch
* High level



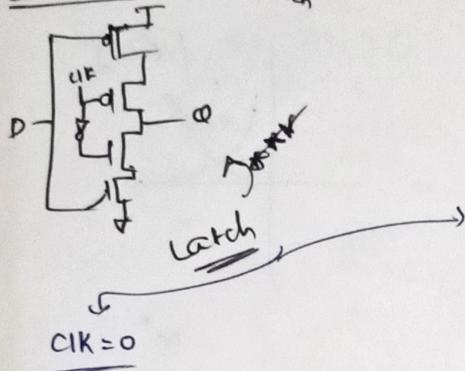
t-11 (both clk &



After t-11 how

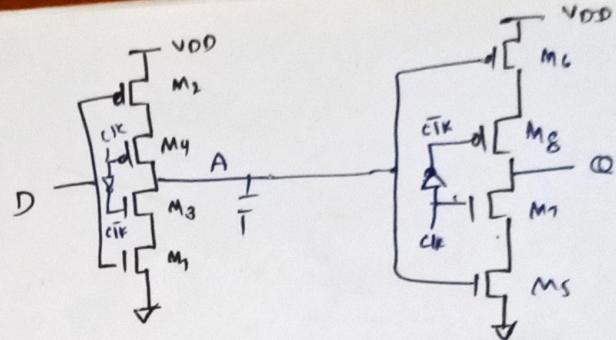


low level * Inverting Latch



CLK = 0

$A = \bar{D}$ $Q = Q_{\text{(odd)}}$ (latched)
 (prev value)

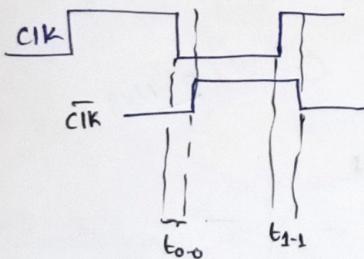


CLK = 1

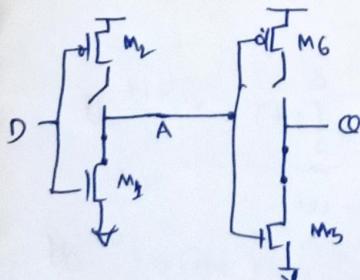
$A = A_{\text{(prev)}}$ $Q = \bar{A} = D$

(Becomes +ve edge triggered)

* cpl (problem) \rightarrow In overlap if input changes \Rightarrow output will get change.



$t-11$ (both $clk = 1$)
 $\bar{clk} = 1$



if $D = 1 \rightarrow 0$
M1 \rightarrow off
A \rightarrow latched
so, Q \rightarrow latched

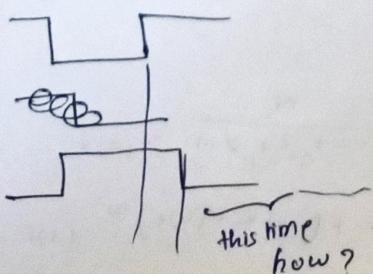
& if $D = 0 \rightarrow 1$
M1 \rightarrow on
A \rightarrow discharging
Means (A : 0 \rightarrow 1)

$\therefore M_5$ is off

$\therefore Q \rightarrow$ latched

M6 turns on
 \Rightarrow but since M8 is already off
so latched (Q).

After t_{11} how switches will behave?



this time how?

Here after ($\overline{Clk} = 1$ & $\overline{Clk} = 0$)

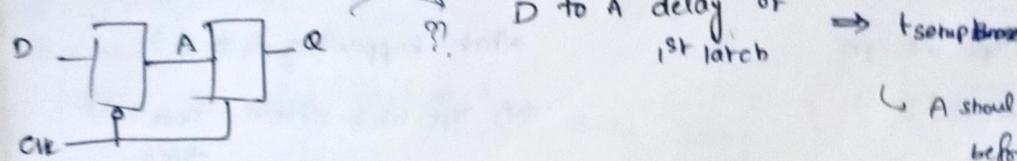
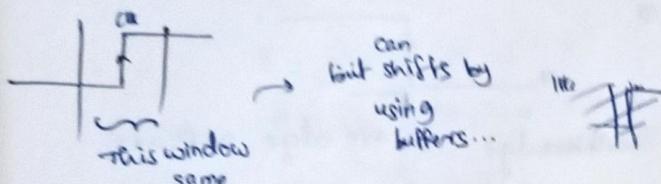
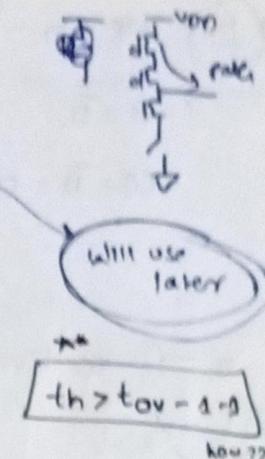
M_1 & M_2 both ON

$\therefore Q \rightarrow$ becomes 1

because of path from VDD to $Q \cdot h$

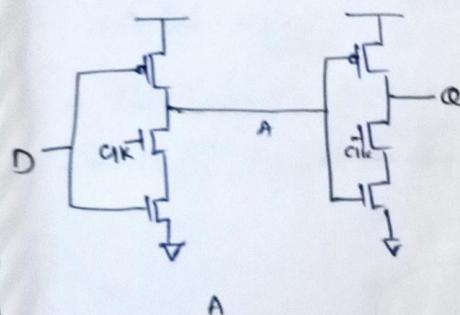
for what time after clock edge arrives we shouldn't change D ??

??



A should be ready before Clk edge

True single phase clock Latch/ff: (TSPC)

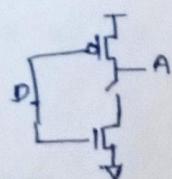


A

(three level sensitive latch)

if $Clk = 0$ & $D = 0$

that switch will be off



then Q will be

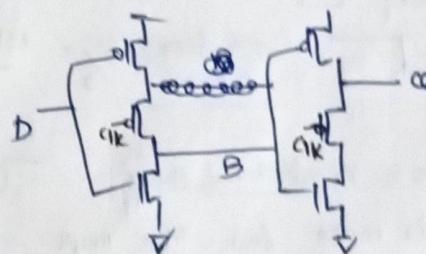
$A = 1$
then
 $Q \Rightarrow$ latched

if $Clk = 1$

$A = \bar{D}$

$Q = \bar{A} = D$

$Q' = D \checkmark Clk = 1$



B
(-ve level)

$D = 1$

$A =$ latched

$Q =$ latched

$Clk = 0$

↓

$Q =$ latched

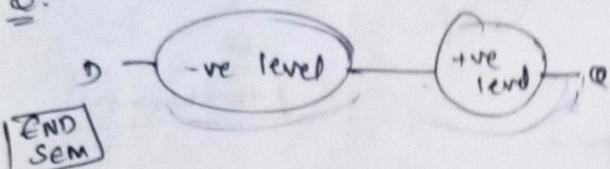
B

$$\text{CLK} = 0$$

$$B = \bar{D}$$

$$Q = \bar{B} = D$$

Q:



$$\text{CLK} = 1$$

$$D = 0$$

$$D = 1$$

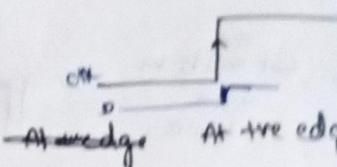
$$A \rightarrow 0$$

$B = \text{latched}$

$Q = \text{latched}$

$$B = 0$$

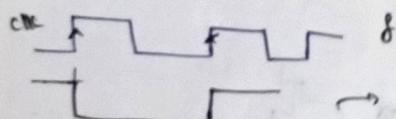
$Q = \text{latched}$



→ TSPC is preferred.
TSPC latch others does hold time t_{HOL}

for high speed FFlops design

TSPC is preferred.

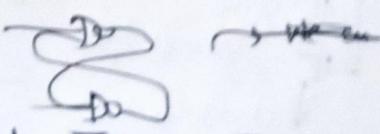


$$\rightarrow \text{freq} = f_{1/2} = \frac{\text{CLK freq}}{2}$$

→ with gates & traditional styles

we can't make fast like loops

$\xrightarrow{\text{loops}}$ $\xrightarrow{\text{T period}}$



delay should be less than Tclk

so not possible using these

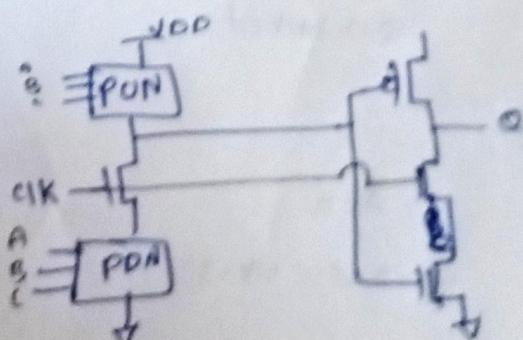
use TSPC

less no. of transistors

less Area &

can insert / add logic to latch

Adding logic to latch:



Clk = 1:

$A \rightarrow$ output (func' of PDN & PON)

$$Q = A$$

Clk = 0

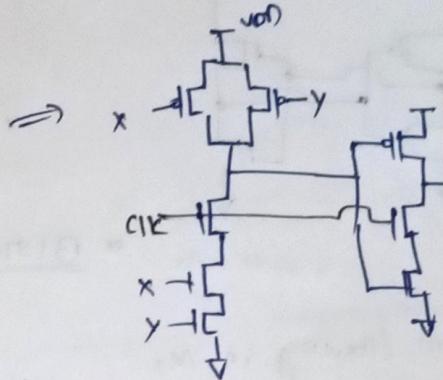
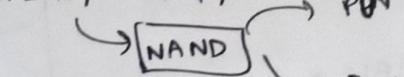
$Q \rightarrow$ latched to prev value

Now I want $Q = XY$ (AND of x & y)



$$\bar{A} = XY$$

$$A = \bar{X}Y = \bar{X} + \bar{Y}$$



####

TO make

$A \oplus B$ try using A, \bar{A}, B, \bar{B} already there

using these

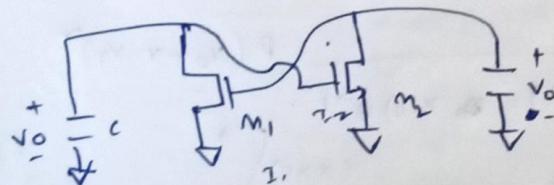
** JMP **

LJSPICE
???

- see circuits → timing analysis
- math path logic design → latches / FF
- logic styles → static → dynamic
- verilog / RTL / HDL

Differential logic

use mosfets as amplifiers



$$V_o > V_T \text{ (Given)}$$

Voltage V_o will start discharging.

• V_o will get reduced to some value less than V_T

Saying
 $V_1 > V_2$

$$V_1 = V_o + n$$

(both greater than V_T)

both discharges

if gate voltage higher , I higher current

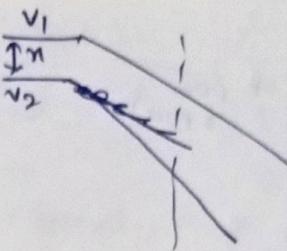
$$V_2 = V_o - n$$

I_2 should be greater than I_1

I_2 is higher

The difference keep on rising

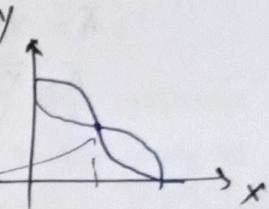
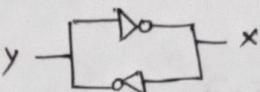
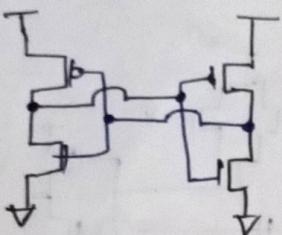
kind of Amplification (on n)



Rising gap b/w them
⇒ Widening ∞

13-11-24

Differential Lo



* BISTABLE *

Current flowing in M₁,

$$I_1 = -c \frac{dV_1}{dt}$$

$$I_2 = -c \frac{dV_2}{dt}$$

$$I_1 - I_2 = -c \frac{dV}{dt} (V_1 - V_2)$$

$$= -2C \frac{dx}{dt}$$

$$B(V_2 - V_T)^2$$

$$B(V_0 - x - V_T)^2$$

$$B(V_0 + x - V_T)^2$$

Assumed saturation

Interview Question

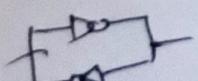
V_1 & V_2 are same
this point is called Meta-stable point

$$\Rightarrow x(t) = x(0) e^{\alpha t} \quad (\alpha > 0)$$

ENDSEM

? something said

We saw ?



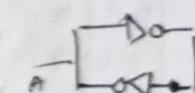
Same Analysis on with time

Take PMOS also //

The voltage through M₁ & M₂

$$\text{if } V_A > V_B \\ V_A =$$

This prop use to build some



1 & 3

Small change will no

$$A = 0, 0.1$$

$$B = 9.817$$

How plot do it

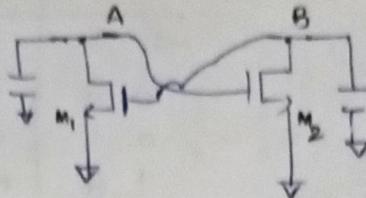
From this latch

$$f = A$$

$$I_w$$

13-11-29

Differential logic:



Saturday
11
classphara

Using gap b/w them
+ Widening E

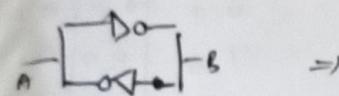
The voltage will discharge
through M_1 & M_2
& becomes zero

if $v_A > v_B$

$$v_A = v_B + \Delta x$$

B will discharge fast

This prop used
to build some circuits.



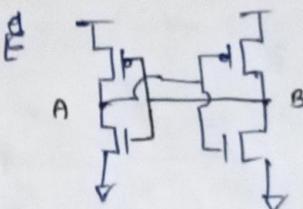
1 & 3 are stable points

Small change happens in v_A & v_B in ① & ③ point
will not change it

$$A = 0, 0.1 \equiv 0$$

$$B = 0.9 \text{ or } 1.8 \equiv 1$$

How plot comes?
do it own *



$$\text{let } V_{DD} = 1.8V$$

0.9V \Rightarrow becomes 0.85 like due to noise

This point
goes left or right due
to some noise. *

Then our output
goes to either 1 or 0
due to smaller ΔV

Metastable

Mean output = 0 (or) 1

From this latch, we can use in circuits - 4

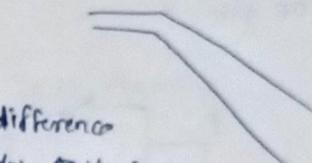
$$\delta = A \cdot B$$

I want

Differential
CMOS logic

\Rightarrow using this latch

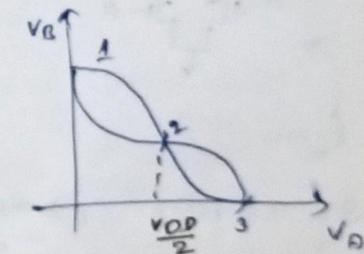
latch ensuring 'in & out' matter 0 1 & 1 0 immediately

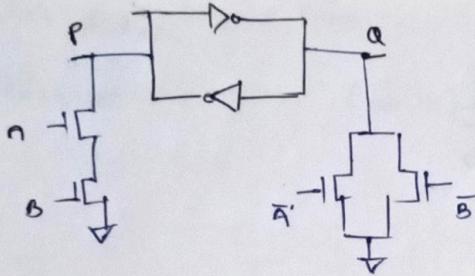


difference

b/w v_A & v_B

Use exponentially
 \rightarrow derived already





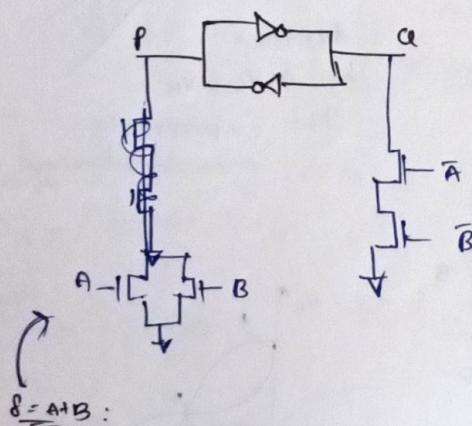
We will get
both AND
& NAND

A	B	P	Q
1	1	0	1
0	0	1	0
0	1	1	0
1	0	1	0

$$P: \text{NAND} \Rightarrow \bar{A}\bar{B}$$

$$Q: \text{AND} \Rightarrow AB$$

Do OR gate : ?



$$S = a\bar{b} + b\bar{a}$$

implement using
differential CMOS logic?

[ENDSCM]

To make this
circuit clock sensitive:

$$\text{if } \phi = 0$$

$$M_3 \Rightarrow \text{open}$$

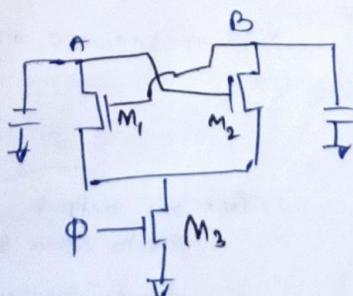
leakage happens

on a period of time \Rightarrow it will get discharge $A + B \cdot t$

if $A \neq B$ same & all identical

A, B goes to zero

$$\text{Clk} = 1$$



but here $\text{Clk} = 1$ comes again

But we assumed
 $M_3 \Rightarrow \text{off}$ means
open
NO leakage

if $A \neq B$ are not same & all ident
difference \uparrow & which (like amplifier)

New circuit

$$\begin{aligned} \phi &= 0 \\ D &= 0 \quad D = 1 \end{aligned}$$

$$\begin{aligned} \phi &= 1 \\ D &= 0 \quad \Rightarrow \text{The} \end{aligned}$$

$$\begin{aligned} V_A &=? \\ V_B &= q \end{aligned}$$

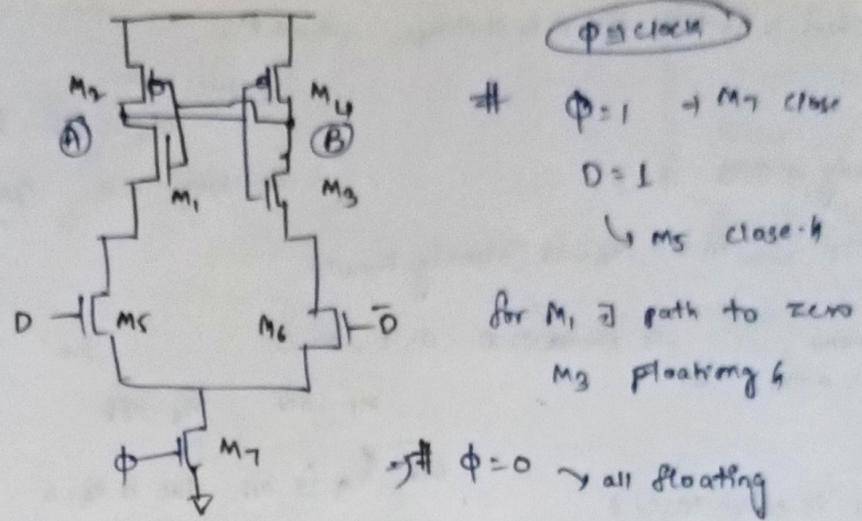
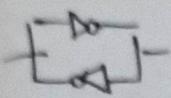
$$\begin{aligned} \text{Now } D &= 0 \\ M_5 &= \text{off} \end{aligned}$$

✓
A some
leakage
due to

$$\begin{aligned} \text{Now } D &= 1 \\ \phi &= \end{aligned}$$

$$\begin{aligned} \downarrow \\ V_A = \end{aligned}$$

if in Evaluation
phase
 D change
 $D \Rightarrow 0, 1$



New circuit

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	0	0
1	1	0	1

$$P \Rightarrow \text{NOR}$$

$$Q \Rightarrow \text{OR}$$

$$\begin{array}{ll} \Phi = 0 & \Phi = 1 \\ D = 0 & D = 1 \end{array}$$

$$\begin{array}{ll} \Phi = 0 & \Phi = 1 \\ D = 0 & D = 1 \end{array}$$

$\Phi = 0$ (Precharge)

V_A & V_B charges to V_{DD}

$M_1 = \text{off}$ if $D = 0$

V_A & V_B hold only (No change)
in V_{DD}

$$\begin{array}{l} \Phi = 1 \\ D = 0 \end{array} \Rightarrow \text{Then,}$$

$$\text{Here } \Phi = 0 \rightarrow 1, D = 0$$

$$\Phi = 1 \Rightarrow M_7 \text{ on}$$

(M_8 & M_9 are off)

V_A & V_B initially 1

↙ NMOS of both inverters (M_1 & M_3) are ON.

Now $D = 0$

$M_5 = \text{off}$

$M_6 = \text{on}$

↙ A some leakage due to

↙ B will discharge quickly

B voltage decreases fastly

↙ But there is a LATCH

due to butterfly it goes to 1 or 0.4

$$V_A = 1, V_B = 0$$

$$\begin{array}{l} \text{Now} \\ D = 1 \end{array}$$

$$\Phi = 0 \rightarrow 1, D = 1 \quad V_A = ? \quad V_B = ?$$

$$V_A = 0, V_B = 1 \quad \text{H}$$

if in Evaluation phase

D changes

$$D \Rightarrow 0 \rightarrow 1$$

$$D = 0, \bar{D} = 1$$

$$M_5 = \text{off}, M_6 = \text{on}$$

$$V_A = q, V_B = 0 \text{ already}$$

so same

lk = 7 always eighth

assumed
 \Rightarrow off means open
on means close

3 There is no path for A to discharge, $A = 0 \vee$

↳ due to this:

M_3 is off \therefore

\therefore No change in B (No path for B also)

already $\Rightarrow D = 0, \phi = 1$

$V_A = 1, V_B = 0$ (already known)

Now
charging
 $D = 0 \rightarrow 1$

$\Rightarrow D = 1, D = 0$

M_5 - ON M_6 - OFF

SAME

This is edge triggered
(true item)

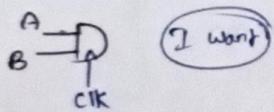
EDGE TRIGGERED

LOGIC

But M_2 is off due to $V_B = 0$

No path to discharge \therefore same output

Fig 9 KRL

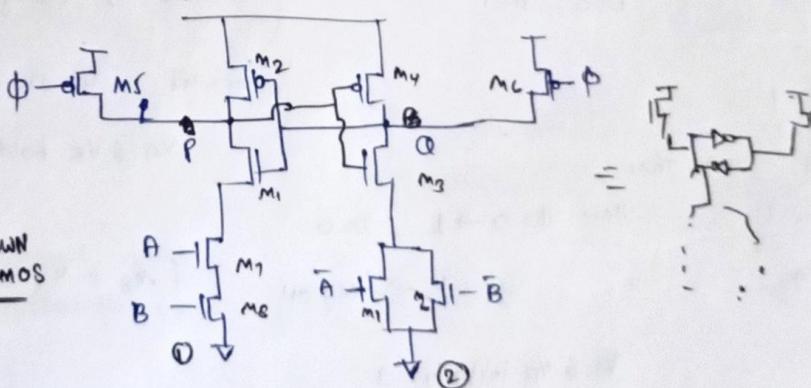


Analyse this
without
DOWN NMOS

$\phi = 0$

P & Q becomes 1 \Rightarrow

If down paths are not on *



If path there to discharge \rightarrow P & Q tries to discharge \therefore

$\underline{Q=1}$

if ① 1 $A = 1, B = 1$

$P = 0, Q = 1$

others $\begin{matrix} A = 0 \\ B = 0 \end{matrix}$

$Q = 0, P = 1$

if we do precharge

• $P \& Q = 1$

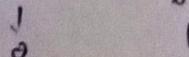
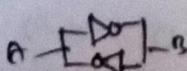
& $\phi = 1$ we evaluate

P: NAND $\Rightarrow \bar{A}\bar{B}$

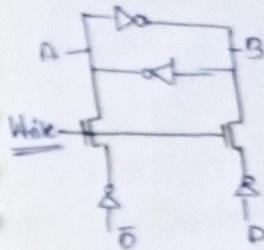
$Q = \text{AND} = AB$

We shouldn't have
path in precharge
to discharge by correct sizing

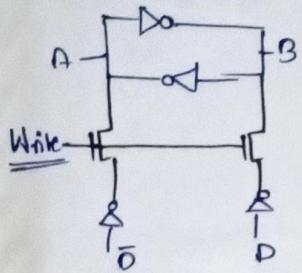
This is
Also edge triggered



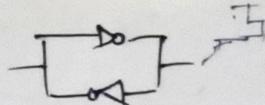
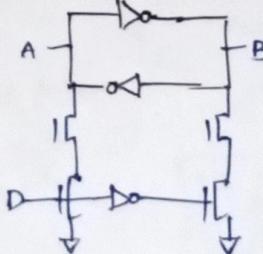
How to write particular logic



How to write particular logic at a node?



\Rightarrow



DO OR
NOR ??

XOR = ?
XNOR = ?

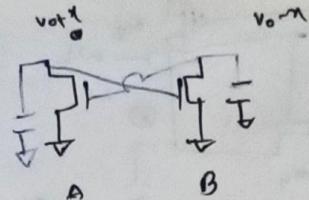
$\phi \Rightarrow \phi'$ is given
Replace

key, acts ... ?

⇒ Recap:

→ Differential logic

①



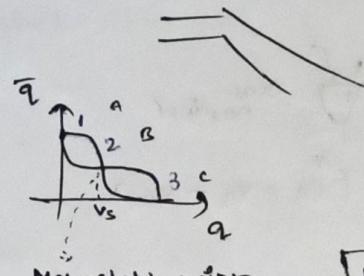
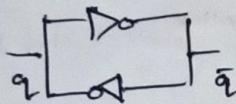
difference voltages

(6-11-24)

• due to V_{out} high

• B transistor more current & fast decaying

②



Amplifying differencing voltages //

at point A & C

$$A: \bar{Q} = 1, Q = 0$$

$$C: \bar{Q} = 0, Q = 1$$

1/3 are Stable States

B: Metastable perturbation

if at ② point we did $V_s + \Delta V$

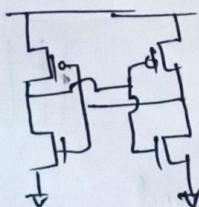
it will go to c //

How can we write in latch??

RAM ??

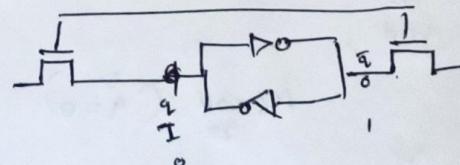
"Access" TRANSISTORS

??



If we enable transistors:

Reading: we will add some circuit



$\frac{G}{T}$
RAM 1

There might be a path from latch

to discharge (O) to set charged up //

(due to some connected circuit)

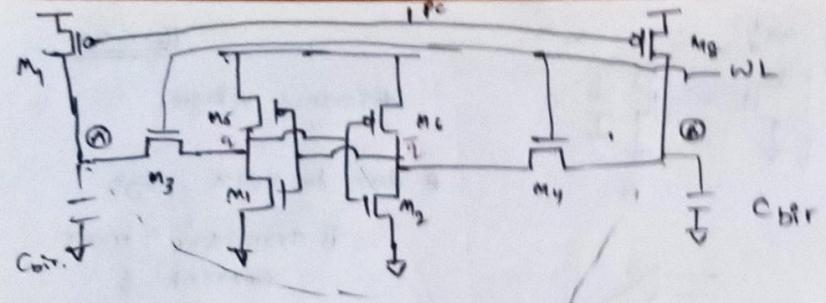
⇒ may not remain necessarily at same value!!

if it is near 0
then

if ensure Q & \bar{Q} change should be very small and shouldn't be too large & near to 1/2

write: If we want to write "0" & "1" then

We have to produce difference at V_s , so that switching happens,



If $PC = 0$, $WL = 0$
 PMOS turns ON
 $C_{bit} \Rightarrow$ precharges to V_{DD} ($V_A \approx V_B \approx V_{DD}$)

* $PC = 1$ &
 $WL = 1$
 $\Rightarrow M_3 \& M_4 \Rightarrow$ turns ON

* when $\bar{q} = 1 \Rightarrow M_1 = ON$
 $q = 0 \quad M_2 = OFF$
 N_{DD} at A
 $\rightarrow M_3 \& M_4$
 ON

\Rightarrow can be a path A to ground

\Rightarrow No path from B to ground

* B \Rightarrow maintaining its value

A \Rightarrow is decreasing #

if metal length very long \Rightarrow overall parasitic cap /edge \Rightarrow that cap to discharge \Rightarrow takes more time \Rightarrow memory access becomes slow

so sense Amplifier \rightarrow if difference

~~discharging structure~~ (Amplifies the difference)

$$A = V_{DD} - V_A$$

$$B \approx V_{DD}$$

$A \approx$

sense Amplifier

we will get in short time one output /

gives either $0 \text{ or } 1$

✓ LESS TIME !

READ operation

\Rightarrow parasitic capacitance

1st step

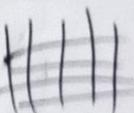
q, \bar{q}

voltage should not change

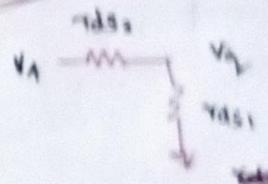
How can we read?

Let $q = 0, \bar{q} = 1$

(already stored)
 we have to read this



Memory
 \downarrow
 address
 sensing ampl



$\# q_{dd} \leq \# q_{ss}$

* $q_{dd} \approx 4 q_{ss}$

Cell high

V_r
 after slow

EAD operation

parametric
capacitance

1 bit info

q, \bar{q}

can't charge M_2

How can
we read?

$v = 0, q = 1$
(already stored
here to read the
data)

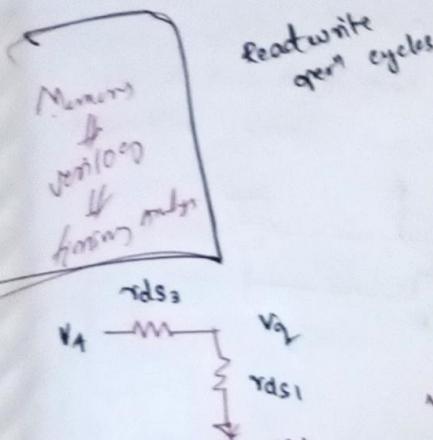


initially $q = 0$
flip turns ON
 $V_Q = ?$ what happens *

$M_3 \rightarrow$ conductance
 \rightarrow resistance R

q should now be greater than zero

** V_Q will rise!! *



$$r_{ds1} \approx \frac{r_{ds3}}{4}$$

$$I_{ds1} \approx 4 I_{ds3}$$

Can be done
by sizing

1 bit
high

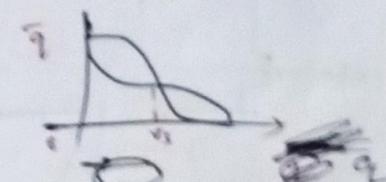
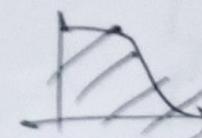
get slow

should be finished
in next repetition
so sense amplifier * fast

(voltage diff
must
be small
to read
do slow)

QFP

Can't be



** read
open *
it shouldn't
increase
till V_S (great
extent)

$$V_Q = \left(\frac{r_{ds1}}{r_{ds3} + r_{ds1}} \right) V_A \quad \text{if order is 4-5 times by } r_{ds3}$$

$$V_Q = \frac{1}{4} - \frac{1}{5} V_A$$

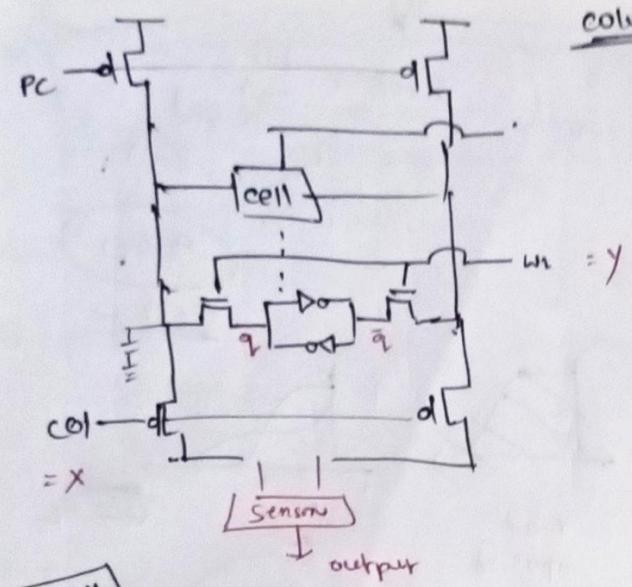
$$\therefore V_Q = \frac{1}{5} V_A \cdot H$$

$$\frac{V_A}{5} \Rightarrow \frac{V_{op}}{5}$$

If smaller
than V_S

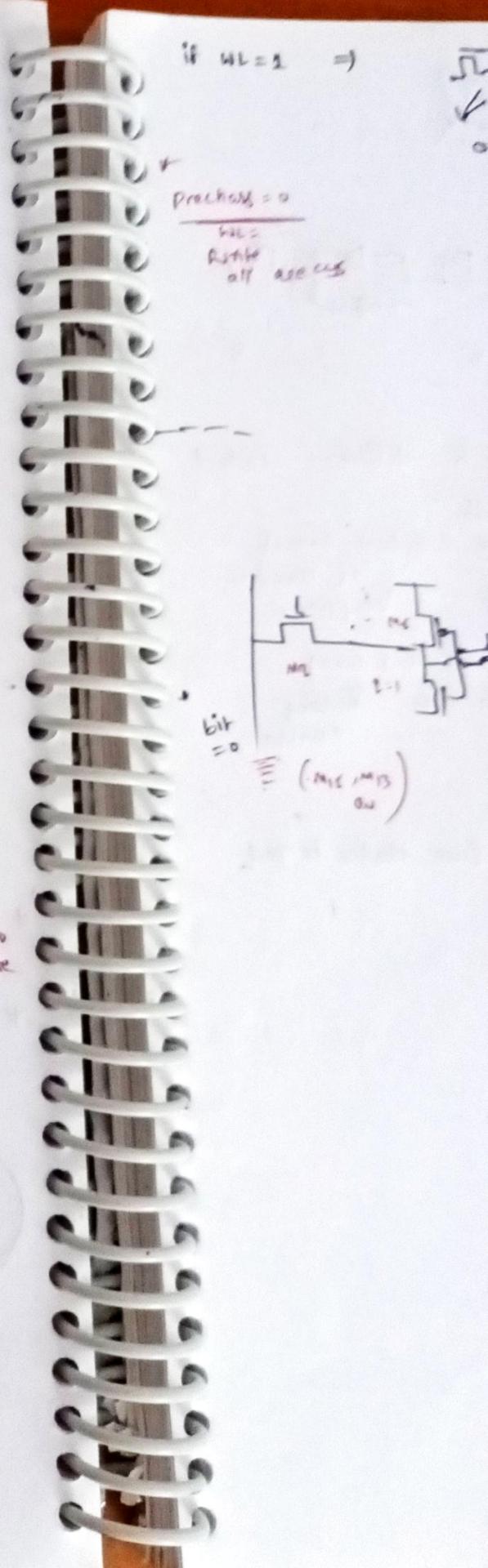
We have no problem
Q2 slower

$\Rightarrow V_Q = \text{const}$
Choose M_1 & M_3 sizing
s.t.
 V_Q rise will be
less than
 V_{op} of M_2 , i.e.



column cell

y, \bar{y} selects
difference to
Sensors
output \Rightarrow



if $WL = 1 \Rightarrow$

Precharge = 0
 V_{DD}
RST =
all access

END SEM

PC
pre charge

Write opern

$q = 1, \bar{q} = 0$ (it has)

we need to change them to $q = 0, \bar{q} = 1$ ✓ 😊

$D = 0 \rightarrow$ we have to write



$M_{13} \Rightarrow ON, M_{14} = OFF$



V_{bit} will start discharging

$V_{\bar{bit}}$ stays at V_{DD} only

Since M_{14} off



⇒ Enable that cell where we want to write

$WL = Y \dots$ ✓

$WT = 1 \rightsquigarrow$
↓ start
↑ always
precharge happening

bit & \bar{bit} pre charged to V_{DD}

$COL = 1$

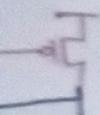
$\Rightarrow M_{15}$ turns on

Apply D & WR signals

xy selects

difference to
baseline
↓
input V_{in}

pass to pr
same voltages



$WT=1 \rightarrow$
we want to
write

Same level
bit & bit

pre charged
to V_{DD}



M_{15} turns on if

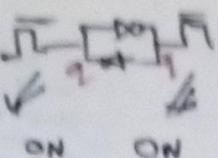
& wr signals

If $WT=1 \rightarrow$

precharge = 0

$WT=1$
 $M_{15} = 1$

$M_{15} = 1$ $M_{15} = 1$



ON ON

V_q will start discharging



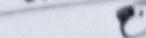
if q goes discharge to V_{DD}

\approx charging

M_{15}

down

size matters



due to feedback

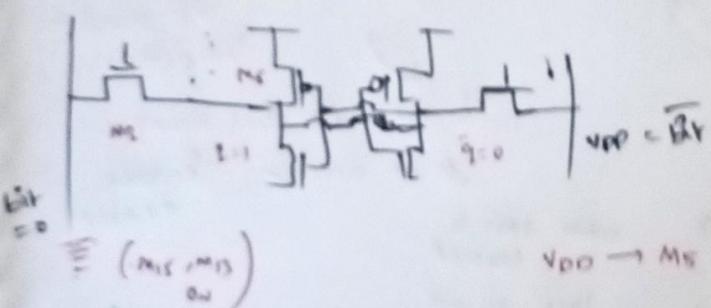
q will end up with 0

q will be 0 only

write over



M_{15} & M_{15} should be
good enough size to
get fast
discharge

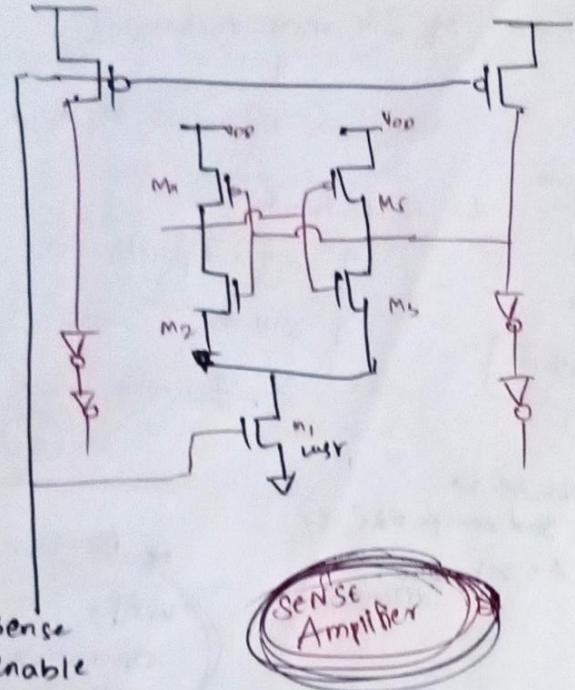


$V_{DD} \rightarrow M_5 \rightarrow M_3 \rightarrow q = 0$
path if $WT=1$

$M_5 \Rightarrow$
push
charge
to q to get
 $q \Rightarrow$ discharge path
 M_3

M_3 should win

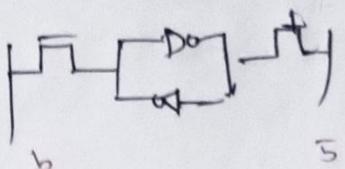
* M_3 should
be 4-5 times larger than M_5 . If
then q will get to zero. (frowny face)



sense enable

Sense Amplifier

sense enable



b & b - difference started

↓
some significant amount
of switch happens

If then (at that time)
& we enable sensing enable

when this is
enabled

laser is on

y will a path from nodes to ground.

Case 1: $b < b$ \Rightarrow

* M_2 will conduct faster
than M_3

\downarrow
 b discharges fast //

so, b becomes 0

[read open?]

& b becomes 1 //