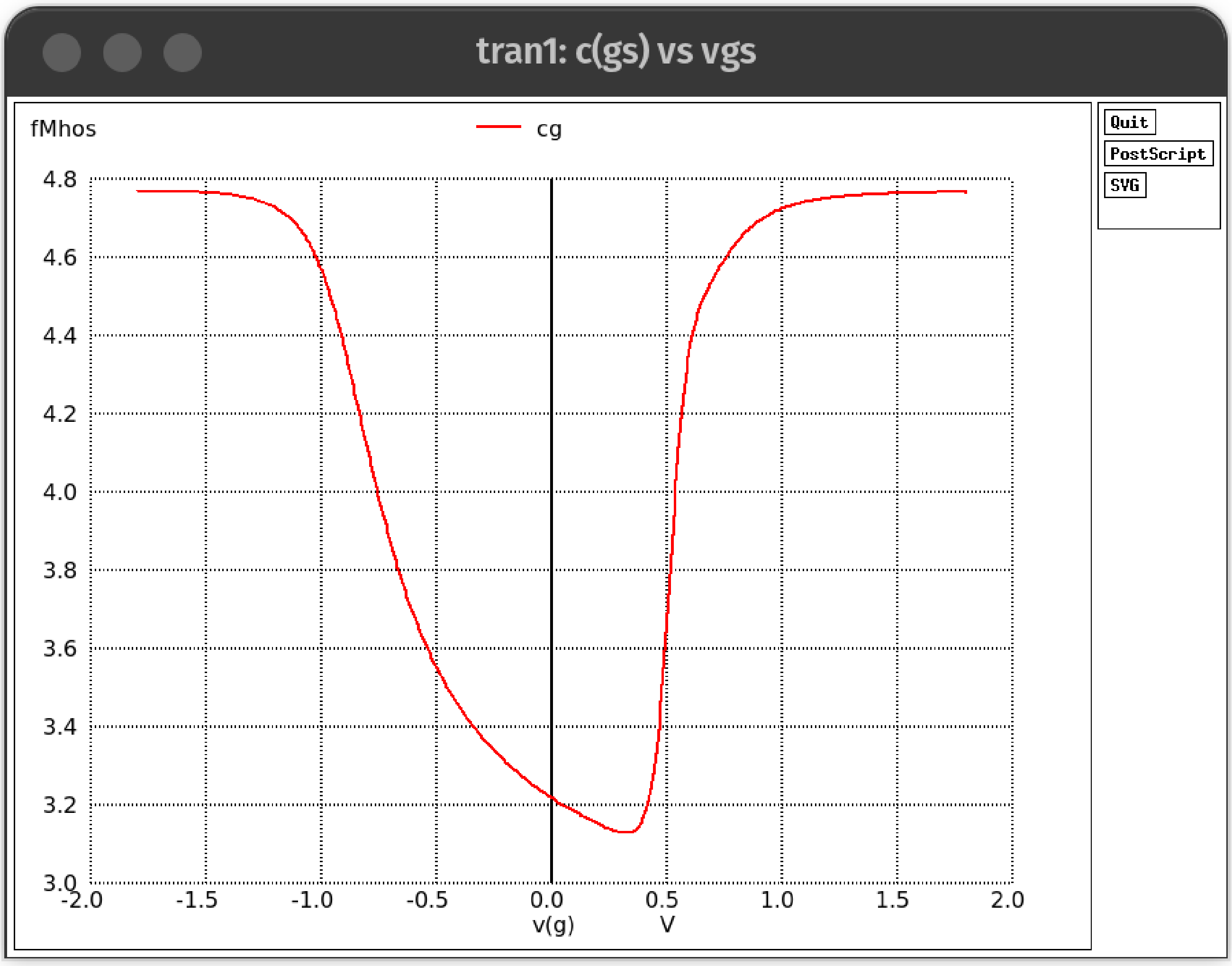
VLSI ASSIGNMENT 1

NITIN RAM SAI G

`2023112026`

QUESTION 2,3,4,5: Handwritten solutions attached at the end of this PDF

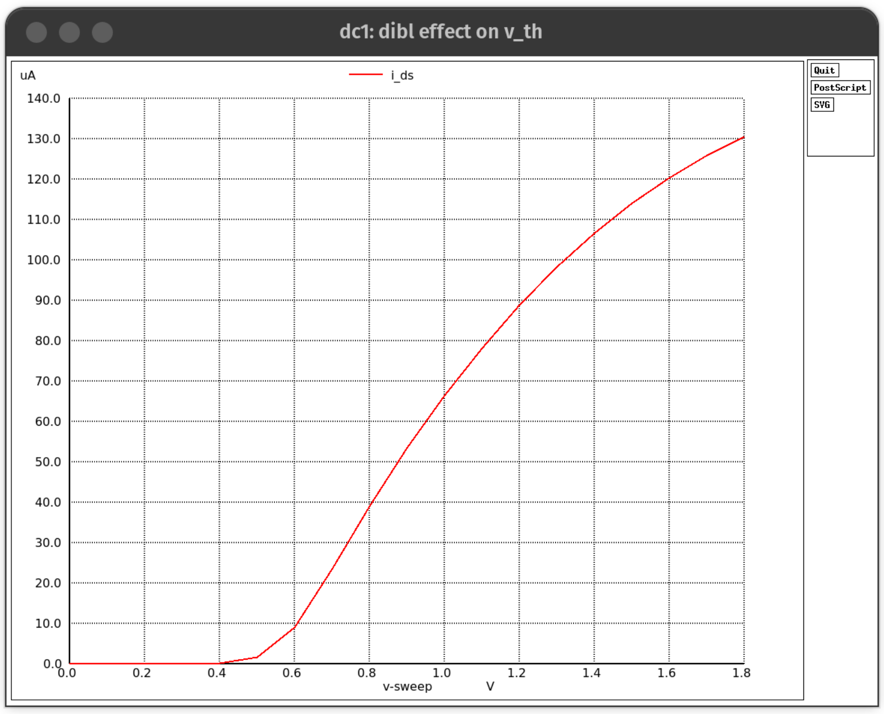
QUESTION 4:

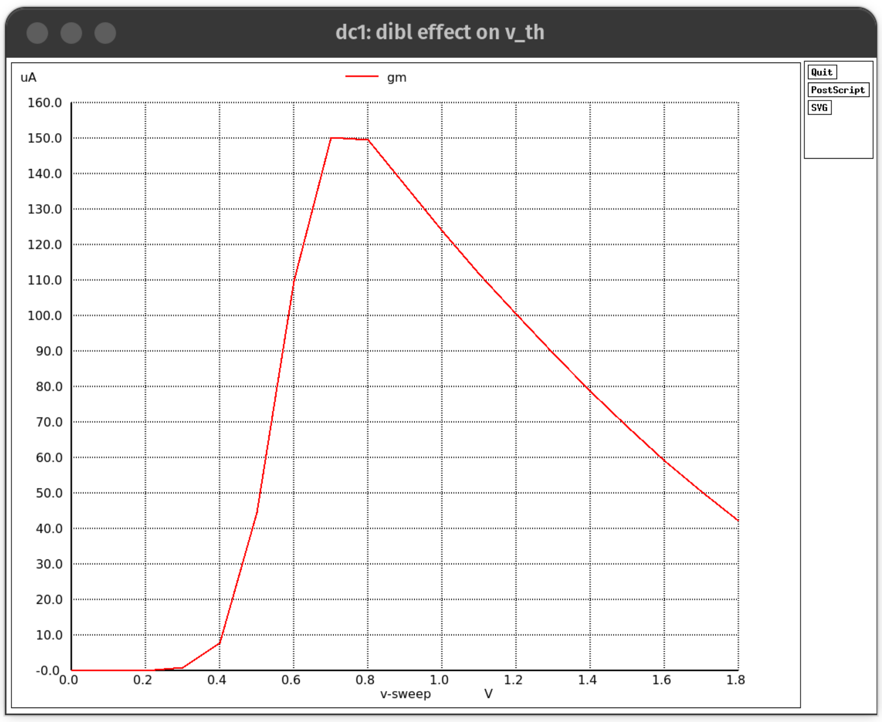


QUESTION 6:

PLOT I_D vs V_{GS} of a NMOS and estimate V_{Th} for

A] V_{DS}= 50mV and V_{DS} is swept from 0 to 1.8V (step 0.1V)





- From the above plot ,we observe that the curve inititally is in Cutoff → Saturation →Linear Region.

> 💡 STEPS TO EXTRACT V_{Th}:
>
> 1. To avoid Second order effects ,we prefer linear region.
>   a. $I_{DS} = \mu.C_{ox}.\frac{W}{L}.((V_{GS} - V_{Th}).V_{DS} - \frac{1}{2}V_{DS}^2)$ in the linear region
> 2. Draw a tangent at max-slope point & extrapolate ,the x-intercept is our threshold voltage

From NGSPICE,

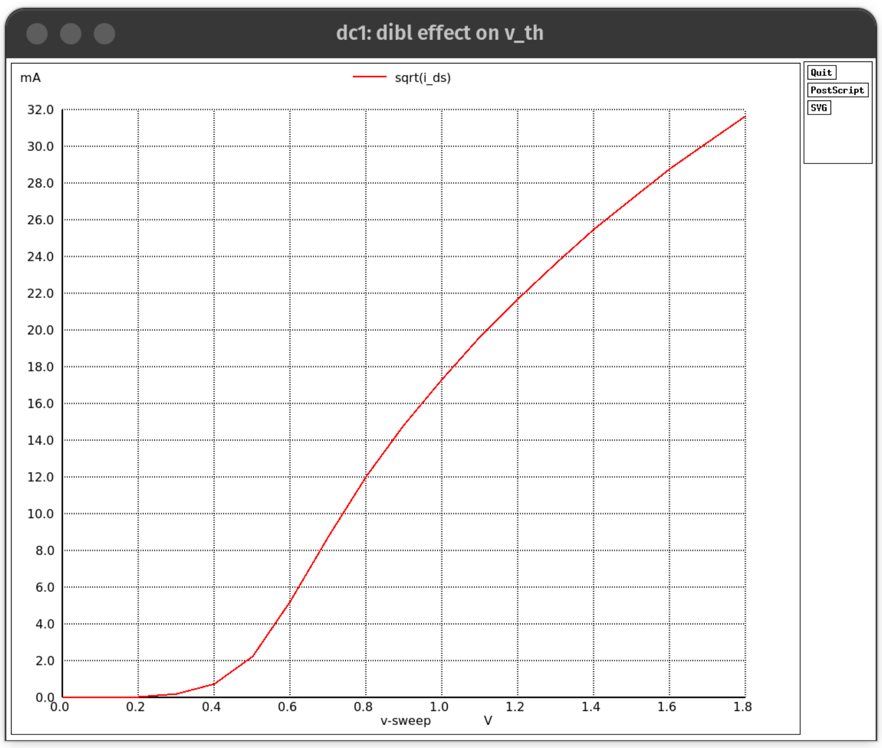
we get g_m = 0.000150104 which is max. at VGS=0.7V

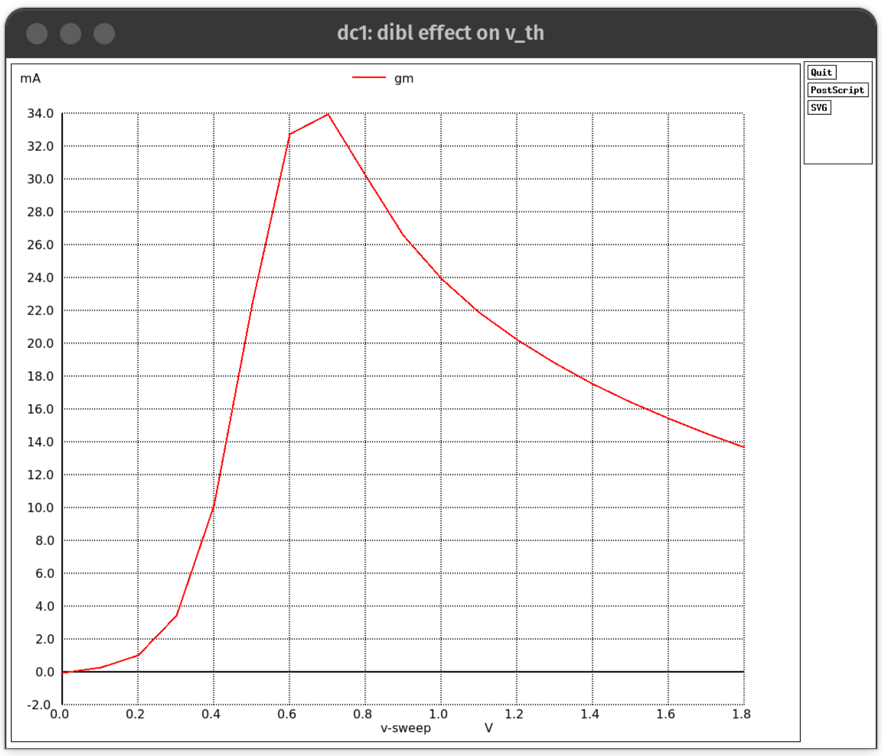
We also found I_{DS}=23.52778 μA , at max slope position VGS=0.7V

So solving line equations ,

we get V_TH=543mV

B] V_{DS}= 1.8V and V_{GS} is swept from 0 to 1.8V (step 0.1V)





In this case , we couldn't find a linear region as $V_{DS} = 1.8V$ & $V_{DS} > V_{GS} - V_{Th}$, So it is forced in Saturation Mode.

💡 STEPS TO EXTRACT V_{Th}:

1. Use current equation
   a. $I_{DS} = \frac{1}{2}.\mu.C_{ox}.\frac{W}{L}.((V_{GS} - V_{Th})^2.V_{DS}$ in the saturation region
   b. We also make derivatives wrt V_{GS} $notV_{GS}^2$ so take sq.root
   c. $\sqrt(I_D) = (\frac{\partial\sqrt{I_D}}{\partial V_{GS}})(V_{GS} - V_{TH})$
2. Draw a tangent at max-slope point & extrapolate ,the x-intercept is our threshold voltage

Max-slope co-ordinates: VGS = 0.700685V, max-slope value=0.0339318

I_DS=77.81170 μA at the same VGS

VTh_new=441mV

C] Do you observe any difference in V_ T values in case (a) and (b) ?

Yes, there is a difference in the V_T (threshold voltage) values observed in cases (a) and (b):

- Case (a): V_TH = 543 mV
- Case (b): V_TH = 441 mV

The difference in threshold voltage values can be attributed to the different operating conditions and extraction methods used in each case:

- In case (a), V_T was extracted using the linear region of operation with V_DS = 50mV
- In case (b), V_T was extracted using the saturation region of operation with V_DS = 1.8V

This difference demonstrates the impact of drain-induced barrier lowering (DIBL), a short-channel effect where the threshold voltage decreases as the drain voltage increases.

SCRIPTING CODE:

```
DIBL effect on V_Th

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS G gnd 'SUPPLY'
VDS D gnd 1.8V

M1    D     G     gnd    gnd  CMOSN  W={width_N}  L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VGS 0 1.8 0.1V
.measure dc current_at_slop FIND I(VDS) WHEN V(G)=0.700685
.control
set hcopypscolor = 1
set color0=white
set color1 = black

run
let I_DS=-VDS#branch
let gm = deriv(sqrt(-VDS#branch))
plot gm
*hardcopy a.eps
```

```
.endc
```

QUESTION 7:

FINDING MOS PARAMETERS ($\mu.C_{ox}$ & V_{Th}) in NMOS

In a NMOS ,the relation between Body Voltage and Vth is

$$V'_{Th} = V_{Th} + \gamma(\sqrt{-2.\phi_F + V_{BS}} - \sqrt{-2.\phi_F} \qquad \phi_{NMOS} < 0 \quad \gamma > 0$$

So we can claim that,

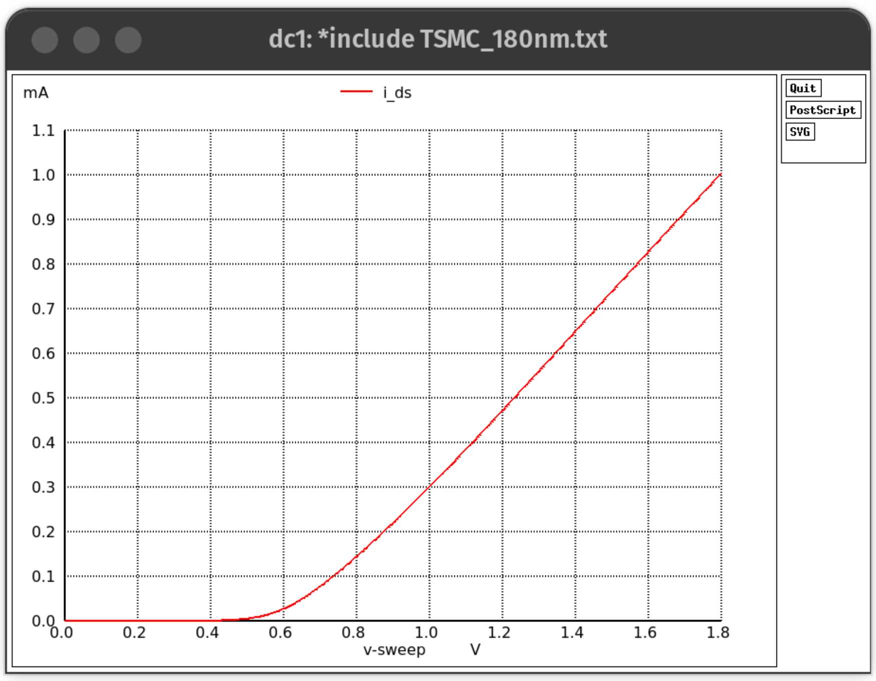
$$V_{TH,900mV} < V_{TH,0V} < V_{TH,-900mV}$$

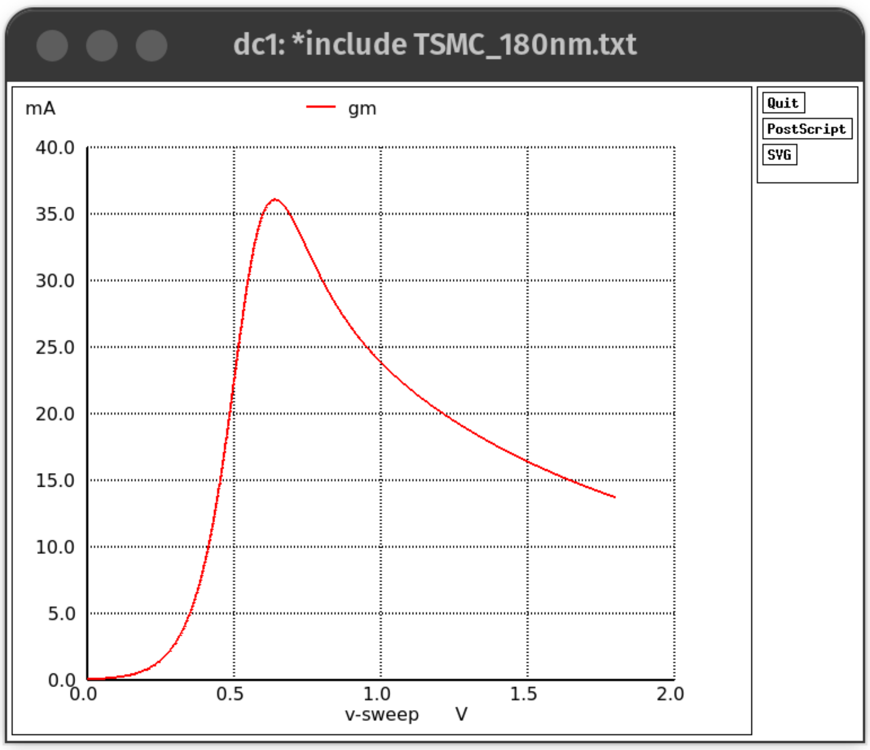
SINCE we have to test these various values ,we have to ensure VDS >max of all VT's to avoid p-n junction so that it behaves as wanted so VDS>900mV

VGS-0.55≤1.8 (always in saturation)

> 💡 STEPS TO EXTRACT V_{Th}:
>
> 1. Use current equation
>   a. $I_{DS} = \frac{1}{2}.\mu.C_{ox}.\frac{W}{L}.((V_{GS} - V_{Th})^2.V_{DS}$ in the saturation region
>   b. We also make derivatives wrt V_{GS} $notV_{GS}^2$ so take sq.root
>   c. $\sqrt(I_D) = (\frac{\partial\sqrt{I_D}}{\partial V_{GS}})(V_{GS} - V_{TH})$
> 2. Draw a tangent at max-slope point & extrapolate ,the x-intercept is our threshold voltage

A]VBS=0V

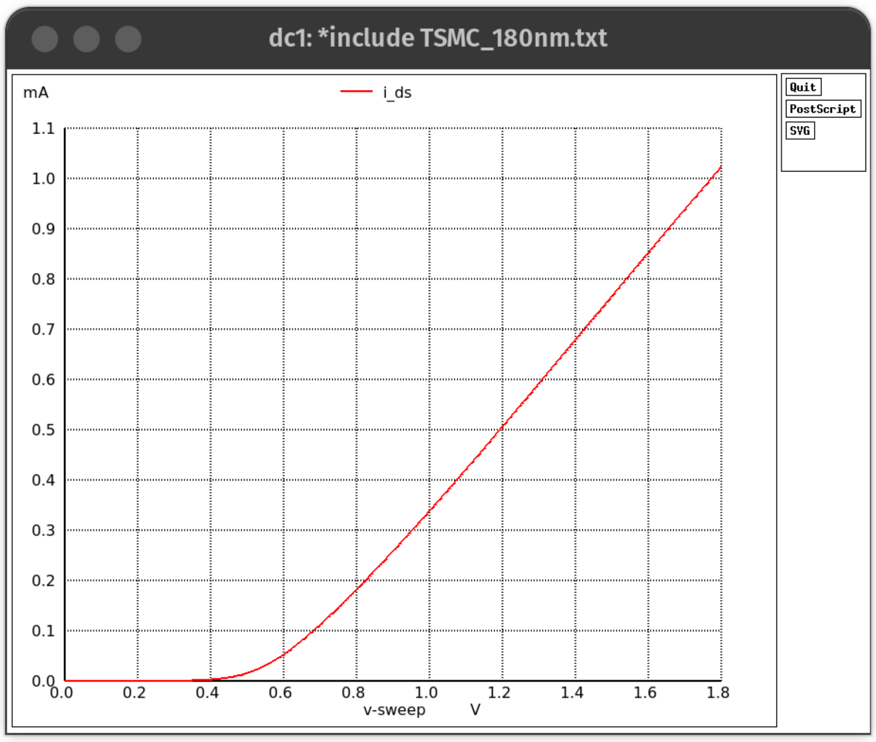


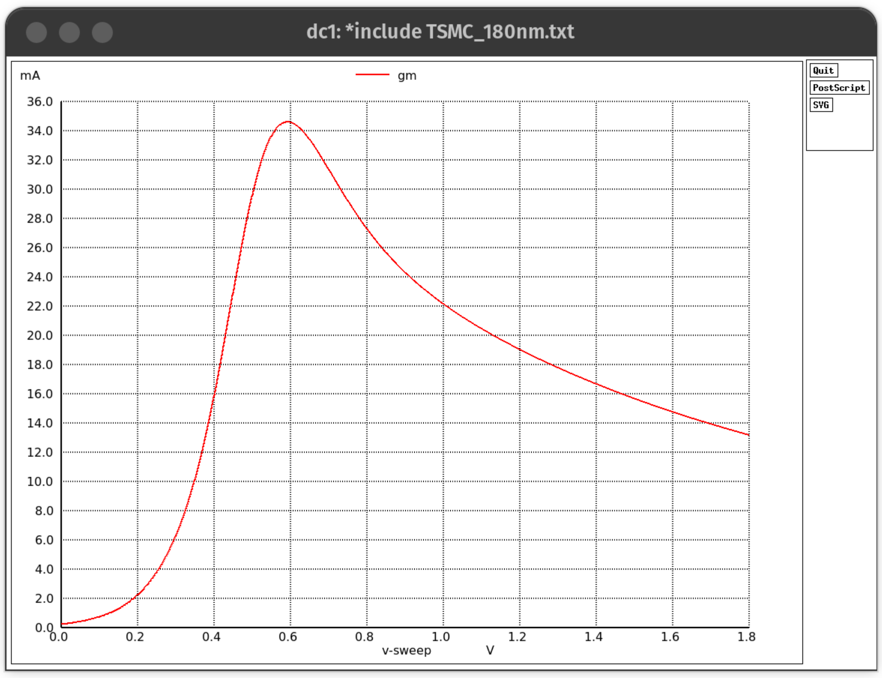



```
VGS for max slope= 0.636986, max_slope = 0.0360976 I_DS=42.97135 mu
V_TH=454mV
```

$\mu.C_{ox} = 1.302 * 10^{-4} A/V^2$

B]VBS=900mV

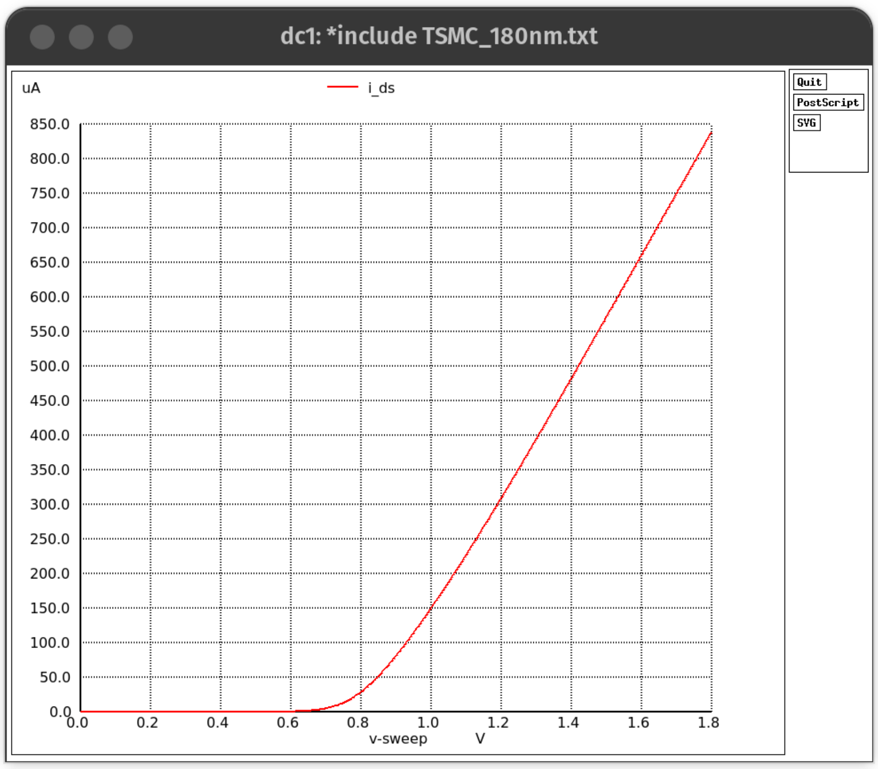


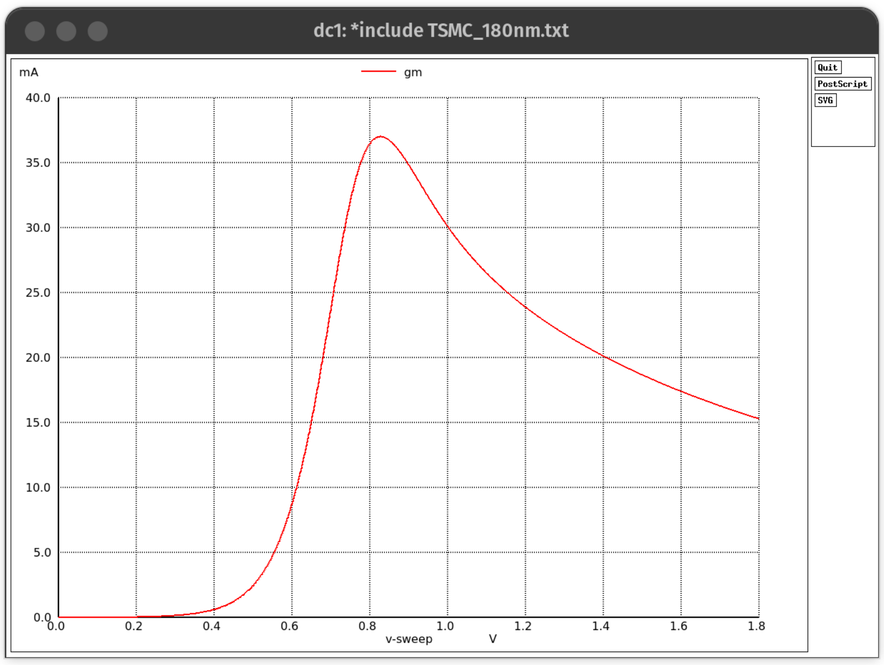



```
VGS for max slope = 0.585616,  max_slope= 0.0347045 I_DS=45.82876 mu
V_TH=389mV
```

$\mu.C_{ox} = 1.204 * 10^{-4} A/V^2$

C]VBS=-900mV






```
VGS for max slope= 0.826027, max_slope = 0.03705 I_DS=40.16905 mu
V_TH=654mV
```

$\mu.C_{ox} = 1.3727 * 10^{-4} A/V^2$

SCRIPTING CODE:

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd


VGS G gnd 'SUPPLY'
```

```
VDS D gnd 1.8V
VBS B gnd -900m

M1    D     G     gnd  B   CMOSN  W={width_N}  L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
.dc VGS 0 1.8 0.001V
.measure dc current_at_slop FIND I(VDS) WHEN V(G)=0.826027

.control
set hcopypscolor = 1
set color0=white
set color1 = black
run
let I_DS=-VDS#branch
let gm = deriv(sqrt(-VDS#branch))
plot gm
plot I_DS

.endc
```

FINDING MOS PARAMETERS ($\mu.C_{ox}$ & V_{Th}) in PMOS

In a PMOS ,the relation between Body Voltage and Vth is

$$V'_{Th} = V_{Th} + \gamma(\sqrt{-2.\phi_F + V_{SB}} - \sqrt{-2.\phi_F} \qquad \phi_{PMOS} > 0 \quad \gamma > 0$$

So we can claim that,

$$V_{TH,900mV} < V_{TH,0V} < V_{TH,-900mV}$$

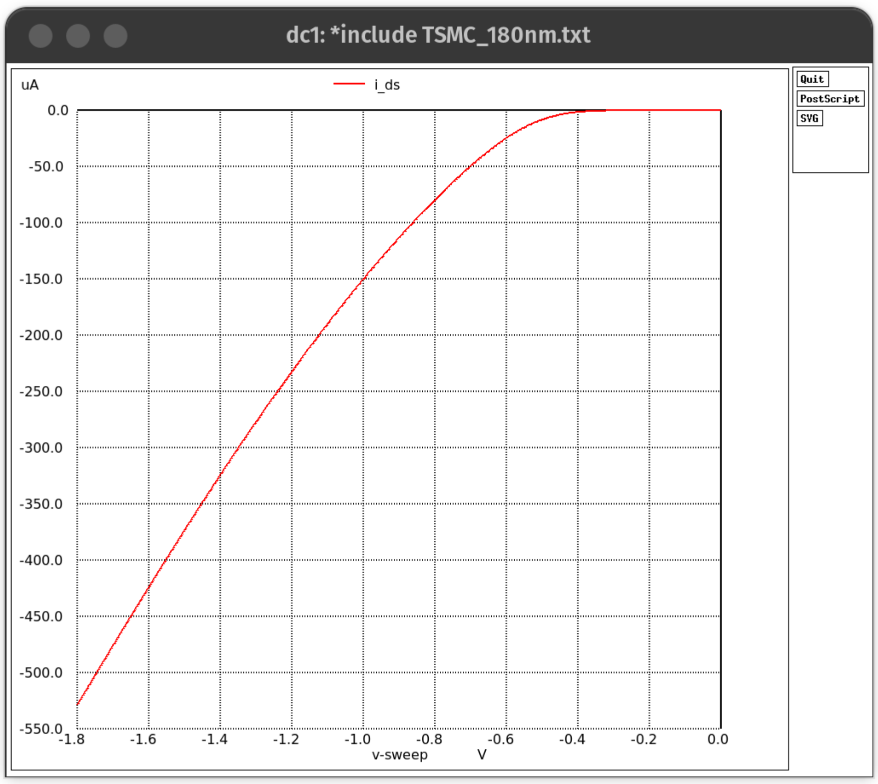
SINCE we have to test these various values ,we have to ensure VDS >max of all VT's to avoid p-n junction so that it behaves as wanted so VDS>900mV

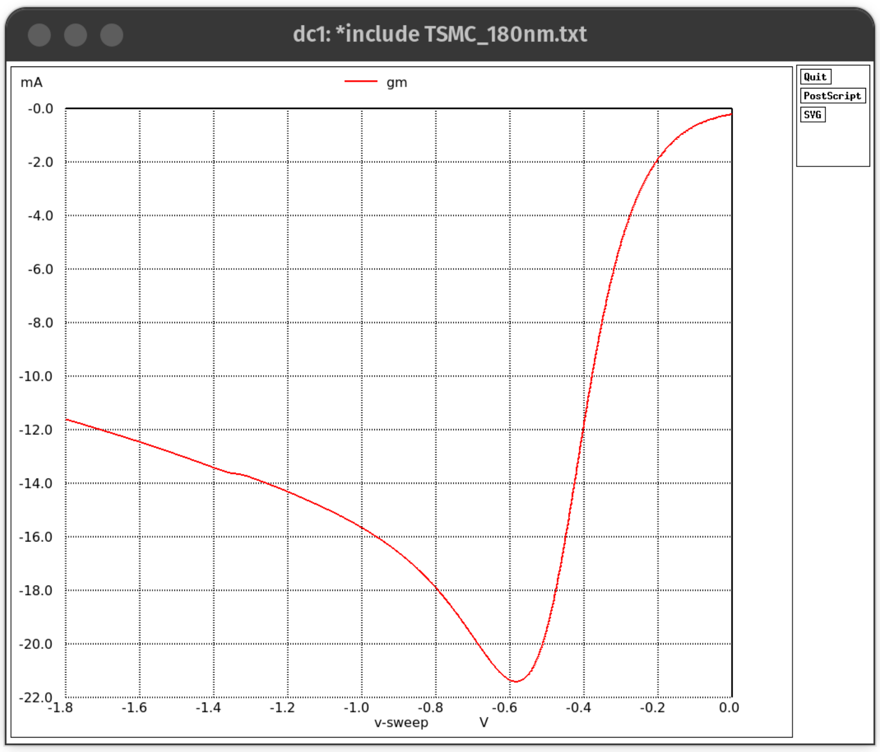
VGS-0.55≤1.8 (always in saturation)

> 💡 STEPS TO EXTRACT V_{Th}:
>
> 1. Use current equation
>   a. $I_{DS} = \frac{1}{2}.\mu.C_{ox}.\frac{W}{L}.((V_{GS} - V_{Th})^2.V_{DS}$ in the saturation region
>   b. We also make derivatives wrt V_{GS} $notV^2_{GS}$ so take sq.root
>   c. $\sqrt{(} - I_D) = (\frac{\partial\sqrt{-I_D}}{\partial V_{GS}})(V_{GS} - V_{TH})$
> 2. Draw a tangent at max-slope point & extrapolate ,the x-intercept is our threshold voltage

A]VBS=-900mV

```
VGS for max slope = -0.582877, max_slope = -0.0213857 I_DS=21.24191e-06
VTH=-366mV
```

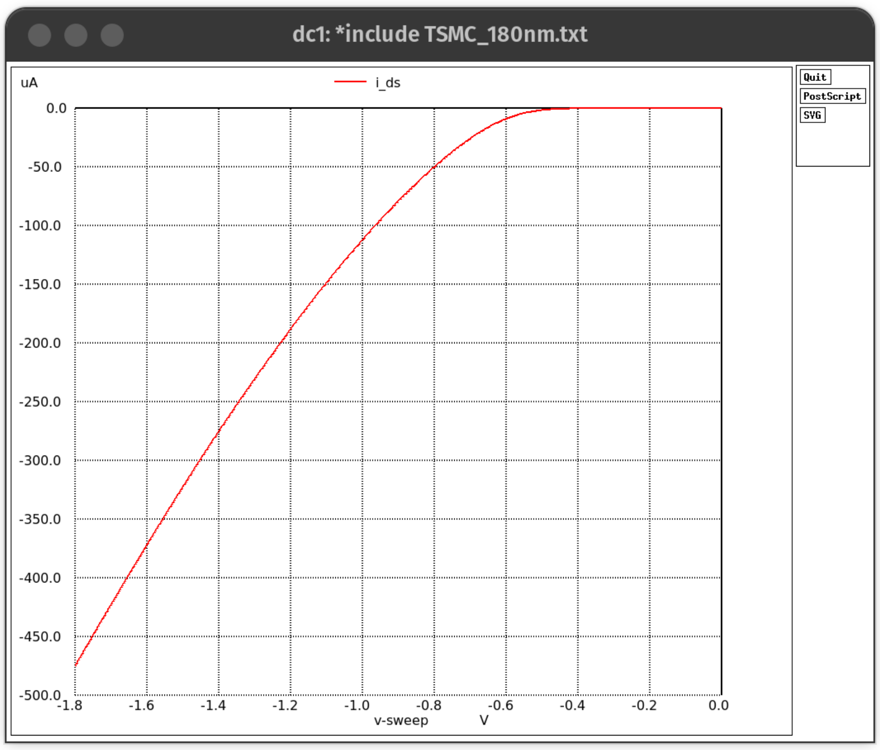


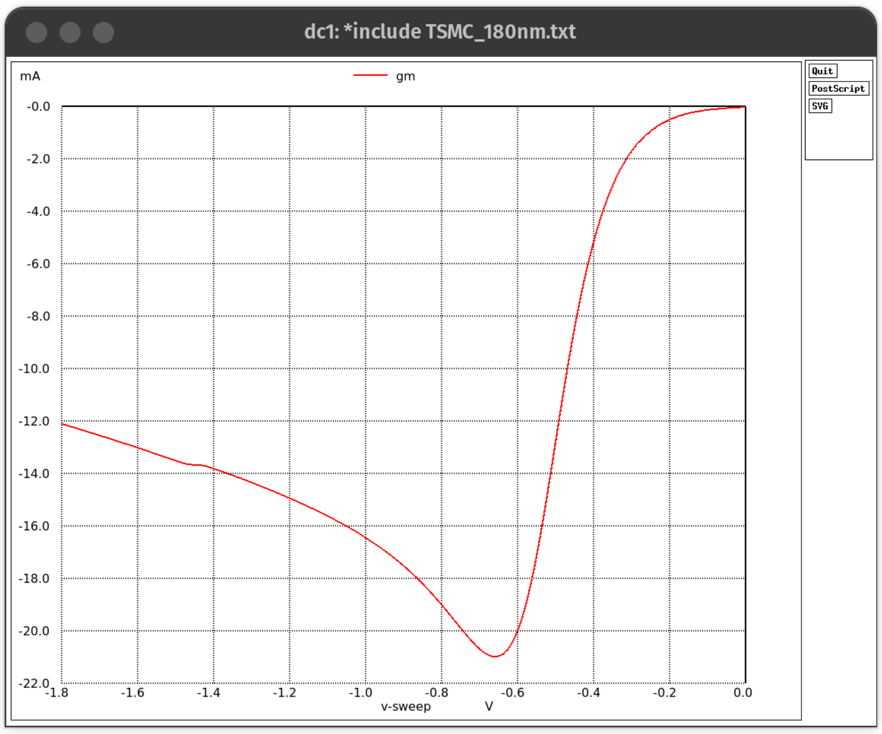


$\mu.C_{ox} = 0.4536 * 10^{-4} A/V^2$

B]VBS=0mV

```
VGS for max slope = -0.660274, max_slope = -0.021  I_DS=18.07544e-06
VTH=-457mV
```

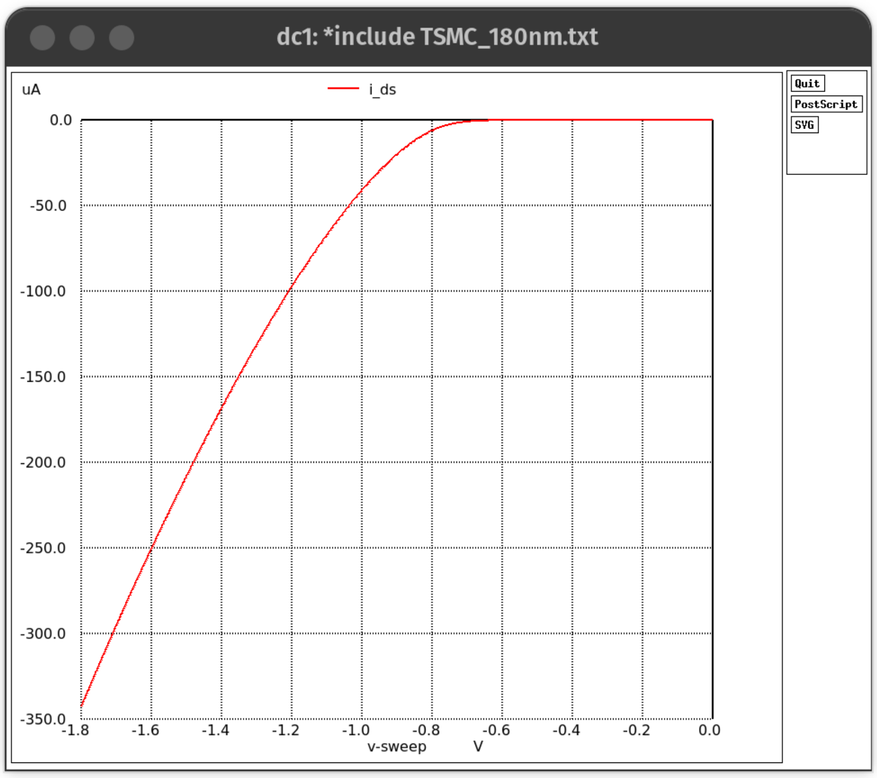


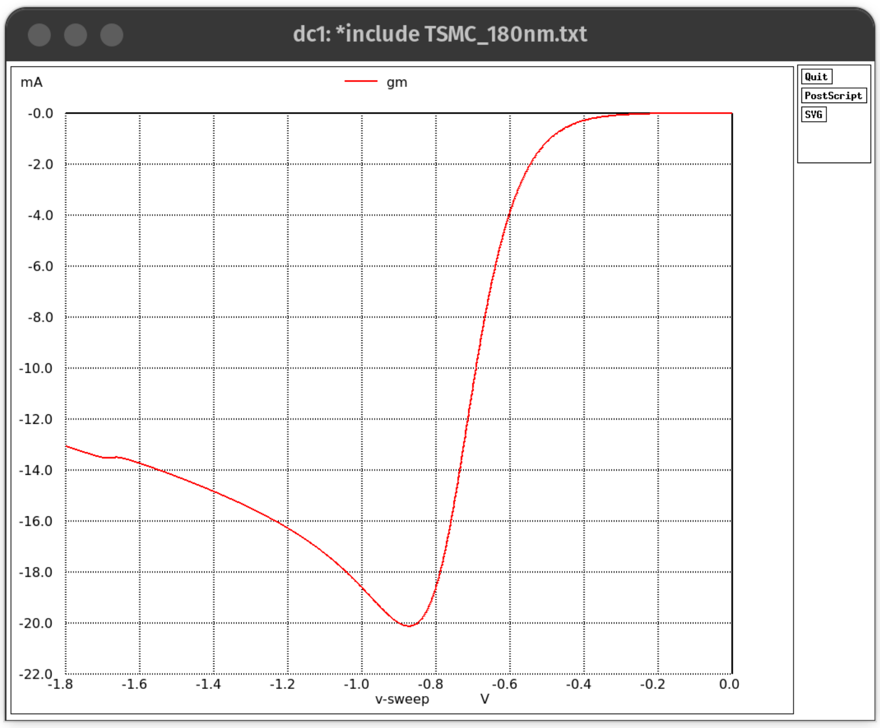


$\mu.C_{ox} = 0.441 * 10^{-4} A/V^2$

C]VBS=900mV

```
VGS for max slope= -0.875229, max_slope = -0.0200244 I_DS=15.74256e-06
VTH=-667mV
```





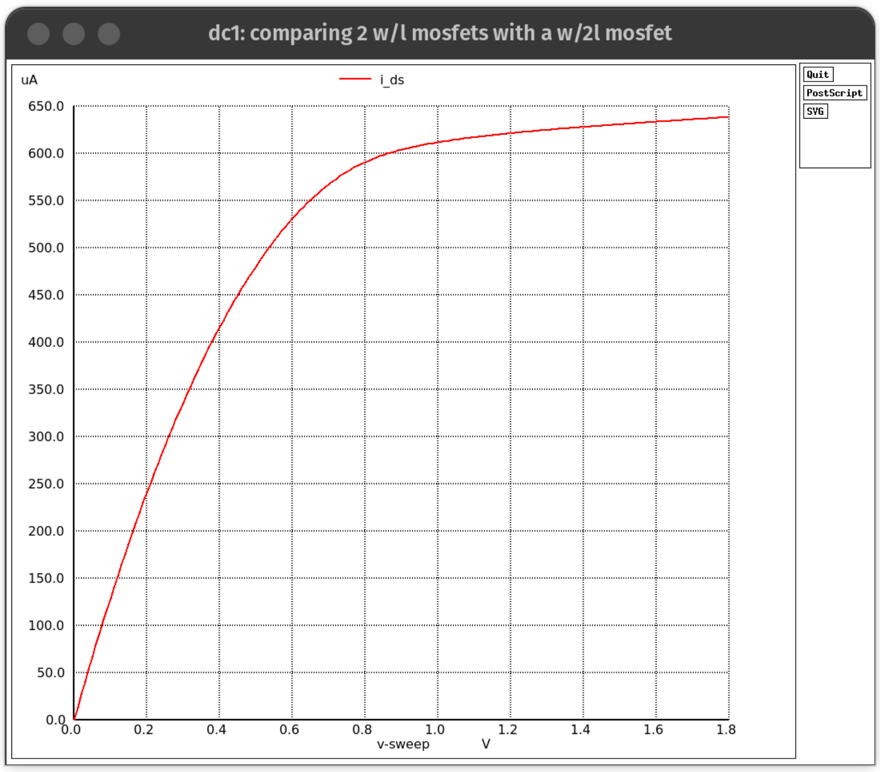
$$\mu.C_{ox} = 0.4 * 10^{-4} A/V^2$$

	900mV	0V	-900mV
V_th,NMOS	389mV	454mV	654mV
V_th,PMOS	-667mV	-457mV	-366mV

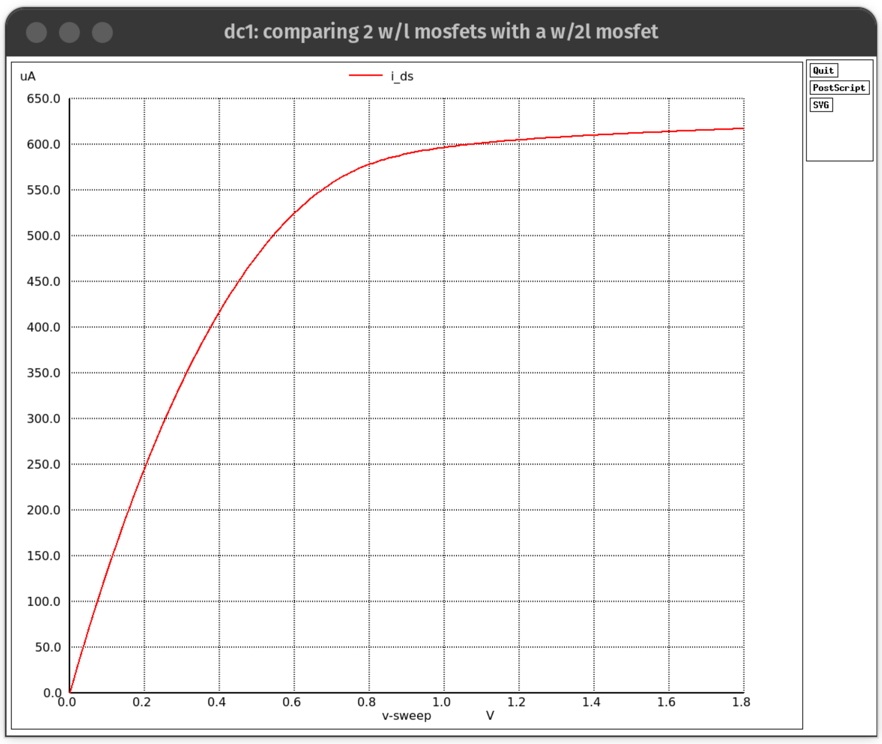
SCRIPTING CODE:

```
.include TSMC_180nm.txt
.param SUPPLY=-1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd


VGS G gnd 'SUPPLY'
VDS D gnd -1.8V
VBS B gnd 900m


M1   gnd    G    D   B   CMOSP  W={width_N}  L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
.dc VGS 0 -1.8 -0.001V
.measure dc current_at_slop FIND I(VDS) WHEN V(G)=-0.875229

.control
set hcopypscolor = 1
set color0=white
set color1 = black
run
let I_DS=-VDS#branch
let gm = deriv(sqrt(VDS#branch))
plot gm
plot I_DS

.endc
```

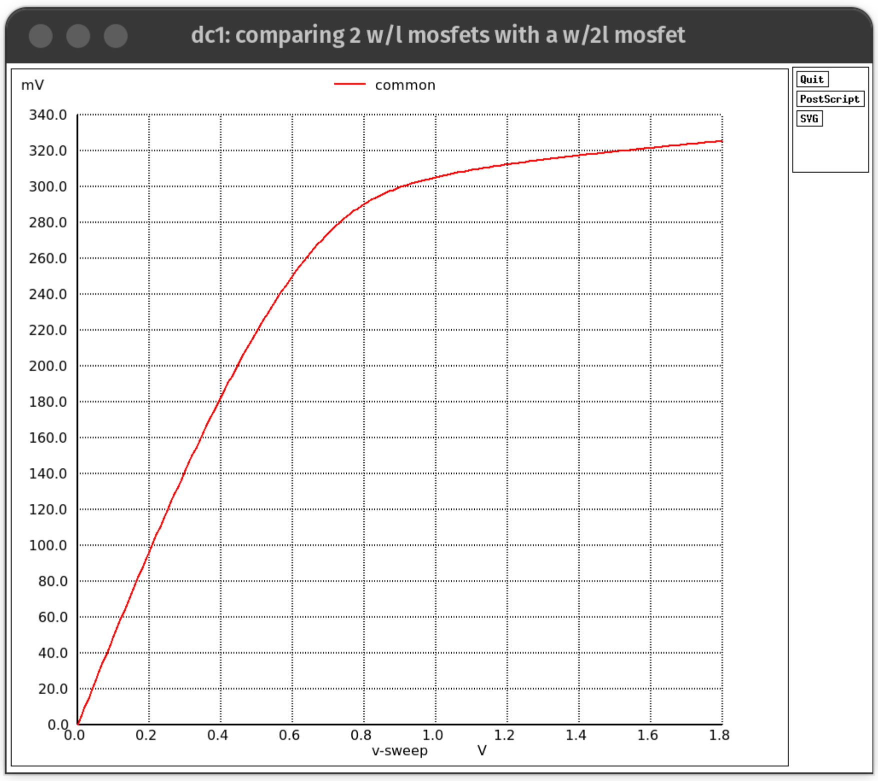
QUESTION 8:



2 MOSFETS With parameter W/L



MOSFET With parameter W/2L



Plot of Common Voltage between M1 and M2

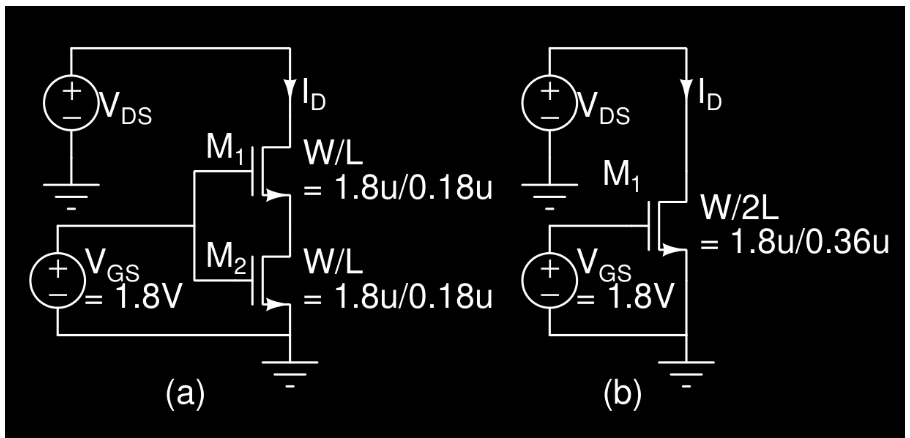


Figure 1

Explain why a W/2L transistor does not behave in exactly the same way as a series combination of two W/L transistors for small values of L?

A W/2L transistor does not behave exactly the same way as a series combination of two W/L transistors for small values of L due to several short-channel effects and parasitic elements:

- **Channel length modulation:** As L decreases, the effect of drain voltage on the channel length becomes more pronounced, leading to different I-V characteristics.
- **Drain-induced barrier lowering (DIBL):** In short-channel devices, the drain voltage can influence the source barrier, affecting the threshold voltage and subthreshold behavior.
- **Body Effect**

These effects become more pronounced as L decreases, causing the W/2L transistor to deviate from the idealized behavior of two W/L transistors in series. In practice, this means that the performance, power consumption, and switching characteristics of the two configurations will differ, especially in advanced technology nodes with very small feature sizes.

VTh=0.55V

Linear Region if VDS<Vgs-Vth → Vd<1.25V for M1 & Vcommon<1.25V for M2

Saturation Region if VDS≥Vgs-Vth → Vd≥1.25V for M1 & Vcommon≥1.25V for M2

Sweep	M1 Mode	M2 Mode
VD = 0.204762, Vcommon = 0.0995238	Linear	Linear
VD= 0.790476, Vcommon= 0.289524	Linear	Linear
VD = 1.5, Vcommon= 0.323333	Saturation	Linear
VD = 1.78333, Vcommon = 0.32619	Saturation	Linear

SCRIPTING CODE:

```
Comparing 2 w/l mosfets with a w/2l mosfet

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VDS D gnd 'SUPPLY'
VGS G gnd 1.8V

M1    D     G     common    gnd  CMOSN  W={width_N}  L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
M2   common    G     gnd    gnd  CMOSN  W={width_N}  L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*M3   D    G     gnd    gnd  CMOSN  W={width_N}  L={4*LAMBDA}
*+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

.dc VDS 0 1.8 0.01V

.control
set hcopypscolor = 1
set color0=white
set color1 = black
run

let I_DS=(-VDS#branch)
plot I_DS
.endc
```

QUESTION 9:

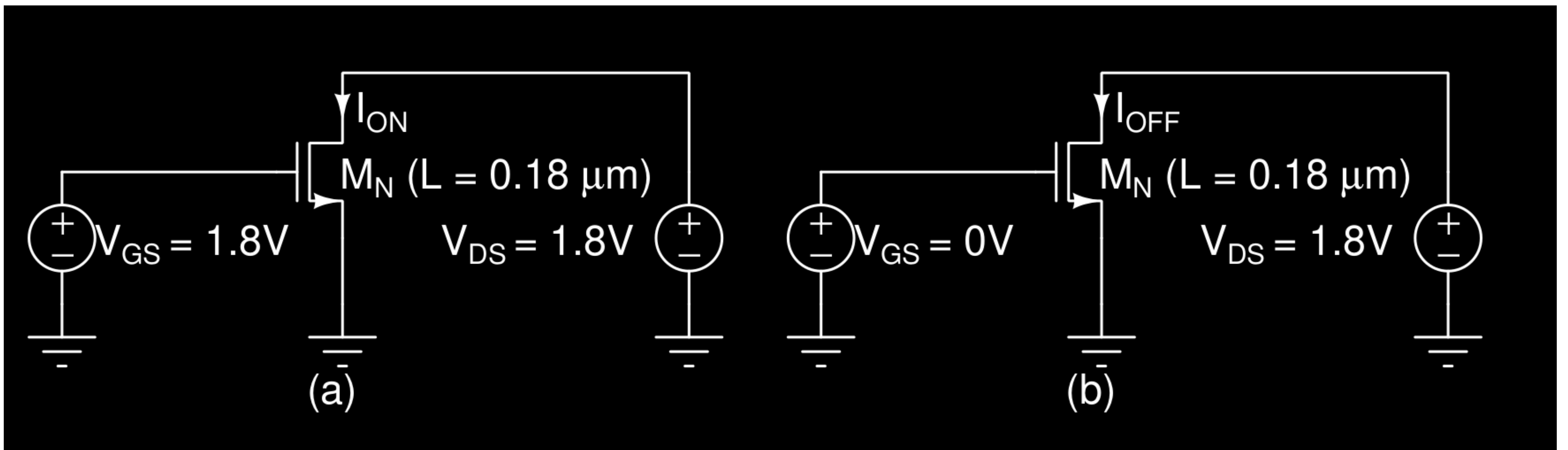
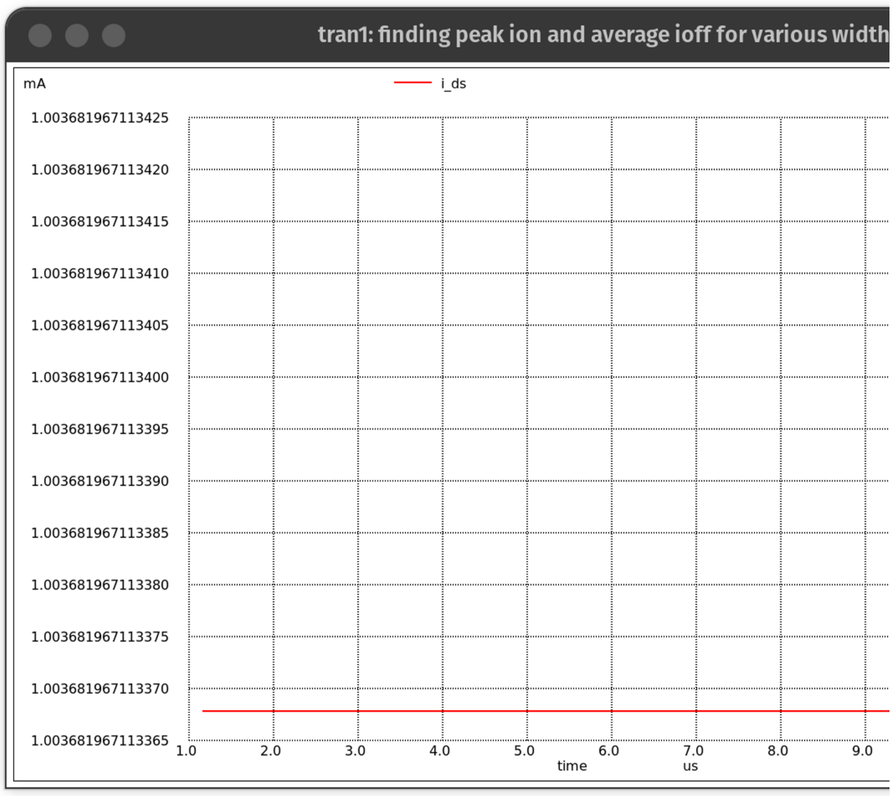
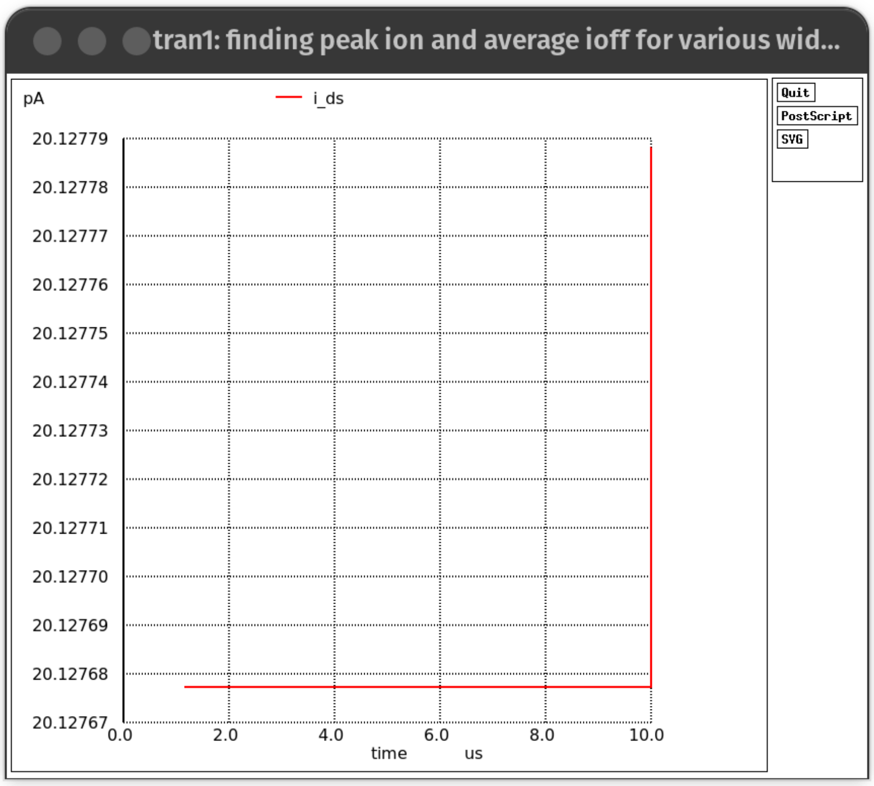
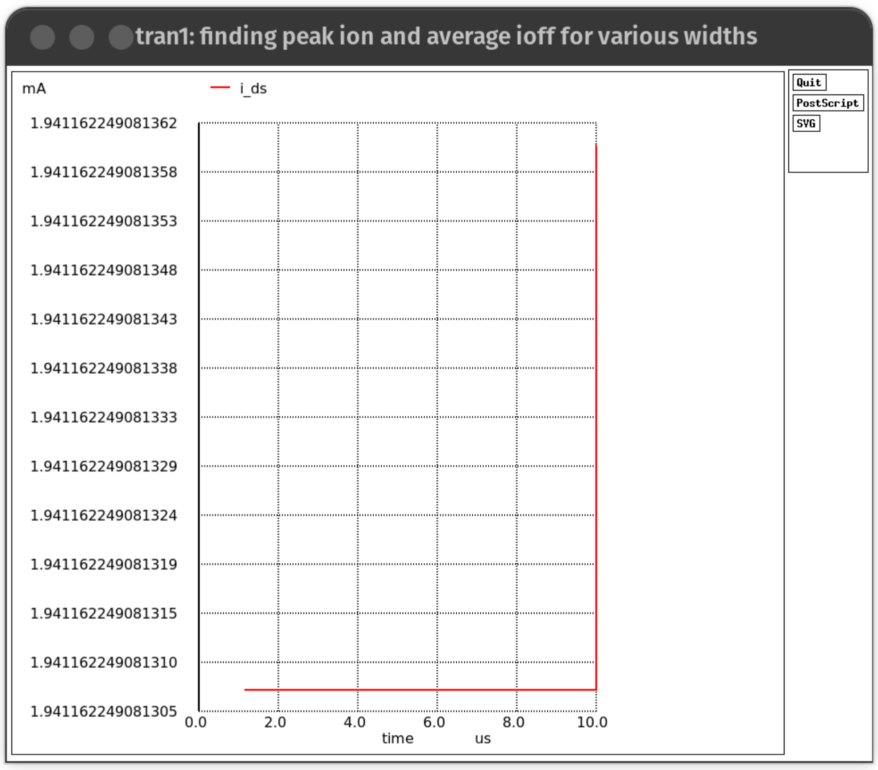


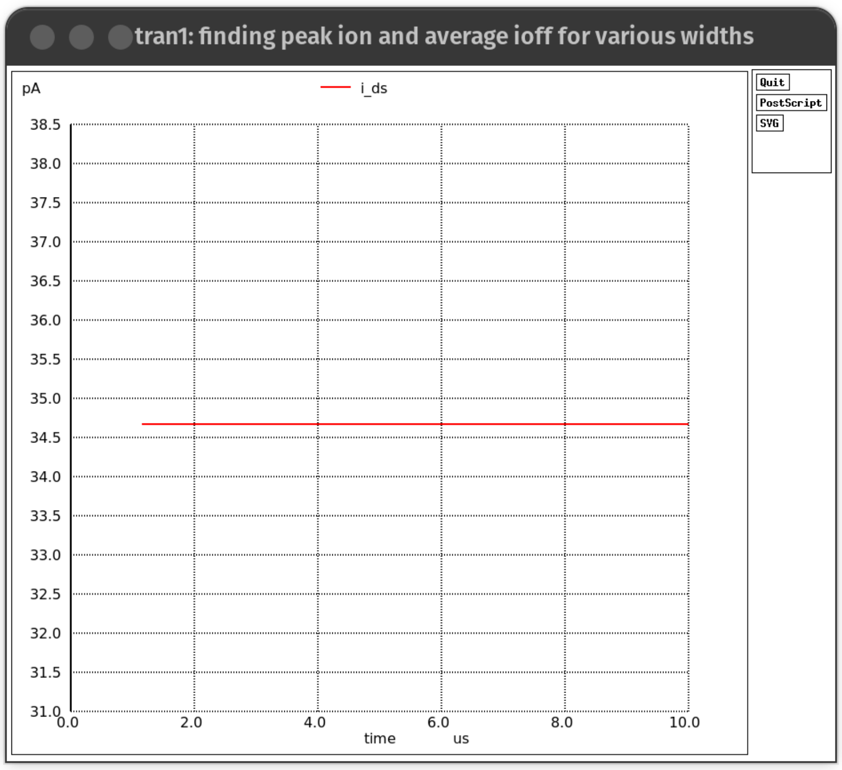
Figure 2



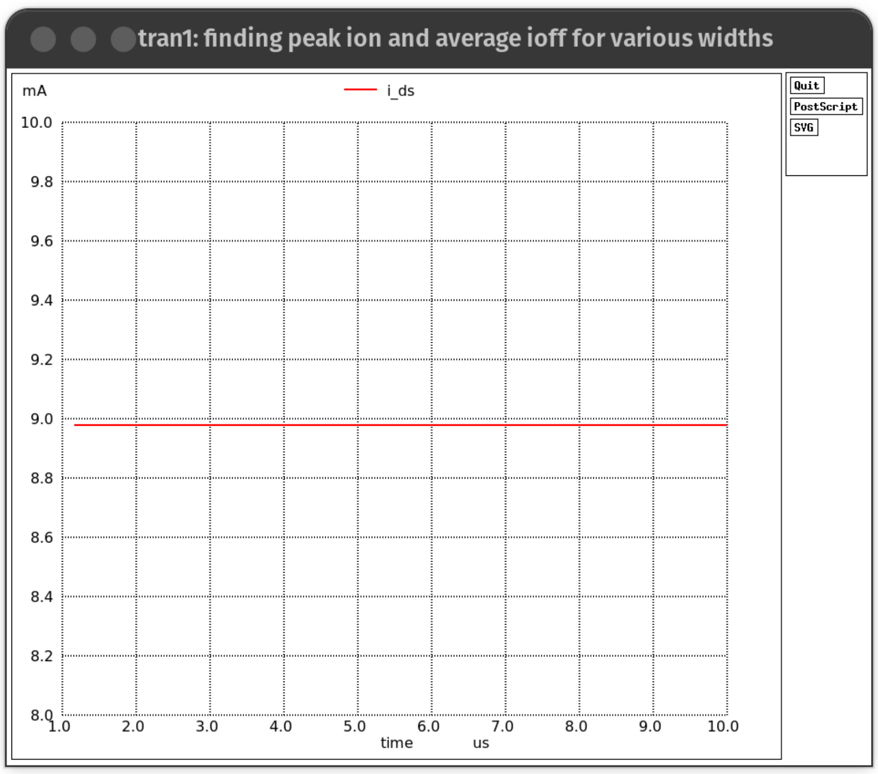


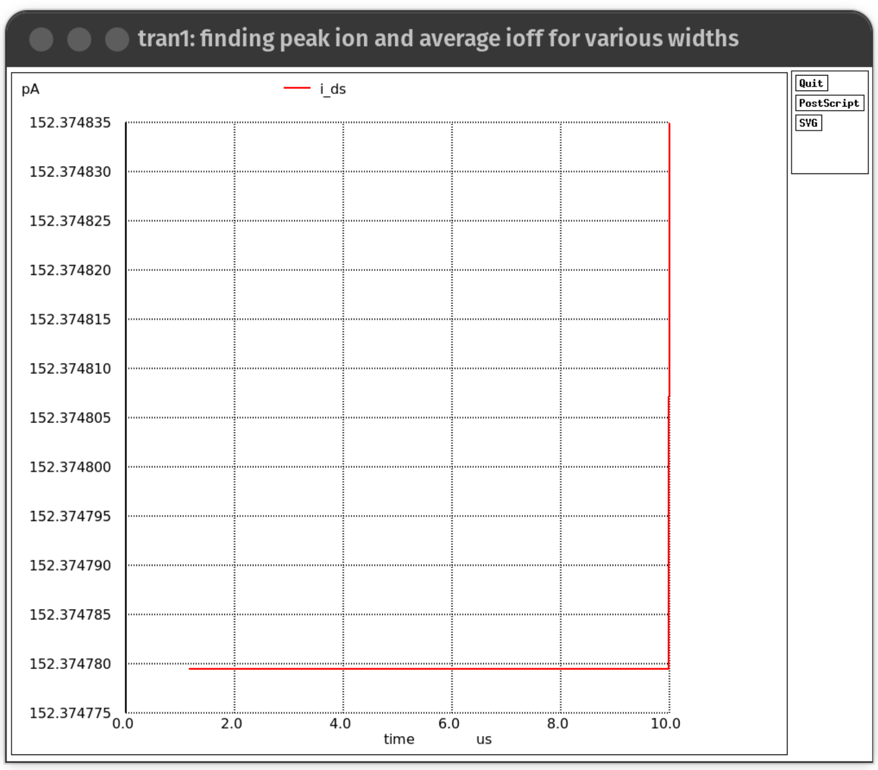
W=1.8u



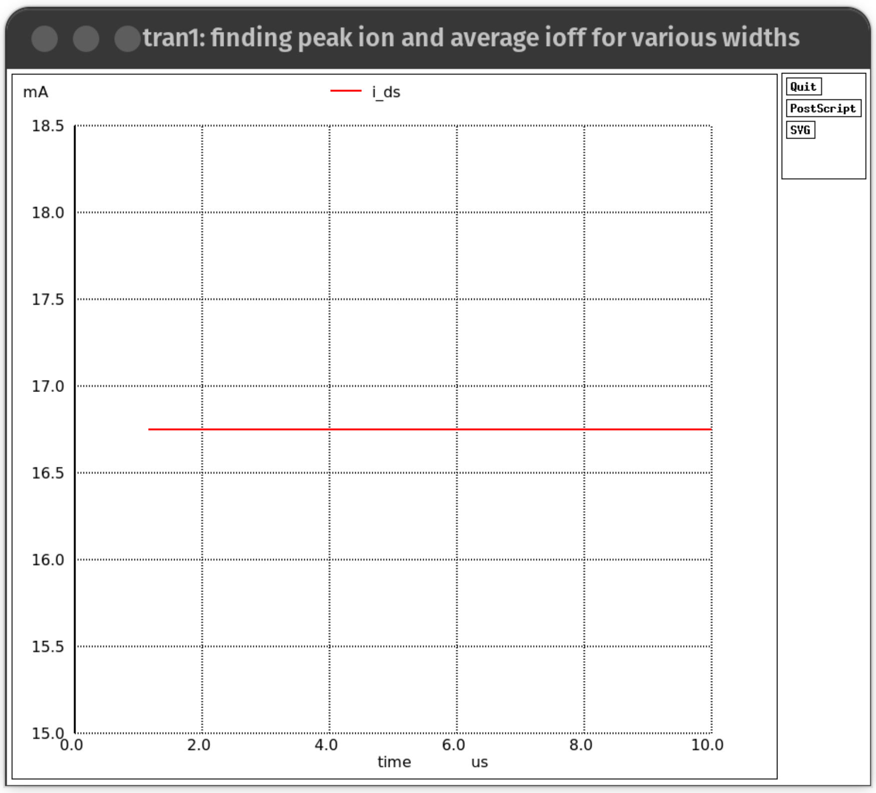


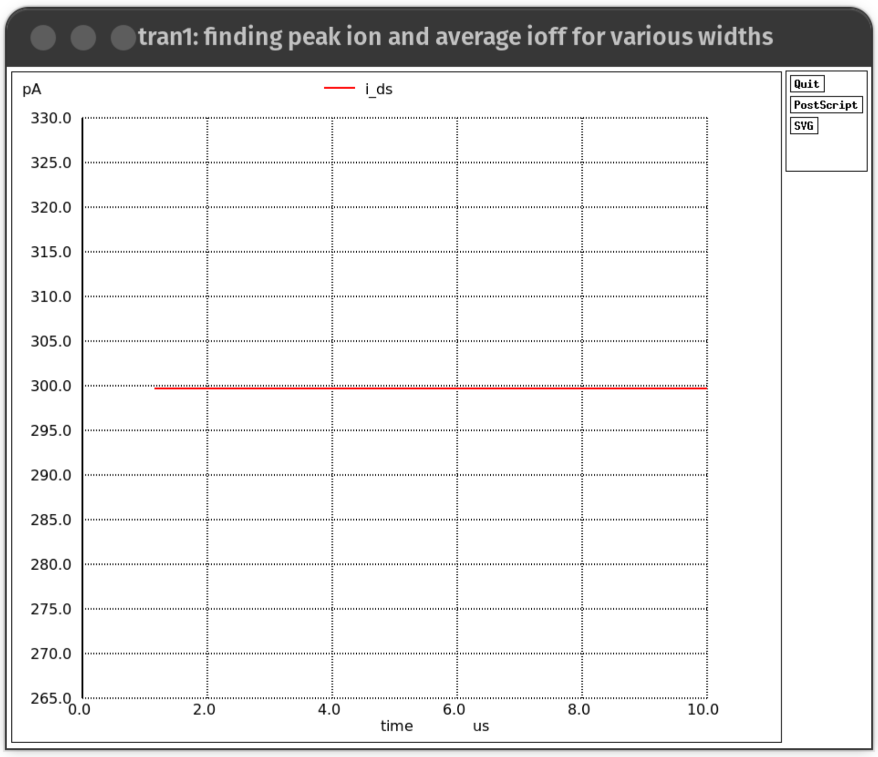
W=3.6u





W=18u





W=36u

Width	Ion	Ioff (in A)
1.8u	0.00100368=1.003mA	2.0127 *10^-11
3.6u	0.00194116=1.94mA	3.47 *10^-11
18u	0.009005=9.005mA	15.2375*10^-11
36u	0.0167368=16.7mA	30.1228*10^-11
	Peak Ion=16.7mA	Avg Ioff=12.70*10^-11

Here in this case, in ON state the transistor will always be in saturation .Now the formula is

$$I_{DS} = \frac{1}{2}\mu.C_{ox}.(W/L)(V_{GS} - V_{TH})^2$$

As we can see $I_{DS} \alpha W$ so we generally get linear curve ,But in practical, we get approximately linear itself ,same in case of Ioff

SCRIPTING CODE:

```
Finding peak Ion and average Ioff for various widths

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VDS D gnd 1.8
VGS G gnd 0


M1    D    G     gnd    gnd  CMOSN  W={10*width_N}  L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
.tran 1u 10u 1u
.control
set hcopypscolor = 1
set color0=white
set color1 = black

run
```

```
let I_DS=(-VDS#branch)
plot I_DS

.endc
```

QUESTION 10:

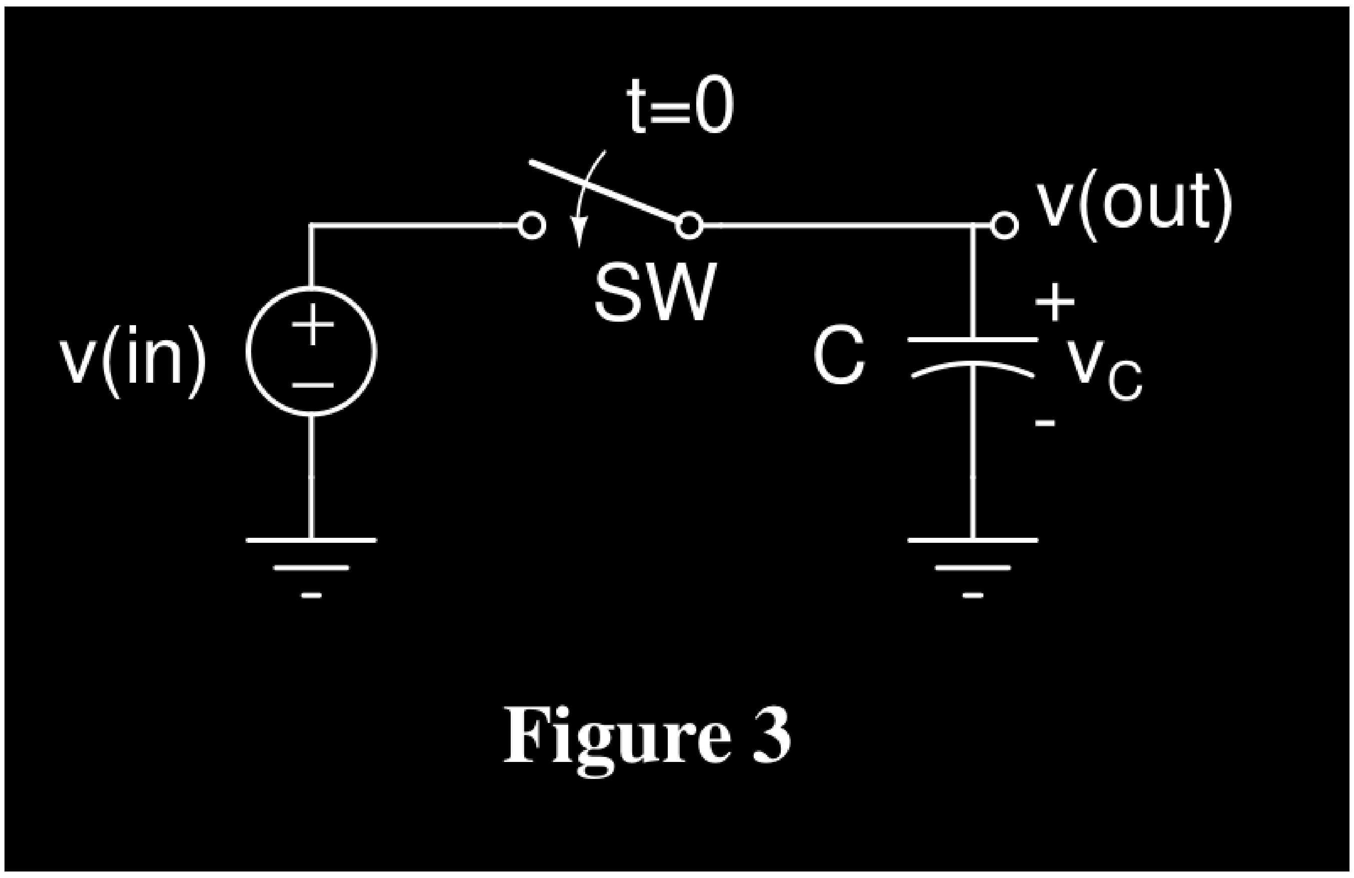
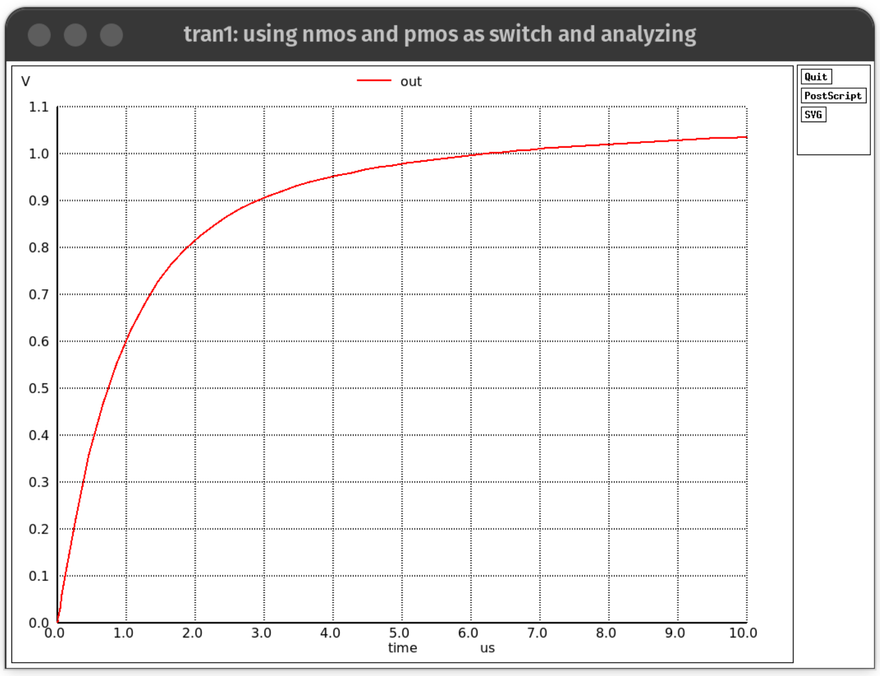
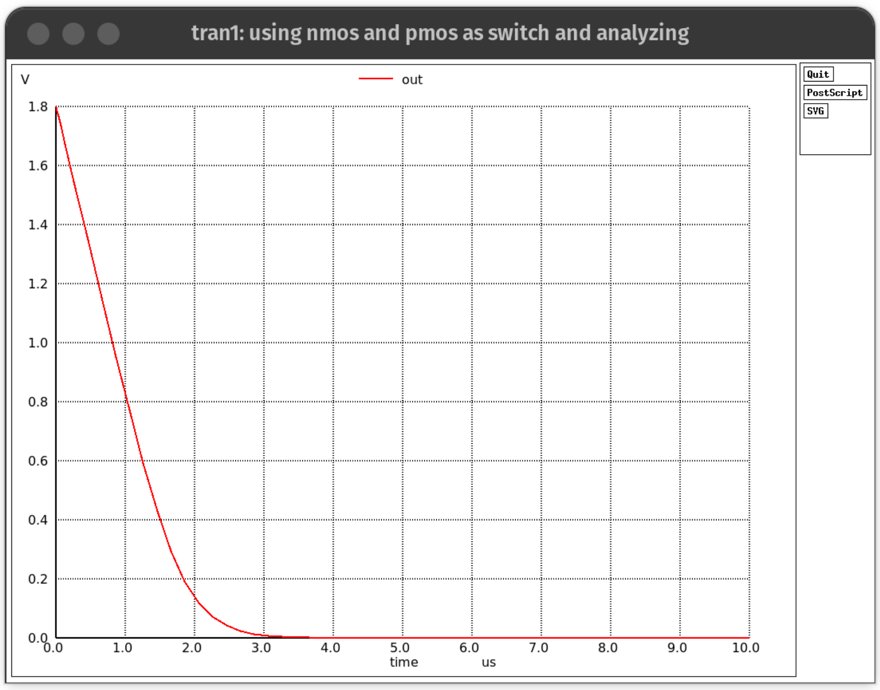


Figure 3

A] Replace the switch ‘SW’ by an NMOS (W/L = 0.18μ) and plot v(out)



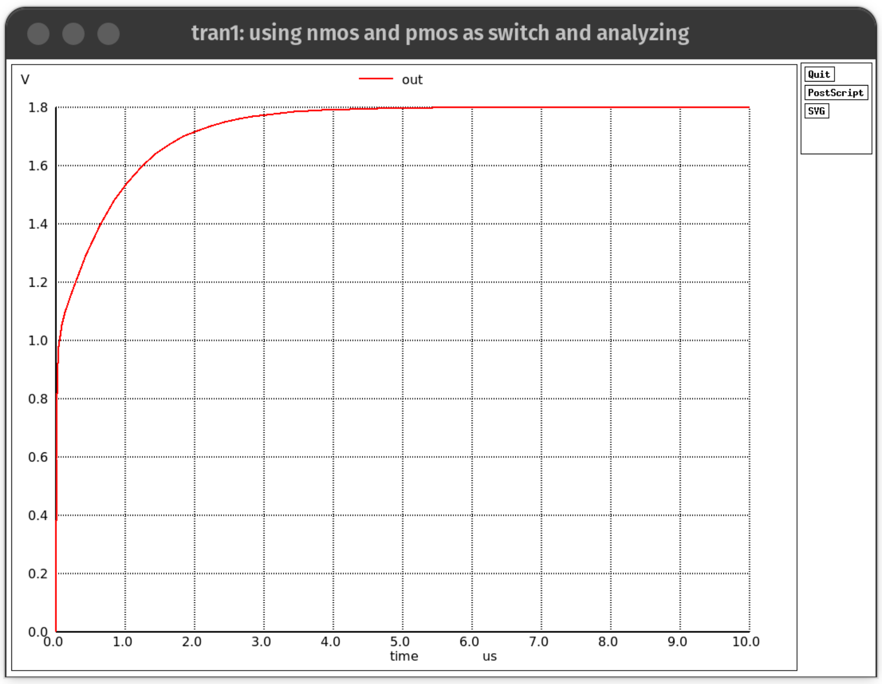
i) vc (0−) = 0V and v(in) = 1.8V



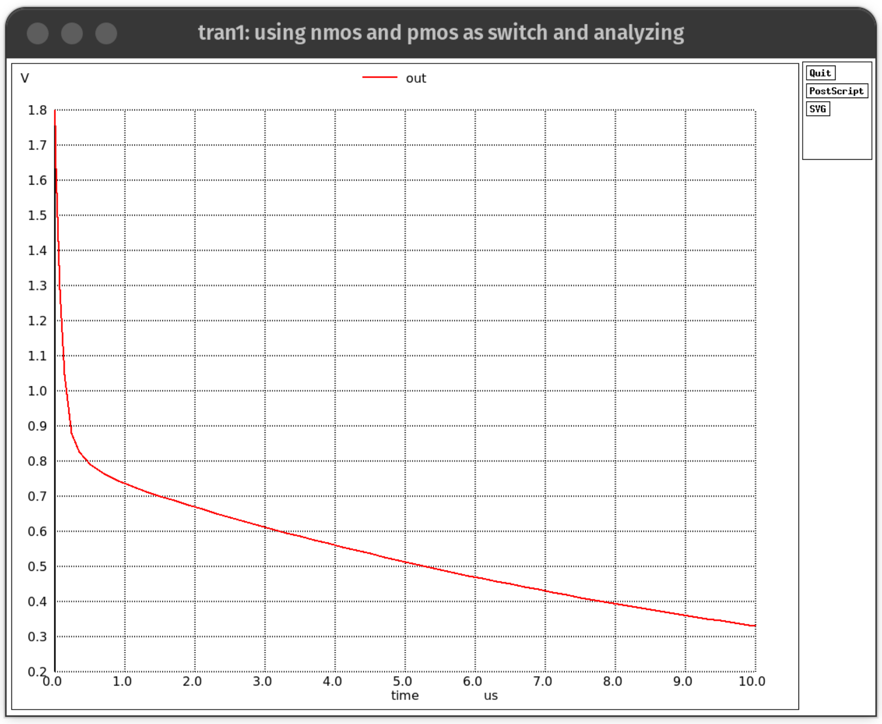
ii) vc (0−) = 1.8V and v(in) = 0V

💡 The NMOS is ON intially and allows source voltage to increase hence charging the capacitor but when it reaches Vgs-Vth voltage , the new Vgs becomes Vgs-(Vgs-Vth) =Vth and a little voltage beyond this , it goes into Cutoff mode and then capacitor retains charge theoritically but MOS goes into sub threshold conduction region also having little bit leak.But discharge is perfect. **Final Capacitance Voltage=Vgs-Vth**

B]Replace the switch ‘SW’ by an PMOS (W/L = 0.18μ) and plot v(out)



i) vc (0−) = 0V and v(in) = 1.8V



ii) vc (0−) = 1.8V and v(in) = 0V

💡 The PMOS is intially ON and then charging is perfect.While discharging ,at Capacitance voltage is |Vth,pmos| ,it goes into cutoff mode and stops discharging theoritically but due to sub threshold conduction ,it reduces a little bit in practical **Final Capacitance Voltage=|Vth,pmos|**

SCRIPTING CODE:

```
Using NMOS and PMOS as switch and analyzing

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VDS D gnd 0
VGS G gnd -1.8

C1 out gnd 10nF
M1     D     G     out    D  CMOSP  W={width_N}   L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
.ic v(out)=1.8
.tran 1u 10u 0u
.control
set hcopypscolor = 1
set color0=white
set color1 = black

run
plot out
.endc
```

QUESTION 11:

GIVEN different λ=0.18um

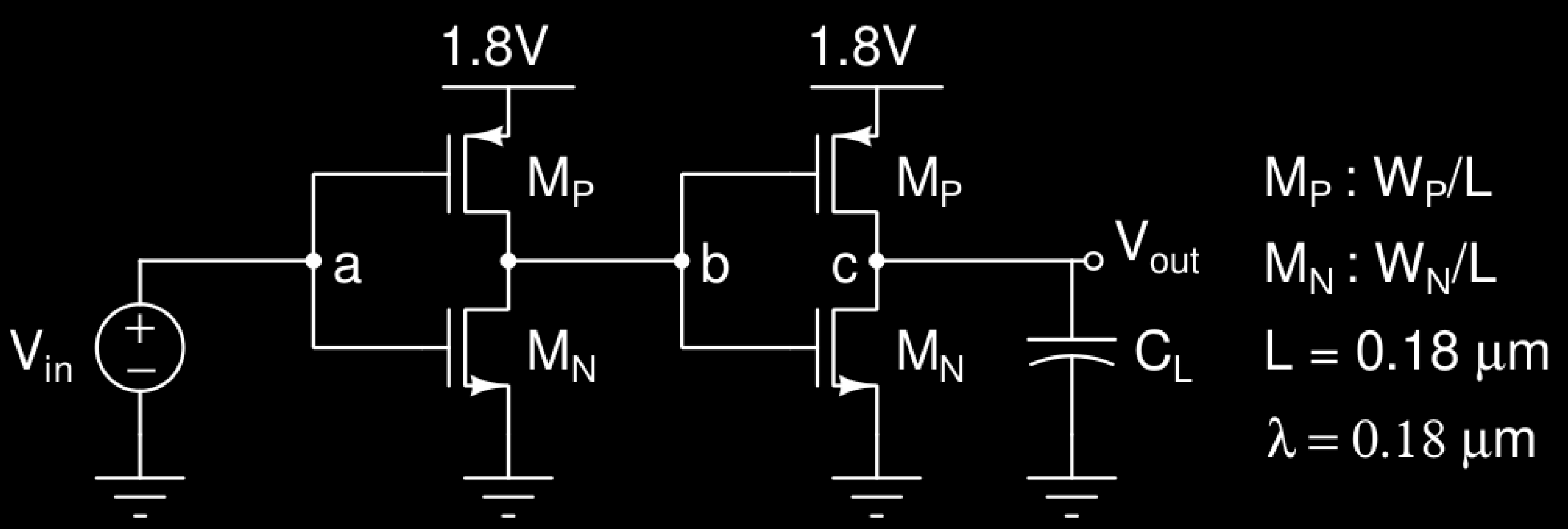
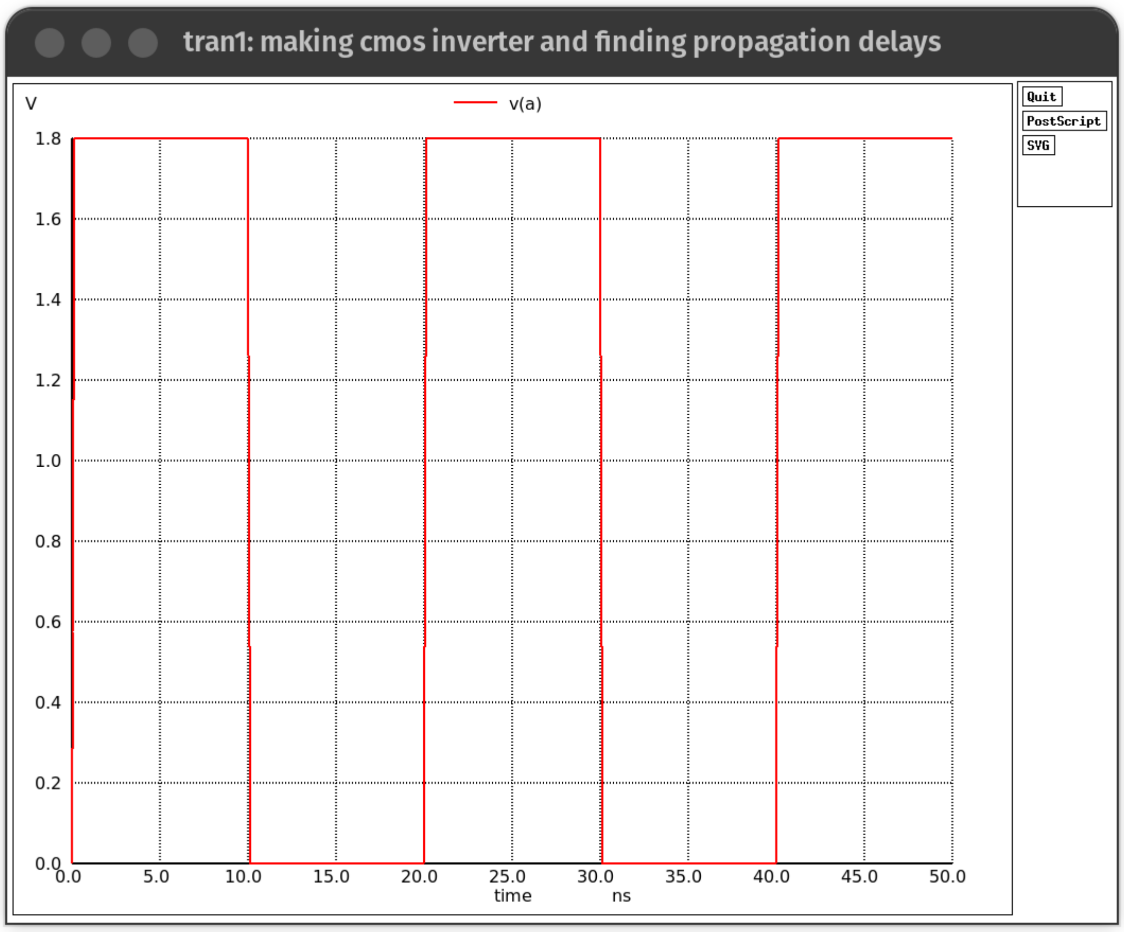
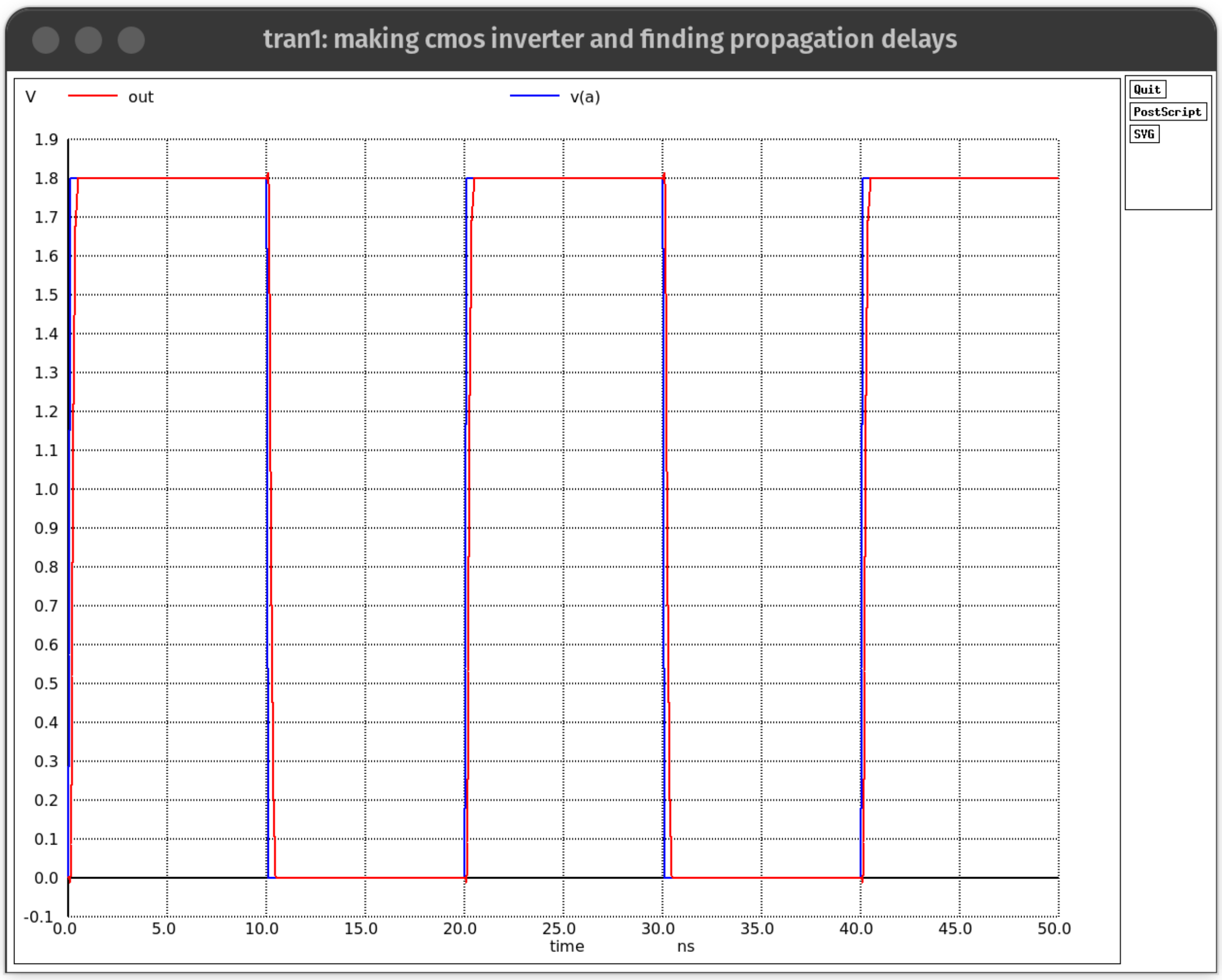


Figure 4

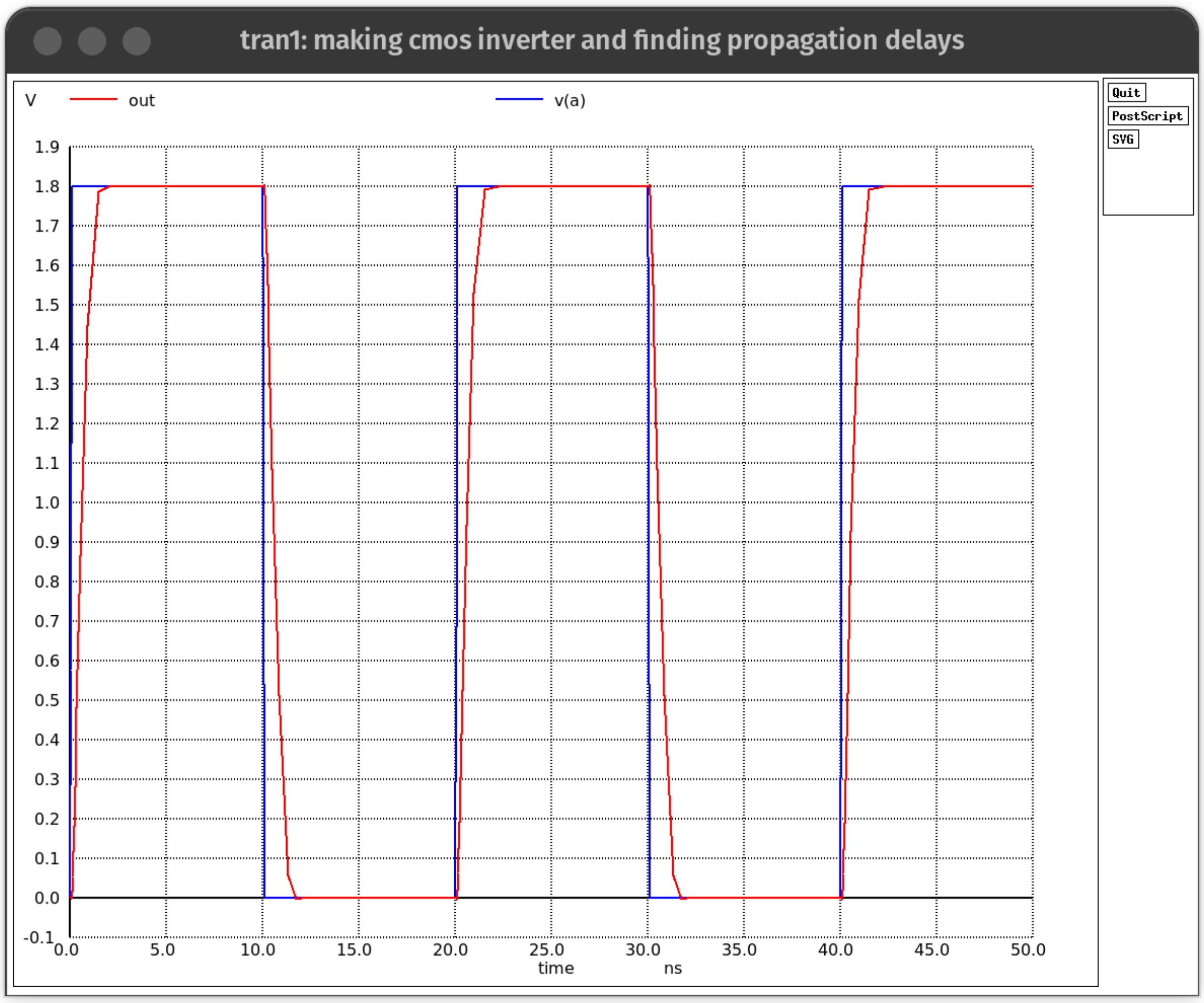
Plot Vout with respect to time and calculate the propagation delay between input and output (tpd) and tabulate them for the following cases:



A]CL =100 fF, Wn = 1.8µm Wp = 2.5 × Wn

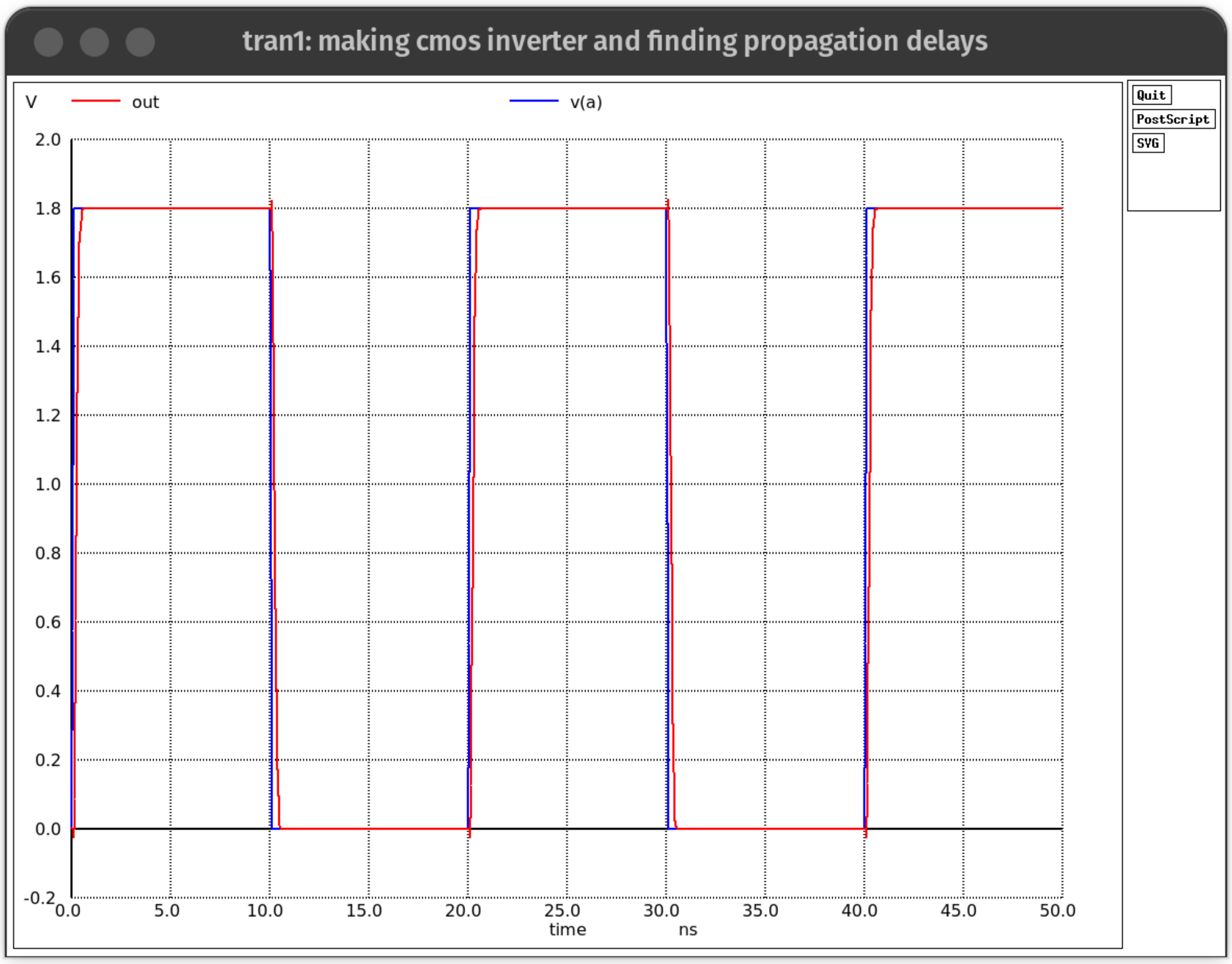


B]CL =500 fF ,Wn = 1.8µm Wp = 2.5 × Wn



Than the previous case , capacitance is increased by 5 times ,the Time constant increases hence the charging and discharging time increases and so we see this delay.

C]CL =500 fF ,Wn = 9µm Wp = 2.5 × Wn



As width is increased , I is increased as Current is proportional to W , so we get 5 times faster current than the previous one ,hence we observe fast charging and discharging and it is similar to (a) because now Cnew=5*C (in case a) and Inew=5*I(in case a)

Condition	time propagation delay in raising(10^-10)	time propagation delay in falling(10^-10)	time propagation delay(10^-10)
(a)	1.639420	1.745791	1.69261
(b)	4.915194	5.497178	5.20619
(c)	1.741052	1.868425	1.80474

D] From the delay table, comment how the scaling up of transistor widths affects the propagation delays.
Note: Delay = (rise-time + fall-time)/2, where rise-time is defined as the delay between rising output and corresponding falling input when both are at their 50% values.Similarly fall-time is defined as the delay between falling output and corresponding rising input when both are at their 50% values.

Comment how the scaling up of transistor widths affects the propagation delays?

From the derivation of rise time & fall time ,we get that

SCRIPTING CODE:

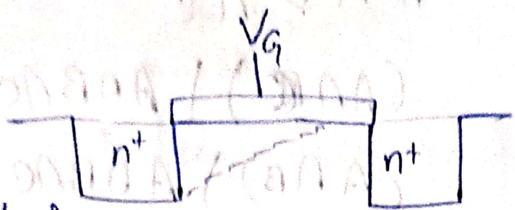
```
Making CMOS Inverter and finding propagation delays

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.18u
.param width_N={10*LAMBDA}
.param  width_P={2.5*width_N}
.global gnd

vin a 0 pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns
VDD D gnd 'SUPPLY'
VGS G gnd 'SUPPLY'


M1N b a gnd gnd CMOSN  W={width_N}   L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}
```

```
M2N out b gnd gnd CMOSN   W={width_N}    L={LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M1P b a D D CMOSP    W={width_P}    L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2P out b D D CMOSP   W={width_P}    L={LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

CL out gnd 100fF
.tran 20n 50n
** MEASURING DELAYS (Refer manual section 15.4.5)
.measure tran tpdr
+ TRIG v(a) VAL='SUPPLY/2' RISE=1
+ TARG v(out) VAL='SUPPLY/2' RISE=1
.measure tran tpdf
+ TRIG v(a) VAL='SUPPLY/2' FALL=1
+ TARG v(out) VAL='SUPPLY/2' FALL=1


.measure tran tpd param='(tpdr+tpdf)/2' goal=0
.control
set hcopypscolor = 1
set color0=white
set color1 = black

run
plot out v(a)

.endc
```

VLSI
Assignment - 1

2023112026
Nitin

Q2].



Saturation

$\vec{v} = \mu \vec{E}$ $\quad E = -\frac{\partial V}{\partial x}$ $\quad v = -\mu \frac{\partial V}{dx}$ $\quad V_{GS} > V_{TH}$

$V_{DS} \geq V_{GS}-$

$Q_x = WL\,C_{ox}(V_{GS} - V_{TH} - V_x)$
↑
at a distance x

$I_D = -v\,Q_{ch}$

$I_D = \mu \frac{dV}{dx} W C_{ox} [V_{GS} - V_{TH} - V_x]$

$\int_0^L I_D\,dx = \int_0^{V_{GS}-V_{TH}} \mu W C_{ox} [V_{GS} - V_{TH} - V_x]\,dx$

$I_D L = \mu W C_{ox} \left[\left[(V_{GS} - V_{TH}) V\right]_0^{V_{GS}-V_{TH}} - \left[\frac{V^2}{2}\right]^{V_{GS}-V_{TH}} \right]$

$I_D = \frac{1}{2} \mu \frac{W}{L} C_{ox} (V_{GS} - V_{TH})^2$

Linear $\quad V_{GS} > V_{TH},\ V_D > 0$

$Q = -WL\,C_{ox}(V_{GS} - V_{TH} - V_x)$

$I_D = -V(Q_{ch})$.

$\int_0^L I_D\,dl = \mu C_{ox} W \int_0^{V_D} (V_{GS} - V_{TH} - V_x)\,dx$

$I_D = \frac{1}{L} \mu W C_{ox} \left[(V_{GS} - V_T) V_D - \frac{V_{DS}^2}{2}\right]$

Q3) MOS Capacitance in various model

intrinsic cap

$C_{gc} = WLC_{ox}$

overlap cap
(due to interaction b/w channel charge & V_g)
C_{gd}
(source & drain)

<u>Cutoff:-</u> $V_{GS} < V_T$ } no inversion.

$|Q_g| = |Q_{body}|$ & for $\underline{-ve\ V_{GS}}$ accumulation $C_g = C_0 = WLC_{ox}$

as $V_g\uparrow$ depletion region forms at the surface as depletion region increases $\Rightarrow$ plate moves downward $\Rightarrow d\uparrow$

$C_{gd} = C_{gs} = WC_{ov}$

$C_{g0} = \frac{\varepsilon_r \varepsilon_0 A}{d}$. $C \propto \frac{1}{d}$ – distance b/w plates

$C_{gd}\downarrow$ as $d\uparrow$

<u>Linear :-</u> $V_{GS} > V_T$ } inversion,

$V_{DS} \leq V_{GS} - V_T$

as there is no connection b/w gate and body there is no C_{gb}

$C_{gs} = C_{gd} = WC_{ov} + \frac{1}{2}WLC_{ox}$

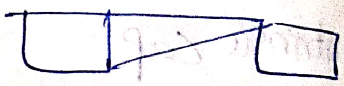
as $V_{DS}\uparrow$ inversion$\downarrow$ at drain so

$C_{GP}\uparrow$ at source

$C_{GP}\downarrow$ at drain

Saturation:-

$$V_{DS} > V_{GS} - V_T$$

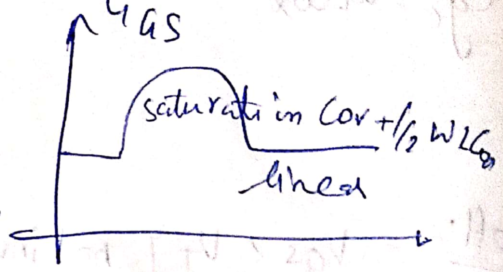


highly inverted

$$C_{gd} \approx W C_{ov}$$

$$C_{gs} \approx W C_{ov} + \frac{2}{3} W L C_{ox}$$

$$C_{gb} = 0$$

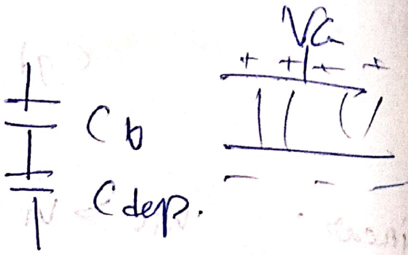


	cutoff	linear	saturation
C_{gb}	WLC_{ox}	0	0
C_{gs}	WC_{ov}	$WC_{ov} + \frac{1}{2} WLC_{ox}$	$WC_{ov} + \frac{2}{3} WLC_{ox}$
C_{gd}	WC_{ov}	$WC_{ov} + \frac{1}{2} WLC_{ox}$	WC_{ov}

Overlap capacitance:-

at weak inversion,

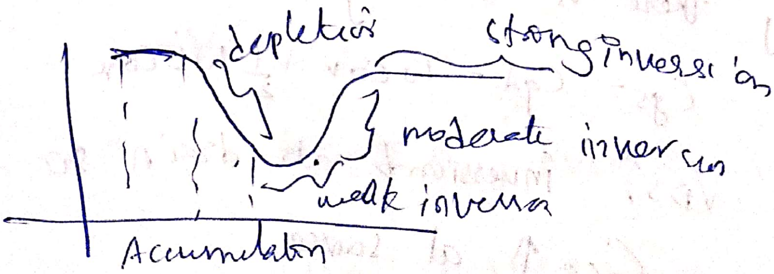
$$C_{gb} = \frac{C_o C_{dep}}{C_o + C_{dep}}$$



for some cases to simplify we take

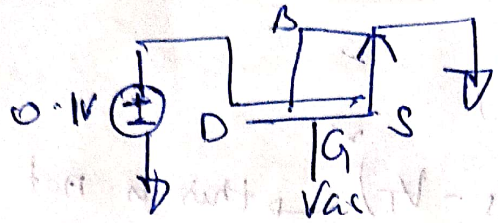
$$C_g = C_{gs} + C_{gd} + C_{gb} = C_o + 2 C_{gs}.$$

Plots:-



Q4) $V_{GS} = 1.8 \sin(2\pi \times 1000 - 90)$

$V_{GS} = -1.8 \cos(2000\pi)$



V_{GS} sweeping from -1.8 to 1.8 (cos oscillates from -1.8 to 1.8]

we need to find C_{gs}

$$Q = C_{GS} V_G$$

$$\therefore I = \frac{dq}{dt} = C\frac{dV_g}{dt}$$

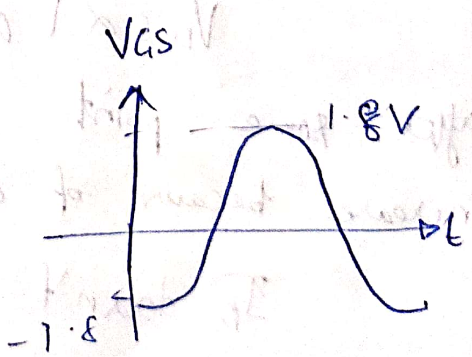
$\cancel{C_{gs} = I}$

$$C_{gs} = \frac{I_g}{(dV_g/dt)}$$

~~from~~ from the circuit, we find I_g and $\frac{dV_g}{dt}$ then to find C_{gs} $\left(C_{gs} = \frac{I_g}{dV_g/dt}\right)$ then we plot C_{gs} v/s V_{gs} we get plot like this.

M1 - D G gnd gnd

Drain Gate Source Body



tran 1u 490u 10u

step final intial

phase

V_{GS} = sin (0, 1.8, 1k, .0004, 0, -90)

DC amp freq delay damping

Q5] Second-order effects in MOSFET.

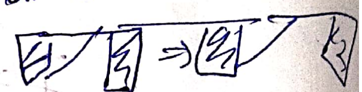
Channel-length modulation (CLM):-

In saturation mode,

$I_D = K_n \frac{W}{L} (V_{GS} - V_T)^2$ → this is not const.

the length of conductive channel is changed by V_{DS}

$V_{DS} \uparrow \Rightarrow$ length of effective channel



$I_D \uparrow , L \downarrow$

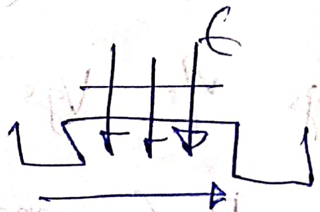
$I_D' = I_D (1 + \lambda V_{DS})$

$I_D' = K_n \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}$

more effective for small size devices.

Velocity saturation:-

as ($V_{DS} \uparrow$ es E $\uparrow$ es)



$V_{DS} \propto E \propto$ Velocity

after some point of V_{DS}, velocity wont ε increase because of collisions & carriers scattering.

I_D doesn't increase as expected.

Mobility degradation:-

$$E_{lateral} = \frac{V_{DS}}{L}$$

or high voltage at the gate of the transistor attracts carriers to the edge of the channel, causing collisions with oxide interface that slows the carriers.

Drain-induced barrier lowering (DIBL):-

$$V_T' = V_T - \eta V_{DS}$$

as $V_{DS} \uparrow$, ($E \uparrow$es) and make causes the current flow even ~~at~~ ~~so~~ ~~for~~ lower V_T

Body effect:-

When source & body terminal are at different potentials, $V_{SB} \rightarrow$ increases width of depletion region,

$V_{TH} \uparrow$

$$V_{TH} = V_{TH_0} + \gamma\left(\sqrt{V_{BS} \mp 2\phi_B} - \sqrt{2\phi_B}\right)$$

Sub-threshold condition:- (weak inversion)

$V_{GS} < V_T$, $I_{DS} \neq 0$ ~~as~~ I_{DS} drops off exponentially rather than abruptly becoming zero

This condition is called sub-threshold conduction.