AEC ASSIGNMENT 5

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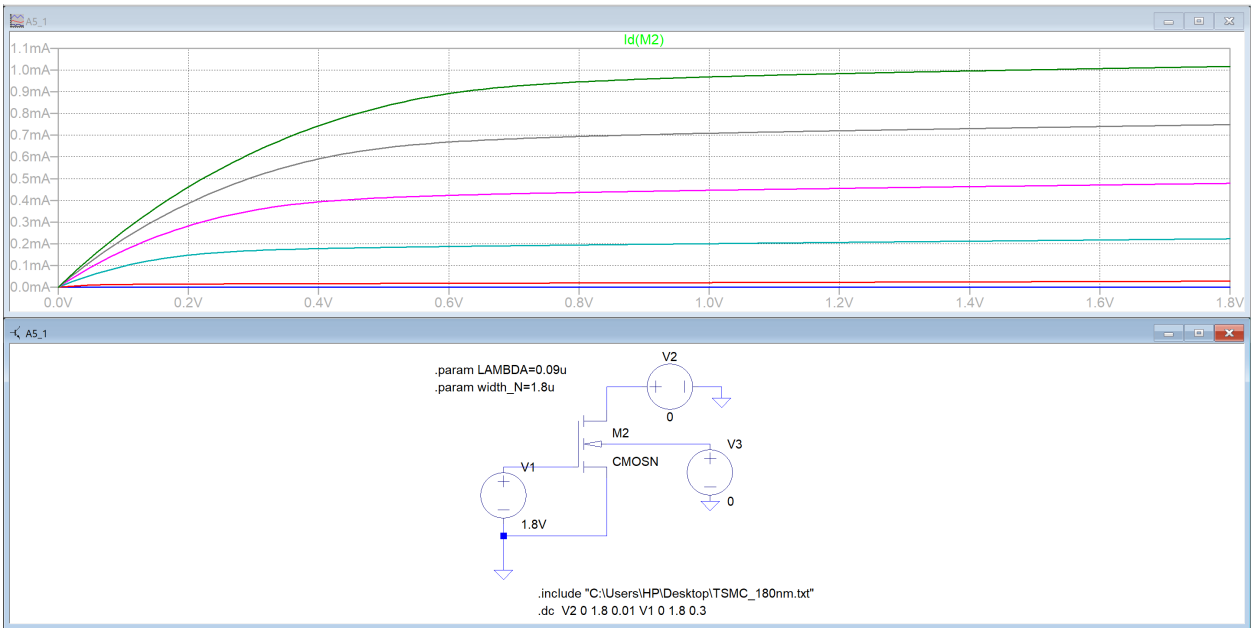
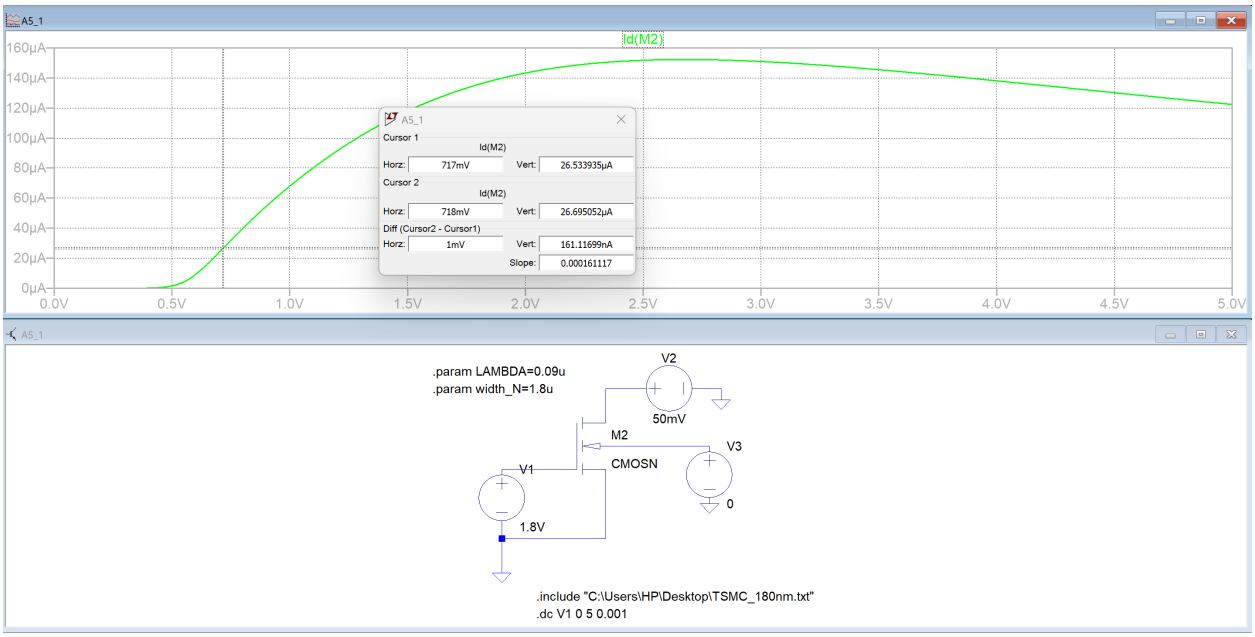
`(2023112026)`

Question 1: Plot of Id vs VDS in a NMOS



Question 2:



>Calculation for Slope

$$m_{slope} = 0.000161117 = \mu C_{ox}\frac{W}{L}V_{DS} = \frac{\partial I_D}{\partial V_{GS}}\ at\ triode\ mode$$

We know W/L =10 and VDS=50mV can calculate μC_{ox}

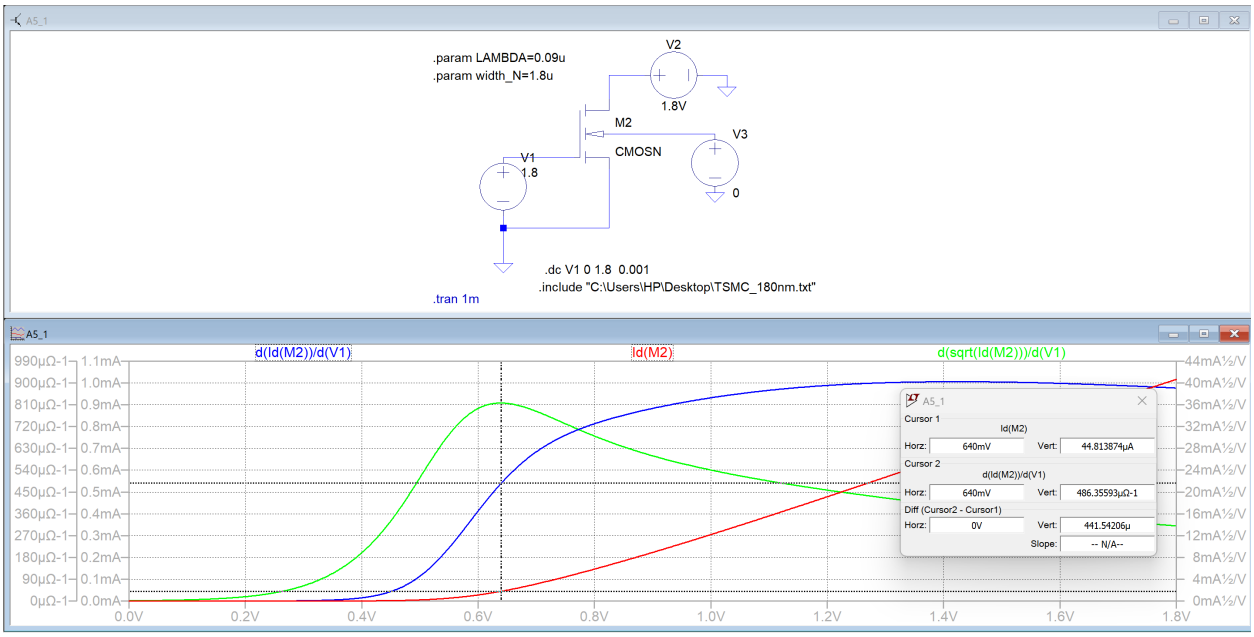
Since we found the max slope of this curve ,we draw a tangent at this point and plot a line equation y=mx+c ,from here we find x=(-c/m) because that is the point at which Id=0 and intercept is Vth

We got $m_{slope} = 0.00016117$ and Using $y - y_1 = m(x - x_1)\ and\ y_1 = 26.695052\mu A, x_1 = 718mV$

Put y=0(i.e Id=0) , we get $x = \frac{-y_1}{m} + x_1$

$$V_{TH} = 552.3mV\ and\ \mu Cox = 322.3 * 10^{-6}\frac{A}{V^2}$$

2B:Doing the same analysis with a Increased VDS



In this graph , when we apply VDS=1.8V and VGS is sweeped from 0 to 1.8V ,

$$V_{DS} \geq V_{GS} - V_{TH}$$

HENCE IT IS ALL TIME IN SATURATION MODE.

SINCE THE GRAPH IS IN SATURATION MODE, due to 2^{nd} order effects more effective in saturation mode ,

$$\frac{\partial \sqrt{I_D}}{\partial V_{GS}} = \sqrt{\mu_n C_{ox} W/L}$$

μ_n is variably changing(decreasing) to the actual μ_n as compared to triode mode , so we try to maximise $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$ and get maximum mobility

So $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$ is maximum obtained at 640mV and slope of Id at this point is 486.3559 $\mu\Omega^{-1}$ and $y = mx + c$

$y = 6.6943166mA½$

$x = 640mV$

$m = 36.326033mA½/V$

$$\sqrt{I_D} = \frac{\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$$

Getting Vth =-c/m ,we get

$$V'_{TH} = 433mV$$

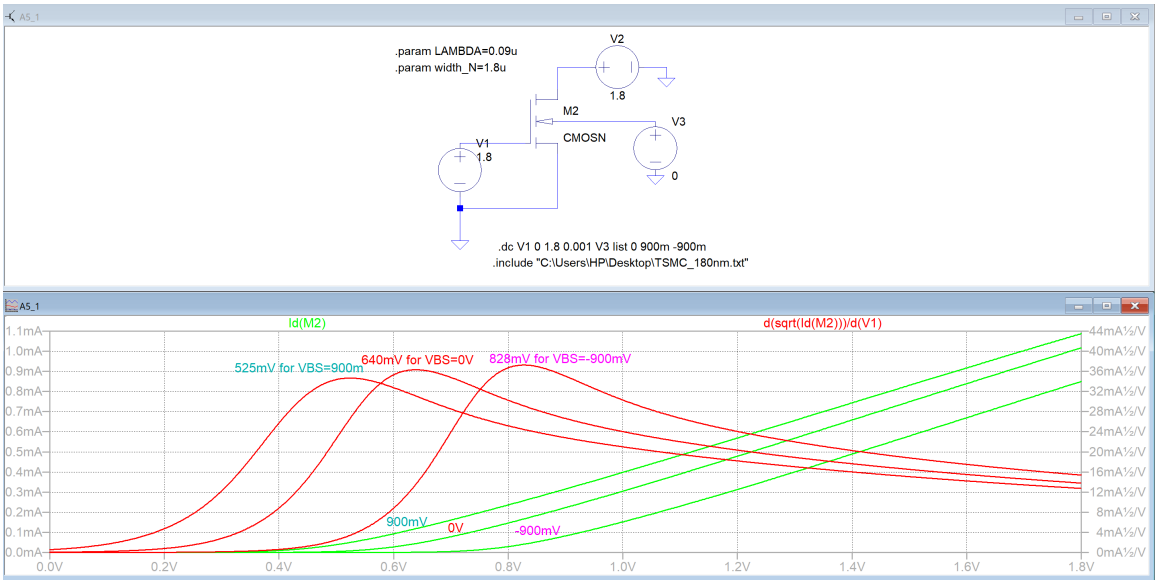
THIS REDUCED VTH is due to DRAIN INDUCED BARRIER LOWERING

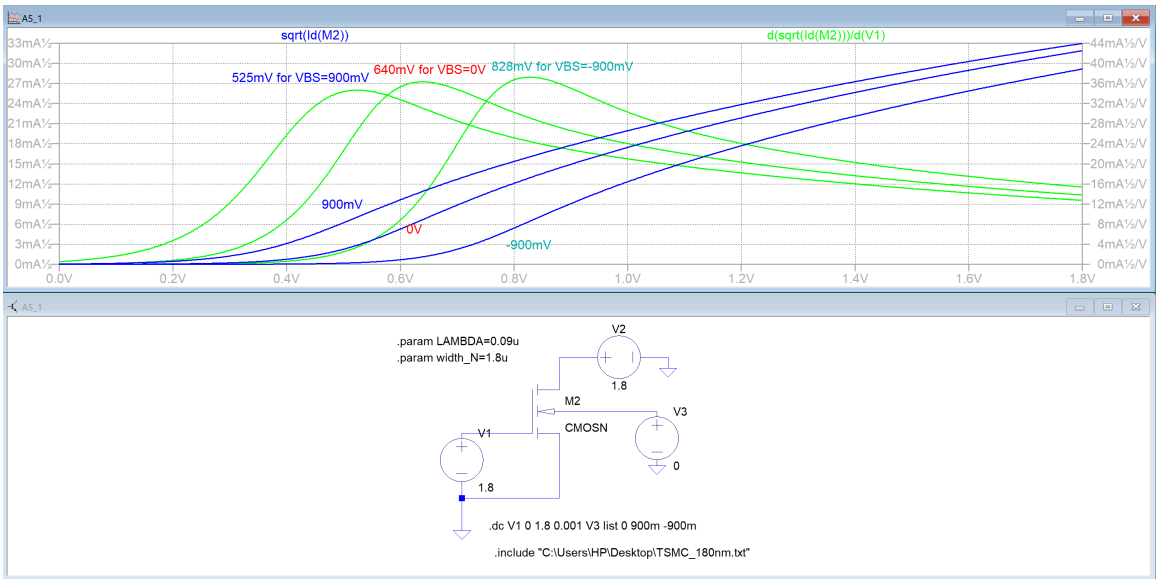
$$V'_{TH} = V_{TH} - \eta V_{DS}$$

When the drain voltage is increased, it is similar to applying a reverse bias voltage to an already reverse-biased diode. This amplifies the voltage at the negative terminal. Consequently, the depletion region around the drain expands, leading to a reduction in voltage required at the gate terminal to create an inversion layer or channel. In other words, an increase in drain voltage causes a decrease in the threshold voltage of the MOSFET. This phenomenon is called drain-induced barrier lowering (DIBL).

Question 3:

FOR NMOS:





To find Vth similar to the previous question ,

Since we know,

$$V'_{TH} = V_{TH} + \gamma(\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \qquad \phi_{F,NMOS} < 0 \quad \gamma > 0$$

So we can claim that,

$$V_{TH,900mV} < V_{TH,0V} < V_{TH,-900mV}$$

which is also depicted in the graph. where { 900mV ,0V ,-900mV} are values of **VBS .**

💡 **RESULTS:**

For VBS=0V,

$\sqrt{I_D} = \frac{\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$

x=640mV , m=36.326033mA½/V, y=6.6943166mA½

>VTH=455mV

For VBS=900mV,

$\sqrt{I_D} = \frac{\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$

x=525mV ,m=34.641599mA½/V ,y=7.0782073mA½

>VTH=320mV

For VBS=-900mV,

$\sqrt{I_D} = \frac{\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$

x=828mV ,m=37.258238mA½/V,y=9.062673mA½

>VTH=584mV

NOTE: These values are also affected by DIBL effect (VDS=1.8V),

IF we take VDS=50mV , we observe a Forward bias between Body and Drain. So to prevent this we take VDS>900mV.

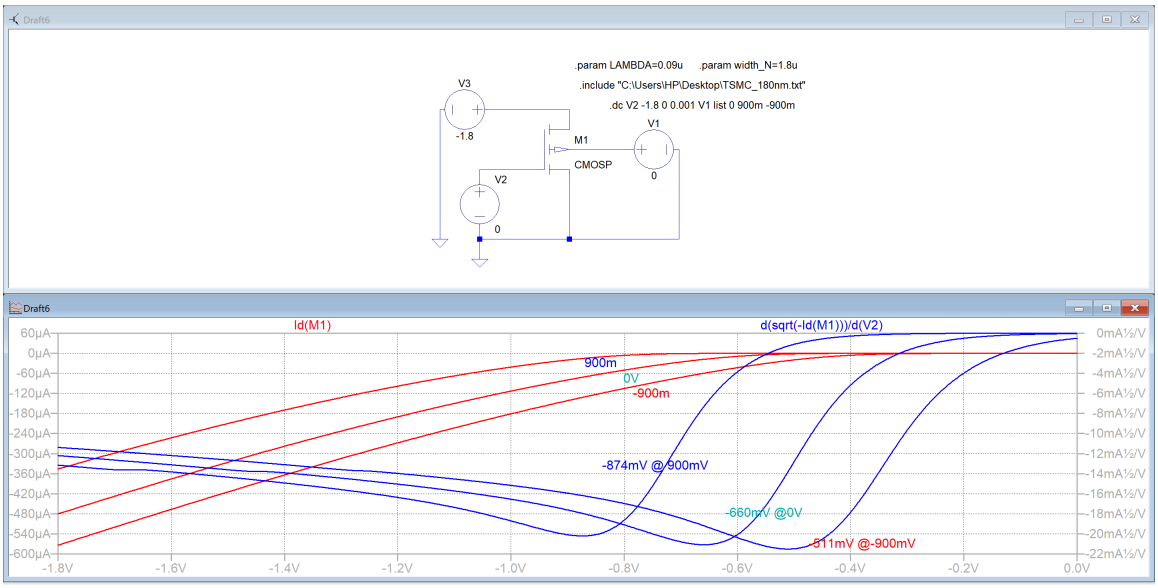
>As Body Voltage increases, Body Source becomes forward biased

>More electrons are released into Body region or p-substrate as VBS ↑ ,the depletion layer region decreases means electrons surrounded across n-substrate decreases, then less VGS is required to drag the electrons from source to drain. So VT ↓ as Concentration of $\bar{e}$ in p-substrate ↑

Increasing the body-source voltage leads to a decrease in the threshold voltage of NMOS.

EXPLANATION:
When explaining the phenomenon of transistor behaviour, two capacitances are considered: the gate-channel capacitance and the channel-body capacitance. In the gate-channel capacitance, the oxide layer acts as a dielectric, while in the channel-body capacitance, the depletion region acts as a capacitance. When the body's terminal voltage increases, it creates a positive charge, which needs to be balanced. To balance this positive charge, the voltage of the channel region becomes more negative. This is because positive charges are transferred to the body terminal side, which acts as the other plate of the channel-body capacitor. As a result, there is an increase in the negative charge or the number of charge carriers in the channel, leading to a decrease in the threshold voltage of the transistor. This means that a lower voltage at the gate terminal is needed to achieve conduction in the transistor. Simply put, the transistor becomes more conductive when the body-source voltage increases, making it easier to control the transistor's behaviour using the gate voltage.

💡 For PMOS:



Since we know,

$$V'_{TH} = V_{TH} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \quad \phi_{F,PMOS} > 0 \quad \gamma < 0$$

So we can claim that,

$$V_{TH,900mV} < V_{TH,0V} < V_{TH,-900mV}$$

which is also depicted in the graph. where { 900mV ,0V ,-900mV} are values of **VBS .**

💡 **RESULTS:**

For VBS=0V,

$\sqrt{-I_D} = \frac{-\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$

>VTH=-558mV

For VBS=900mV,

$\sqrt{-I_D} = \frac{-\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$

>VTH=-776mV

For VBS=-900mV

$\sqrt{-I_D} = \frac{-\partial I_D}{\partial V_{GS}}(V_{GS} - V_{TH})$

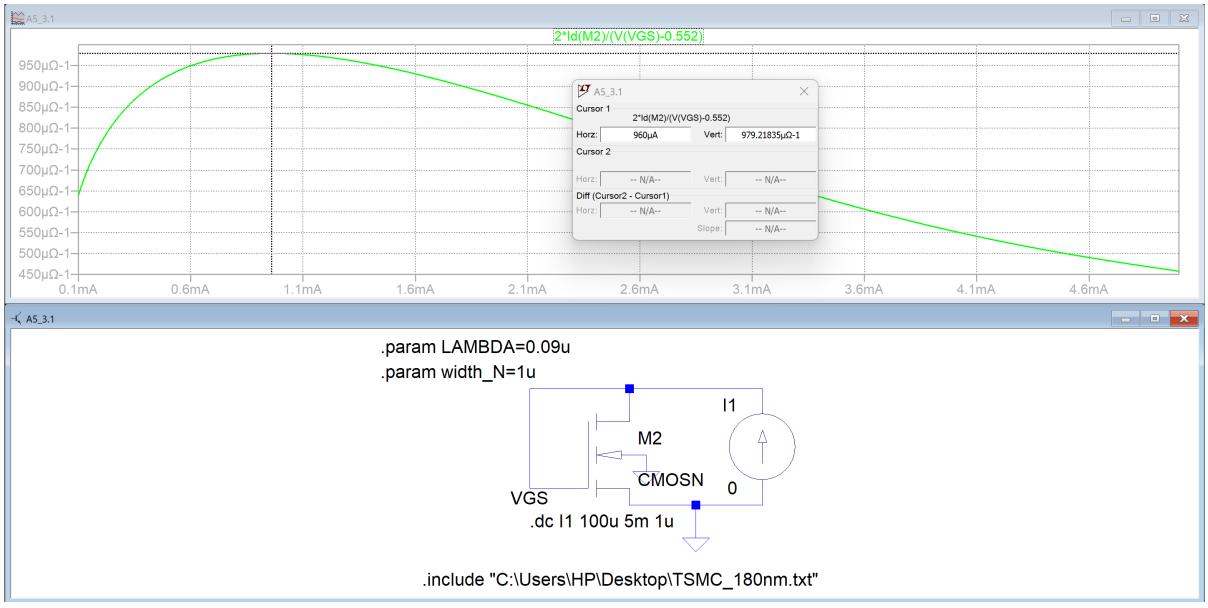
>VTH=-402mV

As Body Voltages increases Body Source becomes reverse Bias then holes in the channel decreases .Since it acts as the positive plate of capacitor.Consequently more negative charge at gate terminal is needed to attaract more holes into the channel and achieve the state of inversions.

In this scenario, we observe that as the body-source voltage becomes more positive, the magnitude of the threshold voltage increases(for PMOS).
This means that a more negative voltage at the gate terminal is required to achieve the conduction in the PMOS transistor.
EXPLANATION:
In PMOS transistors, the polarities of the capacitors are reversed compared to NMOS. The negative plates of their respective capacitors are the gate and body terminals, while the channel acts as the positive plate. This is because PMOS transistors use holes as the charge carriers. When the body voltage becomes more positive, the concentration of holes in the channel decreases,

which leads to a flow of holes from the channel to the body terminal. This happens because the channel acts as the positive plate of the capacitor.
As a result, a more negative charge at the gate terminal is needed to attract more holes into the channel and achieve the state of inversion. To put it simply, increasing the body voltage in PMOS transistors results in a higher threshold voltage. Therefore, a more negative voltage must be applied to the gate terminal to counteract the reduced concentration of holes in the channel and achieve the desired conduction level.

Question 4:



WE KNOW ,

$$g_m = 2I_D/(V_{GS} - V_{TH}) = \mu_n C_{ox} W/L(V_{GS} - V_{TH})$$

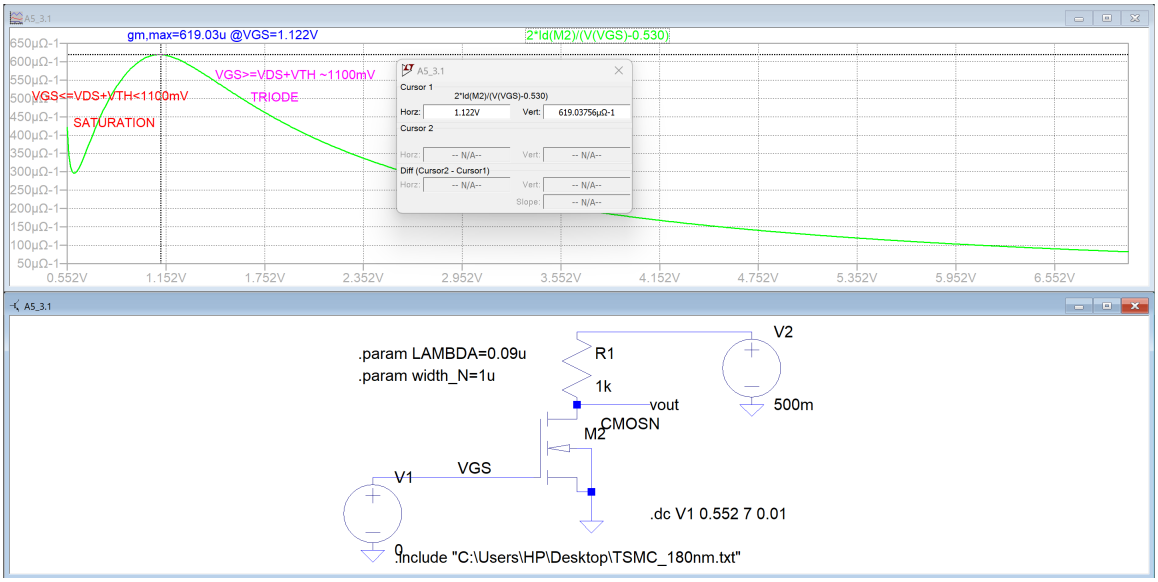
As $\mu_n C_{ox}$ is a MOS parameter whereas W/L is a design parameter and $g_m\ \alpha\ W/L$, we design the parameter as $(W/L)' = 4(W/L)$.

DESIGN PARAMETERS:

$(W/L)' = \frac{4\mu m}{0.18\mu m}$, $\lambda = 0.09\mu m, AS = AD = 1.8 * 10^{-12}m^2, PS = PD = 8.9 * 10^{-6}m^2$ $g_{m,new} = g_m * 4 = 3916.87\mu\Omega^{-1}$

Question 5:

Part A:



IN SATURATION,

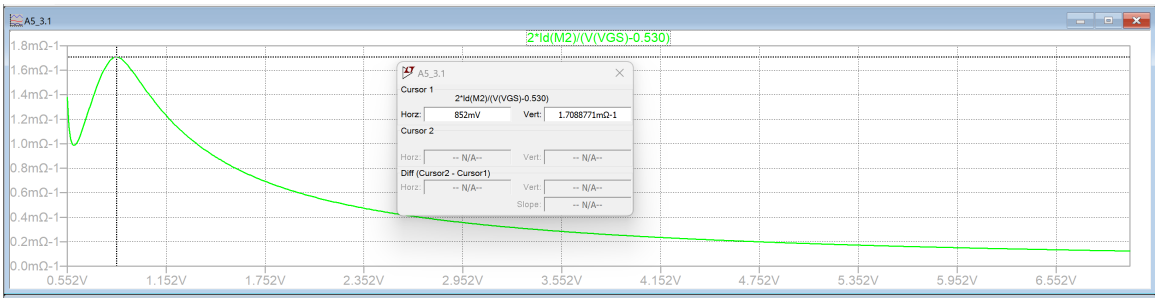
the MOSFET is active ,where drain current is very high and varies linearly with VGS. As a result, transconductance increases with high sensitivity.

IN TRIODE,

Usually ,when MOSFET is in linear mode ,it has low drain currents, In this region ,MOSFET acts like voltage controlled resistor and its transconductance is less as compared with saturation since ID is less

Part B:

gm,max is attained at VGS=852mV



TRADE OFFS:

1)Gain:

$$Gain \ \alpha \ g_m$$

$gm = \mu_n C_{ox} W/L(V_{GS} - V_{TH})$, $hence \ \ g_m \ \alpha \ (W/L).$

2)Swing:

WE Know , V out=VDS,

$$Vout, dc \geq Vin, dc - V_{TH} \quad in \ \ SATURATION$$

Now it also true that $Vout, dc + vout >= Vin + vin - V_{TH} \ \ in \ \ saturation$

> 💡 Now the AC swings which used to reach the verge of saturation and triode at W=1um i,e $Vout = Vin - Vth$ go out of the saturation region as gain increased. So to not defeat the purpose of amplification and get the circuit to be acted as amplifier ,we have to compromise with INPUT SWINGS so that the new smaller swings reach upto verge of triode at max

3)Bandwidth:

When width of the MOSFET is increased ,the gain increased ,along with this there is increase in capacitance.

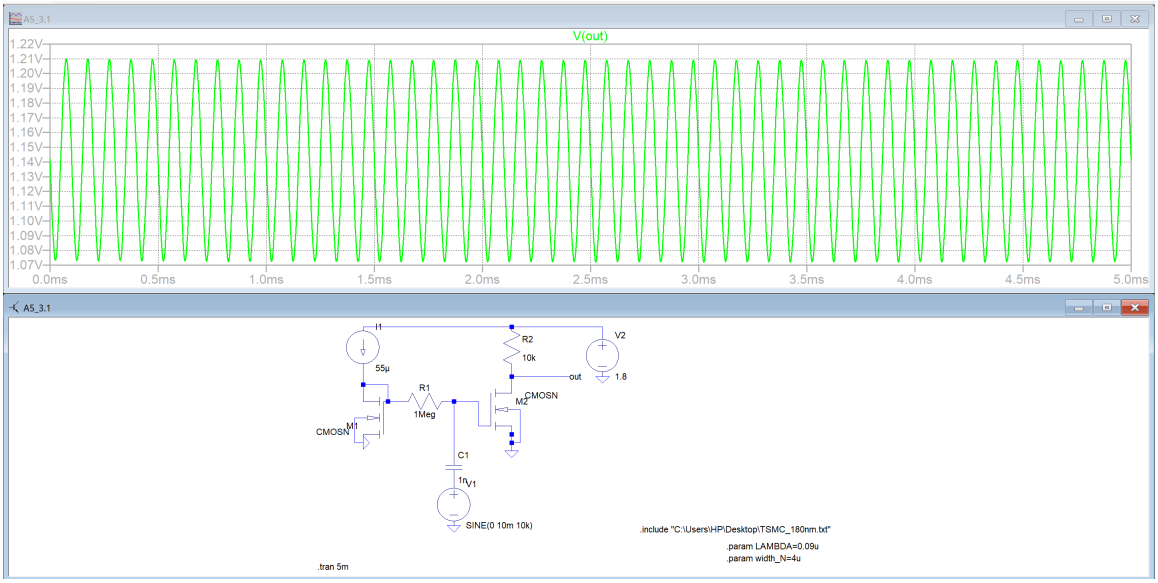
$as \quad W \uparrow \Longrightarrow, A \uparrow, \Longrightarrow C \uparrow = A \uparrow \epsilon_o / d$ hence Overdrive capacitance increases

AS $C \uparrow$,the bandwidth decreases which limits the range of frequencies over which the amplifier can amplify the signals.

>THESE ARE THE TRADEOFFS B/W GAIN,SWING, BANDWIDTH when width is adjusted.

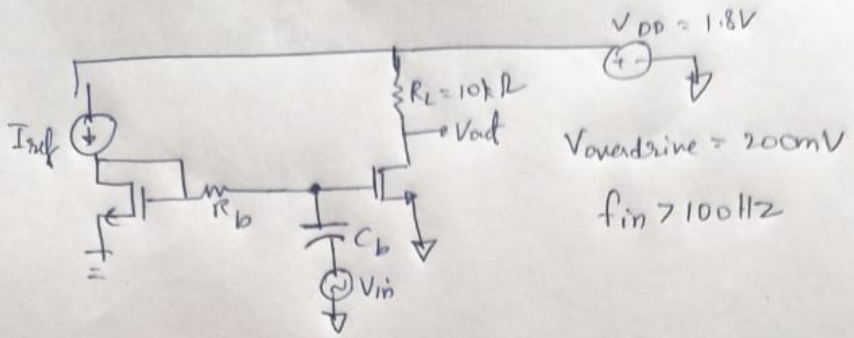
Question 6:

Part A:



Question 6:-

$g_m R_L \geq 5$



Voverdrive = 200mV

$f_{in} > 100Hz$

$g_m(10k) > 5$

$g_m > (500\mu)$

$\frac{2 I_D}{V_{overdrive}} > 500\mu$

$I_D > \frac{500 \times 200mV \times 10^{-6}}{2}$

$5 \times 10^{4} \times 10^{-6} \times 10^{-3}$

$I_D > 50\,\mu A$

$I_{ref} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2$

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2$

$\frac{I_{ref}}{I_D} = \frac{(W/L)_1}{(W/L)_2} = 1$ (as using same transistor)

$I_{ref} = I_D > 50\,\mu A$

$f_{min} \rightarrow \frac{1}{2\pi R_B C_B}$

from previous Q, $\mu_n C_{ox} = 322.3\,\mu A/V^2$.

$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right) V_{overdrive}$.

$\frac{W}{L} > 10 \frac{500\mu}{322.3 \times 10^{-6} \times 200mV}$

$$\frac{W}{L} > \frac{500}{322.3 \times 0.2} \Rightarrow \frac{2500}{322.3}$$

$$\boxed{\frac{W}{L} > 7.756}$$

taking $f_{min} > f_{cutoff}$

$$\frac{1}{2\pi R_B C_B} > 100$$

$$R_B C_B < \frac{1}{2\pi \times 100}$$

lets take $R_B = 1\,Meg$

$$C_B < \frac{1}{2\pi \times 100 \times 10^6}$$

$$C_B < 1.591\,nF$$

$V_1 = 1.8V$

$I(V_1) = 0.000121\,Amp$

$P_1 = 217.8\,mW$

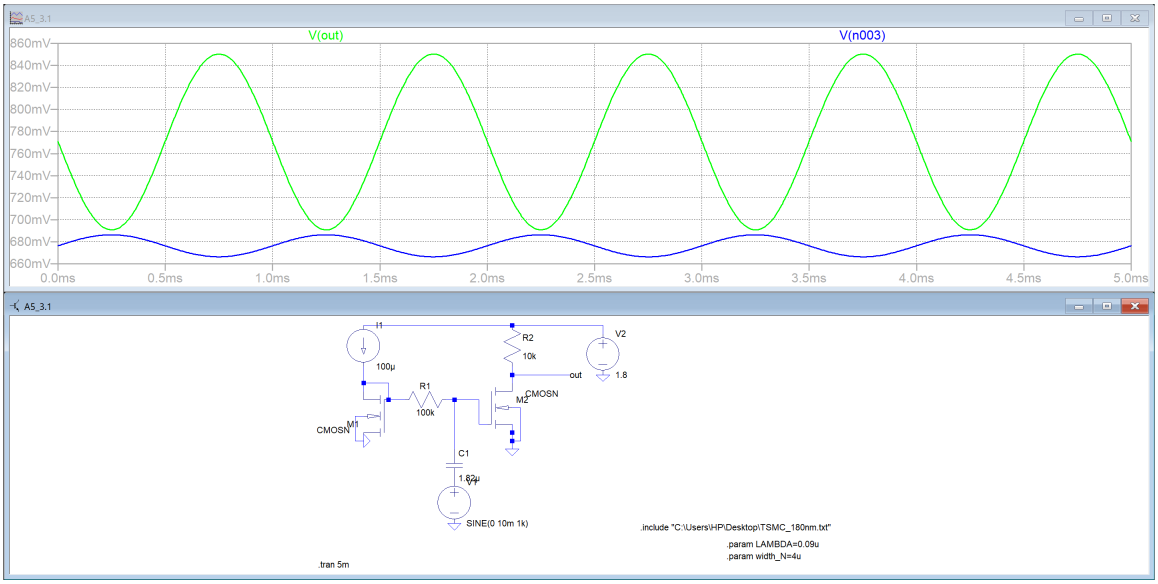
$I_{ref} = 55\mu A$

$V(ref) = 1.198V$

$P_2 = 0.634\,mV$

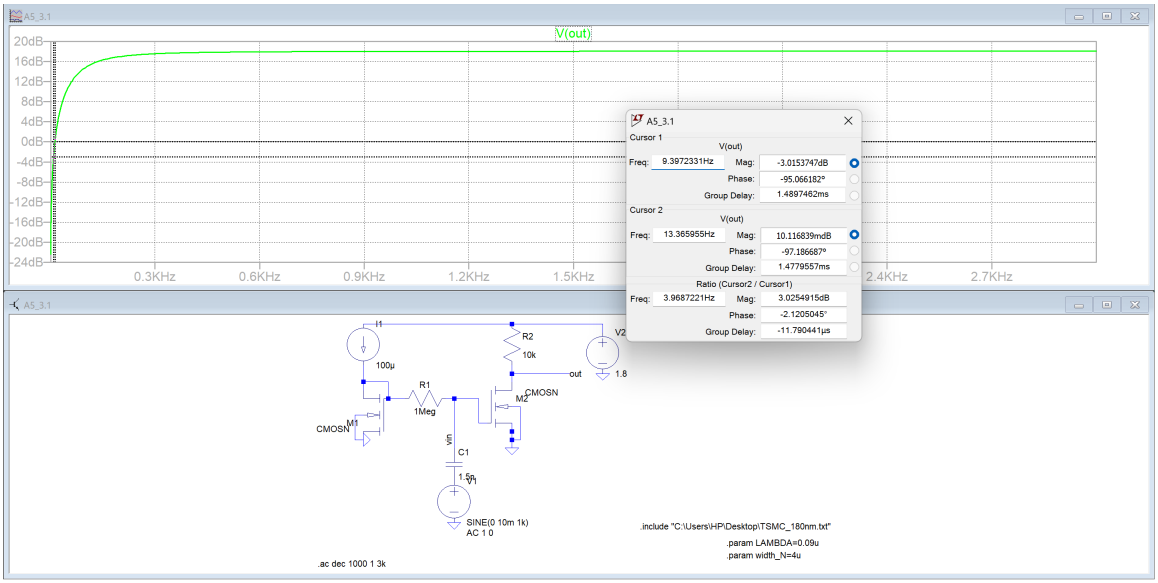
$P_{Total} = 218.4314\,mW$

Part B:

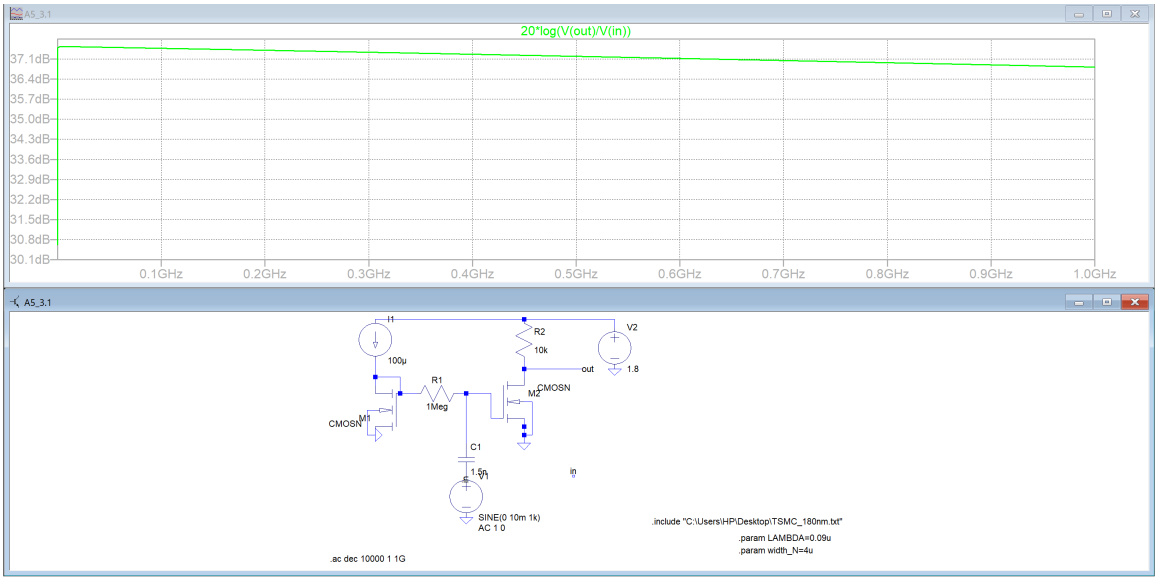


Av= 4.65 which is around 5 as we are neglecting other effects such as Ro and channel length modulation in our calculations.

Part C:



-3dB @ 9.39HZ and Unit band frequency(0dB) @ 14Hz


A5_3.1
20*log(V(out)/V(in))
37.1dB
36.4dB
35.7dB
35.0dB
34.3dB
33.6dB
32.9dB
32.2dB
31.5dB
30.8dB
30.1dB
0.1GHz
0.2GHz
0.3GHz
0.4GHz
0.5GHz
0.6GHz
0.7GHz
0.8GHz
0.9GHz
1.0GHz
A5_3.1
I1
100µ
R1
1Meg
M1
CMOSN
R2
10k
out
V2
1.8
M2
CMOSN
C1
1.5n
in
V1
SINE(0 10m 1k)
AC 1 0
.ac dec 10000 1 1G
.include "C:\Users\HP\Desktop\TSMC_180nm.txt"
.param LAMBDA=0.09u
.param width_N=4u

THANK YOU!!