DE2116D

EXPERIMENT # 8

ASYNCHRONOUS COUNTER

SK MABUNDZA
240576260

Experiment 6 : Asynchronous Counter

1. AIM

This experiment aims to learn how to design and build an asynchronous counter in a breadboard, in this experiment we will learn how to build a counting machine using a flip-flop and understand the function of a flip-flop and its behavior. For this experiment it to be completed, requires the past circuits (assignments). I was assigned to design a counter that counts from 0 to 2 (MOD-3).

2. MATERIALS USED

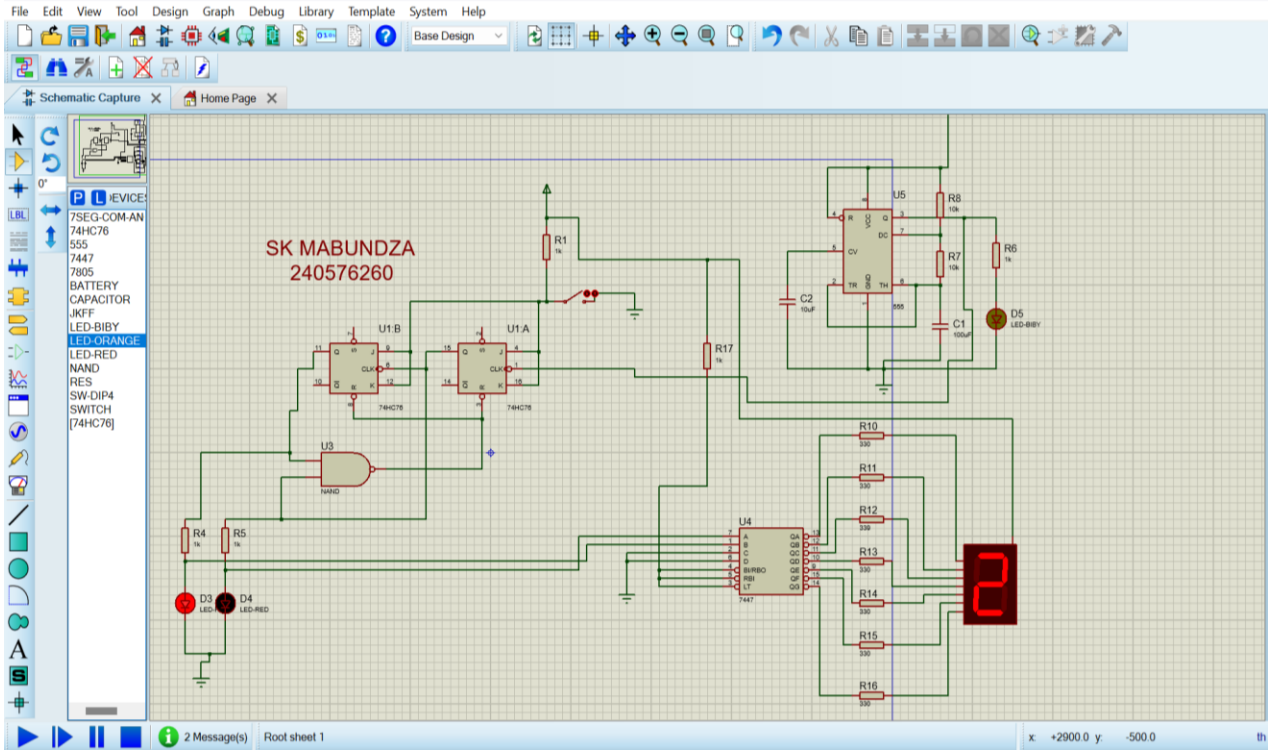
- 2 x 74LS76A / 4027 dual J-K flip-flop.
- Resistors: bunch of 330Ω, and 1.0 kΩ.
- 1 x 7447A BCD/decimal decoder.
- 1 x MAN72 seven-segment display.
- 1 x 555 timer circuit.
- 1 x NAND gate.
- 3 x LEDs.
- 1 x 9V battery
- Breadboard.

3. PROCEDURE

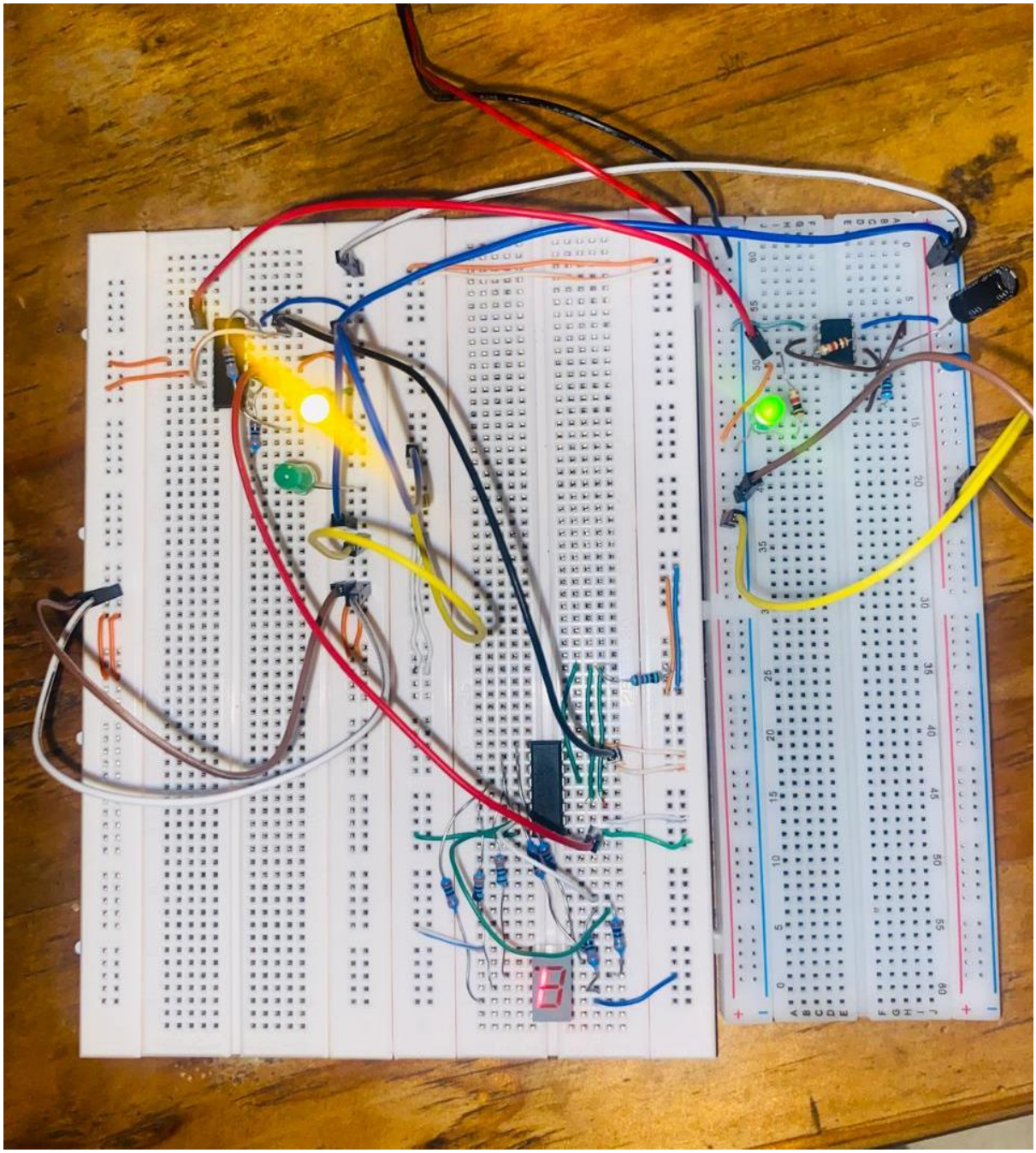
- The 555 timer is already built representing the clock in the experiment's procedure.
- And the decimal decoder and seven-segment display connect also in the past experiment, the only thing you must remove is the switch inputs.
- In the j-k flip flop, the IC is connected to the breadboard bridge.
- Connect the Vcc from the IC (pin 5) to the positive terminal of the breadboard.
- Connect the ground from the IC (pin 13) to the negative terminal of the breadboard.
- The 74LS76A IC contains two j-k flip flops so we are going to use one IC.
- Connect all the J and K inputs of both flip flops (pins 16,4, 12and 9) to the positive terminal.
- Connect the output from the 555-timer circuit to the j-k flip flop (pin 1) clock input.
- Connect the output of the first flip-flop (Q1)(pin 15) to the clock input of the second flip-flop (pin 6) and the 330 resistor to the first LED.
- Connecting the second output of the second flip flop(Q2)(pin 11) to the second 330 resistor to the second LED.

- In the decoder, inputs C and D will be connected to the negative terminal.
- Connect the outputs from the flip flop IC (Q1 and Q2) connect to the decoder input (A and B) respectfully.
- Connecting NAND gate IC to the breadboard.
- Connect the outputs of the flip flops (Q1 and Q2) to the two inputs of the NAND gate.
- Connecting the output from the NAND gate to the RESET inputs of the flip flop (pins 3 and 8).

4. CIRCUIT DIAGRAM (Proteus)



5. PRACTICAL LAYOUT(BREADBOARD)



6. RESULTS

Timing Diagram

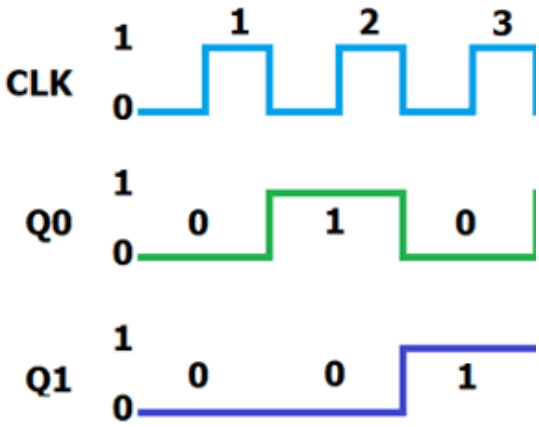


Table results (State sequence)

Clock Pulse	Q1 (MSB)	Q0 (LSB)	Decimal Equivalent
0	0	0	0
1	0	1	1
2	1	0	2
3	Reset to 0 (00)	Reset to 0	

7. CONCLUSION

After we completed building the asynchronous counter circuit and getting the results, the circuit counted from 0 to 2 as assigned, It came to a notice that the ripple to produce these results requires a 555 timer as a clock to the flip-flop input. The results were exactly the same as the timing diagram and the state sequence, where it starts from 0 to 2, and when it reaches 3 it reset to 0.