Simulation Results

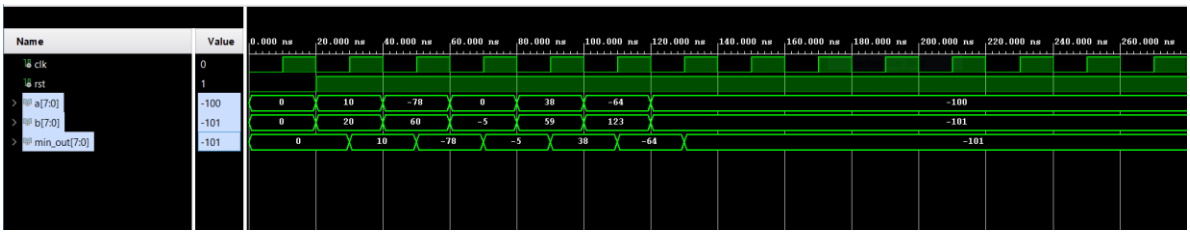

Figure 1. Testbench results of Min_core

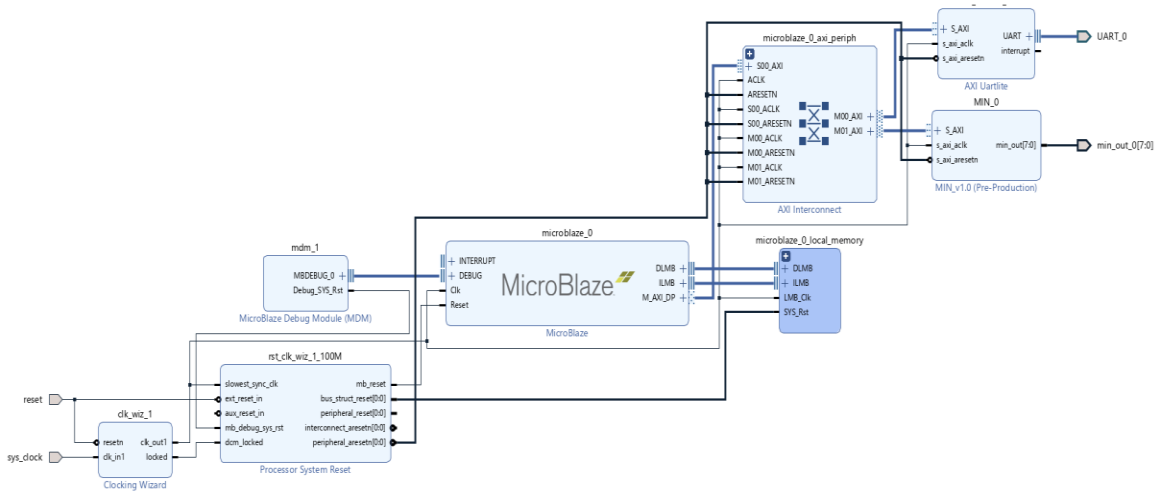

Figure 2. MIN_IP connection diagram

min_out_0 (8)	OUT					
min_out_0[7]	OUT				T10	
min_out_0[6]	OUT				T9	
min_out_0[5]	OUT				J5	
min_out_0[4]	OUT				H5	
min_out_0[3]	OUT				K2	
min_out_0[2]	OUT				H4	
min_out_0[1]	OUT				G4	
min_out_0[0]	OUT				E1	
Scalar ports (0)						

Figure 3. Pin configuration on the FPGA kit

```
Gia tri doc duoc (raw): 0x80
So nho hon la: -128

Nhap so a (trong khoang -128 den 127): -123
Nhap so b (trong khoang -128 den 127): -124
Gia tri doc duoc (raw): 0x84
So nho hon la: -124

Nhap so a (trong khoang -128 den 127): 12
Nhap so b (trong khoang -128 den 127): 123
Gia tri doc duoc (raw): 0xC
So nho hon la: 12

Nhap so a (trong khoang -128 den 127): -12
Nhap so b (trong khoang -128 den 127): 0
Gia tri doc duoc (raw): 0xF4
So nho hon la: -12

Nhap so a (trong khoang -128 den 127):
```

Figure 4. Results on the Terminal

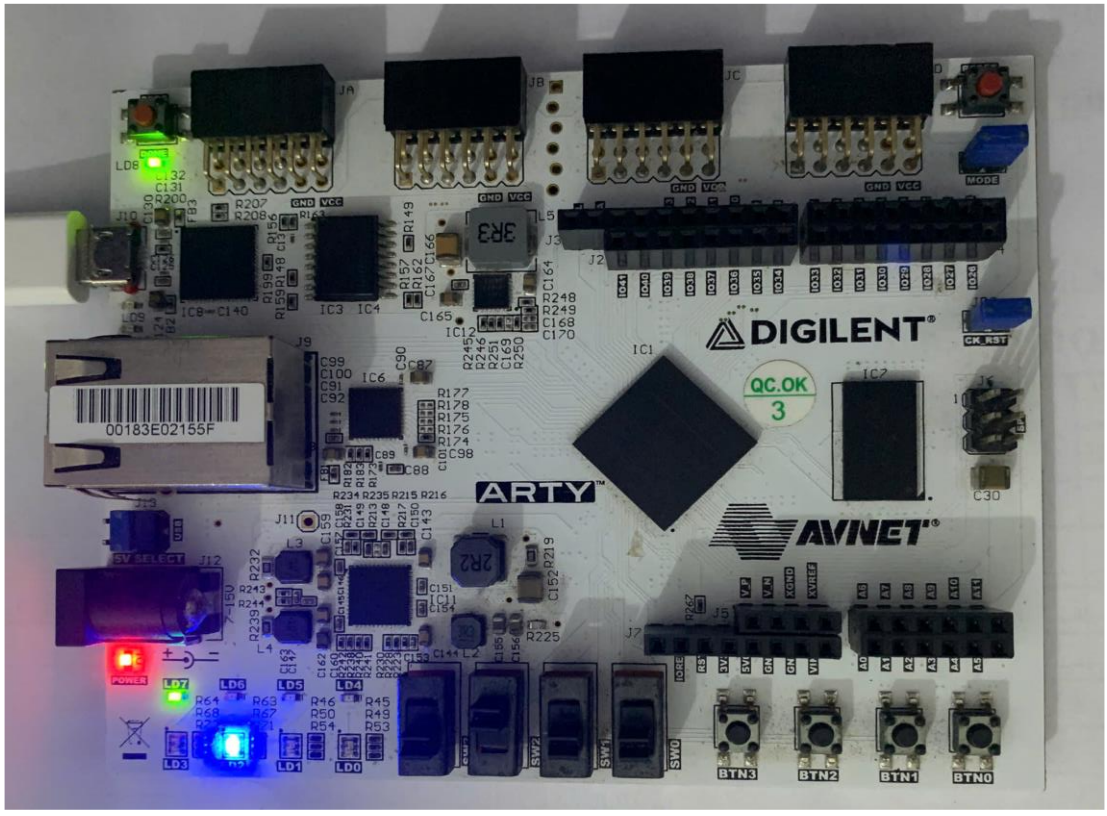

Figure 5. Results on the FPGA Kit

Conclusion:

- The report confirms the successful design and implementation of an IP to find the smallest number between two signed 8-bit integers. The IP has been

successfully deployed on the Vitis platform, and the results are accurately displayed on the Terminal screen. The outcomes demonstrate that the IP operates efficiently, reliably, and fully meets the initial requirements.

- Future development: Investigating and designing an IP to identify the smallest number among multiple numbers, while also focusing on comparing larger values with bit lengths up to 32 bits. This approach aims to fulfill the need for more complex computations in real-world applications.