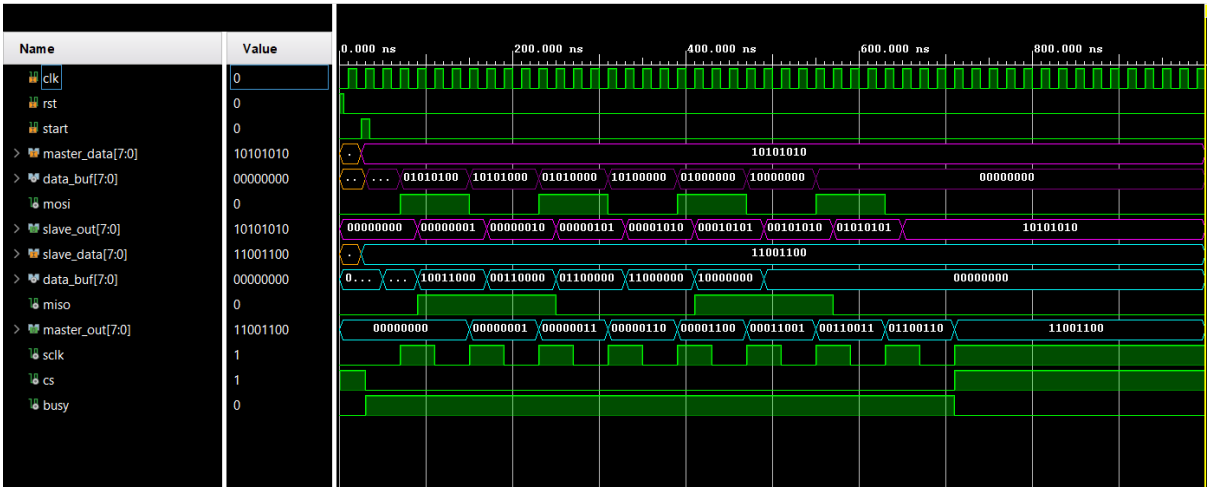
Simulation Results



Application of SPI Design to Read Sensor Values

Scenario: The PmodALS light sensor acts as a slave, transmitting 8-bit data to the Arty-7 35 kit (Master) via the MISO line. A virtual VIO port is used to control the reset and start signals, while the results are monitored on the ILA display.

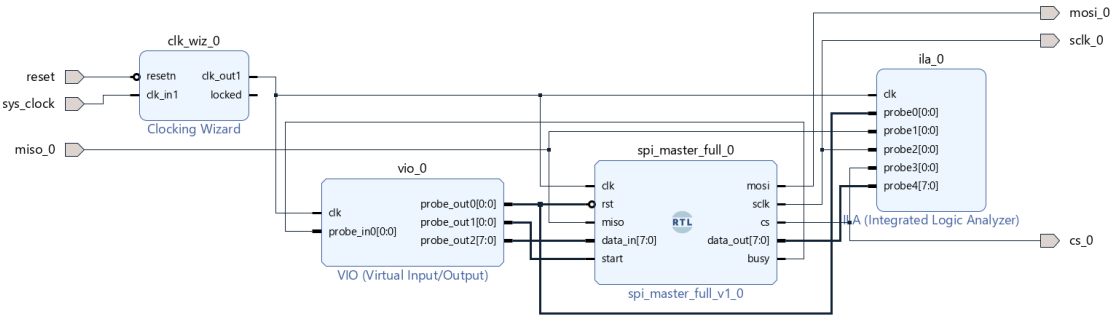


Figure 1. SPI Connection Diagram Between the Sensor and FPGA Kit

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco
All ports (6)									
CLK.SYS_CLOCK_57623 (1)	IN					☑	35	LVCMOS33*	3.300
Scalar ports (1)									
sys_clock	IN	clk			E3	☑	35	LVCMOS33*	3.300
RST.RESET_57623 (1)	IN					☑	35	LVCMOS33*	3.300
Scalar ports (1)									
reset	IN	reset			C2	☑	35	LVCMOS33*	3.300
Scalar ports (4)									
cs_0	OUT				D13	☑	15	LVCMOS33*	3.300
miso_0	IN				A18	☑	15	LVCMOS33*	3.300
mosi_0	OUT				B18	☑	15	LVCMOS33*	3.300
sclk_0	OUT				K16	☑	15	LVCMOS33*	3.300

Figure 2. Pin Configuration for Sensor Communication

hw_vio_1

Name	Value	Activity	Direction	VIO
master_full_i/Net	[B] 0		Output	hw_vio_1
master_full_i/spi_master_full_0_busy	[B] 1		Input	hw_vio_1
master_full_i/vio_0_probe_out1	[B] 1		Output	hw_vio_1
master_full_i/vio_0_probe_out2[7:0]	[H] 00		Output	hw_vio_1

Figure 3. VIO Screen for Controlling

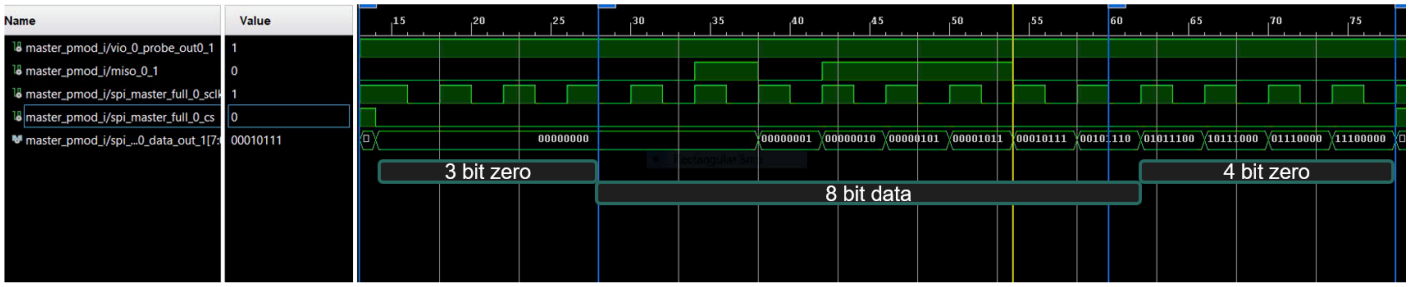


Figure 4. SPI Communication Results Between the Sensor and FPGA Kit on the ILA Display

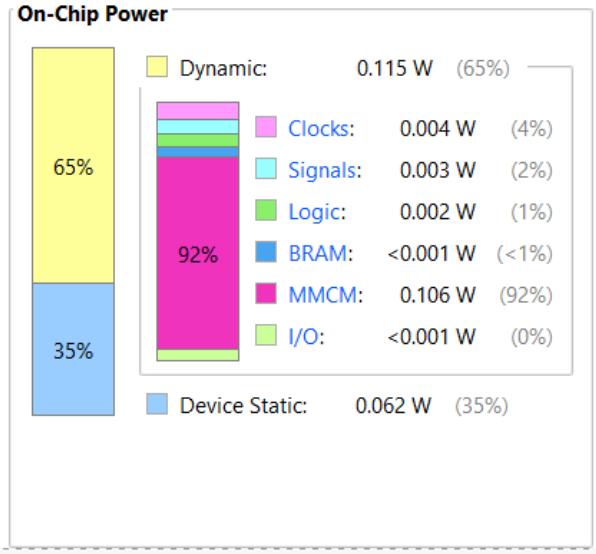
Performance Evaluation:

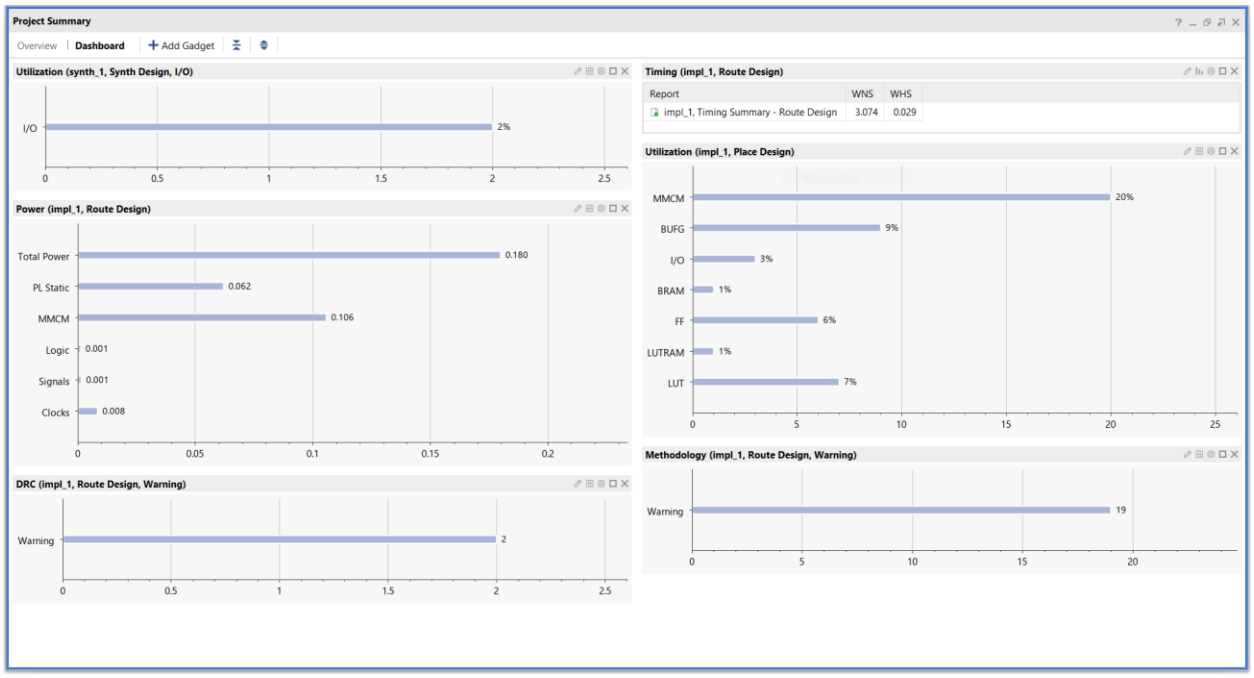
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.177 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.8°C**
Thermal Margin:	74.2°C (15.4 W)
Effective ϑJA:	4.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity





Observations:

The team successfully simulated the data transmission and reception process using SPI communication in Mode 0 while gaining a solid understanding of the PmodALS sensor's operation. During the implementation, the team verified the SPI interface module design and confirmed that data from the PmodALS sensor could be accurately read through the SPI protocol, with the results clearly observable on the ILA display.

However, to enhance the versatility and applicability of SPI communication, further research and development are required to support all SPI modes (Mode 0, 1, 2, 3) and integrate the ability to handle multiple chip select (CS) lines.