Control store data to SDRAM

State	meaning	output			
		clk_read_fifo	data port	addr	wr_en_sdram
Idle	After reset state	0	0	0	0
waitFifo	waitFifoEnough data and SDRAM ready	0	0	0	0
getData1	setClock to get data	1	0	0	0
getData2	clearClock, ready write red data	0	red	addr_red	1
waitSDRAM	wait sdram done	0	0	0	0
GetGreen	ready write green data	0	green	addr_green	1
waitSDRAM	wait sdram done	0	0	0	0
GetBlue	ready write blue data	0	blue	addr_blue	1
waitSDRAM	wait sdram done	0	0	0	0
updatePixelAddr	update pixel addr, check if last pixel	0	0	0	0
finish	set done flag	0	0	0	0

Memory Fetching

state	meaning	output				
		rd_sdram	addr_sdram	wr_ram	addr_ram	data_to_ram
Idle	After reset state	0	0	0	0	from sdram
setAddrSdram0	set addr sdram for ram 0, enable read sdram	1	base+poit0	0	base	from sdram
waitSdramRead	wait sdram done read	0	base+poit0	0	base	from sdram
setAddrRam0	set addr for ram0, enable write ram0	0	base+poit0	1,ram0	base	from sdram
setAddrSdram1	set addr sdram for ram 1, enable read sdram	1	base+poit1	0	base	from sdram
waitSdram	wait sdram done read	0	base+poit1	0	base	from sdram
setAddrRam1	set addr for ram1, enable write ram1	0	base+poit1	1,ram1	base	from sdram
setAddrSdram2	set addr sdram for ram 2, enble read sdram	1	base+poit2	0	base	from sdram
waitSdram	wait sdram done read	0	base+poit2	0	base	from sdram
setAddrRam2	set addr for ram 2, enable write ram 2	0	base+poit2	1,ram2	base	from sdram
update addr	update addr base, check if last data	0	base+poit0	0	base	from sdram
finish	set finish flag	0	0	0	0	from sdram

Memory write back

state	meaning	output				
		wr_sdram	addr_sdram	rd_ram	addr_ram	dataSel
Idle	after reset state	0	0	0	0	0
setAddrRam0	set addr ram 0, ready to read	0	base+poit0	1	base	0
setSdram0	setSdram0, addr, ready to write	1	base+poit0	0	base	0
setAddrRam1	set addr ram 1, ready to read	0	base+poit1	1	base	1
waitSdram	wait Sdram done to write	0	base+poit1	0	base	1
setSdram1	setsdram1, addr, ready to write	1	base+poit1	0	base	1
setAddrRam2	set addr ram 2, ready to read	0	base+poit2	1	base	2
waitSdram	wait Sdram done to write	0	base+poit2	0	base	2
setSdram2	setsdram2, addr, ready to write	1	base+poit2	0	base	2
waitSdram	wait Sdram done to write	0	base+poit2	0	base	2
updateAddrbase	update addr base, check if final data	0	base+poit2	0	base	2
finish	set finish flag	0	0	0	0	0