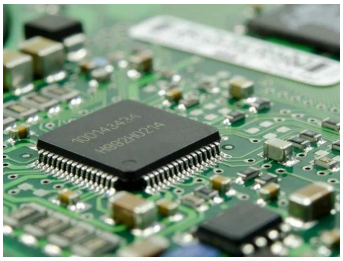
Αρχιτεκτονική Υπολογιστών

Τμήμα Ι (Α –ΚΑΣ)

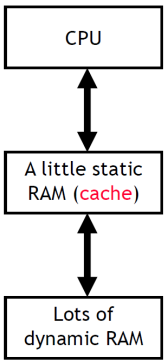
Παραδείγματα Κρυφής Μνήμης

Μάριος Κόνιαρης

Cache



- Associativity
  - Direct Mapped Cache
  - Fully associative
  - N-Way Set Associative
    - 2, 4, 8
    - Direct - mapped w/respect to sets
    - Each set is fully associative with N blocks in it
- Hit / Misses
  - Compulsory Misses → when a program is first started
  - Conflict Misses → two distinct memory addresses map to the same cache location
  - Capacity Misses → cache has a limited size
- Block Replacement Policy
  - Least Recently Used
  - Random
- Write Policy
  - Write Through
  - Write Back
- Multi-level cache
  - L1, L2, L3
- Locality
  - Temporal / Spatial



Memory System Performance

Average Memory Access Time → Hit Time + (Miss Penalty x Miss Rate)