CHAPTER 7

Transistor Amplifiers

IN THIS CHAPTER YOU WILL LEARN

1. How the transistor (a MOSFET or a BJT) can be used to make an amplifier.
2. How to obtain linear amplification from the fundamentally nonlinear MOS and bipolar transistor.
3. How to model the linear operation of a transistor around a bias point by an equivalent circuit that can be used in the analysis and design of transistor amplifiers.
4. The three basic ways to connect a MOSFET or a BJT to construct amplifiers with different properties.
5. Practical circuits for MOS and bipolar transistor amplifiers that can be constructed using discrete components.

Introduction

Having studied the two major transistor types, the MOSFET (Chapter 5) and the BJT (Chapter 6), we now begin the study of their application. There are two distinctly different kinds of transistor application: as a switch, in the design of digital circuits (Chapters 14–16) and as a controlled source, in the design of amplifiers for analog circuits. This chapter and the subsequent six focus on the latter application, namely, the use of the transistor in the design of a variety of amplifier types.

Since the basic principles that underlie the use of the MOSFET and the BJT in amplifier design are the same, the two devices are studied together in this chapter. Besides providing some economy in presentation, this unified study enables us to make important comparisons between MOS and bipolar amplifiers.

The bulk of this chapter is concerned with the fundamental principles and concepts that are the basis for the application of transistors in amplifier design: We study in detail the models that are used to represent both transistor types in the analysis and design of small-signal linear amplifiers. We also study the three basic configurations in which each of the two transistor types can be connected to realize an amplifier.

The chapter concludes with examples of discrete-circuit amplifiers. These are circuits that can be assembled using discrete transistors, resistors, and capacitors on printed-circuit boards (PCBs). They predominantly use BJTs, and their design differs in significant ways from the design of integrated-circuit (IC) amplifiers. The latter predominantly use MOSFETs, and their study begins in Chapter 8. However, the fundamental principles and concepts introduced in this chapter apply equally well to both discrete and integrated amplifiers.

7.1 Basic Principles

7.1.1 The Basis for Amplifier Operation

The basis for the application of the transistor (a MOSFET or a BJT) in amplifier design is that when the device is operated in the active region, a voltage-controlled current source is realized. Specifically, when a MOSFET is operated in the saturation or pinch-off region, also referred to in this chapter as the active region, the voltage between gate and source, v_{GS}, controls the drain current i_D according to the square-law relationship which, for an NMOS transistor, is expressed as

$$i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2 \tag{7.1}$$

We note that in this first-order model of MOSFET operation, the drain current i_D does not depend on the drain voltage v_{DS} because the channel is pinched off at the drain end,[1] thus "isolating" the drain.

Similarly, when a BJT is operated in the active region, the base-emitter voltage v_{BE} controls the collector current i_C according to the exponential relationship which, for an *npn* transistor, is expressed as

$$i_C = I_S e^{v_{BE}/V_T} \tag{7.2}$$

Here, this first-order model of BJT operation indicates that the collector current i_C does not depend on the collector voltage v_{CE} because the collector–base junction is reverse biased, thus "isolating" the collector.

Figure 7.1 shows an NMOS transistor and an *npn* transistor operating in the active mode. Observe that for the NMOS transistor, the pinch-off condition is ensured by keeping $v_{DS} \geq v_{OV}$. Since the overdrive voltage $v_{OV} = v_{GS} - V_{tn}$, this condition implies that $v_{GD} \leq V_{tn}$, which indeed ensures channel pinch-off at the drain end.

Similarly, for the *npn* transistor in Fig. 7.1(b), the CBJ reverse-bias condition is ensured by keeping $v_{CE} \geq 0.3$ V. Since v_{BE} is usually in the vicinity of 0.7 V, v_{BC} is thus kept

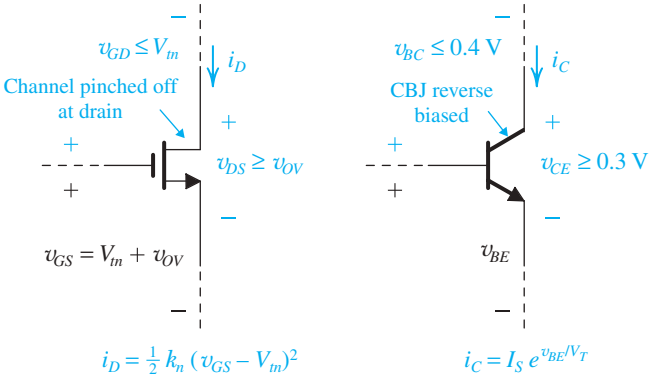


Figure 7.1 Operating (**a**) an NMOS transistor and (**b**) an *npn* transistor in the active mode. Note that $v_{GS} = V_{tn} + v_{OV}$ and $v_{DS} \geq v_{OV}$; thus $v_{GD} \leq V_{tn}$, which ensures channel pinch-off at the drain end. Similarly, $v_{BE} \simeq 0.7$ V, and $v_{CE} \geq 0.3$ V results in $v_{BC} \leq 0.4$ V, which is sufficient to keep the CBJ from conducting.

[1] To focus on essentials, we shall neglect the Early effect until a later point.

smaller than 0.4 V, which is sufficient to prevent this relatively large-area junction from conducting.

Although we used NMOS and *npn* transistors to illustrate the conditions for active-mode operation, similar conditions apply for PMOS and *pnp* transistors, as studied in Chapters 5 and 6, respectively.

Finally, we note that the control relationships in Eqs. (7.1) and (7.2) are nonlinear. Nevertheless, we shall shortly devise a technique for obtaining almost-linear amplification from these fundamentally nonlinear devices.

7.1.2 Obtaining a Voltage Amplifier

From the above we see that the transistor is basically a transconductance amplifier: that is, an amplifier whose input signal is a voltage and whose output signal is a current. More commonly, however, one is interested in voltage amplifiers. A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output. Doing this for a MOSFET results in the simple amplifier circuit shown in Fig. 7.2(a). Here v_{GS} is the input voltage, R_D (known as a **load resistance**) converts the drain current i_D to a voltage ($i_D R_D$), and V_{DD} is the supply voltage that powers up the amplifier and, together with R_D, establishes operation in the active region, as will be shown shortly.

In the amplifier circuit of Fig. 7.2(a) the output voltage is taken between the drain and ground, rather than simply across R_D. This is done because of the need to maintain a common ground reference between the input and the output. The output voltage v_{DS} is given by

$$v_{DS} = V_{DD} - i_D R_D \tag{7.3}$$

Thus it is an inverted version (note the minus sign) of $i_D R_D$ that is shifted by the constant value of the supply voltage V_{DD}.

An exactly similar arrangement applies for the BJT amplifier, as illustrated in Fig. 7.2(c). Here the output voltage v_{CE} is given by

$$v_{CE} = V_{CC} - i_C R_C \tag{7.4}$$

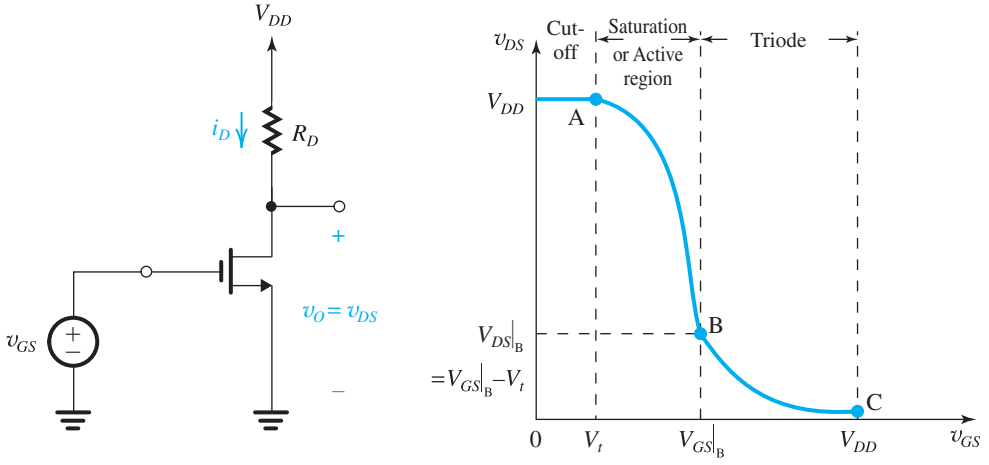


Figure 7.2 (**a**) An NMOS amplifier and (**b**) its VTC; and (**c**) an *npn* amplifier and (**d**) its VTC.

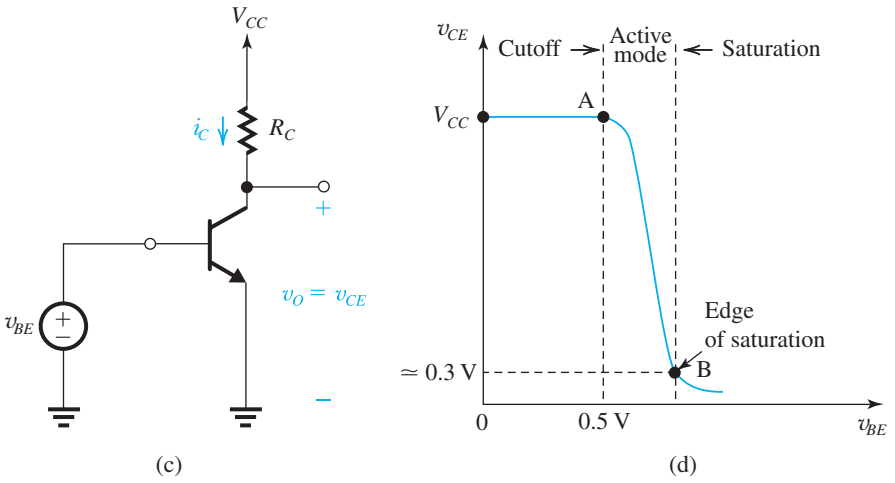


Figure 7.2 *continued*

7.1.3 The Voltage-Transfer Characteristic (VTC)

A useful tool that provides insight into the operation of an amplifier circuit is its voltage-transfer characteristic (VTC). This is simply a plot (or a clearly labeled sketch) of the output voltage versus the input voltage. For the MOS amplifier in Fig. 7.2(a), this is the plot of v_{DS} versus v_{GS} shown in Fig. 7.2(b).

Observe that for $v_{GS} < V_t$, the transistor is cut off, $i_D = 0$ and, from Eq. (7.3), $v_{DS} = V_{DD}$. As v_{GS} exceeds V_t, the transistor turns on and v_{DS} decreases. However, since initially v_{DS} is still high, the MOSFET will be operating in saturation or the active region. This continues as v_{GS} is increased until the value of v_{GS} is reached that results in v_{DS} becoming lower than v_{GS} by V_t volts [point B on the VTC in Fig. 7.2(b)]. For v_{GS} greater than that at point B, the transistor operates in the triode region and v_{DS} decreases more slowly.

The VTC in Fig. 7.2(b) indicates that the segment of greatest slope (hence potentially the largest amplifier gain) is that labeled AB, which corresponds to operation in the active region. When a MOSFET is operated as an amplifier, its operating point is confined to the segment AB at all times. An expression for the segment AB can be obtained by substituting for i_D in Eq. (7.3) by its active-region value from Eq. (7.1), thus

$$v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_t)^2 \tag{7.5}$$

This is obviously a nonlinear relationship. Nevertheless, linear (or almost-linear) amplification can be obtained by using the technique of biasing the MOSFET. Before considering biasing, however, it is useful to determine the coordinates of point B, which is at the boundary between the saturation and the triode regions of operation. These can be obtained by substituting in Eq. (7.5), $v_{GS} = V_{GS}\big|_B$ and $v_{DS} = V_{DS}\big|_B = V_{GS}\big|_B - V_t$. The result is

$$V_{GS}\big|_B = V_t + \frac{\sqrt{2k_n R_D V_{DD} + 1} - 1}{k_n R_D} \tag{7.6}$$

Point B can be alternatively characterized by the overdrive voltage

$$V_{OV}\big|_{\mathrm{B}} \equiv V_{GS}\big|_{\mathrm{B}} - V_t = \frac{\sqrt{2k_nR_DV_{DD}+1}-1}{k_nR_D} \tag{7.7}$$

and

$$V_{DS}\big|_{\mathrm{B}} = V_{OV}\big|_{\mathrm{B}} \tag{7.8}$$

EXERCISE

7.1 Consider the amplifier of Fig. 7.2(a) with $V_{DD} = 1.8$ V, $R_D = 17.5$ kΩ, and with a MOSFET specified to have $V_t = 0.4$ V, $k_n = 4$ mA/V^2, and $\lambda = 0$. Determine the coordinates of the end points of the active-region segment of the VTC. Also, determine $V_{DS}\big|_C$ assuming $V_{GS}\big|_C = V_{DD}$.
Ans. A: 0.4 V, 1.8 V; B: 0.613 V, 0.213 V; $V_{DS}\big|_C = 18$ mV

An exactly similar development applies to the BJT case. This is illustrated in Fig. 7.2(c) and (d). In this case, over the active-region or amplifier segment AB, the output voltage v_{CE} is related to the input voltage v_{BE} by

$$v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T} \tag{7.9}$$

Here also, the input–output relationship is nonlinear. Nevertheless, linear (or almost-linear) amplification can be obtained by using the biasing technique discussed next.

7.1.4 Obtaining Linear Amplification by Biasing the Transistor

Biasing enables us to obtain almost-linear amplification from the MOSFET and the BJT. The technique is illustrated for the MOSFET case in Fig. 7.3(a). A dc voltage V_{GS} is selected to obtain operation at a point Q on the segment AB of the VTC. How to select an appropriate location for the bias point Q will be discussed shortly. For the time being, observe that the coordinates of Q are the dc voltages V_{GS} and V_{DS}, which are related by

$$V_{DS} = V_{DD} - \frac{1}{2}k_nR_D(V_{GS} - V_t)^2 \tag{7.10}$$

Point Q is known as the **bias point** or the **dc operating point**. Also, since at Q no signal component is present, it is also known as the **quiescent point** (which is the origin of the symbol Q).

Next, the signal to be amplified, v_{gs}, a function of time t, is superimposed on the bias voltage V_{GS}, as shown in Fig. 7.4(a). Thus the total instantaneous value of v_{GS} becomes

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

The resulting $v_{DS}(t)$ can be obtained by substituting for $v_{GS}(t)$ into Eq. (7.5). Graphically, we can use the VTC to obtain $v_{DS}(t)$ point by point, as illustrated in Fig. 7.4(b). Here we show

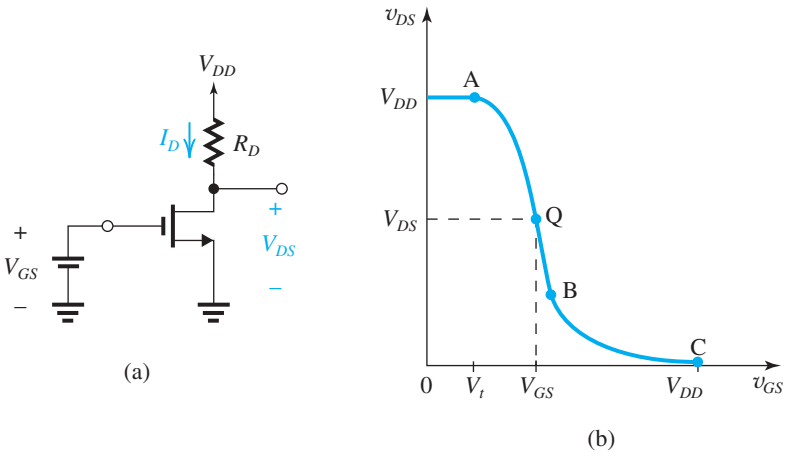


Figure 7.3 Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.

the case of v_{gs} being a triangular wave of "small" amplitude. Specifically, the amplitude of v_{gs} is small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. The shorter the segment, the greater the linearity achieved, and the closer to an ideal triangular wave the signal component at the output, v_{ds}, will be. This is the essence of obtaining linear amplification from the nonlinear MOSFET.

Before leaving Fig. 7.4(b) we wish to draw the reader's attention to the consequence of increasing the amplitude of the signal v_{gs}. As the instantaneous operating point will no longer be confined to the almost-linear segment of the VTC, the output signal v_{ds} will deviate from its ideal triangular shape; that is, it will exhibit nonlinear distortion. Worse yet, if the input signal amplitude becomes sufficiently large, the instantaneous operating point may leave the segment AB altogether. If this happens at the negative peaks of v_{gs}, the transistor will cut off for a portion of the cycle and the positive peaks of v_{ds} will be "clipped off." If it occurs at the positive peaks of v_{gs}, the transistor will enter the triode region for a portion of the cycle, and the negative peaks of v_{ds} will become flattened. It follows that the selection of the location of the bias point Q can have a profound effect on the maximum allowable amplitude of v_{ds}, referred to as the *allowable signal swing at the output*. We will have more to say later on this important point.

An exactly parallel development can be applied to the BJT amplifier. In fact, all we need to do is replace the NMOS transistor in Figs. 7.3 and 7.4 with an *npn* transistor and change the voltage and current symbols to their BJT counterparts. The resulting bias point Q will be characterized by dc voltages V_{BE} and V_{CE}, which are related by

$$V_{CE} = V_{CC} - R_C I_S e^{V_{BE}/V_T} \tag{7.11}$$

and a dc current I_C,

$$I_C = I_S e^{V_{BE}/V_T} \tag{7.12}$$

Also, superimposing a small-signal v_{be} on the dc bias voltage V_{BE} results in

$$v_{BE}(t) = V_{BE} + v_{be}(t)$$

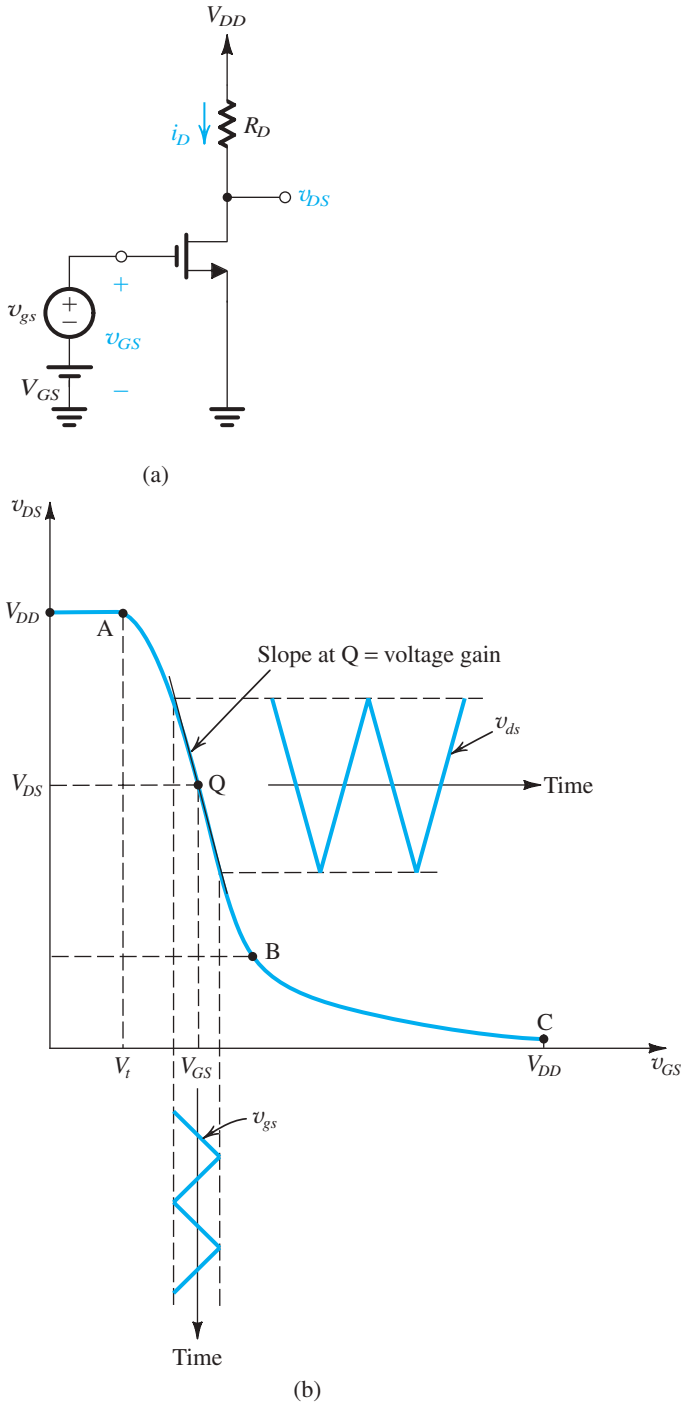


Figure 7.4 The MOSFET amplifier with a small time-varying signal $v_{gs}(t)$ superimposed on the dc bias voltage V_{GS}. The MOSFET operates on a short almost-linear segment of the VTC around the bias point Q and provides an output voltage $v_{ds} = A_v v_{gs}$.

which can be substituted into Eq. (7.9) to obtain the total instantaneous value of the output voltage $v_{CE}(t)$. Here again, almost-linear operation is obtained by keeping v_{be} small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. Similar comments also apply to the maximum allowable signal swing at the output.

7.1.5 The Small-Signal Voltage Gain

The MOSFET Case Consider the MOSFET amplifier in Fig. 7.4(a). If the input signal v_{gs} is kept small, the corresponding signal at the output v_{ds} will be nearly proportional to v_{gs} with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q. This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q,

$$A_v = \left.\frac{dv_{DS}}{dv_{GS}}\right|_{v_{GS}=V_{GS}} \tag{7.13}$$

Utilizing Eq. (7.5) we obtain

$$A_v = -k_n(V_{GS} - V_t)R_D \tag{7.14}$$

which can be expressed in terms of the overdrive voltage at the bias point, V_{OV}, as

$$A_v = -k_n V_{OV} R_D \tag{7.15}$$

We make the following observations on this expression for the voltage gain.

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a 180° phase shift between the input and the output. This inversion is obvious in Fig. 7.4(b) and should have been anticipated from Eq. (7.5).
2. The gain is proportional to the load resistance R_D, to the transistor transconductance parameter k_n, and to the overdrive voltage V_{OV}. This all makes intuitive sense.

Another simple and insightful expression for the voltage gain A_v can be derived by recalling that the dc current in the drain at the bias point is related to V_{OV} by

$$I_D = \frac{1}{2}k_n V_{OV}^2$$

This equation can be combined with Eq. (7.15) to obtain

$$A_v = -\frac{I_D R_D}{V_{OV}/2} \tag{7.16}$$

That is, the gain is simply the ratio of the dc voltage drop across the load resistance R_D to $V_{OV}/2$. It can be expressed in the alternative form

$$A_v = -\frac{V_{DD} - V_{DS}}{V_{OV}/2} \tag{7.17}$$

Since the maximum slope of the VTC in Fig. 7.4(b) occurs at point B, the maximum gain magnitude $|A_{v\max}|$ is obtained by biasing the transistor at point B,

$$|A_{v\max}| = \frac{V_{DD} - V_{DS}|_{\text{B}}}{V_{OV}|_{\text{B}}/2}$$

and since $V_{DS}\big|_B = V_{OV}\big|_B$,

$$|A_{v\max}| = \frac{V_{DD} - V_{OV}\big|_B}{V_{OV}\big|_B/2} \tag{7.18}$$

where $V_{OV}\big|_B$ is given by Eq. (7.7). Of course, this result is only of theoretical importance since biasing at B would leave no room for negative signal swing at the output. Nevertheless, the result in Eq. (7.18) is valuable as it provides an upper bound on the magnitude of voltage gain achievable from this basic amplifier circuit. As an example, for a discrete-circuit amplifier operated with $V_{DD} = 5$ V and $V_{OV}\big|_B = 0.5$ V, the maximum achievable gain is 18 V/V. An integrated-circuit amplifier utilizing a modern submicron MOSFET operated with $V_{DD} = 1.3$ V and with $V_{OV}\big|_B = 0.2$ V realizes a maximum gain of 11 V/V.

Finally, note that to maximize the gain, the bias point Q should be as close to point B as possible, consistent with the required signal swing at the output. This point will be explored further in the end-of-chapter problems.

Example 7.1

Consider the amplifier circuit shown in Fig. 7.4(a). The transistor is specified to have $V_t = 0.4$ V, $k_n' = 0.4$ mA/V^2, $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8$ V, $R_D = 17.5$ kΩ, and $V_{GS} = 0.6$ V.

(a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV}, I_D, V_{DS}, and A_v.
(b) What is the maximum symmetrical signal swing allowed at the drain? Hence, find the maximum allowable amplitude of a sinusoidal v_{gs}.

Solution

(a) With $V_{GS} = 0.6$ V, $V_{OV} = 0.6 - 0.4 = 0.2$ V. Thus,

$$\begin{aligned} I_D &= \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2 \\ &= \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08 \text{ mA} \\ V_{DS} &= V_{DD} - R_D I_D \\ &= 1.8 - 17.5 \times 0.08 = 0.4 \text{ V} \end{aligned}$$

Since V_{DS} is greater than V_{OV}, the transistor is indeed operating in saturation. The voltage gain can be found from Eq. (7.15),

$$\begin{aligned} A_v &= -k_n V_{OV} R_D \\ &= -0.4 \times 10 \times 0.2 \times 17.5 \\ &= -14 \text{ V/V} \end{aligned}$$

An identical result can be found using Eq. (7.17).

(b) Since $V_{OV} = 0.2$ V and $V_{DS} = 0.4$ V, we see that the maximum allowable negative signal swing at the drain is 0.2 V. In the positive direction, a swing of +0.2 V would not cause the transistor to

Example 7.1 *continued*

cut off (since the resulting v_{DS} would be still lower than V_{DD}) and thus is allowed. Thus the maximum symmetrical signal swing allowable at the drain is ±0.2 V. The corresponding amplitude of v_{gs} can be found from

$$\hat{v}_{gs} = \frac{\hat{v}_{ds}}{|A_v|} = \frac{0.2\text{ V}}{14} = 14.2\text{ mV}$$

Since $\hat{v}_{gs} \ll V_{OV}$, the operation will be reasonably linear (more on this in later sections).

Greater insight into the issue of allowable signal swing can be obtained by examining the signal waveforms shown in Fig. 7.5. Note that for the MOSFET to remain in saturation at the negative peak of v_{ds}, we must ensure that

$$v_{DS\min} \geq v_{GS\max} - V_t$$

that is,

$$0.4 - |A_v|\hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

which results in

$$\hat{v}_{gs} \leq \frac{0.2}{|A_v| + 1} = 13.3\text{ mV}$$

This result differs slightly from the one obtained earlier.

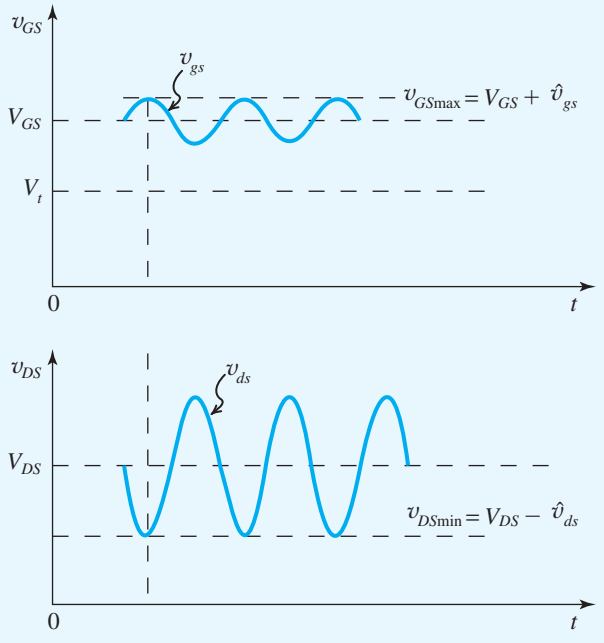


Figure 7.5 Signal waveforms at gate and drain for the amplifier in Example 7.1. Note that to ensure operation in the saturation region at all times, $v_{DS\min} \geq v_{GS\max} - V_t$.

EXERCISE

D7.2 For the amplifier circuit studied in Example 7.1, create two alternative designs, each providing a voltage gain of −10 by (a) changing R_D while keeping V_{OV} constant and (b) changing V_{OV} while keeping R_D constant. For each design, specify V_{GS}, I_D, R_D, and V_{DS}.

Ans. (a) 0.6 V, 0.08 mA, 12.5 kΩ, 0.8 V; (b) 0.54 V, 0.04 mA, 17.5 kΩ, 1.1 V

The BJT Case A similar development can be used to obtain the small-signal voltage gain of the BJT amplifier shown in Fig. 7.6,

$$A_v = \left.\frac{dv_{CE}}{dv_{BE}}\right|_{v_{BE}=V_{BE}} \tag{7.19}$$

Utilizing Eq. (7.9) together with Eq. (7.12), we obtain

$$A_v = -\left(\frac{I_C}{V_T}\right)R_C \tag{7.20}$$

We make the following observations on this expression for the voltage gain:

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a 180° phase shift between the input and the output. This inversion should have been anticipated from Eq. (7.9).
2. The gain is proportional to the collector bias current I_C and to the load resistance R_C.

Additional insight into the voltage gain A_v can be obtained by expressing Eq. (7.20) as

$$A_v = -\frac{I_C R_C}{V_T} \tag{7.21}$$

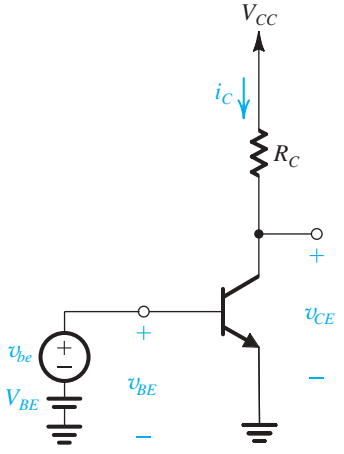


Figure 7.6 BJT amplifier biased at a point Q, with a small voltage signal v_{be} superimposed on the dc bias voltage V_{BE}. The resulting output signal v_{ce} appears superimposed on the dc collector voltage V_{CE}. The amplitude of v_{ce} is larger than that of v_{be} by the voltage gain A_v.

That is, the gain is the ratio of the dc voltage drop across the load resistance R_C to the physical constant V_T (recall that the thermal voltage $V_T \simeq 25$ mV at room temperature). This relationship is similar in form to that for the MOSFET (Eq. 7.16) except that here the denominator is a physical constant (V_T) rather than a design parameter ($V_{OV}/2$). Usually, $V_{OV}/2$ is larger than (V_T), thus we can obtain higher voltage gain from the BJT amplifier than from the MOSFET amplifier. This should not be surprising, as the exponential i_C–v_{BE} relationship is much steeper than the square-law relationship i_D–v_{GS}.

The gain A_v in Eq. (7.21) can be expressed alternately as

$$A_v = -\frac{V_{CC} - V_{CE}}{V_T} \tag{7.22}$$

from which we see that maximum gain is achieved when V_{CE} is at its minimum value of about 0.3 V,

$$|A_{v\max}| = \frac{V_{CC} - 0.3}{V_T} \tag{7.23}$$

Here again, this is only a theoretical maximum, since biasing the BJT at the edge of saturation leaves no room for negative signal swing at the output. Equation (7.23) nevertheless provides an upper bound on the voltage gain achievable from the basic BJT amplifier. As an example, for $V_{CC} = 5$ V, the maximum gain is 188 V/V, considerably larger than in the MOSFET case. For modern low-voltage technologies, a V_{CC} of 1.3 V provides a gain of 40 V/V, again much larger than the MOSFET case. The reader should not, however, jump to the conclusion that the BJT is preferred to the MOSFET in the design of modern integrated-circuit amplifiers; in fact, the opposite is true, as we shall see in Chapter 8 and beyond.

Finally, we conclude from Eq. (7.22) that to maximize $|A_v|$ the transistor should be biased at the lowest possible V_{CE} consistent with the desired value of negative signal swing at the output.

Example 7.2

Consider an amplifier circuit using a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8\,\text{k}\Omega$, and a power supply $V_{CC} = 10$ V.

(a) Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of I_C?

(b) Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE}, find the amplitude of the output sine-wave signal (assume linear operation).

(c) Find the positive increment in v_{BE} (above V_{BE}) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3$ V.

(d) Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff (i.e., to $v_{CE} = 0.99V_{CC}$).

Solution

(a)

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$
$$= \frac{10 - 3.2}{6.8} = 1 \text{ mA}$$

The value of V_{BE} can be determined from

$$1 \times 10^{-3} = 10^{-15} e^{V_{BE}/V_T}$$

which results in

$$V_{BE} = 690.8 \text{ mV}$$

(b)

$$A_v = -\frac{V_{CC} - V_{CE}}{V_T}$$
$$= \frac{10 - 3.2}{0.025} = -272 \text{ V/V}$$
$$\hat{v}_{ce} = 272 \times 0.005 = 1.36 \text{ V}$$

(c) For $v_{CE} = 0.3$ V,

$$i_C = \frac{10 - 0.3}{6.8} = 1.617 \text{ mA}$$

To increase i_C from 1 mA to 1.617 mA, v_{BE} must be increased by

$$\triangle v_{BE} = V_T \ln\left(\frac{1.617}{1}\right)$$
$$= 12 \text{ mV}$$

(d) For $v_{CE} = 0.99V_{CC} = 9.9$ V,

$$i_C = \frac{10 - 9.9}{6.8} = 0.0147 \text{ mA}$$

To decrease i_C from 1 mA to 0.0147 mA, v_{BE} must change by

$$\triangle v_{BE} = V_T \ln\left(\frac{0.0147}{1}\right)$$
$$= -105.5 \text{ mV}$$

EXERCISE

7.3 For the situation described in Example 7.2, while keeping I_C unchanged at 1 mA, find the value of R_C that will result in a voltage gain of −320 V/V. What is the largest negative signal swing allowed at the output (assume that v_{CE} is not to decrease below 0.3 V)? What (approximately) is the corresponding input signal amplitude? (Assume linear operation.)

Ans. 8 kΩ; 1.7 V; 5.3 mV

7.1.6 Determining the VTC by Graphical Analysis

Figure 7.7 shows a graphical method for determining the VTC of the amplifier of Fig. 7.4(a). Although graphical analysis of transistor circuits is rarely employed in practice, it is useful to us at this stage for gaining greater insight into circuit operation, especially in answering the question of where to locate the bias point Q.

The graphical analysis is based on the observation that for each value of v_{GS}, the circuit will be operating at the point of intersection of the i_D–v_{DS} graph corresponding to the particular

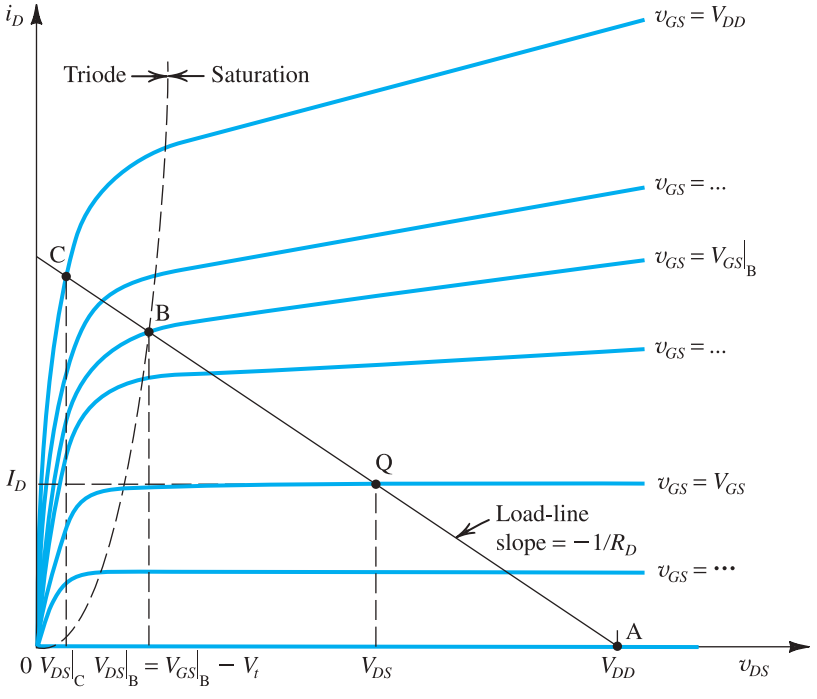


Figure 7.7 Graphical construction to determine the voltage-transfer characteristic of the amplifier in Fig. 7.4(a).

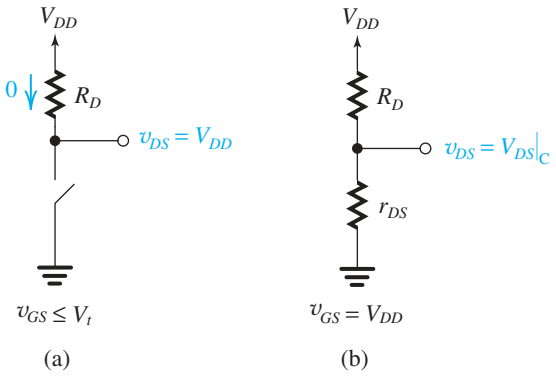


Figure 7.8 Operation of the MOSFET in Fig. 7.4(a) as a switch: **(a)** open, corresponding to point A in Fig. 7.7; **(b)** closed, corresponding to point C in Fig. 7.7. The closure resistance is approximately equal to r_{DS} because V_{DS} is usually very small.

value of v_{GS} and the straight line representing Eq. (7.3), which can be rewritten in the form

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS} \tag{7.24}$$

The straight line representing this relationship is superimposed on the $i_D - v_{DS}$ characteristics in Fig. 7.7. It intersects the horizontal axis at $v_{DS} = V_{DD}$ and has a slope of $-1/R_D$. Since this straight line represents in effect the load resistance R_D, it is called the **load line**. The VTC is then determined point by point. Note that we have labeled four important points: point A at which $v_{GS} = V_t$, point Q at which the MOSFET can be biased for amplifier operation ($v_{GS} = V_{GS}$ and $v_{DS} = V_{DS}$), point B at which the MOSFET leaves saturation and enters the triode region, and point C, which is deep into the triode region and for which $v_{GS} = V_{DD}$. If the MOSFET is to be used as a switch, then operating points A and C are applicable: At A the transistor is off (open switch), and at C the transistor operates as a low-valued resistance r_{DS} and has a small voltage drop (closed switch). The incremental resistance at point C is also known as the **closure resistance**. The operation of the MOSFET as a switch is illustrated in Fig. 7.8. A detailed study of the application of the MOSFET as a switch is undertaken in Chapter 14, dealing with CMOS digital logic circuits.

The graphical analysis method above can be applied to determine the VTC of the BJT amplifier in Fig. 7.2(c). Here point A, Fig. 7.2(d), corresponds to the BJT just turning on ($v_{BE} \simeq 0.5$ V) and point B corresponds to the BJT leaving the active region and entering the saturation region. If the BJT is to be operated as a switch, the two modes of operation are cutoff (open switch) and saturation (closed switch). As discussed in Section 6.2, in saturation, the BJT has a small closure resistance $R_{CE\text{sat}}$ as well as an offset voltage. More seriously, switching the BJT out of its saturation region can require a relatively long delay time to ensure the removal of the charge stored in the BJT base region. This phenomenon has made the BJT much less attractive in digital logic applications relative to the MOSFET.[2]

7.1.7 Deciding on a Location for the Bias Point Q

For the MOSFET amplifier, the bias point Q is determined by the value of V_{GS} and that of the load resistance R_D. Two important considerations in deciding on the location of Q

[2]The only exception is a nonsaturating form of BJT logic circuits known as emitter-coupled logic (ECL).

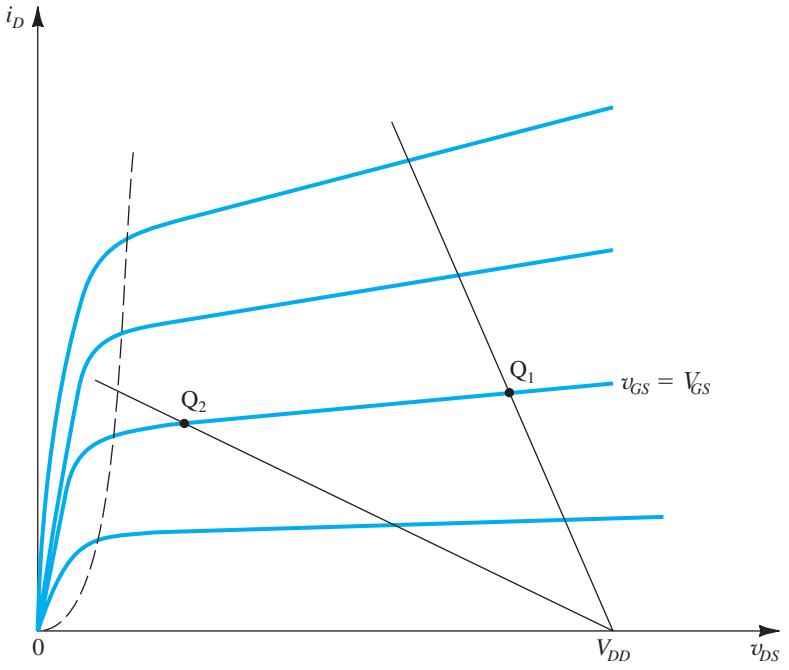


Figure 7.9 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

are the required gain and the desired signal swing at the output. To illustrate, consider the VTC shown in Fig. 7.4(b). Here the value of R_D is fixed and the only variable remaining is the value of V_{GS}. Since the slope increases as we move closer to point B, we obtain higher gain by locating Q as close to B as possible. However, the closer Q is to the boundary point B, the smaller the allowable magnitude of negative signal swing. Thus, as often happens in engineering design, we encounter a situation requiring a trade-off. The answer here is relatively simple: For a given R_D, locate Q as close to the triode region (point B) as possible to obtain high gain but sufficiently distant to allow for the required negative signal swing.

In deciding on a value for R_D, it is useful to refer to the $i_D - v_{DS}$ plane. Figure 7.9 shows two load lines resulting in two extreme bias points: Point Q_1 is too close to V_{DD}, resulting in a severe constraint on the positive signal swing of v_{ds}. Exceeding the allowable positive maximum results in the positive peaks of the signal being clipped off, since the MOSFET will turn off for the part of each cycle near the positive peak. We speak of this situation by saying that the circuit does not have sufficient "headroom." Similarly, point Q_2 is too close to the boundary of the triode region, thus severely limiting the allowable negative signal swing of v_{ds}. Exceeding this limit would result in the transistor entering the triode region for part of each cycle near the negative peaks, resulting in a distorted output signal. In this situation we say that the circuit does not have sufficient "legroom." We will have more to say on bias design in Section 7.4.

Finally, we note that exactly similar considerations apply to the case of the BJT amplifier.

7.2 Small-Signal Operation and Models

In our study of the operation of the MOSFET and BJT amplifiers in Section 7.1 we learned that linear amplification can be obtained by biasing the transistor to operate in the active region and by keeping the input signal small. In this section, we explore the small-signal operation in greater detail.

7.2.1 The MOSFET Case

Consider the conceptual amplifier circuit shown in Fig. 7.10. Here the MOS transistor is biased by applying a dc voltage[3] V_{GS}, and the input signal to be amplified, v_{gs}, is superimposed on the dc bias voltage V_{GS}. The output voltage is taken at the drain.

The DC Bias Point The dc bias current I_D can be found by setting the signal v_{gs} to zero; thus,

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_n V_{OV}^2 \tag{7.25}$$

where we have neglected channel-length modulation (i.e., we have assumed $\lambda = 0$). Here $V_{OV} = V_{GS} - V_t$ is the overdrive voltage at which the MOSFET is biased to operate. The dc voltage at the drain, V_{DS}, will be

$$V_{DS} = V_{DD} - R_D I_D \tag{7.26}$$

To ensure saturation-region operation, we must have

$$V_{DS} > V_{OV}$$

Furthermore, since the total voltage at the drain will have a signal component superimposed on V_{DS}, V_{DS} has to be sufficiently greater than V_{OV} to allow for the required negative signal swing.

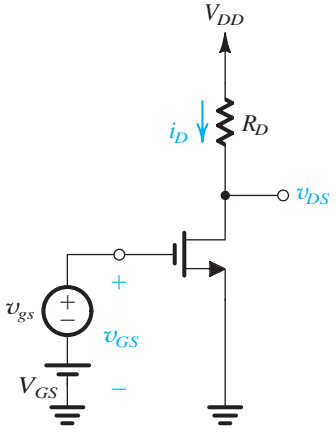


Figure 7.10 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

[3] Practical biasing arrangements will be studied in Section 7.4.

The Signal Current in the Drain Terminal Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \tag{7.27}$$

resulting in a total instantaneous drain current i_D,

$$\begin{aligned} i_D &= \frac{1}{2}k_n\left(V_{GS} + v_{gs} - V_t\right)^2 \\ &= \frac{1}{2}k_n(V_{GS} - V_t)^2 + k_n(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_n v_{gs}^2 \end{aligned} \tag{7.28}$$

The first term on the right-hand side of Eq. (7.28) can be recognized as the dc bias current I_D (Eq. 7.25). The second term represents a current component that is directly proportional to the input signal v_{gs}. The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents *nonlinear distortion*. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2}k_n v_{gs}^2 \ll k_n(V_{GS} - V_t)v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS} - V_t) \tag{7.29}$$

or, equivalently,

$$v_{gs} \ll 2V_{OV} \tag{7.30}$$

If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (7.28) and express i_D as

$$i_D \simeq I_D + i_d \tag{7.31}$$

where

$$i_d = k_n(V_{GS} - V_t)v_{gs}$$

The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_t) \tag{7.32}$$

or in terms of the overdrive voltage V_{OV},

$$g_m = k_n V_{OV} \tag{7.33}$$

Figure 7.11 presents a graphical interpretation of the small-signal operation of the MOSFET amplifier. Note that g_m is equal to the slope of the i_D–v_{GS} characteristic at the bias point,

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}} \tag{7.34}$$

This is the formal definition of g_m, which can be shown to yield the expressions given in Eqs. (7.32) and (7.33).

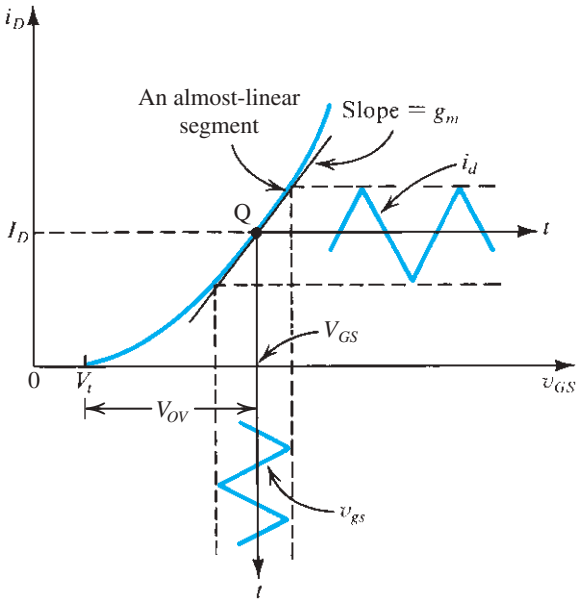


Figure 7.11 Small-signal operation of the MOSFET amplifier.

The Voltage Gain Returning to the circuit of Fig. 7.10, we can express the total instantaneous drain voltage v_{DS} as follows:

$$v_{DS} = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_{DS} = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as

$$v_{DS} = V_{DS} - R_D i_d$$

Thus the signal component of the drain voltage is

$$v_{ds} = -i_d R_D = -g_m v_{gs} R_D \tag{7.35}$$

which indicates that the voltage gain is given by

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D \tag{7.36}$$

The minus sign in Eq. (7.36) indicates that the output signal v_{ds} is 180° out of phase with respect to the input signal v_{gs}. This is illustrated in Fig. 7.12, which shows v_{GS} and v_{DS}. The input signal is assumed to have a triangular waveform with an amplitude much smaller than $2(V_{GS} - V_t)$, the small-signal condition in Eq. (7.29), to ensure linear operation. For operation in the saturation (active) region at all times, the minimum value of v_{DS} should not fall below the corresponding value of v_{GS} by more than V_t. Also, the maximum value of v_{DS} should be

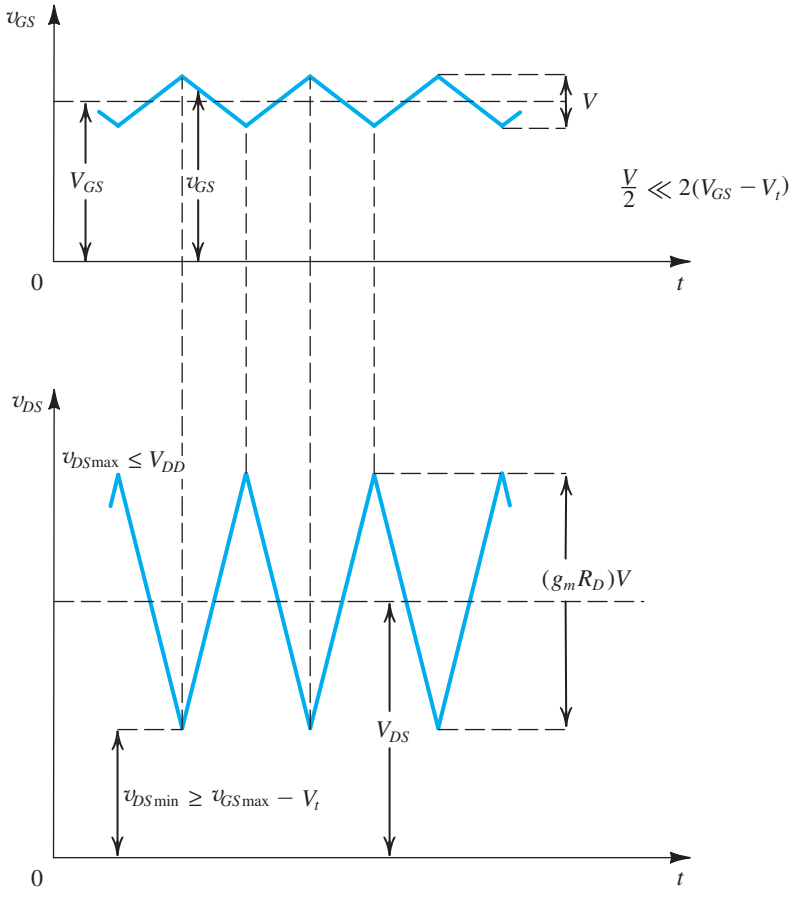


Figure 7.12 Total instantaneous voltages v_{GS} and v_{DS} for the circuit in Fig. 7.10.

smaller than V_{DD}; otherwise the FET will enter the cutoff region and the peaks of the output signal waveform will be clipped off.

Finally, we note that by substituting for g_m from Eq. (7.33) the voltage-gain expression in Eq. (7.36) becomes identical to that derived in Section 7.1—namely, Eq. (7.15).

Separating the DC Analysis and the Signal Analysis From the preceding analysis, we see that under the small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d, the total drain voltage $v_{DS} = V_{DS} + v_{ds}$, and so on. It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations. That is, once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.

Small-Signal Equivalent-Circuit Models From a signal point of view, the FET behaves as a voltage-controlled current source. It accepts a signal v_{gs} between gate and source and provides a current $g_m v_{gs}$ at the drain terminal. The input resistance of this controlled source is very high—ideally, infinite. The output resistance—that is, the resistance looking into the

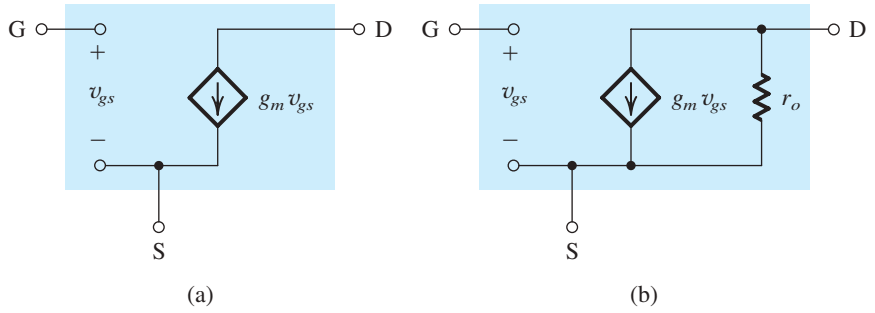


Figure 7.13 Small-signal models for the MOSFET: **(a)** neglecting the dependence of i_D on v_{DS} in the active region (the channel-length modulation effect) and **(b)** including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$. These models apply equally well for both NMOS and PMOS transistors.

drain—also is high, and we have assumed it to be infinite thus far. Putting all of this together, we arrive at the circuit in Fig. 7.13(a), which represents the small-signal operation of the MOSFET and is thus a **small-signal model** or a **small-signal equivalent circuit**.

In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent-circuit model shown in Fig. 7.13(a). The rest of the circuit remains unchanged except that *ideal constant dc voltage sources are replaced by short circuits*. This is a result of the fact that the voltage across an ideal constant dc voltage source does not change, and thus there will always be a zero voltage signal across a constant dc voltage source. A dual statement applies for constant dc current sources; namely, the signal current of an ideal constant dc current source will always be zero, and thus *an ideal constant dc current source can be replaced by an open circuit* in the small-signal equivalent circuit of the amplifier. The circuit resulting can then be used to perform any required signal analysis, such as calculating voltage gain.

The most serious shortcoming of the small-signal model of Fig. 7.13(a) is that it assumes the drain current in saturation to be independent of the drain voltage. From our study of the MOSFET characteristics in saturation, we know that the drain current does in fact depend on v_{DS} in a linear manner. Such dependence was modeled by a finite resistance r_o between drain and source, whose value was given by Eq. (5.27) in Section 5.2.4, which we repeat here (with the prime on I_D dropped) as

$$r_o = \frac{|V_A|}{I_D} \tag{7.37}$$

where $V_A = 1/\lambda$ is a MOSFET parameter that either is specified or can be measured. It should be recalled that for a given process technology, V_A is proportional to the MOSFET channel length. The current I_D is the value of the dc drain current without the channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_n V_{OV}^2 \tag{7.38}$$

Typically, r_o is in the range of 10 kΩ to 1000 kΩ. It follows that the accuracy of the small-signal model can be improved by including r_o in parallel with the controlled source, as shown in Fig. 7.13(b).

It is important to note that the small-signal model parameters g_m and r_o depend on the dc bias point of the MOSFET.

Returning to the amplifier of Fig. 7.10, we find that replacing the MOSFET with the small-signal model of Fig. 7.13(b) results in the voltage-gain expression

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m(R_D \| r_o) \tag{7.39}$$

Thus, the finite output resistance r_o results in a reduction in the magnitude of the voltage gain.

Although the analysis above is performed on an NMOS transistor, the results, and the equivalent-circuit models of Fig. 7.13, apply equally well to PMOS devices, except for using $|V_{GS}|, |V_t|, |V_{OV}|$, and $|V_A|$ and replacing k_n with k_p.

The Transconductance g_m We shall now take a closer look at the MOSFET transconductance given by Eq. (7.32), which we rewrite with $k_n = k_n'(W/L)$ as follows:

$$g_m = k_n'(W/L)(V_{GS} - V_t) = k_n'(W/L)V_{OV} \tag{7.40}$$

This relationship indicates that g_m is proportional to the process transconductance parameter $k_n' = \mu_n C_{ox}$ and to the W/L ratio of the MOS transistor; hence to obtain relatively large transconductance the device must be short and wide. We also observe that for a given device the transconductance is proportional to the overdrive voltage, $V_{OV} = V_{GS} - V_t$, the amount by which the bias voltage V_{GS} exceeds the threshold voltage V_t. Note, however, that increasing g_m by biasing the device at a larger V_{GS} has the disadvantage of reducing the allowable voltage signal swing at the drain.

Another useful expression for g_m can be obtained by substituting for V_{OV} in Eq. (7.40) by $\sqrt{2I_D/(k_n'(W/L))}$ [from Eq. (7.25)]:

$$g_m = \sqrt{2k_n'}\sqrt{W/L}\sqrt{I_D} \tag{7.41}$$

This expression shows two things:

1. For a given MOSFET, g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{W/L}$.

In contrast, as we shall see shortly, the transconductance of the bipolar junction transistor (BJT) is proportional to the bias current and is independent of the physical size and geometry of the device.

To gain some insight into the values of g_m obtained in MOSFETs consider an integrated-circuit device operating at $I_D = 0.5$ mA and having $k_n' = 120\ \mu\text{A/V}^2$. Equation (7.41) shows that for $W/L = 1, g_m = 0.35$ mA/V, whereas a device for which $W/L = 100$ has $g_m = 3.5$ mA/V. In contrast, a BJT operating at a collector current of 0.5 mA has $g_m = 20$ mA/V.

Yet another useful expression for g_m of the MOSFET can be obtained by substituting for $k_n'(W/L)$ in Eq. (7.40) by $2I_D/(V_{GS} - V_t)^2$:

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}} \tag{7.42}$$

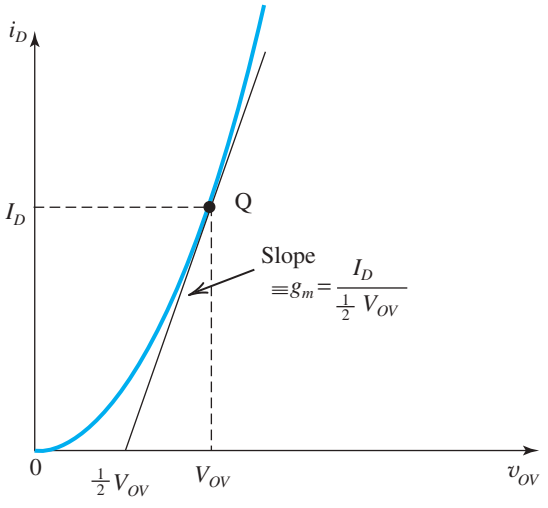


Figure 7.14 The slope of the tangent at the bias point Q intersects the v_{OV} axis at $\frac{1}{2}V_{OV}$. Thus, $g_m = I_D/(\frac{1}{2}V_{OV})$.

A convenient graphical construction that clearly illustrates this relationship is shown in Fig. 7.14.

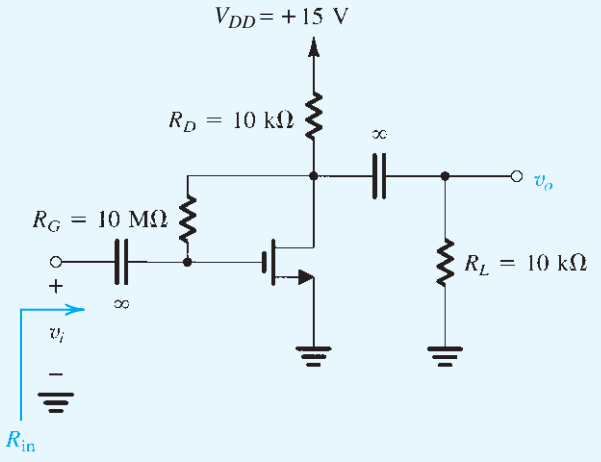
In summary, there are three different relationships for determining g_m—Eqs. (7.40), (7.41), and (7.42)—and there are three design parameters—(W/L), V_{OV}, and I_D, any two of which can be chosen independently. That is, the designer may choose to operate the MOSFET with a certain overdrive voltage V_{OV} and at a particular current I_D; the required W/L ratio can then be found and the resulting g_m determined.[4]

Example 7.3

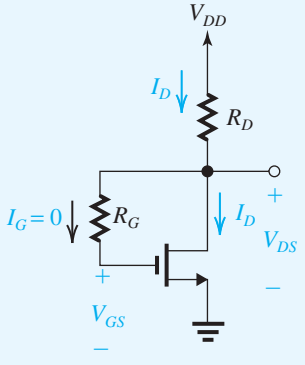
Figure 7.15(a) shows a discrete MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V^2, and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

[4]This assumes that the circuit designer is also designing the device, as is typically the case in IC design. On the other hand, a circuit designer working with a discrete-circuit MOSFET obviously does not have the freedom to change its W/L ratio. Thus, in this case there are only two design parameters—V_{OV} and I_D, and only one can be specified by the designer.

Example 7.3 *continued*



(a)



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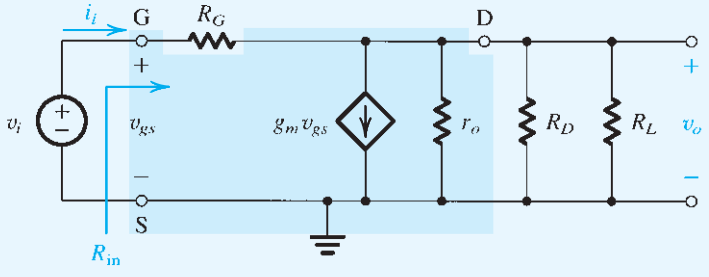
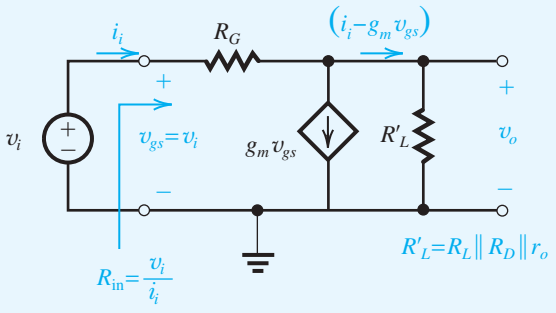


(c)

Figure 7.15 Example 7.3: **(a)** amplifier circuit; **(b)** circuit for determining the dc operating point; **(c)** the amplifier small-signal equivalent circuit; **(d)** a simplified version of the circuit in **(c)**.



(d)

Figure 7.15 *continued*

Solution

We first determine the dc operating point. For this purpose, we eliminate the input signal v_i, and open-circuit the two coupling capacitors (since they block dc currents). The result is the circuit shown in Fig. 7.14(b). We note that since $I_G = 0$, the dc voltage drop across R_G will be zero, and

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \tag{7.43}$$

With $V_{DS} = V_{GS}$, the NMOS transistor will be operating in saturation. Thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \tag{7.44}$$

where, for simplicity, we have neglected the effect of channel-length modulation on the dc operating point. Substituting $V_{DD} = 15$ V, $R_D = 10$ kΩ, $k_n = 0.25$ mA/V^2, and $V_t = 1.5$ V in Eqs. (7.43) and (7.44), and substituting for V_{GS} from Eq. (7.43) into Eq. (7.44) results in a quadratic equation in I_D. Solving the latter and discarding the root that is not physically meaningful yields the solution

$$I_D = 1.06 \text{ mA}$$

which corresponds to

$$V_{GS} = V_{DS} = 4.4 \text{ V}$$

and

$$V_{OV} = 4.4 - 1.5 = 2.9 \text{ V}$$

Next we proceed with the small-signal analysis of the amplifier. Toward that end we replace the MOSFET with its small-signal model to obtain the small-signal equivalent circuit of the amplifier, shown in Fig. 7.15(c). Observe that we have replaced the coupling capacitors with short circuits. The dc voltage supply V_{DD} has also been replaced with a short circuit to ground.

Example 7.3 *continued*

The values of the transistor small-signal parameters g_m and r_o can be determined by using the dc bias quantities found above, as follows:

$$\begin{aligned} g_m &= k_n V_{OV} \\ &= 0.25 \times 2.9 = 0.725 \text{ mA/V} \\ r_o &= \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega \end{aligned}$$

Next we use the equivalent circuit of Fig. 7.15(c) to determine the input resistance $R_{\text{in}} \equiv v_i/i_i$ and the voltage gain $A_v = v_o/v_i$. Toward that end we simplify the circuit by combining the three parallel resistances r_o, R_D, and R_L in a single resistance R_L',

$$\begin{aligned} R_L' &= R_L||R_D||r_o \\ &= 10||10||47 = 4.52 \text{ k}\Omega \end{aligned}$$

as shown in Fig. 7.15(d). For the latter circuit we can write the two equations

$$v_o = (i_i - g_m v_{gs})R_L' \tag{7.45}$$

and

$$i_i = \frac{v_{gs} - v_o}{R_G} \tag{7.46}$$

Substituting for i_i from Eq. (7.46) into Eq. (7.45) results in the following expression for the voltage gain $A_v \equiv v_o/v_i = v_o/v_{gs}$:

$$A_v = -g_m R_L' \frac{1 - (1/g_m R_G)}{1 + (R_L'/R_G)}$$

Since R_G is very large, $g_m R_G \gg 1$ and $R_L'/R_G \ll 1$ (the reader can easily verify this), and the gain expression can be approximated as

$$A_v \simeq -g_m R_L' \tag{7.47}$$

Substituting $g_m = 0.725$ mA/V and $R_L' = 4.52$ kΩ yields

$$A_v = -3.3 \text{ V/V}$$

To obtain the input resistance, we substitute in Eq. (7.46) for $v_o = A_v v_{gs} = -g_m R_L' v_{gs}$, then use $R_{\text{in}} \equiv v_i/i_i = v_{gs}/i_i$ to obtain

$$R_{\text{in}} = \frac{R_G}{1 + g_m R_L'} \tag{7.48}$$

This is an interesting relationship: The input resistance decreases as the gain $(g_m R_L')$ is increased. The value of R_{in} can now be determined; it is

$$R_{in} = \frac{10\ \text{M}\Omega}{1+3.3} = 2.33\ \text{M}\Omega$$

which is still very large.

The largest allowable input signal $\hat{v}_i$ is constrained by the need to keep the transistor in saturation at all times; that is,

$$v_{DS} \geq v_{GS} - V_t$$

Enforcing this condition with equality at the point v_{GS} is maximum and v_{DS} is minimum, we write

$$v_{DS\,\min} = v_{GS\,\max} - V_t$$

$$V_{DS} - |A_v|\hat{v}_i = V_{GS} + \hat{v}_i - V_t$$

Since $V_{DS} = V_{GS}$, we obtain

$$\hat{v}_i = \frac{V_t}{|A_v| + 1}$$

This is a general relationship that applies to this circuit irrespective of the component values. Observe that it simply states that the maximum signal swing is determined by the fact that the bias arrangement makes $V_D = V_G$ and thus, to keep the MOSFET out of the triode region, the signal between D and G is constrained to be equal to V_t. For our particular design,

$$\hat{v}_i = \frac{1.5}{3.3+1} = 0.35\ \text{V}$$

Since $V_{OV} = 2.9$ V, a v_i of 0.35 is indeed much smaller than $2V_{OV} = 5.8$ V; thus the assumption of linear operation is justified.

A modification of this circuit that increases the allowable signal swing is investigated in Problem 7.103.

EXERCISE

D7.4 Consider the amplifier circuit of Fig. 7.15(a) without the load resistance R_L and with channel-length modulation neglected. Let $V_{DD} = 5$ V, $V_t = 0.7$ V, and $k_n = 1$ mA/V^2. Find V_{OV}, I_D, R_D, and R_G to obtain a voltage gain of -25 V/V and an input resistance of 0.5 M Ω. What is the maximum allowable input signal, $\hat{v}_i$?

Ans. 0.319 V; 50.9 μA; 78.5 kΩ; 13 MΩ; 27 mV

The T Equivalent-Circuit Model Through a simple circuit transformation it is possible to develop an alternative equivalent-circuit model for the MOSFET. The development of such a model, known as the T model, is illustrated in Fig. 7.16. Figure 7.16(a) shows the equivalent circuit studied above without r_o. In Fig. 7.16(b) we have added a second $g_m v_{gs}$ current source in series with the original controlled source. This addition obviously does not change the terminal currents and is thus allowed. The newly created circuit node, labeled X, is joined to the gate terminal G in Fig. 7.16(c). Observe that the gate current does not change—that is, it remains equal to zero—and thus this connection does not alter the terminal characteristics. We now note that we have a controlled current source $g_m v_{gs}$ connected across its control voltage v_{gs}. We can replace this controlled source by a resistance as long as this resistance draws an equal current as the source. (See the source-absorption theorem in Appendix D.) Thus the value of the resistance is $v_{gs}/g_m v_{gs} = 1/g_m$. This replacement is shown in Fig. 7.16(d), which depicts

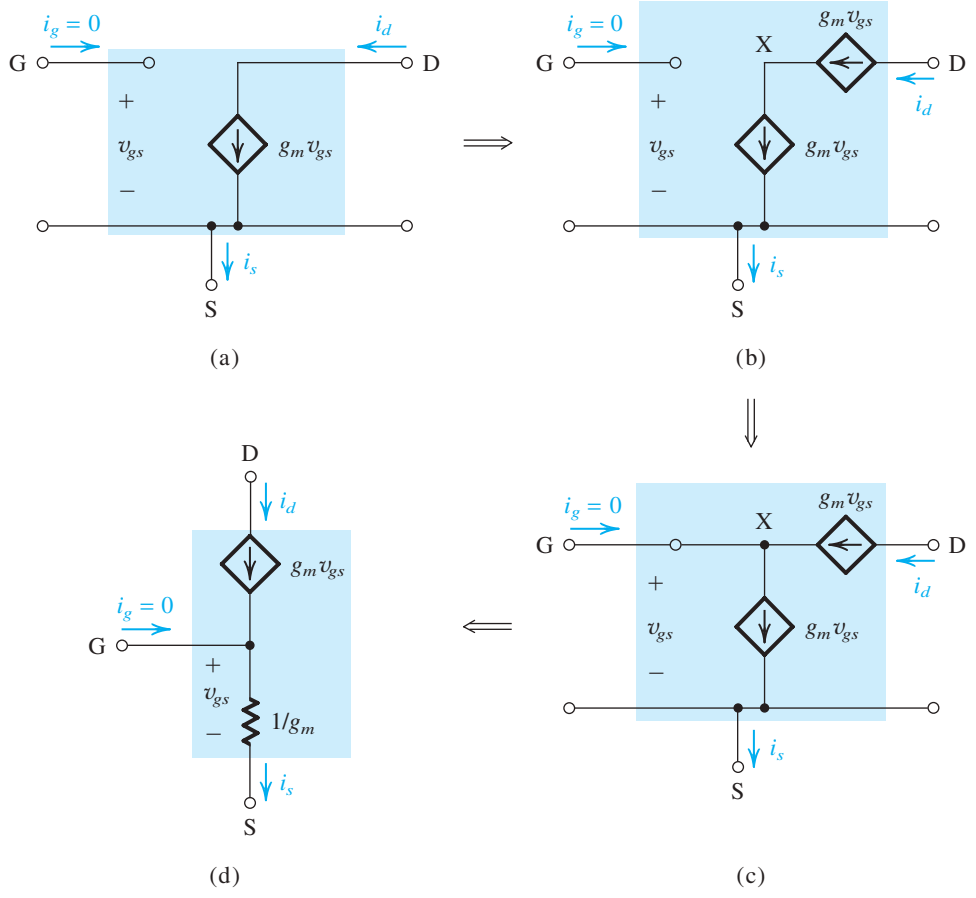


Figure 7.16 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted; however, it may be added between D and S in the T model of **(d)**.

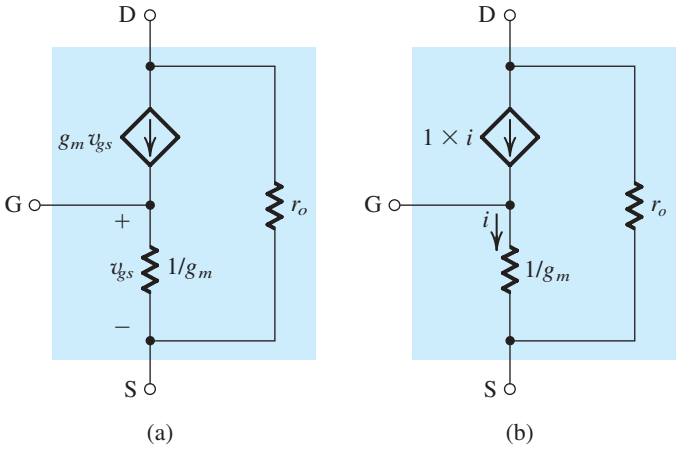


Figure 7.17 **(a)** The T model of the MOSFET augmented with the drain-to-source resistance r_o. **(b)** An alternative representation of the T model.

the alternative model. Observe that i_g is still zero, $i_d = g_m v_{gs}$, and $i_s = v_{gs}/(1/g_m) = g_m v_{gs}$, all the same as in the original model in Fig. 7.16(a).

The model of Fig. 7.16(d) shows that the resistance between gate and source looking into the source is $1/g_m$. This observation and the T model prove useful in many applications. Note that the resistance between gate and source, looking into the gate, is infinite.

In developing the T model we did not include r_o. If desired, this can be done by incorporating in the circuit of Fig. 7.16(d) a resistance r_o between drain and source, as shown in Fig. 7.17(a). An alternative representation of the T model, in which the voltage-controlled current source is replaced with a current-controlled current source, is shown in Fig. 7.17(b).

Finally, we should note that in order to distinguish the model of Fig. 7.13(b) from the equivalent T model, the former is sometimes referred to as the **hybrid-π model**, a carryover from the bipolar transistor literature. The origin of this name will be explained shortly.

Example 7.4

Figure 7.18(a) shows a MOSFET amplifier biased by a constant-current source I. Assume that the values of I and R_D are such that the MOSFET operates in the saturation region. The input signal v_i is coupled to the source terminal by utilizing a large capacitor C_{C1}. Similarly, the output signal at the drain is taken through a large coupling capacitor C_{C2}. Find the input resistance R_{in} and the voltage gain v_o/v_i. Neglect channel-length modulation.

Example 7.4 *continued*

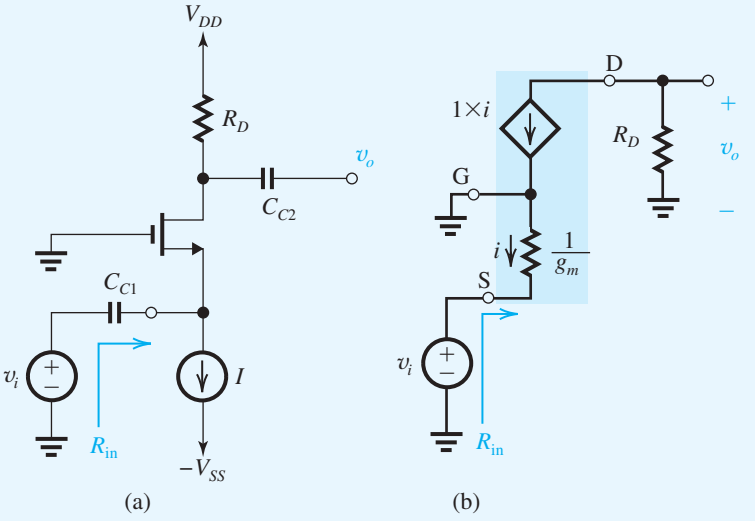


Figure 7.18 **(a)** Amplifier circuit for Example 7.4. **(b)** Small-signal equivalent circuit of the amplifier in **(a)**.

Solution

Replacing the MOSFET with its T equivalent-circuit model results in the amplifier equivalent circuit shown in Fig. 7.18(b). Observe that the dc current source I is replaced with an open circuit and the dc voltage source V_{DD} is replaced by a short circuit. The large coupling capacitors have been replaced by short circuits. From the equivalent-circuit model we determine

$$R_{\text{in}} = \frac{v_i}{-i} = 1/g_m$$

and

$$v_o = -iR_D = \left(\frac{v_i}{1/g_m}\right)R_D = g_m R_D v_i$$

Thus,

$$A_v \equiv \frac{v_o}{v_i} = g_m R_D$$

We note that this amplifier, known as the common-gate amplifier because the gate at ground potential is common to both the input and output ports, has a low input resistance $\left(1/g_m\right)$ and a noninverting gain. We shall study this amplifier type in Section 7.3.5.

EXERCISE

7.5 Use the T model of Fig. 7.17(b) to show that a MOSFET whose drain is connected to its gate exhibits an incremental resistance equal to $[(1/g_m) \| r_o]$.
Ans. See Fig. E7.5.

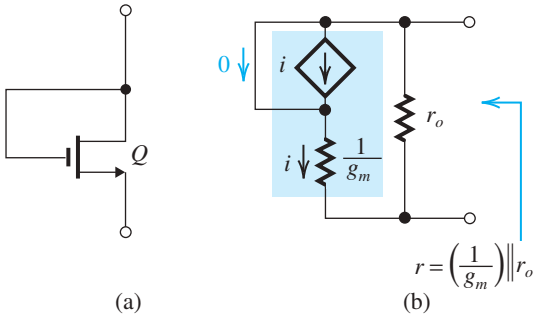


Figure E7.5 Circuits for Exercise 7.5. Note that the bias arrangement of Q is not shown.

Modeling the Body Effect As mentioned earlier (see Section 5.4), the body effect occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most negative power supply in the integrated circuit for n-channel devices and to the most positive for p-channel devices). Thus the substrate (body) will be at signal ground, but since the source is not, a signal voltage v_{bs} develops between the body (B) and the source (S). The substrate then acts as a "second gate" or a **backgate** for the MOSFET. Thus the signal v_{bs} gives rise to a drain-current component, which we shall write as $g_{mb}v_{bs}$, where g_{mb} is the **body transconductance**, defined as

$$g_{mb} \equiv \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{\substack{v_{GS}=\text{constant} \\ v_{DS}=\text{constant}}} \tag{7.49}$$

Recalling that i_D depends on v_{BS} through the dependence of V_t on V_{BS}, we can show that

$$g_{mb} = \chi g_m \tag{7.50}$$

where

$$\chi \equiv \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} \tag{7.51}$$

Typically the value of χ lies in the range 0.1 to 0.3.

Figure 7.19 shows the MOSFET model augmented to include the controlled source $g_{mb}v_{bs}$ that models the body effect. Ideally, this is the model to be used whenever the source is not connected to the substrate. It has been found, however, that except in some very particular

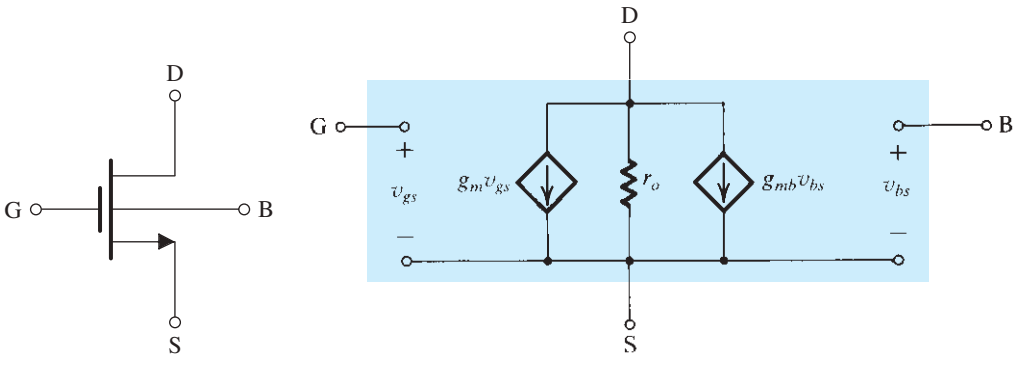


Figure 7.19 Small-signal, equivalent-circuit model of a MOSFET in which the source is not connected to the body.

situations, the body effect can generally be ignored in the initial, pencil-and-paper design of MOSFET amplifiers.

Finally, although the analysis above was performed on an NMOS transistor, the results and the equivalent circuit of Fig. 7.19 apply equally well to PMOS transistors, except for using $|V_{GS}|$, $|V_t|$, $|V_{OV}|$, $|V_A|$, $|V_{SB}|$, $|\gamma|$, and $|\lambda|$ and replacing k_n' with k_p' in the appropriate formula.

EXERCISES

7.6 For the amplifier in Fig. 7.4, let $V_{DD} = 5$ V, $R_D = 10$ kΩ, $V_t = 1$ V, $k_n' = 20\ \mu\text{A/V}^2$, $W/L = 20$, $V_{GS} = 2$ V, and $\lambda = 0$.

(a) Find the dc current I_D and the dc voltage V_{DS}.

(b) Find g_m.

(c) Find the voltage gain.

(d) If $v_{gs} = 0.2 \sin \omega t$ volts, find v_{ds} assuming that the small-signal approximation holds. What are the minimum and maximum values of v_{DS}?

(e) Use Eq. (7.28) to determine the various components of i_D. Using the identity ($\sin^2 \omega t = \frac{1}{2} - \frac{1}{2} \cos 2\,\omega t$), show that there is a slight shift in I_D (by how much?) and that there is a second-harmonic component (i.e., a component with frequency $2\,\omega$). Express the amplitude of the second-harmonic component as a percentage of the amplitude of the fundamental. (This value is known as the second-harmonic distortion.)

Ans. (a) 200 μA, 3 V; (b) 0.4 mA/V; (c) –4 V/V; (d) $v_{ds} = -0.8 \sin \omega t$ volts, 2.2 V, 3.8 V; (e) $i_D = (204 + 80 \sin \omega t - 4 \cos 2\,\omega t)$ μA, 5%

7.7 An NMOS transistor has $\mu_n C_{ox} = 60\ \mu\text{A/V}^2$, $W/L = 40$, $V_t = 1$ V, and $V_A = 15$ V. Find g_m and r_o when (a) the bias voltage $V_{GS} = 1.5$ V, (b) the bias current $I_D = 0.5$ mA.

Ans. (a) 1.2 mA/V, 50 kΩ; (b) 1.55 mA/V, 30 kΩ

7.8 A MOSFET is to operate at $I_D = 0.1$ mA and is to have $g_m = 1$ mA/V. If $k_n' = 50\ \mu A/V^2$, find the required W/L ratio and the overdrive voltage.
Ans. 100; 0.2 V

7.9 For a fabrication process for which $\mu_p \simeq 0.4\,\mu_n$, find the ratio of the width of a PMOS transistor to the width of an NMOS transistor so that the two devices have equal g_m for the same bias conditions. The two devices have equal channel lengths.
Ans. 2.5

7.10 A PMOS transistor has $V_t = -1$ V, $k_p' = 60\ \mu A/V^2$, and $W/L = 16\ \mu m/0.8\ \mu m$. Find I_D and g_m when the device is biased at $V_{GS} = -1.6$ V. Also, find the value of r_o if λ (at $L = 1\ \mu m$) = –0.04 V^{-1}.
Ans. 216 μA; 0.72 mA/V; 92.6 kΩ

7.11 Derive an expression for $(g_m r_o)$ in terms of V_A and V_{OV}. As we shall see in Chapter 8, this is an important transistor parameter and is known as the intrinsic gain. Evaluate the value of $g_m r_o$ for an NMOS transistor fabricated in a 0.8-μm CMOS process for which $V_A' = 12.5$ V/μm of channel length. Let the device have minimum channel length and be operated at an overdrive voltage of 0.2 V.
Ans. $g_m r_o = 2V_A/V_{OV}$; 100 V/V

7.2.2 The BJT Case

We next consider the small-signal operation of the BJT and develop small-signal equivalent-circuit models that represent its operation at a given bias point. The following development parallels what we used for the MOSFET except that here we have an added complication: The BJT draws a finite base current. As will be seen shortly, this phenomenon (finite β) manifests itself as a finite input resistance looking into the base of the BJT (as compared to the infinite input resistance looking into the gate of the MOSFET).

Consider the *conceptual* amplifier circuit shown in Fig. 7.20(a). Here the base–emitter junction is forward biased by a dc voltage V_{BE}. The reverse bias of the collector–base junction is established by connecting the collector to another power supply of voltage V_{CC} through a resistor R_C. The input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE}.

The DC Bias Point We consider first the dc bias conditions by setting the signal v_{be} to zero. The circuit reduces to that in Fig. 7.20(b), and we can write the following relationships for the dc currents and voltages:

$$I_C = I_S e^{V_{BE}/V_T} \tag{7.52}$$

$$I_E = I_C/\alpha \tag{7.53}$$

$$I_B = I_C/\beta \tag{7.54}$$

$$V_{CE} = V_{CC} - I_C R_C \tag{7.55}$$

For active-mode operation, V_{CE} should be greater than $(V_{BE} - 0.4)$ by an amount that allows for the required negative signal swing at the collector.

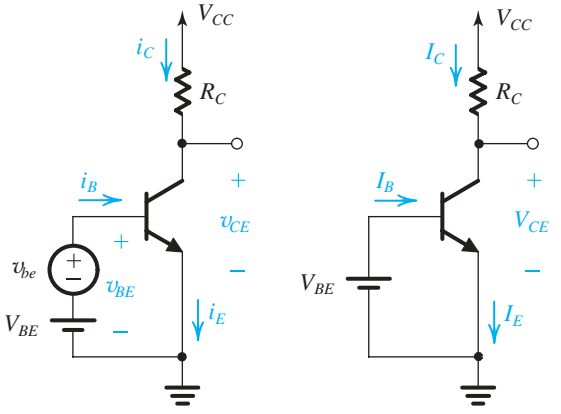


Figure 7.20 (**a**) Conceptual circuit to illustrate the operation of the transistor as an amplifier. (**b**) The circuit of (**a**) with the signal source v_{be} eliminated for dc (bias) analysis.

The Collector Current and the Transconductance If a signal v_{be} is applied as shown in Fig. 7.20(a), the total instantaneous base–emitter voltage v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly, the collector current becomes

$$\begin{aligned} i_C &= I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T} \\ &= I_S e^{V_{BE}/V_T} e^{v_{be}/V_T} \end{aligned}$$

Use of Eq. (7.52) yields

$$i_C = I_C e^{v_{be}/V_T} \tag{7.56}$$

Now, if $v_{be} \ll V_T$, we may approximate Eq. (7.56) as

$$i_C \simeq I_C \left(1 + \frac{v_{be}}{V_T}\right) \tag{7.57}$$

Here we have expanded the exponential in Eq. (7.56) in a series and retained only the first two terms. That is, we have assumed that

$$v_{be} \ll V_T \tag{7.58}$$

so that we can neglect the higher-order terms in the exponential series expansion. The condition in Eq. (7.58) is the **small-signal approximation** for the BJT and corresponds to that in Eq. (7.29) for the MOSFET case. The small-signal approximation for the BJT is valid only for v_{be} less than 5 mV or 10 mV, at most. Under this approximation, the total collector current is given by Eq. (7.57) and can be rewritten

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \tag{7.59}$$

Thus the collector current is composed of the dc bias value I_C and a signal component i_c,

$$i_c = \frac{I_C}{V_T} v_{be} \tag{7.60}$$

This equation relates the signal current in the collector to the corresponding base–emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be} \tag{7.61}$$

where g_m is the **transconductance**, and from Eq. (7.60), it is given by

$$g_m = \frac{I_C}{V_T} \tag{7.62}$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current I_C. Thus to obtain a constant predictable value for g_m, we need a constant predictable I_C. Also, we note that BJTs have relatively high transconductance in comparison to MOSFETs: for instance, at $I_C = 1$ mA, $g_m \simeq 40$ mA/V. Finally, unlike the MOSFET, whose g_m depends on the device dimensions (W and L), g_m of a BJT depends only on the dc collector current at which it is biased to operate.

A graphical interpretation for g_m is given in Fig. 7.21, where it is shown that g_m is equal to the slope of the tangent to the i_C–v_{BE} characteristic curve at $i_C = I_C$ (i.e., at the bias point Q). Thus,

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C} \tag{7.63}$$

The small-signal approximation implies keeping the signal amplitude sufficiently small that *operation is restricted to an almost-linear segment of the i_C–v_{BE} exponential curve.* Increasing the signal amplitude will result in the collector current having components nonlinearly related to v_{be}.

EXERCISES

7.12 Use Eq. (7.63) to derive the expression for g_m in Eq. (7.62).

7.13 Calculate the value of g_m for a BJT biased at $I_C = 0.5$ mA.
Ans. 20 mA/V

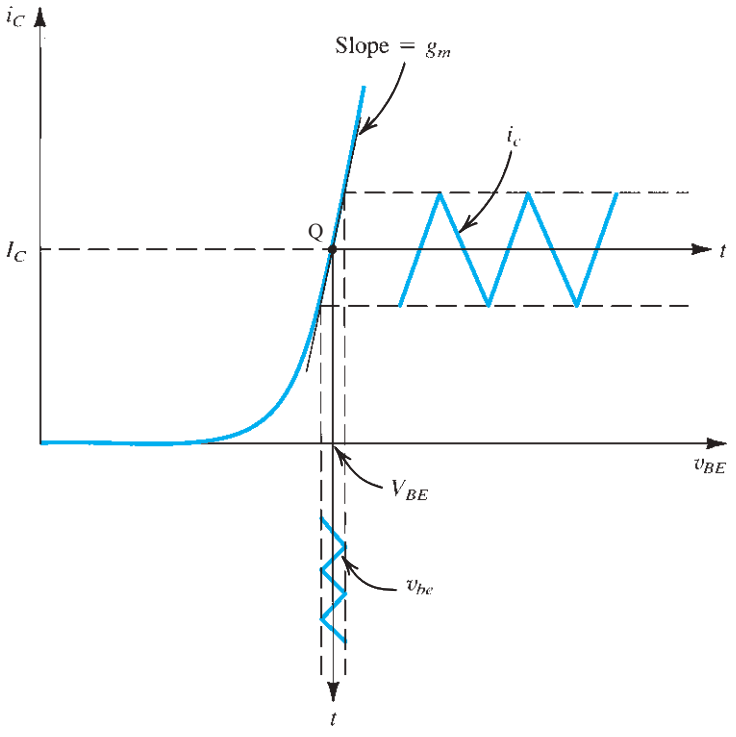


Figure 7.21 Linear operation of the transistor under the small-signal condition: A small-signal v_{be} with a triangular waveform is superimposed on the dc voltage V_{BE}. It gives rise to a collector-signal current i_c, also of triangular waveform, superimposed on the dc current I_C. Here, $i_c = g_m v_{be}$, where g_m is the slope of the i_C–v_{BE} curve at the bias point Q.

The Base Current and the Input Resistance at the Base To determine the resistance seen by v_{be}, we first evaluate the total base current i_B using Eq. (7.59), as follows:

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T}v_{be}$$

Thus,

$$i_B = I_B + i_b \tag{7.64}$$

where I_B is equal to I_C/β and the signal component i_b is given by

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T}v_{be} \tag{7.65}$$

Substituting for I_C/V_T by g_m gives

$$i_b = \frac{g_m}{\beta}v_{be} \tag{7.66}$$

The small-signal input resistance between base and emitter, *looking into the base,* is denoted by r_π and is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b} \tag{7.67}$$

Using Eq. (7.66) gives

$$r_\pi = \frac{\beta}{g_m} \tag{7.68}$$

Thus r_π is directly dependent on β and is inversely proportional to the bias current I_C. Substituting for g_m in Eq. (7.68) from Eq. (7.62) and replacing I_C/β by I_B gives an alternative expression for r_π,

$$r_\pi = \frac{V_T}{I_B} \tag{7.69}$$

Here, we recall that because the gate current of the MOSFET is zero (at dc and low frequencies) the input resistance at the gate is infinite; that is, in the MOSFET there is no counterpart to r_π.[5]

EXERCISE

7.14 A BJT amplifier is biased to operate at a constant collector current $I_C = 0.5$ mA irrespective of the value β. If the transistor manufacturer specifies β to range from 50 to 200, give the expected range of g_m, I_B, and r_π.

Ans. g_m is constant at 20 mA/V; $I_B = 10\ \mu$A to 2.5 μA; $r_\pi = 2.5$ kΩ to 10 kΩ

The Emitter Current and the Input Resistance at the Emitter The total emitter current i_E can be determined using Eq. (7.59) as

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

Thus,

$$i_E = I_E + i_e \tag{7.70}$$

where I_E is equal to I_C/α and the signal current i_e is given by

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be} \tag{7.71}$$

[5]At high frequencies, the input capacitance at the MOSFET gate makes the input current finite (see Chapter 10).

If we denote the small-signal resistance between base and emitter *looking into the emitter* by r_e, it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e} \tag{7.72}$$

Using Eq. (7.71) we find that r_e, called the **emitter resistance**, is given by

$$r_e = \frac{V_T}{I_E} \tag{7.73}$$

Comparison with Eq. (7.62) reveals that

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m} \tag{7.74}$$

The relationship between r_π and r_e can be found by combining their respective definitions in Eqs. (7.67) and (7.72) as

$$v_{be} = i_b r_\pi = i_e r_e$$

Thus,

$$r_\pi = (i_e/i_b) r_e$$

which yields

$$r_\pi = (\beta + 1) r_e \tag{7.75}$$

Figure 7.22 illustrates the definition of r_π and r_e.

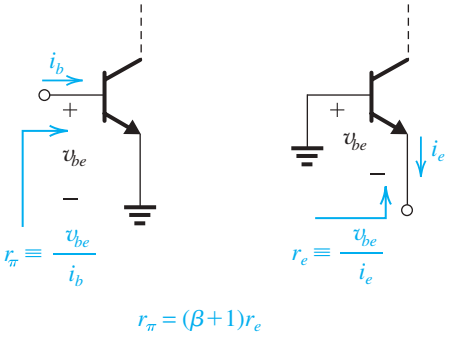


Figure 7.22 Illustrating the definition of r_π and r_e.

Finally, a comparison with the MOSFET would be useful: For the MOSFET, $\alpha = 1$ and the resistance looking into the source is simply $1/g_m$.

SHOCKLEY AND SILICON VALLEY:

In 1956 William Bradford Shockley started a new company, Shockley Semiconductor Laboratory in Mountain View, California (near Stanford, his birthplace). While at Bell Labs, together with John Bardeen and Walter Brattain, he had invented the BJT. At Shockley, the initial concentration was on developing semiconductor devices, particularly a new four-layer diode. But Shockley's scientific genius and ability to select and attract good team members, first demonstrated at Bell Labs, was not accompanied by comparable talent for management. Consequently, in 1957, eight of his team members (the so-called Traitorous Eight, including Gordon Moore and Robert Noyce) left Shockley to create Fairchild Semiconductor. It was a propitious time: The first *Sputnik* was launched a month later, and the ensuing space race accelerated demand for solid-state circuits. Decades passed, and in 2002 a group of some 30 individuals who had been associated with Silicon Valley since 1956 met at Stanford University to reminisce about Shockley's contributions to the information technology age. They unanimously concluded that Shockley was the man who brought silicon to Silicon Valley!

EXERCISE

7.15 A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find the value of g_m, r_e, and r_π at the bias point.

Ans. 40 mA/V; 25 Ω; 2.5 kΩ

The Voltage Gain The total collector voltage v_{CE} is

$$\begin{aligned} v_{CE} &= V_{CC} - i_C R_C \\ &= V_{CC} - (I_C + i_c) R_C \\ &= (V_{CC} - I_C R_C) - i_c R_C \\ &= V_{CE} - i_c R_C \end{aligned} \tag{7.76}$$

Thus, superimposed on the collector bias voltage V_{CE} we have signal voltage v_{ce} given by

$$\begin{aligned} v_{ce} &= -i_c R_C = -g_m v_{be} R_C \\ &= (-g_m R_C) v_{be} \end{aligned} \tag{7.77}$$

from which we find the voltage gain A_v of this amplifier as

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C \tag{7.78}$$

Here again we note that because g_m is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made. Substituting for g_m from Eq. (7.62)

enables us to express the gain in the form

$$A_v = -\frac{I_C R_C}{V_T} \tag{7.79}$$

which is identical to the expression we derived in Section 7.1 (Eq. 7.21). Finally, we note that the gain expression in Eq. (7.78) is identical in form to that for the MOSFET amplifier (namely, $-g_m R_D$).

EXERCISE

7.16 In the circuit of Fig. 7.20(a), V_{BE} is adjusted to yield a dc collector current of 1 mA. Let $V_{CC} = 15$ V, $R_C = 10\,\text{k}\Omega$, and $\beta = 100$. Find the voltage gain v_{ce}/v_{be}. If $v_{be} = 0.005 \sin \omega t$ volt, find $v_C(t)$ and $i_B(t)$.
Ans. -400 V/V; $5 - 2 \sin \omega t$ volts; $10 + 2 \sin \omega t$ μA

Separating the Signal and the DC Quantities The analysis above indicates that every current and voltage in the amplifier circuit of Fig. 7.20(a) is composed of two components: a dc component and a signal component. For instance, $v_{BE} = V_{BE} + v_{be}$, $I_C = I_C + i_c$, and so on. The dc components are determined from the dc circuit given in Fig. 7.20(b) and from the relationships imposed by the transistor (Eqs. 7.52 through 7.54). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. 7.23. Observe that since the voltage of an ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced V_{CC} and V_{BE} with short circuits. Had the circuit contained ideal dc current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. 7.23 is useful only insofar as it shows the various signal currents and voltages; it is *not* an actual amplifier circuit, since the dc bias circuit is not shown.

Figure 7.23 also shows the expressions for the current increments (i_c, i_b, and i_e) obtained when a small signal v_{be} is applied. These relationships can be represented by a circuit. Such

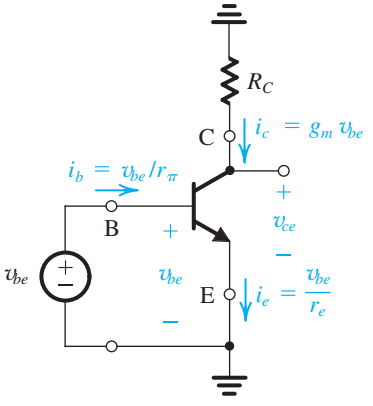


Figure 7.23 The amplifier circuit of Fig. 7.20(a) with the dc sources (V_{BE} and V_{CC}) eliminated (short-circuited). Thus only the signal components are present. Note that this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

a circuit should have three terminals—C, B, and E—and should yield the same terminal currents indicated in Fig. 7.23. The resulting circuit is then *equivalent to the transistor as far as small-signal operation is concerned,* and thus it can be considered an equivalent small-signal circuit model.

The Hybrid-π Model An equivalent-circuit model for the BJT is shown in Fig. 7.24(a). This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base, r_π. The model obviously yields $i_c = g_m v_{be}$ and $i_b = v_{be}/r_\pi$. Not so obvious, however, is the fact that the model also yields the correct expression for i_e. This can be shown as follows: At the emitter node we have

$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi) \\ &= \frac{v_{be}}{r_\pi}(1+\beta) = v_{be} \Big/ \left(\frac{r_\pi}{1+\beta}\right) \\ &= v_{be}/r_e \end{aligned}$$

A slightly different equivalent-circuit model can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b as follows:

$$\begin{aligned} g_m v_{be} &= g_m(i_b r_\pi) \\ &= (g_m r_\pi) i_b = \beta i_b \end{aligned}$$

This results in the alternative equivalent-circuit model shown in Fig. 7.24(b). Here the transistor is represented as a current-controlled current source, with the control current being i_b.

As we have done in the case of the MOSFET's small-signal models, we can account for the Early effect (the slight dependence of i_C on v_{CE} due to basewidth modulation) by adding the resistance $r_o = V_A/I_C$ between collector and emitter, as shown in Fig. 7.25. Note that to conform with the literature, we have renamed v_{be} as v_π. The two models of Fig. 7.25 are versions of the hybrid-π model, the most widely used model for the BJT. The equivalent circuit of Fig. 7.25(a) corresponds to that of the MOSFET [Fig. 7.13(b)] except for r_π, which accounts for the finite base current (or finite β) of the BJT. However, the equivalent circuit of Fig. 7.25(b) has no MOS counterpart.

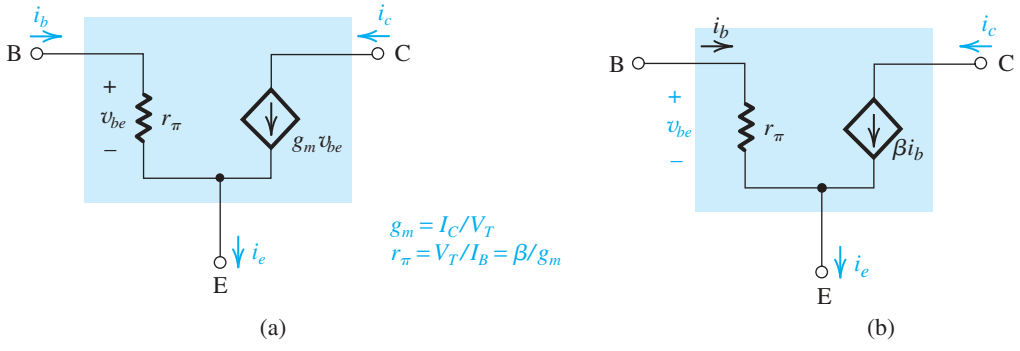


Figure 7.24 Two slightly different versions of the hybrid-π model for the small-signal operation of the BJT. The equivalent circuit in (**a**) represents the BJT as a voltage-controlled current source (a transconductance amplifier), and that in (**b**) represents the BJT as a current-controlled current source (a current amplifier).

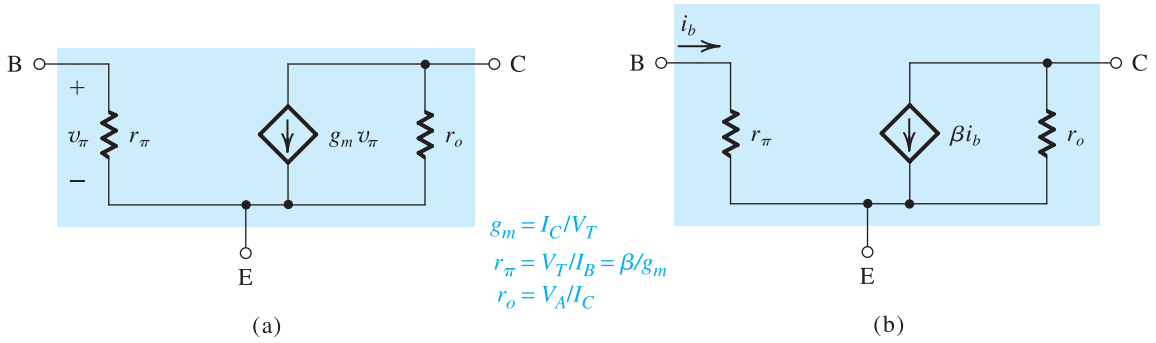


Figure 7.25 The hybrid-π small-signal model, in its two versions, with the resistance r_o included.

It is important to note that the small-signal equivalent circuits of Fig. 7.25 model the operation of the BJT *at a given bias point*. This should be obvious from the fact that the model parameters g_m, r_π, and r_o depend on the value of the dc bias current I_C, as indicated in Fig. 7.25. That is, these equivalent circuits model the *incremental operation* of the BJT around the bias point.

As in the case of the MOSFET amplifier, including r_o in the BJT model causes the voltage gain of the conceptual amplifier of Fig. 7.20(a) to become

$$\frac{v_o}{v_{be}} = -g_m(R_C \parallel r_o) \tag{7.80}$$

Thus, the magnitude of the gain is reduced somewhat.

EXERCISE

7.17 For the model in Fig. 7.24(b) show that $i_c = g_m v_{be}$ and $i_e = v_{be}/r_e$.

The T Model Although the hybrid-π model (in one of its two variants shown in Fig. 7.24) can be used to carry out small-signal analysis of any transistor circuit, there are situations in which an alternative model, shown in Fig. 7.26, is much more convenient. This model, called, as in the case of the MOSFET, the **T model**, is shown in two versions in Fig. 7.26. The model of Fig. 7.26(a) represents the BJT as a voltage-controlled current source with the control voltage being v_{be}. Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown. From Fig. 7.26(a) we see clearly that the model yields the correct expressions for i_c and i_e. It can also be shown to yield the correct expression for i_b (see Exercise 7.18 on the next page).

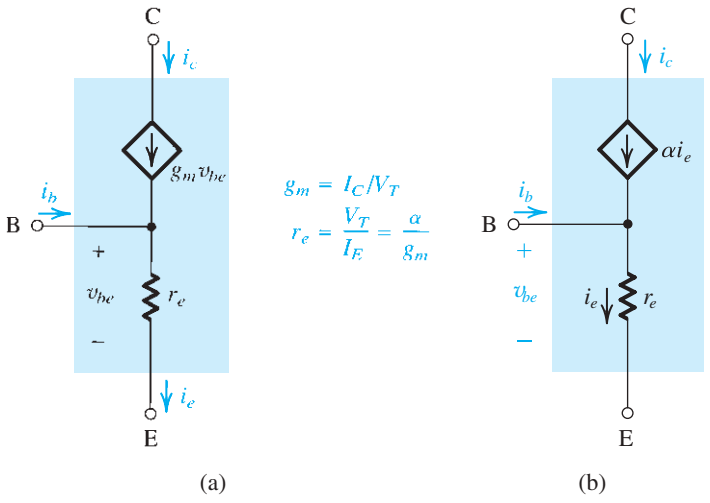


Figure 7.26 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in (**a**) is a voltage-controlled current source representation and that in (**b**) is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid-π model.

If in the model of Fig. 7.26(a) the current of the controlled source is expressed in terms of the emitter current as

$$\begin{aligned} g_m v_{be} &= g_m(i_e r_e) \\ &= (g_m r_e) i_e = \alpha i_e \end{aligned}$$

we obtain the alternative T model shown in Fig. 7.26(b). Here the BJT is represented as a current-controlled current source but with the control signal being i_e.

Finally, the T models can be augmented by r_o to account for the dependence of i_c to v_{ce} (the Early effect) to obtain the equivalent circuits shown in Fig. 7.27.

EXERCISE

7.18 Show that for the T model in Fig. 7.24(a), $i_b = v_{be}/r_\pi$.

Small-Signal Models of the *pnp* Transistor Although the small-signal models in Figs. 7.25 and 7.27 were developed for the case of the *npn* transistor, they apply equally well to the *pnp* transistor *with no change in polarities*.

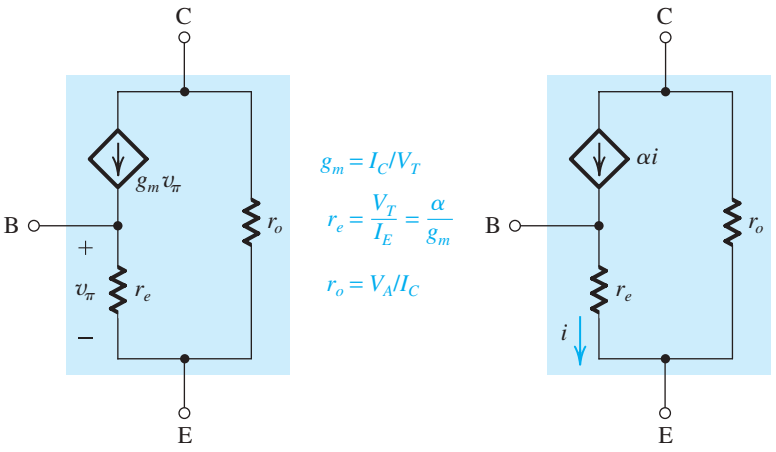


Figure 7.27 The T models of the BJT.

Example 7.5

We wish to analyze the transistor amplifier shown in Fig. 7.28(a) to determine its voltage gain v_o/v_i. Assume $\beta = 100$ and neglect the Early effect.

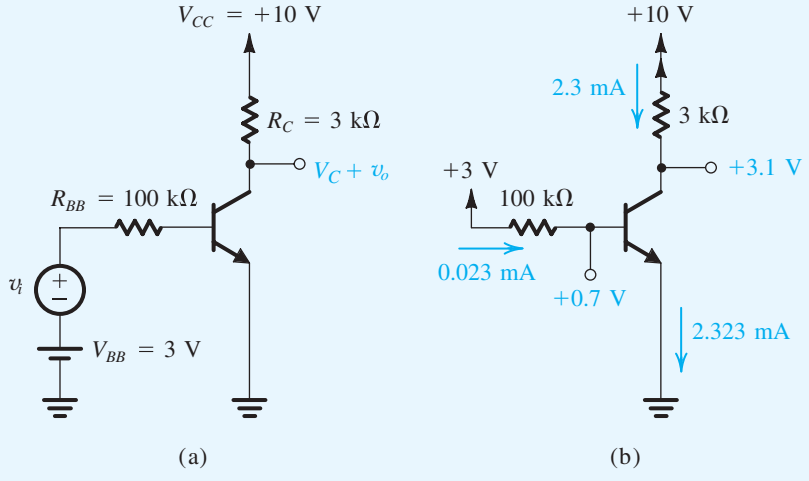


Figure 7.28 Example 7.5: (**a**) amplifier circuit; (**b**) circuit for dc analysis; (**c**) amplifier circuit with dc sources replaced by short circuits; (**d**) amplifier circuit with transistor replaced by its hybrid-π, small-signal model.

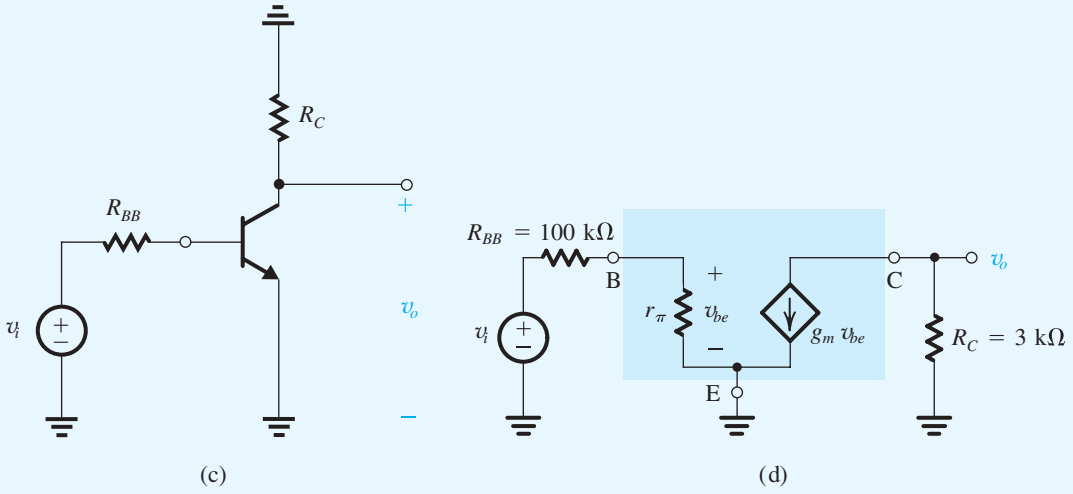


Figure 7.28 *continued*

Solution

We shall follow a five-step process:

1. The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $v_i = 0$ and thus obtain the dc circuit shown in Fig. 7.28(b). The dc base current will be

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} \simeq \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$V_C = V_{CC} - I_C R_C = +10 - 2.3 \times 3 = +3.1 \text{ V}$$

Since V_B at +0.7 V is less than V_C, it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 7.28(b).

Example 7.5 *continued*

2. Having determined the operating point, we can now proceed to determine the small-signal model parameters:

$$r_e = \frac{V_T}{I_E} = \frac{25\text{ mV}}{(2.3/0.99)\text{ mA}} = 10.8\ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3\text{ mA}}{25\text{ mV}} = 92\text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09\text{ k}\Omega$$

3. Replacing V_{BB} and V_{CC} with short circuits results in the circuit in Fig. 7.28(c).
4. To carry out the small-signal analysis it is equally convenient to employ either of the two hybrid-π, equivalent-circuit models of Fig. 7.24 to replace the transistor in the circuit of Fig. 7.28(c). Using the first results in the amplifier equivalent circuit given in Fig. 7.28(d).
5. Analysis of the equivalent circuit in Fig. 7.28(d) proceeds as follows:

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}}$$

$$= v_i \frac{1.09}{101.09} = 0.011 v_i \tag{7.81}$$

The output voltage v_o is given by

$$v_o = -g_m v_{be} R_C$$
$$= -92 \times 0.011 v_i \times 3 = -3.04 v_i$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04\text{ V/V} \tag{7.82}$$

Example 7.6

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that v_i has a triangular waveform. First determine the maximum amplitude that v_i is allowed to have. Then, with the amplitude of v_i set to this value, give the waveforms of the total quantities $i_B(t)$, $v_{BE}(t)$, $i_C(t)$, and $v_C(t)$.

Solution

One constraint on signal amplitude is the small-signal approximation, which stipulates that v_{be} should not exceed about 10 mV. If we take the triangular waveform v_{be} to be 20 mV peak-to-peak and work backward, Eq. (7.81) can be used to determine the maximum possible peak of v_i,

$$\hat{v}_i = \frac{\hat{v}_{be}}{0.011} = \frac{10}{0.011} = 0.91 \text{ V}$$

To check whether the transistor remains in the active mode with v_i having a peak value $\hat{v}_i = 0.91\text{V}$, we have to evaluate the collector voltage. The voltage at the collector will consist of a triangular wave v_o superimposed on the dc value $V_C = 3.1$ V. The peak voltage of the triangular waveform will be

$$\hat{v}_o = \hat{v}_i \times \text{gain} = 0.91 \times 3.04 = 2.77 \text{ V}$$

It follows that when the output swings negative, the collector voltage reaches a minimum of $3.1 - 2.77 = 0.33$ V, which is lower than the base voltage by less than 0.4 V. Thus the transistor will remain in the active mode with v_i having a peak value of 0.91 V. Nevertheless, to be on the safe side, we will use a somewhat lower value for $\hat{v}_i$ of approximately 0.8 V, as shown in Fig. 7.29(a), and complete the analysis of this problem utilizing the equivalent circuit in Fig. 7.28(d). The signal current in the base will be triangular, with a peak value $\hat{i}_b$ of

$$\hat{i}_b = \frac{\hat{v}_i}{R_{BB} + r_\pi} = \frac{0.8}{100 + 1.09} = 0.008 \text{ mA}$$

This triangular-wave current will be superimposed on the quiescent base current I_B, as shown in Fig. 7.29(b). The base–emitter voltage will consist of a triangular-wave component superimposed on the dc V_{BE} that is approximately 0.7 V. The peak value of the triangular waveform will be

$$\hat{v}_{be} = \hat{v}_i \frac{r_\pi}{r_\pi + R_{BB}} = 0.8 \frac{1.09}{100 + 1.09} = 8.6 \text{ mV}$$

The total v_{BE} is sketched in Fig. 7.29(c).

The signal current in the collector will be triangular in waveform, with a peak value $\hat{i}_c$ given by

$$\hat{i}_c = \beta \hat{i}_b = 100 \times 0.008 = 0.8 \text{ mA}$$

This current will be superimposed on the quiescent collector current I_C (= 2.3 mA), as shown in Fig. 7.29(d).

The signal voltage at the collector can be obtained by multiplying v_i by the voltage gain; that is,

$$\hat{v}_o = 3.04 \times 0.8 = 2.43 \text{ V}$$

Figure 7.29(e) shows a sketch of the total collector voltage v_C versus time. Note the phase reversal between the input signal v_i and the output signal v_o.

Finally, we observe that each of the total quantities is the sum of a dc quantity (found from the dc circuit in Fig. 7.28b), and a signal quantity (found from the circuit in Fig. 7.28d).

Example 7.6 *continued*

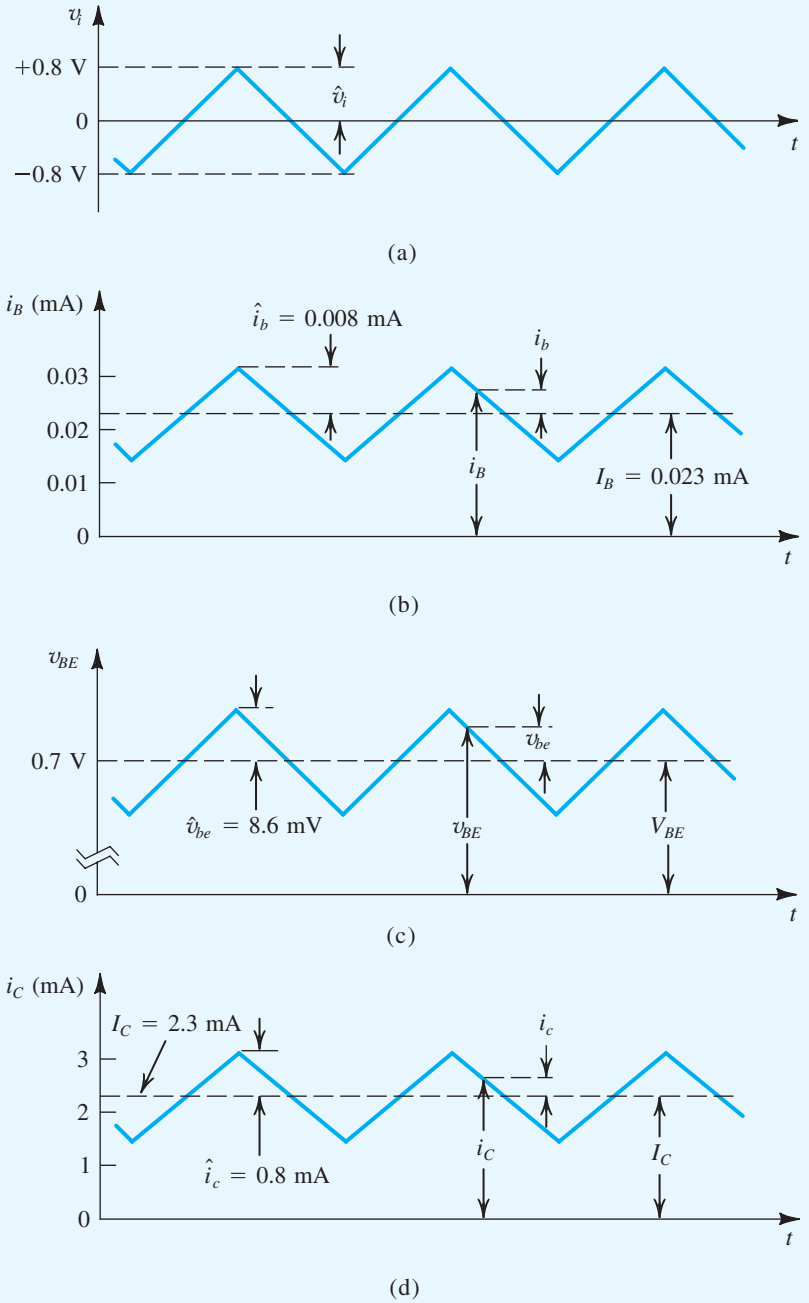


Figure 7.29 Signal waveforms in the circuit of Fig. 7.28.

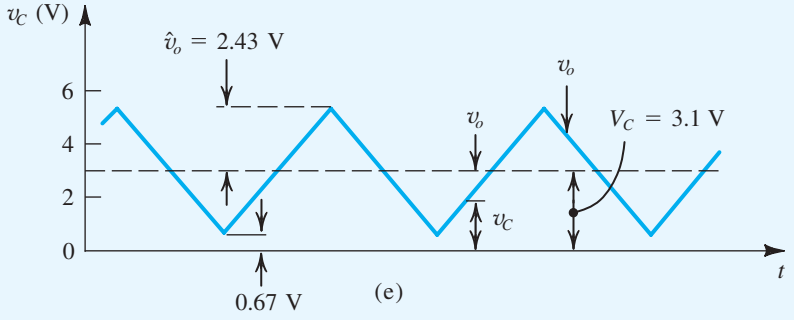


Figure 7.29 *continued*

Example 7.7

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will

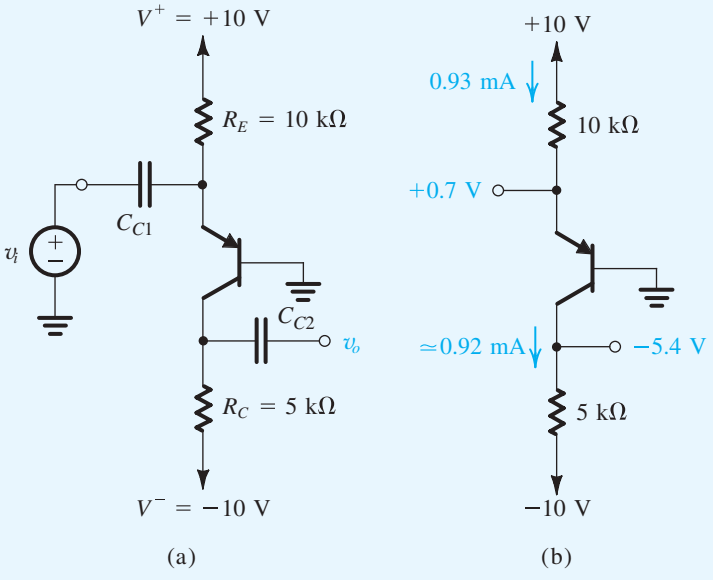


Figure 7.30 Example 7.7: (**a**) circuit; (**b**) dc analysis; (**c**) circuit with the dc sources eliminated; (**d**) small-signal analysis using the T model for the BJT.

Example 7.7 *continued*

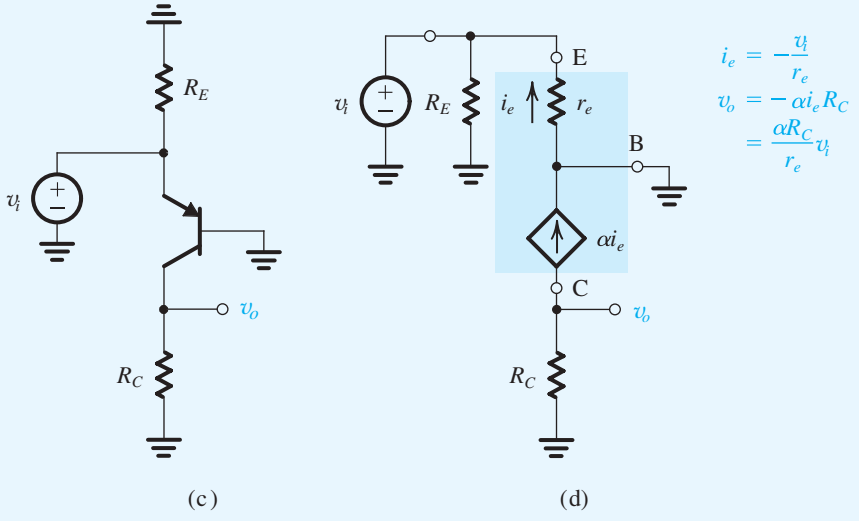


Figure 7.30 *continued*

not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Early effect.

Solution

Here again we shall follow a five-step process:

1. Figure 7.30(b) shows the circuit with the signal source and the coupling capacitors eliminated. The dc operating point can be determined as follows:

$$I_E = \frac{+10 - V_E}{R_E} \simeq \frac{+10 - 0.7}{10} = 0.93 \text{ mA}$$

Assuming $\beta = 100$, then $\alpha = 0.99$, and

$$\begin{aligned} I_C &= 0.99 I_E = 0.92 \text{ mA} \\ V_C &= -10 + I_C R_C \\ &= -10 + 0.92 \times 5 = -5.4 \text{ V} \end{aligned}$$

Thus the transistor is in the active mode.

2. We now determine the small-signal parameters as follows:

$$g_m = \frac{I_C}{V_T} = \frac{0.92}{0.025} = 36.8 \text{ mA/V}$$

$$r_e = \frac{V_T}{I_E} = \frac{0.025}{0.92} = 27.2\ \Omega$$

$$\beta = 100 \qquad \alpha = 0.99$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{36.8} = 2.72\ \text{k}\Omega$$

3. To prepare the circuit for small-signal analysis, we replace the dc sources with short circuits. The resulting circuit is shown in Fig. 7.30(c). Observe that we have also eliminated the two coupling capacitors, since they are assumed to be acting as perfect short circuits.

4. We are now ready to replace the BJT with one of the four equivalent-circuit models of Figs. 7.24 and 7.26. Although any of the four will work, the T models of Fig. 7.26 will be more convenient because the base is grounded. Selecting the version in Fig. 7.26(b) results in the amplifier equivalent circuit shown in Fig. 7.30(d).

5. Analysis of the circuit in Fig. 7.30(d) to determine the output voltage v_o and hence the voltage gain v_o/v_i is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = \frac{\alpha R_C}{r_e} = \frac{0.99 \times 5}{0.0272} = 182 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 7.5. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the *pnp* type.

Returning to the question of allowable signal magnitude, we observe from Fig. 7.30(d) that $v_{eb} = v_i$. Thus, if small-signal operation is desired (for linearity), then the peak of v_i should be limited to approximately 10 mV. With $\hat{V}_i$ set to this value, as shown for a sine-wave input in Fig. 7.31, the peak amplitude at the collector, $\hat{V}_o$, will be

$$\hat{V}_o = 182 \times 0.01 = 1.82 \text{ V}$$

Example 7.7 *continued*

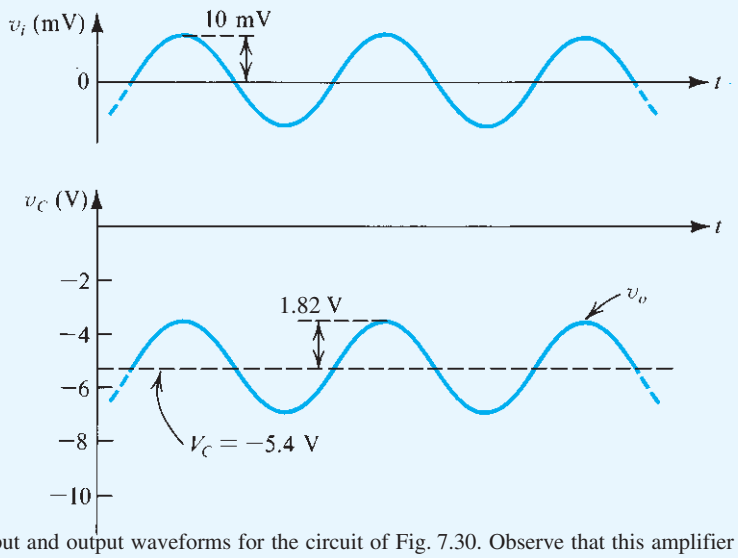


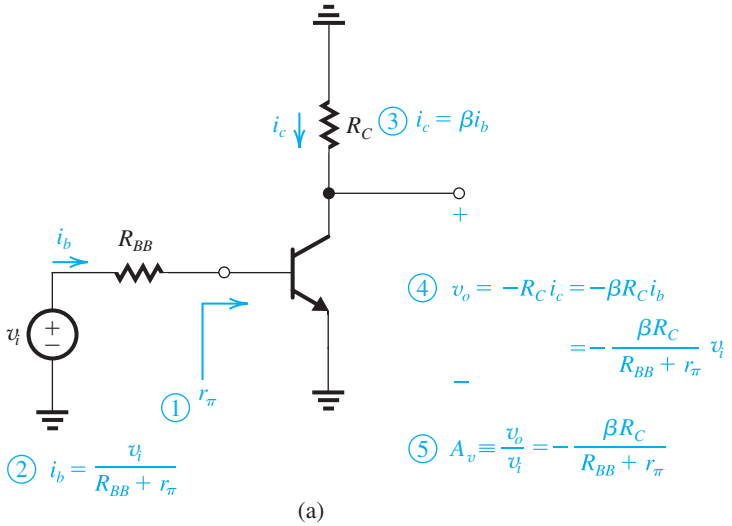
Figure 7.31 Input and output waveforms for the circuit of Fig. 7.30. Observe that this amplifier is noninverting, a property of the grounded-base configuration.

EXERCISE

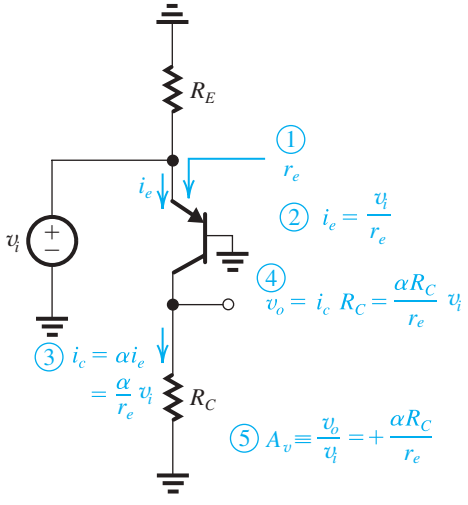
7.19 To increase the voltage gain of the amplifier analyzed in Example 7.7, the collector resistance R_C is increased to 7.5 kΩ. Find the new values of V_C, A_v, and the peak amplitude of the output sine wave corresponding to an input sine wave v_i of 10-mV peak.
Ans. –3.1 V; 276 V/V; 2.76 V

Performing Small-Signal Analysis Directly on the Circuit Diagram In most cases one should explicitly replace each BJT with its small-signal model and analyze the resulting circuit, as we have done in the examples above. This systematic procedure is particularly recommended for beginning students. Experienced circuit designers, however, often perform a first-order analysis directly on the circuit. Figure 7.32 illustrates this process for the two

circuits we analyzed in Examples 7.5 and 7.7. The reader is urged to follow this direct analysis procedure (the steps are numbered). Observe that the equivalent-circuit model is *implicitly* utilized; we are only saving the step of drawing the circuit with the BJT replaced by its model. Direct analysis, however, has an additional very important benefit: It provides insight regarding the signal transmission through the circuit. Such insight can prove invaluable in design, particularly at the stage of selecting a circuit configuration appropriate for a given application. Direct analysis can be utilized also for MOS amplifier circuits.



(a)



(b)

Figure 7.32 Performing signal analysis directly on the circuit diagram with the BJT small-signal model implicitly employed: (**a**) circuit for Example 7.5; (**b**) circuit for Example 7.7.

EXERCISE

7.20 The transistor in Fig. E7.20 is biased with a constant current source $I = 1$ mA and has $\beta = 100$ and $V_A = 100$ V.

(a) Neglecting the Early effect, find the dc voltages at the base, emitter, and collector.

(b) Find g_m, r_π, and r_o.

(c) If terminal Z is connected to ground, X to a signal source v_{sig} with a source resistance $R_{sig} = 2$ kΩ, and Y to an 8-kΩ load resistance, use the hybrid-π model shown earlier (Fig. 7.25) to draw the small-signal equivalent circuit of the amplifier. (Note that the current source I should be replaced with an open circuit.) Calculate the overall voltage gain v_y/v_{sig}. If r_o is neglected, what is the error in estimating the gain magnitude? (*Note:* An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

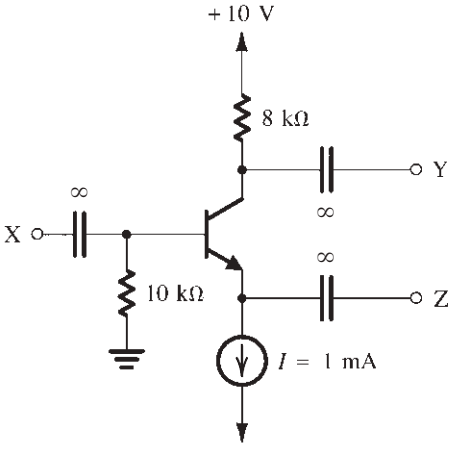


Figure E7.20

Ans. (a) –0.1 V, –0.8 V, +2.1 V; (b) 40 mA/V, 2.5 kΩ, 100 kΩ; (c) –77 V/V, +3.9%

7.2.3 Summary Tables

We conclude this section by presenting three useful summary tables: Table 7.1 lists the five steps to be followed in the analysis of a MOSFET or a BJT amplifier circuit. Table 7.2 presents the MOSFET small-signal, equivalent-circuit models, together with the formulas for calculating the parameter values of the models. Finally, Table 7.3 supplies the corresponding data for the BJT.

Table 7.1 Systematic Procedure for the Analysis of Transistor Amplifier Circuits

1. Eliminate the signal source and determine the dc operating point of the transistor.
2. Calculate the values of the parameters of the small-signal model.
3. Eliminate the dc sources by replacing each dc voltage source by a short circuit and each dc current source by an open circuit.
4. Replace the transistor with one of its small-signal, equivalent-circuit models. Although any of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer in the next section.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance).

Table 7.2 Small-Signal Models of the MOSFET

Small-Signal Parameters

NMOS transistors

- **Transconductance:**

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

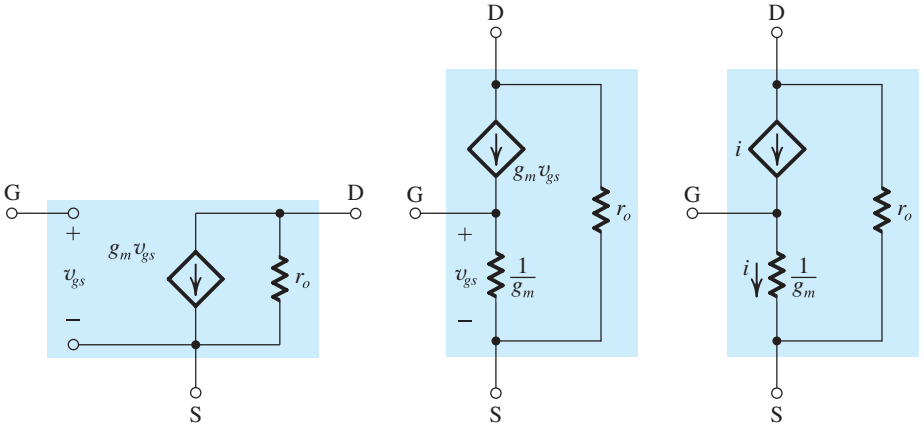
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS *except* using $|V_{OV}|$, $|V_A|$, $|\lambda|$ and replacing μ_n with μ_p.

Small-Signal, Equivalent-Circuit Models

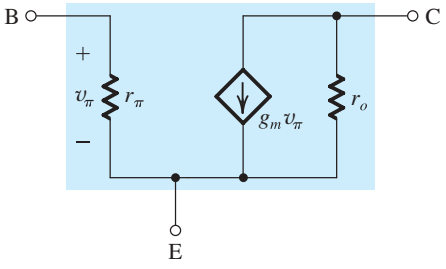


Hybrid-π model T models

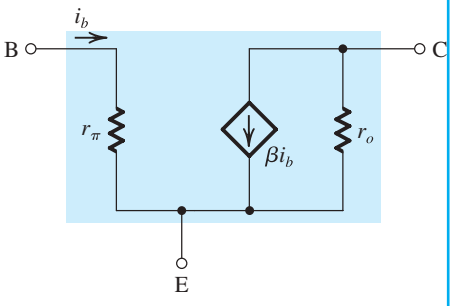
Table 7.3 Small-Signal Models of the BJT

Hybrid-π Model

■ $(g_m v_\pi)$ Version

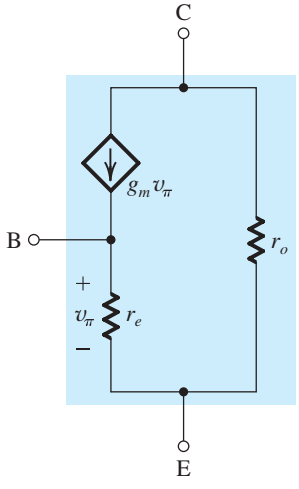


■ (βi_b) Version

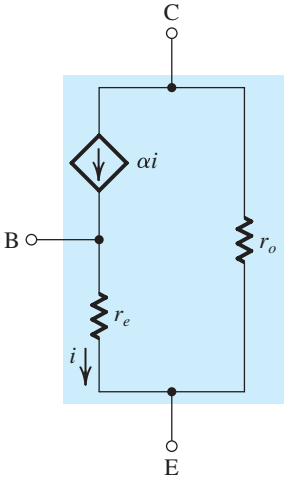


T Model

■ $(g_m v_\pi)$ Version



■ (αi) Version



Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\frac{V_T}{I_C} \qquad r_\pi = \frac{V_T}{I_B} = \beta\frac{V_T}{I_C} \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta + 1 = \frac{1}{1-\alpha}$$

7.3 Basic Configurations

It is useful at this point to take stock of where we are and where we are going in our study of transistor amplifiers. In Section 7.1 we examined the underlying principle for the application of the MOSFET, and of the BJT, as an amplifier. There we found that almost-linear amplification can be obtained by dc biasing the transistor at an appropriate point in its active region of operation, and by keeping the input signal (v_{gs} or v_{be}) small. We then developed, in Section 7.2, circuit models that represent the small-signal operation of each of the two transistor types (Tables 7.2 and 7.3), thus providing a systematic procedure (Table 7.1) for the analysis of transistor amplifiers.

We are now ready to consider the various possible configurations of MOSFET and BJT amplifiers, and we will do that in the present section. To focus our attention on the salient features of the various configurations, we shall present them in their most simple, or "stripped-down," version. Thus, we will not show the dc biasing arrangements, leaving the study of bias design to the next section. Finally, in Section 7.5 we will bring everything together and present practical *discrete-circuit amplifiers*, namely, amplifier circuits that can be constructed using discrete components. The study of integrated-circuit amplifiers begins in Chapter 8.

7.3.1 The Three Basic Configurations

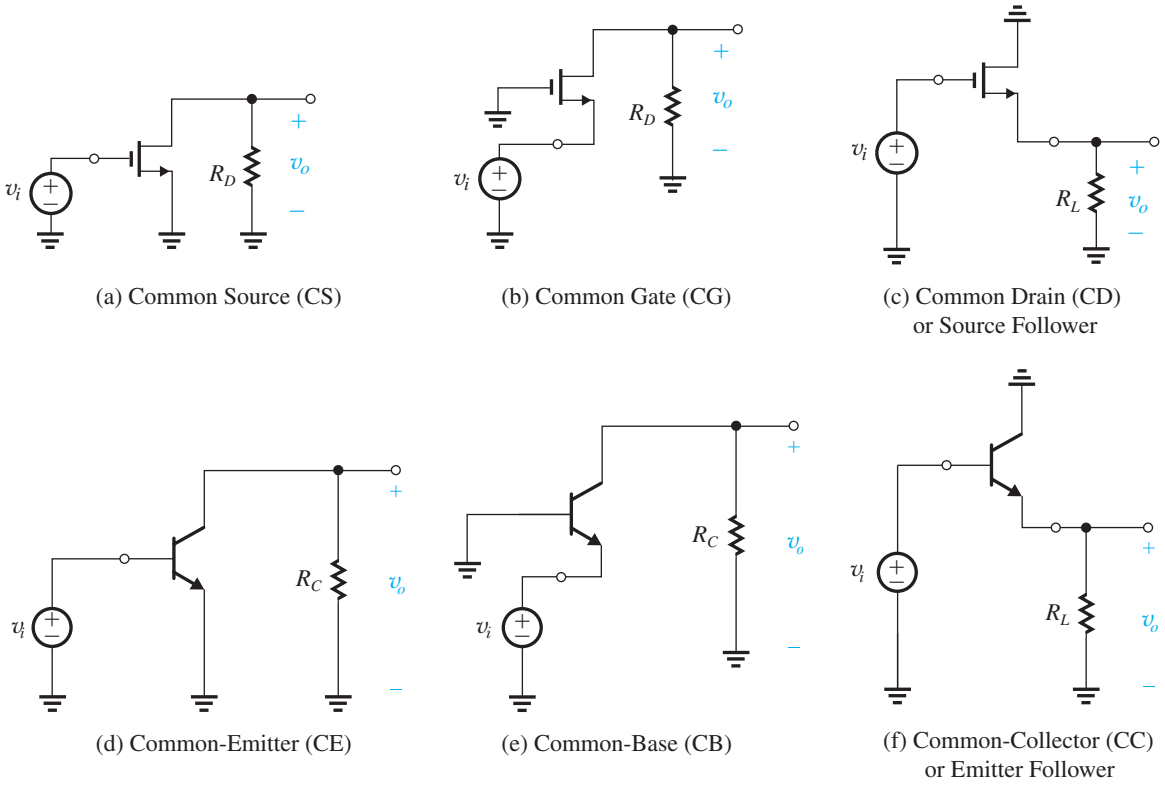
There are three basic configurations for connecting a MOSFET or a BJT as an amplifier. Each of these configurations is obtained by connecting one of the device terminals to ground, thus creating a two-port network with the grounded terminal being *common* to the input and output ports. The resulting configurations are shown in Fig. 7.33(a–c) for the MOSFET and in Fig. 7.33(d–f) for the BJT.

In the circuit of Fig. 7.33(a) the source terminal is connected to ground, the input voltage signal v_i is applied between the gate and ground, and the output voltage signal v_o is taken between the drain and ground, across the resistance R_D. This configuration, therefore, is called the grounded-source or **common-source (CS)** amplifier. It is by far the most popular MOS amplifier configuration, and we utilized it in Sections 7.1 and 7.2 to study MOS amplifier operation. A parallel set of remarks apply to the BJT counterpart, the grounded-emitter or **common-emitter (CE)** amplifier in Fig. 7.33(d).

The **common-gate (CG)** or grounded-gate amplifier is shown in Fig. 7.33(b), and its BJT counterpart, the **common-base (CB)** or grounded-base amplifier in Fig. 7.33(e). Here the gate (base) is grounded, the input signal v_i is applied to the source (emitter), and the output signal v_o is taken at the drain (collector) across the resistance R_D (R_C). We encountered a CG amplifier in Example 7.4 and a CB amplifier in Example 7.7.

Finally, Fig. 7.33(c) shows the **common drain (CD)** or grounded-drain amplifier, and Fig. 7.31(f) shows its BJT counterpart, the **common-collector (CC)** or grounded collector amplifier. Here the drain (collector) terminal is grounded, the input signal v_i is applied between gate (base) and ground, and the output voltage v_o is taken between the source (emitter) and ground, across a resistance R_L. For reasons that will become apparent shortly, this pair of configurations is more commonly called the **source follower** and the **emitter follower**.

Our study of the three basic amplifier configurations of the MOSFET and of the BJT will reveal that each has distinctly different attributes, hence areas of application. As well, it will be shown that although each pair of configurations, (e.g., CS and CE), has many common attributes, important differences remain.



(a) Common Source (CS)

(b) Common Gate (CG)

(c) Common Drain (CD) or Source Follower

(d) Common-Emitter (CE)

(e) Common-Base (CB)

(f) Common-Collector (CC) or Emitter Follower

Figure 7.33 The basic configurations of transistor amplifiers. (**a**)–(**c**) For the MOSFET; (**d**)–(**f**) for the BJT.

Our next step is to replace the transistor in each of the six circuits in Fig. 7.33 by an appropriate equivalent-circuit model (from Tables 7.2 and 7.3) and analyze the resulting circuits to determine important characteristic parameters of the particular amplifier configuration. To simplify matters, we shall not include r_o in the initial analysis. At the end of the section we will offer a number of comments about when to include r_o in the analysis, and on the expected magnitude of its effect.

7.3.2 Characterizing Amplifiers

Before we begin our study of the different transistor amplifier configurations, we consider how to characterize the performance of an amplifier as a circuit building block. An introduction to this topic was presented in Section 1.5.

Figure 7.34(a) shows an amplifier fed with a signal source having an open-circuit voltage v_{sig} and an internal resistance R_{sig}. These can be the parameters of an actual signal source or, in a cascade amplifier, the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study. The amplifier is shown with a load resistance R_L connected to the output terminal. Here, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

Figure 7.34(b) shows the amplifier circuit with the amplifier block replaced by its equivalent-circuit model. The input resistance R_{in} represents the loading effect of the amplifier

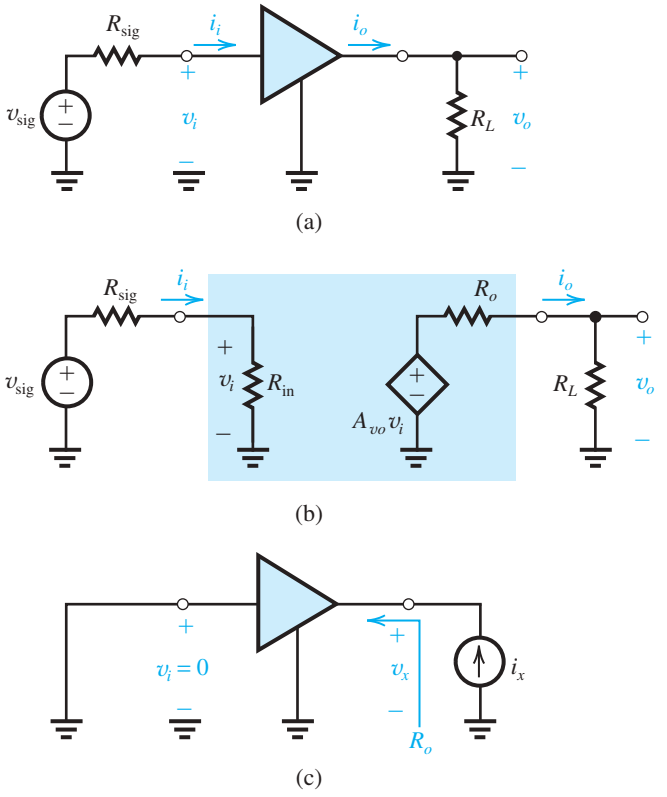


Figure 7.34 Characterization of the amplifier as a functional block: **(a)** An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig}, and feeding a load resistance R_L; **(b)** equivalent-circuit representation of the circuit in **(a)**; **(c)** determining the amplifier output resistance R_o.

input on the signal source. It is found from

$$R_{in} \equiv \frac{v_i}{i_i}$$

and together with the resistance R_{sig} forms a voltage divider that reduces v_{sig} to the value v_i that appears at the amplifier input,

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} \tag{7.83}$$

Most of the amplifier circuits studied in this section are **unilateral**. That is, they do not contain internal feedback, and thus R_{in} will be independent of R_L. However, in general R_{in} may depend on the load resistance R_L. Indeed one of the six configurations studied in this section, the emitter follower, exhibits such dependence.

The second parameter in characterizing amplifier performance is the **open-circuit voltage gain** A_{vo}, defined as

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

The third and final parameter is the output resistance R_o. Observe from Fig. 7.34(b) that R_o is the resistance seen looking back into the amplifier output terminal with v_i set to zero. Thus R_o can be determined, at least conceptually, as indicated in Fig. 7.34(c) with

$$R_o = \frac{v_x}{i_x}$$

Because R_o is determined with $v_i = 0$, the value of R_o does not depend on R_{sig}.

The controlled source $A_{vo}v_i$ and the output resistance R_o represent the Thévenin equivalent of the amplifier output circuit, and the output voltage v_o can be found from

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i \tag{7.84}$$

Thus the **voltage gain of the amplifier proper**, A_v, can be found as

$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \tag{7.85}$$

and the **overall voltage gain**, G_v,

$$G_v \equiv \frac{v_o}{v_{\text{sig}}}$$

can be determined by combining Eqs. (7.83) and (7.85):

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_{vo} \frac{R_L}{R_L + R_o} \tag{7.86}$$

7.3.3 The Common-Source (CS) and Common-Emitter (CE) Amplifiers

Of the three basic transistor amplifier configurations, the common-source (common-emitter, for BJT), is the most widely used. Typically, in an amplifier formed by cascading a number of gain stages, the bulk of the voltage gain is obtained by using one or more common-source (or common-emitter, for BJT) stages in cascade.

Characteristic Parameters of the CS Amplifier Figure 7.35(a) shows a common-source amplifier (with the biasing arrangement omitted) fed with a signal source v_{sig} having a source resistance R_{sig}. We wish to analyze this circuit to determine R_{in}, A_{vo}, and R_o. For this purpose, we assume that R_D is part of the amplifier; thus if a load resistance R_L is connected to the amplifier output, R_L appears in parallel with R_D. In such a case, we wish to determine A_v and G_v as well.

Replacing the MOSFET with its hybrid-π model (without r_o), we obtain the CS amplifier equivalent circuit in Fig. 7.35(b) for which, tracing the signal from input to output, we can write by inspection

$$\begin{aligned} R_{\text{in}} &= \infty \\ v_i &= v_{\text{sig}} \\ v_{gs} &= v_i \\ v_o &= -g_m v_{gs} R_D \end{aligned} \tag{7.87}$$

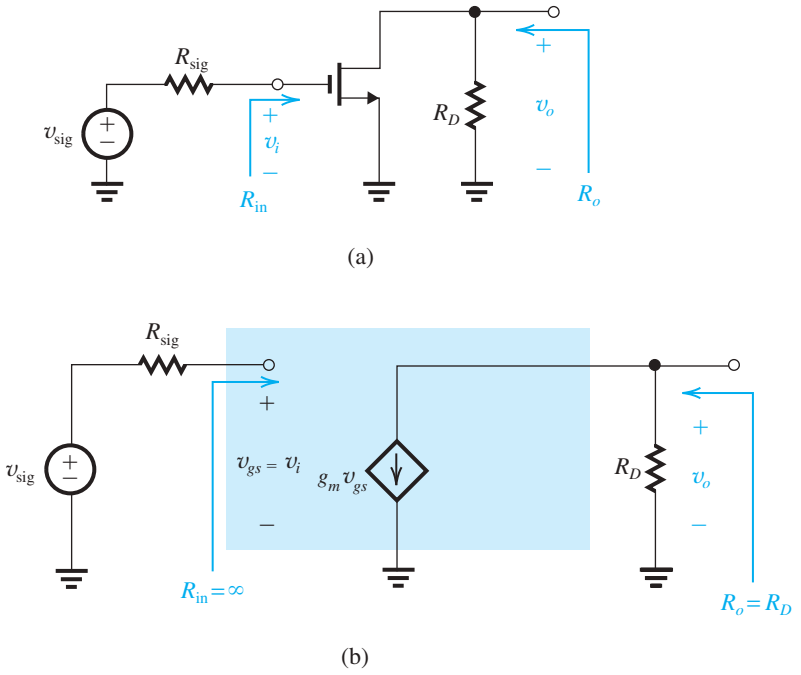


Figure 7.35 **(a)** Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig}. The bias circuit is omitted. **(b)** The common-source amplifier with the MOSFET replaced with its hybrid-π model.

Thus,

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_D \tag{7.88}$$

$$R_o = R_D \tag{7.89}$$

If a load resistance R_L is connected across R_D, the voltage gain A_v can be obtained from

$$A_v = A_{vo} \frac{R_L}{R_L + R_o} \tag{7.90}$$

where A_{vo} is given by Eq. (7.88) and R_o by Eq. (7.89), or alternatively by simply adding R_L in parallel with R_D in Eq. (7.88), thus

$$A_v = -g_m (R_D \| R_L) \tag{7.91}$$

The reader can easily show that the expression obtained from Eq. (7.90) is identical to that in Eq. (7.91). Finally, since $R_{in} = \infty$ and thus $v_i = v_{sig}$, the overall voltage gain G_v is equal to A_v,

$$G_v \equiv \frac{v_o}{v_{sig}} = -g_m (R_D \| R_L) \tag{7.92}$$

EXERCISE

7.21 A CS amplifier utilizes a MOSFET biased at $I_D = 0.25$ mA with $V_{OV} = 0.25$ V and $R_D = 20$ kΩ. The amplifier is fed with a signal source having $R_{sig} = 100$ kΩ, and a 20-kΩ load is connected to the output. Find R_{in}, A_{vo}, R_o, A_v, and G_v. If, to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of $2V_{OV}$, what is the peak of the sine-wave voltage at the output?
Ans. ∞; −40 V/V; 20 kΩ; −20 V/V; −20 V/V; 1 V

Characteristic Parameters of the CE Amplifier Figure 7.36(a) shows a common-emitter amplifier. Its equivalent circuit, obtained by replacing the BJT with its hybrid-π model (without r_o), is shown in Fig. 7.36(b). The latter circuit can be analyzed to obtain the characteristic parameters of the CE amplifier. The analysis parallels that for the MOSFET above except that here we have the added complexity of a finite input resistance r_π. Tracing the signal through the amplifier from input to output, we can write by inspection

$$R_{in} = r_\pi$$

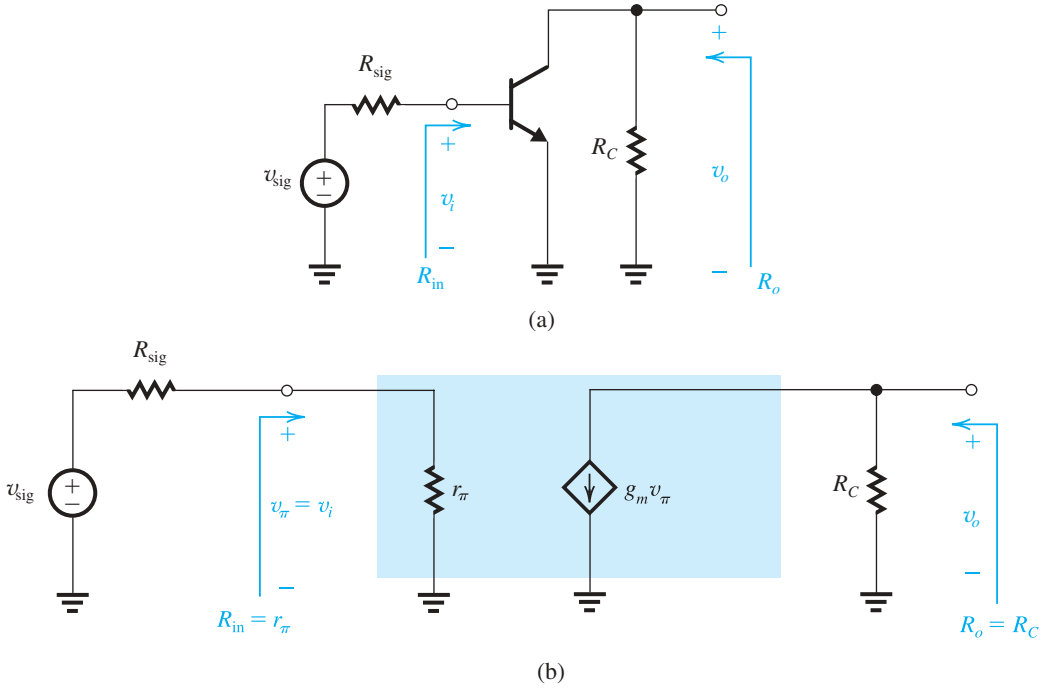


Figure 7.36 (**a**) Common-emitter amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig}. The bias circuit is omitted. (**b**) The common-emitter amplifier circuit with the BJT replaced by its hybrid-π model.

Then we write

$$v_i = \frac{r_\pi}{r_\pi + R_{\text{sig}}} v_{\text{sig}} \tag{7.93}$$

$$v_\pi = v_i$$

$$v_o = -g_m v_\pi R_C$$

Thus,

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m R_C \tag{7.94}$$

$$R_o = R_C \tag{7.95}$$

With a load resistance R_L connected across R_C,

$$A_v = -g_m (R_C \| R_L) \tag{7.96}$$

and the overall voltage gain G_v can be found from

$$G_v \equiv \frac{v_o}{v_{\text{sig}}} = \frac{v_i}{v_{\text{sig}}} \frac{v_o}{v_i}$$

Thus,

$$G_v = -\frac{r_\pi}{r_\pi + R_{\text{sig}}} g_m (R_C \| R_L) \tag{7.97}$$

It is important to note here the effect of the finite input resistance (r_π) in reducing the magnitude of the voltage gain by the voltage-divider ratio $r_\pi/(r_\pi + R_{\text{sig}})$. The extent of the gain reduction depends on the relative values of r_π and R_{sig}. However, there is a compensating effect in the CE amplifier: g_m of the BJT is usually much higher than the corresponding value of the MOSFET.

Example 7.8

A CE amplifier utilizes a BJT with $\beta = 100$ is biased at $I_C = 1$ mA and has a collector resistance $R_C = 5\,\text{k}\Omega$. Find R_{in}, R_o, and A_{vo}. If the amplifier is fed with a signal source having a resistance of 5 kΩ, and a load resistance $R_L = 5\,\text{k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v. If $\hat{v}_\pi$ is to be limited to 5 mV, what are the corresponding $\hat{v}_{\text{sig}}$ and $\hat{v}_o$ with the load connected?

Solution

At $I_C = 1$ mA,

$$g_m = \frac{I_C}{V_T} = \frac{1\text{ mA}}{0.025\text{ V}} = 40\text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40\text{ mA/V}} = 2.5\,\text{k}\Omega$$

Example 7.8 *continued*

The amplifier characteristic parameters can now be found as

$$\begin{aligned} R_{\text{in}} &= r_\pi = 2.5\,\text{k}\Omega \\ A_{vo} &= -g_m R_C \\ &= -40\,\text{mA/V} \times 5\,\text{k}\Omega \\ &= -200\,\text{V/V} \\ R_o &= R_C = 5\,\text{k}\Omega \end{aligned}$$

With a load resistance $R_L = 5\,\text{k}\Omega$ connected at the output, we can find A_v by either of the following two approaches:

$$\begin{aligned} A_v &= A_{vo}\frac{R_L}{R_L + R_o} \\ &= -200 \times \frac{5}{5+5} = -100\,\text{V/V} \end{aligned}$$

or

$$\begin{aligned} A_v &= -g_m(R_C \,\|\, R_L) \\ &= -40(5 \,\|\, 5) = -100\,\text{V/V} \end{aligned}$$

The overall voltage gain G_v can now be determined as

$$\begin{aligned} G_v &= \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_v \\ &= \frac{2.5}{2.5+5} \times -100 = -33.3\,\text{V/V} \end{aligned}$$

If the maximum amplitude of v_π is to be 5 mV, the corresponding value of $\hat{v}_{\text{sig}}$ will be

$$\hat{v}_{\text{sig}} = \left(\frac{R_{\text{in}} + R_{\text{sig}}}{R_{\text{in}}}\right)\hat{v}_\pi = \frac{2.5+5}{2.5} \times 5 = 15\,\text{mV}$$

and the amplitude of the signal at the output will be

$$\hat{v}_o = G_v \hat{v}_{\text{sig}} = 33.3 \times 0.015 = 0.5\,\text{V}$$

EXERCISE

7.22 The designer of the amplifier in Example 7.8 decides to lower the bias current to half its original value in order to raise the input resistance and hence increase the fraction of v_{sig} that appears at the input of the amplifier proper. In an attempt to maintain the voltage gain, the designer decides to double the value of R_C. For the new design, determine R_{in}, A_{vo}, R_o, A_v, and G_v. If the peak amplitude of v_π is to be limited to 5 mV, what are the corresponding values of $\hat{v}_{sig}$ and $\hat{v}_o$ (with the load connected)?
Ans. 5 kΩ; −200 V/V; 10 kΩ; −66.7 V/V; −33.3 V/V; 10 mV; 0.33 V

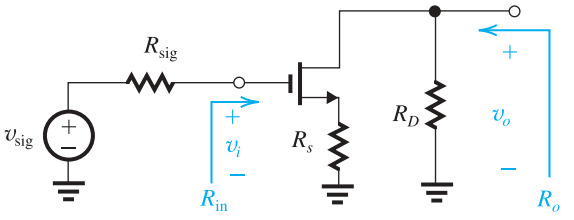
Comment: Although a larger fraction of the input signal reaches the amplifier input, linearity considerations cause the output signal to be in fact smaller than in the original design!

Final Remarks

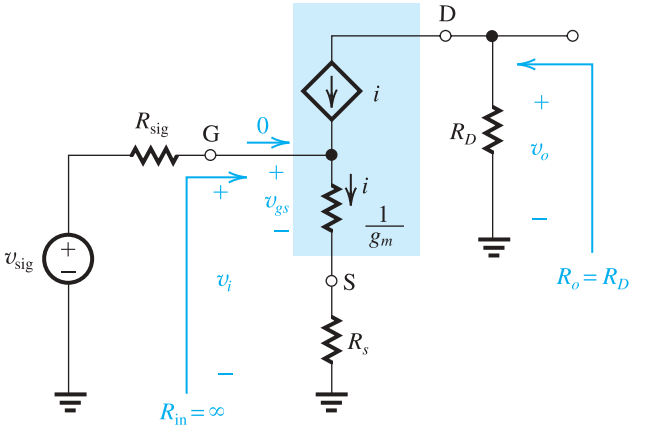
1. The CS and CE amplifiers are the most useful of all transistor amplifier configurations. They exhibit a moderate to high input resistance (infinite for the CS), a moderate to high output resistance, and reasonably high voltage gain.
2. The input resistance of the CE amplifier, $R_{in} = r_\pi = \beta/g_m$, is inversely proportional to the dc bias current I_C. To increase R_{in} one is tempted to lower the bias current I_C; however, this also lowers g_m and hence the voltage gain. This is a significant design trade-off. If a much higher input resistance is desired, then a modification of the CE configuration (to be discussed in Section 7.3.4) can be applied, or an emitter-follower stage can be inserted between the signal source and the CE amplifier (see Section 7.3.6).
3. Reducing R_D or R_C to lower the output resistance of the CS or CE amplifier, respectively, is usually not a viable proposition because the voltage gain is also reduced. Alternatively, if a very low output resistance (in the ohms or tens-of-ohms range) is needed, a source-follower or an emitter-follower stage can be utilized between the output of the CS or CE amplifier and the load resistance (see Section 7.3.6).
4. Although the CS and the CE configurations are the workhorses of transistor amplifiers, both suffer from a limitation on their high-frequency response. As will be shown in Chapter 10, combining the CS (CE) amplifier with a CG (CB) amplifier can extend the bandwidth considerably. The CG and CB amplifiers are studied in Section 7.3.5.

7.3.4 The Common-Source (Common-Emitter) Amplifier with a Source (Emitter) Resistance

It is often beneficial to insert a resistance R_s (a resistance R_e) in the source lead (the emitter lead) of a common-source (common-emitter) amplifier. Figure 7.37(a) shows a CS amplifier with a resistance R_s in its source lead. The corresponding small-signal equivalent circuit is shown



(a)



(b)

Figure 7.37 The CS amplifier with a source resistance R_s: **(a)** circuit without bias details; **(b)** equivalent circuit with the MOSFET represented by its T model.

in Fig. 7.37(b), where we have utilized the T model for the MOSFET. The T model is used in preference to the hybrid-π model because it makes the analysis in this case considerably simpler. In general, *whenever a resistance is connected in the source lead, the T model is preferred*. The source resistance then simply appears in series with the model resistance $1/g_m$ and can be added to it.

From Fig. 7.37(b) we see that as expected, the input resistance R_{in} is infinite and thus $v_i = v_{sig}$. Unlike the CS amplifier, however, here only a fraction of v_i appears between gate and source as v_{gs}. The voltage divider composed of $1/g_m$ and R_s, which appears across the amplifier input, can be used to determine v_{gs}, as follows:

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s} \tag{7.98}$$

Thus we can use the value of R_s to control the magnitude of the signal v_{gs} and thereby ensure that v_{gs} does not become too large and cause unacceptably high nonlinear distortion. This is the first benefit of including resistor R_s. Other benefits will be encountered in later sections and chapters. For instance, it will be shown in Chapter 10 that R_s causes the useful bandwidth of the amplifier to be extended. The mechanism by which R_s causes such improvements in amplifier performance is *negative feedback*. To see how R_s introduces negative feedback, refer to Fig. 7.37(a): If with v_{sig} and hence v_i kept constant, the drain current increases for some

reason, the source current also will increase, resulting in an increased voltage drop across R_s. Thus the source voltage rises, and the gate-to-source voltage decreases. The latter effect causes the drain current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 11 we shall study negative feedback formally. There we will learn that the improvements that negative feedback provides are obtained at the expense of a reduction in gain. We will now show this to be the case in the circuit of Fig. 7.37.

The output voltage v_o is obtained by multiplying the controlled-source current i by R_D,

$$v_o = -iR_D$$

The current i in the source lead can be found by dividing v_i by the total resistance in the source,

$$i = \frac{v_i}{1/g_m + R_s} = \left(\frac{g_m}{1 + g_m R_s}\right) v_i \tag{7.99}$$

Thus, the voltage gain A_{vo} can be found as

$$A_{vo} \equiv \frac{v_o}{v_i} = -\frac{g_m R_D}{1 + g_m R_s} \tag{7.100}$$

which can also be expressed as

$$A_{vo} = -\frac{R_D}{1/g_m + R_s} \tag{7.101}$$

Equation (7.100) indicates that including the resistance R_s reduces the voltage gain by the factor $(1 + g_m R_s)$. This is the price paid for the improvements that accrue as a result of R_s. It is interesting to note that in Chapter 11, we will find that the factor $(1 + g_m R_s)$ is the "amount of negative feedback" introduced by R_s. It is also the same factor by which linearity, bandwidth, and other performance parameters improve. Because of the negative-feedback action of R_s it is known as a **source-degeneration resistance**.

There is another useful interpretation of the expression for the drain current in Eq. (7.99): The quantity between brackets on the right-hand side can be thought of as the "effective transconductance with R_s included." Thus, including R_s reduces the transconductance by the factor $(1 + g_m R_s)$. This, of course, is simply the result of the fact that only a fraction $1/(1 + g_m R_s)$ of v_i appears as v_{gs} (see Eq. 7.98).

The alternative gain expression in Eq. (7.101) has a powerful and insightful interpretation: The voltage gain between gate and drain is equal to the ratio of the total resistance in the drain (R_D) to the total resistance in the source $(1/g_m + R_s)$,

$$\text{Voltage gain from gate to drain} = -\frac{\text{Total resistance in drain}}{\text{Total resistance in source}} \tag{7.102}$$

This is a general expression. For instance, setting $R_s = 0$ in Eq. (7.101) yields A_{vo} of the CS amplifier.

Finally, we consider the situation of a load resistance R_L connected at the output. We can obtain the gain A_v using the open-circuit voltage gain A_{vo} together with the output resistance R_o, which can be found by inspection to be

$$R_o = R_D$$

Alternatively, A_v can be obtained by simply replacing R_D in Eq. (7.101) or (7.100) by $(R_D \| R_L)$; thus,

$$A_v = -\frac{g_m(R_D \| R_L)}{1 + g_m R_s} \tag{7.103}$$

or

$$A_v = -\frac{R_D \| R_L}{1/g_m + R_s} \tag{7.104}$$

Observe that Eq. (7.104) is a direct application of the ratio of total resistance rule of Eq. (7.102). Finally, note that because R_{in} is infinite, $v_i = v_{\text{sig}}$ and the overall voltage gain G_v is equal to A_v.

EXERCISE

7.23 In Exercise 7.21 we applied an input signal v_{sig} of 50 mV peak and obtained an output signal of approximately 1 V peak. Assume that for some reason we now have an input signal v_{sig} that is 0.2 V peak and that we wish to modify the circuit to keep v_{gs} unchanged, and thus keep the nonlinear distortion from increasing. What value should we use for R_s? What value of G_v will result? What will the peak signal at the output become? Assume $r_o = \infty$.

Ans. 1.5 kΩ; −5 V/V; 1 V

We next turn our attention to the BJT case. Figure 7.38(a) shows a CE amplifier with a resistance R_e in its emitter. The corresponding equivalent circuit, utilizing the T model, is shown in Fig. 7.38(b). Note that in the BJT case also, as a general rule, the T model results in a simpler analysis and should be employed whenever there is a resistance in series with the emitter.

To determine the amplifier input resistance R_{in}, we note from Fig. 7.38(b) that

$$R_{\text{in}} \equiv \frac{v_i}{i_b}$$

where

$$i_b = (1 - \alpha) i_e = \frac{i_e}{\beta + 1} \tag{7.105}$$

and

$$i_e = \frac{v_i}{r_e + R_e} \tag{7.106}$$

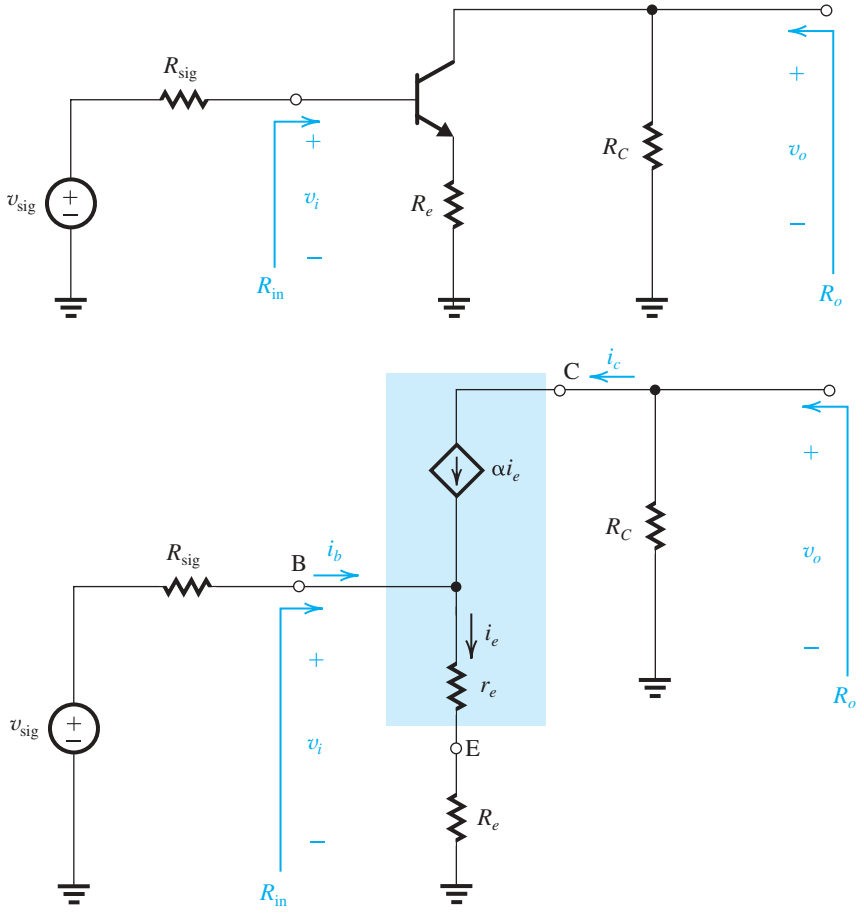


Figure 7.38 The CE amplifier with an emitter resistance R_e; (**a**) circuit without bias details; (**b**) equivalent circuit with the BJT replaced with its T model.

Thus,

$$R_{in} = (\beta + 1)(r_e + R_e) \tag{7.107}$$

This is a very important result. It states that *the input resistance looking into the base is* $(\beta + 1)$ *times the total resistance in the emitter*, and is known as the **resistance-reflection rule**. The factor $(\beta + 1)$ arises because the base current is $1/(\beta + 1)$ times the emitter current. The expression for R_{in} in Eq. (7.107) shows clearly that including a resistance R_e in the emitter can substantially increase R_{in}, a very desirable result. Indeed, the value of R_{in} is increased by the ratio

$$\frac{R_{in}(\text{with } R_e \text{ included})}{R_{in}(\text{without } R_e)} = \frac{(\beta + 1)(r_e + R_e)}{(\beta + 1)r_e}$$

$$= 1 + \frac{R_e}{r_e} \simeq 1 + g_m R_e \tag{7.108}$$

Thus the circuit designer can use the value of R_e to control the value of R_{in}.

To determine the voltage gain A_{vo}, we see from Fig. 7.38(b) that

$$\begin{aligned} v_o &= -i_c R_C \\ &= -\alpha i_e R_C \end{aligned}$$

Substituting for i_e from Eq. (7.106) gives

$$A_{vo} = -\alpha \frac{R_C}{r_e + R_e} \tag{7.109}$$

This is a very useful result: It states that the gain from base to collector is α times the ratio of the total resistance in the collector to the total resistance in the emitter (in this case, $r_e + R_e$),

$$\text{Voltage gain from base to collector} = -\alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}} \tag{7.110}$$

This is the BJT version of the MOSFET expression in Eq. (7.102) except that here we have the additional factor α. This factor arises because $i_c = \alpha i_e$, unlike the MOSFET case where $i_d = i_s$. Usually, $\alpha \simeq 1$ and can be dropped from Eq. (7.110).

The open-circuit voltage gain in Eq. (7.109) can be expressed alternatively as

$$A_{vo} = -\frac{\alpha}{r_e} \frac{R_C}{1 + R_e/r_e}$$

Thus,

$$A_{vo} = -\frac{g_m R_C}{1 + R_e/r_e} \simeq -\frac{g_m R_C}{1 + g_m R_e} \tag{7.111}$$

Thus, including R_e reduces the voltage gain by the factor $(1 + g_m R_e)$, which is the same factor by which R_{in} is increased. This points out an interesting trade-off between gain and input resistance, a trade-off that the designer can exercise through the choice of an appropriate value for R_e.

The output resistance R_o can be found from the circuit in Fig. 7.38(b) by inspection:

$$R_o = R_C$$

If a load resistance R_L is connected at the amplifier output, A_v can be found as

$$\begin{aligned} A_v &= A_{vo} \frac{R_L}{R_L + R_o} \\ &= -\alpha \frac{R_C}{r_e + R_e} \frac{R_L}{R_L + R_C} \\ &= -\alpha \frac{R_C \parallel R_L}{r_e + R_e} \end{aligned} \tag{7.112}$$

which could have been written directly using Eq. (7.110). The overall voltage gain G_v can now be found:

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \times -\alpha \frac{R_C \parallel R_L}{r_e + R_e}$$

Substituting for R_{in} from Eq. (7.107) and replacing α with $\beta/(\beta+1)$ results in

$$G_v = -\beta \frac{R_C \parallel R_L}{R_{\text{sig}} + (\beta+1)(r_e + R_e)} \tag{7.113}$$

Careful examination of this expression reveals that the denominator comprises the total resistance in the base circuit [recall that $(\beta+1)(r_e+R_e)$ is the reflection of (r_e+R_e) from the emitter side to the base side]. Thus the expression in Eq. (7.113) states that the voltage gain from base to collector is equal to β times the ratio of the total resistance in the collector to the total resistance in the base. The factor β appears because it is the ratio of the collector current to the base current. This general and useful expression has no counterpart in the MOS case. We observe that the overall voltage gain G_v is lower than the value without R_e, namely,

$$G_v = -\beta \frac{R_C \parallel R_L}{R_{\text{sig}} + (\beta+1) r_e} \tag{7.114}$$

because of the additional term $(\beta+1)R_e$ in the denominator. The gain, however, is now less sensitive to the value of β, a desirable result because of the typical wide variability in the value of β.

Another important consequence of including the resistance R_e in the emitter is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion. This is because only a fraction of the input signal at the base, v_i, appears between the base and the emitter. Specifically, from the circuit in Fig. 7.38(b), we see that

$$\frac{v_\pi}{v_i} = \frac{r_e}{r_e + R_e} \simeq \frac{1}{1 + g_m R_e} \tag{7.115}$$

Thus, for the same v_π, the signal at the input terminal of the amplifier, v_i, can be greater than for the CE amplifier by the factor $(1+g_m R_e)$.

To summarize, including a resistance R_e in the emitter of the CE amplifier results in the following characteristics:

1. The input resistance R_{in} is increased by the factor $(1+g_m R_e)$.
2. The voltage gain from base to collector, A_v, is reduced by the factor $(1+g_m R_e)$.
3. For the same nonlinear distortion, the input signal v_i can be increased by the factor $(1+g_m R_e)$.
4. The overall voltage gain is less dependent on the value of β.
5. The high-frequency response is significantly improved (as we shall see in Chapter 10).

With the exception of gain reduction, these characteristics represent performance improvements. Indeed, the reduction in gain is the price paid for obtaining the other performance improvements. In many cases this is a good bargain; it is the underlying philosophy for the use of negative feedback. That the resistance R_e introduces negative feedback in the amplifier circuit can be verified by utilizing a procedure similar to that we used above for the MOSFET case. In Chapter 11, where we shall study negative feedback formally, we will find that the factor $(1+g_m R_e)$, which appears repeatedly, is the "amount of negative feedback" introduced by R_e. Finally, we note that the negative-feedback action of R_e gives it the name **emitter degeneration resistance**.

Example 7.9

For the CE amplifier specified in Example 7.8, what value of R_e is needed to raise R_{in} to a value four times that of R_{sig}? With R_e included, find A_{vo}, R_o, A_v, and G_v. Also, if $\hat{v}_\pi$ is limited to 5 mV, what are the corresponding values of $\hat{v}_{sig}$ and $\hat{v}_o$?

Solution

To obtain $R_{in} = 4R_{sig} = 4 \times 5 = 20\ \text{k}\Omega$, the required R_e is found from

$$20 = (\beta + 1)(r_e + R_e)$$

With $\beta = 100$,

$$r_e + R_e \simeq 200\ \Omega$$

Thus,

$$\begin{aligned}
R_e &= 200 - 25 = 175\ \Omega \\
A_{vo} &= -\alpha \frac{R_C}{r_e + R_e} \\
&\simeq -\frac{5000}{25 + 175} = -25\ \text{V/V} \\
R_o &= R_C = 5\ \text{k}\Omega\ \text{(unchanged)} \\
A_v &= A_{vo} \frac{R_L}{R_L + R_o} = -25 \times \frac{5}{5+5} = -12.5\ \text{V/V} \\
G_v &= \frac{R_{in}}{R_{in} + R_{sig}} A_v = -\frac{20}{20+5} \times 12.5 = -10\ \text{V/V}
\end{aligned}$$

For $\hat{v}_\pi = 5$ mV,

$$\begin{aligned}
\hat{v}_i &= \hat{v}_\pi \left(\frac{r_e + R_e}{r_e} \right) \\
&= 5\left(1 + \frac{175}{25}\right) = 40\ \text{mV} \\
\hat{v}_{sig} &= \hat{v}_i \frac{R_{in} + R_{sig}}{R_{in}} \\
&= 40\left(1 + \frac{5}{20}\right) = 50\ \text{mV} \\
\hat{v}_o &= \hat{v}_{sig} \times |G_v| \\
&= 50 \times 10 = 500\ \text{mV} = 0.5\ \text{V}
\end{aligned}$$

Thus, while $|G_v|$ has decreased to about a third of its original value, the amplifier is able to produce as large an output signal as before for the same nonlinear distortion.

EXERCISE

7.24 Show that with R_e included, and v_π limited to a maximum value $\hat{v}_\pi$, the maximum allowable input signal, $\hat{v}_{sig}$, is given by

$$\hat{v}_{sig} = \hat{v}_\pi \left(1 + \frac{R_e}{r_e} + \frac{R_{sig}}{r_\pi}\right)$$

If the transistor is biased at $I_C = 0.5$ mA and has a β of 100, what value of R_e is needed to permit an input signal $\hat{v}_{sig}$ of 100 mV from a source with a resistance $R_{sig} = 10\,\text{k}\Omega$ while limiting $\hat{v}_\pi$ to 10 mV? What is R_{in} for this amplifier? If the total resistance in the collector is 10 kΩ, what G_v value results?
Ans. 350 Ω; 40.4 kΩ; −19.8 V/V

7.3.5 The Common-Gate (CG) and the Common-Base (CB) Amplifiers

Figure 7.39(a) shows a common-gate amplifier with the biasing circuit omitted. The amplifier is fed with a signal source characterized by v_{sig} and R_{sig}. Since R_{sig} appears in series with the source, it is more convenient to represent the transistor with the T model than with the π model. Doing this, we obtain the amplifier equivalent circuit shown in Fig. 7.39(b).

From inspection of the equivalent circuit of Fig. 7.39(b), we see that the input resistance

$$R_{in} = \frac{1}{g_m} \tag{7.116}$$

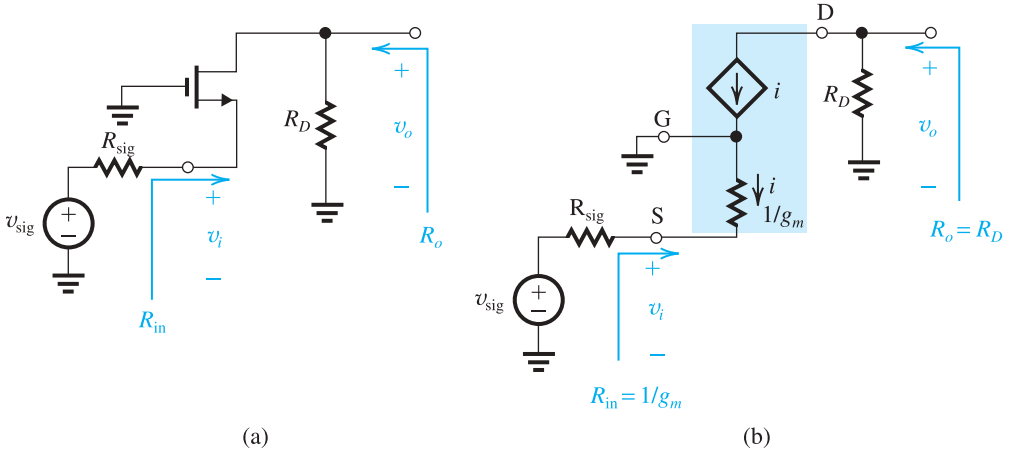


Figure 7.39 **(a)** Common-gate (CG) amplifier with bias arrangement omitted. **(b)** Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.

This should have been expected, since we are looking into the source and the gate is grounded. Typically $1/g_m$ is a few hundred ohms; thus the CG amplifier has a low input resistance.

To determine the voltage gain A_{vo}, we write at the drain node

$$v_o = -iR_D$$

and substitute for the source current i from

$$i = -\frac{v_i}{1/g_m}$$

to obtain

$$A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D \tag{7.117}$$

which except for the positive sign is identical to the expression for A_{vo} of the CS amplifier.

The output resistance of the CG circuit can be found by inspection of the circuit in Fig. 7.39(b) as

$$R_o = R_D \tag{7.118}$$

which is the same as in the case of the CS amplifier.

Although the gain of the CG amplifier proper has the same magnitude as that of the CS amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CG amplifier can cause the input signal to be severely attenuated. Specifically,

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} = \frac{1/g_m}{1/g_m + R_{\text{sig}}} \tag{7.119}$$

from which we see that except for situations in which R_{sig} is on the order of $1/g_m$, the signal transmission factor v_i/v_{sig} can be very small and the overall voltage gain G_v can be correspondingly small. Specifically, with a resistance R_L connected at the output

$$G_v = \frac{1/g_m}{R_{\text{sig}} + 1/g_m}[g_m(R_D \parallel R_L)]$$

Thus,

$$G_v = \frac{(R_D \parallel R_L)}{R_{\text{sig}} + 1/g_m} \tag{7.120}$$

Observe that *the overall voltage gain is simply the ratio of the total resistance in the drain circuit to the total resistance in the source circuit*. If R_{sig} is of the same order as R_D and R_L, G_v will be very small.

Because of its low input resistance, the CG amplifier alone has very limited application. One such application is to amplify high-frequency signals that come from sources with relatively low resistances. These include cables, where it is usually necessary for the input resistance of the amplifier to match the characteristic resistance of the cable. As will be shown in Chapter 10, the CG amplifier has excellent high-frequency response. Thus it can be combined with the CS amplifier in a very beneficial way that takes advantage of the best features of each of the two configurations. A very significant circuit of this kind will be studied in Chapter 8.

EXERCISE

7.25 A CG amplifier is required to match a signal source with $R_{sig} = 100\ \Omega$. At what current I_D should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 kΩ, what overall voltage gain is realized?
Ans. 1 mA; 10 V/V

Very similar results can be obtained for the CB amplifier shown in Fig. 7.40(a). Specifically, from the equivalent circuit in Fig. 7.40(b) we can find

$$R_{in} = r_e = \frac{\alpha}{g_m} \simeq 1/g_m \tag{7.121}$$

$$A_{vo} = \frac{\alpha}{r_e} R_C = g_m R_C \tag{7.122}$$

$$R_o = R_C \tag{7.123}$$

and with a load resistance R_L connected to the output, the overall voltage gain is given by

$$G_v \equiv \frac{v_o}{v_{sig}} = \alpha \frac{R_C \| R_L}{R_{sig} + r_e} \tag{7.124}$$

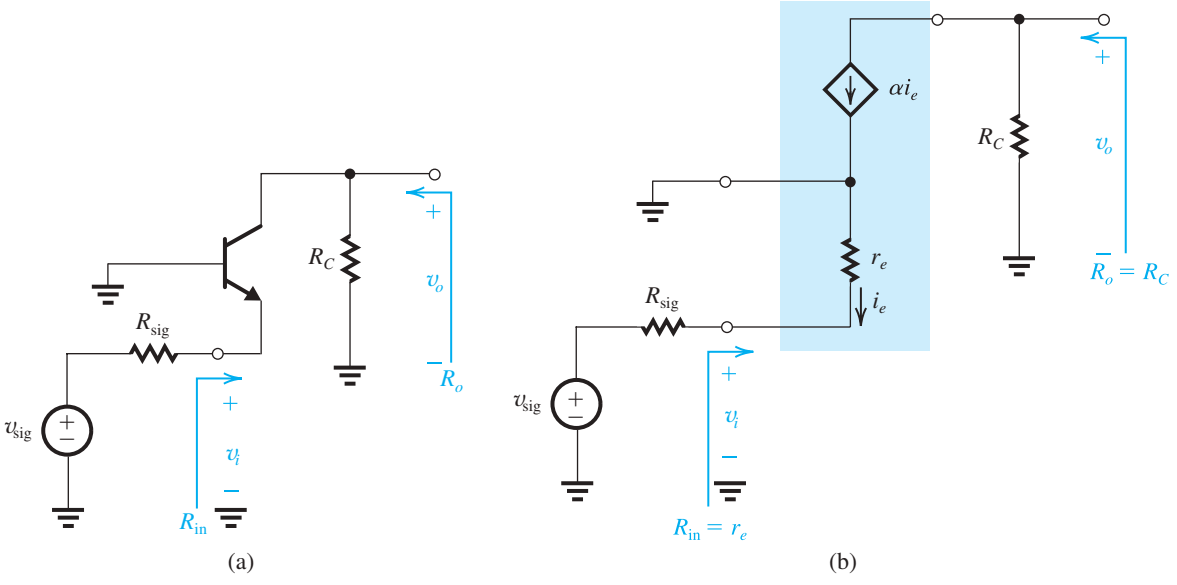


Figure 7.40 (**a**) CB amplifier with bias details omitted; (**b**) amplifier equivalent circuit with the BJT represented by its T model.

Since $\alpha \simeq 1$, we see that as in the case of the CG amplifier, the overall voltage gain is simply the ratio of the total resistance in the collector to the total resistance in the emitter. We also note that the overall voltage gain is almost independent of the value of β (except through the small dependence of α on β), a desirable property. Observe that for R_{sig} of the same order as R_C and R_L, the gain will be very small.

In summary, the CB and CG amplifiers exhibit a very low input resistance ($1/g_m$), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE (CG) amplifier ($g_m R_C$ or $g_m R_D$), and, like the CE (CS) amplifier, a relatively high output resistance (R_C or R_D). Because of its very low input resistance, the CB (CG) circuit *alone* is not attractive as a voltage amplifier except in specialized applications, such as the cable amplifier mentioned above. The CB (CG) amplifier has excellent high-frequency performance, which as we shall see in Chapters 8 and 10, makes it useful in combination with other circuits in the implementation of high-frequency amplifiers.

EXERCISES

7.26 Consider a CB amplifier utilizing a BJT biased at $I_C = 1$ mA and with $R_C = 5$ kΩ. Determine R_{in}, A_{vo}, and R_o. If the amplifier is loaded in $R_L = 5$ kΩ, what value of A_v results? What G_v is obtained if $R_{sig} = 5$ kΩ?
Ans. 25 Ω; 200 V/V; 5 kΩ; 100 V/V; 0.5 V/V

7.27 A CB amplifier is required to amplify a signal delivered by a coaxial cable having a characteristic resistance of 50 Ω. What bias current I_C should be utilized to obtain R_{in} that is matched to the cable resistance? To obtain an overall voltage gain of G_v of 40 V/V, what should the total resistance in the collector (i.e., $R_C \| R_L$) be?
Ans. 0.5 mA; 4 kΩ

7.3.6 The Source and Emitter Followers

The last of the basic transistor amplifier configurations is the common-drain (common-collector) amplifier, an important circuit that finds application in the design of both small-signal amplifiers and amplifiers that are required to handle large signals and deliver substantial amounts of signal power to a load. This latter variety will be studied in Chapter 12. The common-drain amplifier is more commonly known as the *source follower*, and the common-collector amplifier is more commonly known as the *emitter follower*. The reason behind these names will become apparent shortly.

The Need for Voltage Buffers Before embarking on the analysis of the source and the emitter followers, it is useful to look at one of their more common applications. Consider the situation depicted in Fig. 7.41(a). A signal source delivering a signal of reasonable strength (1 V) with an internal resistance of 1 MΩ is to be connected to a 1-kΩ load resistance. Connecting the source to the load directly as in Fig. 7.41(b) would result in severe attenuation

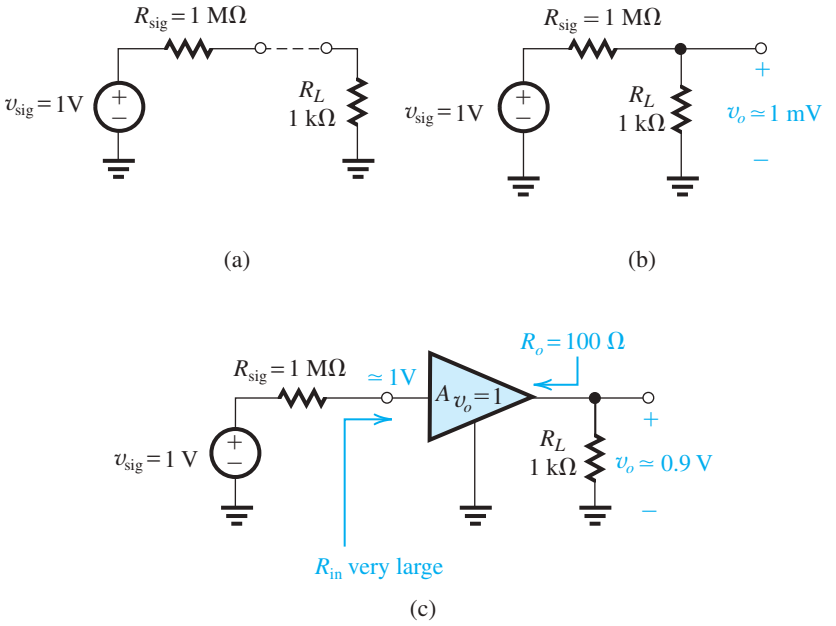


Figure 7.41 Illustrating the need for a unity-gain voltage buffer amplifier.

of the signal; the signal appearing across the load will be only $1/(1000 + 1)$ of the input signal, or about 1 mV. An alternative course of action is suggested in Fig. 7.41(c). Here we have interposed an amplifier between the source and the load. Our amplifier, however, is unlike the amplifiers we have been studying in this chapter thus far; it has a voltage gain of only unity. This is because our signal is already of sufficient strength and we do not need to increase its amplitude. Note, however, that our amplifier has a very high input resistance, thus almost all of v_{sig} (i.e., 1 V) will appear at the input of the amplifier proper. Since the amplifier has a low output resistance (100 Ω), 90% of this signal (0.9 V) will appear at the output, obviously a very significant improvement over the situation without the amplifier. As will be seen next, the source follower can easily implement the unity-gain buffer amplifier shown in Fig. 7.41(c).

Characteristic Parameters of the Source Follower Figure 7.42(a) shows a source follower with the bias circuit omitted. The source follower is fed with a signal generator (v_{sig}, R_{sig}) and has a load resistance R_L connected between the source terminal and ground. We shall assume that R_L includes both the actual load and any other resistance that may be present between the source terminal and ground (e.g., for biasing purposes). Normally, the actual load resistance would be much lower in value than such other resistances and thus would dominate.

Since the MOSFET has a resistance R_L connected in its source terminal, it is most convenient to use the T model, as shown in Fig. 7.40(b). From the latter circuit we can write by inspection

$$R_{in} = \infty$$

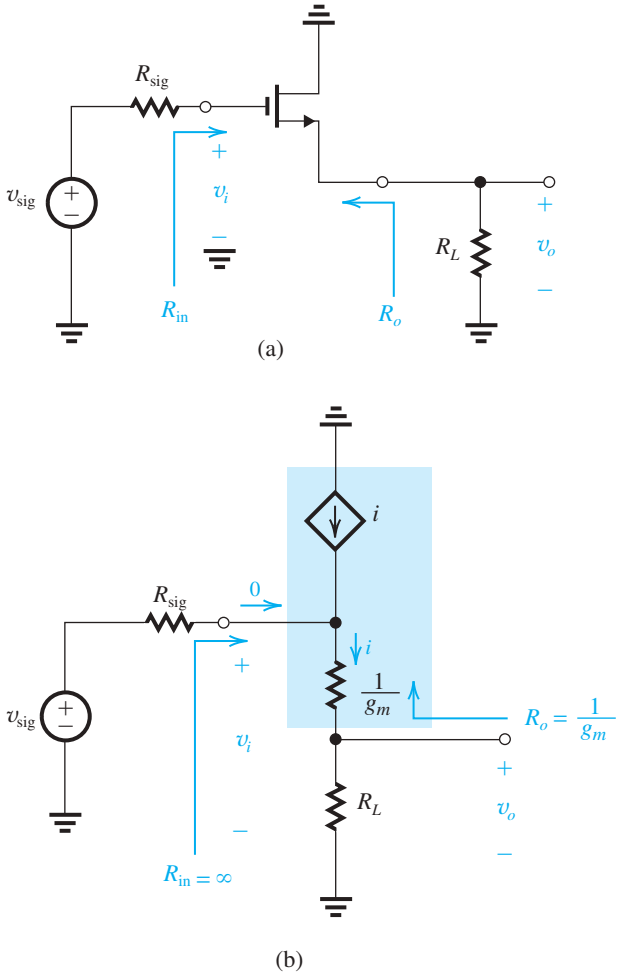


Figure 7.42 **(a)** Common-drain amplifier or source follower with the bias circuit omitted. **(b)** Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model.

and obtain A_v from the voltage divider formed by $1/g_m$ and R_L as

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} \tag{7.125}$$

Setting $R_L = \infty$ we obtain

$$A_{vo} = 1 \tag{7.126}$$

The output resistance R_o is found by setting $v_i = 0$ (i.e., by grounding the gate). Now looking back into the output terminal, excluding R_L, we simply see $1/g_m$, thus

$$R_o = 1/g_m \tag{7.127}$$

The unity open-circuit voltage gain together with R_o in Eq. (7.127) can be used to find A_v when a load resistance R_L is connected. The result is simply the expression in Eq. (7.125).

Finally, because of the infinite R_{in}, $v_i = v_{sig}$, and the overall voltage gain is

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m} \tag{7.128}$$

Thus G_v will be lower than unity. However, because $1/g_m$ is usually low, the voltage gain can be close to unity. The unity open-circuit voltage gain in Eq. (7.126) indicates that the voltage at the source terminal will follow that at the input, hence the name *source follower*.

In conclusion, the source follower features a very high input resistance (ideally, infinite), a relatively low output resistance ($1/g_m$), and an open-circuit voltage gain that is near unity (ideally, unity). Thus the source follower is ideally suited for implementing the unity-gain voltage buffer of Fig. 7.41(c). The source follower is also used as the output (i.e., last) stage in a multistage amplifier, where its function is to equip the overall amplifier with a low output resistance, thus enabling it to supply relatively large load currents without loss of gain (i.e., with little reduction of output signal level). The design of output stages is studied in Chapter 12.

EXERCISES

D7.28 It is required to design a source follower that implements the buffer amplifier shown in Fig. 7.41(c). If the MOSFET is operated with an overdrive voltage $V_{OV} = 0.25$ V, at what drain current should it be biased? Find the output signal amplitude and the signal amplitude between gate and source.
Ans. 1.25 mA; 0.91 V; 91 mV

D7.29 A MOSFET is connected in the source-follower configuration and employed as the output stage of a cascade amplifier. It is required to provide an output resistance of 200 Ω. If the MOSFET has $k_n' = 0.4$ mA/V^2 and is operated at $V_{OV} = 0.25$ V, find the required W/L ratio. Also specify the dc bias current I_D. If the amplifier load resistance varies over the range 1 kΩ to 10 kΩ, what is the range of G_v of the source follower?
Ans. 50; 0.625 mA; 0.83 V/V to 0.98 V/V

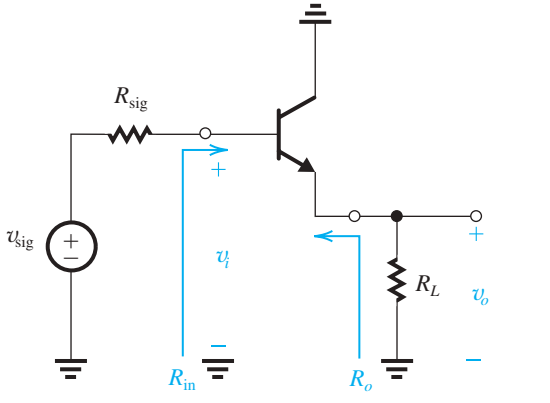
Characteristic Parameters of the Emitter Follower Although the emitter follower does not have an infinite input resistance (as in the case of the source follower), it is still widely used as a voltage buffer. In fact, it is a very versatile and popular circuit. We will therefore study it in some detail.

Figure 7.43(a) shows an emitter follower with the equivalent circuit shown in Fig. 7.43(b). The input resistance R_{in} is found from

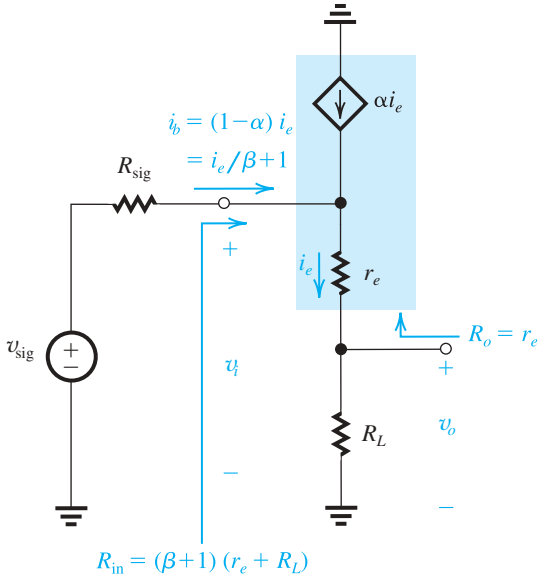
$$R_{in} = \frac{v_i}{i_b}$$

Substituting for $i_b = i_e/(\beta + 1)$ where i_e is given by

$$i_e = \frac{v_i}{r_e + R_L}$$



(a)



(b)

Figure 7.43 (**a**) Common-collector amplifier or emitter follower with the bias circuit omitted. (**b**) Equivalent circuit obtained by replacing the BJT with its T model.

we obtain

$$R_{in} = (\beta + 1)(r_e + R_L) \tag{7.129}$$

a result that we could have written directly, utilizing the resistance-reflection rule. Note that as expected the emitter follower takes the low load resistance and reflects it to the base side, where the signal source is, after increasing its value by a factor $(\beta + 1)$. It is this impedance transformation property of the emitter follower that makes it useful in

connecting a low-resistance load to a high-resistance source, that is, to implement a buffer amplifier.

The voltage gain A_v is given by

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + r_e} \tag{7.130}$$

Setting $R_L = \infty$ yields A_{vo},

$$A_{vo} = 1 \tag{7.131}$$

Thus, as expected, the open-circuit voltage gain of the emitter follower proper is unity, which means that the signal voltage at the emitter *follows* that at the base, which is the origin of the name "emitter follower."

To determine R_o, refer to Fig. 7.43(b) and look back into the emitter (i.e., behind or excluding R_L) while setting $v_i = 0$ (i.e., grounding the base). You will see r_e of the BJT, thus

$$R_o = r_e \tag{7.132}$$

This result together with $A_{vo} = 1$ yields A_v in Eq. (7.130), thus confirming our earlier analysis.

We next determine the overall voltage gain G_v, as follows:

$$\begin{aligned} \frac{v_i}{v_{\text{sig}}} &= \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \\ &= \frac{(\beta+1)(r_e + R_L)}{(\beta+1)(r_e + R_L) + R_{\text{sig}}} \\ G_v \equiv \frac{v_o}{v_{\text{sig}}} &= \frac{v_i}{v_{\text{sig}}} \times A_v \end{aligned}$$

Substituting for A_v from Eq. (7.130) results in

$$G_v = \frac{(\beta+1)R_L}{(\beta+1)R_L + (\beta+1)r_e + R_{\text{sig}}} \tag{7.133}$$

This equation indicates that the overall gain, though lower than one, can be close to one if $(\beta+1)R_L$ is larger or comparable in value to R_{sig}. This again confirms the action of the emitter follower in delivering a large proportion of v_{sig} to a low-valued load resistance R_L even though R_{sig} can be much larger than R_L. The key point is that R_L is multiplied by $(\beta+1)$ before it is "presented to the source." Figure 7.44(a) shows an equivalent circuit of the emitter follower obtained by simply reflecting r_e and R_L to the base side. The overall voltage gain $G_v \equiv v_o/v_{\text{sig}}$ can be determined directly and very simply from this circuit by using the voltage divider rule. The result is the expression for G_v already given in Eq. (7.133).

Dividing all resistances in the circuit of Fig. 7.44(a) by $\beta + 1$ does not change the voltage ratio v_o/v_{sig}. Thus we obtain another equivalent circuit, shown in Fig. 7.44(b), that can be used to determine $G_v \equiv v_o/v_{\text{sig}}$ of the emitter follower. A glance at this circuit reveals that it is simply the equivalent circuit obtained by reflecting v_{sig} and R_{sig} from the base side to the emitter side. In this reflection, v_{sig} does not change, but R_{sig} is divided by $\beta + 1$. Thus, we

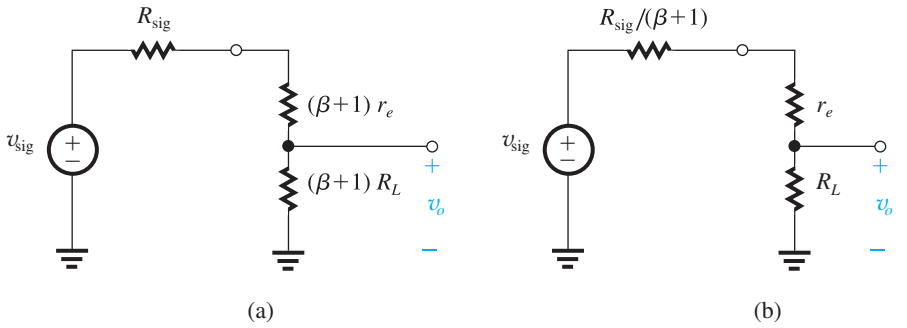


Figure 7.44 Simple equivalent circuits for the emitter follower obtained by (**a**) reflecting r_e and R_L to the base side, and (**b**) reflecting v_{sig} and R_{sig} to the emitter side. Note that the circuit in (**b**) can be obtained from that in (**a**) by simply dividing all resistances by $(\beta + 1)$.

either reflect to the base side and obtain the circuit in Fig. 7.44(a) or reflect to the emitter side and obtain the circuit in Fig. 7.44(b). From the latter, G_v can be found as

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + r_e + R_{sig}/(\beta + 1)} \tag{7.134}$$

Observe that this expression is the same as that in Eq. (7.133) except for dividing both the numerator and denominator by $\beta + 1$.

The expression for G_v in Eq. (7.134) has an interesting interpretation: The emitter follower reduces R_{sig} by the factor $(\beta + 1)$ before "presenting it to the load resistance R_L" : an impedance transformation that has the same buffering effect.

At this point it is important to note that although the emitter follower does not provide voltage gain it has a current gain of $\beta + 1$.

Thévenin Representation of the Emitter-Follower Output A more general representation of the emitter-follower output is shown in Fig. 7.45(a). Here G_{vo} is the overall open-circuit voltage gain that can be obtained by setting $R_L = \infty$ in the circuit of Fig. 7.44(b), as illustrated in Fig. 7.45(b). The result is $G_{vo} = 1$. The output resistance R_{out} is *different* from R_o. To determine R_{out} we set v_{sig} to zero (rather than setting v_i to zero). Again we can use the equivalent circuit in Fig. 7.44(b) to do this, as illustrated in Fig. 7.45(c). We see that

$$R_{out} = r_e + \frac{R_{sig}}{\beta + 1} \tag{7.135}$$

Finally, we show in Fig. 7.45(d) the emitter-follower circuit together with its R_{in} and R_{out}. Observe that R_{in} is determined by reflecting r_e and R_L to the base side (by multiplying their values by $\beta + 1$). To determine R_{out}, grab hold of the emitter and walk (or just look!) backward while $v_{sig} = 0$. You will see r_e in series with R_{sig}, which because it is in the base must be divided by $(\beta + 1)$.

We note that unlike the amplifier circuits we studied earlier, the emitter follower is *not* unilateral. This is manifested by the fact that R_{in} depends on R_L and R_{out} depends on R_{sig}.

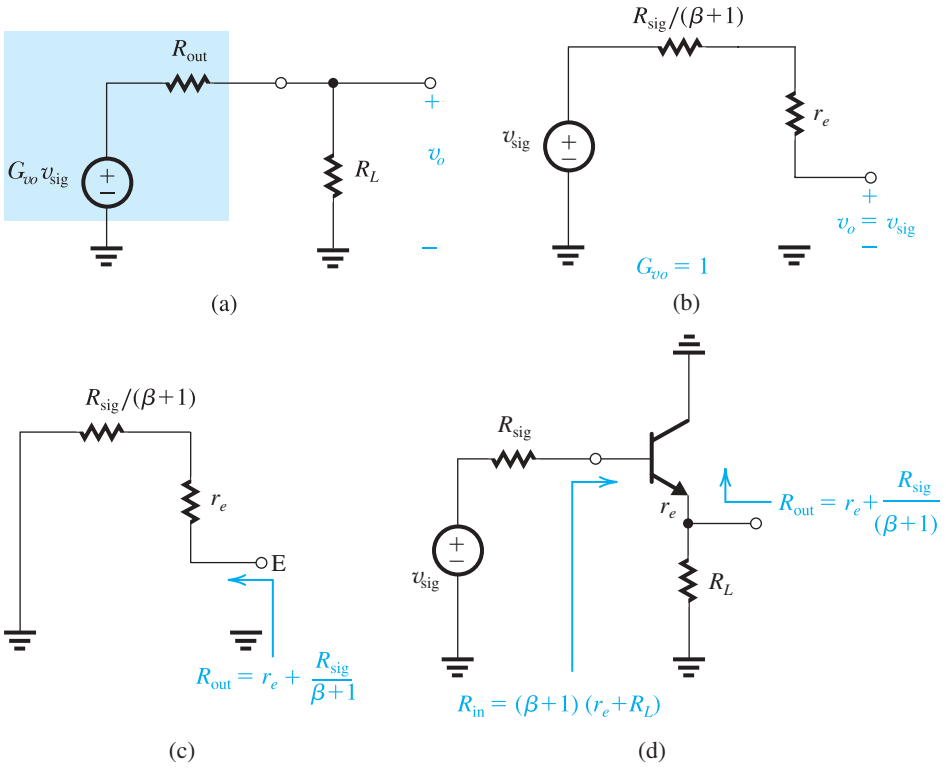


Figure 7.45 (**a**) Thévenin representation of the output of the emitter follower. (**b**) Obtaining G_{vo} from the equivalent circuit in Fig. 7.44(b). (**c**) Obtaining R_{out} from the equivalent circuit in Fig. 7.44(b) with v_{sig} set to zero. (**d**) The emitter follower with R_{in} and R_{out} determined simply by looking into the input and output terminals, respectively.

Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{sig} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 kΩ, and to 0.5 kΩ.

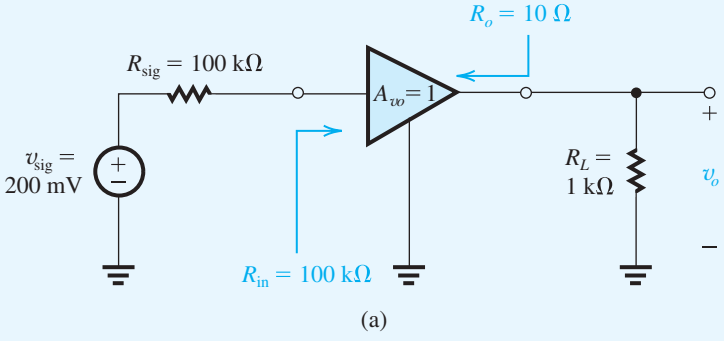
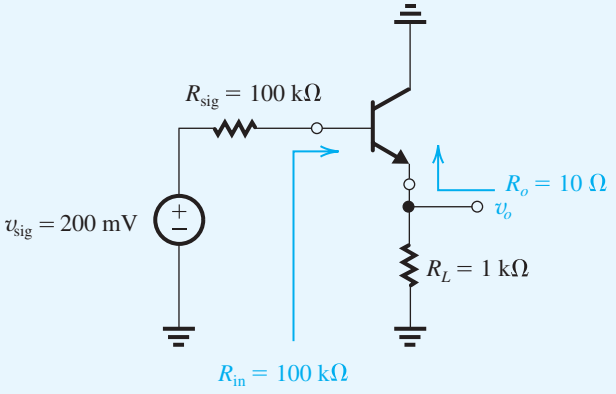


Figure 7.46 Circuit for Example 7.10.

Example 7.10 *continued*



(b)

Figure 7.46 *continued*

Solution

The emitter-follower circuit is shown in Fig. 7.46(b). To obtain $R_o = 10\ \Omega$, we bias the transistor to obtain $r_e = 10\ \Omega$. Thus,

$$10\ \Omega = \frac{V_T}{I_E}$$
$$I_E = 2.5\ \text{mA}$$

The input resistance R_{in} will be

$$R_{in} = (\beta + 1)(r_e + R_L)$$
$$100 = (\beta + 1)(0.01 + 1)$$

Thus, the BJT should have a β with a minimum value of 98. A higher β would obviously be beneficial.

The overall voltage gain can be determined from

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + r_e + \dfrac{R_{sig}}{(\beta + 1)}}$$

Assuming $\beta = 100$, the value of G_v obtained is

$$G_v = 0.5$$

Thus when $v_{sig} = 200$ mV, the signal at the output will be 100 mV. Since the 100 mV appears across the 1-kΩ load, the signal across the base–emitter junction can be found from

$$v_\pi = \frac{v_o}{R_L} \times r_e$$
$$= \frac{100}{1000} \times 10 = 1 \text{ mV}$$

If $\hat{v}_\pi = 5$ mV then v_{sig} can be increased by a factor of 5, resulting in $\hat{v}_{sig} = 1$ V.

To obtain v_o as the load is varied, we use the Thévenin equivalent of the emitter follower, shown in Fig. 7.45(a) with $G_{vo} = 1$ and

$$R_{out} = \frac{R_{sig}}{\beta + 1} + r_e = \frac{100}{101} + 0.01 = 1 \text{ k}\Omega$$

to obtain

$$v_o = v_{sig} \frac{R_L}{R_L + R_{out}}$$

For $R_L = 2$ kΩ,

$$v_o = 200 \text{ mV} \times \frac{2}{2+1} = 133.3 \text{ mV}$$

and for $R_L = 0.5$ kΩ,

$$v_o = 200 \text{ mV} \times \frac{0.5}{0.5+1} = 66.7 \text{ mV}$$

EXERCISE

7.30 An emitter follower utilizes a transistor with $\beta = 100$ and is biased at $I_C = 5$ mA. It operates between a source having a resistance of 10 kΩ and a load of 1 kΩ. Find R_{in}, G_{vo}, R_{out}, and G_v. What is the peak amplitude of v_{sig} that results in v_π having a peak amplitude of 5 mV? Find the resulting peak amplitude at the output.

Ans. 101.5 kΩ; 1 V/V; 104 Ω; 0.91 V/V; 1.1 V; 1 V

7.3.7 Summary Tables and Comparisons

For easy reference and to enable comparisons, we present in Tables 7.4 and 7.5 the formulas for determining the characteristic parameters for the various configurations of MOSFET and BJT amplifiers, respectively. In addition to the remarks made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

1. MOS amplifiers provide much higher, ideally infinite input resistances (except, of course, for the CG configuration). This is a definite advantage over BJT amplifiers.
2. BJTs exhibit higher g_m values than MOSFETs, resulting in higher gains.
3. For discrete-circuit amplifiers—that is, those that are assembled from discrete components on a printed-circuit board (PCB)—the BJT remains the device of choice. This is because discrete BJTs are much easier to handle physically than discrete MOSFETs and, more important, a very wide variety of discrete BJTs is available commercially. The remainder of this chapter is concerned with discrete-circuit amplifiers.
4. Integrated-circuit (IC) amplifiers predominantly use MOSFETs, although BJTs are utilized in certain niche areas. Chapters 8 to 13 are mainly concerned with IC amplifiers.
5. The CS and CE configurations are the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
6. Including a resistance R_s in the source of the CS amplifier (a resistance R_e in the emitter of the CE amplifier) provides a number of performance improvements at the expense of gain reduction.

Table 7.4 Characteristics of MOSFET Amplifiers

	Characteristics[a]				
Amplifier type	R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 7.35)	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s (Fig. 7.37)	∞	$-\dfrac{g_m R_D}{1+g_m R_s}$	R_D	$\dfrac{-g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$	$-\dfrac{g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\dfrac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 7.39)	$\dfrac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\dfrac{R_D \parallel R_L}{R_{\text{sig}} + 1/g_m}$
Source follower (Fig. 7.42)	∞	1	$\dfrac{1}{g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$	$\dfrac{R_L}{R_L + 1/g_m}$

[a] For the interpretation of R_{in}, A_{vo}, and R_o, refer to Fig. 7.34(b).

Table 7.5 Characteristics of BJT Amplifiers[a,b]

	R_{in}	A_{vo}	R_o	A_v	G_v
Common emitter (Fig. 7.36)	$(\beta+1)r_e$	$-g_m R_C$	R_C	$-g_m(R_C \parallel R_L)$ $-\alpha\dfrac{R_C \parallel R_L}{r_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{sig}+(\beta+1)r_e}$
Common emitter with R_e (Fig. 7.38)	$(\beta+1)(r_e+R_e)$	$-\dfrac{g_m R_C}{1+g_m R_e}$	R_C	$\dfrac{-g_m(R_C \parallel R_L)}{1+g_m R_e}$ $-\alpha\dfrac{R_C \parallel R_L}{r_e+R_e}$	$-\beta\dfrac{R_C \parallel R_L}{R_{sig}+(\beta+1)(r_e+R_e)}$
Common base (Fig. 7.40)	r_e	$g_m R_C$	R_C	$g_m(R_C \parallel R_L)$ $\alpha\dfrac{R_C \parallel R_L}{r_e}$	$\alpha\dfrac{R_C \parallel R_L}{R_{sig}+r_e}$
Emitter follower (Fig. 7.43)	$(\beta+1)(r_e+R_L)$	1	r_e	$\dfrac{R_L}{R_L+r_e}$	$\dfrac{R_L}{R_L+r_e+R_{sig}/(\beta+1)}$ $G_{vo}=1$ $R_{out}=r_e+\dfrac{R_{sig}}{\beta+1}$

[a] For the interpretation of R_m, A_{vo}, and R_o refer to Fig. 7.34.
[b] Setting $\beta=\infty$ ($\alpha=1$) and replacing r_e with $1/g_m$, R_C with R_D, and R_e with R_s results in the corresponding formulas for MOSFET amplifiers (Table 7.4).

7. The low input resistance of the CG and CB amplifiers makes them useful only in specific applications. As we shall see in Chapter 10, these two configurations exhibit a much better high-frequency response than that available from the CS and CE amplifiers. This makes them useful as high-frequency amplifiers, especially when combined with the CS or CE circuit. We shall study one such combination in Chapter 8.
8. The source follower (emitter follower) finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load, and as the output stage in a multistage amplifier, where its purpose is to equip the amplifier with a low output resistance.

7.3.8 When and How to Include the Output Resistance r_o

So far we have been neglecting the output resistance r_o of the MOSFET and the BJT. We have done this for two reasons:

1. To keep things simple and focus attention on the significant features of each of the basic configurations, and
2. Because our main interest in this chapter is discrete-circuit design, where the circuit resistances (e.g., R_C, R_D, and R_L) are usually much smaller than r_o.

LEE DE FOREST—A FATHER OF THE ELECTRONICS AGE:

In 1906 self-employed inventor Lee de Forest (1873–1961) created a three-terminal vacuum tube; it was the first electronic amplifier of weak signals. The device was known initially as the de Forest valve. The patent filed in 1907, however, used the name Audion, with the "-ion" indicating that the device was not completely evacuated. By 1919, engineers had realized that complete evacuation of internal gases produced a more reliable device.

De Forest's first amplifier became known as the vacuum tube triode. Through its impact on radio, telephony, motion picture sound, and television, this invention, one of de Forest's 180 patents, is credited with introducing the electronics age. The vacuum tube, in a variety of types, remained the device for implementing amplifiers until the appearance of transistors in the early 1950s.

Nevertheless, in some instances it is relatively easy to include r_o in the analysis. Specifically:

1. In the CS and CE amplifiers, it can be seen that r_o of the transistor appears in parallel with R_D and R_C, respectively, and can be simply included in the corresponding formulas in Tables 7.4 and 7.5 by replacing R_D with $(R_D \| r_o)$ and R_C with $(R_C \| r_o)$. The effect will be a reduction in the magnitude of gain, of perhaps 5% to 10%.
2. In the source and emitter followers, it can be seen that the transistor r_o appears in parallel with R_L and can be taken into account by replacing R_L in the corresponding formulas with $(R_L \| r_o)$. Thus, here too, the effect of taking r_o into account is a small reduction in gain. More significant, however, taking r_o into account reduces the open-circuit voltage gain A_{vo} from unity to

$$A_{vo} = \frac{r_o}{r_o + (1/g_m)} \tag{7.136}$$

There are configurations in which taking r_o into account complicates the analysis considerably. These are the CS (CE) amplifiers with a source (emitter) resistance, and the CG (CB) amplifier. Fortunately, for discrete implementation of these configurations, the effect of neglecting r_o is usually small (which can be verified by computer simulation).

Finally, a very important point: *In the analysis and design of IC amplifiers, r_o must always be taken into account.* This is because, as will be seen in the next chapter, all the circuit resistances are of the same order of magnitude as r_o; thus, neglecting r_o can result in completely erroneous results.

7.4 Biasing

As discussed in Section 7.1, an essential step in the design of a transistor amplifier is the establishment of an appropriate dc operating point for the transistor. This is the step known as biasing or bias design. In this section, we study the biasing methods commonly employed in discrete-circuit amplifiers. Biasing of integrated-circuit amplifiers will be studied in Chapter 8.

Bias design aims to establish in the drain (collector) a dc current that is predictable and insensitive to variations in temperature and to the large variations in parameter values between devices of the same type. For instance, discrete BJTs belonging to the same manufacturer's part number can exhibit β values that range, say, from 50 to 150. Nevertheless, the bias design

for an amplifier utilizing this particular transistor type may specify that the dc collector current shall always be within, say, ±10% of the nominal value of, say, 1 mA. A similar statement can be made about the desired insensitivity of the dc drain current to the wide variations encountered in V_t of discrete MOSFETs.

A second consideration in bias design is locating the dc operating point in the active region of operation of the transistor so as to obtain high voltage gain while allowing for the required output signal swing without the transistor leaving the active region at any time (in order to avoid nonlinear distortion). We discussed this point in Section 7.1.7.

Although we shall consider the biasing of MOSFET and BJT amplifiers separately, the resulting circuits are very similar. Also, it will be seen that good bias designs incorporate a feedback mechanism that works to keep the dc bias point as constant as possible.

In order to keep matters simple and thus focus our attention on significant issues, we will neglect the Early effect; that is assume $\lambda = 0$ or $V_A = \infty$. This is certainly allowed in initial designs of discrete circuits. Of course, the design can be fine-tuned at a later point with the assistance of a circuit-simulation program such as SPICE.

7.4.1 The MOSFET Case

Biasing by Fixing V_{GS} The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required[6] to provide the desired I_D. This voltage value can be derived from the power-supply voltage V_{DD} through the use of an appropriate voltage divider, as shown in Fig. 7.47(a). Alternatively, it can be derived from another suitable reference voltage that might be available in the system. Independent of how the voltage V_{GS} may be generated, this is *not* a good approach to biasing a MOSFET. To understand the reason for this statement, recall that

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

and note that the values of the threshold voltage V_t, the oxide-capacitance C_{ox}, and (to a lesser extent) the transistor aspect ratio W/L vary widely among devices of supposedly the same size and type. This is certainly the case for discrete devices, in which large spreads in the values of these parameters occur among devices of the same manufacturer's part number. The spread can also be large in integrated circuits, especially among devices fabricated on different wafers and certainly between different batches of wafers. Furthermore, both V_t and μ_n depend on temperature, with the result that if we fix the value of V_{GS}, the drain current I_D becomes very much temperature dependent.

To emphasize the point that biasing by fixing V_{GS} is not a good technique, we show in Fig. 7.47 two i_D–v_{GS} characteristic curves representing extreme values in a batch of MOSFETs of the same type. Observe that for the fixed value of V_{GS}, the resultant spread in the values of the drain current can be substantial.

Biasing by Fixing V_G and Connecting a Resistance in the Source An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G, and connecting a resistance in the source lead, as shown in Fig. 7.48(a). For this circuit

[6]That is indeed what we were doing in Section 7.1. However, the amplifier circuits studied there were conceptual ones, not actual practical circuits. Our purpose in this section is to study the latter.

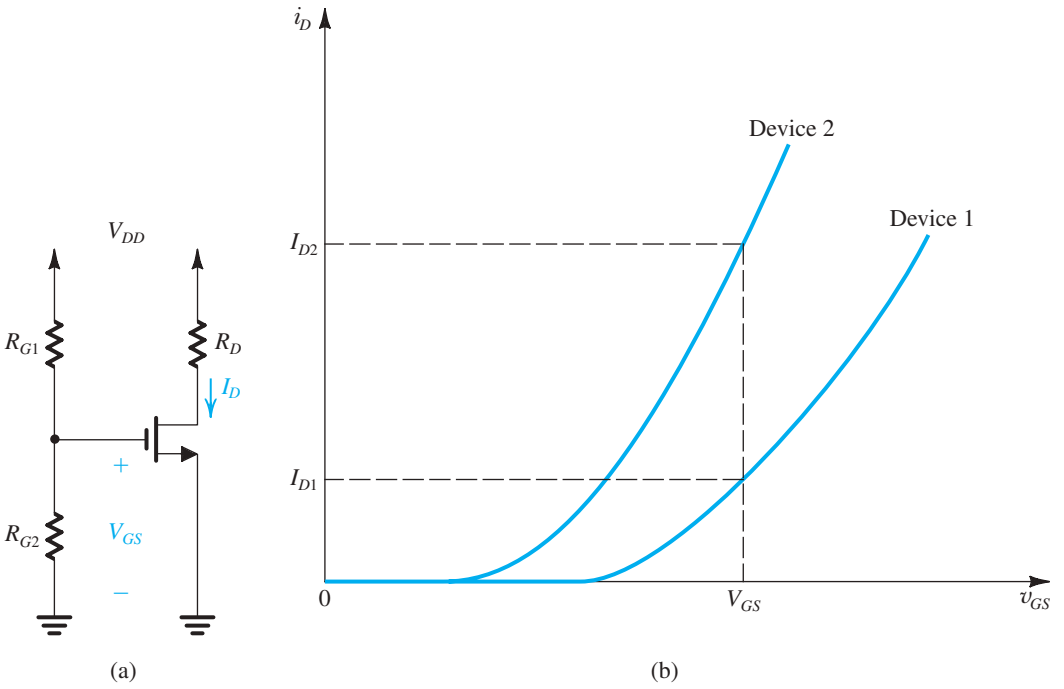


Figure 7.47 (**a**) Biasing the MOSFET with a constant V_{GS} generated from V_{DD} using a voltage divider (R_{G1},R_{G2}); (**b**) the use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

we can write

$$V_G = V_{GS} + R_S I_D \tag{7.137}$$

Now, if V_G is much greater than V_{GS}, I_D will be mostly determined by the values of V_G and R_S. However, even if V_G is not much larger than V_{GS}, resistor R_S provides *negative feedback,* which acts to stabilize the value of the bias current I_D. To see how this comes about, consider what happens when I_D increases for whatever reason. Equation (7.137) indicates that since V_G is constant, V_{GS} will have to decrease. This in turn results in a decrease in I_D, a change that is opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible.[7]

Figure 7.48(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here too we show the i_D–v_{GS} characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit—namely, Eq. (7.137). The intersection of this straight line with the i_D–v_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point. Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_S are made larger (thus providing a bias line that is less steep).

Two possible practical discrete implementations of this bias scheme are shown in Fig. 7.48(c) and (e). The circuit in Fig. 7.48(c) utilizes one power-supply V_{DD} and derives V_G

[7]The action of R_S in stabilizing the value of the bias current I_D is not unlike that of the resistance R_s, which we included in the source lead of a CS amplifier in Section 7.3.4. In the latter case also, R_s works to reduce the change in i_D with the result that the amplifier gain is reduced.

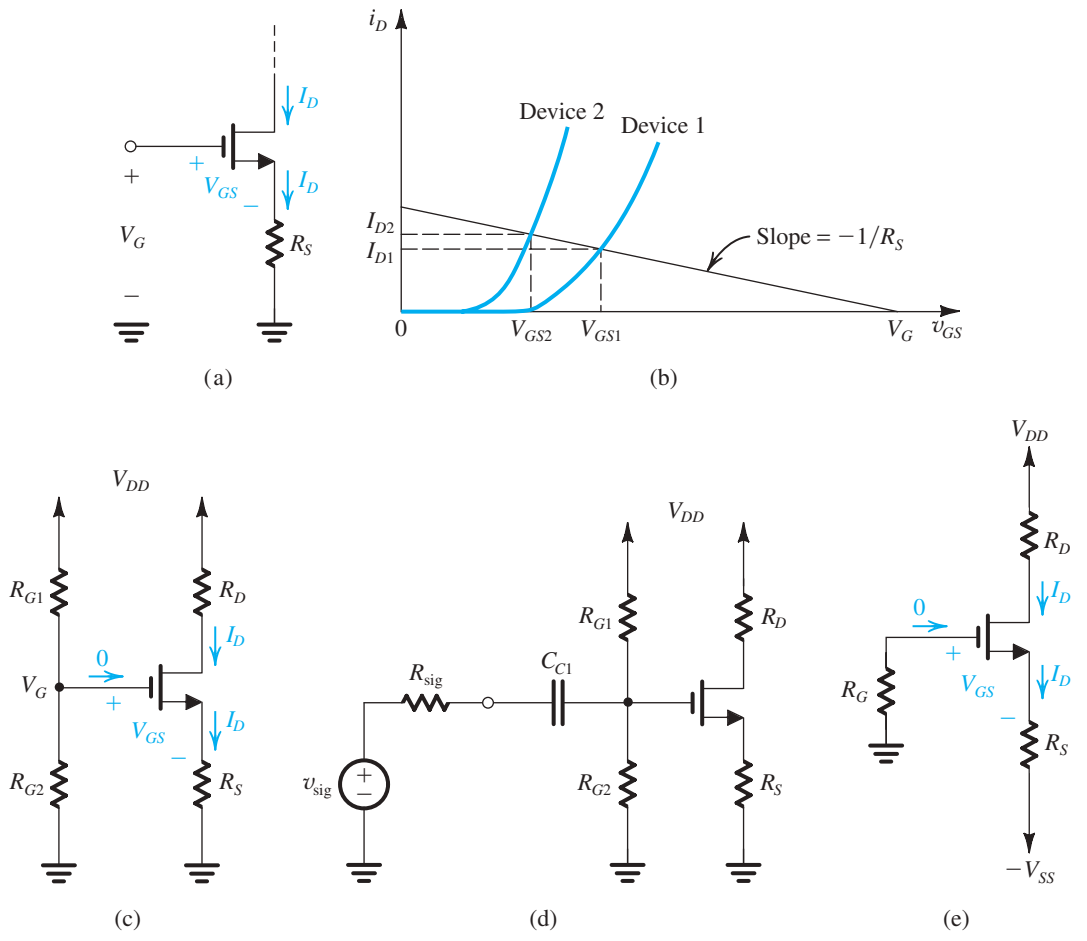


Figure 7.48 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

through a voltage divider (R_{G1}, R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the megohm range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor, as shown in Fig. 7.48(d). Here capacitor C_{C1} blocks dc and thus allows us to couple the signal v_{sig} to the amplifier input without disturbing the MOSFET dc bias point. The value of C_{C1} should be selected large enough to approximate a short circuit at all signal frequencies of interest. We shall study capacitively coupled MOSFET amplifiers, which are suitable only in discrete-circuit design, in Section 7.5. Finally, note that in the circuit of Fig. 7.48(c), resistor R_D is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, as is often the case, the somewhat simpler bias arrangement of Fig. 7.48(e) can be utilized. This circuit is an implementation of Eq. (7.137), with V_G replaced by V_{SS}. Resistor R_G establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

Example 7.11

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n'W/L = 1$ mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'W/L$ but $V_t = 1.5$ V.

Solution

As a rule of thumb for designing this classical biasing circuit, we choose R_D and R_S to provide one-third of the power-supply voltage V_{DD} as a drop across each of R_D, the transistor (i.e., V_{DS}), and R_S. For $V_{DD} = 15$ V, this choice makes $V_D = +10$ V and $V_S = +5$ V. Now, since I_D is required to be 0.5 mA, we can find the values of R_D and R_S as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10\ \text{k}\Omega$$

$$R_S = \frac{V_S}{R_S} = \frac{5}{0.5} = 10\ \text{k}\Omega$$

The required value of V_{GS} can be determined by first calculating the overdrive voltage V_{OV} from

$$I_D = \frac{1}{2}k_n'(W/L)V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

which yields $V_{OV} = 1$ V, and thus,

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2\ \text{V}$$

Now, since $V_S = +5$ V, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7\ \text{V}$$

To establish this voltage at the gate we may select $R_{G1} = 8$ MΩ and $R_{G2} = 7$ MΩ. The final circuit is shown in Fig. 7.49. Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to V_{DD}) and a negative signal swing of 4 V [i.e., down to $(V_G - V_t)$].

If the NMOS transistor is replaced with another having $V_t = 1.5$ V, the new value of I_D can be found as follows:

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \tag{7.138}$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10I_D \tag{7.139}$$

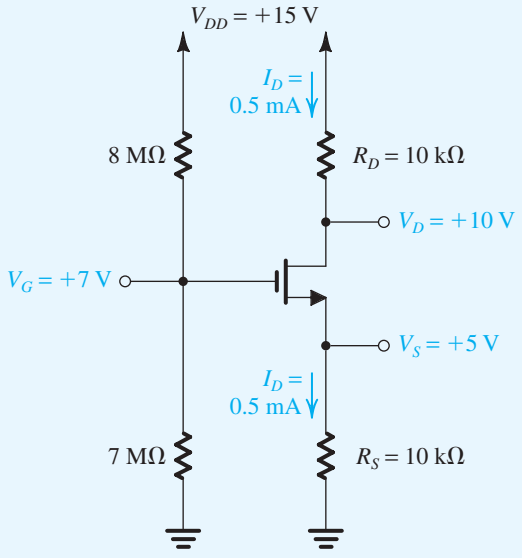


Figure 7.49 Circuit for Example 7.11.

Solving Eqs. (7.138) and (7.139) together yields

$$I_D = 0.455 \text{ mA}$$

Thus the change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is $\dfrac{-0.045}{0.5} \times 100 = -9\%$ change.

EXERCISES

7.31 Consider the MOSFET in Example 7.11 when fixed-V_{GS} bias is used. Find the required value of V_{GS} to establish a dc bias current $I_D = 0.5$ mA. Recall that the device parameters are $V_t = 1$ V, $k_n'W/L = 1$ mA/V^2, and $\lambda = 0$. What is the percentage change in I_D obtained when the transistor is replaced with another having $V_t = 1.5$ V?

Ans. $V_{GS} = 2$ V; –75%

D7.32 Design the circuit of Fig. 7.48(e) to operate at a dc drain current of 0.5 mA and $V_D = +2$ V. Let $V_t = 1$ V, $k_n'W/L = 1$ mA/V^2, $\lambda = 0$, $V_{DD} = V_{SS} = 5$ V. Use standard 5% resistor values (see Appendix J), and give the resulting values of I_D, V_D, and V_S.

Ans. $R_D = R_S = 6.2$ kΩ; $I_D = 0.49$ mA, $V_S = -1.96$ V, and $V_D = +1.96$ V. R_G can be selected in the range of 1 MΩ to 10 MΩ.

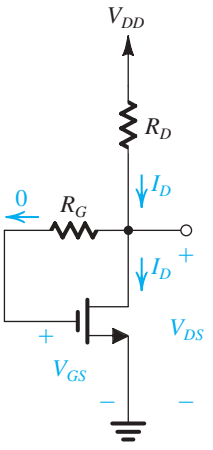


Figure 7.50 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

Biasing Using a Drain-to-Gate Feedback Resistor A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 7.50. Here the large feedback resistance R_G (usually in the megohm range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D \tag{7.140}$$

which is identical in form to Eq. (7.137), which describes the operation of the bias scheme discussed above [that in Fig. 7.48(a)]. Thus, here too, if I_D for some reason changes, say increases, then Eq. (7.140) indicates that V_{GS} must decrease. The decrease in V_{GS} in turn causes a decrease in I_D, a change that is opposite in direction to the one originally assumed. Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

The circuit of Fig. 7.50 can be utilized as an amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The amplified output signal at the drain can be coupled to another part of the circuit, again via a capacitor. We considered such an amplifier circuit in Section 7.2 (Example 7.3).

EXERCISE

D7.33 Design the circuit in Fig. 7.50 to operate at a dc drain current of 0.5 mA. Assume $V_{DD} = +5$ V, $k_n'W/L = 1$ mA/V^2, $V_t = 1$ V, and $\lambda = 0$. Use a standard 5% resistance value for R_D, and give the actual values obtained for I_D and V_D.

Ans. $R_D = 6.2\ \text{k}\Omega$; $I_D \simeq 0.49$ mA; $V_D \simeq 1.96$ V

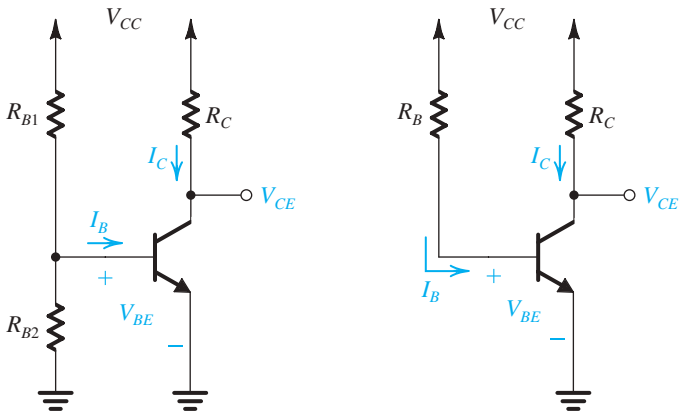


Figure 7.51 Two obvious schemes for biasing the BJT: (**a**) by fixing V_{BE}; (**b**) by fixing I_B. Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be "bad." Neither scheme is recommended.

7.4.2 The BJT Case

Before presenting the "good" biasing schemes, we should point out why two obvious arrangements are *not* good. First, attempting to bias the BJT by fixing the voltage V_{BE} by, for instance, using a voltage divider across the power supply V_{CC}, as shown in Fig. 7.51(a), is not a viable approach: The very sharp exponential relationship $i_C - v_{BE}$ means that any small and inevitable differences in V_{BE} from the desired value will result in large differences in I_C and in V_{CE}. Second, biasing the BJT by establishing a constant current in the base, as shown in Fig. 7.51(b), where $I_B \simeq (V_{CC} - 0.7)/R_B$, is also not a recommended approach. Here the typically large variations in the value of β among units of the same device type will result in correspondingly large variations in I_C and hence in V_{CE}.

The Classical Discrete-Circuit Bias Arrangement Figure 7.52(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1, R_2. In addition, a resistor R_E is connected to the emitter. This circuit is very similar to one we used for the MOSFET [Fig. 7.48(c)]. Here, however, the design must take into account the finite base current.

Figure 7.52(b) shows the same circuit with the voltage-divider network replaced by its Thévenin equivalent,

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{7.141}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{7.142}$$

The current I_E can be determined by writing a Kirchhoff loop equation for the base–emitter–ground loop, labeled L, and substituting $I_B = I_E/(\beta + 1)$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{7.143}$$

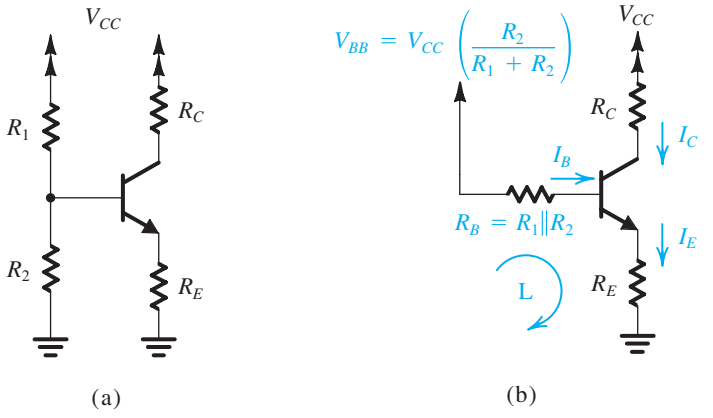


Figure 7.52 Classical biasing for BJTs using a single power supply: (**a**) circuit; (**b**) circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

To make I_E insensitive to temperature and β variation,[8] we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE} \tag{7.144}$$

$$R_E \gg \frac{R_B}{\beta + 1} \tag{7.145}$$

Condition (7.144) ensures that small variations in V_{BE} ($\simeq 0.7$ V) will be swamped by the much larger V_{BB}. There is a limit, however, on how large V_{BB} can be: For a given value of the supply voltage V_{CC}, the higher the value we use for V_{BB}, the lower will be the sum of voltages across R_C and the collector–base junction (V_{CB}). On the other hand, we want the voltage across R_C to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want V_{CB} (or V_{CE}) to be large, to provide a large signal swing (before transistor saturation). Thus, as is the case in any design, we have a set of conflicting requirements, and the solution must be a trade-off. As a rule of thumb, one designs for V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC}$, and $I_C R_C$ about $\frac{1}{3}V_{CC}$.

Condition (7.145) makes I_E insensitive to variations in β and could be satisfied by selecting R_B small. This in turn is achieved by using low values for R_1 and R_2. Lower values for R_1 and R_2, however, will mean a higher current drain from the power supply, and will result in a lowering of the input resistance of the amplifier (if the input signal is coupled to the base),[9] which is the trade-off involved in this part of the design. It should be noted that condition (7.145) means that we want to make the base voltage independent of the value of β and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$.

Further insight regarding the mechanism by which the bias arrangement of Fig. 7.52(a) stabilizes the dc emitter (and hence collector) current is obtained by considering the feedback

[8] Bias design seeks to stabilize either I_E or I_C since $I_C = \alpha I_E$ and α varies very little. That is, a stable I_E will result in an equally stable I_C, and vice versa.

[9] If the input signal is coupled to the transistor base, the two bias resistances R_1 and R_2 effectively appear in parallel between the base and ground. Thus, low values for R_1 and R_2 will result in lowering R_{in}.

action provided by R_E. Consider that for some reason the emitter current increases. The voltage drop across R_E, and hence V_E, will increase correspondingly. Now, if the base voltage is determined primarily by the voltage divider R_1, R_2, which is the case if R_B is small, it will remain constant, and the increase in V_E will result in a corresponding decrease in V_{BE}. This in turn reduces the collector (and emitter) current, a change opposite to that originally assumed. Thus R_E provides a *negative feedback* action that stabilizes the bias current. This should remind the reader of the resistance R_e that we included in the emitter lead of the CE amplifier in Section 7.3.4. Also, the feedback action of R_E in the circuit of Fig. 7.52(a) is similar to the feedback action of R_S in the circuit of Fig. 7.48(c). We shall study negative feedback formally in Chapter 11.

Example 7.12

We wish to design the bias network of the amplifier in Fig. 7.52 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.

Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across R_2 and another one-third to the voltage drop across R_C, leaving one-third for possible negative signal swing at the collector. Thus,

$$V_B = +4 \text{ V}$$
$$V_E = 4 - V_{BE} \simeq 3.3 \text{ V}$$

and R_E is determined from

$$R_E = \frac{V_E}{I_E} = \frac{3.3}{1} = 3.3 \text{ k}\Omega$$

From the discussion above we select a voltage-divider current of $0.1I_E = 0.1 \times 1 = 0.1$ mA. Neglecting the base current, we find

$$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

and

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

Thus $R_2 = 40$ kΩ and $R_1 = 80$ kΩ.

At this point, it is desirable to find a more accurate estimate for I_E, taking into account the nonzero base current. Using Eq. (7.143),

$$I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \dfrac{(80 \| 40)(\text{k}\Omega)}{101}} = 0.93 \text{ mA}$$

Example 7.12 *continued*

This is quite a bit lower than 1 mA, the value we are aiming for. It is easy to see from the above equation that a simple way to restore I_E to its nominal value would be to reduce R_E from 3.3 kΩ by the magnitude of the second term in the denominator (0.267 kΩ). Thus a more suitable value for R_E in this case would be $R_E = 3$ kΩ, which results in $I_E = 1.01$ mA $\simeq 1$ mA.[10]

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to I_E (i.e., 1 mA), resulting in $R_1 = 8$ kΩ and $R_2 = 4$ kΩ. We shall refer to the circuit using these latter values as design 2, for which the actual value of I_E using the initial value of R_E of 3.3 kΩ will be

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1 \text{ mA}$$

In this case, design 2, we need not change the value of R_E.

Finally, the value of R_C can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99$ mA $\simeq 1$ mA results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4 \text{ kΩ}$$

EXERCISE

7.34 For design 1 in Example 7.12, calculate the expected range of I_E if the transistor used has β in the range of 50 to 150. Express the range of I_E as a percentage of the nominal value ($I_E \simeq 1$ mA) obtained for $\beta = 100$. Repeat for design 2.

Ans. For design 1: 0.94 mA to 1.04 mA, a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.

A Two-Power-Supply Version of the Classical Bias Arrangement A somewhat simpler bias arrangement is possible if two power supplies are available, as shown in Fig. 7.53.

[10] Although reducing R_E restores I_E to the design value of 1 mA, it does not solve the problem of the dependence of the value of I_E on β. See Exercise 7.34.

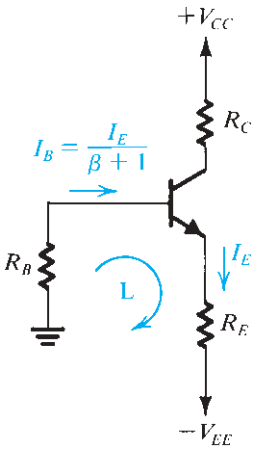


Figure 7.53 Biasing the BJT using two power supplies. Resistor R_B is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β-independence of the bias current.

Writing a loop equation for the loop labeled L gives

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{7.146}$$

This equation is identical to Eq. (7.143) except for V_{EE} replacing V_{BB}. Thus the two constraints of Eqs. (7.144) and (7.145) apply here as well. Note that if the transistor is to be used with the base grounded (i.e., in the common-base configuration), then R_B can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then R_B is needed. We shall study complete circuits of the various BJT amplifier configurations in Section 7.5. Finally, observe that the circuit in Fig. 7.53 is the counterpart of the MOS circuit in Fig. 7.48(e).

EXERCISE

D7.35 The bias arrangement of Fig. 7.53 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a signal swing at the collector of ±2 V. Use +10-V and –5-V power supplies.
Ans. $R_B = 0$; $R_E = 4.3\ \text{k}\Omega$; $R_C = 8.4\ \text{k}\Omega$

Biasing Using a Collector-to-Base Feedback Resistor In the BJT case, there is a counterpart to the MOSFET circuit of Fig. 7.50. Figure 7.54(a) shows such a simple but effective biasing arrangement that is suitable for common-emitter amplifiers. The circuit employs a resistor R_B connected between the collector and the base. Resistor R_B provides negative feedback, which helps to stabilize the bias point of the BJT.

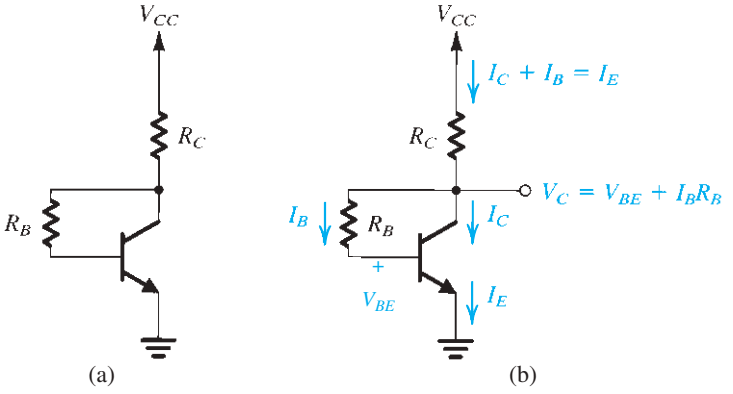


Figure 7.54 (**a**) A common-emitter transistor amplifier biased by a feedback resistor R_B. (**b**) Analysis of the circuit in (**a**).

Analysis of the circuit is shown in Fig. 7.54(b), from which we can write

$$\begin{aligned} V_{CC} &= I_E R_C + I_B R_B + V_{BE} \\ &= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE} \end{aligned}$$

Thus the emitter bias current is given by

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)} \tag{7.147}$$

It is interesting to note that this equation is identical to Eq. (7.143), which governs the operation of the traditional bias circuit, except that V_{CC} replaces V_{BB} and R_C replaces R_E. It follows that to obtain a value of I_E that is insensitive to variation of β, we select $R_B/(\beta + 1) \ll R_C$. Note, however, that the value of R_B determines the allowable negative signal swing at the collector since

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta + 1} \tag{7.148}$$

EXERCISE

D7.36 Design the circuit of Fig. 7.54 to obtain a dc emitter current of 1 mA, maximum gain, and a ±2-V signal swing at the collector; that is, design for $V_{CE} = +2.3$ V. Let $V_{CC} = 10$ V and $\beta = 100$.

Ans. $R_B = 162\ \text{k}\Omega$; $R_C = 7.7\ \text{k}\Omega$. Note that if standard 5% resistor values are used (Appendix J), we select $R_B = 160\ \text{k}\Omega$ and $R_C = 7.5\ \text{k}\Omega$. This results in $I_E = 1.02$ mA and $V_C = +2.3$ V.

7.5 Discrete-Circuit Amplifiers

With our study of transistor amplifier basics complete, we now put everything together by presenting practical circuits for discrete-circuit amplifiers. These circuits, which utilize the amplifier configurations studied in Section 7.3 and the biasing methods of Section 7.4, can be assembled using off-the-shelf discrete transistors, resistors, and capacitors. Though practical and carefully selected to illustrate some important points, the circuits presented in this section should be regarded as examples of discrete-circuit transistor amplifiers. Indeed, there is a great variety of such circuits, a number of which are explored in the end-of-chapter problems.

As mentioned earlier, the vast majority of discrete-circuit amplifiers utilize BJTs. This is reflected in this section where all the circuits presented except for one utilize BJTs. Of course, if desired, one can utilize MOSFETs in the same amplifier configurations presented here. Also, the MOSFET is the device of choice in the design of integrated-circuit (IC) amplifiers. We begin our study of IC amplifiers in Chapter 8.

As will be seen shortly, the circuits presented in this section utilize large capacitors (in the μF range) to couple the signal source to the input of the amplifier, and to couple the amplifier output signal to a load resistance or to the input of another amplifier stage. As well, a large capacitor is employed to establish a signal ground at the desired terminal of the transistor (e.g., at the emitter of a CE amplifier). The use of capacitors for these purposes simplifies the design considerably: Since capacitors block dc, one is able to first carry out the dc bias design and then connect the signal source and load to the amplifier without disturbing the dc design. There amplifiers are therefore known as **capacitively coupled amplifiers.**

7.5.1 A Common-Source (CS) Amplifier

As mentioned in Section 7.3, the common-source (CS) configuration is the most widely used of all MOSFET amplifier circuits. A common-source amplifier realized using the bias circuit of Fig. 7.48(c) is shown in Fig. 7.55(a). Observe that to establish a **signal ground**, or an **ac ground** as it is sometimes called, at the source, we have connected a large capacitor, C_S, between the source and ground. This capacitor, usually in the microfarad range, is required to provide a very small impedance (ideally, zero impedance—i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the signal current passes through C_S to ground and thus *bypasses* the resistance R_S; hence, C_S is called a **bypass capacitor**. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 10.1. For our purposes here we shall assume that C_S is acting as a perfect short circuit and thus is establishing a zero signal voltage at the MOSFET source.

To prevent disturbances to the dc bias current and voltages, the signal to be amplified, shown as voltage source v_{sig} with an internal resistance R_{sig}, is connected to the gate through a large capacitor C_{C1}. Capacitor C_{C1}, known as a **coupling capacitor**, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again, we note that as the signal frequency is lowered, the impedance of C_{C1} (i.e., $1/j\omega C_{C1}$) will increase and its effectiveness as a coupling capacitor will be correspondingly reduced. This problem, too, will be considered in Section 10.1 in connection with the dependence of the amplifier

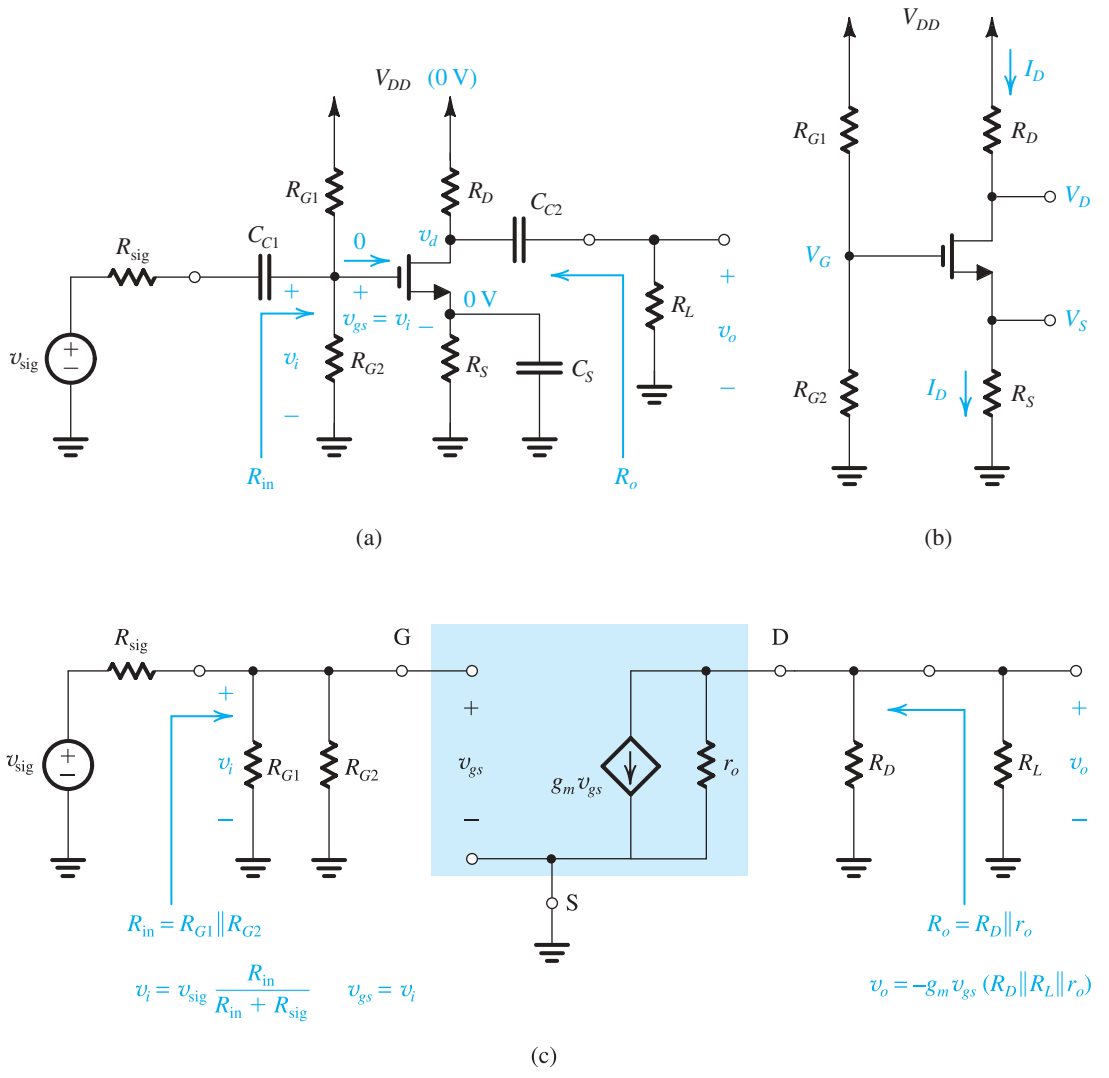


Figure 7.55 (**a**) A common-source amplifier using the classical biasing arrangement of Fig. 7.48(c). (**b**) Circuit for determining the bias point. (**c**) Equivalent circuit and analysis.

operation on frequency. For our purposes here we shall assume that C_{C1} is acting as a perfect short circuit as far as the signal is concerned.

The voltage signal resulting at the drain is coupled to the load resistance R_L via another coupling capacitor C_{C2}. We shall assume that C_{C2} acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage $v_o = v_d$. Note that R_L can be either an actual load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of another amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 9).

Since a capacitor behaves as an open circuit at dc, the circuit for performing the dc bias design and analysis is obtained by open-circuiting all capacitors. The resulting circuit is shown in Fig. 7.55(b) and can be designed as discussed in Section 7.4.1.

To determine the terminal characteristics of the CS amplifier of Fig. 7.55(a)—that is, its input resistance, voltage gain, and output resistance—we replace the MOSFET with its hybrid-π small-signal model, replace V_{DD} with a signal ground, and replace all coupling and bypass capacitors with short circuits. The result is the circuit in Fig. 7.55(c). Analysis is straightforward and is shown on the figure, thus

$$R_{\text{in}} = R_{G1} \| R_{G2} \tag{7.149}$$

which shows that to keep R_{in} high, large values should be used for R_{G1} and R_{G2}, usually in the megohm range. The overall voltage gain G_v is

$$G_v = -\frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} g_m (R_D \| R_L \| r_o) \tag{7.150}$$

Observe that we have taken r_o into account, simply because it is easy to do so. Its effect, however, is usually small (this is not the case for IC amplifiers, as will be explained in Chapter 8). Finally, to encourage the reader to do the small-signal analysis directly on the original circuit diagram, with the MOSFET model used implicitly, we show some of the analysis on the circuit of Fig. 7.55(a).

EXERCISES

D7.37 Design the bias circuit in Fig.7.55(b) for the CS amplifier of Fig. 7.55(a). Assume the MOSFET is specified to have $V_t = 1$ V, $k_n = 4$ mA/V^2, and $V_A = 100$ V. Neglecting the Early effect, design for $I_D = 0.5$ mA, $V_S = 3.5$ V, and $V_D = 6$ V using a power-supply $V_{DD} = 15$ V. Specify the values of R_S and R_D. If a current of 2 μA is used in the voltage divider, specify the values of R_{G1} and R_{G2}. Give the values of the MOSFET parameters g_m and r_o at the bias point.

Ans. $R_S = 7$ kΩ; $R_D = 18$ kΩ; $R_{G1} = 5$ MΩ; $R_{G2} = 2.5$ MΩ; $g_m = 2$ mA/V; $r_o = 200$ kΩ

7.38 For the CS amplifier of Fig. 7.55(a) use the design obtained in Exercise 7.37 to determine R_{in}, R_o, and the overall voltage gain G_v when $R_{\text{sig}} = 100$ kΩ and $R_L = 20$ kΩ.

Ans. 1.67 MΩ; 16.5 kΩ; −17.1 V/V

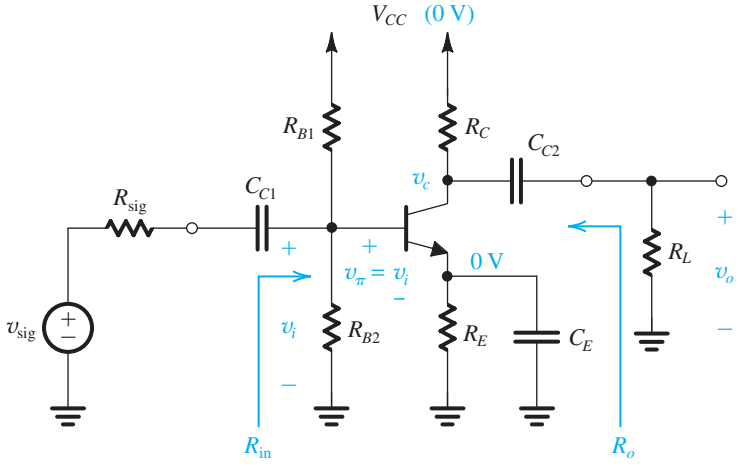
D7.39 As discussed in Section 7.3, beneficial effects can be realized by having an unbypassed resistance R_s in the source lead of the CS amplifier. This can be implemented in the circuit of Fig. 7.55(a) by splitting the resistance R_S into two resistances: R_s, which is left unbypassed, and $(R_S - R_s)$, across which the bypass capacitor C_S is connected. Now, if in order to improve linearity of the amplifier in Exercises 7.37 and 7.38, v_{gs} is to be reduced to half its value, what value should R_s have? What would the amplifier gain G_v become? Recall that when R_s is included it becomes difficult to include r_o in the analysis, so neglect it.

Ans. $R_s = 500$ Ω; $G_v = -8.9$ V/V

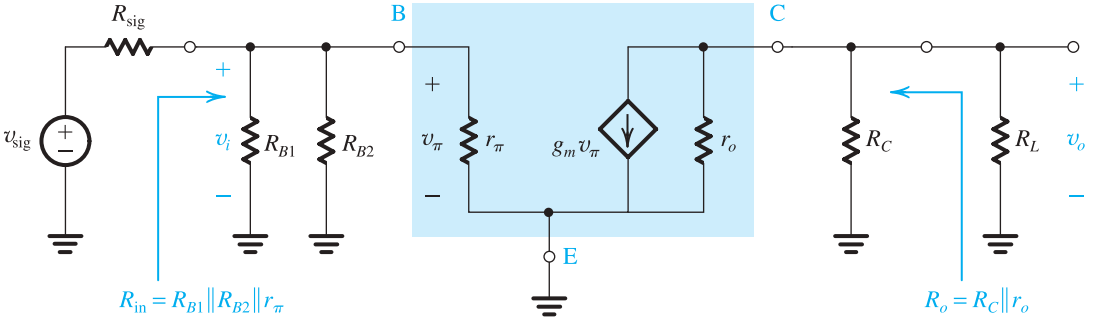
7.5.2 A Common-Emitter Amplifier

The common-emitter (CE) amplifier is the most widely used of all BJT amplifier configurations. Figure 7.56(a) shows a CE amplifier utilizing the classical biasing arrangement of Fig. 7.48(c), the design of which was considered in Section 7.4. The CE circuit in Fig. 7.54(a) is the BJT counterpart of the CS amplifier of Fig. 7.55(a). It utilizes coupling capacitors C_{C1} and C_{C2} and bypass capacitor C_E. Here we assume that these capacitors, while blocking dc, behave as perfect short circuits at all signal frequencies of interest.

To determine the characteristic parameters of the CE amplifier, we replace the BJT with its hybrid-π model, replace V_{CC} with a short circuit to ground, and replace the coupling and bypass capacitor with short circuits. The resulting small-signal equivalent circuit of the CE amplifier is shown in Fig. 7.56(b). The analysis is straightforward and is given in the



(a)



(b)

Figure 7.56 (**a**) A common-emitter amplifier using the classical biasing arrangement of Fig. 7.52(a). (**b**) Equivalent circuit and analysis.

figure, thus

$$R_{\text{in}} = R_{B1} \parallel R_{B2} \parallel r_\pi \tag{7.151}$$

which indicates that to keep R_{in} relatively high, R_{B1} and R_{B2} should be selected large (typically in the range of tens or hundreds of kilohms). This requirement conflicts with the need to keep R_{B1} and R_{B2} low so as to minimize the dependence of the dc current I_C on the transistor β. We discussed this design trade-off in Section 7.4.

The voltage gain G_v is given by

$$G_v = -\frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} g_m (R_C \parallel R_L \parallel r_o) \tag{7.152}$$

Note that we have taken r_o into account because it is easy to do so. However, as already mentioned, the effect of this parameter on discrete-circuit amplifier performance is usually small.

EXERCISES

D7.40 Design the bias circuit of the CE amplifier of Fig. 7.56(a) to obtain $I_E = 0.5$ mA and $V_C = +6$ V. Design for a dc voltage at the base of 5 V and a current through R_{B2} of 50 μA. Let $V_{CC} = +15$ V, $\beta = 100$, and $V_{BE} \simeq 0.7$ V. Specify the values of R_{B1}, R_{B2}, R_E, and R_C. Also give the values of the BJT small-signal parameters g_m, r_π, and r_o at the bias point. (For the calculation of r_o, let $V_A = 100$ V.)

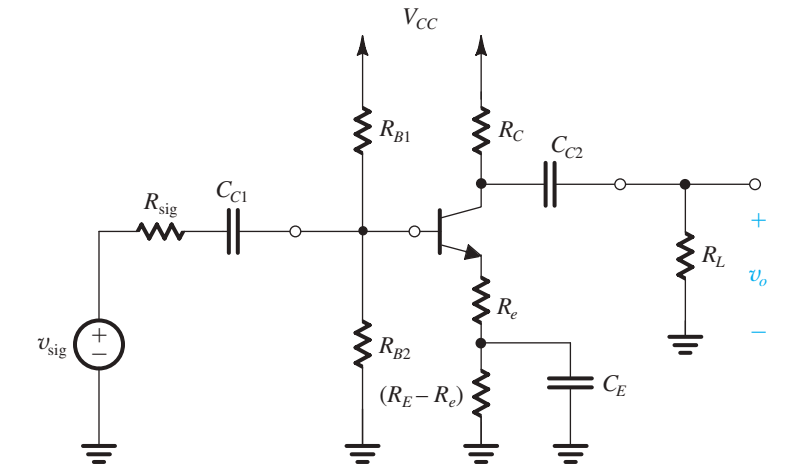
Ans. $R_{B1} = 182\,\text{k}\Omega$; $R_{B2} = 100\,\text{k}\Omega$; $R_E = 8.6\,\text{k}\Omega$; $R_C = 18\,\text{k}\Omega$; $g_m = 20$ mA/V, $r_\pi = 5\,\text{k}\Omega$, $r_o = 200\,\text{k}\Omega$

7.41 For the amplifier designed in Exercise 7.40, find R_{in}, R_o, and G_v when $R_{\text{sig}} = 10\,\text{k}\Omega$ and $R_L = 20\,\text{k}\Omega$.

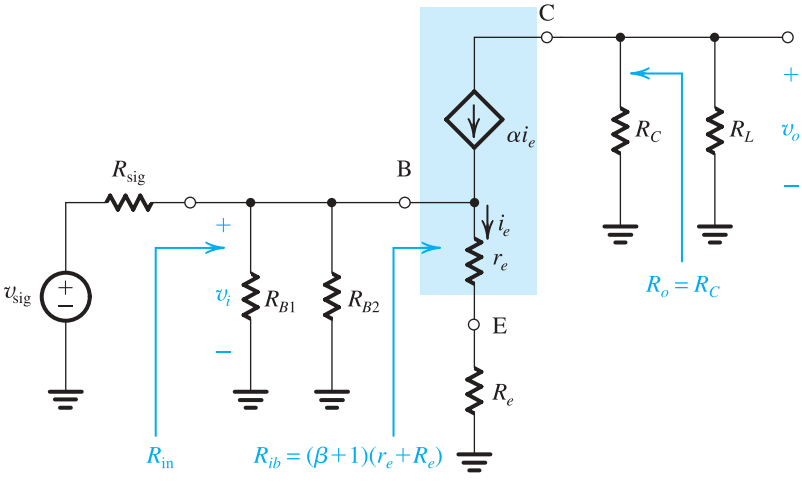
Ans. $R_{\text{in}} = 4.64\,\text{k}\Omega$; $R_o = 16.51\,\text{k}\Omega$; $G_v = -57.3$ V/V

7.5.3 A Common-Emitter Amplifier with an Emitter Resistance R_e

As discussed in Section 7.3.4, it is beneficial to include a small resistance in the transistor emitter lead. This can be implemented in the circuit of Fig. 7.56(a) by splitting the emitter bias resistance R_E into two components: an unbypassed resistance R_e, and a resistance $(R_E - R_e)$ across which the bypass capacitor C_E is connected. The resulting circuit is shown in Fig. 7.57(a) and its small-signal model is shown in Fig. 7.57(b). In the latter we utilize the T model of the BJT because it results in much simpler analysis (recall that this is always the case when a resistance is connected in series with the emitter). Also note that we have not included r_o, for doing so would complicate the analysis significantly. This burden would not be justified given that r_o has little effect on the performance of discrete-circuit amplifiers.



(a)



$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} \times \alpha \frac{(R_C \| R_L)}{r_e + R_e}$$

(b)

Figure 7.57 (**a**) A common-emitter amplifier with an unbiased emitter resistance R_e. (**b**) The amplifier small-signal model and analysis.

Analysis of the circuit in Fig. 7.57(b) is straightforward and is shown in the figure. Thus,

$$\begin{aligned} R_{in} &= R_{B1} \| R_{B2} \| (\beta + 1)(r_e + R_e) \\ &= R_{B1} \| R_{B2} \| [r_\pi + (\beta + 1)R_e] \end{aligned} \tag{7.153}$$

from which we note that including R_e increases R_{in} because it increases the input resistance looking into the base by adding a component $(\beta + 1)R_e$ to r_π. The overall voltage gain G_v is

$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} \times \alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}}$$

$$= -\alpha \frac{R_{in}}{R_{in} + R_{sig}} \frac{R_C \| R_L}{r_e + R_e} \tag{7.154}$$

EXERCISE

7.42 For the amplifier designed in Exercise 7.40 and analyzed in Exercise 7.41, let it be required to raise R_{in} to 10 kΩ. What is the required value of R_e, and what does the overall voltage gain G_v become?
Ans. $R_e = 67.7\ \Omega$; $G_v = -39.8$ V/V

7.5.4 A Common-Base (CB) Amplifier

Figure 7.58(a) shows a CB amplifier designed using the biasing arrangement of Fig. 7.53. Note that the availability of two power supplies, V_{CC} and $-V_{EE}$, enables us to connect the base directly to ground, obviating the need for a large bypass capacitor to establish a signal ground at the base.

The small-signal equivalent circuit of the CB amplifier is shown in Fig 7.58(b). As expected, we have utilized the T model of the BJT and have not included r_o. Including r_o would complicate the analysis significantly without making much difference to the results in the case of discrete-circuit amplifiers. From the circuit in Fig. 7.58(b) we find

$$R_{in} = r_e \| R_E \simeq r_e \simeq 1/g_m$$

which as expected can be very small, causing v_i to be a small fraction of v_{sig},

$$v_i = v_{sig} \frac{R_{in}}{R_{in} + R_{sig}}$$

Now,

$$i_e = -\frac{v_i}{r_e}$$

and

$$v_o = -\alpha i_e (R_C \| R_L)$$

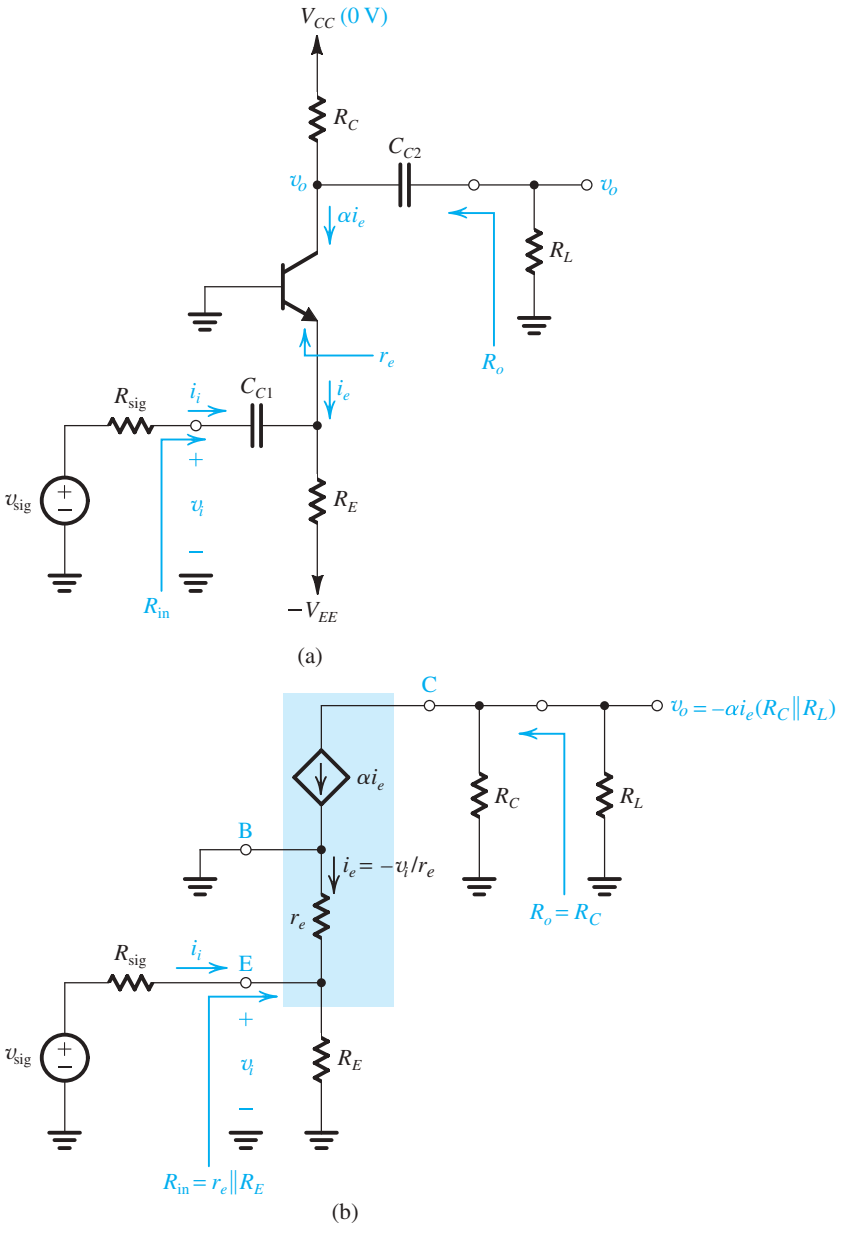


Figure 7.58 (**a**) A common-base amplifier using the structure of Fig. 7.53 with R_B omitted (since the base is grounded). (**b**) Equivalent circuit obtained by replacing the transistor with its T model.

Thus, the overall voltage gain is given by

$$G_v = \alpha \frac{R_{in}}{R_{in} + R_{sig}} \frac{R_C \| R_L}{r_e} = \frac{R_{in}}{R_{in} + R_{sig}} g_m (R_C \| R_L) \tag{7.155}$$

EXERCISE

D7.43 Design the CB amplifier of Fig. 7.58(a) to provide an input resistance R_{in} that matches the source resistance of a cable with a characteristic resistance of 50 Ω. Assume that $R_E \gg r_e$. The available power supplies are ±5 V and $R_L = 8$ kΩ. Design for a dc collector voltage $V_C = +1$ V. Specify the values of R_C and R_E. What overall voltage gain is obtained? If v_{sig} is a sine wave with a peak amplitude of 10 mV, what is the peak amplitude of the output voltage? Let $\alpha \simeq 1$.
Ans. $R_C = 8$ kΩ; $R_E = 8.6$ kΩ; 40 V/V; 0.4 V

7.5.5 An Emitter Follower

Figure 7.59(a) shows an emitter follower designed using the bias arrangement of Fig. 7.53 and two power supplies, V_{CC} and $-V_{EE}$. The bias resistance R_B affects the input resistance of the follower and should be chosen as large as possible while limiting the dc voltage drop across it to a small fraction of V_{EE}; otherwise the dependence of the bias current I_C on β can become unacceptably large.

Figure 7.59(b) shows the small-signal equivalent circuit of the emitter follower. Here, as expected, we have replaced the BJT with its T model and included r_o (since this can be done very simply). The input resistance of the emitter follower can be seen to be

$$R_{in} = R_B \| R_{ib} \tag{7.156}$$

where R_{ib}, the input resistance looking into the base, can be obtained by using the resistance-reflection rule. Toward that end, note that r_o appears in parallel with R_E and R_L (which is why it can be easily taken into account). Thus,

$$R_{ib} = (\beta + 1)[r_e + (R_E \| r_o \| R_L)] \tag{7.157}$$

The overall voltage gain can be determined by tracking the signal transmission from source to load,

$$v_i = v_{sig} \frac{R_{in}}{R_{in} + R_{sig}} \tag{7.158}$$

and

$$v_o = v_i \frac{R_E \| r_o \| R_L}{r_e + (R_E \| r_o \| R_L)} \tag{7.159}$$

Thus,

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} \frac{(R_E \| r_o \| R_L)}{r_e + (R_E \| r_o \| R_L)} \tag{7.160}$$

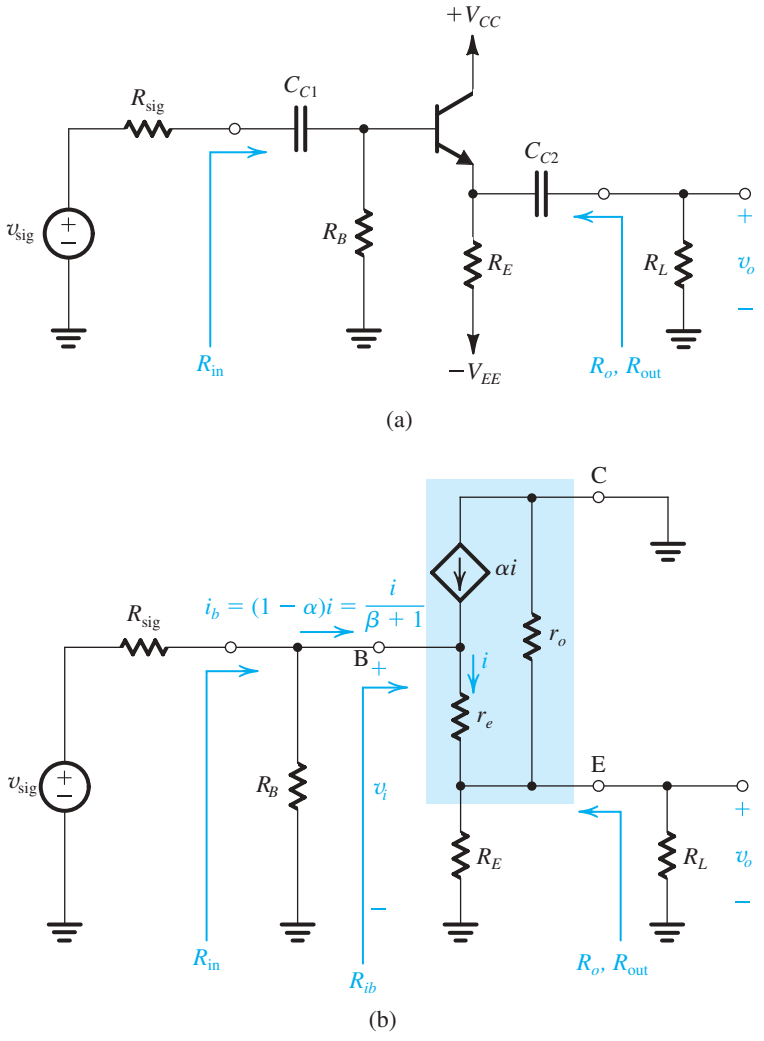


Figure 7.59 (**a**) An emitter-follower circuit. (**b**) Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model. Note that r_o is included because it is easy to do so. Normally, its effect on performance is small.

Finally, the output resistance R_{out} can be obtained by short-circuiting v_{sig} and looking back into the output terminal, excluding R_L, as

$$R_{\text{out}} = r_o \,\|\, R_E \,\|\, \left[r_e + \frac{R_B \,\|\, R_{\text{sig}}}{\beta + 1} \right] \tag{7.161}$$

Note that we have used the inverse resistance-reflection rule, namely, dividing the total resistance in the base, $(R_B \,\|\, R_{\text{sig}})$, by $(\beta + 1)$.

EXERCISE

D7.44 Design the emitter follower of Fig. 7.59(a) to operate at a dc emitter current $I_E = 1$ mA. Allow a dc voltage drop across R_B of 1 V. The available power supplies are ± 5 V, $\beta = 100$, $V_{BE} = 0.7$ V, and $V_A = 100$ V. Specify the values required for R_B and R_E. Now if $R_{sig} = 50$ kΩ and $R_L = 1$ kΩ, find R_{in}, v_i/v_{sig}, v_o/v_i, G_v, and R_{out}. (*Note*: In performing the bias design, neglect the Early effect.)

Ans. $R_B = 100$ kΩ; $R_E = 3.3$ kΩ; 44.3 kΩ; 0.469 V/V; 0.968 V/V; 0.454 V/V; 320 Ω

7.5.6 The Amplifier Frequency Response

Thus far, we have assumed that the gain of transistor amplifiers is constant independent of the frequency of the input signal. This would imply that transistor amplifiers have infinite bandwidth, which of course is not true. To illustrate, we show in Fig. 7.60 a sketch of the magnitude of the gain of a common-emitter or a CS amplifier such as those shown in Figs. 7.56 and 7.55, respectively, versus frequency. Observe that there is indeed a wide frequency range over which the gain remains almost constant. This obviously is the useful frequency range of

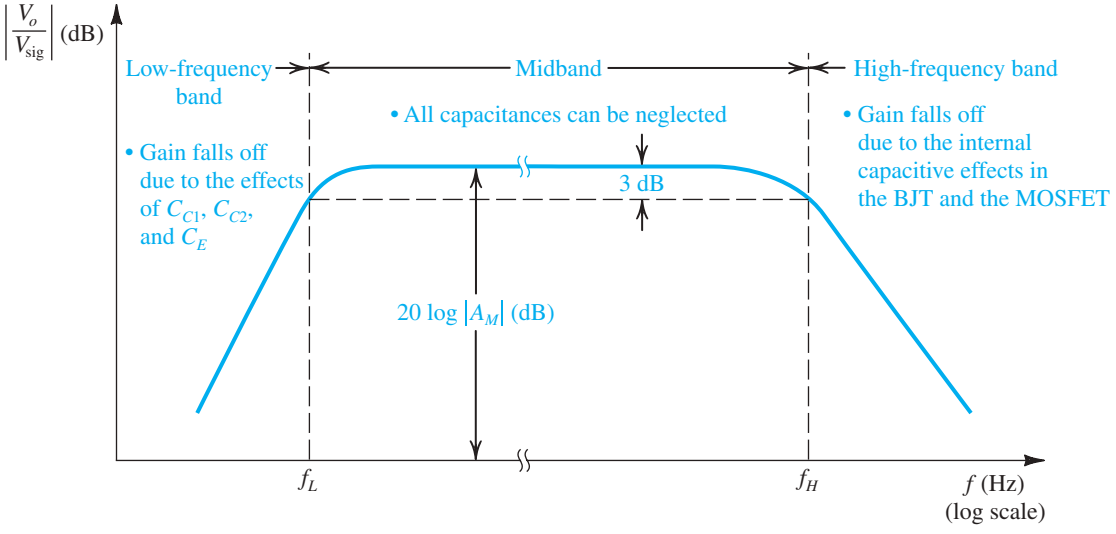


Figure 7.60 Sketch of the magnitude of the gain of a CE (Fig. 7.56) or CS (Fig. 7.55) amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency-response determination.

operation for the particular amplifier. Thus far, we have been assuming that our amplifiers are operating in this frequency band, called the **midband**.

Figure 7.60 indicates that at lower frequencies, the magnitude of amplifier gain falls off. This is because the coupling and bypass capacitors no longer have low impedances. Recall that we assumed that their impedances were small enough to act as short circuits. Although this can be true at midband frequencies, as the frequency of the input signal is lowered, the reactance $1/j\omega C$ of each of these capacitors becomes significant, and it can be shown that this results in the overall voltage gain of the amplifier decreasing.

Figure 7.60 indicates also that the gain of the amplifier falls off at the high-frequency end. This is due to the internal capacitive effects in the BJT and the MOSFET. In Chapter 10 we shall study the internal capacitive effects of both transistor types and will augment their hybrid-π models with capacitances that model these effects.

We will undertake a detailed study of the frequency response of transistor amplifiers in Chapter 10. For the time being, however, it is important for the reader to realize that for every transistor amplifier, there is a finite band over which the gain is almost constant. The boundaries of this useful frequency band, or midband, are the two frequencies f_L and f_H at which the gain drops by a certain number of decibels (usually 3 dB) below its value at midband. As indicated in Fig. 7.60, the amplifier **bandwidth**, or 3-dB bandwidth, is defined as the difference between the lower (f_L) and upper or higher (f_H) 3-dB frequencies:

$$BW = f_H - f_L$$

and since usually $f_L \ll f_H$,

$$BW \simeq f_H$$

A figure of merit for the amplifier is its **gain–bandwidth product**, defined as

$$GB = |A_M| BW$$

where $|A_M|$ is the magnitude of the amplifier gain in the midband. It will be seen in Chapter 10 that in amplifier design it is usually possible to trade off gain for bandwidth. One way to accomplish this, for instance, is by including resistance R_e in the emitter of the CE amplifier.

Summary

- The essence of the use of the MOSFET (the BJT) as an amplifier is that when the transistor is operated in the active region, v_{GS} controls i_D (v_{BE} controls i_C) in the manner of a voltage-controlled current source. When the device is dc biased in the active region, and the signal v_{gs} (v_{be}) is kept small, the operation becomes almost linear, with $i_d = g_m v_{gs}$ ($i_c = g_m v_{be}$).
- The most fundamental parameter in characterizing the small-signal linear operation of a transistor is the transconductance g_m. For a MOSFET, $g_m = \mu_n C_{ox}(W/L)V_{OV} = \sqrt{2\mu_n C_{ox}(W/L)I_D} = 2I_D/V_{OV}$; and for the BJT, $g_m = I_C/V_T$.
- A systematic procedure for the analysis of a transistor amplifier circuit is presented in Table 7.1. Tables 7.2 and 7.3 present the small-signal models for the MOSFET and the BJT, respectively.
- When a resistance is connected in series with the source (or emitter), the T model is the most convenient to use.
- The three basic configurations of MOS and BJT amplifiers are presented in Fig. 7.33. Their characteristic parameter values are provided in Table 7.4 (for the MOS case) and in Table 7.5 (for the BJT case).
- The CS amplifier, which has (ideally) infinite input resistance and a reasonably high gain but a rather high output resistance and a limited high-frequency response (more on the latter point in Chapter 10), is used to obtain most of the gain in a cascade amplifier. Similar remarks apply to the CE amplifier, except that it has a relatively low input resistance ($r_\pi = \beta/g_m$) arising from the finite base current of the BJT (finite β). Its voltage gain, however, can be larger than that of the CS amplifier because of the higher values of g_m obtained with BJTs.
- Adding a resistance R_s in the source of a CS amplifier (a resistance R_e in the emitter of a CE amplifier) can lead to beneficial effects including the following: raising the input resistance of the CE amplifier, increasing linearity, and extending the useful amplifier bandwidth, at the expense of reducing the gain, all by a factor equal to $(1 + g_m R_s)$ [$(1 + g_m R_e)$ for the BJT case].
- The CG (CB) amplifier has a low input resistance and thus, used alone, it has limited and specialized applications. However, its excellent high-frequency response makes it attractive in combination with the CS (CE) amplifier (Chapters 8 and 10).
- The source follower has (ideally) infinite input resistance, a voltage gain lower than but close to unity, and a low output resistance. It is employed as a voltage buffer and as the output stage of a multistage amplifier. Similar remarks apply to the emitter follower except that its input resistance, though large, is finite. Specifically, the emitter follower multiplies the total resistance in the emitter by $(\beta + 1)$ before presenting it to the signal source.
- The resistance-reflection rule is a powerful tool in the analysis of BJT amplifier circuits: All resistances in the emitter circuit including the emitter resistance r_e can be reflected to the base side by multiplying them by $(\beta + 1)$. Conversely, we can reflect all resistances in the base circuit to the emitter side by dividing them by $(\beta + 1)$.
- In the analysis and design of discrete-circuit amplifiers, it is rarely necessary to take the transistor output resistance r_o into account. In some situations, however, r_o can be easily taken into account; specifically in the CS (CE) amplifier and in the source (emitter) follower. In IC amplifiers, r_o must always be taken into account.
- A key step in the design of transistor amplifiers is to bias the transistor to operate at an appropriate point in the active region. A good bias design ensures that the parameters of the operating point (I_D, V_{OV}, and V_{DS} for the MOSFET; I_C and V_{CE} for the BJT) are predictable and stable and do not vary by large amounts when the transistor is replaced by another of the same type. The bias methods studied in this chapter are suited for discrete-circuit amplifiers only because they utilize large coupling and bypass capacitors.
- Discrete-circuit amplifiers predominantly employ BJTs. The opposite is true for IC amplifiers, where the device of choice is the MOSFET.

Computer Simulation Problems

SIM Problems identified by the Multisim/PSpice icon are intended to demonstrate the value of using SPICE simulation to verify hand analysis and design, and to investigate important issues such as allowable signal swing and amplifier nonlinear distortion. Instructions to assist in setting up PSpice and Multisim simulations for all the indicated problems can be found in the corresponding files on the website. Note that if a particular parameter value is not specified in the problem statement, you are to make a reasonable assumption.

Section 7.1: Basic Principles

7.1 For the MOS amplifier of Fig. 7.2(a) with $V_{DD} = 5$ V, $V_t = 0.5$ V, $k_n = 10$ mA/V^2, and $R_D = 20$ kΩ, determine the coordinates of the active-region segment (AB) of the VTC [Fig. 7.2(b)].

D 7.2 For the MOS amplifier of Fig. 7.2(a) with $V_{DD} = 5$ V and $k_n = 5$ mA/V^2, it is required to have the end point of the VTC, point B, at $V_{DS} = 0.5$ V. What value of R_D is required? If the transistor is replaced with another having twice the value of the transconductance parameter k_n, what new value of R_D is needed?

D 7.3 It is required to bias the MOS amplifier of Fig. 7.3 at point Q for which $V_{OV} = 0.2$ V and $V_{DS} = 1$ V. Find the required value of R_D when $V_{DD} = 5$ V, $V_t = 0.5$ V, and $k_n = 10$ mA/V^2. Also specify the coordinates of the VTC end point B. What is the small-signal voltage gain of this amplifier? Assuming linear operation, what is the maximum allowable negative signal swing at the output? What is the corresponding peak input signal?

7.4 The MOS amplifier of Fig. 7.4(a), when operated with $V_{DD} = 2$ V, is found to have a maximum small-signal voltage gain magnitude of 14 V/V. Find V_{OV} and V_{DS} for bias point Q at which a voltage gain of −12 V/V is obtained.

7.5 Consider the amplifier of Fig. 7.4(a) for the case $V_{DD} = 5$ V, $R_D = 24$ kΩ, $k_n'(W/L) = 1$ mA/V^2, and $V_t = 1$ V.

(a) Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig. 7.4(b).

(b) If the amplifier is biased to operate with an overdrive voltage V_{OV} of 0.5 V, find the coordinates of the bias point Q on the transfer characteristic. Also, find the value of I_D and of the incremental gain A_v at the bias point.

(c) For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

7.6 Various measurements are made on an NMOS amplifier for which the drain resistor R_D is 20 kΩ. First, dc measurements show the voltage across the drain resistor, V_{RD}, to be 1.5 V and the gate-to-source bias voltage to be 0.7 V. Then, ac measurements with small signals show the voltage gain to be −10 V/V. What is the value of V_t for this transistor? If the process transconductance parameter k_n' is 200 μA/V^2, what is the MOSFET's W/L?

***7.7** The expression for the incremental voltage gain A_v given in Eq. (7.16) can be written in as

$$A_v = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

where V_{DS} is the bias voltage at the drain. This expression indicates that for given values of V_{DD} and V_{OV}, the gain magnitude can be increased by biasing the transistor at a lower V_{DS}. This, however, reduces the allowable output signal swing in the negative direction. Assuming linear operation around the bias point, show that the largest possible negative output signal peak $\hat{v}_o$ that is achievable while the transistor remains saturated is

$$\hat{v}_o = (V_{DS} - V_{OV}) \Big/ \left(1 + \frac{1}{|A_v|}\right)$$

For $V_{DD} = 5$ V and $V_{OV} = 0.5$ V, provide a table of values for A_v, $\hat{v}_o$, and the corresponding $\hat{v}_i$ for $V_{DS} = 1$ V, 1.5 V, 2 V, and 2.5 V. If $k_n'(W/L) = 1$ mA/V^2, find I_D and R_D for the design for which $V_{DS} = 1$ V.

D *7.8 Design the MOS amplifier of Fig. 7.4(a) to obtain maximum gain while allowing for an output voltage swing of at least ±0.5 V. Let $V_{DD} = 5$ V, and utilize an overdrive

voltage of approximately 0.2 V.

(a) Specify V_{DS} at the bias point.
(b) What is the gain achieved? What is the signal amplitude $\hat{v}_{gs}$ that results in the 0.5-V signal amplitude at the output?
(c) If the dc bias current in the drain is to be 100 μA, what value of R_D is needed?
(d) If $k_n' = 200\ \mu A/V^2$, what W/L ratio is required for the MOSFET?

***7.9** Figure P7.9 shows an amplifier in which the load resistor R_D has been replaced with another NMOS transistor Q_2 connected as a two-terminal device. Note that because v_{DG} of Q_2 is zero, it will be operating in saturation at all times, even when $v_I = 0$ and $i_{D2} = i_{D1} = 0$. Note also that the two transistors conduct equal drain currents. Using $i_{D1} = i_{D2}$, show that for the range of v_I over which Q_1 is operating in saturation, that is, for

$$V_{t1} \le v_I \le v_O + V_{t1}$$

the output voltage will be given by

$$v_O = V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}}V_t - \sqrt{\frac{(W/L)_1}{(W/L)_2}}v_I$$

where we have assumed $V_{t1} = V_{t2} = V_t$. Thus the circuit functions as a linear amplifier, even for large input signals. For $(W/L)_1 = (50\ \mu m/0.5\ \mu m)$ and $(W/L)_2 = (5\ \mu m/0.5\ \mu m)$, find the voltage gain.

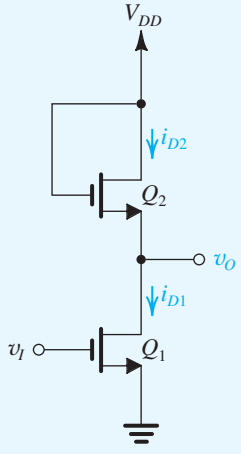


Figure P7.9

7.10 A BJT amplifier circuit such as that in Fig. 7.6 is operated with $V_{CC} = +5$ V and is biased at $V_{CE} = +1$ V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

7.11 For the amplifier circuit in Fig. 7.6 with $V_{CC} = +5$ V and $R_C = 1$ kΩ, find V_{CE} and the voltage gain at the following dc collector bias currents: 0.5 mA, 1 mA, 2.5 mA, 4 mA, and 4.5 mA. For each, give the maximum possible positive- and negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

D 7.12 Consider the CE amplifier circuit of Fig. 7.6 when operated with a dc supply $V_{CC} = +5$ V. It is required to find the point at which the transistor should be biased; that is, find the value of V_{CE} so that the output sine-wave signal v_{ce} resulting from an input sine-wave signal v_{be} of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (*Hint:* To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without v_{CE} decreasing below 0.3 V.)

7.13 A designer considers a number of low-voltage BJT amplifier designs utilizing power supplies with voltage V_{CC} of 1.0, 1.5, 2.0, or 3.0 V. For transistors that saturate at $V_{CE} = 0.3$ V, what is the largest possible voltage gain achievable with each of these supply voltages? If in each case biasing is adjusted so that $V_{CE} = V_{CC}/2$, what gains are achieved? If a negative-going output signal swing of 0.4 V is required, at what V_{CE} should the transistor be biased to obtain maximum gain? What is the gain achieved with each of the supply voltages? (Notice that all of these gains are independent of the value of I_C chosen!)

D *7.14 A BJT amplifier such as that in Fig. 7.6 is to be designed to support relatively undistorted sine-wave output signals of peak amplitudes P volt without the BJT entering saturation or cutoff and to have the largest possible voltage gain, denoted A_v V/V. Show that the minimum supply voltage V_{CC} needed is given by

$$V_{CC} = V_{CEsat} + P + |A_v|V_T$$

Also, find V_{CC}, specified to the nearest 0.5 V, for the following situations:

(a) $A_v = -20$ V/V, $P = 0.2$ V
(b) $A_v = -50$ V/V, $P = 0.5$ V
(c) $A_v = -100$ V/V, $P = 0.5$ V
(d) $A_v = -100$ V/V, $P = 1.0$ V
(e) $A_v = -200$ V/V, $P = 1.0$ V
(f) $A_v = -500$ V/V, $P = 1.0$ V
(g) $A_v = -500$ V/V, $P = 2.0$ V

7.15 The transistor in the circuit of Fig. P7.15 is biased at a dc collector current of 0.3 mA. What is the voltage gain? (*Hint:* Use Thévenin's theorem to convert the circuit to the form in Fig. 7.6.)

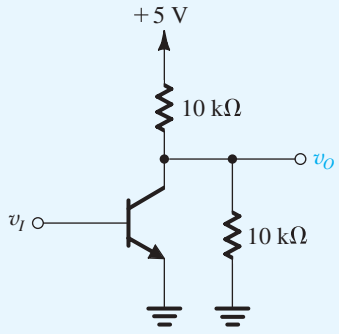


Figure P7.15

7.16 Sketch and label the voltage-transfer characteristics of the *pnp* amplifiers shown in Fig. P7.16.

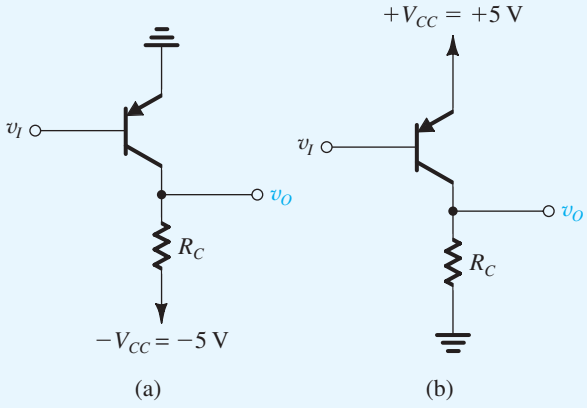


Figure P7.16

***7.17** In deriving the expression for small-signal voltage gain A_v in Eq. (7.21) we neglected the Early effect. Derive this expression including the Early effect by substituting

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

in Eq. (7.4) and including the factor $(1 + V_{CE}/V_A)$ in Eq. (7.11). Show that the gain expression changes to

$$A_v = \frac{-I_C R_C/V_T}{\left[1 + \dfrac{I_C R_C}{V_A + V_{CE}}\right]} = -\frac{(V_{CC} - V_{CE})/V_T}{\left[1 + \dfrac{V_{CC} - V_{CE}}{V_A + V_{CE}}\right]}$$

For the case $V_{CC} = 5$ V and $V_{CE} = 3$ V, what is the gain without and with the Early effect taken into account? Let $V_A = 100$ V.

7.18 When the amplifier circuit of Fig. 7.6 is biased with a certain V_{BE}, the dc voltage at the collector is found to be +2 V. For $V_{CC} = +5$ V and $R_C = 1$ kΩ, find I_C and the small-signal voltage gain. For a change $\Delta v_{BE} = +5$ mV, calculate the resulting Δv_O. Calculate it two ways: by using the transistor exponential characteristic Δi_C, and approximately, using the small-signal voltage gain. Repeat for $\Delta v_{BE} = -5$ mV. Summarize your results in a table.

***7.19** Consider the amplifier circuit of Fig. 7.6 when operated with a supply voltage $V_{CC} = +3$V.

(a) What is the theoretical maximum voltage gain that this amplifier can provide?
(b) What value of V_{CE} must this amplifier be biased at to provide a voltage gain of –60 V/V?
(c) If the dc collector current I_C at the bias point in (b) is to be 0.5 mA, what value of R_C should be used?
(d) What is the value of V_{BE} required to provide the bias point mentioned above? Assume that the BJT has $I_S = 10^{-15}$ A.
(e) If a sine-wave signal v_{be} having a 5-mV peak amplitude is superimposed on V_{BE}, find the corresponding output voltage signal v_{ce} that will be superimposed on V_{CE} assuming linear operation around the bias point.
(f) Characterize the signal current i_c that will be superimposed on the dc bias current I_C.

(g) What is the value of the dc base current I_B at the bias point? Assume $\beta = 100$. Characterize the signal current i_b that will be superimposed on the base current I_B.

(h) Dividing the amplitude of v_{be} by the amplitude of i_b, evaluate the incremental (or small-signal) input resistance of the amplifier.

(i) Sketch and clearly label correlated graphs for v_{BE}, v_{CE}, i_C, and i_B versus time. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

7.20 The essence of transistor operation is that a change in v_{BE}, Δv_{BE}, produces a change in i_C, Δi_C. By keeping Δv_{BE} small, Δi_C is approximately linearly related to Δv_{BE}, $\Delta i_C = g_m \Delta v_{BE}$, where g_m is known as the transistor transconductance. By passing Δi_C through R_C, an output voltage signal Δv_O is obtained. Use the expression for the small-signal voltage gain in Eq. (7.20) to derive an expression for g_m. Find the value of g_m for a transistor biased at $I_C = 0.5$ mA.

7.21 The purpose of this problem is to illustrate the application of graphical analysis to the circuit shown in Fig. P7.21. Sketch $i_C - v_{CE}$ characteristic curves for the BJT for $i_B = 10\ \mu$A, 20 μA, 30 μA, and 40 μA. Assume the lines to be horizontal (i.e., neglect the Early effect), and let $\beta = 100$. For $V_{CC} = 5$ V and $R_C = 1$ kΩ, sketch the load line. What peak-to-peak collector voltage swing will result for i_B varying over the range 10 μA to 40 μA? If the BJT is biased at $V_{CE} = \frac{1}{2}V_{CC}$, find the value of I_C and I_B. If at this current $V_{BE} = 0.7$ V and if $R_B = 100$ kΩ, find the required value of V_{BB}.

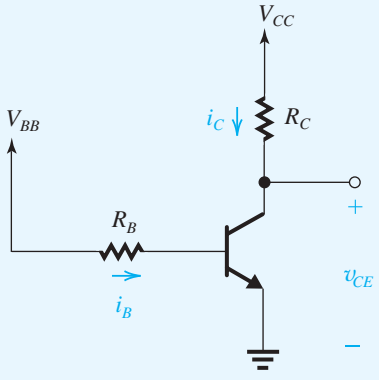


Figure P7.21

***7.22** Sketch the $i_C - v_{CE}$ characteristics of an *npn* transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves for $i_B = 20\ \mu$A, 50 μA, 80 μA, and 100 μA. For the purpose of this sketch, assume that $i_C = \beta i_B$ at $v_{CE} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_C = 1$ kΩ. If the dc bias current into the base is 50 μA, write the equation for the corresponding $i_C - v_{CE}$ curve. Also, write the equation for the load line, and solve the two equations to obtain V_{CE} and I_C. If the input signal causes a sinusoidal signal of 30-μA peak amplitude to be superimposed on I_B, find the corresponding signal components of i_C and v_{CE}.

Section 7.2: Small-Signal Operation and Models

***7.23** This problem investigates the nonlinear distortion introduced by a MOSFET amplifier. Let the signal v_{gs} be a sine wave with amplitude V_{gs}, and substitute $v_{gs} = V_{gs} \sin \omega t$ in Eq. (7.28). Using the trigonometric identity $\sin^2\theta = \frac{1}{2} - \frac{1}{2}\cos 2\theta$, show that the ratio of the signal at frequency 2ω to that at frequency ω, expressed as a percentage (known as the second-harmonic distortion) is

$$\text{Second-harmonic distortion} = \frac{1}{4}\frac{V_{gs}}{V_{OV}} \times 100$$

If in a particular application V_{gs} is 10 mV, find the minimum overdrive voltage at which the transistor should be operated so that the second-harmonic distortion is kept to less than 1%.

7.24 Consider an NMOS transistor having $k_n = 10$ mA/V^2. Let the transistor be biased at $V_{OV} = 0.2$ V. For operation in saturation, what dc bias current I_D results? If a 0.02-V signal is superimposed on V_{GS}, find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias current I_D. Repeat for a –0.02-V signal. Use these results to estimate g_m of the FET at this bias point. Compare with the value of g_m obtained using Eq. (7.33).

7.25 Consider the FET amplifier of Fig. 7.10 for the case $V_t = 0.4$ V, $k_n = 5$ mA/V^2, $V_{GS} = 0.6$ V, $V_{DD} = 1.8$ V, and $R_D = 10$ kΩ.

(a) Find the dc quantities I_D and V_{DS}.
(b) Calculate the value of g_m at the bias point.
(c) Calculate the value of the voltage gain.
(d) If the MOSFET has $\lambda = 0.1$ V^{-1}, find r_o at the bias point and calculate the voltage gain.

D ***7.26** An NMOS amplifier is to be designed to provide a 0.20-V peak output signal across a 20-kΩ load that can be used as a drain resistor. If a gain of at least 10 V/V is needed, what g_m is required? Using a dc supply of 1.8 V, what values of I_D and V_{OV} would you choose? What W/L ratio is required if $\mu_n C_{ox} = 200\ \mu$A/V^2? If $V_t = 0.4$ V, find V_{GS}.

D ***7.27** In this problem we investigate an optimum design of the CS amplifier circuit of Fig. 7.10. First, use the voltage gain expression $A_v = -g_m R_D$ together with Eq. (7.42) for g_m to show that

$$A_v = -\frac{2I_D R_D}{V_{OV}} = -\frac{2(V_{DD} - V_{DS})}{V_{OV}}$$

Next, let the maximum positive input signal be $\hat{v}_i$. To keep the second-harmonic distortion to an acceptable level, we bias the MOSFET to operate at an overdrive voltage $V_{OV} \gg \hat{v}_i$. Let $V_{OV} = m\hat{v}_i$. Now, to maximize the voltage gain $|A_v|$, we design for the lowest possible V_{DS}. Show that the minimum V_{DS} that is consistent with allowing a negative signal voltage swing at the drain of $|A_v|\ \hat{v}_i$ while maintaining saturation-mode operation is given by

$$V_{DS} = \frac{V_{OV} + \hat{v}_i + 2V_{DD}(\hat{v}_i/V_{OV})}{1 + 2(\hat{v}_i/V_{OV})}$$

Now, find V_{OV}, V_{DS}, A_v, and $\hat{v}_o$ for the case $V_{DD} = 2.5$ V, $\hat{v}_i = 20$ mV, and $m = 15$. If it is desired to operate this transistor at $I_D = 200\ \mu$A, find the values of R_D and W/L, assuming that for this process technology $k_n' = 100\ \mu$A/V^2.

7.28 In the table below, for MOS transistors operating under a variety of conditions, complete as many entries as possible. Although some data is not available, it is always possible to calculate g_m using one of Eqs. (7.40), (7.41), or (7.42). Assume $\mu_n = 500$ cm^2/V· s, $\mu_p = 250$ cm^2/V · s, and $C_{ox} = 0.4$ fF/μm^2.

			Voltages (V)			Dimensions (μm)				
Case	**Type**	I_D **(mA)**	$\lvert V_{GS}\rvert$	$\lvert V_t\rvert$	V_{OV}	W	L	W/L	$k'(W/L)$	g_m**(mA/V)**
a	N	1	3	2			1			
b	N	1		0.7	0.5	50				
c	N	10			2		1			
d	N	0.5			0.5					
e	N	0.1				10	2			
f	N		1.8	0.8		40	4			
g	P	0.5						25		
h	P		3	1					0.5	
i	P	10				4000	2			
j	P	10			4					
k	P				1	30	3			
l	P				5				0.08	

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

7.29 An NMOS technology has $\mu_n C_{ox} = 250\ \mu A/V^2$ and $V_t = 0.5$ V. For a transistor with $L = 0.5\ \mu m$, find the value of W that results in $g_m = 2$ mA/V at $I_D = 0.25$ mA. Also, find the required V_{GS}.

7.30 For the NMOS amplifier in Fig. P7.30, replace the transistor with its T equivalent circuit, assuming $\lambda = 0$. Derive expressions for the voltage gains v_s/v_i and v_d/v_i.

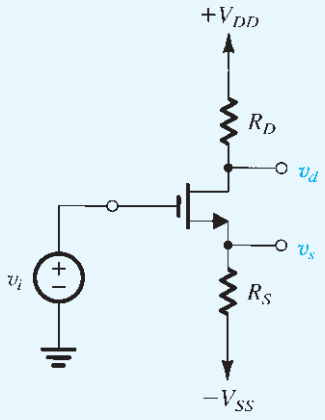


Figure P7.30

SIM **7.31** In the circuit of Fig. P7.31, the NMOS transistor has $|V_t| = 0.5$ V and $V_A = 50$ V and operates with $V_D = 1$ V. What is the voltage gain v_o/v_i ? What do V_D and the gain become for I increased to 1 mA?

7.32 For a 0.18-μm CMOS fabrication process: $V_{tn} = 0.5$ V, $V_{tp} = -0.5$ V, $\mu_n C_{ox} = 400\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $C_{ox} = 8.6\ fF/\mu m^2$, V_A (n-channel devices) $= 5L$ (μm), and $|V_A|$ (p-channel devices) $= 6L$ (μm). Find the small-signal model parameters (g_m and r_o) for both an NMOS and a PMOS transistor having $W/L = 10\ \mu m/0.5\ \mu m$ and operating at $I_D = 100\ \mu A$. Also, find the overdrive voltage at which each device must be operating.

***7.33** Figure P7.33 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). All capacitors behave as short circuits for signals and as open circuits for dc.

(a) If the transistor has $V_t = 1$ V, and $k_n = 4\ mA/V^2$, verify that the bias circuit establishes $V_{GS} = 1.5$ V, $I_D = 0.5$ mA, and $V_D = +7.0$ V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
(b) Find g_m and r_o if $V_A = 100$ V.
(c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.
(d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

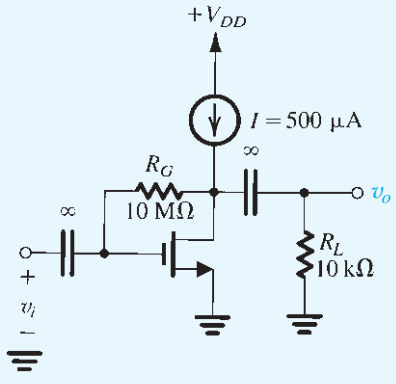


Figure P7.31

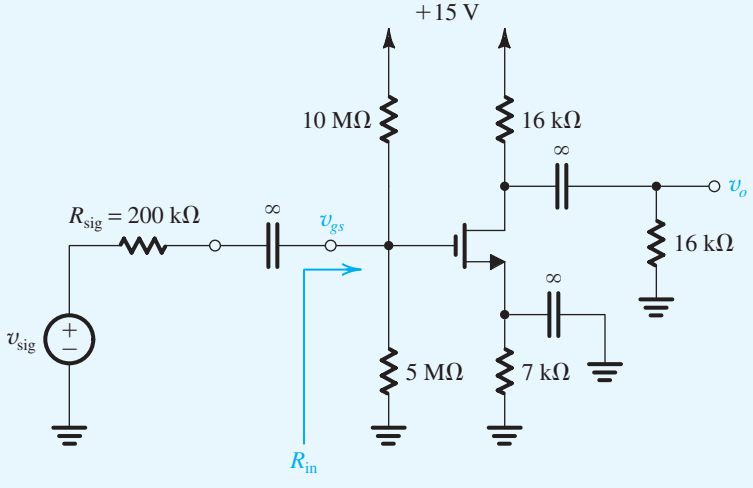


Figure P7.33

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

7.34 Consider a transistor biased to operate in the active mode at a dc collector current I_C. Calculate the collector signal current as a fraction of I_C (i.e., i_c/I_C) for input signals v_{be} of +1 mV, –1 mV, +2 mV, –2 mV, +5 mV, –5 mV, +8 mV, –8 mV, +10 mV, –10 mV, +12 mV, and –12 mV. In each case do the calculation two ways:

(a) using the exponential characteristic, and
(b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

7.35 An *npn* BJT with grounded emitter is operated with $V_{BE} = 0.700$ V, at which the collector current is 0.5 mA. A 5-kΩ resistor connects the collector to a +5-V supply. What is the resulting collector voltage V_C? Now, if a signal applied to the base raises v_{BE} to 705 mV, find the resulting total collector current i_C and total collector voltage v_C using the exponential i_C–v_{BE} relationship. For this situation, what are v_{be} and v_c? Calculate the voltage gain v_c/v_{be}. Compare with the value obtained using the small-signal approximation, that is, $-g_m R_C$.

7.36 A transistor with $\beta = 100$ is biased to operate at a dc collector current of 0.5 mA. Find the values of g_m, r_π, and r_e. Repeat for a bias current of 50 μA.

7.37 A *pnp* BJT is biased to operate at $I_C = 1.0$ mA. What is the associated value of g_m? If $\beta = 100$, what is the value of the small-signal resistance seen looking into the emitter (r_e)? Into the base (r_π)? If the collector is connected to a 5-kΩ load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

D 7.38 A designer wishes to create a BJT amplifier with a g_m of 30 mA/V and a base input resistance of 3000 Ω or more. What collector-bias current should he choose? What is the minimum β he can tolerate for the transistor used?

7.39 A transistor operating with nominal g_m of 40 mA/V has a β that ranges from 50 to 150. Also, the bias circuit, being less than ideal, allows a ±20% variation in I_C. What are the extreme values found of the resistance looking into the base?

7.40 In the circuit of Fig. 7.20, V_{BE} is adjusted so that $V_C = 1$ V. If $V_{CC} = 3$ V, $R_C = 2$ kΩ, and a signal $v_{be} = 0.005 \sin \omega t$ volts is applied, find expressions for the total instantaneous quantities $i_C(t)$, $v_C(t)$, and $i_B(t)$. The transistor has $\beta = 100$. What is the voltage gain?

D *7.41 We wish to design the amplifier circuit of Fig. 7.20 under the constraint that V_{CC} is fixed. Let the input signal $v_{be} = \hat{V}_{be} \sin \omega t$, where $\hat{V}_{be}$ is the maximum value for acceptable linearity. For the design that results in the largest signal at the collector, without the BJT leaving the active region, show that

$$R_C I_C = (V_{CC} - 0.3) \Big/ \left(1 + \frac{\hat{V}_{be}}{V_T}\right)$$

and find an expression for the voltage gain obtained. For $V_{CC} = 3$ V and $\hat{V}_{be} = 5$ mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

7.42 The table below summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifiers under various conditions. Provide the missing entries. (*Note:* Isn't it remarkable how much two parameters can reveal?)

7.43 A BJT is biased to operate in the active mode at a dc collector current of 1 mA. It has a β of 100 and V_A of 100 V. Give the four small-signal models (Figs. 7.25 and 7.27) of the BJT complete with the values of their parameters.

Transistor	a	b	c	d	e	f	g
α	1.000					0.90	
β		100		∞			
I_C (mA)	1.00		1.00				
I_E (mA)		1.00				5	
I_B (mA)			0.020				1.10
g_m (mA/V)							700
r_e (Ω)				25	100		
r_π (Ω)					10.1 kΩ		

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

7.44 Using the T model of Fig. 7.26(a), show that the input resistance between base and emitter, looking into the base, is equal to r_π.

7.45 Show that the collector current provided by the model of Fig. 7.26(b) is equal to that provided by the model in Fig. 7.26(a).

7.46 Show that the hybrid-π model of Fig. 7.24(b) is the incremental version of the large-signal model of Fig. 6.5(d).

7.47 Show that the T model of Fig. 7.26(b) is the incremental version of the large-signal model of Fig. 6.5(b).

7.48 The transistor amplifier in Fig. P7.48 is biased with a current source I and has a very high β. Find the dc voltage at the collector, V_C. Also, find the value of r_e. Replace the transistor with the T model of Fig. 7.26(b) (note that the dc current source I should be replaced with an open circuit). Hence find the voltage gain v_c/v_i.

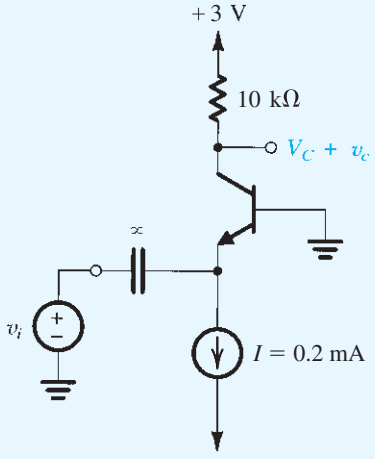


Figure P7.48

7.49 For the conceptual circuit shown in Fig. 7.23, $R_C = 2\,\text{k}\Omega$, $g_m = 50$ mA/V, and $\beta = 100$. If a peak-to-peak output voltage of 1 V is measured at the collector, what are the peak-to-peak values of v_{be} and i_b?

7.50 Figure P7.50 shows the circuit of an amplifier fed with a signal source v_{sig} with a source resistance R_{sig}. The bias circuitry is not shown. Replace the BJT with its hybrid-π equivalent circuit of Fig. 7.24(a). Find the input resistance $R_{in} \equiv v_\pi/i_b$, the voltage transmission from source to amplifier input, v_π/v_{sig}, and the voltage gain from base to collector, v_o/v_π. Use these to show that the overall voltage gain v_o/v_{sig} is given by

$$\frac{v_o}{v_{sig}} = -\frac{\beta R_C}{r_\pi + R_{sig}}$$

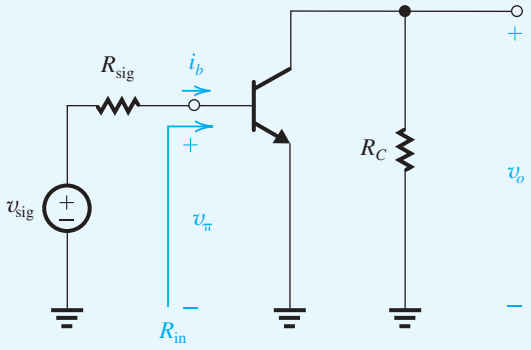


Figure P7.50

7.51 Figure P7.51 shows a transistor with the collector connected to the base. The bias arrangement is not shown. Since a zero v_{BC} implies operation in the active mode, the BJT can be replaced by one of the small-signal models of Figs. 7.24 and 7.26. Use the model of Fig. 7.26(b) and show that the resulting two-terminal device, known as a diode-connected transistor, has a small-signal resistance r equal to r_e.

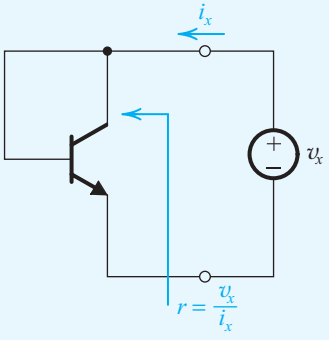


Figure P7.51

7.52 Figure P7.52 shows a particular configuration of BJT amplifiers known as "emitter follower." The bias arrangement is not shown. Replace the BJT with its T equivalent-circuit

model of Fig. 7.26(b). Show that

$$R_{\text{in}} \equiv \frac{v_i}{i_b} = (\beta + 1)(r_e + R_e)$$

$$\frac{v_o}{v_i} = \frac{R_e}{R_e + r_e}$$

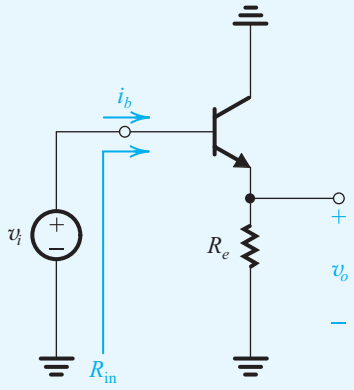


Figure P7.52

7.53 For the circuit shown in Fig. P7.53, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (use $\alpha = 0.99$). Your circuit should show the values of all components, including the model parameters. What is the input resistance R_{in}? Calculate the overall voltage gain (v_o/v_{sig}).

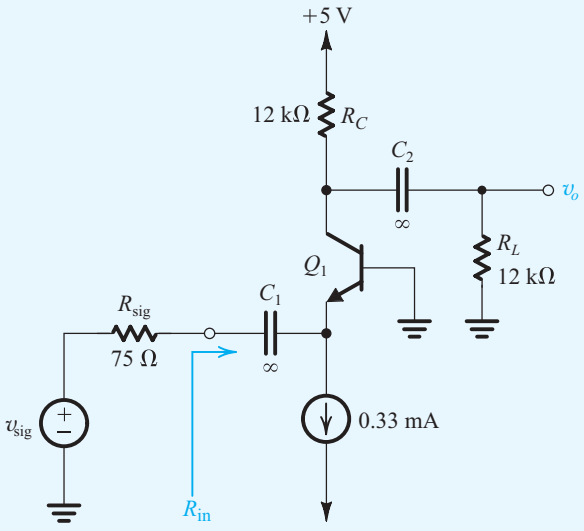


Figure P7.53

7.54 In the circuit shown in Fig. P7.54, the transistor has a β of 200. What is the dc voltage at the collector? Replacing the BJT with one of the hybrid-π models (neglecting r_o), draw the equivalent circuit of the amplifier. Find the input resistances R_{ib} and R_{in} and the overall voltage gain (v_o/v_{sig}). For an output signal of ±0.4 V, what values of v_{sig} and v_b are required?

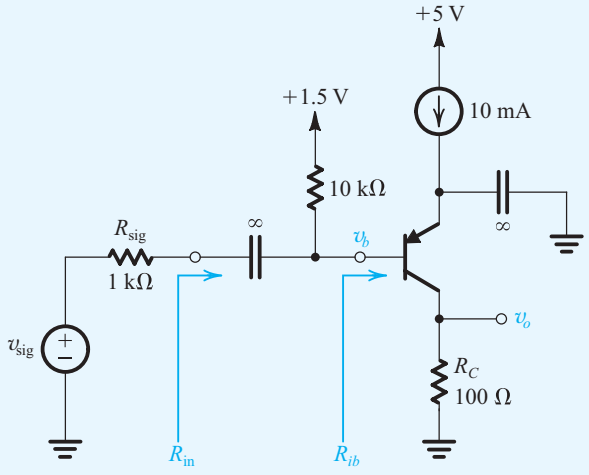


Figure P7.54

7.55 Consider the augmented hybrid-π model shown in Fig. 7.25(a). Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for $V_A = 25$ V and $V_A = 125$ V.

D 7.56 Redesign the circuit of Fig. 7.30(a) by raising the resistor values by a factor n to increase the resistance seen by the input v_i to 75 Ω. What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be "matched" to the equivalent resistances of the interconnecting cables.

D *7.57 Design an amplifier using the configuration of Fig. 7.30(a). The power supplies available are ±5 V. The input signal source has a resistance of 50 Ω, and it is required that the amplifier input resistance match this value. (Note that $R_{\text{in}} = r_e \| R_E \simeq r_e$.) The amplifier is to have the greatest possible voltage gain and the largest possible output signal but retain small-signal linear operation (i.e., the signal component across the base–emitter junction should be limited to no more

than 10 mV). Find appropriate values for R_E and R_C. What is the value of voltage gain realized from signal source to output?

***7.58** The transistor in the circuit shown in Fig. P7.58 is biased to operate in the active mode. Assuming that β is very large, find the collector bias current I_C. Replace the transistor with the small-signal equivalent-circuit model of Fig. 7.26(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

$$\frac{v_{o1}}{v_i} = \frac{R_E}{R_E + r_e}$$
$$\frac{v_{o2}}{v_i} = \frac{-\alpha R_C}{R_E + r_e}$$

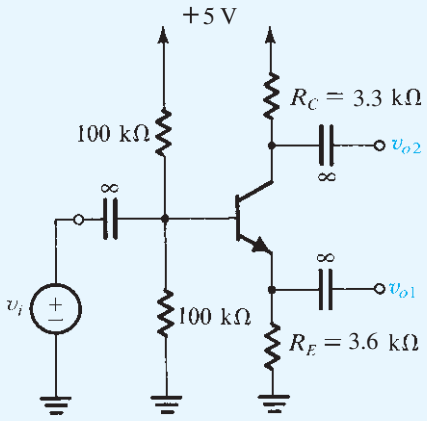


Figure P7.58

Find the values of these voltage gains (for $\alpha \simeq 1$). Now, if the terminal labeled v_{o1} is connected to ground, what does the voltage gain v_{o2}/v_i become?

Section 7.3: Basic Configurations

7.59 An amplifier with an input resistance of 100 kΩ, an open-circuit voltage gain of 100 V/V, and an output resistance of 100 Ω is connected between a 20-kΩ signal source and a 2-kΩ load. Find the overall voltage gain G_v. Also find the current gain, defined as the ratio of the load current to the current drawn from the signal source.

D 7.60 Specify the parameters R_{in}, A_{vo}, and R_o of an amplifier that is to be connected between a 100-kΩ source and a 2-kΩ load and is required to meet the following specifications:

(a) No more than 5% of the signal strength is lost in the connection to the amplifier input;
(b) If the load resistance changes from the nominal value of 2 kΩ to a low value of 1 kΩ, the change in output voltage is limited to 5% of nominal value; and
(c) The nominal overall voltage gain is 10 V/V.

7.61 Figure P7.61 shows an alternative equivalent-circuit representation of an amplifier. If this circuit is to be equivalent to that in Fig. 7.34(b) show that $G_m = A_{vo}/R_o$. Also convince yourself that the transconductance G_m is defined as

$$G_m = \left.\frac{i_o}{v_i}\right|_{R_L=0}$$

and hence is known as the short-circuit transconductance. Now, if the amplifier is fed with a signal source $(v_{\text{sig}}, R_{\text{sig}})$ and is connected to a load resistance R_L show that the gain of the amplifier proper A_v is given by $A_v = G_m(R_o \parallel R_L)$ and the overall voltage gain G_v is given by

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} G_m (R_o \parallel R_L)$$

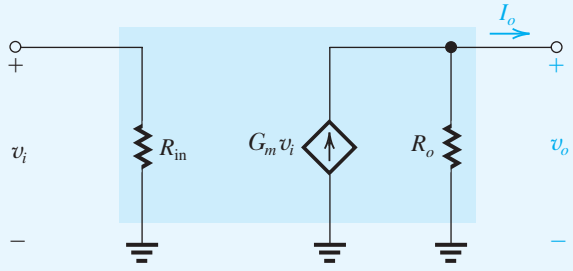


Figure P7.61

7.62 An alternative equivalent circuit of an amplifier fed with a signal source $(v_{\text{sig}}, R_{\text{sig}})$ and connected to a load R_L is shown in Fig. P7.62. Here G_{vo} is the open-circuit overall voltage gain,

$$G_{vo} = \left.\frac{v_o}{v_{\text{sig}}}\right|_{R_L=\infty}$$

and R_{out} is the output resistance with v_{sig} set to zero. This is different than R_o. Show that

$$G_{vo} = \frac{R_i}{R_i + R_{sig}} A_{vo}$$

where $R_i = R_{in}\big|_{R_L=\infty}$.

Also show that the overall voltage gain is

$$G_v = G_{vo} \frac{R_L}{R_L + R_{out}}$$

**7.63 Most practical amplifiers have internal feedback that make them non-unilateral. In such a case, R_{in} depends on R_L. To illustrate this point we show in Fig. P7.63 the equivalent circuit of an amplifier where a feedback resistance R_f models the internal feedback mechanism that is present in this amplifier. It is R_f that makes the amplifier non-unilateral. Show that

$$R_{in} = R_1 \| \left[\frac{R_f + (R_2 \| R_L)}{1 + g_m (R_2 \| R_L)} \right]$$

$$A_{vo} = -g_m R_2 \frac{1 - 1/(g_m R_f)}{1 + (R_2/R_f)}$$

$$R_o = R_2 \| R_f$$

Evaluate R_{in}, A_{vo}, and R_o for the case $R_1 = 100\,\text{k}\Omega$, $R_f = 1\,\text{M}\Omega$, $g_m = 100\,\text{mA/V}$, $R_2 = 100\ \Omega$, and $R_L = 1\,\text{k}\Omega$. Which of the amplifier characteristic parameters is most affected by R_f (that is, relative to the case with $R_f = \infty$)? For $R_{sig} = 100\,\text{k}\Omega$ determine the overall voltage gain, G_v, with and without R_f present.

7.64 Calculate the overall voltage gain of a CS amplifier fed with a 1-MΩ source and connected to a 10-kΩ load. The MOSFET has $g_m = 2\,\text{mA/V}$, and a drain resistance $R_D = 10\,\text{k}\Omega$ is utilized.

7.65 A CS amplifier utilizes a MOSFET with $\mu_n C_{ox} = 400\,\mu\text{A/V}^2$ and $W/L = 10$. It is biased at $I_D = 320\,\mu\text{A}$ and uses $R_D = 10\,\text{k}\Omega$. Find R_{in}, A_{vo}, and R_o. Also, if a load resistance of $10\,\text{k}\Omega$ is connected to the output, what overall voltage gain G_v is realized? Now, if a 0.2-V peak sine-wave signal is required at the output, what must the peak amplitude of v_{sig} be?

7.66 A common-source amplifier utilizes a MOSFET operated at $V_{OV} = 0.25\,\text{V}$. The amplifier feeds a load resistance $R_L = 15\,\text{k}\Omega$. The designer selects $R_D = 2R_L$. If it is required to realize an overall voltage gain G_v of $-10\,\text{V/V}$ what g_m is needed? Also specify the bias current I_D. If, to increase the output signal swing, R_D is reduced to $R_D = R_L$, what does G_v become?

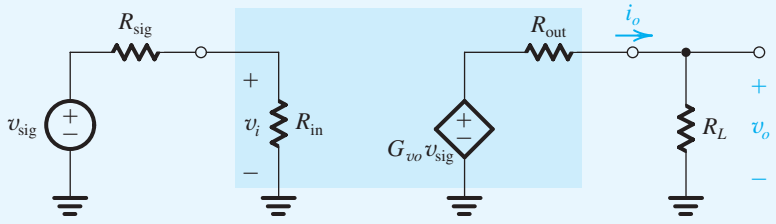


Figure P7.62

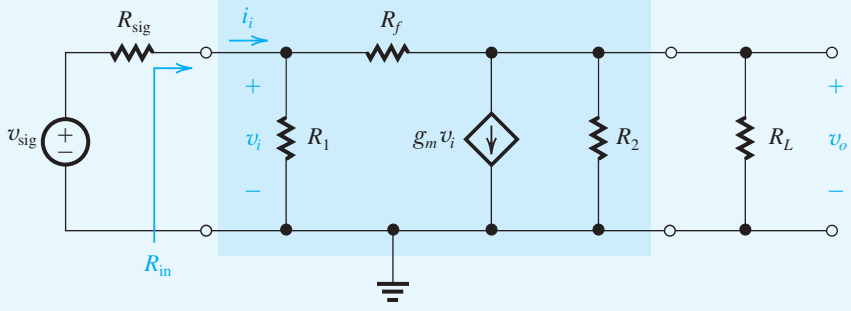


Figure P7.63

7.67 Two identical CS amplifiers are connected in cascade. The first stage is fed with a source v_{sig} having a resistance $R_{sig} = 200\,\text{k}\Omega$. A load resistance $R_L = 10\,\text{k}\Omega$ is connected to the drain of the second stage. Each MOSFET is biased at $I_D = 0.3\,\text{mA}$ and operates with $V_{OV} = 0.2\,\text{V}$. Each stage utilizes a drain resistance $R_D = 10\,\text{k}\Omega$.

(a) Sketch the equivalent circuit of the two-stage amplifier.
(b) Calculate the overall voltage gain G_v.

7.68 A CE amplifier utilizes a BJT with $\beta = 100$ biased at $I_C = 0.5\,\text{mA}$; it has a collector resistance $R_C = 10\,\text{k}\Omega$. Find R_{in}, R_o, and A_{vo}. If the amplifier is fed with a signal source having a resistance of $10\,\text{k}\Omega$, and a load resistance $R_L = 10\,\text{k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v. If the peak voltage of the sine wave appearing between base and emitter is to be limited to 5 mV, what $\hat{v}_{sig}$ is allowed, and what output voltage signal appears across the load?

D ***7.69** In this problem we investigate the effect of the inevitable variability of β on the realized gain of the CE amplifier. For this purpose, use the overall gain expression in Eq. (7.114).

$$|G_v| = \frac{R_L'}{(R_{sig}/\beta) + (1/g_m)}$$

where $R_L' = R_L \,\|\, R_C$.

Consider the case $R_L' = 10\,\text{k}\Omega$ and $R_{sig} = 10\,\text{k}\Omega$, and let the BJT be biased at $I_C = 1\,\text{mA}$. The BJT has a nominal β of 100.

(a) What is the nominal value of $|G_v|$?
(b) If β can be anywhere between 50 and 150, what is the corresponding range of $|G_v|$?
(c) If in a particular design, it is required to maintain $|G_v|$ within $\pm 20\%$ of its nominal value, what is the maximum allowable range of β?
(d) If it is not possible to restrict β to the range found in (c), and the designer has to contend with β in the range 50 to 150, what value of bias current I_C would result in $|G_v|$ falling in a range of $\pm 20\%$ of a new nominal value? What is the nominal value of $|G_v|$ in this case?

7.70 Two identical CE amplifiers are connected in cascade. The first stage is fed with a source v_{sig} having a resistance $R_{sig} = 10\,\text{k}\Omega$. A load resistance $R_L = 10\,\text{k}\Omega$ is connected to the collector of the second stage. Each BJT is biased at $I_C = 0.25\,\text{mA}$ and has $\beta = 100$. Each stage utilizes a collector resistance $R_C = 10\,\text{k}\Omega$.

(a) Sketch the equivalent circuit of the two-stage amplifier.
(b) Find the overall voltage gain, v_{o2}/v_{sig}.

7.71 A MOSFET connected in the CS configuration has a transconductance $g_m = 5\,\text{mA/V}$. When a resistance R_s is connected in the source lead, the effective transconductance is reduced to 2 mA/V. What do you estimate the value of R_s to be?

7.72 A CS amplifier using an NMOS transistor with $g_m = 2\,\text{mA/V}$ is found to have an overall voltage gain of $-10\,\text{V/V}$. What value should a resistance R_s inserted in the source lead have to reduce the overall voltage gain to $-5\,\text{V/V}$?

7.73 The overall voltage gain of a CS amplifier with a resistance $R_s = 0.5\,\text{k}\Omega$ in the source lead was measured and found to be $-10\,\text{V/V}$. When R_s was shorted, but the circuit operation remained linear, the gain doubled. What must g_m be? What value of R_s is needed to obtain an overall voltage gain of $-16\,\text{V/V}$?

7.74 A CE amplifier utilizes a BJT with $\beta = 100$ biased at $I_C = 0.5\,\text{mA}$ and has a collector resistance $R_C = 12\,\text{k}\Omega$ and a resistance $R_e = 250\,\Omega$ connected in the emitter. Find R_{in}, A_{vo}, and R_o. If the amplifier is fed with a signal source having a resistance of $10\,\text{k}\Omega$, and a load resistance $R_L = 12\,\text{k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v. If the peak voltage of the sine wave appearing between base and emitter is to be limited to 5 mV, what $\hat{v}_{sig}$ is allowed, and what output voltage signal appears across the load?

D **7.75** Design a CE amplifier with a resistance R_e in the emitter to meet the following specifications:

(i) Input resistance $R_{in} = 15\,\text{k}\Omega$.
(ii) When fed from a signal source with a peak amplitude of 0.15 V and a source resistance of $30\,\text{k}\Omega$, the peak amplitude of v_π is 5 mV.

Specify R_e and the bias current I_C. The BJT has $\beta = 74$. If the total resistance in the collector is $6\,\text{k}\Omega$, find the overall voltage gain G_v and the peak amplitude of the output signal v_o.

SIM **D** **7.76** Inclusion of an emitter resistance R_e reduces the variability of the gain G_v due to the inevitable wide variance in the value of β. Consider a CE amplifier operating between a signal source with $R_{sig} = 10\,\text{k}\Omega$ and a total collector resistance $R_C \,\|\, R_L$ of $10\,\text{k}\Omega$. The BJT is biased at $I_C = 1\,\text{mA}$ and its β is specified to be nominally 100 but can lie in the range of 50 to 150. First determine the nominal value and the range of

$|G_v|$ without resistance R_e. Then select a value for R_e that will ensure that $|G_v|$ be within ±20% of its new nominal value. Specify the value of R_e, the new nominal value of $|G_v|$, and the expected range of $|G_v|$.

7.77 A CG amplifier using an NMOS transistor for which $g_m = 2$ mA/V has a 5-kΩ drain resistance R_D and a 5-kΩ load resistance R_L. The amplifier is driven by a voltage source having a 750-Ω resistance. What is the input resistance of the amplifier? What is the overall voltage gain G_v ? By what factor must the bias current I_D of the MOSFET be changed so that R_{in} matches R_{sig}?

7.78 A CG amplifier when fed with a signal source having $R_{sig} = 100$ Ω is found to have an overall voltage gain of 12 V/V. When a 100-Ω resistance was added in series with the signal generator the overall voltage gain decreased to 10 V/V. What must g_m of the MOSFET be? If the MOSFET is biased at $I_D = 0.25$ mA, at what overdrive voltage must it be operating?

D 7.79 A CB amplifier is operating with $R_L = 10$ kΩ, $R_C = 10$ kΩ, and $R_{sig} = 50$ Ω. At what current I_C should the transistor be biased for the input resistance R_{in} to equal that of the signal source? What is the resulting overall voltage gain? Assume $\alpha \simeq 1$.

7.80 For the circuit in Fig. P7.80, let $R_{sig} \gg r_e$ and $\alpha \simeq 1$. Find v_o.

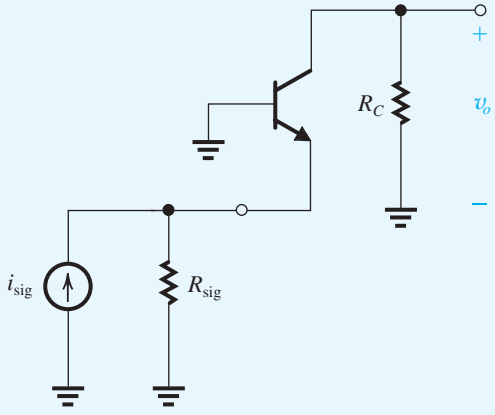


Figure P7.80

7.81 A CB amplifier is biased at $I_E = 0.2$ mA with $R_C = R_L = 10$ kΩ and is driven by a signal source with $R_{sig} = 0.5$ kΩ. Find the overall voltage gain G_v. If the maximum signal amplitude of the voltage between base and emitter is limited to 10 mV, what are the corresponding amplitudes of v_{sig} and v_o? Assume $\alpha \simeq 1$.

7.82 A source follower is required to connect a high-resistance source to a load whose resistance is nominally 2 kΩ but can be as low as 1.5 kΩ and as high as 5 kΩ. What is the maximum output resistance that the source follower must have if the output voltage is to remain within ±10% of nominal value? If the MOSFET has $k_n = 2.5$ mA/V^2, at what current I_D must it be biased? At what overdrive voltage is the MOSFET operating?

D 7.83 A source follower is required to deliver a 0.5-V peak sinusoid to a 2-kΩ load. If the peak amplitude of v_{gs} is to be limited to 50 mV, and the MOSFET transconductance parameter k_n is 5 mA/V^2, what is the lowest value of I_D at which the MOSFET can be biased? At this bias current, what are the maximum and minimum currents that the MOSFET will be conducting (at the positive and negative peaks of the output sine wave)? What must the peak amplitude of v_{sig} be?

D 7.84 An emitter follower is required to deliver a 0.5-V peak sinusoid to a 2-kΩ load. If the peak amplitude of v_{be} is to be limited to 5 mV, what is the lowest value of I_E at which the BJT can be biased? At this bias current, what are the maximum and minimum currents that the BJT will be conducting (at the positive and negative peaks of the output sine wave)? If the resistance of the signal source is 200 kΩ, what value of G_v is obtained? Thus determine the required amplitude of v_{sig}. Assume $\beta = 100$.

7.85 An emitter follower with a BJT biased at $I_C = 2$ mA and having $\beta = 100$ is connected between a source with $R_{sig} = 10$ kΩ and a load $R_L = 0.5$ kΩ.

(a) Find R_{in}, v_b/v_{sig}, and v_o/v_{sig}.
(b) If the signal amplitude across the base–emitter junction is to be limited to 10 mV, what is the corresponding amplitude of v_{sig} and v_o?
(c) Find the open-circuit voltage gain G_{vo} and the output resistance R_{out}. Use these values first to verify the value of G_v obtained in (a), then to find the value of G_v obtained with R_L reduced to 250 Ω.

7.86 An emitter follower is operating at a collector bias current of 0.5 mA and is used to connect a 10-kΩ source to a 1-kΩ load. If the nominal value of β is 100, what output resistance R_{out} and overall voltage gain G_v result? Now if

transistor β is specified to lie in the range 50 to 150, find the corresponding range of R_{out} and G_v.

7.87 An emitter follower, when driven from a 5-kΩ source, was found to have an output resistance R_{out} of 150 Ω. The output resistance increased to 250 Ω when the source resistance was increased to 10 kΩ. Find the overall voltage gain when the follower is driven by a 10-kΩ source and loaded by a 1-kΩ resistor.

7.88 For the general amplifier circuit shown in Fig. P7.88 neglect the Early effect.

(a) Find expressions for v_c/v_{sig} and v_e/v_{sig}.
(b) If v_{sig} is disconnected from node X, node X is grounded, and node Y is disconnected from ground and connected to v_{sig}, find the new expression for v_c/v_{sig}.

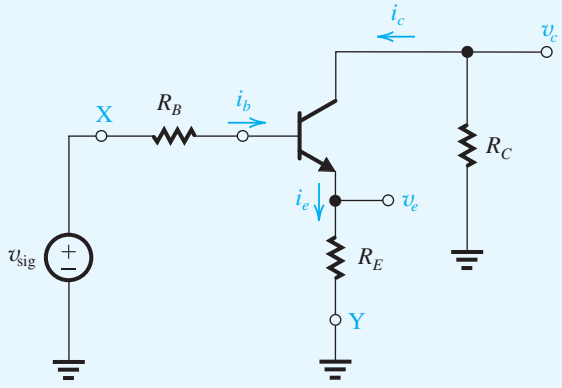


Figure P7.88

7.89 When the Early effect is neglected, the overall voltage gain of a CE amplifier with a collector resistance $R_C = 10$ kΩ is calculated to be −100 V/V. If the BJT is biased at $I_C = 1$ mA and the Early voltage is 100 V, provide a better estimate of the voltage gain G_v.

***7.90** Show that when r_o is taken into account, the voltage gain of the source follower becomes

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

Now, with R_L removed, the voltage gain is carefully measured and found to be 0.98. Then, when R_L is connected and its value is varied, it is found that the gain is halved at $R_L = 500$ Ω. If the amplifier remained linear throughout this measurement, what must the values of g_m and r_o be?

D 7.91 In this problem, we investigate the effect of changing the bias current I_C on the overall voltage gain G_v of a CE amplifier. Consider the situation of a CE amplifier operating with a signal source having $R_{sig} = 10$ kΩ and having $R_C || R_L = 10$ kΩ. The BJT is specified to have $\beta = 100$ and $V_A = 25$ V. Use Eq. (7.114) (with r_o included in parallel with R_C and R_L in the numerator) to find $|G_v|$ at $I_C = 0.1$ mA, 0.2 mA, 0.5 mA, 1.0 mA, and 1.25 mA. Observe the effect of r_o on limiting $|G_v|$ as I_C is increased. Find the value of I_C that results in $|G_v| = 50$ V/V.

Section 7.4: Biasing

D 7.92 Consider the classical biasing scheme shown in Fig. 7.48(c), using a 9-V supply. For the MOSFET, $V_t = 1$ V, $\lambda = 0$, and $k_n = 2$ mA/V^2. Arrange that the drain current is 1 mA, with about one-third of the supply voltage across each of R_S and R_D. Use 22 MΩ for the larger of R_{G1} and R_{G2}. What are the values of R_{G1}, R_{G2}, R_S, and R_D that you have chosen? Specify them to two significant digits. For your design, how far is the drain voltage from the edge of saturation?

D 7.93 Using the circuit topology displayed in Fig. 7.48(e), arrange to bias the NMOS transistor at $I_D = 0.5$ mA with V_D midway between cutoff and the beginning of triode operation. The available supplies are ±5 V. For the NMOS transistor, $V_t = 1.0$ V, $\lambda = 0$, and $k_n = 1$ mA/V^2. Use a gate-bias resistor of 10 MΩ. Specify R_S and R_D to two significant digits.

D *7.94 In an electronic instrument using the biasing scheme shown in Fig. 7.48(c), a manufacturing error reduces R_S to zero. Let $V_{DD} = 15$ V, $R_{G1} = 10$ MΩ, and $R_{G2} = 5.1$ MΩ. What is the value of V_G created? If supplier specifications allow k_n to vary from 0.2 to 0.3 mA/V^2 and V_t to vary from 1.0 V to 1.5 V, what are the extreme values of I_D that may result? What value of R_S should have been installed to limit the maximum value of I_D to 1.5 mA? Choose an appropriate standard 5% resistor value (refer to Appendix J). What extreme values of current now result?

7.95 An NMOS transistor is connected in the bias circuit of Fig. 7.48(c), with $V_G = 5$ V and $R_S = 3$ kΩ. The transistor has $V_t = 1$ V and $k_n = 2$ mA/V^2. What bias current results? If a transistor for which k_n is 50% higher is used, what is the resulting percentage increase in I_D?

SIM 7.96 The bias circuit of Fig. 7.48(c) is used in a design with $V_G = 5$ V and $R_S = 2$ kΩ. For a MOSFET with

$k_n = 2\ \text{mA/V}^2$, the source voltage was measured and found to be 2 V. What must V_t be for this device? If a device for which V_t is 0.5 V less is used, what does V_S become? What bias current results?

D 7.97 Design the circuit of Fig. 7.48(e) for a MOSFET having $V_t = 1$ V and $k_n = 4\ \text{mA/V}^2$. Let $V_{DD} = V_{SS} = 5$ V. Design for a dc bias current of 0.5 mA and for the largest possible voltage gain (and thus the largest possible R_D) consistent with allowing a 2-V peak-to-peak voltage swing at the drain. Assume that the signal voltage on the source terminal of the FET is zero.

SIM **D 7.98** Design the circuit in Fig. P7.98 so that the transistor operates in saturation with V_D biased 1 V from the edge of the triode region, with $I_D = 1$ mA and $V_D = 3$ V, for each of the following two devices (use a 10-μA current in the voltage divider):

(a) $|V_t| = 1$ V and $k_p' W/L = 0.5\ \text{mA/V}^2$
(b) $|V_t| = 2$ V and $k_p' W/L = 1.25\ \text{mA/V}^2$

For each case, specify the values of V_G, V_D, V_S, R_1, R_2, R_S, and R_D.

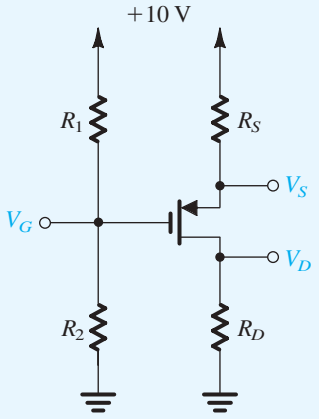


Figure P7.98

D **7.99 A very useful way to characterize the stability of the bias current I_D is to evaluate the sensitivity of I_D relative to a particular transistor parameter whose variability might be large. The sensitivity of I_D relative to the MOSFET parameter $K \equiv \frac{1}{2}k'(W/L)$ is defined as

$$S_K^{I_D} \equiv \frac{\partial I_D/I_D}{\partial K/K} = \frac{\partial I_D}{\partial K}\frac{K}{I_D}$$

and its value, when multiplied by the variability (or tolerance) of K, provides the corresponding expected variability of I_D,

$$\frac{\Delta I_D}{I_D} = S_K^{I_D}\left(\frac{\Delta K}{K}\right)$$

The purpose of this problem is to investigate the use of the sensitivity function in the design of the bias circuit of Fig. 7.48(e).

(a) Show that for V_t constant,

$$S_K^{I_D} = 1\Big/\left(1 + 2\sqrt{KI_D}R_S\right)$$

(b) For a MOSFET having $K = 100\ \mu\text{A/V}^2$ with a variability of ±10% and $V_t = 1$ V, find the value of R_S that would result in $I_D = 100\ \mu$A with a variability of ±1%. Also, find V_{GS} and the required value of V_{SS}.
(c) If the available supply $V_{SS} = 5$ V, find the value of R_S for $I_D = 100\ \mu$A. Evaluate the sensitivity function, and give the expected variability of I_D in this case.

D **7.100 The variability ($\Delta I_D/I_D$) in the bias current I_D due to the variability ($\Delta V_t/V_t$) in the threshold voltage V_t can be evaluated from

$$\frac{\Delta I_D}{I_D} = S_{V_t}^{I_D}\left(\frac{\Delta V_t}{V_t}\right)$$

where $S_{V_t}^{I_D}$, the sensitivity of I_D relative to V_t, is defined as

$$S_{V_t}^{I_D} = \frac{\partial I_D}{\partial V_t}\frac{V_t}{I_D}$$

(a) For the case of a MOSFET biased with a fixed V_{GS}, show that

$$S_{V_t}^{I_D} = -\frac{2V_t}{V_{OV}}$$

and find the variability in I_D for $V_t = 0.5$ V and $\Delta V_t/V_t = \pm 5\%$. Let the MOSFET be biased at $V_{OV} = 0.25$ V.
(b) For the case of a MOSFET biased with a fixed gate voltage V_G and a resistance R_S included in the source lead, show that

$$S_{V_t}^{I_D} = -\frac{2V_t}{V_{OV} + 2I_D R_S}$$

For the same parameters given in (a), find the required value of $(I_D R_S)$ and V_G to limit $\Delta I_D/I_D$ to ±5%. What value of R_S is needed if I_D is 100 μA?

SIM 7.101 In the circuit of Fig. 7.50, let $R_G = 10\ \text{M}\Omega$, $R_D = 10\ \text{k}\Omega$, and $V_{DD} = 10\ \text{V}$. For each of the following two transistors, find the voltages V_D and V_G.

(a) $V_t = 1\ \text{V}$ and $k_n = 0.5\ \text{mA/V}^2$
(b) $V_t = 2\ \text{V}$ and $k_n = 1.25\ \text{mA/V}^2$

D 7.102 Using the feedback bias arrangement shown in Fig. 7.50 with a 5-V supply and an NMOS device for which $V_t = 1\ \text{V}$ and $k_n = 10\ \text{mA/V}^2$, find R_D to establish a drain current of 0.2 mA.

D 7.103 Figure P7.103 shows a variation of the feedback-bias circuit of Fig. 7.50. Using a 5-V supply with an NMOS transistor for which $V_t = 0.8\ \text{V}$, $k_n = 8\ \text{mA/V}^2$, and $\lambda = 0$, provide a design that biases the transistor at $I_D = 1\ \text{mA}$, with V_{DS} large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use 22 MΩ as the largest resistor in the feedback-bias network. What values of R_D, R_{G1}, and R_{G2} have you chosen? Specify all resistors to two significant digits.

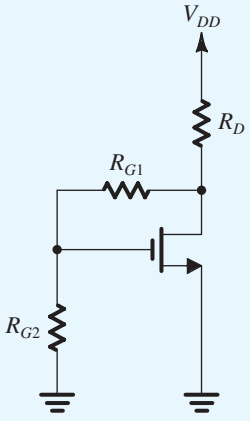


Figure P7.103

D 7.104 For the circuit in Fig. 7.51(a), neglect the base current I_B in comparison with the current in the voltage divider. It is required to bias the transistor at $I_C = 1\ \text{mA}$, which requires selecting R_{B1} and R_{B2} so that $V_{BE} = 0.710\ \text{V}$. If $V_{CC} = 3\ \text{V}$, what must the ratio R_{B1}/R_{B2} be? Now, if R_{B1} and R_{B2} are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for V_{BE}? What is the corresponding range of I_C? If $R_C = 2\ \text{k}\Omega$, what is the range obtained for V_{CE}? Comment on the efficacy of this biasing arrangement.

D 7.105 It is required to bias the transistor in the circuit of Fig. 7.51(b) at $I_C = 1\ \text{mA}$. The transistor β is specified to be nominally 100, but it can fall in the range of 50 to 150. For $V_{CC} = +3\ \text{V}$ and $R_C = 2\ \text{k}\Omega$, find the required value of R_B to achieve $I_C = 1\ \text{mA}$ for the "nominal" transistor. What is the expected range for I_C and V_{CE}? Comment on the efficacy of this bias design.

D 7.106 Consider the single-supply bias network shown in Fig. 7.52(a). Provide a design using a 9-V supply in which the supply voltage is equally split between R_C, V_{CE}, and R_E with a collector current of 0.6 mA. The transistor β is specified to have a minimum value of 90. Use a voltage-divider current of $I_E/10$, or slightly higher. Since a reasonable design should operate for the best transistors for which β is very high, do your initial design with $\beta = \infty$. Then choose suitable 5% resistors (see Appendix J), making the choice in a way that will result in a V_{BB} that is slightly higher than the ideal value. Specify the values you have chosen for R_E, R_C, R_1, and R_2. Now, find V_B, V_E, V_C, and I_C for your final design using $\beta = 90$.

D 7.107 Repeat Problem 7.106, but use a voltage-divider current that is $I_E/2$. Check your design at $\beta = 90$. If you have the data available, find how low β can be while the value of I_C does not fall below that obtained with the design of Problem 7.106 for $\beta = 90$.

D *7.108 It is required to design the bias circuit of Fig. 7.52 for a BJT whose nominal $\beta = 100$.

(a) Find the largest ratio (R_B/R_E) that will guarantee I_E remains within ±5% of its nominal value for β as low as 50 and as high as 150.
(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BB} \equiv V_{CC}R_2/(R_1 + R_2)$ that will result in a voltage drop of $V_{CC}/3$ across R_E.
(c) For $V_{CC} = 5\ \text{V}$, find the required values of R_1, R_2, and R_E to obtain $I_E = 0.5\ \text{mA}$ and to satisfy the requirement for stability of I_E in (a).
(d) Find R_C so that $V_{CE} = 1.0\ \text{V}$ for β equal to its nominal value.

Check your design by evaluating the resulting range of I_E.

D *7.109 Consider the two-supply bias arrangement shown in Fig. 7.53 using ±5-V supplies. It is required to design the circuit so that $I_C = 0.5$ mA and V_C is placed 2 V above V_E.

(a) For $\beta = \infty$, what values of R_E and R_C are required?
(b) If the BJT is specified to have a minimum β of 50, find the largest value for R_B consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across R_E.
(c) What standard 5% resistor values (see Appendix J) would you use for R_B, R_E, and R_C? In making your selection, use somewhat lower values in order to compensate for the low-β effects.
(d) For the values you selected in (c), find I_C, V_B, V_E, and V_C for $\beta = \infty$ and for $\beta = 50$.

D *7.110 Utilizing ±3-V power supplies, it is required to design a version of the circuit in Fig. 7.53 in which the signal will be coupled to the emitter and thus R_B can be set to zero. Find values for R_E and R_C so that a dc emitter current of 0.4 mA is obtained and so that the gain is maximized while allowing ±1 V of signal swing at the collector. If temperature increases from the nominal value of 25°C to 125°C, estimate the percentage change in collector bias current. In addition to the –2 mV/°C change in V_{BE}, assume that the transistor β changes over this temperature range from 50 to 150.

SIM **D 7.111** Using a 3-V power supply, design a version of the circuit of Fig. 7.54 to provide a dc emitter current of 0.5 mA and to allow a ±1-V signal swing at the collector. The BJT has a nominal $\beta = 100$. Use standard 5% resistor values (see Appendix J). If the actual BJT used has $\beta = 50$, what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for $\beta = 150$.

D *7.112 (a) Using a 3-V power supply, design the feedback bias circuit of Fig. 7.54 to provide $I_C = 1$ mA and $V_C = V_{CC}/2$ for $\beta = 100$.
(b) Select standard 5% resistor values, and reevaluate V_C and I_C for $\beta = 100$.
(c) Find V_C and I_C for $\beta = \infty$.
(d) To improve the situation that obtains when high-β transistors are used, we have to arrange for an additional current to flow through R_B. This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P7.112. Design this circuit for $\beta = 100$. Use a current through R_{B2} equal to the base current. Now, what values of V_C and I_C result with $\beta = \infty$?

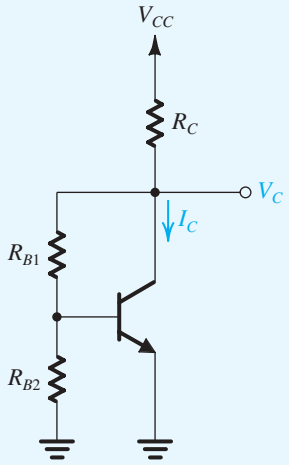


Figure P7.112

D 7.113 A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P7.113. Find the values of I and R_B to bias the BJT at $I_C = 1$ mA and $V_C = 1.5$ V. Let $\beta = 100$.

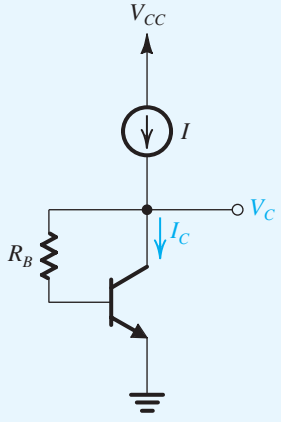


Figure P7.113

7.114 The circuit in Fig. P7.114 provides a constant current I_o as long as the circuit to which the collector is

connected maintains the BJT in the active mode. Show that

$$I_O = \alpha \frac{V_{CC}[R_2/(R_1+R_2)] - V_{BE}}{R_E + (R_1 \| R_2)/(\beta+1)}$$

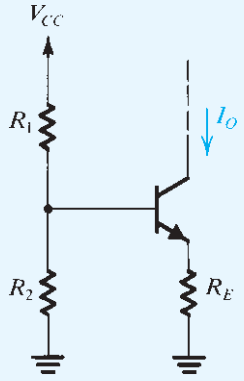


Figure P7.114

SIM **D *7.115** For the circuit in Fig. P7.115, assuming all transistors to be identical with β infinite, derive an expression for the output current I_O, and show that by selecting

$$R_1 = R_2$$

and keeping the current in each junction the same, the current I_O will be

$$I_O = \frac{V_{CC}}{2R_E}$$

which is independent of V_{BE}. What must the relationship of R_E to R_1 and R_2 be? For $V_{CC} = 10$ V and $V_{BE} = 0.7$ V, design the circuit to obtain an output current of 0.5 mA. What is the lowest voltage that can be applied to the collector of Q_3?

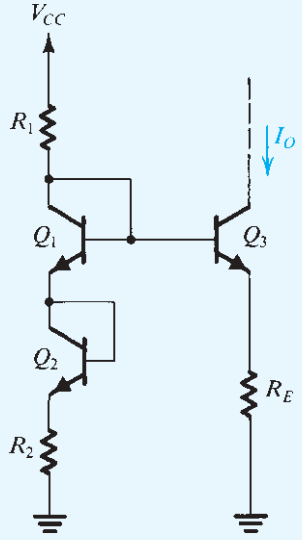


Figure P7.115

D 7.116 For the circuit in Fig. P7.116 find the value of R that will result in $I_O \simeq 0.5$ mA. What is the largest voltage that can be applied to the collector? Assume $|V_{BE}| = 0.7$ V.

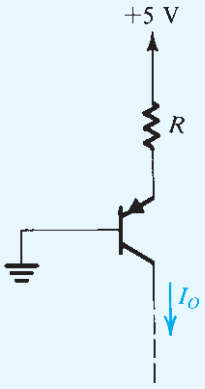


Figure P7.116

Section 7.5: Discrete-Circuit Amplifiers

7.117 Calculate the overall voltage gain G_v of a common-source amplifier for which $g_m = 3$ mA/V, $r_o = 100$ kΩ, $R_D = 10$ kΩ, and $R_G = 10$ MΩ. The amplifier is fed from a signal source with a Thévenin resistance of 1 MΩ, and the amplifier output is coupled to a load resistance of 20 kΩ.

SIM **7.118** The NMOS transistor in the CS amplifier shown in Fig. P7.118 has $V_t = 0.7$ V and $V_A = 50$ V.

(a) Neglecting the Early effect, verify that the MOSFET is operating in saturation with $I_D = 0.5$ mA and $V_{OV} = 0.3$ V. What must the MOSFET's k_n be? What is the dc voltage at the drain?
(b) Find R_{in} and G_v.
(c) If v_{sig} is a sinusoid with a peak amplitude $\hat{v}_{sig}$, find the maximum allowable value of $\hat{v}_{sig}$ for which the transistor remains in saturation. What is the corresponding amplitude of the output voltage?

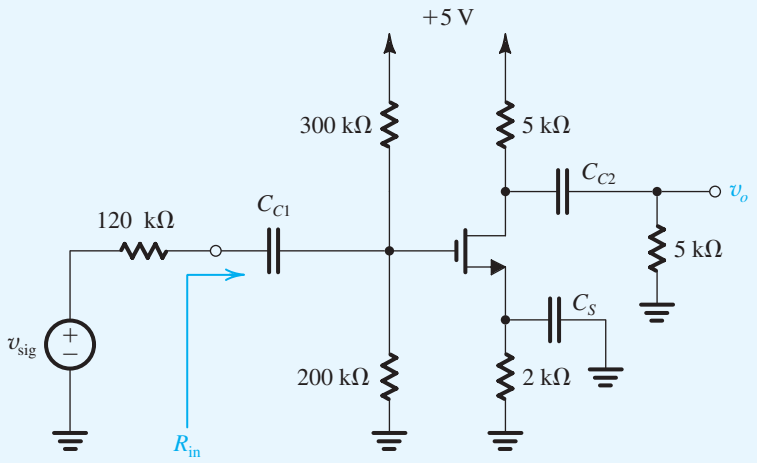


Figure P7.118

(d) What is the value of resistance R_s that needs to be inserted in series with capacitor C_S in order to allow us to double the input signal $\hat{v}_{sig}$? What output voltage now results?

SIM **D *7.119** The PMOS transistor in the CS amplifier of Fig. P7.119 has $V_{tp} = -0.7$ V and a very large $|V_A|$.

(a) Select a value for R_S to bias the transistor at $I_D = 0.3$ mA and $|V_{OV}| = 0.3$ V. Assume v_{sig} to have a zero dc component.

(b) Select a value for R_D that results in $G_v = -10$ V/V.

(c) Find the largest sinusoid $\hat{v}_{sig}$ that the amplifier can handle while remaining in the saturation region. What is the corresponding signal at the output?

(d) If to obtain reasonably linear operation, $\hat{v}_{sig}$ is limited to 50 mV, what value can R_D be increased to while maintaining saturation-region operation? What is the new value of G_v?

7.120 Figure P7.120 shows a scheme for coupling and amplifying a high-frequency pulse signal. The circuit utilizes

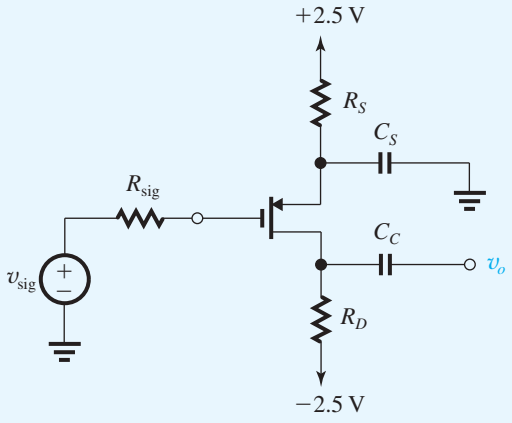


Figure P7.119

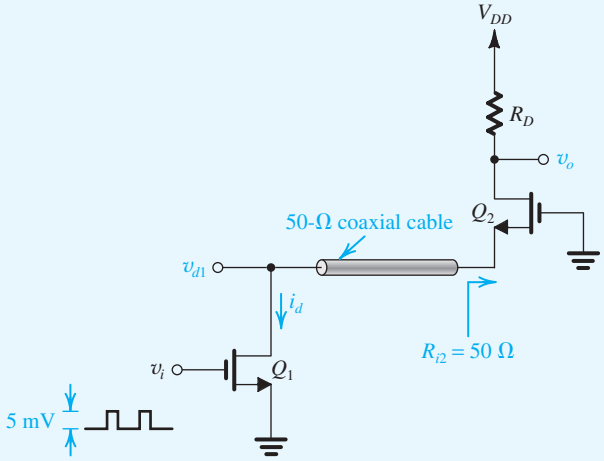


Figure P7.120

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

two MOSFETs whose bias details are not shown and a 50-Ω coaxial cable. Transistor Q_1 operates as a CS amplifier and Q_2 as a CG amplifier. For proper operation, transistor Q_2 is required to present a 50-Ω resistance to the cable. This situation is known as "proper termination" of the cable and ensures that there will be no signal reflection coming back on the cable. When the cable is properly terminated, its input resistance is 50 Ω. What must g_{m2} be? If Q_1 is biased at the same point as Q_2, what is the amplitude of the current pulses in the drain of Q_1? What is the amplitude of the voltage pulses at the drain of Q_1? What value of R_D is required to provide 1-V pulses at the drain of Q_2?

D ***7.121** The MOSFET in the circuit of Fig. P7.121 has $V_t = 0.8$ V, $k_n = 5$ mA/V^2, and $V_A = 40$ V.

(a) Find the values of R_S, R_D, and R_G so that $I_D = 0.4$ mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ±0.8 V is possible, and the input resistance at the gate is 10 MΩ. Neglect the Early effect.

(b) Find the values of g_m and r_o at the bias point.

(c) If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 1 MΩ, and terminal Y is connected to a load resistance of 10 kΩ, find the voltage gain from signal source to load.

(d) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower?

(e) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 50 μA and having a resistance of 100 kΩ, find the voltage signal that can be measured at Y. For simplicity, neglect the effect of r_o.

***7.122**

(a) The NMOS transistor in the source-follower circuit of Fig. P7.122(a) has $g_m = 10$ mA/V and a large r_o. Find the open-circuit voltage gain and the output resistance.

(b) The NMOS transistor in the common-gate amplifier of Fig. P7.122(b) has $g_m = 10$ mA/V and a large r_o. Find the input resistance and the voltage gain.

(c) If the output of the source follower in (a) is connected to the input of the common-gate amplifier in (b), use the results of (a) and (b) to obtain the overall voltage gain v_o/v_i.

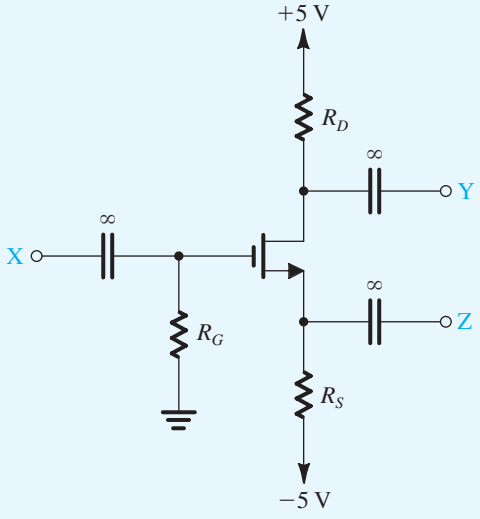


Figure P7.121

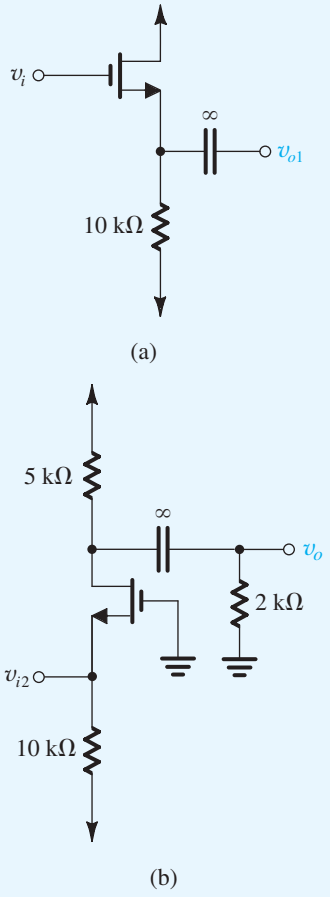


Figure P7.122

D **7.123 The MOSFET in the amplifier circuit of Fig. P7.123 has $V_t = 0.6$ V, $k_n = 5$ mA/V^2, and $V_A = 60$ V. The signal v_{sig} has a zero average.

(a) It is required to bias the transistor to operate at an overdrive voltage $V_{OV} = 0.2$ V. What must the dc voltage at the drain be? Calculate the dc drain current I_D taking into account V_A. Now, what value must the drain resistance R_D have?

(b) Calculate the values of g_m and r_o at the bias point established in (a).

(c) Using the small-signal equivalent circuit of the amplifier, show that the voltage gain is given by

$$\frac{v_o}{v_{sig}} = -\frac{R_2/R_1}{1 + \dfrac{1 + R_2/R_1}{g_m(R_D \| r_o \| R_2)(1 - 1/g_m R_2)}}$$

and find the value of the gain.

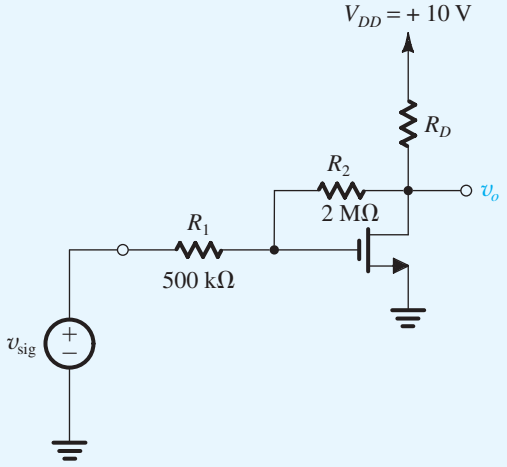


Figure P7.123

P.S. This feedback amplifier and the gain expression should remind you of an op amp utilized in the inverting configuration. We shall study feedback formally in Chapter 11.

D **7.124 The MOSFET in the amplifier circuit of Fig. P7.124 has $V_t = 0.6$ V and $k_n = 5$ mA/V^2. We shall assume that V_A is sufficiently large so that we can ignore the Early effect. The input signal v_{sig} has a zero average.

(a) It is required to bias the transistor to operate at an overdrive voltage $V_{OV} = 0.2$ V. What must the dc voltage at the drain be? Calculate the dc drain current I_D. What value must R_D have?

(b) Calculate the value of g_m at the bias point.

(c) Use the small-signal equivalent circuit of the amplifier to show that

$$\frac{v_o}{v_{sig}} = \frac{1 + (R_2/R_1)}{1 + \dfrac{(1 + R_2/R_1)}{g_m R_D'}}$$

and

$$R_{in} = \frac{1}{g_m}\left(1 + g_m R_D' \frac{R_1}{R_1 + R_2}\right)$$

where

$$R_D' = R_D \| (R_1 + R_2)$$

(d) Evaluate v_o/v_{sig} and R_{in}.

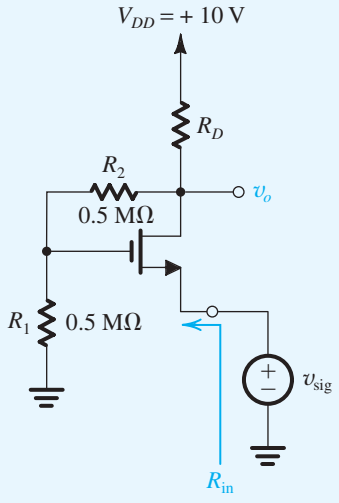


Figure P7.124

P.S. This feedback amplifier circuit and the gain formula should remind you of an op amp connected in the noninverting configuration. We shall study feedback formally in Chapter 11.

7.125 For the common-emitter amplifier shown in Fig. P7.125, let $V_{CC} = 15$ V, $R_1 = 27$ kΩ, $R_2 = 15$ kΩ, $R_E = 2.4$ kΩ, and $R_C = 3.9$ kΩ. The transistor has $\beta = 100$. Calculate the dc bias current I_C. If the amplifier operates between a source for which $R_{sig} = 2$ kΩ and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, and the overall voltage gain v_o/v_{sig}.

D 7.126 Using the topology of Fig. P7.125, design an amplifier to operate between a 2-kΩ source and a 2-kΩ load with a gain v_o/v_{sig} of –40 V/V. The power supply available is 15 V. Use an emitter current of approximately 2 mA and a current of about one-tenth of that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has $\beta = 100$. Use standard 5% resistors (see Appendix J).

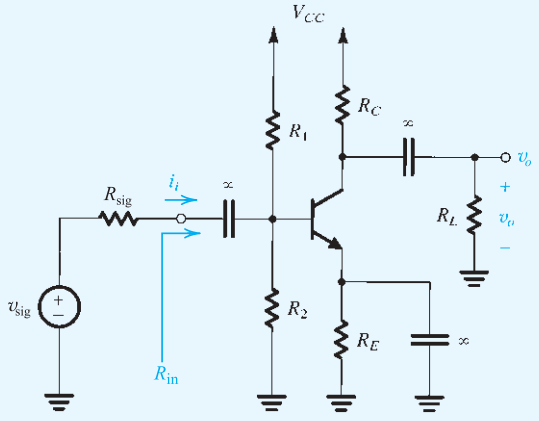


Figure P7.125

D 7.127 A designer, having examined the situation described in Problem 7.125 and estimating the available gain to be approximately –36.3 V/V, wants to explore the possibility of improvement by reducing the loading of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3: R_1 to 82 kΩ, R_2 to 47 kΩ, R_E to 7.2 kΩ, and R_C to 12 kΩ (standard values of 5%-tolerance resistors). With $V_{CC} = 15$ V, $R_{sig} = 2$ kΩ, $R_L = 2$ kΩ, and $\beta = 100$, what does the gain become? Comment.

D 7.128 The CE amplifier circuit of Fig. P7.128 is biased with a constant-current source I. It is required to design the circuit (i.e., find values for I, R_B, and R_C) to meet the following specifications:

(a) $R_{in} \simeq 10$ kΩ.
(b) The dc voltage drop across R_B is approximately 0.2 V.
(c) The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never fall by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that v_{sig} is a sinusoidal source, the available supply $V_{CC} = 5$ V, and the transistor has $\beta = 100$. Use standard 5% resistance values, and specify the value of I to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If $R_{sig} = R_L = 20$ kΩ, what is the overall voltage gain?

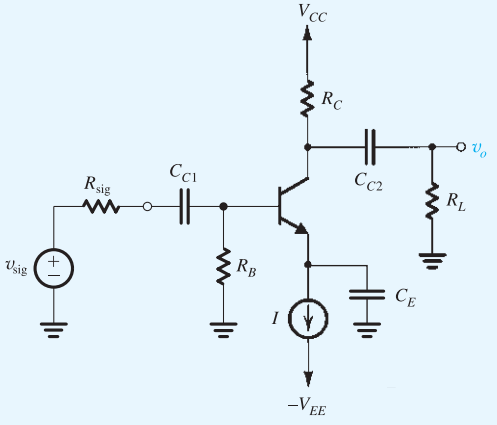


Figure P7.128

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

D 7.129 In the circuit of Fig. P7.129, v_{sig} is a small sine-wave signal with zero average. The transistor β is 100.

(a) Find the value of R_E to establish a dc emitter current of about 0.5 mA.

(b) Find R_C to establish a dc collector voltage of about +0.5 V.

(c) For $R_L = 10$ kΩ, draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

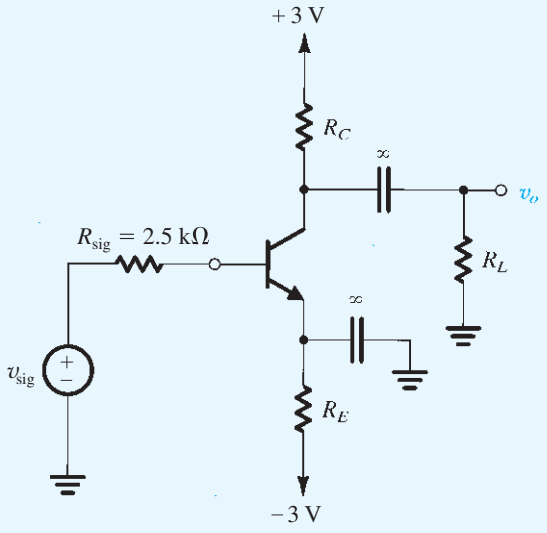


Figure P7.129

***7.130** The amplifier of Fig. P7.130 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage, R_{in2}, constitutes the load resistance of the first stage.

(a) For $V_{CC} = 15$ V, $R_1 = 100$ kΩ, $R_2 = 47$ kΩ, $R_E = 3.9$ kΩ, $R_C = 6.8$ kΩ, and $\beta = 100$, determine the dc collector current and dc collector voltage of each transistor.

(b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components.

(c) Find R_{in1} and v_{b1}/v_{sig} for $R_{sig} = 5$ kΩ.

(d) Find R_{in2} and v_{b2}/v_{b1}.

(e) For $R_L = 2$ kΩ, find v_o/v_{b2}.

(f) Find the overall voltage gain v_o/v_{sig}.

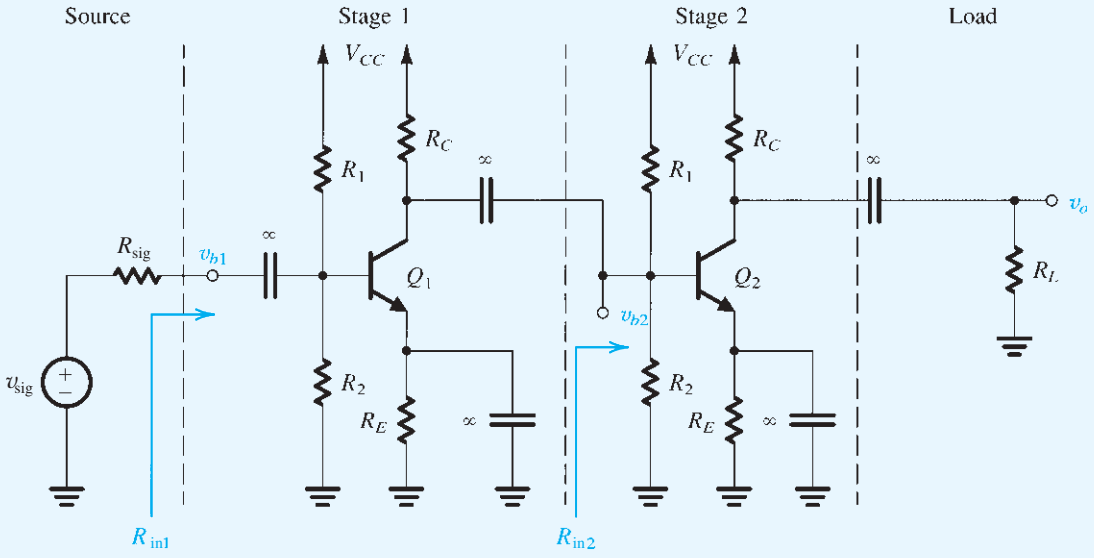


Figure P7.130

7.131 In the circuit of Fig. P7.131, the BJT is biased with a constant-current source, and v_{sig} is a small sine-wave signal. Find R_{in} and the gain v_o/v_{sig}. Assume $\beta = 100$. If the amplitude of the signal v_{be} is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

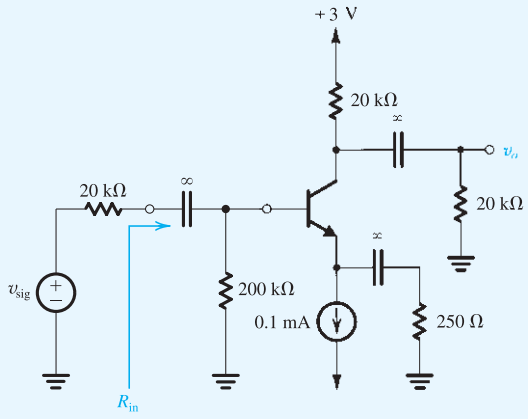


Figure P7.131

***7.132** The BJT in the circuit of Fig. P7.132 has $\beta = 100$.

(a) Find the dc collector current and the dc voltage at the collector.

(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_o/v_i.

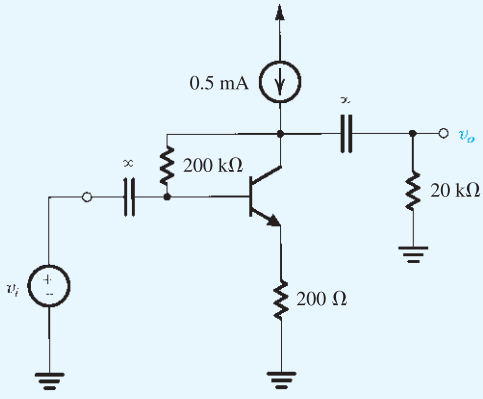


Figure P7.132

7.133 For the circuit in Fig. P7.133, find the input resistance R_{in} and the voltage gain v_o/v_{sig}. Assume that the source provides a small signal v_{sig} and that $\beta = 100$.

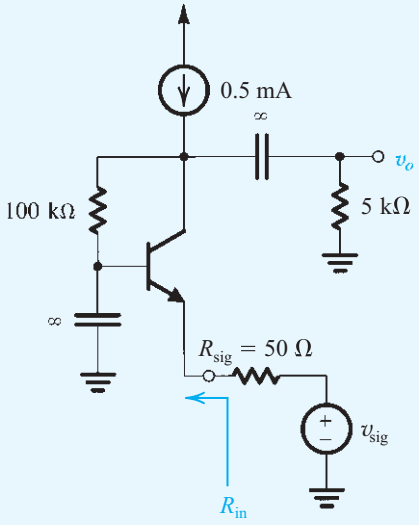


Figure P7.133

7.134 For the emitter-follower circuit shown in Fig. P7.134, the BJT used is specified to have β values in the range of 50 to 200 (a distressing situation for the circuit designer).

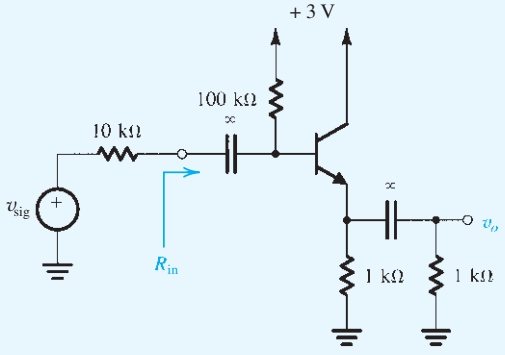


Figure P7.134

For the two extreme values of β ($\beta = 50$ and $\beta = 200$), find:

(a) I_E, V_E, and V_B
(b) the input resistance R_{in}
(c) the voltage gain v_o/v_{sig}

7.135 For the emitter follower in Fig. P7.135, the signal source is directly coupled to the transistor base. If the dc component of v_{sig} is zero, find the dc emitter current. Assume $\beta = 100$. Neglecting r_o, find R_{in}, the voltage gain v_o/v_{sig}, the current gain i_o/i_i, and the output resistance R_{out}.

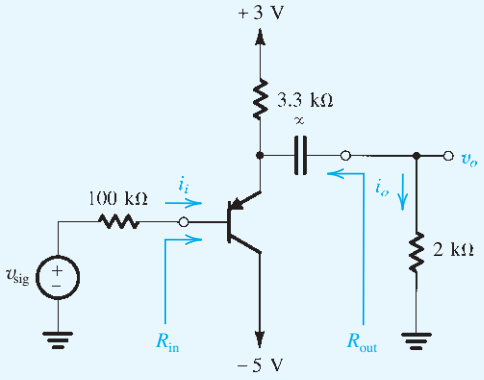


Figure P7.135

7.136 For the circuit in Fig. P7.136, called a **bootstrapped follower:**

(a) Find the dc emitter current and g_m, r_e, and r_π. Use $\beta = 100$.
(b) Replace the BJT with its T model (neglecting r_o), and analyze the circuit to determine the input resistance R_{in} and the voltage gain v_o/v_{sig}.
(c) Repeat (b) for the case when capacitor C_B is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

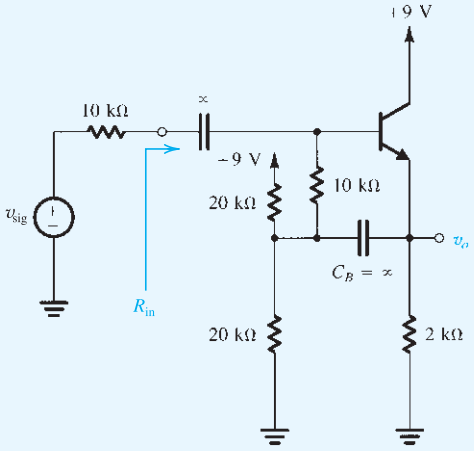


Figure P7.136

7.137 For the follower circuit in Fig. P7.137, let transistor Q_1 have $\beta = 50$ and transistor Q_2 have $\beta = 100$, and neglect the effect of r_o. Use $V_{BE} = 0.7$ V.

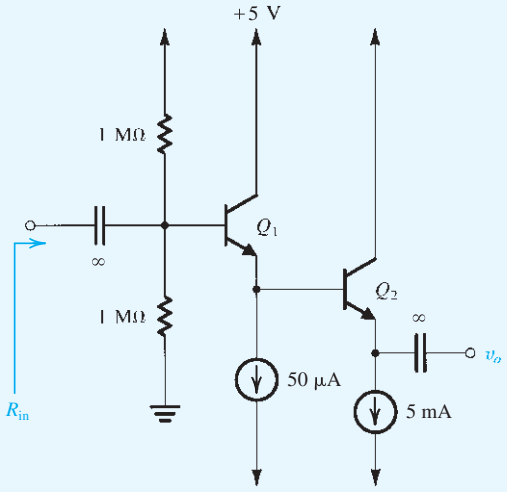


Figure P7.137

SIM = Multisim/PSpice; * = difficult problem; ** = more difficult; *** = very challenging; D = design problem

(a) Find the dc emitter currents of Q_1 and Q_2. Also, find the dc voltages V_{B1} and V_{B2}.

(b) If a load resistance $R_L = 1\ \text{k}\Omega$ is connected to the output terminal, find the voltage gain from the base to the emitter of Q_2, v_o/v_{b2}, and find the input resistance R_{ib2} looking into the base of Q_2. (*Hint:* Consider Q_2 as an emitter follower fed by a voltage v_{b2} at its base.)

(c) Replacing Q_2 with its input resistance R_{ib2} found in (b), analyze the circuit of emitter follower Q_1 to determine its input resistance R_{in}, and the gain from its base to its emitter, v_{e1}/v_{b1}.

(d) If the circuit is fed with a source having a 100-kΩ resistance, find the transmission to the base of Q_1, v_{b1}/v_{sig}.

(e) Find the overall voltage gain v_o/v_{sig}.

D 7.138 A CE amplifier has a midband voltage gain of $|A_M| = 100$ V/V, a lower 3-dB frequency of $f_L = 100$ Hz, and a higher 3-dB frequency $f_H = 500$ kHz. In Chapter 10 we will learn that connecting a resistance R_e in the emitter of the BJT results in lowering f_L and raising f_H by the factor $(1 + g_m R_e)$. If the BJT is biased at $I_C = 1$ mA, find R_e that will result in f_H at least equal to 2 MHz. What will the new values of f_L and A_M be?