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Nicholas Turner

SKILLS

-Programming Languages
- Advanced: C++, C, VHDL, SystemVerilog, Python, MATLAB & Simulink
- Intermediate: Java, HTML, Javascript

-Vivado, cocotb
-PyTorch, TensorFlow
-System controller analysis and design

RELEVANT COURSEWORK

-Computer Architecture: CS33, ECE M16, M116C
-Machine Learning/AI: ECE 131A, CS 161, M146, 247
-Control Systems: ECE 102, 141
-Communication Systems: ECE 113, 132A
-Circuit Analysis: ECE 10, 110, 111L, 115A
-Programming & Algorithms: CS 31, 32, 180

Interpersonal Skills: Excellent communication skills, with an appreciation for teamwork; ability to decompose an overarching goal into individually accomplishable tasks; dynamic mindset; keen eye for detail

WORK EXPERIENCE

UCLA Physics & Astronomy Department @ CERN — *R&D Engineer I*
August 2024 - Present

- Developed HDL for CMS trigger, part of the Large Hadron Collider
- Designed and implemented low-latency, parallelized modules in VHDL on an FPGA
  - Deghosting module — eliminates artifacts, reducing false positive rate by 85%
  - BRAM ring buffer and windowing module — stores and multiplexes large data packets
  - Trimmed bitonic sorting network — created a generalized N->M sorting network, reducing LUTs by ~90,000 (~90% from standard bitonic network)
  - Out-of-time correction algorithm — corrects for imperfect time resolution of individual hits by efficiently identifying local maxima, boosting efficiency by 17%
- Optimized existing modules to further reduce LUTs by ~80,000 (~25% total reduction)
- Built a Python backend for JTAG programming of EEPROMs and FPGAs via RPI GPIO
- Led investigations to analyze and debug custom electronics boards

Particle Beam Physics Laboratory @ UCLA — *Undergraduate Researcher*
June 2023 - September 2023

- Designed and built an electrical switching relay box to improve experiment efficiency
- Investigated methods to compare experimental results with an analytic undulator matrix

Communications Systems Laboratory @ UCLA — *Undergraduate Researcher*
June 2022 - August 2022

- Contributed to developing an efficient Viterbi decoding algorithm on an FPGA in VHDL, for use with a tail-biting convolutional encoder

PROJECTS

Digital Audio Visualizer

- Implemented a 32 point FFT processor and VGA controller on an FPGA in SystemVerilog
- Integrated several modules (microphone input, signal processing, VGA display output) into a functional system that displays the frequency decomposition of microphone input

Neural Network for EEG Classification

- Trained various architectures: CNN, RNN, ResNet, CNN+LSTM (70% test accuracy)
- Leveraged batch normalization, pooling, and dropout to maximize performance

RISC-V CPU & Memory Hierarchy

- In C++, simulated a functional RISC-V CPU and memory accompanied by multiple caches

HydrateMate

- Built a system to track water consumption via microcontroller and ultrasonic sensor, paired via Bluetooth with a user-friendly web application

EDUCATION

UCLA — *Electrical Engineering (B.S.) & Physics (B.A.)*
September 2020 - June 2024 GPA: 3.922