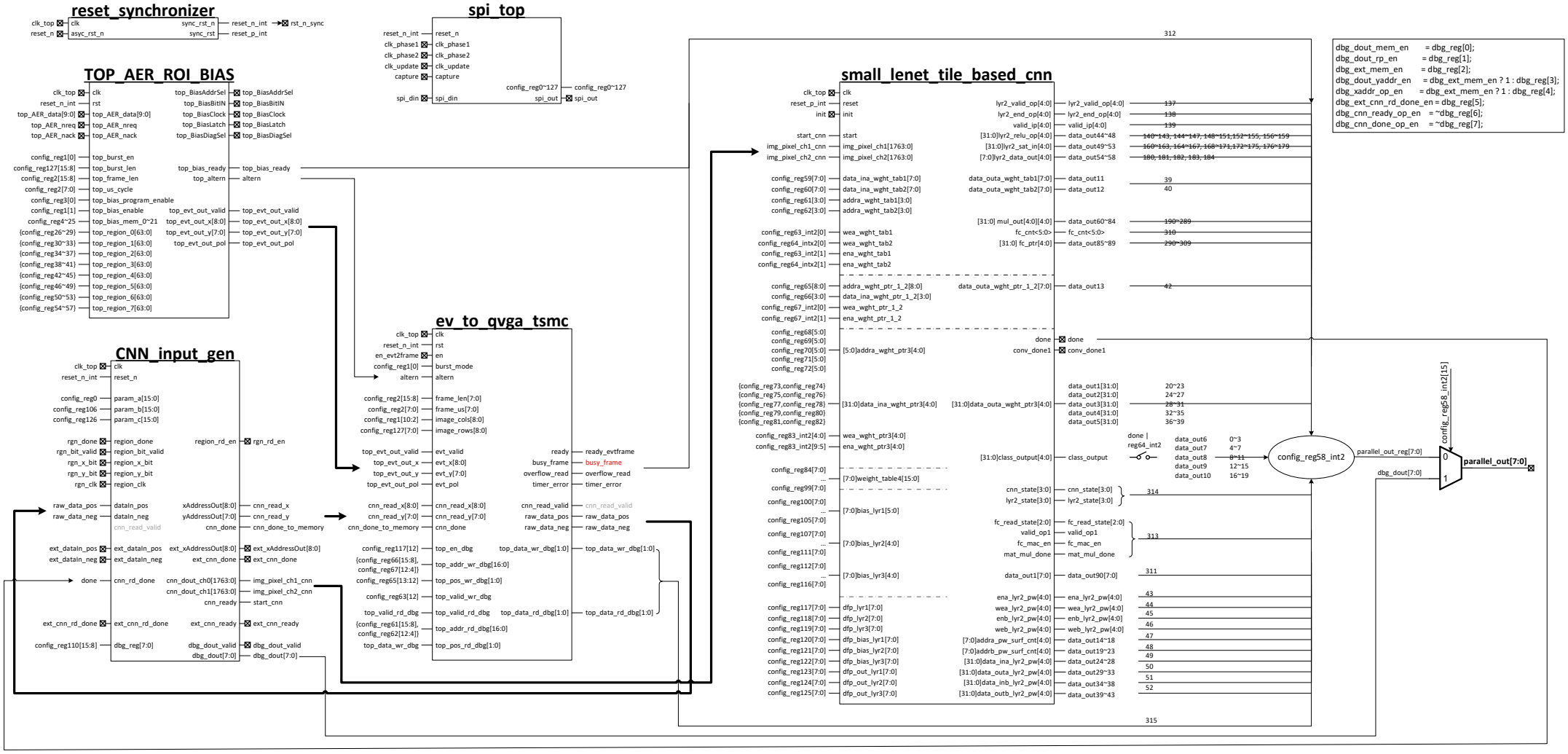
reset_synchronizer
clk_top
reset_n
clk
async_rst_n
sync_rst_n
sync_rst
reset_n_int
reset_p_int
rst_n_sync
spi_top
reset_n_int
clk_phase1
clk_phase2
clk_update
capture
spi_din
reset_n
clk_phase1
clk_phase2
clk_update
capture
spi_din
spi_out
config_reg0~127
config_reg0~127
spi_out
TOP_AER_ROI_BIAS
clk_top
reset_n_int
top_AER_data[9:0]
top_AER_nreq
top_AER_nack
config_reg1[0]
config_reg127[15:8]
config_reg2[15:8]
config_reg2[7:0]
config_reg3[0]
config_reg1[1]
config_reg4~25
{config_reg26~29}
{config_reg30~33}
{config_reg34~37}
{config_reg38~41}
{config_reg42~45}
{config_reg46~49}
{config_reg50~53}
{config_reg54~57}
clk
rst
top_AER_data[9:0]
top_AER_nreq
top_AER_nack
top_burst_en
top_burst_len
top_frame_len
top_us_cycle
top_bias_program_enable
top_bias_enable
top_bias_mem_0~21
top_region_0[63:0]
top_region_1[63:0]
top_region_2[63:0]
top_region_3[63:0]
top_region_4[63:0]
top_region_5[63:0]
top_region_6[63:0]
top_region_7[63:0]
top_BiasAddrSel
top_BiasBitIN
top_BiasClock
top_BiasLatch
top_BiasDiagSel
top_bias_ready
top_altern
top_evt_out_valid
top_evt_out_x[8:0]
top_evt_out_y[7:0]
top_evt_out_pol
top_BiasAddrSel
top_BiasBitIN
top_BiasClock
top_BiasLatch
top_BiasDiagSel
top_bias_ready
altern
top_evt_out_valid
top_evt_out_x[8:0]
top_evt_out_y[7:0]
top_evt_out_pol
CNN_input_gen
clk_top
reset_n_int
config_reg0
config_reg106
config_reg126
rgn_done
rgn_bit_valid
rgn_x_bit
rgn_y_bit
rgn_clk
raw_data_pos
raw_data_neg
cnn_read_valid
ext_dataIn_pos
ext_dataIn_neg
done
ext_cnn_rd_done
config_reg110[15:8]
clk
reset_n
param_a[15:0]
param_b[15:0]
param_c[15:0]
region_done
region_bit_valid
region_x_bit
region_y_bit
region_clk
dataIn_pos
dataIn_neg
ext_dataIn_pos
ext_dataIn_neg
cnn_rd_done
ext_cnn_rd_done
dbg_reg[7:0]
region_rd_en
xAddressOut[8:0]
yAddressOut[7:0]
cnn_done
ext_xAddressOut[8:0]
ext_cnn_done
cnn_dout_ch0[1763:0]
cnn_dout_ch1[1763:0]
cnn_ready
ext_cnn_ready
dbg_dout_valid
dbg_dout[7:0]
rgn_rd_en
cnn_read_x
cnn_read_y
cnn_done_to_memory
ext_xAddressOut[8:0]
ext_cnn_done
img_pixel_ch1_cnn
img_pixel_ch2_cnn
start_cnn
ext_cnn_ready
dbg_dout_valid
dbg_dout[7:0]
ev_to_qvga_tsmc
clk_top
reset_n_int
en_evt2frame
config_reg1[0]
altern
config_reg2[15:8]
config_reg2[7:0]
config_reg1[10:2]
config_reg127[7:0]
top_evt_out_valid
top_evt_out_x
top_evt_out_y
top_evt_out_pol
cnn_read_x[8:0]
cnn_read_y[7:0]
cnn_done_to_memory
config_reg117[12]
{config_reg66[15:8], config_reg67[12:4]}
config_reg65[13:12]
config_reg63[12]
top_valid_rd_dbg
{config_reg61[15:8], config_reg62[12:4]}
top_data_wr_dbg
clk
rst
en
burst_mode
altern
frame_len[7:0]
frame_us[7:0]
image_cols[8:0]
image_rows[8:0]
evt_valid
evt_x[8:0]
evt_y[7:0]
evt_pol
cnn_read_x[8:0]
cnn_read_y[7:0]
cnn_done
top_en_dbg
top_addr_wr_dbg[16:0]
top_pos_wr_dbg[1:0]
top_valid_wr_dbg
top_valid_rd_dbg
top_addr_rd_dbg[16:0]
top_pos_rd_dbg[1:0]
ready
busy_frame
overflow_read
timer_error
cnn_read_valid
raw_data_pos
raw_data_neg
top_data_wr_dbg[1:0]
top_data_rd_dbg[1:0]
ready_evtframe
busy_frame
overflow_read
timer_error
cnn_read_valid
raw_data_pos
raw_data_neg
top_data_wr_dbg[1:0]
top_data_rd_dbg[1:0]
312
small_lenet_tile_based_cnn
clk_top
reset_p_int
init
start_cnn
img_pixel_ch1_cnn
img_pixel_ch2_cnn
config_reg59[7:0]
config_reg60[7:0]
config_reg61[3:0]
config_reg62[3:0]
config_reg63_int2[0]
config_reg64_intx2[0]
config_reg63_int2[1]
config_reg64_intx2[1]
config_reg65[8:0]
config_reg66[3:0]
config_reg67_int2[0]
config_reg67_int2[1]
config_reg68[5:0]
config_reg69[5:0]
config_reg70[5:0]
config_reg71[5:0]
config_reg72[5:0]
{config_reg73,config_reg74}
{config_reg75,config_reg76}
{config_reg77,config_reg78}
{config_reg79,config_reg80}
{config_reg81,config_reg82}
config_reg83_int2[4:0]
config_reg83_int2[9:5]
config_reg84[7:0]
config_reg99[7:0]
config_reg100[7:0]
config_reg105[7:0]
config_reg107[7:0]
config_reg111[7:0]
config_reg112[7:0]
config_reg116[7:0]
config_reg117[7:0]
config_reg118[7:0]
config_reg119[7:0]
config_reg120[7:0]
config_reg121[7:0]
config_reg122[7:0]
config_reg123[7:0]
config_reg124[7:0]
config_reg125[7:0]
reset
init
start
img_pixel_ch1[1763:0]
img_pixel_ch2[1763:0]
data_ina_wght_tab1[7:0]
data_ina_wght_tab2[7:0]
addra_wght_tab1[3:0]
addra_wght_tab2[3:0]
wea_wght_tab1
wea_wght_tab2
ena_wght_tab1
ena_wght_tab2
addra_wght_ptr_1_2[8:0]
data_ina_wght_ptr_1_2[3:0]
wea_wght_ptr_1_2
ena_wght_ptr_1_2
[5:0]addra_wght_ptr3[4:0]
[31:0]data_ina_wght_ptr3[4:0]
wea_wght_ptr3[4:0]
ena_wght_ptr3[4:0]
[7:0]weight_table4[15:0]
[7:0]bias_lyr1[5:0]
[7:0]bias_lyr2[4:0]
[7:0]bias_lyr3[4:0]
dfp_lyr1[7:0]
dfp_lyr2[7:0]
dfp_lyr3[7:0]
dfp_bias_lyr1[7:0]
dfp_bias_lyr2[7:0]
dfp_bias_lyr3[7:0]
dfp_out_lyr1[7:0]
dfp_out_lyr2[7:0]
dfp_out_lyr3[7:0]
lyr2_valid_op[4:0]
lyr2_end_op[4:0]
valid_ip[4:0]
[31:0]lyr2_relu_op[4:0]
[31:0]lyr2_sat_in[4:0]
[7:0]lyr2_data_out[4:0]
data_outa_wght_tab1[7:0]
data_outa_wght_tab2[7:0]
[31:0] mul_out[4:0][4:0]
fc_cnt<5:0>
[31:0] fc_ptr[4:0]
data_outa_wght_ptr_1_2[7:0]
done
conv_done1
[31:0]data_outa_wght_ptr3[4:0]
[31:0]class_output[4:0]
cnn_state[3:0]
lyr2_state[3:0]
fc_read_state[2:0]
valid_op1
fc_mac_en
mat_mul_done
data_out1[7:0]
ena_lyr2_pw[4:0]
wea_lyr2_pw[4:0]
enb_lyr2_pw[4:0]
web_lyr2_pw[4:0]
[7:0]addra_pw_surf_cnt[4:0]
[7:0]addrb_pw_surf_cnt[4:0]
[31:0]data_ina_lyr2_pw[4:0]
[31:0]data_outa_lyr2_pw[4:0]
[31:0]data_inb_lyr2_pw[4:0]
[31:0]data_outb_lyr2_pw[4:0]
lyr2_valid_op[4:0]
lyr2_end_op[4:0]
valid_ip[4:0]
data_out44~48
data_out49~53
data_out54~58
data_out11
data_out12
data_out60~84
data_out85~89
data_out13
done
conv_done1
data_out1[31:0]
data_out2[31:0]
data_out3[31:0]
data_out4[31:0]
data_out5[31:0]
cnn_state[3:0]
lyr2_state[3:0]
fc_read_state[2:0]
valid_op1
fc_mac_en
mat_mul_done
data_out90[7:0]
ena_lyr2_pw[4:0]
wea_lyr2_pw[4:0]
enb_lyr2_pw[4:0]
web_lyr2_pw[4:0]
data_out14~18
data_out19~23
data_out24~28
data_out29~33
data_out34~38
data_out39~43
137
138
139
140~143, 144~147, 148~151,152~155, 156~159
160~163, 164~167, 168~171,172~175, 176~179
180, 181, 182, 183, 184
39
40
190~289
310
290~309
42
done | reg64_int2
data_out6
data_out7
data_out8
data_out9
data_out10
0~3
4~7
8~11
12~15
16~19
config_reg58_int2
parallel_out_reg[7:0]
dbg_dout[7:0]
config_reg58_int2[15]
0
1
parallel_out[7:0]
314
313
311
43
44
45
46
47
48
49
50
51
52
315
dbg_dout_mem_en = dbg_reg[0];
dbg_dout_rp_en = dbg_reg[1];
dbg_ext_mem_en = dbg_reg[2];
dbg_dout_yaddr_en = dbg_ext_mem_en ? 1 : dbg_reg[3];
dbg_xaddr_op_en = dbg_ext_mem_en ? 1 : dbg_reg[4];
dbg_ext_cnn_rd_done_en = dbg_reg[5];
dbg_cnn_ready_op_en = ~dbg_reg[6];
dbg_cnn_done_op_en = ~dbg_reg[7];