

Computer Organization and Operating System

Computer Performance

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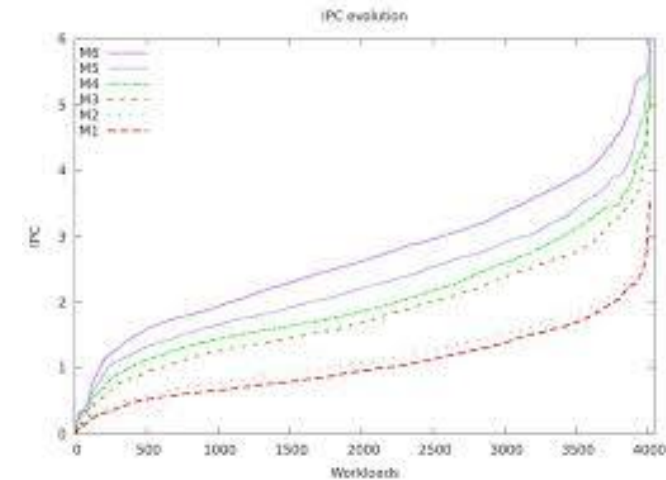
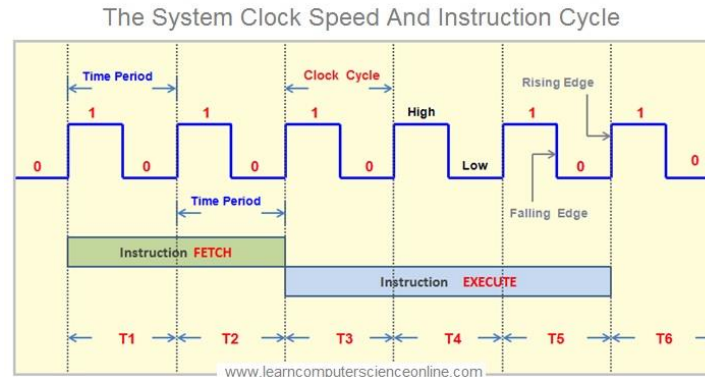
Topic

- Computer Performance Overview
- Performance Techniques
- Clock Speed
 - Overview, Effects
- Pipeline
 - Overview, Effects
- Parallel Processing
- Conclusion

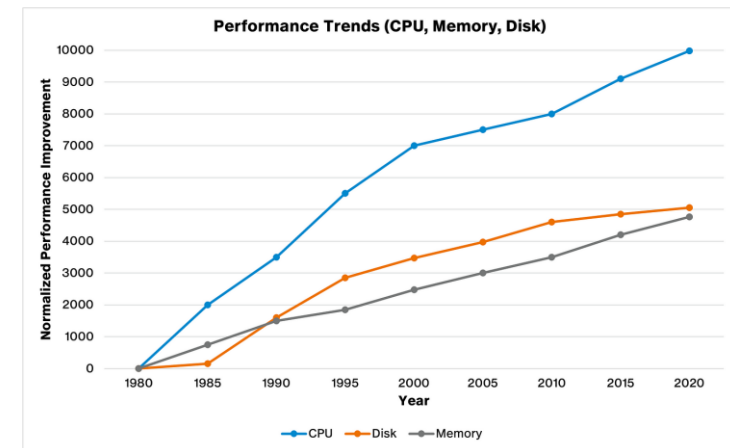


Computer Performance Overview

- Need for higher speed of processing
 - High Performance
- Performance Measurements
 - Instructions Per Second
 - MIPS – Million Inst. Per Sec.
 - Operations Per Second
 - FLOPS – Floating Point Op./ Sec.
 - Cycle Per Instruction (CPI)
 - *Instruction Per Cycle (IPC)*
- Performance Effects
 - Clock Speed
 - Instruction Execution Time
 - Instructions in Program
- Benchmarks / Standards

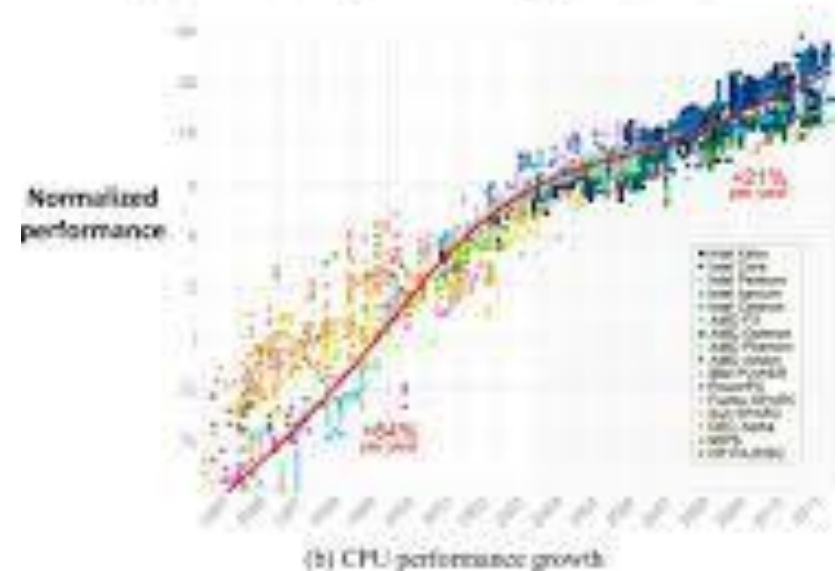
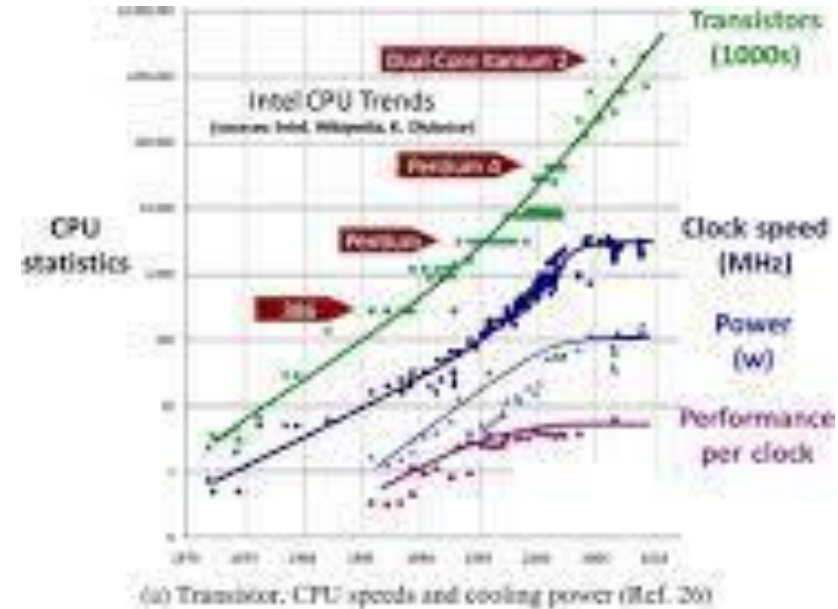
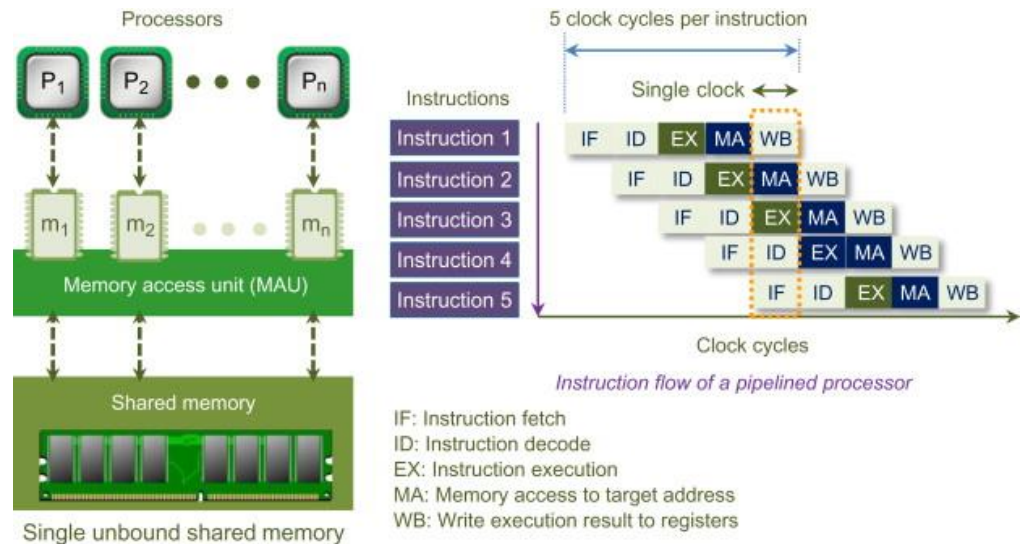


$$CPI = \frac{\text{CPU clock cycles for the program}}{\text{Instruction count}}$$
$$CPU \text{ time} = \text{Instruction count} \times CPI \times \text{Clock cycle time}$$
$$= \frac{\text{Instruction count} \times CPI}{\text{Clock rate}}$$



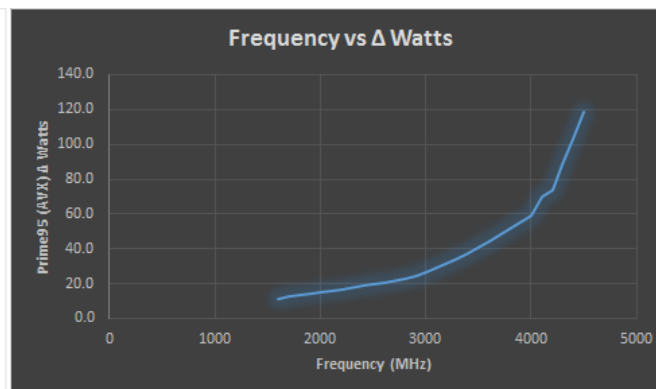
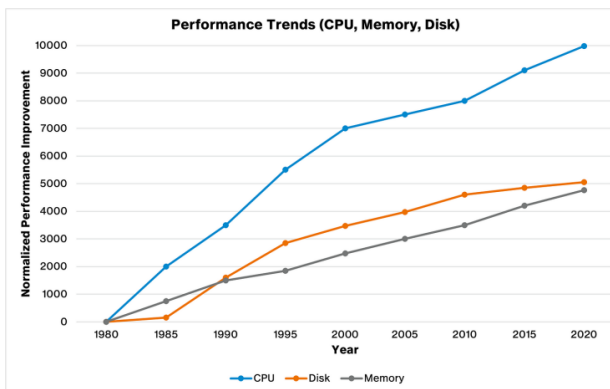
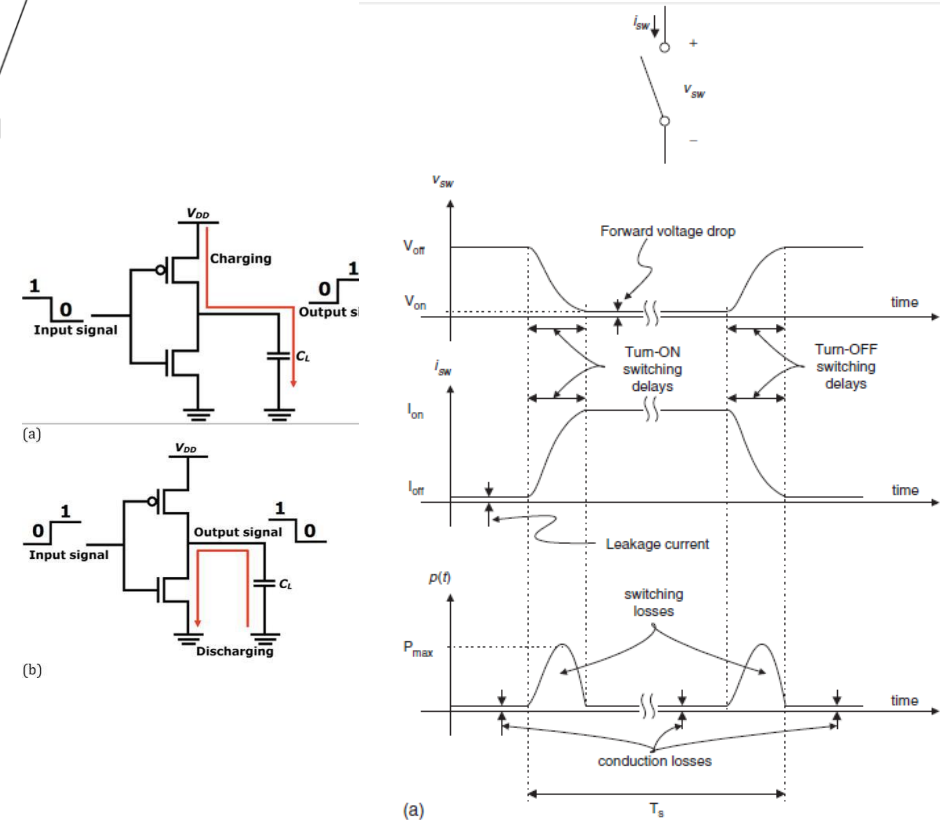
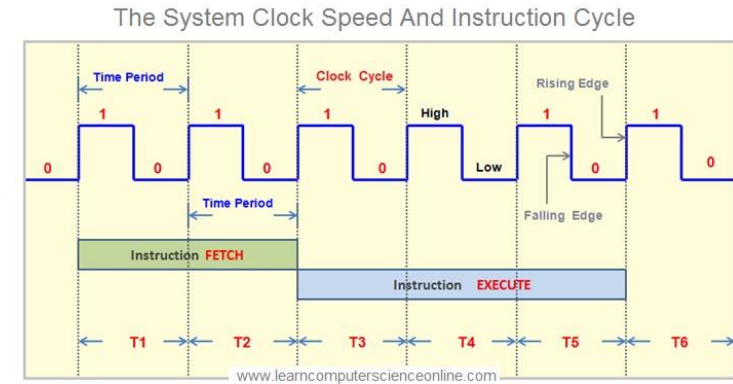
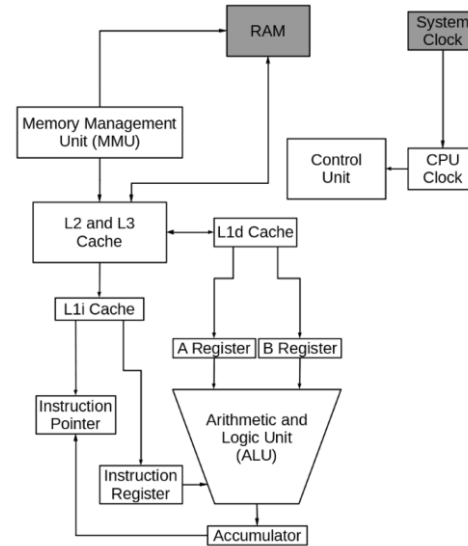
Performance Techniques

- Clock Speed
- Pipelining
- Parallel Processing
 - Multi-Core
 - Clustering



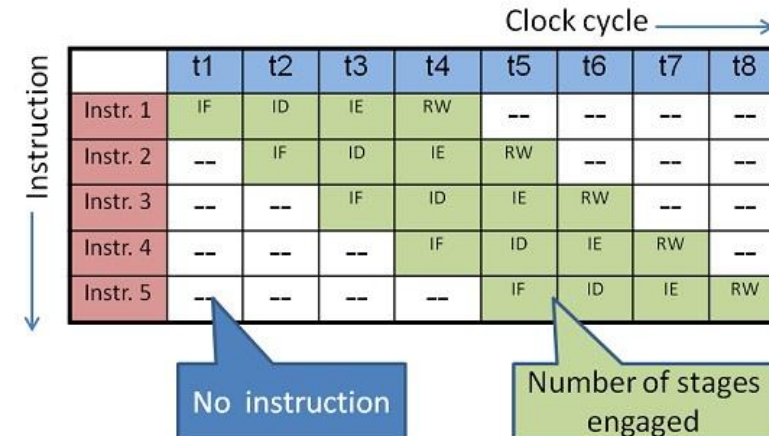
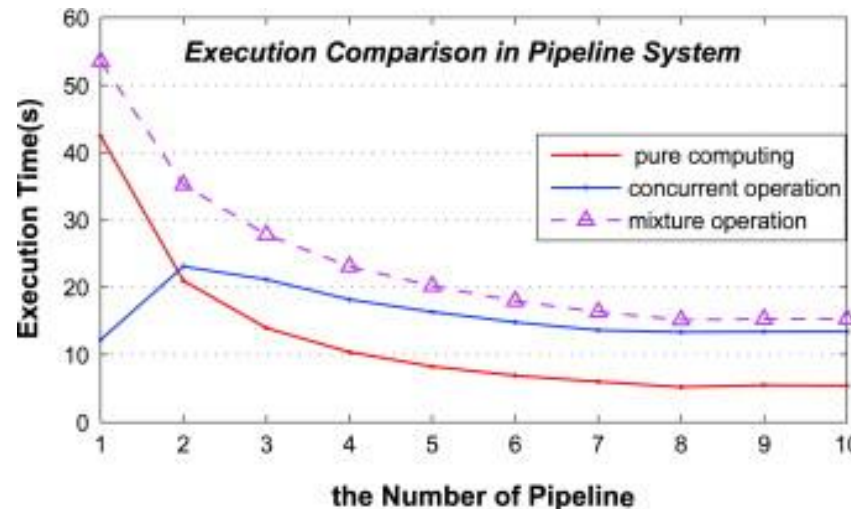
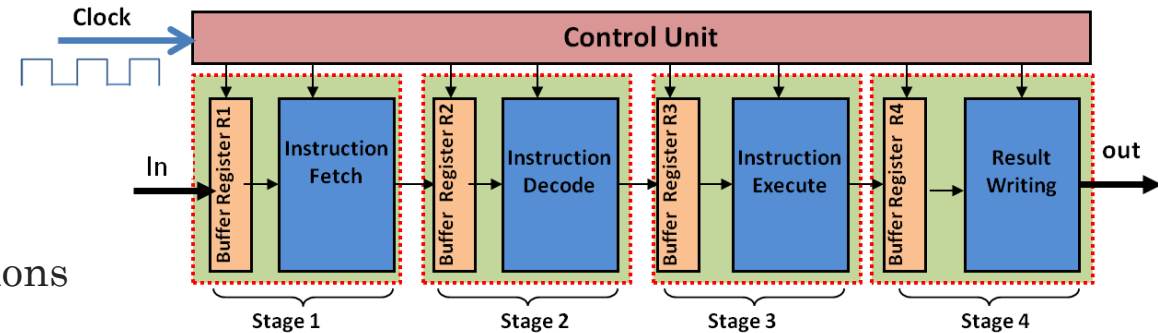
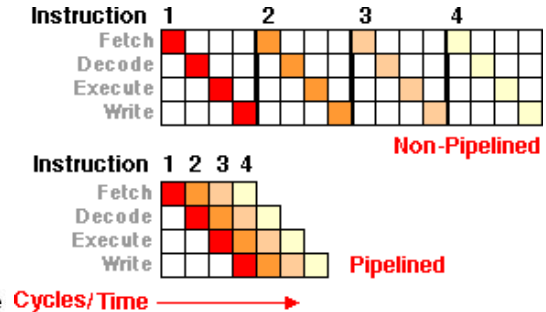
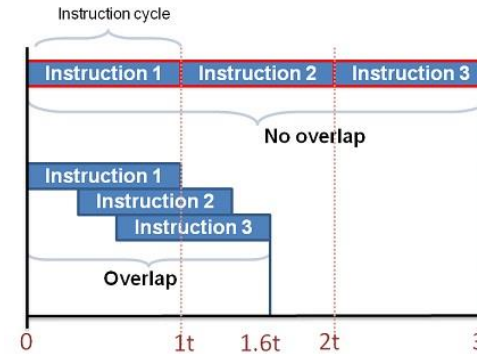
Clock Speed

- CPU synchronized to clock
- Increase Clock Speed – Hz
- Physical Limits
 - Electronics
 - Size / Distance
- Clock Speed vs Power Consumption
 - Heat
- CPU-RAM Speed difference
 - Cache Memory



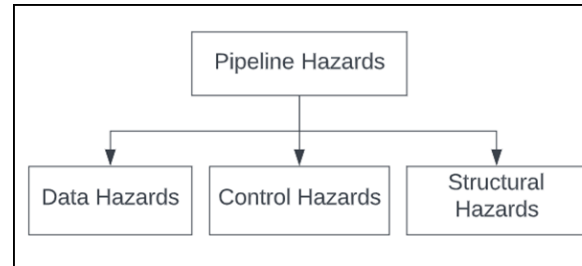
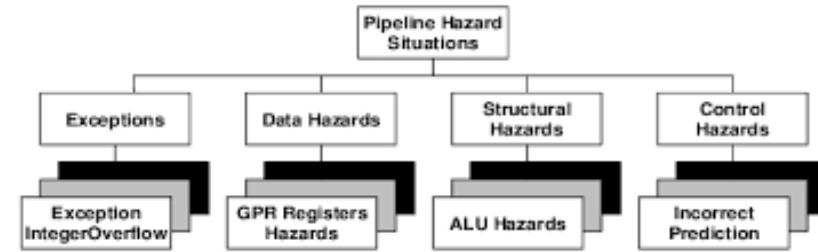
Pipelining

- Instruction Cycle => Multiple Stages
- Execute Multiple Instructions Simultaneously
 - Instruction Stages Overlapping
- Number of Instruction Stages
 - => Number of Parallel Instructions in Pipeline
- Increase Instruction Per Cycle (IPC)
 - One Clock Cycle => Execute Multiple Instructions
- Pre-Execution

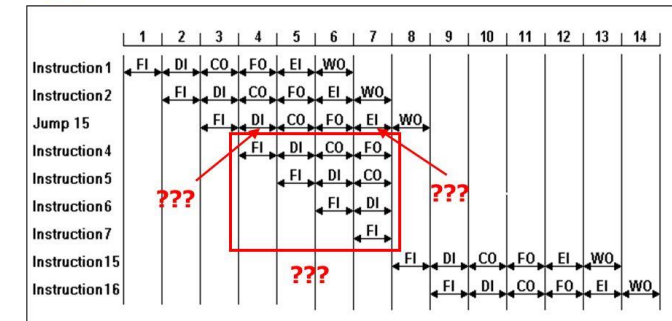


Pipeline Problems / Hazards

- Multiple Instructions execute simultaneously
- Data Hazard
 - Data Access from multiple instructions
- Control Hazard
 - Sequences of instructions execution
 - Branch
- Structural Hazard
 - Resources conflicts from multiple instructions



Instruction pipelining Problems – Control hazard

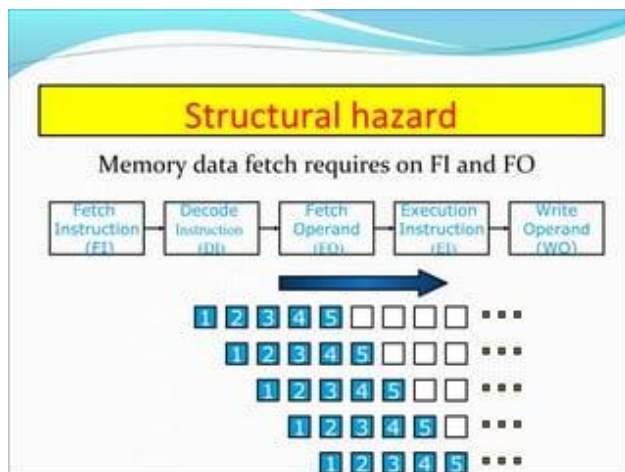
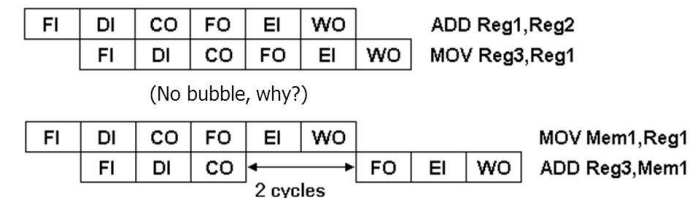


Instruction pipelining Problems – Data hazard

■ Data hazard

An instruction may produce data that is needed by a later instruction

Examples:



Data Hazard / Data Dependency

$i : R_1 \leftarrow R_2 * R_3$
 $i + 1 : R_4 \leftarrow R_1 + R_5$

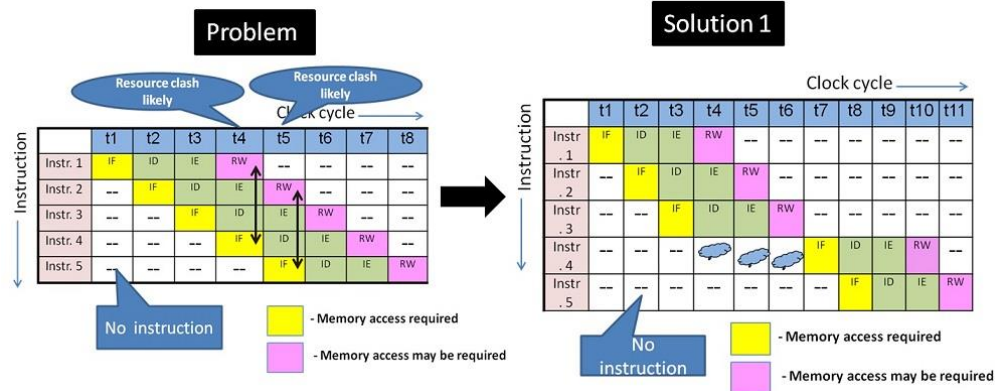
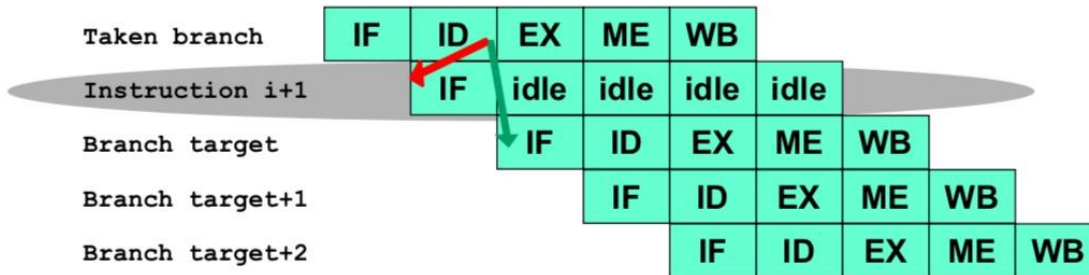
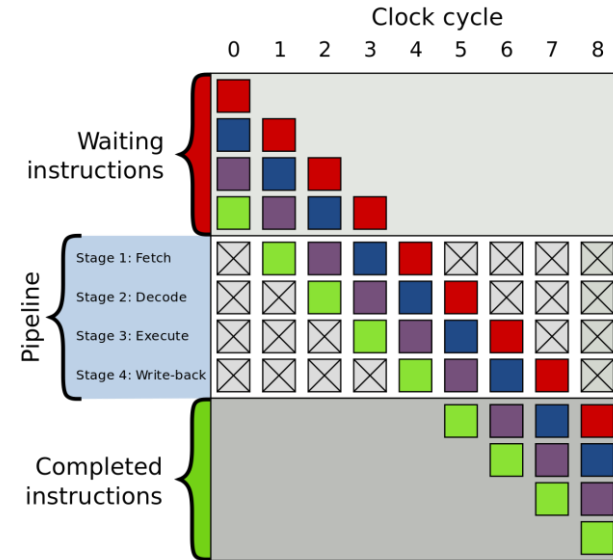


Pipeline Hazard Solutions

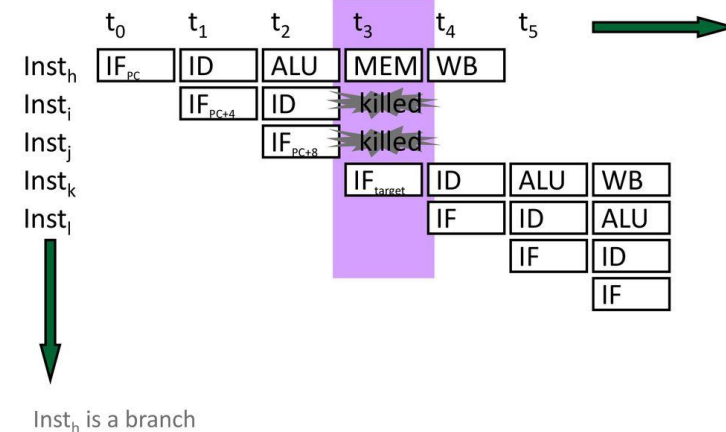
- Branch Prediction
 - Misprediction
- Delayed Execution
 - Added Clock
- ...

State	Instruction Cycle							
Fetch	I1	ST	ADD	I3	I4	I4	I5	I6
Decode		I1	ST	ADD	I3	I3	I4	I5
Operands			I1	ST	ADD	ADD	I3	I4
Execute				I1	ST	-	ADD	I4

Extra cycle added

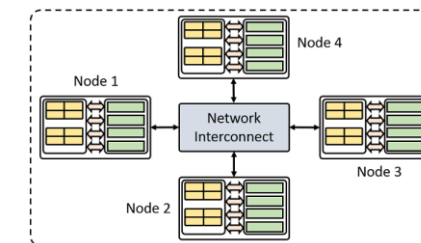
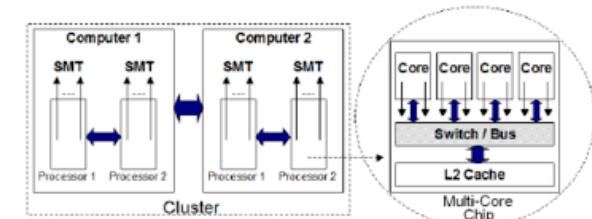
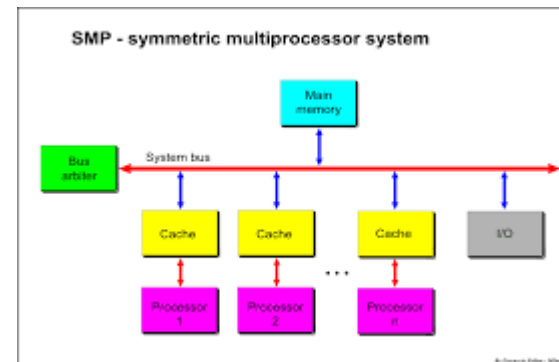
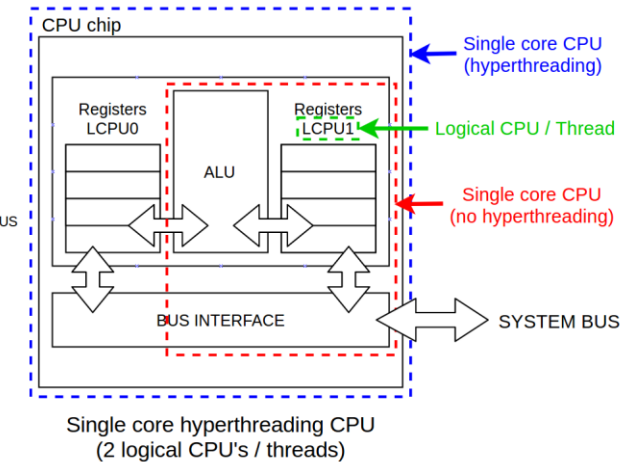
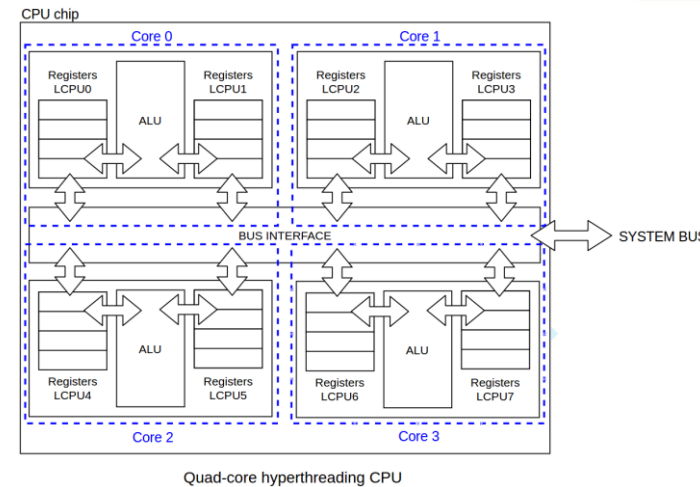
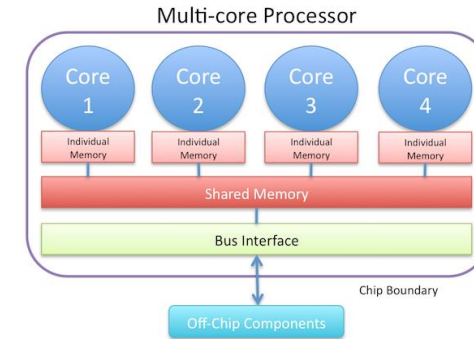


Pipeline Flush on a Misprediction



Parallel Processing

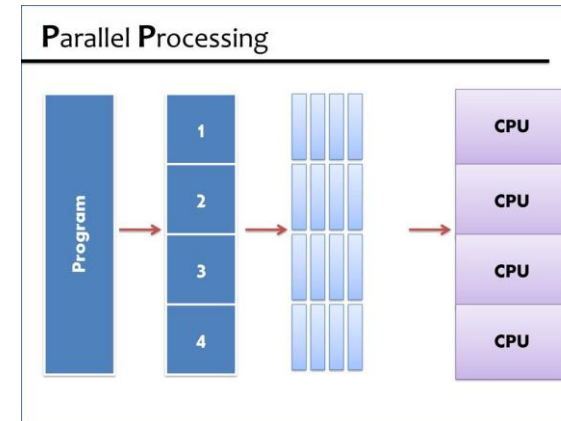
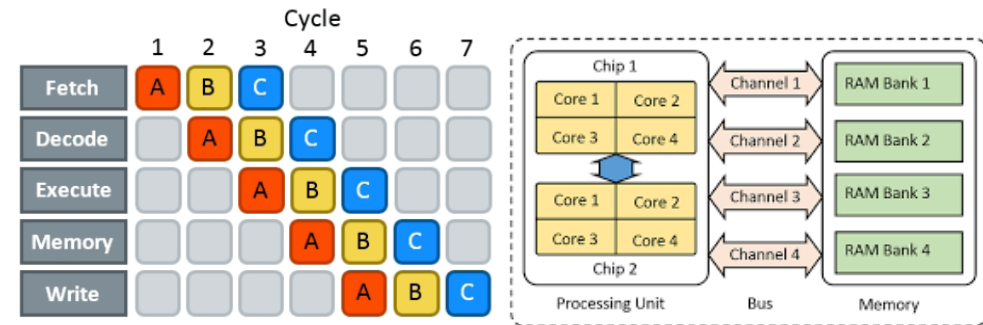
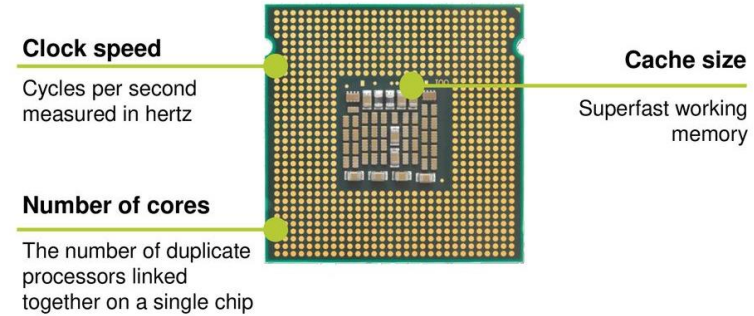
- Multiple Executing Units Simultaneously
- Multiple Cores
 - Core => CPU (REG+ALU+CU)
- Multiple Threads
 - Threads – Virtual CPU
 - Executing Status
 - Registers
 - Shared CPU-Components
 - ALU, Control Unit
- Multi-Processors
 - Multiple CPU in multiple sockets
 - Each CPU may be Multi-Cores
 - Shared Memory
- Multi-Computers
 - Multiple sets of CPU-Memory
 - Shared I/O
 - Separate I/O => Computer Cluster



Conclusion

- Computer Performance continuously increased, using many techniques
- Increasing clock speed is a basic way
 - Limits by physics
 - Different component speeds
 - For main memory, solved by cache memory
- Pipeline increased parallel instructions execute in overlapped instruction stages
 - Multiple instruction executions hazards reduced the performance
- Increasing number of executing units in parallel
 - Multiple executors at the same times
 - Multiple Cores/Threads/Processors/Computers
- Final words, Computer Performance can be improved by Increasing
 - clock speed
 - parallel instructions and execution units

Factors affecting CPU performance



END

Questions?