1300 Henley Court
Pullman, WA 99163
509.334.6306
www.digilentinc.com

AXI DPTI 1.0 IP Core User Guide

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1 Introduction

This user guide describes the Digilent AXI DPTI Intellectual Property. The purpose of this IP is to implement an interface between DPTI and AXI4 Stream. This interface will be controlled using Microblaze via control and status registers and it will theoretically be capable of speeds up to 480 megabits per second.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx: AXI4 Lite, AXI4 Stream Digilent: DPTI
Provided with core	
Design files	VHDL
Simulation model	N/A
Constraints file	XDC
Software driver	Standalone
Tested design flows	
Design entry	Vivado™ Design Suite 2015.4
Synthesis	Vivado Synthesis 2015.4

2 Features

- Provides high-speed bidirectional data transfers
- Implements 3 AXI4 Lite registers: 2 for control, 1 for status
- AXI DMA – style length register
- Supports transfer sizes of up to 8 MB

3 Performance

The IP will transfer data between the DPTI protocol and AXI4 Stream. It is a half-duplex synchronous interface working on the DPTI clock generated by the FTDI chip. Data is passed via an 8bit bidirectional data bus, when the handshake signals allow it, on each rising edge of the 60MHz clock.

The AXI4 Stream interface implemented by the IP is comprised of a 32bit wide TDATA bus, 4bit TKEEP bus and the TREADY, TVALID and TLAST signals. The maximum transfer rate is 480 megabits per second, the same as for the USB 2.0 High Speed protocol.

The IP consists of several individual modules as can be seen in Figure 1, the most important parts being the two converters: DPTI to AXI4 Stream and AXI4 Stream to DPTI. Two AXI4 Stream FIFOs are used for clock domain crossing, both of them with the minimum depth of 16. The AXI4 Lite registers are synchronized using the “HandshakeData” module for the control registers and “SyncAsync“ for the status register.

4 Overview

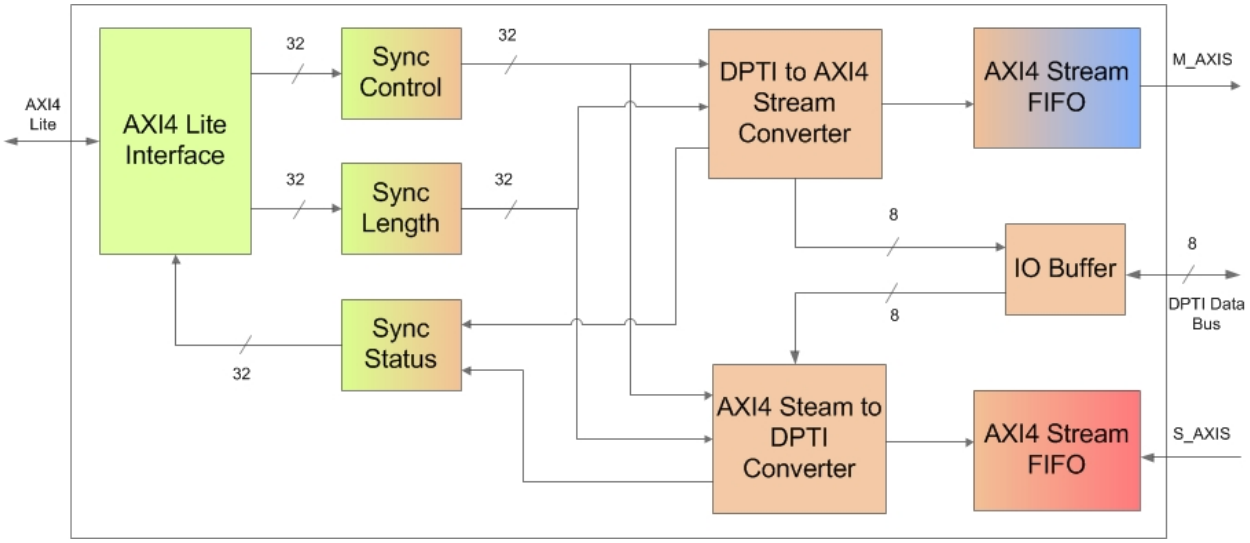


Figure 1. AXI DPTI block diagram.

The IP is built from multiple blocks and has 4 clock signals, one for each of the interfaces involved in the core as depicted in the image, most of the logic being driven by the FTDI clock.

4.1 DPTI protocol

A "Write" transfer is performed when data is sent from the FPGA to the FTDI chip using the PROG_TXEN – PROG_WRN signals. When data is moved in the other direction, a "Read" transfer is performed and the handshake signals in this case are PROG_RXFN – PROG_RDN. A fifth signal called PROG_OEN is used to inform the FT2232H regarding the transfer direction: low when reading and high when writing data. PROG_OEN, PROG_RDN and PROG_WRN are generated by the IP and PROG_RXFN and PROG_TXEN by the FTDI IC.

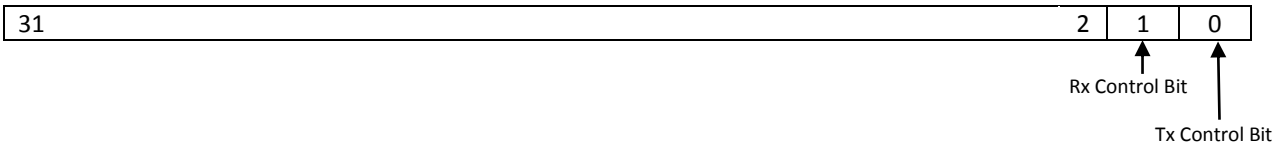
4.2 AXI4 Lite registers

The AXI DPTI core implements two control registers and one status register which can be accessed using the AXI4 Lite interface. The first register is used for writing the transfer length and it uses the base address. The next register is used for the IP core's control. And the third one is the status register.

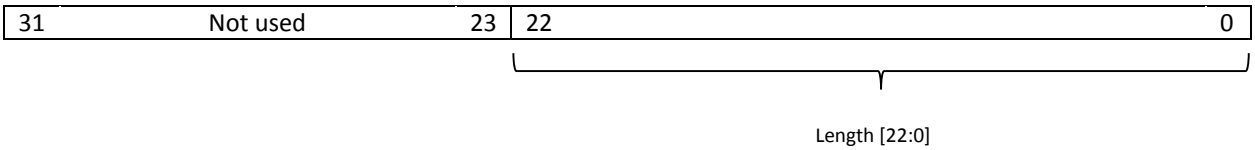
Address Space Offset	Name	Description
00h	Length	AXI DPTI transfer length in bytes
04h	Control	AXI DPTI transfer direction
08h	Status	AXI DPTI status

Table 1. AXI4 Lite register space

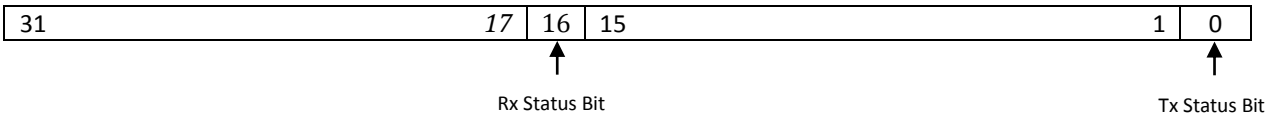
Control register



Length register



Status register



4.3 Transfer control

Transfers will be performed by first configuring the Control register, setting the direction. Only one converter can work at a given time since DPTI is a half-duplex interface. In order to enable a converter, the corresponding bit must be set to 1 while the other converter must be disabled. For “Write” transfers bit 0 will be asserted and bit 1 will be de-asserted; for “Read” transfers bit 1 will be de-asserted and bit 1 will be asserted.

After the transfer direction has been selected, writing the Length register will determine the transfer to start. While the core is busy, the transfer direction cannot be changed. After the transfer was completed, another transfer in the same direction can be performed without needing to write the control register again.

The status of the IP can be determined by reading the status register. Bits 0 and 16 of this register will each inform the user about the state of each of the converters. A true value will indicate an available module. Both bits must be true in order for a new transfer to be requested.

5 Port descriptions

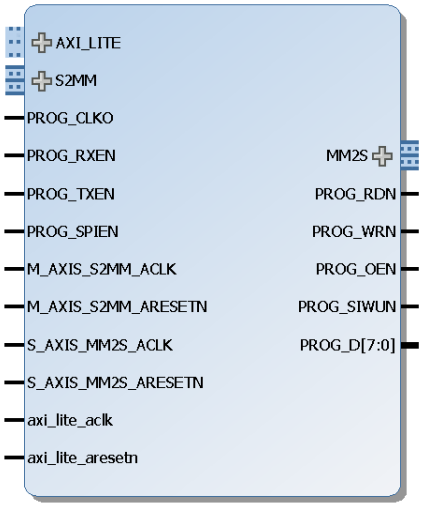


Figure 2. AXI DPTI IP Core.

The table below will present the signals and interfaces implemented by the AXI DPTI core.

Signal Name	Interface	Signal Type	Init State	Description
PROG_CLKO	DPTI	Input	N/A	DPTI protocol clock signal
PROG_RXEN	DPTI	Input	N/A	Pixel clock.
PROG_TXEN	DPTI	Input	N/A	Video data valid: • 1 = Active video. • 0 = Blanking period.
PROG_SPIEN	DPTI	Input	N/A	SPI enable
PROG_RDN	DPTI	Output	N/A	Read signal. When low, data byte is valid.
PROG_WRN	DPTI	Output	N/A	Write signal. When low, data byte is valid.
PROG_OEN	DPTI	Output	N/A	Output enable signal. Determines transfer direction
PROG_SIWUN	DPTI	Output	N/A	Send Imediate / Wake-up signal
PROG_D [8]	DPTI	Input / Output	N/A	Bidirectional data bus
M_AXIS_S2MM_ACLK	MM2S	Input	N/A	MM2S interface clock signal
S_AXIS_MM2S_ACLK	S2MM	Input	N/A	S2MM interface clock signal
axi_lite_aclk	AXI_LITE	Input	N/A	AXI_LITE interface clock signal
M_AXIS_S2MM_ARESETN	MM2S	Input	N/A	M2SS
S_AXIS_MM2S_ARESETN	S2MM	Input	N/A	S2MM reset signal
axi_lite_aresetn	AXI_LITE	Input	N/A	AXI_LITE reset signal

AXI4 Lite Interface Signals		
AXI_LITE*	Input / Output	AXI4 Lite interface used to communicate with the control and status registers
AXI4 Stream Interface Signals		
S2MM*	Input	AXI4 Stream interface - input for data which will be converted to the DPTI protocol
MM2S*	Output	AXI4 Stream interface - output for data which has been received from the DPTI port

Table 2. Port descriptions

6 Designing with the core

6.1 Constraints

The AXI DPTI core includes the timing constraints needed for the DPTI protocol for boards where the signal traces are equal in length. The HandshakeData and SyncAsync modules are also constrained.

An out-of-context XDC file is included which will provide constraints for the AXI4 Stream clock signals.

7 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.4, May 13, 2014.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Xilinx Inc., *UG903: Using Constraints, v2014.3, October 31, 2014*
4. Xilinx Inc., *PG021: AXI DMA logiCORE IP Product Gudie, v7.1, november 18, 2015*
5. FTDI, *FT2232H Dual High Speed USB to Multipurpose UART/FIFO IC*, v2.5
6. FTDI, *AN_165: Establishing Synchronous 245 FIFO Communications using a Morph-ICII*, v1.1, June 26,2012