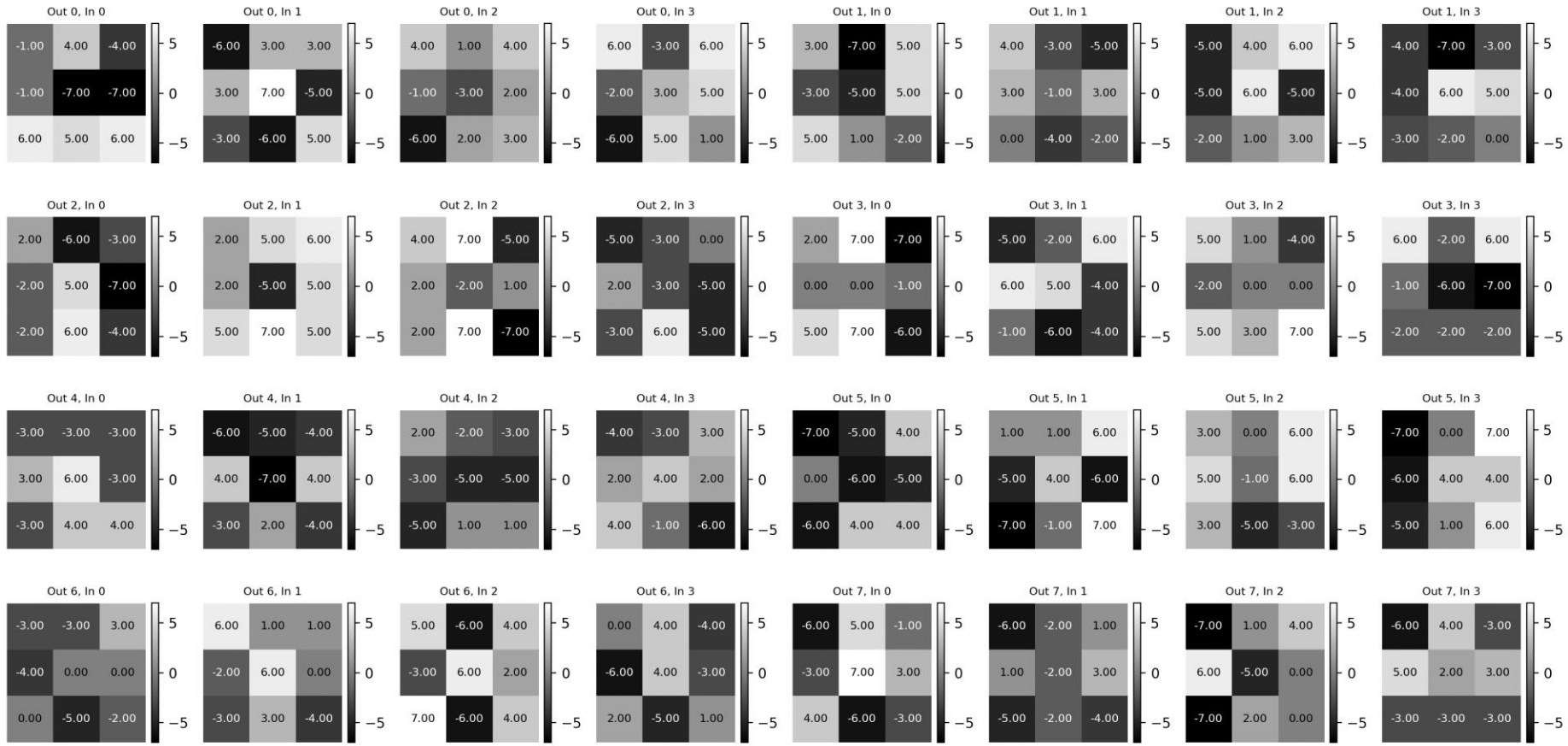
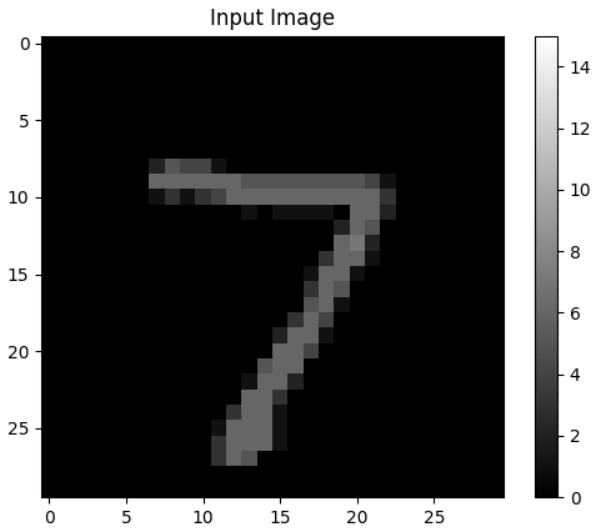
Weight distribution of layer 2



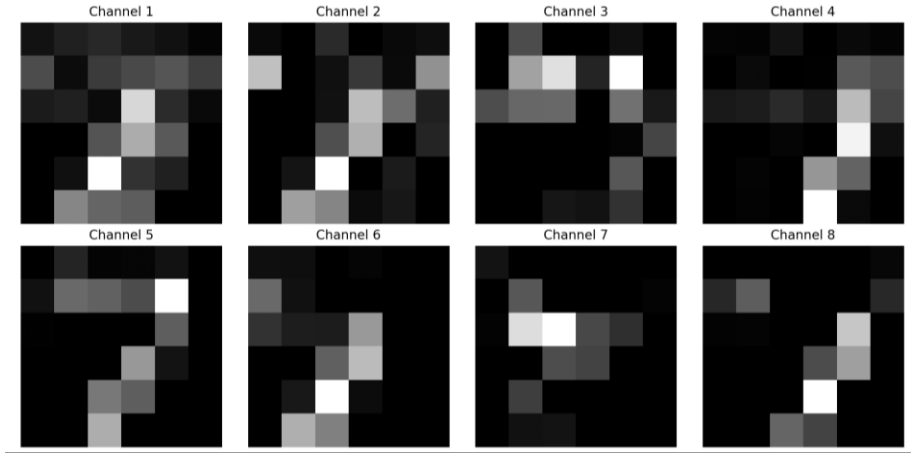
Automatic Scaling in Matplotlib's imshow

- Matplotlib’s imshow function displays an image by mapping data values to colors. When no explicit limits (vmin, vmax) are provided, it automatically determines these limits based on the data.
- When you call ax.imshow(image, cmap='gray'), Matplotlib scans the entire array image to find the smallest and largest values.
- The smallest value becomes the default **minimum limit**.
- The largest value becomes the default **maximum limit**.
- **Lower Bound:** The minimum value is mapped to the beginning of the colormap (e.g., black in the grayscale).
- **Upper Bound:** The maximum value is mapped to the end of the colormap (e.g., white in the grayscale).

Conv2 output with imshow

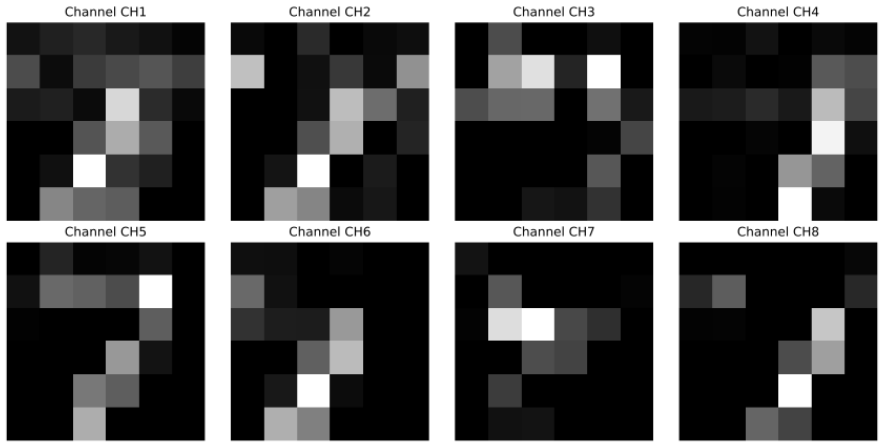


This data is in floating-point



Pooling Layer 2 Output (8 Channels)
From Training Model (Python)

This data is in voltages

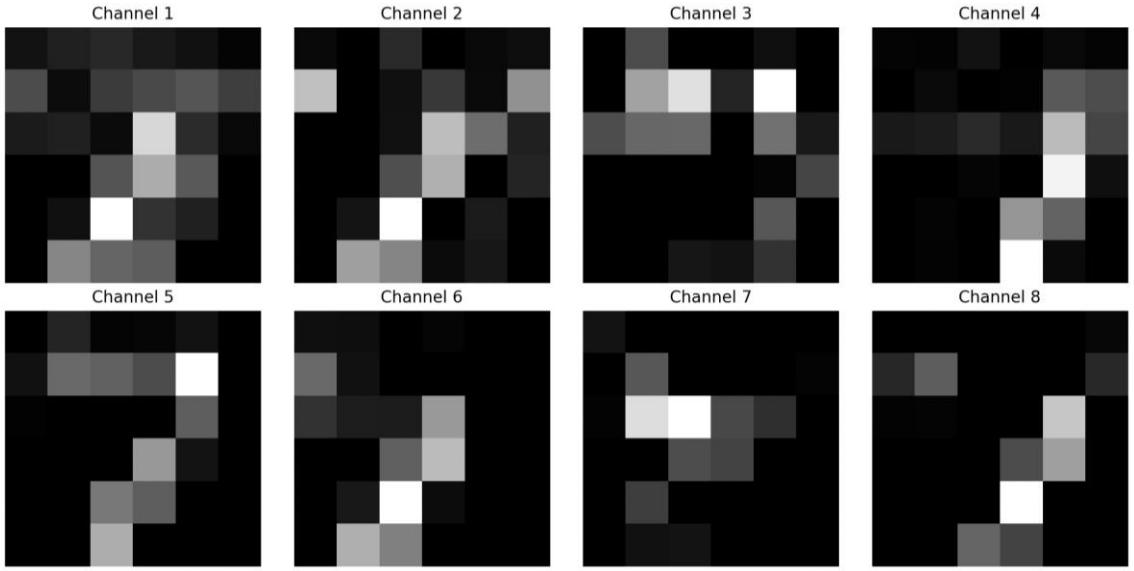


Pooling Layer 2 Output (8 Channels)
From Verilog-A (No ADC)

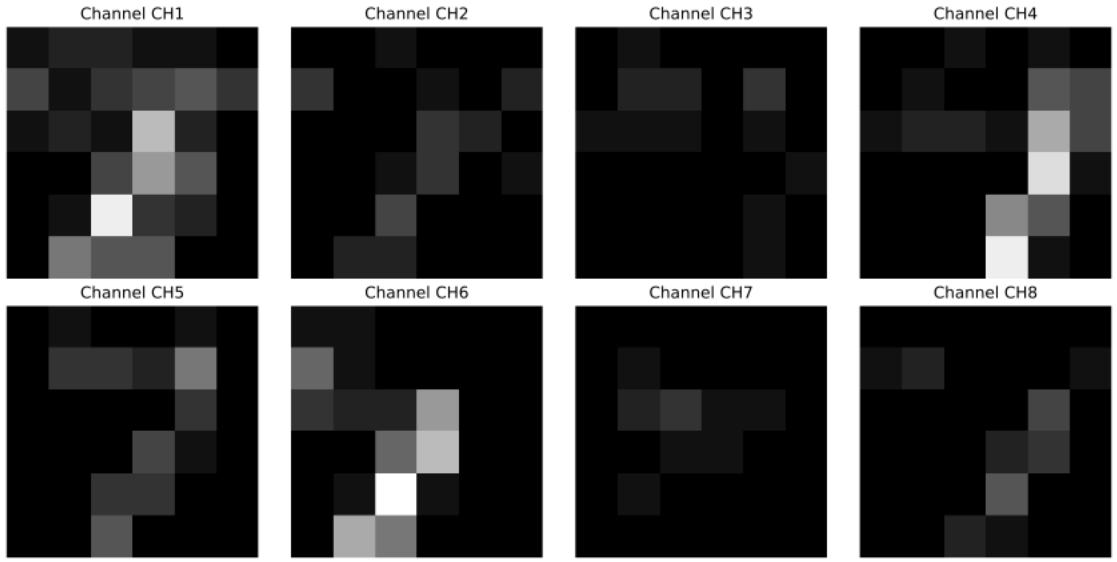
Results are Identical

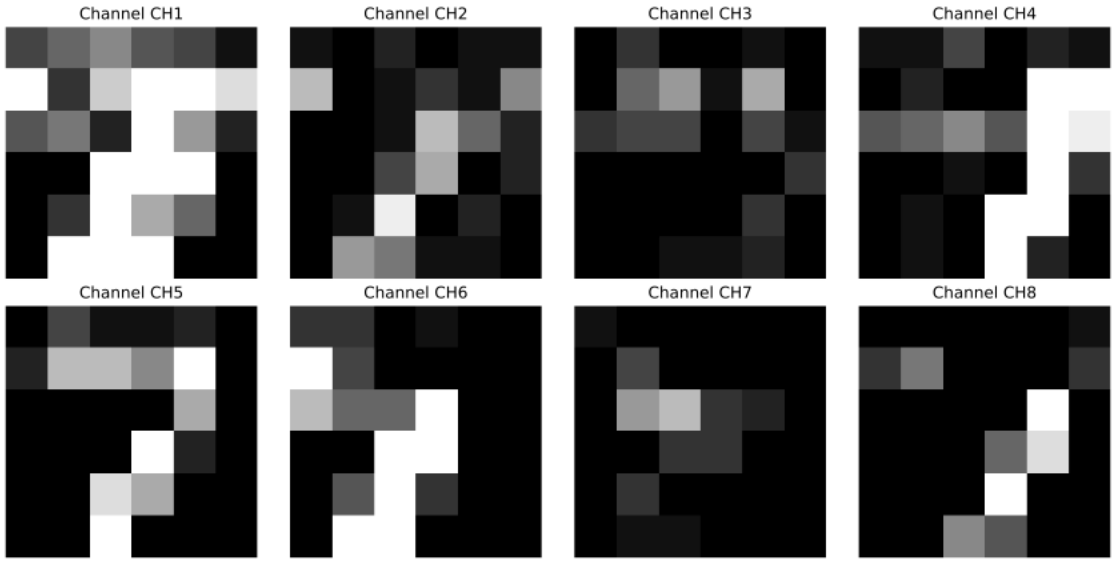
ADC Conversion for Conv2 Outputs

- Conv2 outputs are converted to digital signals for the fully-connected layer. ADCs perform this conversion by mapping an analog voltage range to digital codes.
- ADC Design and Reference Voltages:
  - **Critical Parameters:** ADC reference voltages determine conversion accuracy. ADC resolution is not very critical for this small network (see next slides).
  - **Low Reference Voltage:** Chosen to match the minimum expected input signal (e.g., 0.6 V).
  - **High Reference Voltage:** Set to the maximum expected analog input, for instance, 0.7875 V (matching the highest DAC value).
  - **Mapping Example: I**n a 4-bit ADC, 0.6 V is mapped to digital code **0** and 0.7875 V to digital code **15**.
- Floating Point Outputs in the Training Model:
  - The training model produces floating point outputs that are not quantized.
  - These outputs are directly fed into the fully-connected layer without scaling or clipping.
- Determining the Optimal High Reference (Vref):
  - Analyze the distribution of Conv2 layer outputs.
  - Use a statistical measure (e.g., selecting the 3σ level) to decide on the ADC high reference voltage.
  - This ensures that the majority of the data falls within the ADC’s dynamic range, matching the physical voltage limits.



Model (Python)

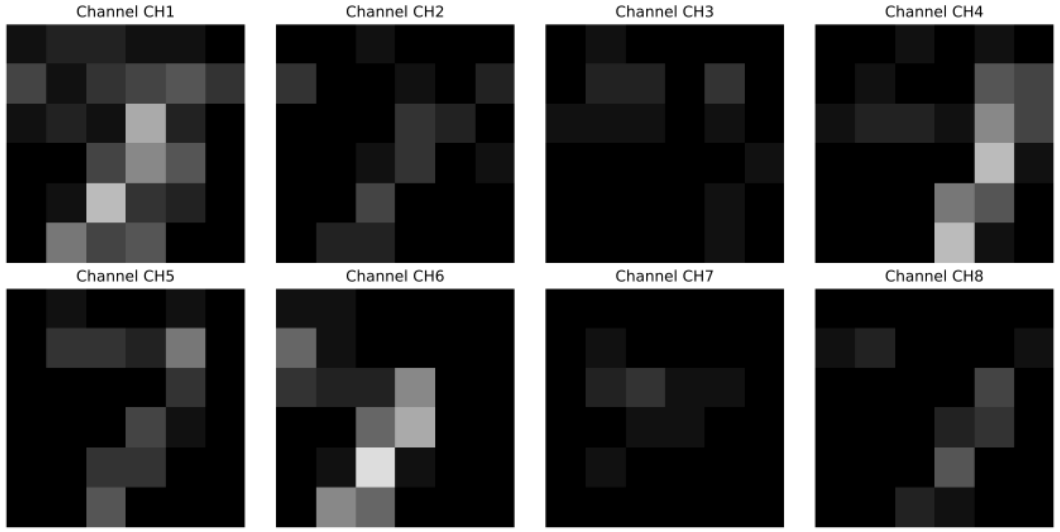




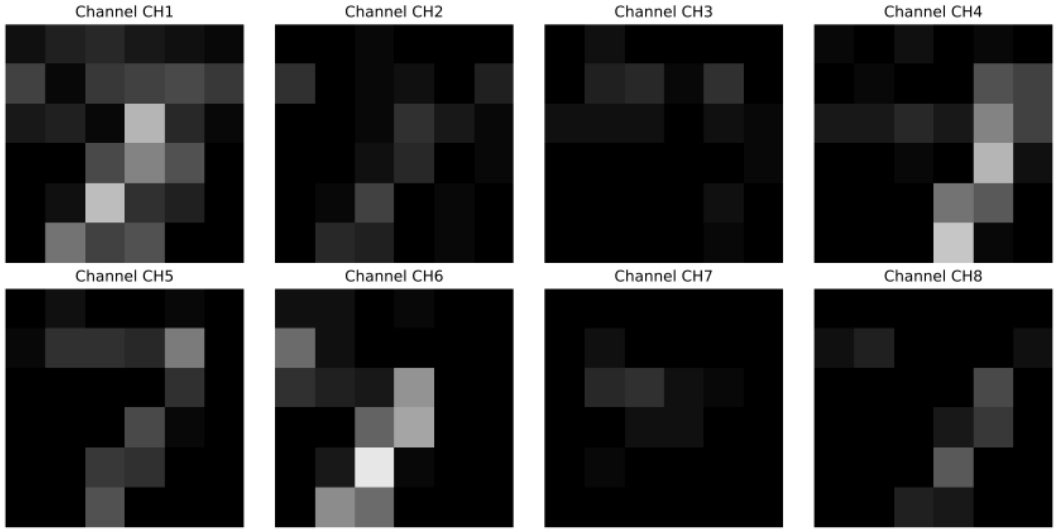
Verilog-A (4-bit ADC)
V_FS = 0.7875 V
V_ZS = 0.6 V

High Reference Voltage is changed

Verilog-A (4-bit ADC)
V_FS = 0.65 V
V_ZS = 0.6 V

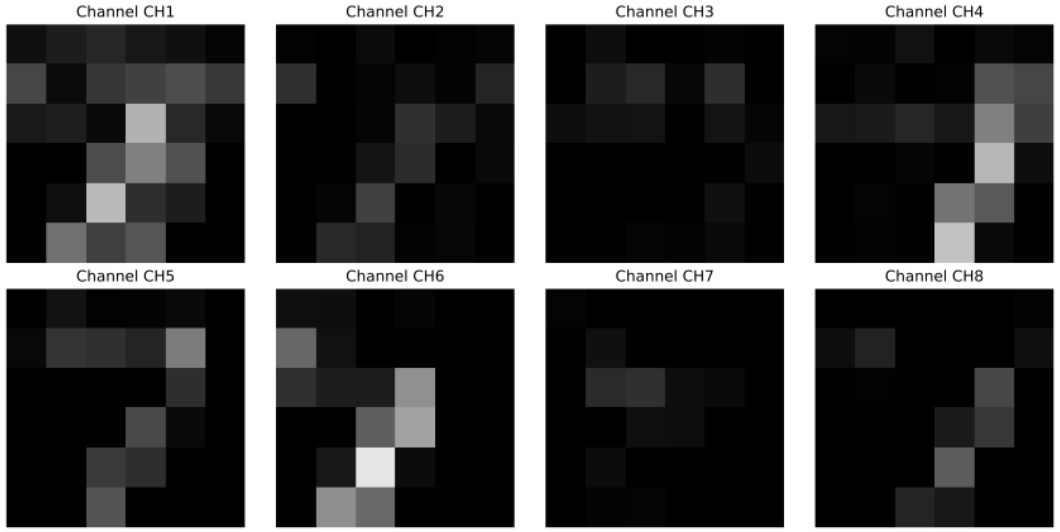


4-bit ADC

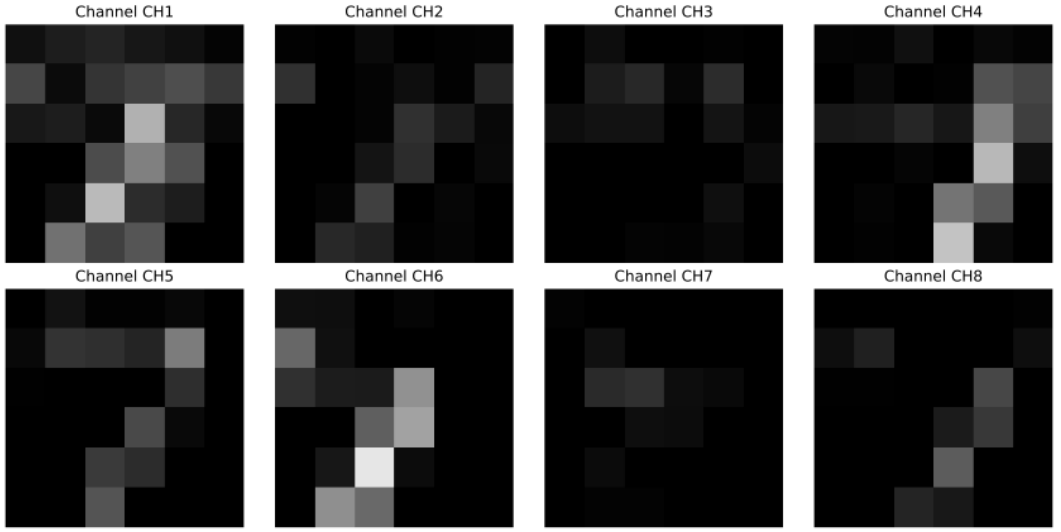


5-bit ADC

ADC resolution is not critical!



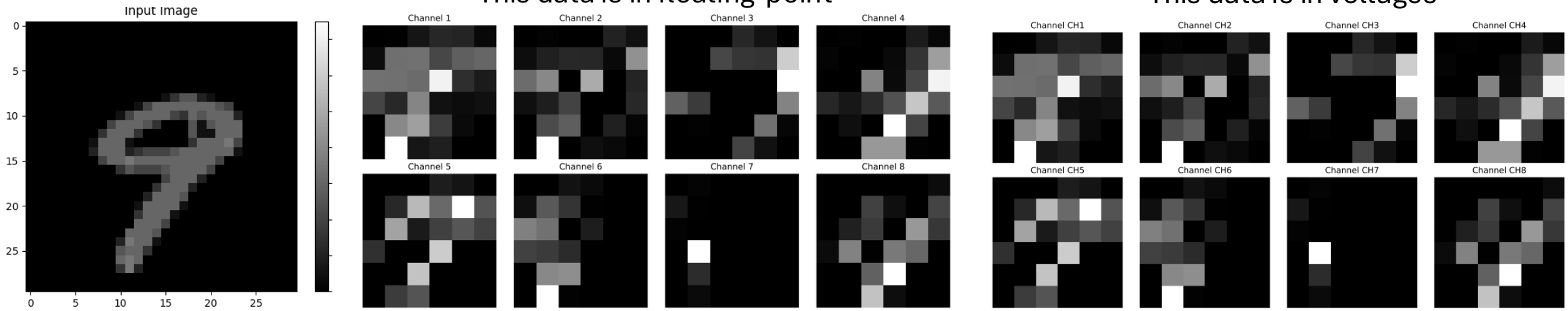
8-bit ADC



12-bit ADC

Conv2 output with imshow (Example 2)

This data is in floating-point

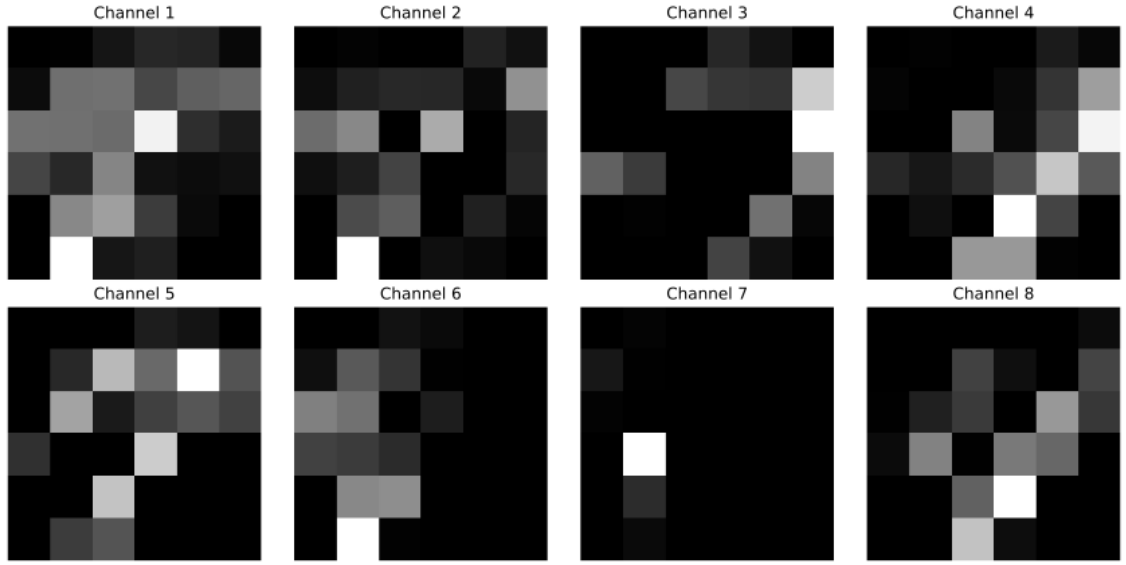


Pooling Layer 2 Output (8 Channels)
From Training Model (Python)

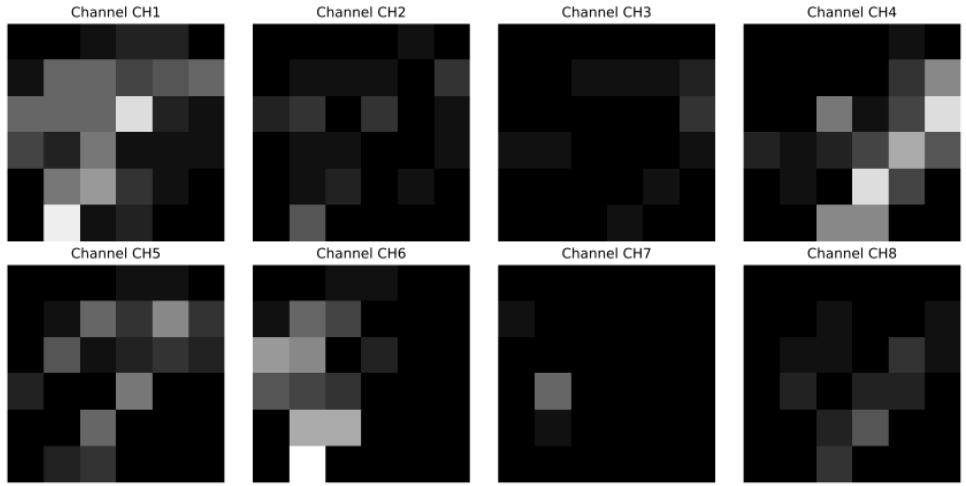
This data is in voltages

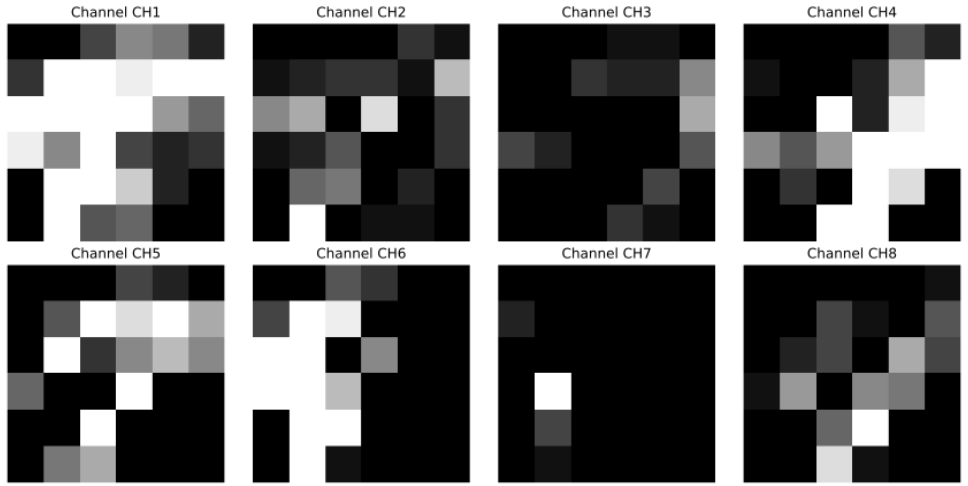
Pooling Layer 2 Output (8 Channels)
From Verilog-A (No ADC)

Results are Identical



Model (Python)





Verilog-A (4-bit ADC)
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High Reference Voltage is changed

Verilog-A (4-bit ADC)
V_FS = 0.65 V
V_ZS = 0.6 V