

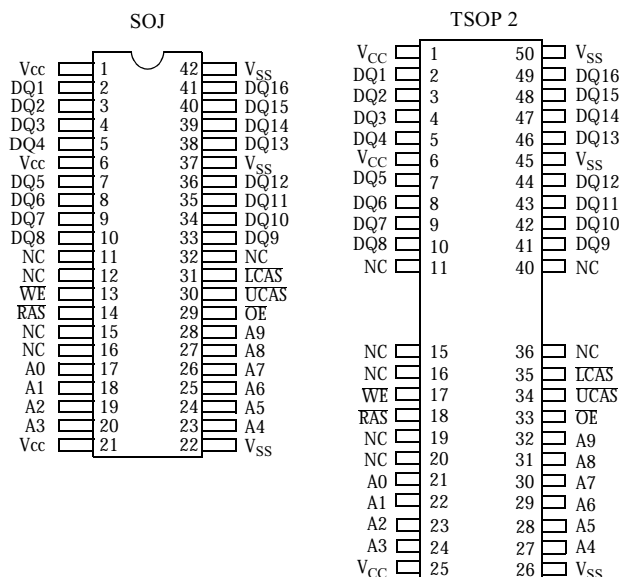


5V 1M×16 CMOS DRAM (EDO)

Features

- Organization: 1,048,576 words × 16 bits
- High speed
 - 45/50/60 ns $\overline{\text{RAS}}$ access time
 - 20/20/25 ns hyper page cycle time
 - 10/12/15 ns $\overline{\text{CAS}}$ access time
- Low power consumption
 - Active: 740 mW max (AS4C1M16E5-60)
 - Standby: 5.5 mW max, CMOS DQ
- Extended data out
- 1024 refresh cycles, 16 ms refresh interval
 - $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh Read-modify-write
- TTL-compatible, three-state DQ
- JEDEC standard package and pinout
 - 400 mil, 42-pin SOJ
 - 400 mil, 44/50-pin TSOP 2
- 5V power supply
- Industrial and commercial temperature available

Pin arrangement



Pin designation

Pin(s)	Description
A0 to A9	Address inputs
$\overline{\text{RAS}}$	Row address strobe
DQ1 to DQ16	Input/output
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{UCAS}}$	Column address strobe, upper byte
$\overline{\text{LCAS}}$	Column address strobe, lower byte
V_{CC}	Power
V_{SS}	Ground

Selection guide

	Symbol	-45	-50	-60	Unit
Maximum $\overline{\text{RAS}}$ access time	t_{RAC}	45	50	60	ns
Maximum column address access time	t_{AA}	23	25	30	ns
Maximum $\overline{\text{CAS}}$ access time	t_{CAC}	10	12	15	ns
Maximum output enable ($\overline{\text{OE}}$) access time	t_{OEA}	12	13	15	ns
Minimum read or write cycle time	t_{RC}	75	80	100	ns
Minimum hyper page mode cycle time	t_{HPC}	20	20	25	ns
Maximum operating current	I_{CC1}	155	145	135	mA
Maximum CMOS standby current	I_{CC5}	2.0	2.0	2.0	mA



Functional description

The AS4C1M16E5 is a high performance 16-megabit CMOS Dynamic Random Access Memory (DRAM) organized as 1,048,576 words \times 16 bits. The device is fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in personal and portable PCs, workstations, and multimedia and router switch applications.

The AS4C1M16E5 features hyper page mode operation where read and write operations within a single row (or page) can be executed at very high speed by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ inputs, respectively. Also, $\overline{\text{RAS}}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{\text{CAS}}$ assertion. The AS4C1M16E5 provides dual $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ for independent byte control of read and write access.

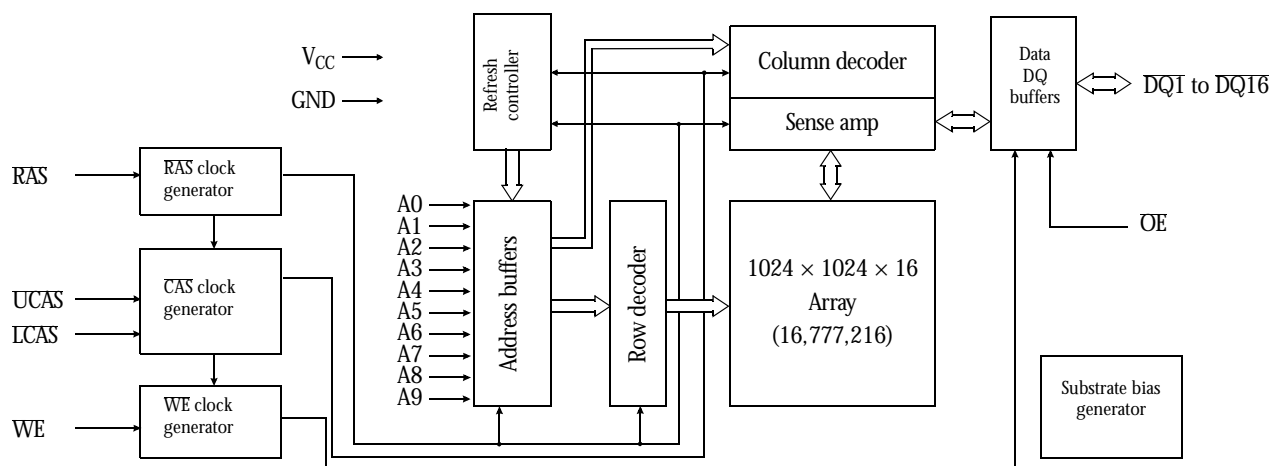
Extended data out (EDO), also known as 'hyper-page mode,' enables high speed operation. In contrast to 'fast-page mode' devices, data remains active on outputs after $\overline{\text{CAS}}$ is de-asserted high, giving system logic more time to latch the data. Use $\overline{\text{OE}}$ and $\overline{\text{WE}}$ to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrence of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ going high.

Refresh on the 1024 address combinations of A0 to A9 must be performed every 16 ms using:

- $\overline{\text{RAS}}$ -only refresh: $\overline{\text{RAS}}$ is asserted while $\overline{\text{CAS}}$ is held high. Each of the 1024 rows must be strobed. Outputs remain high impedance.
- Hidden refresh: $\overline{\text{CAS}}$ is held low while $\overline{\text{RAS}}$ is toggled. Outputs remain low impedance with previous valid data.
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh (CBR): At least one $\overline{\text{CAS}}$ is asserted prior to $\overline{\text{RAS}}$. Refresh address is generated internally. Outputs are high-impedance ($\overline{\text{OE}}$ and $\overline{\text{WE}}$ are don't care).
- Normal read or write cycles refresh the row being accessed.

The AS4C1M16E5 is available in the standard 42-pin plastic SOJ and 44/50-pin TSOP 2 packages, respectively. The AS4C1M16E5 device operates with a single power supply of $5\text{V} \pm 0.5\text{V}$ and provides TTL compatible inputs and outputs.

Logic block diagram



Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.4	–	V_{CC}	V
	V_{IL}	-0.5^{\dagger}	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	70	$^{\circ}\text{C}$
	Industrial	T_A	-40	85	$^{\circ}\text{C}$

$^{\dagger}V_{IL}$ min -3.0V for pulse widths less than 5 ns.

Recommended operating conditions apply throughout this document unless otherwise specified.



Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in}	-1.0	+7.0	V
Input voltage (DQs)	V_{DQ}	-1.0	$V_{CC} + 0.5$	V
Power supply voltage	V_{CC}	-1.0	+7.0	V
Storage temperature (plastic)	T_{STG}	-65	+150	°C
Soldering temperature × time	T_{SOLDER}	–	260×10	°C × sec
Power dissipation	P_D	–	1	W
Short circuit output current	I_{out}	–	50	mA

Truth table

Operation		RAS	LCAS	UCAS	WE	OE	Addresses		DQ0 to DQ15	Notes
							t_R	t_C		
Standby		H	H to X	H to X	X	X	X	X	High-Z	
Word read		L	L	L	H	L	ROW	COL	Data out	
Lower byte read		L	L	H	H	L	ROW	COL	Lower byte, Upper byte, Data out	
Upper byte read		L	H	L	H	L	ROW	COL	Lower byte, Data out, Upper byte	
Word (early) write		L	L	L	L	X	ROW	COL	Data in	
Lower byte (early) write		L	L	H	L	X	ROW	COL	Lower byte, Data in, Upper byte, High-Z	
Upper byte (early) write		L	H	L	L	X	ROW	COL	Lower byte, High-Z, Upper byte, Data in	
Read write		L	L	L	H to L	L to H	ROW	COL	Data out, Data in	1,2
EDO read	1st cycle	L	H to L	H to L	H	L	ROW	COL	Data out	2
	2nd cycle	L	H to L	H to L	H	L	n/a	COL	Data out	2
	Any cycle	L	L to H	L to H	H	L	n/a	n/a	Data out	2
EDO write	1st cycle	L	H to L	H to L	L	X	ROW	COL	Data in	1
	2nd cycle	L	H to L	H to L	L	X	n/a	COL	Data in	1
EDO read write	1st cycle	L	H to L	H to L	H to L	L to H	ROW	COL	Data out, Data in	1,2
	2nd cycle	L	H to L	H to L	H to L	L to H	n/a	COL	Data out, Data in	1,2
RAS only refresh		L	H	H	X	X	ROW	n/a	High Z	
CBR refresh		H to L	L	L	H	X	X	X	High Z	3



DC electrical characteristics

Parameter	Symbol	Test conditions	-45		-50		-60		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input leakage current	I_{IL}	$0V \leq V_{in} \leq V_{CC} \text{ (max)}$ Pins not under test = 0V	-5	+5	-5	+5	-5	+5	μA	
Output leakage current	I_{OL}	D_{OUT} disabled, $0V \leq V_{out} \leq V_{CC} \text{ (max)}$	-5	+5	-5	+5	-5	+5	μA	
Operating power supply current	I_{CC1}	\overline{RAS} , \overline{UCAS} , \overline{LCAS} , Address cycling; $t_{RC} = \text{min}$	-	155	-	145	-	135	mA	4,5
TTL standby power supply current	I_{CC2}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} \geq V_{IH}$, all other inputs at V_{IH} or V_{IL}	-	2.0	-	2.0	-	2.0	mA	
Average power supply current, \overline{RAS} refresh mode or CBR	I_{CC3}	\overline{RAS} cycling, $\overline{UCAS} = \overline{LCAS} \geq V_{IH}$, $t_{RC} = \text{min}$ of \overline{RAS} low after \overline{XCAS} low.	-	145	-	135	-	125	mA	4
EDO page mode average power supply current	I_{CC4}	$\overline{RAS} = V_{IL}$, \overline{UCAS} or \overline{LCAS} , address cycling: $t_{HPC} = \text{min}$	-	130	-	120	-	110	mA	4, 5
CMOS standby power supply current	I_{CC5}	$\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC} - 0.2V$, $F = 0$	-	2.0	-	2.0	-	2.0	mA	
Output voltage	V_{OH}	$I_{OUT} = -5.0 \text{ mA}$	2.4	-	2.4	-	2.4	-	V	
	V_{OL}	$I_{OUT} = 4.2 \text{ mA}$	-	0.4	-	0.4	-	0.4	V	
\overline{CAS} before \overline{RAS} refresh current	I_{CC6}	\overline{RAS} , \overline{UCAS} or \overline{LCAS} cycling, $t_{RC} = \text{min}$	-	155	-	145	-	135	mA	



AC parameters common to all waveforms

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random read or write cycle time	75	–	80	–	100	–	ns	
t_{RP}	\overline{RAS} precharge time	30	–	30	–	40	–	ns	
t_{RAS}	\overline{RAS} pulse width	45	10K	50	10K	60	10K	ns	
t_{CAS}	\overline{CAS} pulse width	8	10K	8	10K	10	10K	ns	
t_{RCD}	\overline{RAS} to \overline{CAS} delay time	15	35	15	35	15	43	ns	9
t_{RAD}	\overline{RAS} to column address delay time	8	25	9	25	10	30	ns	10
t_{RSH}	\overline{CAS} to \overline{RAS} hold time	10	–	10	–	10	–	ns	
t_{CSH}	\overline{RAS} to \overline{CAS} hold time	40	–	40	–	50	–	ns	
t_{CRP}	\overline{CAS} to \overline{RAS} precharge time	5	–	5	–	5	–	ns	
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns	
t_{RAH}	Row address hold time	8	–	8	–	10	–	ns	
t_T	Transition time (rise and fall)	1	50	1	50	1	50	ns	7,8
t_{REF}	Refresh period	–	16	–	16	–	16	ms	6
t_{CP}	\overline{CAS} precharge time	8	–	8	–	10	–	ns	
t_{RAL}	Column address to \overline{RAS} lead time	25	–	25	–	30	–	ns	
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns	
t_{CAH}	Column address hold time	8	–	8	–	10	–	ns	

Read cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access time from \overline{RAS}	–	45	–	50	–	60	ns	9
t_{CAC}	Access time from \overline{CAS}	–	10	–	12	–	15	ns	9,16
t_{AA}	Access time from address	–	23	–	25	–	30	ns	10,16
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns	
t_{RCH}	Read command hold time to \overline{CAS}	0	–	0	–	0	–	ns	12
t_{RRH}	Read command hold time to \overline{RAS}	0	–	0	–	0	–	ns	12



Write cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write command setup time	0	–	0	–	0	–	ns	14
t_{WCH}	Write command hold time	10	–	10	–	10	–	ns	14
t_{WP}	Write command pulse width	10	–	10	–	10	–	ns	
t_{RWL}	Write command to \overline{RAS} lead time	10	–	10	–	10	–	ns	
t_{CWL}	Write command to \overline{CAS} lead time	8	–	8	–	10	–	ns	
t_{DS}	Data-in setup time	0	–	0	–	0	–	ns	15
t_{DH}	Data-in hold time	8	–	8	–	10	–	ns	15

Read-modify-write cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-write cycle time	105	–	113	–	135	–	ns	
t_{RWD}	\overline{RAS} to \overline{WE} delay time	65	–	67	–	77	–	ns	14
t_{CWD}	\overline{CAS} to \overline{WE} delay time	30	–	32	–	35	–	ns	14
t_{AWD}	Column address to \overline{WE} delay time	40	–	42	–	47	–	ns	14

Refresh cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CSR}	\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS})	5	–	5	–	5	–	ns	6
t_{CHR}	\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS})	8	–	8	–	10	–	ns	6
t_{RPC}	\overline{RAS} precharge to \overline{CAS} hold time	0	–	0	–	0	–	ns	
t_{CPT}	\overline{CAS} precharge time (CBR counter test)	10	–	10	–	10	–	ns	



Hyper page mode cycle

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{CPWD}	$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	45	–	45	–	52	–	ns	
t _{CPA}	Access time from $\overline{\text{CAS}}$ precharge	–	28	–	28	–	35	ns	16
t _{RASP}	$\overline{\text{RAS}}$ pulse width	45	100K	50	100K	60	100K	ns	
t _{DOH}	Previous data hold time from $\overline{\text{CAS}}$	5	–	5	–	5	–	ns	
t _{REZ}	Output buffer turn off delay from $\overline{\text{RAS}}$	0	13	0	13	0	15	ns	
t _{WEZ}	Output buffer turn off delay from $\overline{\text{WE}}$	0	13	0	13	0	15	ns	
t _{OEZ}	Output buffer turn off delay from $\overline{\text{OE}}$	0	13	0	13	0	15	ns	
t _{HPC}	Hyper page mode cycle time	20	–	20	–	25	–	ns	
t _{HPRWC}	Hyper page mode RMW cycle	47	–	47	–	56	–	ns	
t _{RHCP}	$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$	30	–	30	–	35	–	ns	

Output enable

Symbol	Parameter	-45		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t _{CLZ}	$\overline{\text{CAS}}$ to output in Low Z	0	–	0	–	0	–	ns	11
t _{ROH}	$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	8	–	8	–	10	–	ns	
t _{OEa}	$\overline{\text{OE}}$ access time	–	13	–	13	–	15	ns	
t _{OED}	$\overline{\text{OE}}$ to data delay	13	–	13	–	15	–	ns	
t _{OEZ}	Output buffer turnoff delay from $\overline{\text{OE}}$	0	13	0	13	0	15	ns	11
t _{OEh}	$\overline{\text{OE}}$ command hold time	10	–	10	–	10	–	ns	
t _{OLZ}	$\overline{\text{OE}}$ to output in Low Z	0	–	0	–	0	–	ns	
t _{OFF}	Output buffer turn-off time	0	13	0	13	0	15	ns	11,13



Notes

- 1 Write cycles may be byte write cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
- 2 Read cycles may be byte read cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
- 3 One $\overline{\text{CAS}}$ must be active (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$).
- 4 I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC6} are dependent on frequency.
- 5 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 6 An initial pause of 200 μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- 7 AC Characteristics assume $t_{\text{T}} = 2 \text{ ns}$. All AC parameters are measured with a load as described in AC test conditions below.
- 8 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- 9 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
- 10 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
- 11 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).
- 12 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 13 t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. t_{OFF} is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
- 14 t_{WCS} , t_{WCH} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only.
If $t_{\text{WS}} \geq t_{\text{WS}}(\text{min})$ and $t_{\text{WH}} \geq t_{\text{WH}}(\text{min})$, the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle.
If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- 15 These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-write cycles.
- 16 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}
- 17 $t_{\text{ASC}} \geq t_{\text{CP}}$ to achieve $t_{\text{PC}}(\text{min})$ and $t_{\text{CPA}}(\text{max})$ values.
- 18 These parameters are sampled and not 100% tested.
- 19 These characteristics apply to AS4C1M16E5 5V devices.

AC test conditions

- Access times are measured with output reference levels of
 $V_{\text{OH}} = 2.4\text{V}$ and $V_{\text{OL}} = 0.4\text{V}$,
 $V_{\text{IH}} = 2.4\text{V}$ and $V_{\text{IL}} = 0.8\text{V}$
- Input rise and fall times: 2 ns

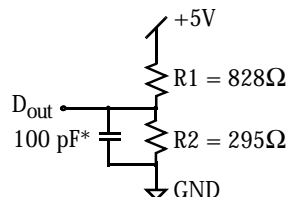


Figure A: Equivalent output load

Key to switching waveforms



Rising input



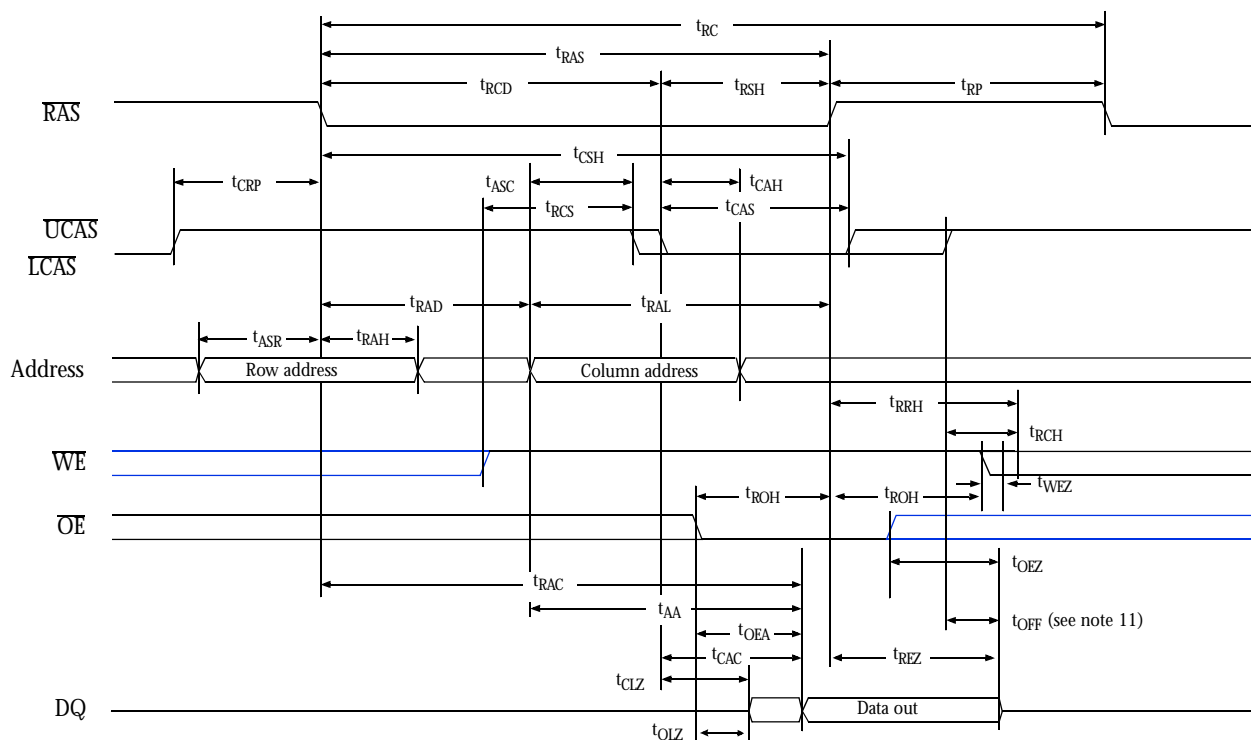
Falling input



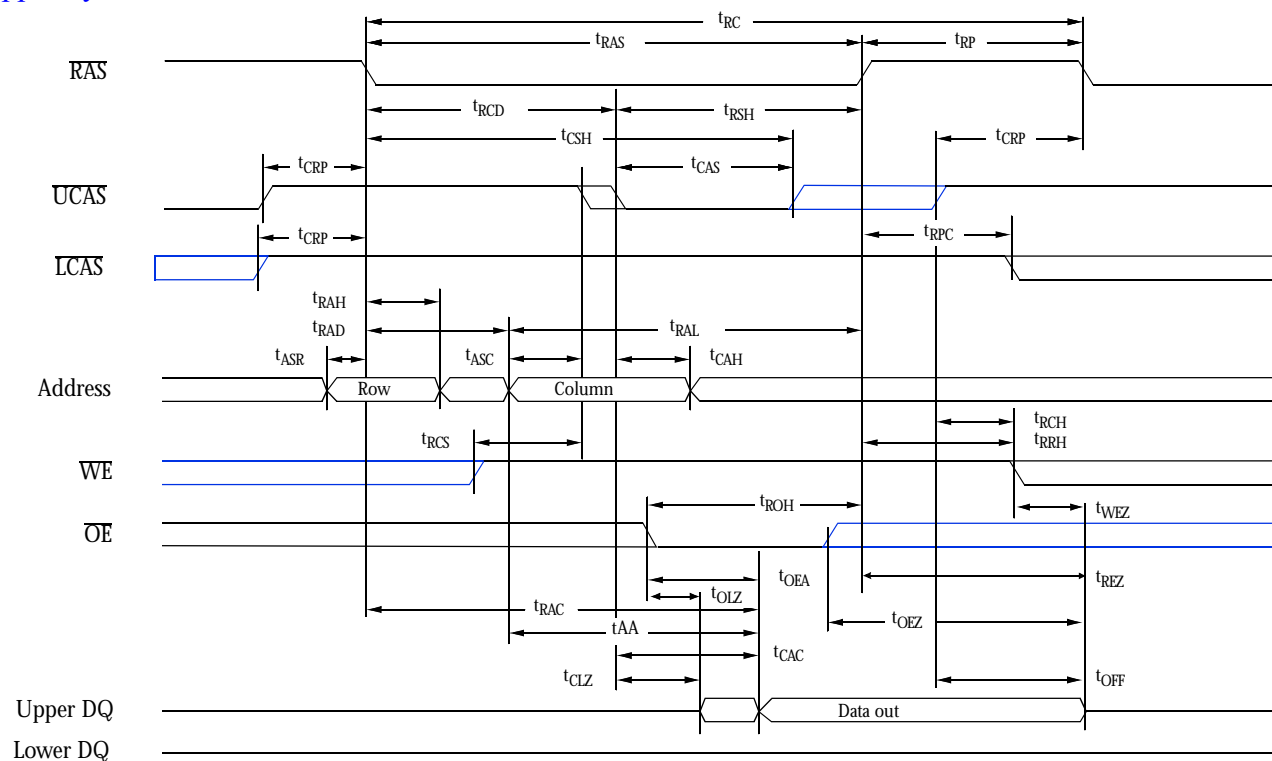
Undefined output/don't care



Read waveform



Upper byte read waveform



The diagram illustrates the timing relationships for a 2D64T160000 memory device. The signals shown are RAS, LCAS, UCAS, Address, WE, OE, Upper DQ, and Lower DQ. The timing parameters are defined as follows:

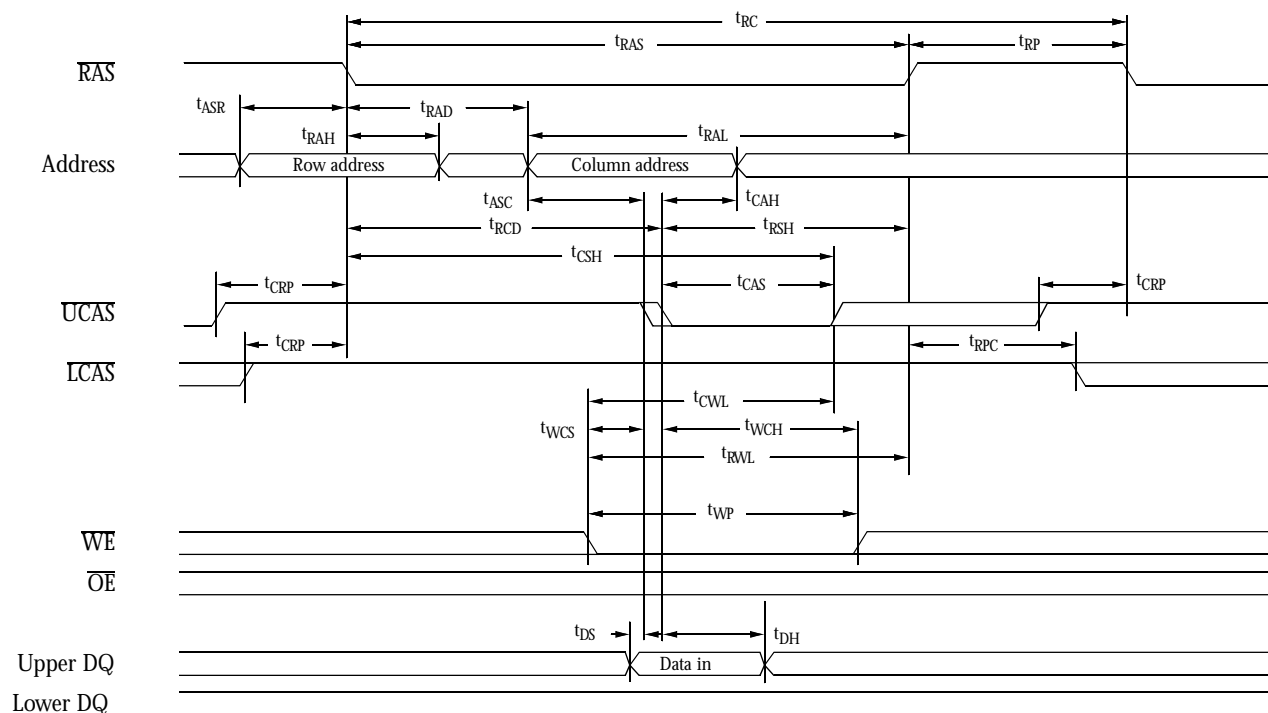
- t_{RAS} : RAS access time
- t_{RC} : RAS to CAS delay
- t_{RP} : RAS precharge time
- t_{RCD} : RAS to CAS delay
- t_{RSH} : RAS to SH output delay
- t_{CRP} : CAS to RAS precharge time
- t_{CAS} : CAS access time
- t_{RPC} : RAS to CAS precharge time
- t_{RAH} : RAS to AH output delay
- t_{RAD} : RAS to AD output delay
- t_{ASR} : Address strobe to RAS delay
- t_{ASC} : Address strobe to CAS delay
- t_{RCS} : RAS to CAS delay
- t_{RAL} : RAS to AL output delay
- t_{CAH} : CAS to AH output delay
- t_{RCH} : RAS to CH output delay
- t_{RRH} : RAS to RH output delay
- t_{ROH} : RAS to OH output delay
- t_{WEZ} : WE to Z output delay
- t_{OEA} : OE to A output delay
- t_{OLZ} : OE to L output delay
- t_{RAC} : RAS to AC output delay
- t_{AA} : RAS to AA output delay
- t_{CLZ} : CAS to L output delay
- t_{CAC} : CAS to C output delay
- t_{OEZ} : OE to Z output delay
- t_{OFF} : OE to F output delay

The diagram illustrates the timing relationships for a memory device. The signals and their associated timing parameters are as follows:

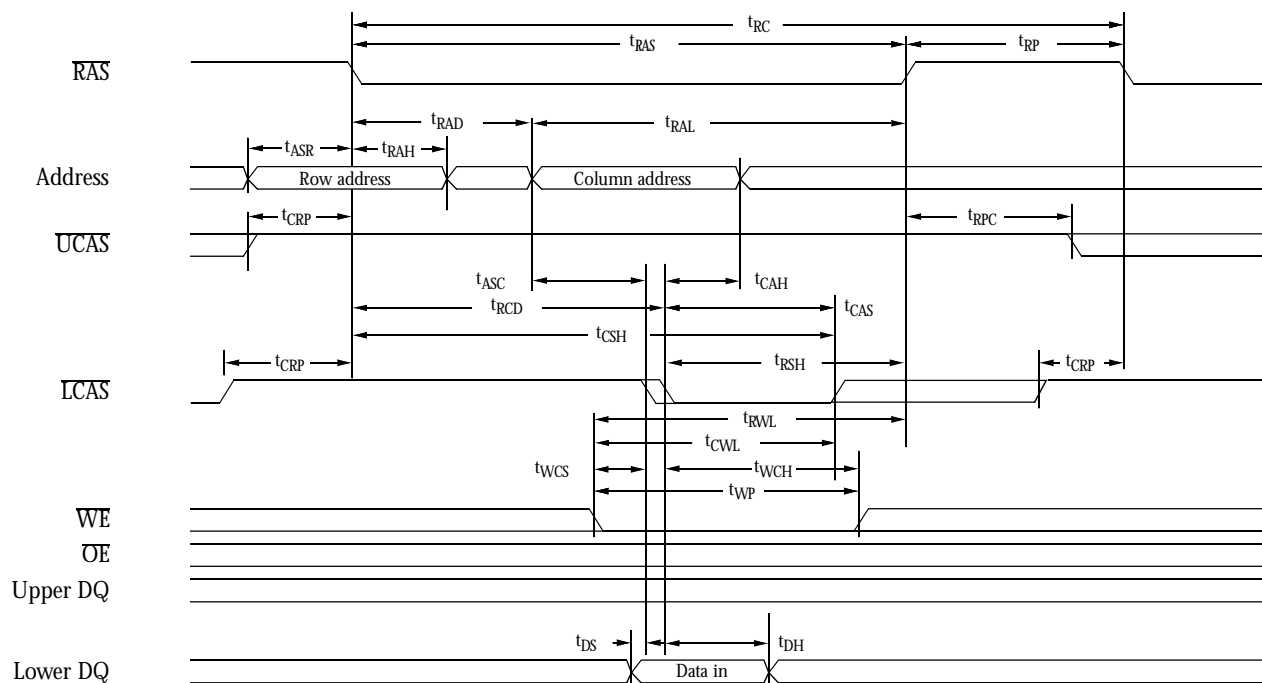
- RAS**: t_{RAS} (RAS to data), t_{RC} (RAS to column address), t_{RP} (RAS precharge).
- UCAS, ICAS**: t_{CRP} (UCAS/ICAS precharge), t_{RCD} (UCAS/ICAS to RAS), t_{CAS} (UCAS/ICAS to data), t_{RAD} (UCAS/ICAS to row address), t_{ASC} (UCAS/ICAS to column address), t_{RAH} (UCAS/ICAS to row address hold), t_{CAH} (UCAS/ICAS to column address hold).
- Address**: t_{ASR} (Address setup), t_{RAH} (Row address hold), t_{CAH} (Column address hold).
- WE**: t_{WCS} (WE to column address), t_{WCH} (WE to column address hold), t_{WP} (WE precharge), t_{WCH} (WE to column address hold).
- OE**: t_{DS} (OE to data), t_{DH} (OE to data hold).
- DQ**: t_{DS} (OE to data), t_{DH} (OE to data hold).



Upper byte early write waveform

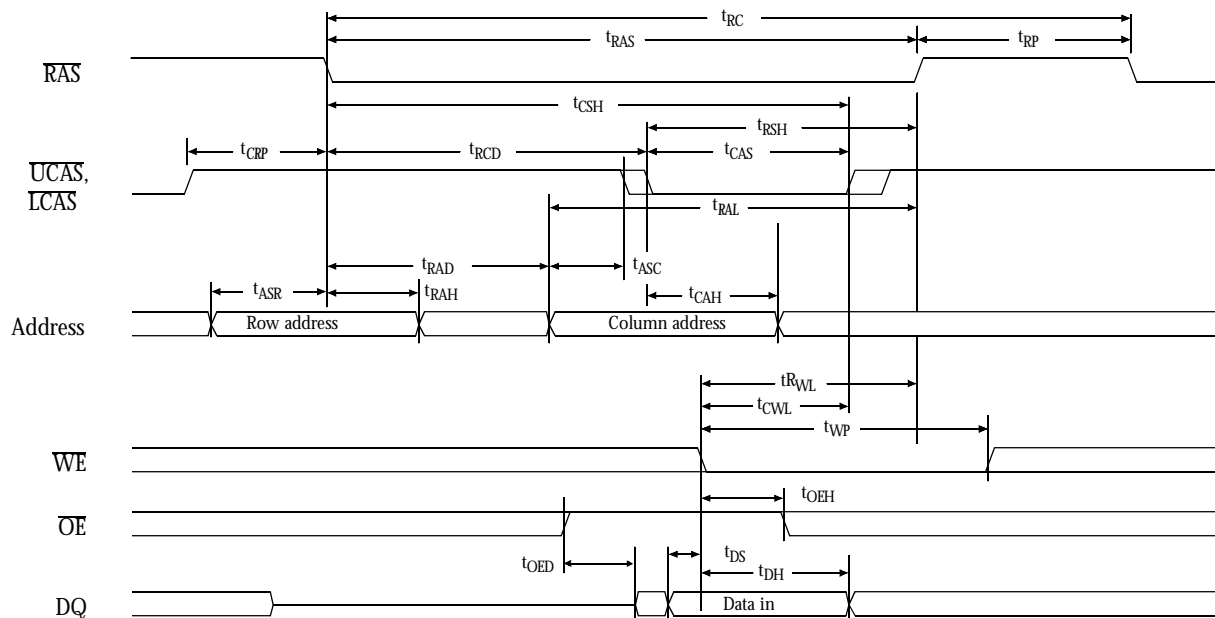


Lower byte early write waveform

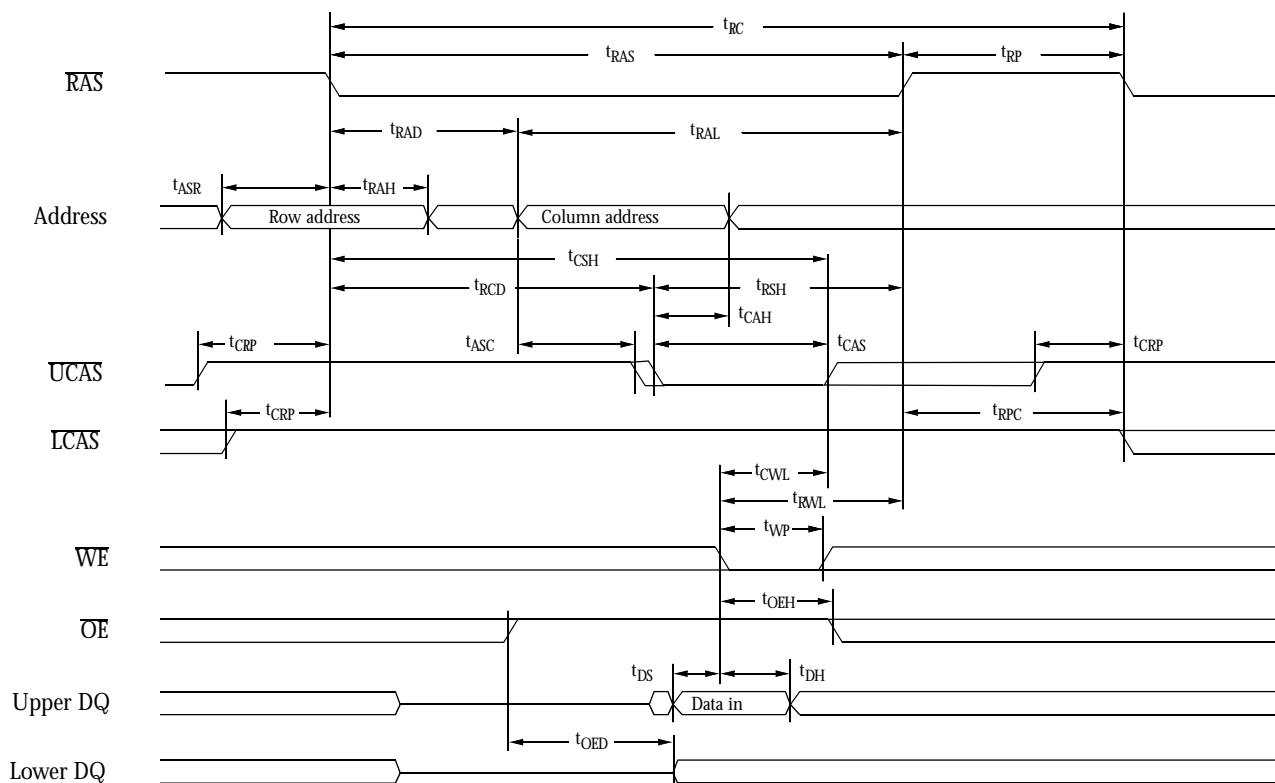




Write waveform

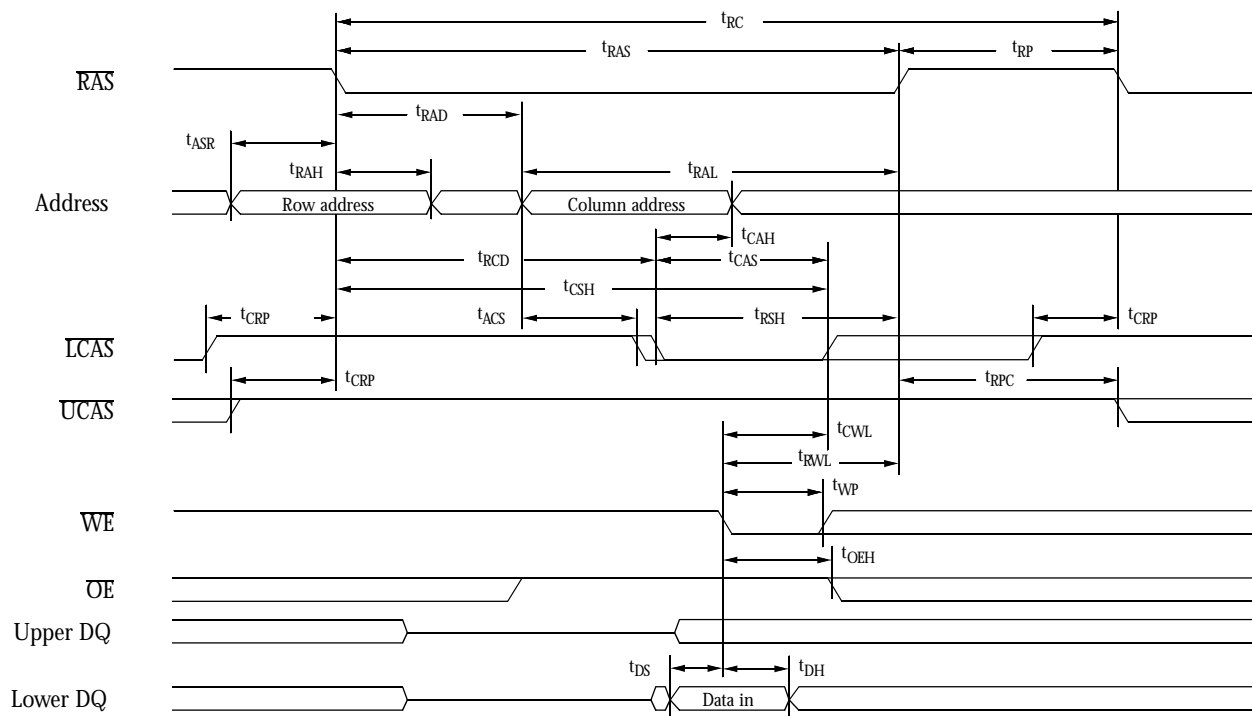
 $\overline{\text{OE}}$ controlled

Upper byte write waveform

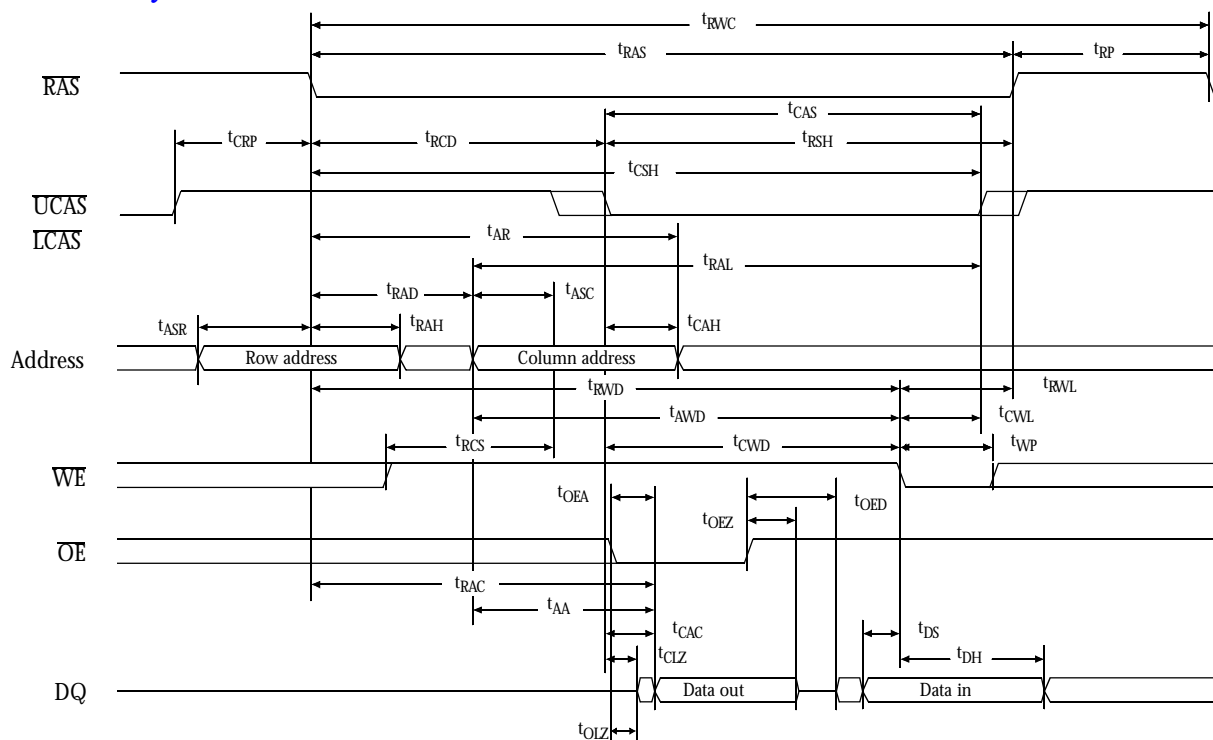
 $\overline{\text{OE}}$ controlled



Lower byte write waveform

 \overline{OE} controlled

Read-modify-write waveform



The diagram illustrates the timing relationships for a 256Kbit DRAM. The signals and their associated timing parameters are as follows:

- RAS**: t_{RAS} (RAS access time), t_{RVC} (RAS to VCS delay), t_{RP} (RAS precharge time).
- UCAS**: t_{RCD} (RAS to CAS delay), t_{CSH} (CAS high pulse width), t_{CAS} (CAS access time), t_{RSH} (RAS to SH delay), t_{CRP} (CAS to RAS precharge time).
- LCAS**: t_{CRP} (CAS to RAS precharge time), t_{RPC} (RAS to CAS precharge time).
- Address**: t_{ASR} (Address strobe to RAS delay), t_{RAD} (Address strobe to RAS delay), t_{RAH} (Address strobe to RAS delay), t_{ACS} (Address strobe to CAS delay), t_{RAL} (Address strobe to RAS delay), t_{CAH} (Address strobe to CAS delay).
- WE**: t_{RCS} (RAS to CAS delay), t_{RWD} (RAS to WE delay), t_{AWD} (Address strobe to WE delay), t_{CWL} (CAS to WE delay), t_{RWL} (RAS to WE delay), t_{WP} (WE precharge time).
- OE**: t_{OEA} (OE enable to RAS delay), t_{OLZ} (OE enable to RAS delay), t_{OED} (OE enable to RAS delay), t_{DSH} (OE enable to RAS delay), t_{DS} (OE enable to RAS delay).
- Upper input**: t_{CLZ} (OE enable to RAS delay), t_{CAC} (OE enable to RAS delay), t_{AA} (OE enable to RAS delay).
- Upper output**: t_{RAC} (RAS to CAS delay), t_{OEZ} (OE enable to RAS delay).
- Lower input**: t_{OED} (OE enable to RAS delay).
- Lower output**: t_{OED} (OE enable to RAS delay).

The diagram illustrates the timing relationships between various DRAM control and data signals. The signals shown are:

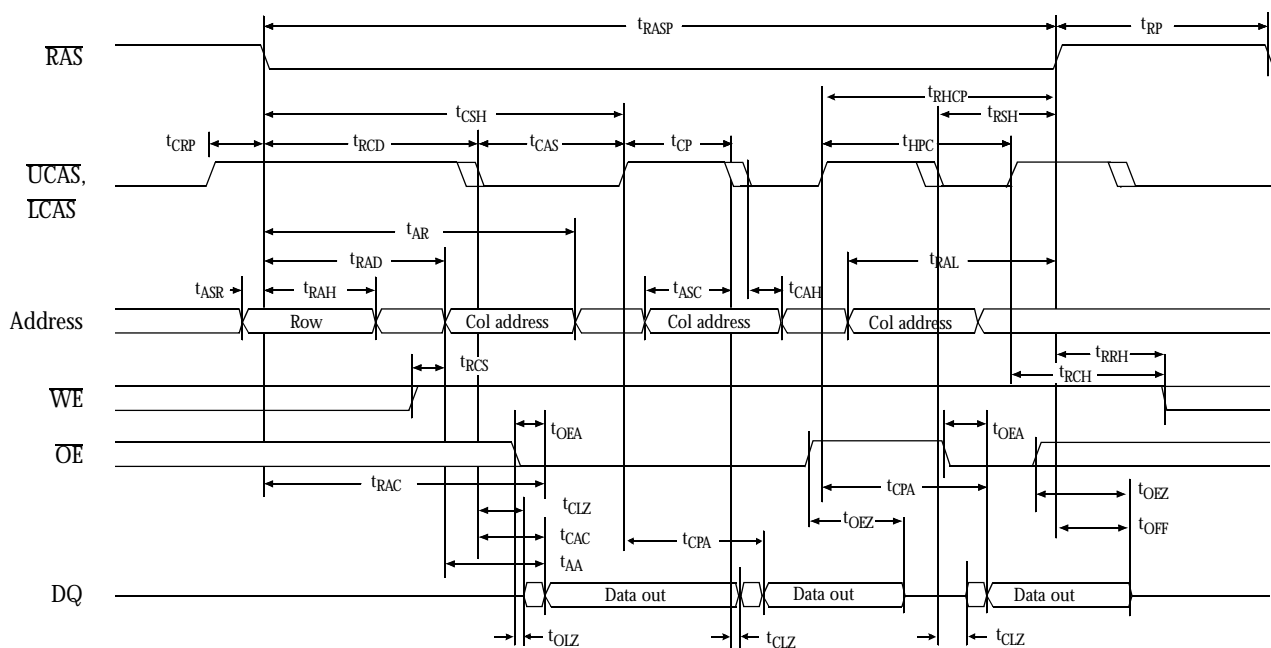
- RAS**: Row Address Strobe
- UCAS**: Universal Column Address Strobe
- LCAS**: Local Column Address Strobe
- Address**: Split into Row address and Column address.
- WE**: Write Enable
- OE**: Output Enable
- Upper input / Upper output**: Data bus for upper memory bank
- Lower input / Lower output**: Data bus for lower memory bank

Key timing parameters indicated by arrows include:

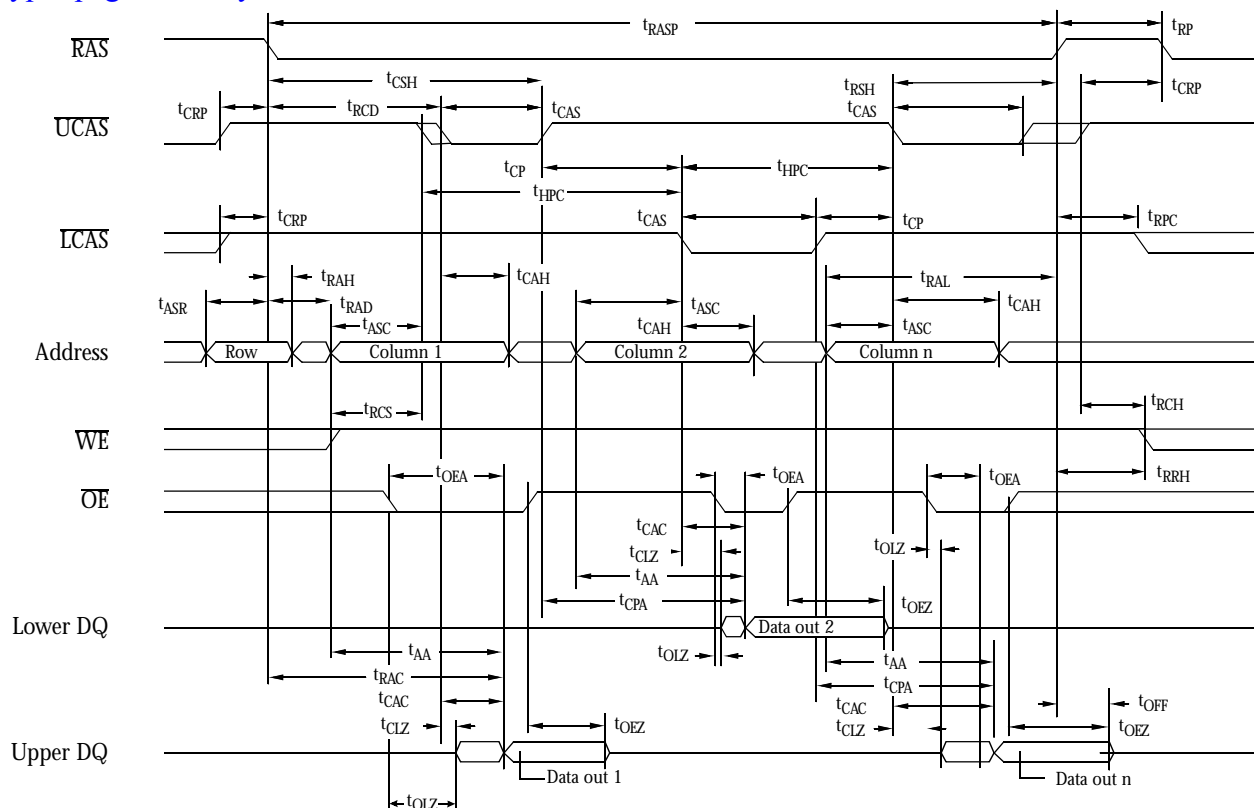
- t_{RAS} , t_{RWC} , t_{RP}
- t_{CRP} , t_{RPC}
- t_{RCD} , t_{CSH} , t_{CAS} , t_{RSH}
- t_{RAD} , t_{ASR} , t_{ACS} , t_{CAH} , t_{RAL}
- t_{RAH}
- t_{RWD} , t_{AWD} , t_{CWL} , t_{RWL}
- t_{RCS} , t_{CWD} , t_{WP}
- t_{OEA} , t_{OLZ} , t_{OED}
- t_{DH} , t_{DS}
- t_{TRAC} , t_{AA} , t_{CAC} , t_{CLZ} , t_{OEZ}



Hyper page mode read waveform



Hyper page mode byte write waveform



The diagram illustrates the timing relationships for a 2D DRAM array. The signals and their associated timing parameters are as follows:

- RAS:** Timing parameters include t_{RAH} (RAS access hold), t_{RASP} (RAS access period), and t_{RWL} (RAS write level).
- UCAS, LCAS:** Timing parameters include t_{CRP} (UCAS/LCAS setup), t_{RCD} (RAS to UCAS/LCAS delay), t_{CSH} (UCAS/LCAS setup), t_{CAS} (UCAS/LCAS access), t_{ASC} (UCAS/LCAS setup), t_{WCS} (UCAS/LCAS write), t_{CP} (UCAS/LCAS period), t_{CAH} (UCAS/LCAS hold), and t_{RSH} (UCAS/LCAS setup).
- Address:** Timing parameters include t_{ASR} (Address setup), t_{RAD} (Address read delay), t_{AR} (Address read), and t_{RAL} (Address read level).
- WE:** Timing parameters include t_{WCH} (WE setup), t_{CWL} (WE write level), t_{WP} (WE write period), and t_{WOH} (WE write hold).
- OE:** Timing parameters include t_{HDR} (OE hold delay), t_{DS} (OE data setup), t_{DH} (OE data hold), and t_{OED} (OE output delay).
- DQ:** Data in/out signals.

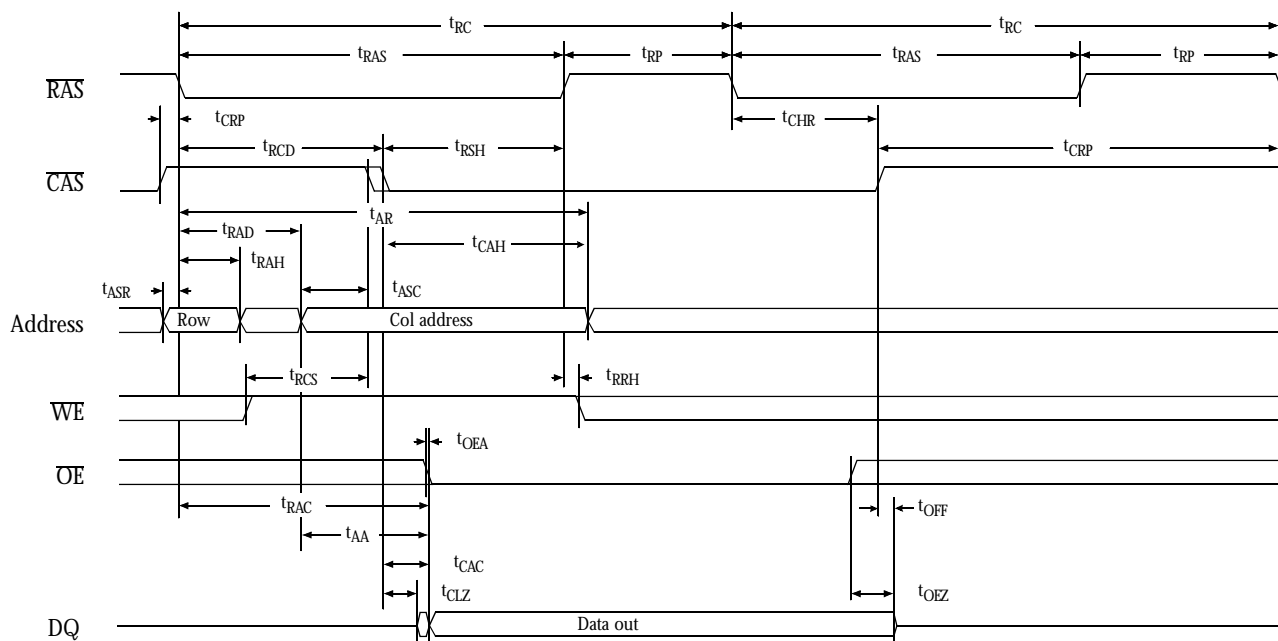
The diagram illustrates the timing relationships for a 2D array DRAM. The signals shown are RAS, UCAS, LCAS, Address, WE, OE, and Data (Lower DQ, Upper DQ). The Address signal is divided into Row and Column (Column 1, Column 2, ..., Column n) phases. The Data signal is divided into Data in 1, Data in 2, and Data in n phases. The timing parameters are defined as follows:

- t_{RAS} : RAS to CAS delay
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS to RAS delay
- t_{HPC} : High period of CAS
- t_{CP} : CAS to Precharge delay
- t_{RAD} : RAS to Address delay
- t_{RAH} : RAS to Address delay
- t_{ASC} : Address to CAS delay
- t_{CAH} : Address to CAS delay
- t_{WCS} : Write to CAS delay
- t_{WP} : Write to Precharge delay
- t_{CWL} : CAS to Write delay
- t_{DS} : Data to Strobe delay
- t_{DH} : Data to Hold delay

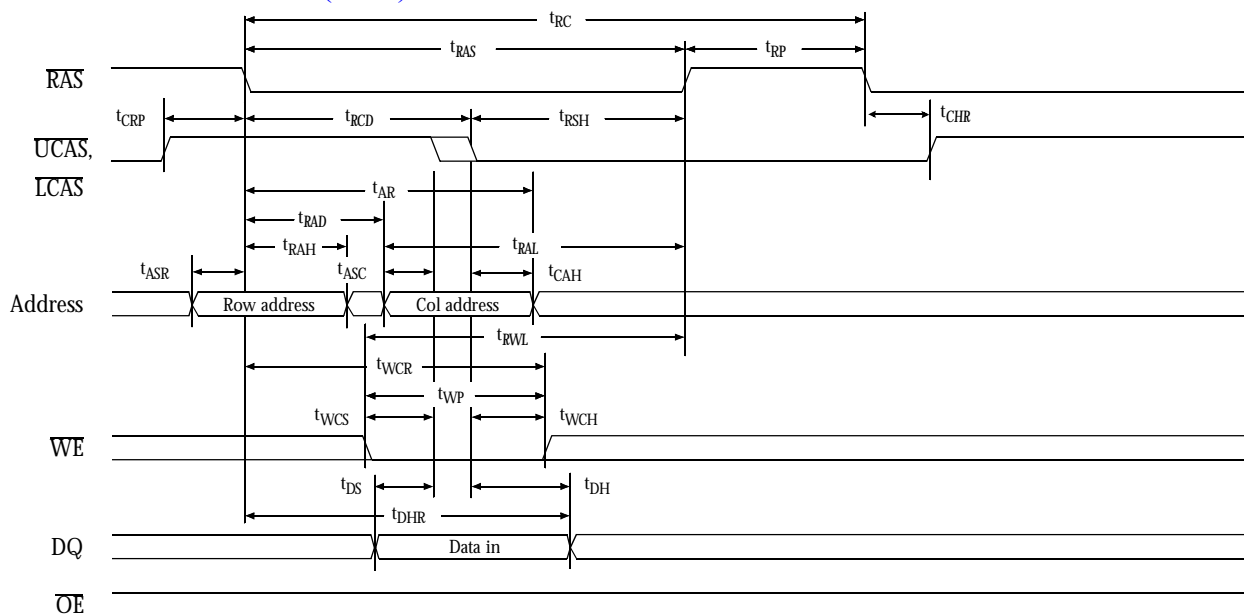
[illegible]



Hidden refresh waveform (read)

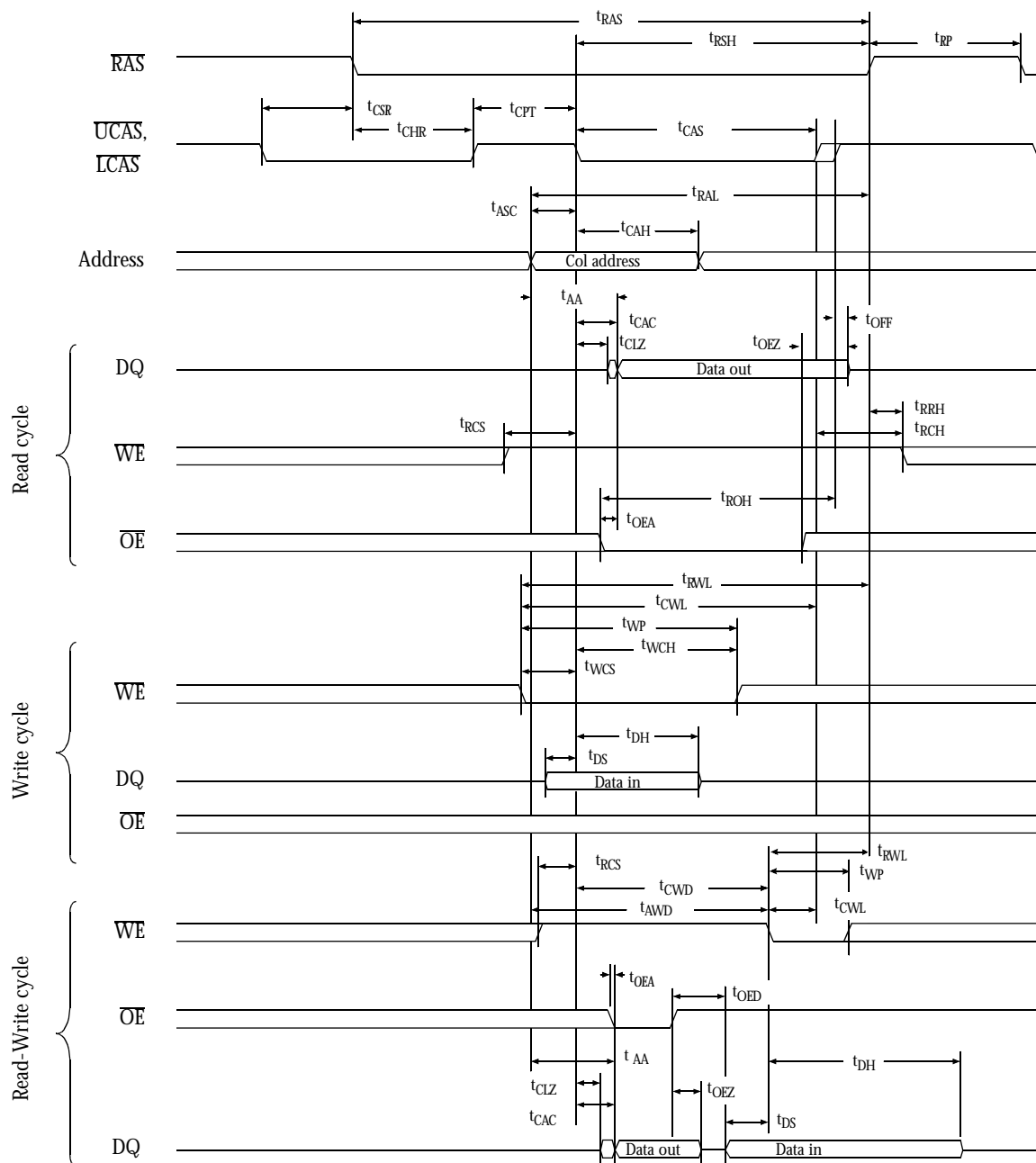


Hidden refresh waveform (write)



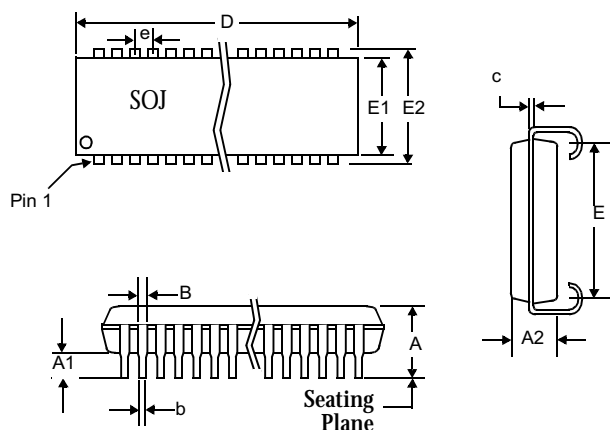


CAS before RAS refresh counter test waveform



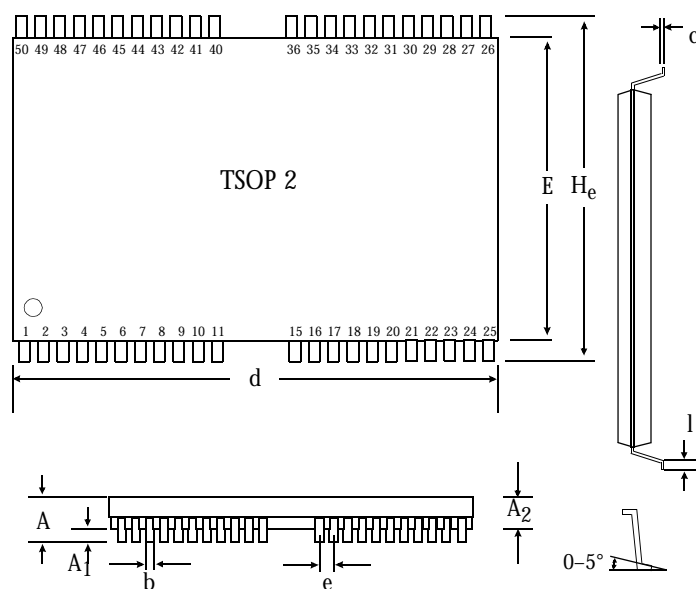


Package dimensions



42-pin SOJ

	Min	Max
A	0.128	0.148
A1	0.025	-
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.070	1.080
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	



50-pin TSOP 2

	Min (mm)	Max (mm)
A		1.2
A ₁	0.05	
A ₂	0.95	1.05
b	0.30	0.45
c	0.12	0.21
d	20.85	21.05
E	10.03	10.29
H _e	11.56	11.96
e	0.80 (typical)	
l	0.40	0.60

Capacitance¹⁵

$f = 1 \text{ MHz}$, $T_a = \text{Room temperature}$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN1}	A0 to A9	$V_{in} = 0V$	5	pF
	C_{IN2}	RAS, UCAS, LCAS, WE, OE	$V_{in} = 0V$	7	pF
DQ capacitance	C_{DQ}	DQ0 to DQ15	$V_{in} = V_{out} = 0V$	7	pF



AS4C1M16E5 ordering information

Package \ $\overline{\text{RAS}}$ access time	45 ns	50 ns	60 ns
Plastic SOJ, 400 mil, 42-pin	AS4C1M16E5-45JC	AS4C1M16E5-50JC AS4C1M16E5-50JI	AS4C1M16E5-60JC AS4C1M16E5-60JI
TSOP 2, 400 mil, 44/50-pin	AS4C1M16E5-45TC	AS4C1M16E5-50TC AS4C1M16E5-50TI	AS4C1M16E5-60TC AS4C1M16E5-60TI

AS4C1M16E5 part numbering system

AS4	C	1M16E5	-XX	X	X
DRAM prefix	C = 5V CMOS	Device number	$\overline{\text{RAS}}$ access time	Package: J = 42-pin SOJ 400 mil T = 44/50-pin TSOP 2 400 mil	Temperature range C=Commercial, 0°C to 70 °C I=Industrial, -40°C to 85°C