

R1 in Phase 1			
PHASE 1 ENABLED			
	<b>R1IN(fb)</b> R1OUT @t-1		<b>R1OUT(ff)</b> 1+IN(fb)
ITER			
	-1		0
	0	0	1
PHASE 1 DISABLED			
	<b>R1IN(fb)</b> R1OUT @t-1		<b>R1OUT(ff)</b> NO-OP (disabled)
ITER			
prev			1
	1	1	1
	2	1	1
PHASE 1 ENABLED AGAIN			
	<b>R1IN(fb)</b> R1OUT @t-1		<b>R1OUT(ff)</b> 1+IN(fb)
ITER			
prev			1
	3	1	2
	4	2	3