PROGRAM AT A GLANCE

		July 15th	Tuesday, July 16th			
		Auditoire **CO2**	**CO 123** *Floor 1*	**CO 015** *Floor 0*	**CO 124** *Floor 1*	**CO 016** *Floor 0*
07:30	08:00		**Registration opens**			
08:00	08:20					
08:20	08:40		**Opening Session** **Room: *Auditoire* CO2**			
08:40	09:00					
09:00	09:20		**Plenary Talk – *Prof. Andreas Burg*** **Room: *Auditoire* CO2**			
09:20	09:40					
09:40	10:00					
10:00	10:20		**Coffee Break, Company Fair and Posters**			
10:20	10:40		**Analog Circuits and Sub-systems I**	**Digital Circuits and Sub-sytems I**	*Special Session* **Do you still handcraft your analog and RF layouts?**	**Radio Frequency, Microwave & mm-wave**
10:40	11:00					
11:00	11:20					
11:20	11:40					
11:40	12:00					
12:00	12:20					
12:20	12:40		**Lunch**			
12:40	13:00					
13:00	13:20	**Registration Opens**				
13:20	13:40		**Power Circuits and Harvesting**	**Digital Circuits and Sub-sytems II**	*Special Session* **Cutting edge test solutions for analog, mixed-signal and RF ICs**	**Modeling the next generation of Electronics and Sensors**
13:40	14:00					
14:00	14:20	**Tutorial – *Dr. Andrei Müller***				
14:20	14:40					
14:40	15:00					
15:00	15:20					
15:20	15:40	**Coffee Break**	**Coffee Break, Company Fair and Posters**			
15:40	16:00	**Tutorial – *Prof. Danilo Demarchi***	**Radio Frequency Circuits and Systems I**	**Sensing and Biomedical Circuits I**	**“Powering the Smarts” Competition**	
16:00	16:20					
16:20	16:40					
16:40	17:00					
17:00	17:20	**Tutorial – *Dr. Jean-Michel Sallese***	**Industrial Sponsors Presentation** ***Room: Auditoire CO2***			
17:20	17:40					
17:40	18:00					
18:00	18:20		**Welcome Reception** ***Apéritif à l'École polytechnique fédérale de Lausanne***			
18:20	18:40					
18:40	19:00					

PRIME 2019 Technical Session

SMACD 2019 Technical Session

PROGRAM AT A GLANCE

		Wednesday, July 17th				
		Auditoire **CO2**	**CO 123** *Floor 1*	**CO 015** *Floor 0*	**CO 124** *Floor 1*	**CO 016** *Floor 0*
08:00	08:20	**Registration opens**				
08:20	08:40					
08:40	09:00					
09:00	09:20	**Plenary Talk – *Dr. Onur Kazanc* Room: *Auditoire* CO2**				
09:20	09:40					
09:40	10:00					
10:00	10:20	**Coffee Break, Company Fair and Posters**				
10:20	10:40		**Data Converters**	**Sensing and Optical Circuits**	**Design Techniques and Optimization Methods**	**Bioelectronics**
10:40	11:00					
11:00	11:20					
11:20	11:40					
11:40	12:00					
12:00	12:20	**Lunch**				
12:20	12:40					
12:40	13:00					
13:00	13:20					
13:20	13:40	**EDA Competition: Part I**	**Radio Frequency Circuits and Systems II**	**Circuits for Reliability and Resiliency**	**Powering Everyday Electronics**	
13:40	14:00					
14:00	14:20					
14:20	14:40					
14:40	15:00					
15:00	15:20	**Coffee Break, Company Fair and Posters**				
15:20	15:40	**EDA Competition: Part II**	**Analog Circuits and Sub-systems II**	**Digital Circuits and Emerging Technologies**	**Very Large Scale Reliability**	
15:40	16:00					
16:00	16:20					
16:20	16:40					
16:40	17:00					
17:00	17:20					
17:20	17:40					
17:40	18:00					
18:00	18:20	**Visit to the *Musée Olympique***				
18:20	18:40					
18:40	19:00					
19:00	19:20	***Apéritif* and Gala Dinner at the *Musée Olympique***				
19:20	19:40					
19:40	20:00					

PROGRAM AT A GLANCE

		Thursday, July 17th			
		CO 123 *Floor 1*	**CO 015** *Floor 0*	**CO 124** *Floor 1*	**CO 016** *Floor 0*
08:00	08:20	**Registration opens**			
08:20	08:40				
08:40	09:00				
09:00	09:20	**Plenary Talk – *Prof. David Atienza*** **Room: *Auditoire* CO2**			
09:20	09:40				
09:40	10:00				
10:00	10:20	**Coffee Break, Company Fair and Posters**			
10:20	10:40	**Image and Data Processing**	**Sensing and Biomedical Circuits II**	*Special Session* **MEMS & Heterogeneous Systems: Which design tools and methodologies are missing?**	**Variability and Aging**
10:40	11:00				
11:00	11:20				
11:20	11:40				
11:40	12:00				
12:00	12:20	**Lunch**			
12:20	12:40				
12:40	13:00				
13:00	13:20				
13:20	13:40	**Industrial Sponsors Presentation** **Room: *Auditoire* CO2**			
13:40	14:00				
14:00	14:20	**Modeling, Optimization and Characterization**	**MEMS and Piezoelectrical Sensors**	*Special Session* **Deep Learning for analog EDA: Are we there yet?**	**System-level Methodologies**
14:20	14:40				
14:40	15:00				
15:00	15:20				
15:20	15:40				
15:40	16:00	**Award Ceremony & Closing Session** **Room: *Auditoire* CO2**			
16:00	16:20				
16:20	16:40				
16:40	17:00				

PRIME 2019 Technical Session

SMACD 2019 Technical Session

TECHNICAL SESSIONS DETAILS

Tuesday Morning, July 16th

PRIME Technical Session
"Analog Circuits and Sub-systems I" **Tuesday 10:20 - 12:00** *Room CO 123*
Chair: Alberto Gola, *ams AG*

10:20 Implementation of a Fully-Differential Operational Amplifier with Wide-Input Range, High-Impedance Common-Mode Feedback

Yannick Wenger and Bernd Meinerzhagen
TU Braunschweig, Germany

Stabilizing the common-mode in fully-differential amplifiers is a well-known challenge. Conventional approaches usually are not able to deal with output nodes that have both: a high impedance and a high voltage swing. In this work, we implement a common-mode feedback architecture that was previously proposed in [2] but not yet realized. A two-stage fullydifferential operational amplifier in a 0.25µm CMOS technology is used to demonstrate the feasibility of the new architecture. Measurements of the overall amplifier verify that the studied common-mode feedback is indeed a good candidate for opamps with high ouput impedance and rail-to-rail swing.

10:40 A 150MHz TIA with un-conventional feed-forward opamp stabilization technique

Mohammadmehdi Deilam Salehi, Danilo Manstretta and Rinaldo Castello
University of Pavia, Italy

To satisfy the requirements of the 5G standards the base-band of the wireless transceiver includes circuits able to process signals with hundreds of MHz of bandwidth e.g. an active-RC filter with 150 MHz cut-off frequency. An operational transconductance amplifier with a loop gain of 36 dB at 100 MHz and 2 GHz unity gain bandwidth was designed using an unconventional feedforward topology. the feedforward (FF) path is returned to the input node as opposed to the output as it is classically done. This allows to use heavy current reuse (stacking) in the FF path without large distortion and signal losses at the output node. The circuit is operated from a 1.8 V supply and consume 4 mW of power. Post layout simulations based on a 28 nm CMOS process shows an input referred noise integrated up to 120 MHz of 80 nV and an outstanding IIP3 of more than 52 dBm across the all band. The resulting in band FoM of 188 [dBJ-1] greatly exceeds the state of the art.

11:00 A Sub-1V CMOS Switched Capacitor Voltage Reference with high output current capability

Andrea Ria, Alessandro Catania, Mattia Cicalini, Lorenzo Benvenuti, Massimo Piotto and Paolo Bruschi
University of Pisa, Italy

This paper presents an original low-voltage CMOS, bipolar transistor free, sub-threshold voltage reference capable of operating with sub-1V supply voltages. Novel aspects of the proposed solution are (i) use of a bandgap core with a single MOSFET to avoid threshold voltage error terms and (ii) adoption of an high-gain, low offset inverter-like amplifier in the bandgap feedback loop. Relativiely high output current sourcing capabilities are obtained by means of an output source follwer stage based on native MOSFETs. The circuit potentiality is demonstrated by means of electrical simulations performed on a prototype designed with a standard 0.18um CMOS process. A reference voltage is 0.483 V with a maximum variation of 4mV in a temperature range of -20/80°C, has been obtained with a supply voltage of 0.7 V. The maximum output current is 200µA with a quescient current consumpion of only 9.8µA.

11:20 Modified Current-reuse OTA to Achieve High CMRR by utilizing Cross-coupled Load

Erwin Habibzadeh Tonekabony Shad, Marta Molinas and Trond Ytterdal
Norwegian University of Science and Technology, Norway

Since biomedical signals have very low amplitude and high common-mode like environmental noise, the amplifiers used with these signals should have high CMRR. The cross-coupled amplifier attenuates common-mode signal strongly because of its load behavior for differential and common-mode signal which leads to high CMRR. Since cross-coupled amplifier differential gain is low, its load is combined with current-reuse operational amplifier. The final CMRR of a fully differential current-reuse OTA with conventional common-mode feedback and modified load is simulated and compared in a 0.18 m CMOS technology. Their CMRR is simulated for mismatch and process variation. According to the simulation, for the same power consumption, W and L, the modified current-reuse with cross-coupled load has the best performance. Its CMRR in the worst case was about 90 dB while the total power consumption was 18 uW at 1.8 V supply voltage. The Bandwidth is 4.8 kHz and the total input referred noise in this bandwidth is 1:04

uVrms and 0:43 uVrms from 0.5 to 100 Hz which is acceptable noise and bandwidth for the EEG application considered in this study.

11:40 A Generic Procedural Generator for Sizing of Analog Integrated Circuits

Matthias Schweikardt[1], Yannick Uhlmann[1], Florian Leber[1], Husni Habal[2] and Jürgen Scheible[1]
[1]Reutlingen University, Germany [2]Infineon, Germany

In this paper, we address the novel EDP (Expert Design Plan) principle for procedural design automation of analog integrated circuits, which captures the knowledge-based design strategy of human circuit designers in an executable script, making it reusable. We present the EDP Player, which enables the creation and execution of EDPs for arbitary circuits in the Cadence® Virtuoso® Design Environment. The tool provides a generic version of an instruction set, called EDPL (EDP-Language), enabling emulation of a typical manual analog sizing flow. To automate the design of a Miller Operational Amplifier and to create variants of a Smart Power IC, several EDPs were implemented using this tool. Employing these EDPs leads to a strong reduction of design time without compromising design quality or reliability.

PRIME Technical Session
"Digital Circuits and Sub-sytems I" Tuesday 10:20 - 12:00 *Room CO 015*
Chair: Bernd Deutschmann, *Technische Universität Graz, Austria*

10:20 A 5 ps resolution, 8.6 ns delay range digital delay line using combinatorial redundancy

Thomas Van den Dries, Hans Ingelberts, Sven Boulanger and Maarten Kuijk
Vrije Universiteit Brussel, Belgium

A novel digital delay line architecture is presented, which is able to achieve a high resolution of 5 ps and a wide delay range of 8.6 ns simultaneously. It does so by combining elements of digital and analog delay locked loops and uses a replica circuit to compensate for temperature variations. Furthermore, accurate and precise delay steps with 3.8 ps RMS jitter are obtained by using combinatorial redundancy. Its overall performance is superior to state-of-the-art approaches, which make a trade-off for at least one of the performance metrics.

10:40 Impact of Adiabatic Logic Families on the Power-Clock Generator Energy Efficiency

Sachin Maheshwari and Izzet Kale
University of Westminster, United Kingdom

Due to the low-power requirement by devices deployed in NFC application operating at low frequencies, adiabatic logic is a good candidate for their implementation and can be used to reduce energy consumption. Adiabatic logic works using an AC power-clock supply. However, generating the AC power-clock increases the energy consumption of the complete adiabatic system. A lot of work has been done on generating the AC power-clocks using resonant circuits and a handful by using stepwise capacitor based circuit. But the literature lacks the study of the impact of adiabatic logic families' on the power-clock generator energy dissipation and efficiency. In this paper, we investigate the effect of adiabatic logic families working with 4-phase power-clock generators designed using a dual-StepWise (only 2-steps) Charging (SWC) circuit. The analysis of the energy dissipation for single power-clock is done taking into account the parasitic resistance and capacitance of the adiabatic logic and power-clock network. Experiments based on simulation results show that the adiabatic logic families' impacts both the energy consumption and efficiency of the complete adiabatic system.

11:00 Selector-Memory Device Voltage Compatibility Considerations in 1S1R Crosspoint Arrays

Yilkal A. Belay, Alessandro Cabrini and Guido Torelli
University of Pavia, Italy

In 1S1R (one-selector one-resistor) memory arrays, the nonlinear selector device is serially connected to each memory element to address the inherent sneak (or leakage) current paths problem. It is crucial that this selector device achieves voltage compatibility with the memory element for acceptable write and read performance of the array. We present a study on the relationship between the switching voltage of the memory element, Vsw (with variation denoted as αVsw) and the threshold voltage of the selector device, Vth (with variation denoted as αVth), that is required for voltage compatibility. Using analytical models and circuit simulations, we demonstrate that the write and read requirements, respectively, set the maximum and the minimum allowed values of Vsw/Vth(i.e., the ratio of Vsw to Vth), which determines the design space for 1S1R crosspoint memory array implementation.

11:20 A Novel Delay Generator for the Triggering of Particle Detectors at the CERN LHC

Jordan Lee Gauci[1], Edward Gatt[1], Owen Casha[1], Giacinto De Cataldo[2], Ivan Grech[1] and Joseph Micallef[1]
[1]University of Malta, Malta [2]INFN Bari, Italy

This paper presents the design and implementation of a novel remotely programmable delay generator that will be used in the triggering of the High Momentum Particle Detector at the CERN LHC. The architecture is based on a delay locked loop, that is used to generate a look up table delay transfer characteristic for digitally controlling a delay

line and to provide the required delay. The delay generator was implemented using the X-FAB 0.18 um technology and occupies a total area of 2.434x2.434mm2. It consumes a total power consumption of around 6 mW from a 1.8 V supply.

11:40 New ASICs for the Very Front-End Card Upgrade of the CMS ECAL Barrel at the HL-LHC

Simona Cometti[1,2] and Giovanni Mazza[2]
[1]Politecnico di Torino, Italy [2]INFN Torino (IT), Italy

The Compact Muon Solenoid detector (CMS) is operating at the Large Hadron Collider (LHC) with proton-proton collisions at 13 TeV center-of-mass energy. CMS was originally designed to operate for about ten years, for LHC instantaneous luminosity up to 1·10^34 cm^(−2) s^(−1) and integrated luminosity of 500 fb^(-1). The High Luminosity LHC (HL-LHC) will increase instantaneous luminosity by about a factor of 5 from current levels and CMS will accumulate an integrated luminosity of 3000 fb^(−1) by about 2035. The CMS electromagnetic calorimeter (ECAL) will face a challenging environment at the HL-LHC: higher event pileup, increasing data rates and harsher radiation environment. The ECAL Very Front-End (VFE) readout electronics have been completely redesigned, with goals of providing precision timing, low noise and increased sampling rate from 40 MS/s to 160MS/s with 12-bits resolution. Therefore, a high-speed, high-resolution ADC has been designed to be placed after the Trans-Impedance Amplifier (TIA) stage. Each readout channel will produce an amount of data which will require fast data transmission circuitry and high speed serial links. A new digital architecture has been developed in order to decrease the data bandwidth by means of lossless data compression. These functions has been integrated in two ASICs: CATIA and LiTE-DTU, designed in commercial CMOS 130 nm and 65 nm technology, respectively.

SMACD Special Session

"Do you still handcraft your analog and RF layouts?" **Tuesday 10:20-12:00** *Room CO 124*

Organizers/Chairs: Prof. Hung-Ming Chen and Prof. Chien-Nan Liu, *National Chiao Tung University, Taiwan*

10:20 Comparison of ELTs with different shapes and a regular layout transistor in 180 nm CMOS process

Sadik Ilik, Nergiz Sahin-Solmaz, Aykut Kabaoglu and Mustafa Berke Yelten
Istanbul Technical University Electronics and Communications Engineering, Turkey

Radiation tolerance of electronic devices and systems is mandatory for defence and space applications. In order to increase this tolerance for CMOS FETs, different layout techniques such as enclosed layout transistors (ELTs) can be employed. In this paper, a regular layout transistor is compared with two ELTs, which have square and octagonal shaped gates. For this purpose, a test circuit in 180 nm device technology has been designed and fabricated. Experimental comparison of the same size transistors with different layouts is performed in terms of the impact of process variations, and radiation tolerance. It is concluded that ELTs with different shapes behave similarly under radiation at least upto a dose of 1 Mrad. Furthermore, octagonal shaped ELTs are slightly less impacted from process variations in regard to square ELTs.

10:40 On the Exploration of Design Tradeoffs in Analog IC Placement with Layout-dependent Effects

Ricardo Martins, Nuno Lourenço, Ricardo Póvoa and Nuno Horta
Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon, Portugal

At advanced integration nodes, the impact of layout-dependent effects (LDEs) turn the performance of MOSFET devices strongly dependent on the layout implementation details, but also, of its surrounding neighborhood. However, in the traditional design flow, the real LDEs-impact is only known after complete extraction and post-layout simulation, causing re-design iterations with no valuable feedback information to fix the problem. This paper proposes an automatic placement methodology for analog integrated circuit (IC) layout design, that minimizes the mobility and threshold-voltage-related variations caused by the two major sources of LDEs above the 40 nm technology nodes, i.e., well-proximity effect and length of oxide diffusion. An absolute representation of the floorplan is adopted, and, a multi-objective optimization (MOO) algorithm with LDE-impact mitigation operators, is applied. Established LDE formulations used in BSIM models are used to guide placement optimization, shorting the gap between pre and post-layout performance.

11:00 Analog Layout Placement Based on Unit Elements and Routing Channel Estimation

Sherif Ahmed[1], Mohamed Dessouky[2], Fady Atef[2] and Soha Hamed[2]
[1]mixel, Egypt [2]Ain Shams University, Egypt

This paper presents an analog layout placement and routing flow based on device unit elements. Device placement is based on Satisfiability Modulo Theories techniques, while device routing uses a predefined procedural router. The placer tool implicitly generates multiple layouts that fulfill the given constraints and hence constructs the layout shape function. A routing channel estimator then calculates the area required by device routing for each placement solution

without any layout generation. It takes into account the type of matched groups as well as net currents. This allows a more realistic choice of the optimum layout based on the overall system aspect ratio and area constraints. The flow is demonstrated using a Folded-Cascode OTA layout generation.

11:20 A Structure-Based Methodology for Analog Layout Generation

Yu-Hsien Chen[1], Hao-Yu Chi[2], Ling-Yen Song[2], Chien-Nan Liu[2] and Hung-Ming Chen[2]
[1]Department of Electrical Engineering, National Central University, Taiwan [2]National Chiao Tung University, Taiwan

In order to speed up analog design cycles, analog layout automation is a popular research in recent years. However, most previous works assume the required design constraints are given by users manually. Designers still take a lot of time to fill-in the required design information. Template-based layout generation is another approach to consider the design constraints, but considerable development efforts are required for each new design and each new technology. In this paper, we propose a structure-based methodology for analog layout generation. This methodology starts from a structure analysis that divides the circuit netlist into several building blocks automatically. It can help to reduce the dependence on users' input and generate corresponding design constraints for the succeeding layout steps. With the help from structure analysis, the layouts of those analog structures are generated, placed, and routed automatically with proper constraints. As shown in the demo cases, the required layout can be generated accurately without users' intervention and still keep the post-layout performance without too much loss.

11:40 Using EDA Tools to Push the Performance Boundaries of an Ultralow-Power IoT-VCO at 65nm

Ricardo Martins[1], Nuno Lourenço[1], Nuno Horta[1], Jun Yin[2], Pui-In Mak[2] and Rui P. Martins[2]
[1]Instituto de Telecomunicações, IST–UL, Portugal [2]State-Key Lab. of Analog and Mixed-Signal VLSI and FST-ECE, China

Voltage-controlled oscillators (VCOs) embedded in state-of-the-art radio-frequency (RF) integrated circuit (IC) multi-standard transceivers must comply with extreme ultralow power requirements for modern IoT applications. However, due to the countless tradeoffs that must be considered, their manual design hardly approaches the full potential that a certain topology can achieve at advanced integration nodes. In this paper, the design and optimization of a complex IoT-VCO for a 65 nm process design kit (PDK) is fully supported by electronic design automation (EDA) tools. Firstly, a 108-dimensional performance space is optimized, providing 48 sizing solutions where the power consumption varies from 0.145 mW to 0.329 mW on the worst-case corner performance of the worst-case tuning range. Afterwards, the layout-versus-schematic (LVS) correct layout of each solution is automatically generated using a hierarchical Placer and group-based Router. Post-layout validation is carried in all solutions, and, a promising solution with 0.348 mW of worst-case post-layout power consumption is proposed for fabrication.

SMACD Technical Session
"Radio Frequency, Microwave & mm-wave" **Tuesday 10:20-12:00** *Room CO 016*
Chair: Elisenda Roca, *IMSE, CNM, CSIC and Universidad de Sevilla, Spain*

10:20 Design, Simulation and Implementation of Very Compact Dual-band Microstrip Bandpass Filter for 4G and 5G Applications

Yasir Al-Yasir, Naser Ojaroudiparchin, Ali Alabdullah, Widad Mshwat, Ahmed Abdulkhaleq, Khalid Hameed, Mohammed Al-Sadoon and Raed Abd-Alhameed
University of Bradford, United Kingdom

This article proposes a very compact planer open-loop bandpass filter (BPF) with asymmetric frequency response and covering the 2.5 to 2.6 GHz and 3.6 to 3.7 GHz spectrum for 4G and 5G applications, respectively. The microstrip BPF employs four open-loop ring resonators with 50 Ω tapped lines for input and output ports. To achieve sharper cut-off frequencies, one infinite and three finite transmission zeros are successfully generated on the upper and lower edges of the 4G and 5G passbands. The utilization of the planer four-section resonators not only reduces the size of the structure, but also provides either positive or negative cross-coupling. The cross-coupling coefficients between the resonators are optimized to resonate at the required frequency with proper bandwidth. The reported BPF is designed and optimized using CST software, and is implemented on a Rogers RO3010 substrate with a relative dielectric constant of 10.2 and a very compact size of 11×9×1.27 mm3. Good agreement is achieved between the simulated and measured results.

10:40 Methodology for Performance Optimization in Noise- and Distortion-Canceling LNA

Antonio Dionisio Martínez-Pérez[1], Cecilia Gimeno[2], Denis Flandre[2], Francisco Aznar[1], Guillermo Royo[1] and Carlos Sánchez-Azqueta[1]
[1]Universidad de Zaragoza, Spain [2]Université Catholique de Louvain, Belgium

This paper proposes a general methodology for designing noise-canceling low noise amplifiers (LNA). The procedure provides designers better information of the topology trade-offs and which restrictions must be imposed to design variables to attain target specifications. Thus, it is especially desirable when opposite specification, such as cut-off frequency, linearity, noise figure or power consumption are required. A CG-CS LNA in a 45 nm SOI CMOS technology is presented, although authors give guidelines to extrapolate the method to other topologies and technologies.

11:00 Verilog-A based Behavioral Modeling of an FBMC Transmitter

Patrick Döll, Oner Hanay, Erkan Bayram and Renato Negra
RWTH Aachen University, Germany

In this paper a Verilog-A based behavioral modeling of a filter-bank multicarrier (FBMC) transmitter with main focus on the RF-DAC cores is presented. Multiple switching signals within the transmitter yield to a tremendous degradation in simulation performance. Because of that, the simulation of the entire system at transistor level is time-consuming. The abstracted model leads to a reduction in simulation time of up to 70% with only half memory usage compared to theoriginal model by still getting sufficient results. Furthermore, a performance friendly and simple technique is presented to generate signals with equidistantly spaced frequencies with additional abstraction level to generate jitter and deterministic phase noise. Verilog-A has been used to design the models in combination with Spectre simulator to verify the results.

11:20 New Pattern Reconfigurable Circular Disk Antenna Using Two PIN Diodes for WiMax/WiFi (IEEE 802.11a) Applications

Yasir Al-Yasir, Naser Ojaroudiparchin, Ali Alabdullah, Widad Mshwat, Atta Ullah and Raed Abd-Alhameed
University of Bradford, United Kingdom

Reconfigurable beam shaping using circular disc microstrip patch antenna with a slot ring is proposed. The proposed antenna has an overall dimension of 70×70mm2 printed on a substrate of a dielectric constant 4.3. The designed antenna operates at 5.35 GHz with a central coaxial probe feed. By changing the configuration of two PIN-diodes switches, the designed antenna has three different beam patterns in the yz plane. Activating each diode individually result in a near 60o shift in the main beam direction, whereas the frequency characteristics are largely unchanged. At resonance, the peak gains are approximately 3 dB, 4 dB and 4.3 dB, in the three states of diodes configurations. Return loss, peak gains and radiation pattern are presented, which are in very good agreement for WiMax/WiFi (IEEE 802.11a) applications.

11:40 Synthesis of mm-Wave circuits using EM simulated passive structure libraries

F. Passos[1,2], Elisenda Roca[1], Rafael Castro Lopez[1], Nuno Horta[2] and Francisco Fernandez[1]
[1]IMSE-CNM, CSIC and Universidad de Sevilla, Spain [2]Instituto de Telecomunicações, IST-ULisbon, Portugal

Millimeter-wave circuit design is extremely complex and time-consuming. One of the reasons is the dependence on electromagnetic simulators used to accurately predict the performance of the high amount of passive structures that compose such circuits. Also, achieving optimal performances is not trivial in the millimeter-wave regime. Although synthesis methodologies can aid the designer to achieve optimal circuit performances, the usage of electromagnetic simulators is prohibitive in such methodologies due to efficiency issues. In this work, a new synthesis methodology is presented where the accuracy of electromagnetic simulations can be included without losing efficiency.

Tuesday Afternoon, July 16th

PRIME Technical Session
"Power Circuits and Harvesting" **Tuesday, 13:20-15:20** *Room CO 123*
Chair: Prof. Günhan Dündar, *Boğaziçi University, Turkey*

13:20 AC/DC Buck Boost Converter for Wind-Powered Wireless Sensors

Mohammad Haidar[1], Hussein Chible[2], Remy Morasso[1] and Daniele D. Caviglia[1]
[1]University of Genova, Italy [2]Lebanese University, Beirut, Lebanon

As the Wireless Sensor Networks (WSN) and Internet of Things (IoT) are increasingly getting popular, an important issue that lies in the power supply was always present. Moreover, creating new solutions for power consumption and finding alternative power sources was always under the scope of modern researches. Many of those researches nowadays are tackling the idea of energy harvesting, due to its unlimited availability. Even though, the task is challenging given the unpredictable behavior of the environment, and the constraints on the physical setup. The harvesters usually capture available energy from the environment, and transform it to a useful DC electrical signal using specialized circuits. In this work, a power management system for the fluttering wind energy harvester is presented and tested. The proposed system uses a low power microcontroller running a simple power management algorithm, and an optimised self-powered circuit, providing high power efficiency on the output. This approach gives an advantage over the commercial converters tested on the same harvester in terms of efficiency, as well as a possible flexibility in the power monitoring and management.

13:40 Hysteretic Buck-Boost Converter for Wearable Applications

Kemal Ozanoglu[1], Pier Cavallini[2], M. Berke Yelten[3] and Gunhan Dundar[1]

[1]Bogazici University, Turkey [2]Dialog Semiconductor, United Kingdom [3]Istanbul Technical University, Turkey

This paper presents a novel Buck-Boost converter architecture targeting wearable applications, utilizing hysteretic control. The topology consists of three comparators, a derivative circuit, logic, timers and power switches. Macromodel level simulation results show < 5mV line and load regulation results, demonstrating that this topology promises to be a convenient solution for wearable platforms and other applications where good line regulation and low quiescent current are essential.

14:00 A Fully-Integrated 6:1 Cascaded Switched-Capacitor DC-DC Converter Achieving 74% Efficiency at 0.1 W/mm²

Tuur Van Daele, Elly De Pelecijn, Tim Thielemans, Michiel Steyaert and Filip Tavernier
Katholieke Universiteit Leuven , Belgium

This paper introduces a cascading technique for monolithic switched-capacitor DC-DC converters with a high voltage conversion step. With this technique, the converter is divided into subconverters, each with a low voltage rating. This enables the use of MOS instead of MIM/MOM capacitors, leading to high efficiencies and power densities thanks to the superior MOS capacitance density. A 6:1 cascade topology that converts an input voltage of 7.25V into an output voltage of 1V, is implemented in a standard 90nm CMOS technology. The simulated converter achieves an efficiency of 74:2% at a power density of 0.1 W/mm2. As a result, the proposed design achieves the best high-density figure of merit compared to the state-of-the-art.

14:20 Startup Behaviour of Power Managment Unit for an Integrated Gate Driver

Leo Rolff, Eva Schulte Bocholt, Ralf Wunderlich and Stefan Heinen
RWTH Aachen University, Germany

The start-up is a critical part for supply voltage generation of integrated circuits. Especially ICs utilizing multiple voltage rails demand a careful consideration of the start-up. This task is generally fulfilled by a power management unit (PMU) which, despite the increasing integration level, still is mostly implemented discretely. This paper proposes an integrated PMU generating three different supply voltages, featuring one buck converter to efficiently generate the most energy consuming supply. The start-up of the PMU is considered and the functioning is verified by measurement results.

14:40 A novel method for dynamic battery model identification based on CFSO

Gabriele Maria Lozito, Valentina Lucaferri, Francesco Riganti Fulginei and Alessandro Salvini
Roma Tre University, Italy

Maximum battery runtime and low power dissipation are the key points for energy harvesting devices development. Therefore, an accurate battery model, describing the static and dynamic battery behaviour, plays an important role in estimating battery state over time and in a wide range of operating conditions. This paper proposes a dynamic hybrid model to approximate both the battery State of Charge (SOC) and the discharge characteristic, using a swarm-intelligence optimization algorithm, the Continuous Flock of Starling Optimization (CFSO). Simulation and results are discussed, demonstrating the efficiency of the proposed identification method.

15:00 Fast transient thermomechanical stress to set a pressure-assisted sintering process

Marco Santopá[1], Sebastiano Russo[1], Marco Torrisi[1], Marco Renna[1], Alessandro Sitta[2] and Michele Calabretta[1]
[1]STMicroelectronics, Italy [2]Universita' degli Studi di Catania, Italy

High temperature application and long term reliability are the future trends for power electronics. A key factor to enable future applications is the interconnection durability improvement under high temperature and thermo-mechanical cycling loads. Nowadays, the standard solders cannot fulfill the reliability requirements of future power electronic devices, therefore interconnection technologies have to be developed. One of the most promising joining technique is Ag sintering. Combining properly temperature, time and pressure, a strong, highly electrically and thermally conductive bond is formed. The aim of this work is to develop a methodology to assess the Ag sintering die attach process for a SiC power MOSFET. Different process parameters have been benchmarked by means of physical analyses, performed not only on just assembled devices but also considering the aging effect induced by a liquid-to-liquid thermal shock test.

PRIME Technical Session
"Digital Circuits and Sub-sytems II" Tuesday, 13:20-15:20 *Room CO 015*
Chair: Elena Blokhina, *University College Dublin, Ireland*

13:20 Efficient FPGA Implementation of PCA Algorithm for Large Data using High Level Synthesis

Mohammad Amir Mansoori and Mario Casu
Politecnico di Torino, Italy

Principal Component Analysis (PCA) is a widely used method for dimensionality reduction in different application areas, including microwave imaging where the size of input data is large. Despite its popularity, one of the difficulties in using PCA is its high computational complexity, especially for large dimensional data. In recent years several FPGA implementations have been proposed to accelerate PCA computation. However, most of them use manual RTL design, which requires more time for design and development. In this paper, we propose an FPGA implementation of PCA using High Level Synthesis (HLS), which allows us to explore the design space more efficiently than with hand-coded RTL design. Starting from a PCA algorithm written in C++, we apply various hardware optimization techniques to the same code using Vivado HLS in order to quickly explore the design space. Our experiments show that the performance of the design obtained with the proposed method is superior to the state-of-the-art RTL design in terms of resource utilization, latency and frequency.

13:40 FPGA Implementation of Novel Routing Algorithm for Butterfly-Fat-Tree Topology based NoC Design

Veda Bhanu P, Samala Jagadheesh, Vasanth Bhat, Garima Agarwal and Soumya J
BITS-Pilani, Hyderabad campus, India

This paper presents a novel routing algorithm for Butterfly-Fat-Tree (BFT) topology based Network-on-Chip (NoC) design. It proposes a routing algorithm along with router addressing scheme for BFT topology which can be used in any generic NoC router architecture. The proposed algorithm has been implemented in software using C, followed by hardware implementation using Verilog. It has been validated using FPGA based hardware and the results show that proposed routing algorithm routes the data from source to destination seamlessly. This can be incorporated with NoC router architecture to verify several functionalities on a hardware based prototype

14:00 A High Performance Full-Word Barrett Multiplier Designed for FPGAs with DSP Resources

Erdem Ozcan and Serdar S. Erdem
Gebze Technical University, Turkey

Modular multiplication with large integers is the fundamental operation in public-key cryptosystems. In this paper, a high performance, full-word Barrett modular multiplier design utilizing the DSP resources in modern FPGAs is presented. The operand size of the multiplier is multiples of 528 bits. Proposed design consists of 48x48 bit multiplier blocks built from the DSP slices which perform 24x16 bit multiplications and a carry select accumulator built from the DSP slices which perform 48 bit additions. The proposed design first multiplies operands and accumulate the result and then, reduces the accumulated result using Barrett's method. A Xilinx Virtex-7 implementation of the proposed hardware takes 0.49 us and 1.88 us for 528 bit and 1056 bit modular multiplications for any modulus respectively. To the best of authors' knowledge, this is the first work which gives the detailed implementation results for full-word Barrett modular multiplier targeting FPGAs with DSP resources.

14:20 An High-level Implementation Framework for Non-Recurrent Artificial Neural Networks on FPGA

Luciano Prono[1], Alex Marchioni[2], Mauro Mangia[2], Fabio Pareschi[1], Riccardo Rovatti[2] and Gianluca Setti[1]
[1]Politecnico di Torino, Italy [2]University of Bologna, Italy

This paper presents a fully parametrized framework, entirely described in VHDL, to simplify the FPGA implementation of non-recurrent Artificial Neural Networks (ANNs), which works independently of the complexity of the networks in terms of number of neurons, layers and, to some extent, overall topology. More specifically, the network may consist of fully-connected, max-pooling or convolutional layers which can be arbitrarily combined. The ANN is used only for inference, while back-propagation is performed off-line during the ANN learning phase. Target of this work is to achieve fast-prototyping, small, low-power and cost-effective implementation of ANNs to be employed directly on the sensing nodes of IOT (i.e. Edge Computing). The performance of so-implemented ANNs is assessed for two real applications, namely hand movement recognition based on electromyographic signals and handwritten character recognition. Energy per operation is measured in the FPGA realization and compared with the corresponding ANN implemented on a microcontroller (μC) to demonstrate the advantage of the FPGA based solution.

14:40 Self-Synchronized Encryption Using an FPE Block Cipher for Gigabit Ethernet

Adrián Perez-Resa, Miguel Garcia-Bosque, Carlos Sánchez-Azqueta and Santiago Celma
Zaragoza University, Spain

In this work, a new solution for self-synchronized encryption in physical layer at Gigabit Ethernet optical links is proposed. The solution is based in the block cipher operating mode called PSCFB (Pipelined Statistical Cipher Feedback) using as underlying PRF (Pseudo Random Function) an FPE (Format Preserving Encryption) block cipher. Thanks to this structure is possible to encrypt 8b10b Ethernet symbols preserving its coding properties at Physical layer in an optical Gigabit Ethernet interface. The IND-CPA (Indistinguishability under Chosen-Plaintext Attack) advantage is analysed for the first time concluding that this mode can be considered secure in the same way as traditional encryption modes are. In addition it provides self-synchronization while keeping an encryption throughput near 100%. Finally, the proposed mechanism has been simulated and synthetized in an FPGA (Field Programmable Gate Array) electronic device.

15:00 The Navigation of Robotic Fiber Positioners in SDSS-V Project: Design and Implementation

Matin Macktoobian, Denis Gillet and Jean-Paul Kneib
Ecole Polytechnique Fédérale de Lausanne, Switzerland

SDSS-V project is one of the major observational cosmological projects which aims to generate the map of the observable universe by collecting spectroscopic data from the sky using optical fibers. Each optical fiber is attached to a robotic positioner to be automatically coordinated. This paper illustrates the solution to the navigation problem of robotic fiber positioners corresponding to the SDSS-V project. We note the principal challenging requirements to navigate the robotic fiber positioners. These requirements are those which differentiate the navigation problem of the SDSS-V project from that of the other projects. Then, we discuss the solution in view of both design and implementation. In particular, we specify the hardware and the software components of the solution in a systematic perspective. We illustrate the effectiveness of our solution based on practical results.

SMACD Special Session — *Room CO 124*
"Cutting edge test solutions for analog, mixed-signal and RF ICs" — Tuesday, 13:20-15:20
Organizer/Chair: Haralampos Stratigopoulos, *Sorbonne Université, CNRS, LIP6, Paris, France*

13:20 Requirements for Industrial Analog Fault Simulator

Vladimir Zivkovic
Cadence Design Systems, United Kingdom

This article will discuss prerequisites that enable practical EDA solution for analog fault simulation. It will be shown that a strict and realistic definition set of targets, compliant with emerging IEEE standards for analog test is crucial for the success of such a product. Cadence product for analog fault simulation will be presented and options to mitigate the ever-green problem of analog fault simulation adoption in industrial applications will also be listed.

13:40 Adaptive defect simulation flow for Defect-oriented Test evaluation

Valentin Gutierrez and Gildas Leger
Instituto de Microelectronica de Sevilla (IMSE-CNM-CSIC), Spain

For AMS-RF circuits, functional test is usually considered the best way to test a circuit. By construction, it should detect any fault (i.e. performance loss) and consequently it does not require a-priori validation. However, defect-oriented strategies require an evaluation of the test quality prior to their implementation. This implies resorting to computationally intensive defect simulation campaigns. In this work, we propose an adaptive defect simulation loop that evaluates at each step the defect coverage and the fault escape rate of the test under validation and determines the best way to employ the computational power as a function of the test target metrics. That is to say, if it is better to simulate the performance setup to update the fault escape metric or, conversely, to simulate the proposed test setup to update the defect coverage metric.

14:00 Feature selection and feature design for machine learning indirect test: a tutorial review

Manuel Barragan[1] and Gildas Leger[2]
[1]TIMA Laboratory, France [2]Instituto de Microelectronica de Sevilla (IMSE-CNM-CSIC), Spain

Machine learning indirect test replaces costly specification measurements by simpler signatures and use modern learning algorithms to map these signatures to specifications. Defining a set of relevant signatures that appropriately captures the circuit performance degradation mechanisms is then a key point for enabling machine learning indirect test. In this tutorial we review some methodologies for selecting and designing such a set of information rich signatures.

14:20 Which metrics to use for RF indirect test strategy?

Hassan El Badawi[1], Florence Azais[1], Serge Bernard[1], Mariane Comte[1], Vincent Kerzérho[1] and François Lefevre[2]
[1]LIRMM, France [2]NXP Semiconductors France

This paper aims at opening a discussion on the quality assessment of indirect test strategies in the context of analog and RF integrated circuit testing. Many parameters may influence the prediction efficiency of the indirect test model (choice and number of indirect parameters taken into account, learning algorithm used to build the model…). In order to evaluate the quality of a given model, several metrics can be evaluated, that reflect either the average prediction error, a global reliability or a misclassification rate. But what are the most pertinent metrics to reflect the level of confidence that can be expected from the indirect test to efficiently replace a traditional test based on RF measurements? Which metrics can lead to an informed choice of an indirect test strategy for its stability and predictive power? These considerations are investigated in this paper and illustrated in a practical case study.

14:40 Post-Production Calibration of Analog/RF ICs: Recent Developments and A Fully Integrated Solution

Angelos Antonopoulos, Georgios Volanis, Yichuan Lu and Yiorgos Makris

The University of Texas at Dallas, United States

We present recent developments on post-production calibration of analog and radio frequency (RF) integrated circuits (ICs) mainly focusing on on-chip solutions. Specifically, we summarize the state-of-the-art on both direct as well as statistical-based calibration techniques. The latter typically employ on-die sensors which estimate the circuit under test (CUT) performances as well as tuning knobs, which along with machine learning-based methods are capable of calibrating the CUT. Existing sensors, tuning knobs as well as machine learning-based implementations are discussed and their limitations are outlined. Finally, a fully integrated new architecture for on-chip calibration of a low-noise amplifier (LNA) through the use of an analog neural network is introduced.

15:00 Self-Testing Analog Spiking Neuron Circuit

Sarah A. El-Sayed[1], Luis A. Camuñas-Mesa[2], Bernabé Linares-Barranco[2] and Haralampos-G. Stratigopoulos[1]
[1]Sorbonne Université, CNRS, LIP6, France [2]IMSE-CNM, CSIC y Universidad de Sevilla, Spain

Hardware-implemented neural networks are foreseen to play an increasing role in numerous applications. In this paper, we address the problem of post-manufacturing test and self-test of hardware-implemented neural networks. In particular, we propose a self-testable version of a spiking neuron circuit. The self-test wrapper is a compact circuit composed of a low-precision ramp generator and a small digital block. The self-test principle is demonstrated on a spiking neuron circuit design in an 0.35µm CMOS technology.

SMACD Technical Session *Room CO 016*
"Modeling the next generation of Electronics and Sensors" **Tuesday, 13:20-15:20**
Chair: Axel Hald, *Robert Bosch GmbH, Germany*

13:20 Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs

Esteban Garzón[1], Raffaele De Rose[1], Felice Crupi[1], Lionel Trojman[2], Giovanni Finocchio[3], Mario Carpentieri[4] and Marco Lanuzza[1]
[1]DIMES - University of Calabria, Italy [2]Universidad San Francisco de Quitom, Ecuador [3]MIFT Department - University of Messina, Italy [4]DEI - Politecnico di Bari, Italy

This paper explores performance and technology-scalability of STT-MRAMs exploiting double-barrier MTJs (DMTJs) as comparatively evaluated with respect to conventional solution based on single-barrier MTJs (SMTJs). The comparative study was carried out at different design abstraction levels: (i) a bitcell-level analysis relying on the use of Verilog-A compact models, and (ii) an architecture-level analysis for various memory sizes. Overall, our simulation results point out that, thanks to the reduced switching currents, DMTJ-based STTMRAMs allow reducing write latency of about 60% than their SMTJ-based counterparts. This is achieved while assuring lower energy consumption under both write (-40%) and read (-27%) accesses, at the cost of reduced sensing margins.

13:40 A Sparsity-Aware MOR Methodology for Fast and Accurate Timing Analysis of VLSI Interconnects

Dimitrios Garyfallou, Charalampos Antoniadis, Nestor Evmorfopoulos and Georgios Stamoulis
University of Thessaly, Greece

Signoff timing analysis is essential in order to verify the proper operation of VLSI circuits. As process technologies scale down towards nanometer regimes, the fast and accurate timing analysis of interconnects has become crucial, since interconnect delay represents an increasingly dominant portion of the overall circuit delay. It is a common view that traditional SPICE transient simulation of very large interconnect models is not feasible for full-chip timing analysis, while static Elmore-based methods can be inaccurate by orders of magnitude. Model Order Reduction (MOR) techniques are typically employed to provide a good compromise between accuracy and performance. However, all established MOR techniques result in dense system matrices that render their simulation impractical. To this end, in this paper we propose a sparsity-aware MOR methodology for the timing analysis of complex interconnects. Experimental results demonstrate that the proposed method achieves up to 30x simulation time speedups over SPICE transient simulation of the initial model, maintaining a reasonable typical accuracy of 4%.

14:00 A Modeling Approach for 7nm Technology Node Area-Consuming Circuit Optimization and Beyond

Qiang Huo, Zhenhua Wu, Feng Zhang and Ling Li
Institute of Microelectronics, Chinese Academy of Sciences, China

This work presents a novel statistical-based general compact model for 7nm technology node devices like FinFETs. Unlike conventional compact model based on less accurate elements including one-dimensional Poisson equation for three-dimensional devices and analytical equations for short channel effects, quantum effects and other physical effects, the general compact model combining few TCAD calibrated compact models with statistical methods can eliminate the tedious physical derivations. The general compact model has the advantages of high accuracy, strong scaling capability, good robustness and excellent transfer capability. It is demonstrated that the performance of 6T SRAM and RC control ESD power clamp through the trade-off between two key design knobs of FinFET can be improved extremely with implementation of the newly proposed general compact model. This framework is also

suitable for path-finding researches on 5nm node gate-all-around devices, like nanowire FETs, nanosheet FETs and beyond.

14:20 Error-Free Calculation of Total Referred Noises in Electronic Circuits

Sotoudeh Hamedi-Hagh
San Jose State University, United States

Noise of Electronic devices can be accurately modelled if noise transformations are not oversimplified to incorporate errors. The absence of manual techniques to calculate network noises accurately have contributed to such oversimplifications. Calculation of network noises using three universal rules are presented in this paper. Network noises are then transferred to input and output of the network as voltages or currents to represent the total referred noises of the network. The noise of four amplifiers are derived in this paper and are compared with results generated by a simulator to verify the accuracy of the proposed manual technique.

14:40 Modeling of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors

Federico Pace[1], Olivier Marcelot[1], Philippe Martin-Gonthier[1], Olivier Saint-Pé[2], Michel Breart de Boisanger[2], Rose-Marie Sauvage[3] and Pierre Magnan[1]
[1]ISAE-SUPAERO, France [2]Airbus, France [3]Direction Générale de l'Armement, France

This paper aims to model Parasitic Light Sensitivity (PLS) in Global Shutter CMOS Image Sensors (GS-CIS) through separation of the optical problem from the carriers motion one, reducing required simulation time. The optical problem is solved thanks to Finite-Differences Time-Domain (FDTD) simulations. Solution to the carriers motion problem is shown in two ways: through use of Boltzmann Transport Equation (BTE) and through a straight line type of motion. The results show good reproduction of experimental data behavior, though fitting could still be improved.

15:00 Model-Based Engineering of Magnetic Sensors

Zsombor Lázár[1], Yves Bidaux[1], Markus Roos[2] and Gael Close[1]
[1]Melexis, Switzerland [2]NM Numerical Modelling GmbH, Switzerland

A modern car contains about 30 magnetic sensors on average. Their performance depend on the readout circuit imperfections, the magnetic environment, and mechanical assembly tolerances. For angle sensors, this yields a complex physics with magnet tilt and off-axis rotation. Traditionally these effects are studied separately in finite-element-method (FEM) simulators, separated from traditional system and circuit design simulation tools. This creates a simulation gap. A new modeling method for physical modeling of magnetic position sensors is presented. The method is based on spherical harmonic decomposition, and is implemented in Matlab. In this representation, any rigid-body 3-D motion of the magnet and sensor is modeled by matrix operations. Critical physical effects for the sensor accuracy can then be explored directly in system simulation tools such as Matlab, Simulink, Python or even in an integrated circuit simulator. The method maintains finite-element-method (FEM) accuracy. It represents a paradigm shift in magnetic position sensor design, and brings FEM accuracy to a much wider range of users.

PRIME Technical Session
"Radio Frequency Circuits and Systems I" — Tuesday, 15:40-17:00 — *Room CO 123*
Chair: Piero Malcovati, *University of Pavia, Italy*

15:40 Fully digital-IF based RF-DAC Transmitter

Erkan Bayram, Oner Hanay, Mohamed Saeed and Renato Negra
RWTH Aachen University, Germany

This work presents the first digital-IF based RF- DAC transmitter. This approach uses a digital IF signal to up-convert the baseband data into the IF-band before mixing it with the LO signal based on the proposed technique. The systematic problems like LO-leakage and pulling effect of the VCO on the LO-signal of direct transmission based RF-DACs are eliminated in this new concept. Therefore, higher SNR within the desired bandwidth can be achieved which allows to use complex modulation schemes and, in return, increases the transmitted data rate of the overall system. The digital-IF based RF-DAC consists of unit cells with a segmented architecture and a resolution for 12-bit in the I and Q paths. The chip was designed in TSMC 65-nm CMOS technology. The core size of the chip is 0.4 mm2 and it consumes 150 mW. More than 53 dB of spurious free dynamic range (SFDR) can be handed based on the post-layout simulation results.

16:00 A 6-15 GHz ultra-wideband signal generator with 82 % continuous tuning range for FMCW radar

Tom Drechsel, Niko Joram and Frank Ellinger
TU Dresden, Dresden

This paper presents an ultra-wideband signal generator for FMCW radar application. The system is based on a charge pump phase-locked loop architecture and features a continuous tuning range from 6 GHz to 15 GHz combined with

low in-band phase noise of -80 dBc/Hz and 105 dBc/Hz in average at 1 MHz offset to the carrier. The system utilizes a hybrid structure where the voltage controlled oscillator was fabricated using 130 nm SiGe BiCMOS technology and the lower frequency components are off-the-shelf. An FPGA enables different waveform generation in the frequency domain. The synthesizer is suitable to operate as an ultra-wideband, low phase noise, small and low cost signal generator for frequency domain waveform generation like frequency chirps for FMCW primary radar with ultra high range resolution. The power consumption of the core components amounts to 340 mW and the size of the system is 6 cm x 7 cm.

16:20 Design and Comparison of Low Power Pulse Combining IR-UWB Transmitters in 180nm CMOS

Okan Zafer Batur[1], Semih Ramazanoğlu[2] and Günhan Dündar[2]

[1]İstanbul Bilgi University, Turkey [2]Boğaziçi University, Turkey

This paper presents design and comparison of low power pulse shaping methods for achieving low energy per pulse (EPP), Impulse Radio Ultra-Wideband (IR-UWB) transmitter. The proposed transmitters are composed of all digital single pulse generator, multiple delay lines, a pulse combination circuit, and pulse shaping stages with a pulse shaping capacitor and wire-bond inductor at the output. The generated mono pulse width and the consecutive mono pulse positions are determined by the delay lines. The proposed transmitter architectures are designed in 180 nm CMOS. The simulation results show that the energy required to generate the Gaussian mono-cycle, triplet, and quintuplet pulses are 10.5 pJ, 22.15 pJ, and 36.5 pJ respectively at 200 MHz pulse repetition frequency (PRF) without band pass filter (BPF). The required energies utilizing a BPF to generate output signals are 17.5 pJ, 31.5 pJ, and 46 pJ respectively.

16:40 JESD204B Compliant 12.5 Gb/s LVDS and SST Transmitters in 28 nm FD-SOI CMOS

Firat Celik[1], Ayca Akkaya[1], Armin Tajalli[2], Andreas Burg[1] and Yusuf Leblebici[1]

[1]Ecole Polytechnique Fédérale de Lausanne, Switzerland [2]University of Utah, United States

JESD204B compliant low-voltage differential signaling (LVDS), and source-series-terminated (SST) transmitters in 28 nm FD-SOI CMOS technology are presented with 1.1 pJ/bit and 1.7 pJ/bit at 12.5 Gb/s, respectively. An external 6.25 GHz single-ended clock, which is terminated internally with mid-common-mode termination, is used for half-rate operation in both designs, which can achieve open eye diagrams at 12.5 Gb/s data rate. Both transmitters are measured and compared in terms of design complexity, power consumption, area, and signal integrity performance. From architecture selection to circuit design, power consumption is minimized while maintaining the maximum data rate that the JESD204B standard supports. High-speed standard cell ESD diodes are employed for the pads to achieve >1kV HBM ESD protection, while adding 200 fF parasitic capacitance.

PRIME Technical Session
"Sensing and Biomedical Circuits I" — Tuesday, 15:40-17:00 — *Room CO 015*
Chair: Gianluca Giustolisi, *University of Catania, Italy*

15:40 On Chip Counting and Localisation of Magnetite Pollution Nanoparticles

Siming Zuo[1], Jiuge Chen[1], Hua Fan[2], Rami Ghannam[1] and Hadi Heidari[1]

[1]University of Glasgow, United Kingdom [2]University of Science and Technology of China, China

Magnetic nanoparticles are generally smaller than 200 nm surrounding our environment and can easily enter the human brain through the respiratory system. The harm of such nanoparticles may endanger people's health. This paper focuses on modelling and simulation based on a new kind of magnetic sensors, which can count and localize these magnetite nanoparticles. The proposed sensors could help to prevent these nanoparticles from the polluted environment and undoubtedly reduce their adverse risks to humans. The modelled magnetic system consists of a tunnelling magnetoresistive (TMR) sensor array, a conducting line, and the detected magnetite nanoparticles. The localization and quantization of these nanoparticles can be achieved by analysing total output voltages from the TMR sensor array.

16:00 Post-CMOS 3D-Integration of a Nanopellistor

Finja Marina Münchenberger[1], Stefan Dreiner[1], Holger Kappert[1] and Holger Vogt[2]

[1]Fraunhofer, Germany [2]University Duisburg Essen, Fraunhofer Institute for Microelectronic Circuits and Systems IMS, Germany

To further optimize micro pellistors and reduce the required chip area, one possibility is to fabricate the sensor on top of the integrated circuit (IC). Therefore a sacrificial layer process developed by the Fraunhofer IMS combining deep reactive ion etching (DRIE) and atomic layer deposition (ALD) is modified. First fundamentals of pellistors and Joule heating are described. Then simulations to determine ideal heater shapes are presented and an approach for a process to fabricate pellistors on top of an IC is introduced.

16:20 An integrated nanoplasmonic biosensor for monitoring single-cell cytokine secretion

Xiaokang Li[1], Maria Soler[2], Crispin Szydzik[3], Khashayar Khoshmanesh[3], Julien Schmidt[4], Filiz Yesilköy[1], Alexander Belushkin[1], George Coukos[4], Arnan Mitchell[3] and Hatice Altug[1]
[1]EPFL, Switzerland [2]Catalan Institute of Nanoscience and Nanotechnology, Spain [3]RMIT University, Australia, [4]University of Lausanne, Switzerland

We introduce an innovative label-free nanoplasmonic biosensor for real-time analysis of cytokine secretion at single-cell resolution. Our biosensor is integrated with a novel design of a microfluidic device with low-volume microchamber and fluid regulation for analyzing cytokine secretion from individual cells in real-time. We detect and distinguish different spatiotemporal profiles of interleukin-2 secretion from single lymphoma cells. This new biosensor configuration is anticipated to be a powerful tool for single-cell studies.

16:40 Comparison of Direct Digitization Current Sensing Circuits for EIS

Mahdi Rajabzadeh, Matthias Häberle and Maurits Ortmanns
University of Ulm, Germany

In this work, a qualitative comparison between state of the art current recorders for biomedical applications is presented. Prior work showed that direct digitizing frontends outweight their analog counterparts. This work performs a comparison between the direct digitization frontends, namely time-based and current-input CTSDM frontends. It is shown that time-based converters - due to usage of current conveyors to generate a low impedance node - suffer from inferior linearity. Also the trade-off between SNR versus conversion time limits their achievable SNR and the maximum input signal frequency. On the other hand, with the usage of a FIR-DAC within a current input CTSDM, the requirements of the critical first amplifier are highly relaxed. In addition, the FIR-DAC reduces the influence of clock jitter and allows the current-input CTSDM to achieve a higher SNR and linearity compared to the time-based converters.

SMACD Competition Event
"Powering the Smarts" Competition — Tuesday, 15:40-17:00 — *Room CO 124*
Organizer: Dialog Semiconductor
Chair: Giulia Di Capua, *University of Salerno, Italy*

15:40 Wide Frequency Range Impedance Measurement of a Li-ion Prismatic Cell for Power Line Communication Technique

Arash Pake Talei[1], Wolfgang Pribyl[2] and Günter Hofer[1]
[1]Infineon Technologies Austria, Austria [2]Graz University of Technology, Austria

This paper explains the proper way of measuring a prismatic li-ion battery cell which is used in electric vehicles. The challenges and the solution of connecting a battery cell to a vector network analyzer are discussed. It is shown how to properly measure, calculate and de-embed the parasitic components of the medium connector. At the end a prismatic cell is measured in a wide frequency range from 1MHz to 1GHz.

16:00 Modeling of Low-dropout Regulator (LDO) to Optimize Power Supply Rejection (PSR) in System-On-Chip (SoC) Applications

Jun Tan and Ralf Sommer
IMMS, Germany

This paper presents a methodology to model and optimize the power supply rejection (PSR) for a low-dropout regulator (LDO) in system-on-chip (SoC) applications. Since SoC designs integrate multiple functions on a single chip, the PMU becomes crucial to meet the requirements for multiple sub-blocks. The supply ripple, which has a significant impact on sensitive analog/RF sub-blocks, needs to be reduced by achieving optimized PSR performance in LDO designs. This paper begins by modeling the conventional LDO topology. The transfer function of the model is calculated, so that the system behaviour can be remapped to the parameters of the sub-blocks. Additionally, the verification is done by comparing the model and a transistor level design. Finally, the methodologies are discussed in two cases, namely a PSR of -50 dB @ 100 kHz and a full-spectrum PSR of -50 dB. The results show that different design strategies generate practical design trade-offs, although all strategies can theoretically achieve the cases. With the proposed methodologies, the design parameters can be clearly and efficiently optimized to achieve optimum PSR performance.

16:20 Wireless Power Transmission of a Smartphone by Three-dimensional Magnetic Resonance

Min Gu Kim, Ye Rim Lee and Jun Rim Choi
Kyungpook National University, South Korea

In this paper, a 4-coil resonance-based wireless power transfer system is designed at 6.78 MHz to wirelessly charge the smartphones. The proposed design is simulated using a magnetic field simulator and is validated through experiment. Additionally, the power transfer efficiency (PTE) of the system is analyzed under perfect alignment, lateral and angular misalignments. The coil is designed with a PTE of more than 74% of the A4WP specification at any

location. The measurement results confirmed that PTE does not change drastically under misalignment conditions and is over an average of 60% when measured at any alignment conditions.

16:40 3-D Maximum Power Point Searching and Tracking for Ultra Low Power RF Energy Harvesters

Michele Caselli and Andrea Boni
University of Parma, Italy

Radio-frequency (RF) energy harvesting must cope with the limited availability and high variability of the energy source. In this paper, the modeling of an RF harvester for ultra low power environments is presented. Simulation results and theoretical analysis demonstrate that the maximum transferred power point is located in a three-dimensional space defined by the input capacitance, the output voltage, and the load resistance of the rectifier circuit. The paper proposes also the implementation in ST 65 nm CMOS technology of a mixed signal system for the 3-D MPPT, to be embedded in an RF harvester. The circuit exhibits a power consumption lower than 100 nW, making this solution suitable for ultra low power harvesting.

Wednesday Morning, July 17th

PRIME Technical Session
Data Converters **Wednesday, 10:20-12:00** *Room CO 123*
Chair: Franceso Mazzilli, *Melexis*

10:20 A 0.3 V 15 nW 69 dB SNDR Inverter-Based Delta-Sigma Modulator in 0.18 um CMOS

Lorenzo Benvenuti, Alessandro Catania, Mattia Cicalini, Andrea Ria, Massimo Piotto and Paolo Bruschi
University of Pisa, Italy

This paper presents an ultra-low voltage, ultra-low power, inverter-based, discrete time delta sigma modulator. The modulator employs a novel, two-stage, switched capacitor integrator that overcomes most of the issues introduced by ultra-low voltage inverter-like amplifiers. A prototype designed in 0.18 µm CMOS technology is presented. With a supply voltage of only 0.3 V, the modulator reaches an SNDR of 69.9 dB for a signal bandwidth of 80 Hz and a clock frequency of 20 kHz. Thanks to a power consumption of only 15.47 nW, this analog-to-digital converter is suitable for interfacing a wide variety of sensors in energy harvesting applications. Different bandwidth-power consumption trade-offs are possible by moderate increase of the power supply voltage.

10:40 Design of a 12-bit SAR ADC with digital self-calibration for radiation detectors front-ends

Andrea Di Salvo
Politecnico di Torino - INFN Torino, Italy

The paper describes the design of a 12-bit SAR ADC with digital self-calibration to be used in multi-channel ASICs for radiation detectors employed in nuclear and particle physics. In these systems, a highly segmented sensor is coupled to a front-end chip with many channels operating in parallel. The details of the signal processing to be performed depend on the particular applications, but in several cases it is necessary to embed on the front-end chip a large number of analog-to-digital converters (32 or more) that have to operate simultaneously. Typical requirements for the converter are a resolution in the 10-12 bits range, a sampling frequency above 20 Msamples/sec, very low power consumption and good radiation hardness. The ADC discussed in this paper is based on a fully differential SAR architecture assisted by a digital background calibration that relies on the Offset Double Conversion (ODC) method. The algorithm uses an analog offset injection to compute the intrinsic error of the ADC conversion due to mismatch among the DAC capacitors. The approach allows to find a set of weights, which are then applied at each conversion to achieve a real-time correction. The ADC was preliminary modelled with a high level C++ code. Physical implemented in both in 110 nm and 65 nm CMOS technologies is underway. The paper focuses on the design and hardware implementation of the calibration algorithm. The average ENOB after correction is incremented by 4 bits by using a 15% random capacitor mismatch. The SFDR is hold below -90 dB. The power consumption of the calibration circuit is 5.6 mW and 3 mW respectevely for 110 nm and 65 nm node. A further study investigated how many bit have to be calibrated to hold a reasonable ENOB.

11:00 A 1-1 MASH using two Noise-Shaping Switched-Capacitor Dual-Slope converters

Christopher Rogi[1], Ruben Garvi[2] and Enrique Prefasi[2]
[1]Infineon, Austria [2]Universidad Carlos III de Madrid, Spain

In Multi-stAge noise-SHaping (MASH) topologies a higher order of noise-shaping is achieved via converter cascading. The quantization error of the first stage is extracted, processed by another stage and ideally cancelled from a reconstructed output signal. However, often the quantization error must be derived by a separate Digital-to-Analog Converter (DAC). This requires additional hardware and design effort. Noise-shaping dual-slope converters show an interesting property which can be exploited in MASH converters. At certain time points an equivalent representation of the quantization error is available in the voltage domain which can be simply sampled be the cascaded stage. This property is utilized in this paper by building a audio bandwidth 1-1 MASH using two switched-capacitor dual-slope converters. Circuit level details including the timing diagram and MASH parameter estimation give adequate design insight. Digital and analog matching are the main disadvantage of MASH topologies. This quantization error leakage is discussed using system level mismatch analysis.

11:20 A Practical Architecture for SAR-based ADCs with Embedded Compressed Sensing Capabilities

Carmine Paolino[1], Fabio Pareschi[1], Mauro Mangia[2], Riccardo Rovatti[2] and Gianluca Setti[1]
[1]Politecnico di Torino, Italy [2]University of Bologna, Italy

In this paper we propose an innovative A/D architecture with the ability to acquire an input signal according to the recently introduced Compressed Sensing (CS) paradigm. The architecture relies on the hardware blocks already found in traditional successive-approximation-register (SAR) A/D converter, requiring only the addition of a limited number of switches. The capacitive array at the core of the circuit is used both by the SAR conversion algorithm and

to realize the linear combination of consecutive signal samples, as required by the CS framework. The lack of additional active blocks allows for a remarkable saving in sampling energy with respect to published solutions. The role of some design parameters is investigated and solutions to ease the circuital implementation are analyzed.

PRIME Technical Session
Sensing and Optical Circuits **Wednesday, 10:20-12:00** *Room CO 015*
Chair: Hadi Heidari, *University of Glasgow, United Kingdom*

10:20 Design of a Capacitive Humidity Sensor Frontend with an Adaptive Resolution for Energy Autonomous Applications

Maximilian Wiener and Benjamin Saft
IMMS GmbH, Germany

We present a 9-bit energy-efficient capacitive sensor frontend for the parallel measurement of soil moisture and air humidity with an adaptive resolution. The circuit is based on already published successive approximation (SAR) capacitance-to-digital-converter (CDC) but offers two improvements for range extension specifically for humidity sensing. Commercial sensor elements for humidity sensing show a big variety of dynamic ranges and a considerable large offset capacitance. Hence, a fixed resolution and dynamic range of the CDC would lead to non-optimal range utilization. To overcome this issue, our implementation provides offset subtraction and adaptive range adjustment. The proposed circuit was implemented in a commercial 0.18-µm CMOS process. Simulations were performed and the CDC achieved an energy per conversion of 11.49 pJ from a 1.8-V supply. The capacitive input range is adjustable in the range of 52-825 pF what corresponds to CLSB = 0.1-1.61 pF.

10:40 A Versatile Mixed-Signal Large Dynamic Range Front-End ASIC for High Capacitance Detectors

Weishuai Cheng
Politecnico di Torino INFN, Sezione di Torino, Italy

A 64-channel mixed-mode ASIC, suitable for particle detectors of large dynamic range and high capacitance up to 100 pF, is presented. Each channel features an analogue front-end for signal amplification and filtering, and a mixed signal back-end to digitize and store the signal information. The analogue part consists of a versatile low impedance pre-amplifier based on RCG (Regulated Common-Gate) amplifier, and two shapers optimised for time and energy measurements. The back-end part mainly includes discriminators, TDCs and ADCs, which are used to process the signal and encode both the time of arrival and the charge of the input signal with a fully digital output. The programmable gain of the front-end (2-400 fC input dynamic range) and the versatile back-end allow the readout of different types of gaseous detectors. The ASIC is designed for an event rate up to 100 kHz per channel with a power consumption less than 10 mW/channel, has been fabricated in a 110 nm CMOS technology. This chip is a revised version of the TIGER ASIC, which was developed for the readout of the new BESIII CGEM Inner Tracker.

11:00 Low-Cost and High-Integration Optical Time Domain Reflectometer using CMOS Technology

Jee Hun Yeom, Keunyeol Park, Jaehyuk Choi, Minkyu Song and Soo Youn Kim
Dongguk University, South Korea

This paper describes the design of application specific integrated circuit (ASIC) technology for optical time domain reflectometer (OTDR) which is used for optical signal transmission and reception. Conventional OTDR products are implemented with discrete integrated circuit (IC) devices. However, these configurations are vulnerable to noise, leading to the limitation to achieving high dynamic range (DR) and signal to noise ratio (SNR). In addition, it is difficult to lower power consumption and cost, since each IC requires its own power consumption with large area. Therefore, we propose high-DR OTDR that shows low power consumption and small chip area. The proposed OTDR chip is fabricated with a 350nm 2-poly 4-metal CMOS process and the area iss 5mm x 4mm. The measurement results show that power consumption of analog-to-digital converter (ADC) is under 100µW with 3.3V of the power supply.

11:20 Wide Range AWG-Based FBG Interrogation System With Improved Sensitivity

Vincenzo Romano Marrazzo, Michele Riccio, Luca Maresca, Andrea Irace and Giovanni Breglio
University of Naples Federico II, Italy

In this paper, a Fiber Bragg Grating (FBG) sensor's interrogation system is presented. The concept employs an Arrayed Waveguide Grating (AWG) whose working principle is to demultiplex the light reflected from the FBG (that is sensitive with temperature and strain variation) in many channels in dependence with the frequency. The wavelength can be sensed as the power ratio between two adjacent AWG channels with a dynamic range that is equal to the whole AWG spectrum. In this case of study, four channel are employed. From the optical part, the signal is then converted in electrical through photodiode array and read with a low-noise transimpedance amplifier. The output signal is then elaborated from a custom conversion algorithm in FPGA environment. The aim of the work is to demonstrate, through analytical approach and numerical simulations from an optoelectronic point of view, the feasibility of the system erasing the typical trade-off sensitivity/dynamic range that affects the current AWG-based interrogation system.

11:40 Conceptual Study for Ultra Miniaturized High-Precision Optical CMOS Sensors Unaffected by Gradients in Illumination

André Feiler, Jürgen Oehm, Dominik Veit and Lukas Straczek
Ruhr-University Bochum (AG AIS), Germany

In this study a specially revised version of the concept for measuring the angle of incidence of light [1] was used, which is particularly well suited for the construction of trigonometric sensor concepts with external dimensions of only a few millimeters. The aim of the study was to break down the interrelationships for the overall systemically achievable accuracies. The study therefore focused on the lowest possible power consumption of the LED light source used, minimum component dimensions and quantities, outline of the practicable minimum distances between LED light source and integrated sensor unit, robustness of the sensor against gradients and intensity changes in lighting, illumination intensity and sensor noise, as well as the requirements for the precision of the mechanical components used. It could be shown that the key limiting factor isn't the optical/electronic precision of the CMOS sensor concept used, but the finite precision of the mechanical components used.

SMACD Technical Session
Design Techniques and Optimization Methods Wednesday, 10:20-12:00 *Room CO 124*
Chair: Jean-Michel Sallese, *École polytechnique fédérale de Lausanne, Switzerland*

10:20 Power-Down Mode Verification for Hierarchical Analog Circuits

Maximilian Neuner and Helmut Graeb
Chair of Electronic Design Automation, Technical University of Munich, Germany

To reduce the power consumption of modern system-on-chips, parts of the system can be switched off when not required for system operation. Additional circuitry realizes this power-down mode functionality of an analog circuit by shutting off all of its bias currents. When connecting several circuit blocks with individually verified power-down modes together, the correct power-down functionality of the overall circuit cannot be guaranteed anymore as new short-circuit paths might emerge due to the resulting connectivity. In this paper, a new method for power-down mode verification of hierarchical analog circuits is presented. It will be explained how the obtained verification results can be used to revise and correct detected errors. The presented concepts are illustrated for a high input impedance differential amplifier formed by three Miller operational amplifiers and a network of resistors.

10:40 Efficient Circuit Reduction in Limited Frequency Windows

George Floros, Nestor Evmorfopoulos and George Stamoulis
University of Thessaly, Greece

Model Order Reduction (MOR) has become key enabler for the efficient simulation of large circuit models. MOR techniques based on Balanced Truncation (BT) offer very good error estimates and can provide compact models with any desired accuracy over the whole range of frequencies (from DC to infinity). However, in most applications the circuit is only intended to operate at specific frequency windows, which means that the reduced-order model can become unnecessarily large to achieve approximation over all frequencies. In this paper, we present a frequency-limited approach which, combined with low-rank factorized solution, can handle large input models and provably leads to reduced-order models that are either smaller or exhibit better accuracy than full-frequency BT.

11:00 Automatic Modeling of Transistor Level Circuits by Hybrid Systems with Parameter Variable Matrices

Ahmad Tarraf and Lars Hedrich
University of Frankfurt, Germany

Model abstraction of transistor-level circuits, while preserving an accurate behavior, is still an open problem. In this paper an approach is presented that automatically generates a hybrid automaton (HA) with linear states. The resulting HA is used for reachability analysis. Each of the locations of the HA is modeled with a system matrix described as a matrix zonotope or interval matrix. This leads to an acceptable over approximation, but guarantees that the system behavior is covered. The approach starts with a netlist at transistor level with full SPICE accuracy and ends at the system level description of the circuit. To illustrate our methodology, an example of a circuit containing complex poles and strong nonlinear limiting behavior is analyzed.

11:20 Pseudo Expected Improvement Based Optimization for CMOS Analog Circuit Design

Nawel Drira[1,2], Mouna Kotti[1,3], Mourad Fakhfakh[3], Patrick Siarry[2] and Esteban Tlelo-Cuautle[4]
[1]Univ. of Gabès, Tunisia [2]Univ. of Paris-Est Créteil, France [3]University of Sfax, Tunisia [4]INAOE, Mexico

In this paper, we consider the use of a new parallel efficient global optimization algorithm based on the use of the pseudo expected improvement (PEI) criterion, for the optimal design of analog circuits. A comparison with the conventional efficient global optimization algorithm (EGO) is presented. We show, via two analog circuit designs that the proposed approach gives the same optimal circuit sizing but within reduced computing time.

11:40 A New Adaptation of Particle Swarm Optimization Applied to Modern FPGA Placement

Yun Zhou, Dries Vercruyce and Dirk Stroobandt
Ghent University, Belgium

This paper presents a new adaptation of the discrete particle swarm optimization method applied to the FPGA placement problem, a crucial and time-consuming step in the FPGA synthesis flow. We evaluate the performance of the new optimizer against the existing version by embedding them into a publicly available FPGA placer Liquid to replace the simulated annealing-based optimizer used for the hard block optimization. The benchmark testing using Titan23 circuits shows the runtime efficiency of the new optimizer with comparable post-routed results achieved to that of Liquid using simulated annealing.

SMACD Technical Session
Bioelectronics **Wednesday, 10:20-12:00** *Room CO 016*
Chair: Mustafa Berke Yelten, *Istanbul Technical University, Turkey*

10:20 A Low-Frequency 3-Coil Inductive System for Wirelessly Powering Leadless Pacemakers

Krithikaa Mohanarangam, Min Gu Kim and Jun Rim Choi
Kyungpook National University , South Korea

The purpose of this study is to investigate the outcome of a small-sized implant at low frequency for powering the pacemakers. To do so, a 3-coil inductive wireless power transfer system having a solenoid implantable coil is designed at low-frequency in the air and tissue mediums and the performance is evaluated on the basis of power transfer efficiency (PTE). The PTE of the designed system is analyzed at perfect alignment, lateral and/or angular misalignments with respect to varying distances between the coils and input powers. The simulations are carried out by a magnetic field simulator at 13.56 MHz for input powers of 1 W and 500 mW. The maximum lateral and angular misalignments considered are 20 mm and 60 degrees respectively. When the distance between the external and implantable coils in air is 40 mm, a maximum PTE of 0.24 % is achieved at perfect alignment and conversely, a minimum PTE of 0.11 % is obtained at 60 degrees of angular misalignment. The efficiency drops by 0.10 % at perfect alignment with tissue in between the coils. Based on the simulated results it is observed that, a minimum of 600 mW input power is required for powering the pacemaker at 13.56 MHz in tissue medium even under severe misalignment of coils.

10:40 Wireless Readout System Modeling for Electrodeless QCM

Okan Zafer Batur[1], Ahmet Sarı[1] and Ceyhun Kırımlı[2]
[1]İstanbul Bilgi University, Turkey [2]Acıbadem University, Turkey

In this paper, we present a wireless and electrodeless Quartz Crystal Microbalance (WE-QCM) sensor measurement system. The QCM characteristics are measured using a network analyzer and microstrip antennas and the results are modeled by Butterworth Van Dyke (BVD) electrical equivalent circuit model. The WE-QCM model and the proposed energy detection transceiver based wireless measurement system are simulated using analog mixed signal (AMS) tools. The mixed signal simulations show that less than 0.5 kHz sensitivity in frequency variations can be achieved with the proposed system model.

11:00 Modeling and performance investigation of insulin injection pen for diabetic persons

Maria-Alexandra Paun[1] and Catherine Dehollain[2]
[1]Swiss Federal Institute of Technology (EPFL), Switzerland [2]Ecole Polytechnique Fédérale de Lausanne, Switzerland

This paper is focused on modeling and performance investigation of insulin injection pens used by diabetic persons. A smart pen cap with two electrodes is used as a capacitive sensor for insulin dose detection and is presented in details. To faithfully analyze this medical device, both an analytical model and a fully parametrized three-dimensional physical model in ANSYS have been developed. The electrode capacitance is evaluated (by both simulations and analytical model), for the smart pen cap alone as well as for different insulin fill states in the insulin injection pen + smart pen cap complete system.

11:20 Will There be Light? - Simulative Prediction of Fluorescence Measurements

Florian Kögler, Alexander Hofmann and Georg Gläser
IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, Germany

Fluorescence-based methods of measurement play a vital role in biochemical sensing applications. To design integrated measurement circuitry, the properties of the signal to be measured have to be known. Since there is no comprehensive framework for these estimations available, this approximation has to be done manually. By using an divide-and-conquer approach, we separate fluorescent measurement systems into three components that can be described with existing radiometric or electrical models. Based on this modeling, we show a framework to estimate properties of time-resolved fluorescence signals in the sense of electrical signals. Out of these equations, we present a case-study for deriving a measurement system's specification for a given scenario.

11:40 A Low-Noise CMOS Inverter-Based OTA for Biomedical and Healthcare Signal Receivers

Ricardo Póvoa[1], Ricardo Martins[1], Nuno Lourenço[1], António Canelas[1], Nuno Horta[1] and Joao Goes[2]
[1]Instituto de Telecomunicações, IST–Ulisbon, Portugal [2]Faculdade de Ciências e Tecnologia - UNL, Portugal

This paper presents an innovative topology for an operational transconductance amplifier (OTA) based on a CMOS inverter topology. This OTA is proper for biomedical and healthcare circuits and systems, due to a low level of noise and power consumption, together with elevated gain. This is a fully-differential implementation, with a double CMOS branch biased by two pairs of voltage-combiners, in both NMOS and PMOS configurations, highly improving the gain and the gain-bandwidth product, improving the OTA energy-efficiency. An elevated figure-of-merit is achieved, i.e., a 1628 MHz×pF/mA, and a gain of 53 dB, under a voltage supply source of 2 V. The results are compared with state-of-the-art OTAs in this field of study and the potential is fully fulfilled with a state-of-the-art layout-aware optimization tool, AIDA, particularly important to overcome the device stacking problematic in lower supplies.

Wednesday Afternoon, July 17th

PRIME Technical Session
Radio Frequency Circuits and Systems II **Wednesday, 13:20-15:00** *Room CO 123*
Chair: Maria-Alexandra Paun, *École polytechnique fédérale de Lausanne, Switzerland*

13:20 Design Approach for a Broadband Class-D Power Amplifier for Low Power Application in a 28 nm Digital CMOS Technology

Mantas Sakalas, Jens Wagner, Niko Joram and Frank Ellinger
TU Dresden, Germany

This work presents a class D Power Amplifier (PA) analysis and design in digital CMOS technology. Two topologies of a class D PA were implemented, fabricated and tested under lab conditions. The 1st topology uses no bandwidth limiting linearization network and demonstrates an ultra-wideband 0 – 11 GHz operation. It features a very compact design, a peak power added efficiency (PAE) of 38 % and a flat output power of POUT = 10.5 dBm. The 2nd topology on the other hand, features harmonic filtering on the output side, yielding 2nd and 3rd harmonic suppression of 26 dBc and 32 dBc respectively, an output power POUT = 11 dBm and a peak PAE of 22.5 % within a 1 – 4 GHz bandwidth.

13:40 A Ka-Band Low-Noise Amplifier for Space Applications in a 100 nm GaN on Si technology

Lorenzo Pace[1], Walter Ciccognani[1], Sergio Colangeli[1], Patrick Ettore Longhi[1], Ernesto Limiti[1] and Rémy Leblanc[2]
[1]University of Rome Tor Vergata, Italy [2]OMMIC SAS, France

In this paper a MMIC Low-Noise Amplifier operating in Ka-band is presented. The chosen technology is a 100 nm GaN HEMT on a High Resistivity Silicon substrate. A fully deterministic approach based on constant mismatch circles has been used for the preliminary synthesis of matching networks. The designed four-stages LNA presents a 33 dB gain, Input/Output matching better than 21 dB and a Noise Figure of no more than 2.3 dB in the whole operating band, showing the suitability of the chosen technology to low-noise, high gain and linearity applications.

14:00 A Ka-band Doherty Power Amplifier using an innovative Stacked-FET Cell

Ferdinando Costanzo[1], Rocco Giofrè[1], Vittorio Camarchia[2], Paolo Colantonio[1] and Ernesto Limiti[1]
[1]University of Roma Tor Vergata, Italy [2]Electronics and Telecommunications Department, Politecnico di Torino, Italy

This paper presents an innovative stacked-FET cell useful to enhance both, gain and output power of RF and mm-wave power amplifiers. The new structure has been validated through the design of a downlink Ka-band Doherty Power Amplifier. The resulting module is a two stages Microwave Monolithic Integrated Circuit (MMIC) fabricated on a commercial 100nm gate length Gallium nitride on Silicon technology. The design was carried out to satisfy not only the power requirements but also to meet the thermal constraints for space use. Simulation results have shown a power added efficiency (PAE) greater of 30% at 6dB of output power back-off with a peak of output power of 38dBm inside the operative band, from 17.3 GHz to 20.3 GHz. Whereas, a saturated gain above 17dB has been achieved with a gain flatness better than 0.5dB in the overall band. The chip area is 5x3.7mm2.

14:20 Band Specific Suppression of Harmonics and its Effects on Power Efficiency

Rahul Nadgouda and Bernd Deutschmann
Institute of Electronics, Graz University of Technology, Austria

Certain applications demand band specific linearity i.e removing harmonics which lie in a specific band while the rest of the spectrum is kept unaffected. The shape of the signal waveform changes by altering the amplitude and phase of these harmonics. This change in shape of the signal affects power efficiency (PE) in different ways. The effects

become more dominant for power amplifiers driving a large load. In this paper, some effects of harmonic cancellation on PE are observed and documented. The waveform used is a square wave in low frequency domain.

14:40 A Dual-Band Impedance Transfomer for Matching Frequency Dependent Complex Source and Load Impedances

Antra Saxena[1], Deepayan Banerjee[1], Mohammad Hashmi[2] and Medet Auyenur[2]
[1]Indraprastha Institute of Information Technology Delhi, India [2]Nazarbayev University, Kazakhstan

A dual-band matching network capable of providing impedance matching between two arbitrary frequency dependent complex source and load impedances is reported. The proposed topology consists of three sections namely two L-network and a π-network and possesses closed-form design equations. A number of case studies are included to demonstrate the effectiveness of the proposed technique for distinct source and load impedances at two arbitrary frequencies of interest. A prototype, working at two uncorrelated frequencies of f1 = 1 GHz and f2 = 1.8 GHz, fabricated on RO5880 shows a very good agreement between the measured and simulated results.

PRIME Technical Session
Circuits for Reliability and Resiliency — Wednesday, 13:20-15:00 — *Room CO 015*
Chair: Flavio Sestagalli, *Coilcraft*

13:20 Quality Aware Approximate Memory in RISC-V Linux Kernel

Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri and Francesco Menichelli
Sapienza University of Rome, Italy

Improving power consumption and performance of error tolerant applications is the target of the design paradigm known as approximate computing. One of the units of a computational architecture where approximations can be introduced is the memory subsystem, leveraging on the resilience of an application to maintain an acceptable output quality even if its input data are subject to imprecision and errors. This paper proposes and implements the management, in the Linux kernel, of multiple approximate memory banks. Applications can then allocate approximate memory for their data structures selecting between different level of approximation, depending on the requirements on output quality. This allows to design an architecture where approximate physical memory, instead of being composed of a unit intercepting a single point in the energy-quality tradeoff curve, can be split in multiple banks adopting different tradeoffs between approximation level and energy savings. We finally show a case study in the results, where we explore the allocation of different data structures of a signal processing application, depending on sensitivity to errors and desired output quality.

13:40 Circuit Design and Verification Method of Integrated Sensor-Front-End Elements for Spaceborne Fluxgate Magnetometers

Maximilian Scherzer[1], Mario Auer[1], Aris Valavanoglou[2], Stefan Leitner[2] and Werner Magnes[2]
[1]Technische Universität Graz, Austria [2]Austrian Academy of Sciences, Austria

To date nearly all sensor-front-end implementations for spaceborne fluxgate magnetometers are discrete. In order to assure a lightweight and power efficient design it is therefore crucial to integrate the essential components on a single chip. This work describes the design of highly integrated sensor-frontend elements for spaceborne fluxgate magnetometers. The design of a current-source required for the linearization of the fluxgate magnetometer via current feedback is shown. It uses a Howland current-source to realize a current-controlled current-source (CCCS) on chip. Harsh environmental conditions mandate the use of system monitoring and temperature calibration. The ADC used for monitoring environmental conditions is implemented as a 2nd order discrete time delta-sigma modulator. This interface circuit was realized in a 180nm technology using an active area of less than 1mm2. To evaluate the system performance a verification method is proposed based on a MCU that drives a highly linear chopped 1-bit DAC.

14:00 Analysis of FTB stress propagation in an Integrated Circuit

Lorenzo Quazzo[1], Yann Bacher[1], Nicolas Froidevaux[1], Henri Braquet[2] and Gilles Jacquemod[2]
[1]ST Microelectronics, France [2]Polytech'Lab, France

In this paper, the FTB stress propagation is analyzed in the case of a MCU. The common to differential mode conversion is demonstrated. The PDN and its resonance frequencies are the key element for understanding the weakness or robustness of the circuit. The main objective of this work is to study the stress propagation in order to increase the robustness of the MCU against FTB stress. Correlations between resonance frequencies and FTB stress are given.

14:20 Analysis of a Circuit Primitive for the Reliable Design of Digital Nonlinear Oscillators

Tommaso Addabbo, Ada Fort, Riccardo Moretti, Marco Mugnaini and Valerio Vignoli
University of Siena, Italy

We propose a heuristic generalized modeling aiming to investigate relevant aspects concerning the stability of circuits that combine asynchronous digital gates in feedback networks. After the theoretical inspection of some specific cases,

we propose the design of novel low-complexity digital oscillators, that in FPGAs can reach decorrelation times half the ones of the fastest Ring Oscillator obtainable following conventional methods.

14:40 Effect of SSN on signal and power integrity on 32-bit microcontroller : modeling and correlation

Melanie Moign[1], Jean Pierre Leca[2], Nicolas Froidevaux[2], Gilles Jacquemod[1] and Yves Leduc[1]
[1]Polytech'Lab, France [2]STMicroelectronics, France

This paper presents a methodology to create a Simultaneous Switching Noise (SSN) predictive SPICE model for a 32-bit microcontroller. Here, the purpose is to predict the noise interference generated by switching IOs and establish new design/layout rules for the next product generation in order to reduce these interferences. This model achieves an accurate correlation between measurements done on a 32-bit MCU and Eldo simulations. Then, features are defined in order to build this accurate model. Having this, a deeper research work can be done only by simulation.

SMACD Technical Session
Powering Everyday Electronics **Wednesday, 13:20-15:00** *Room CO 124*
Chair: Ricardo Póvoa, *Instituto de Telecomunicações, Portugal*

13:20 Design of Differential-Mode Input Filters for DC-DC Switching Regulators

Giulia Di Capua, Nicola Femia and Kateryna Stoyka
DIEM - University of Salerno, Italy

This paper discusses a novel approach to EMI filter design, based on parametric charts that allow to achieve optimal damping by matching the winding resistance of the damping inductor with the ratio between filter and damping inductances. The proposed approach simplifies the identification of the smallest commercial components complying with attenuation and efficiency requirements. Experimental results presented in the paper validate the proposed model and design method.

13:40 A Piecewise-Affine Inductance Model for Inductors Working in Nonlinear Region

Alberto Oliveri, Matteo Lodi and Marco Storace
University of Genoa, Italy

In this paper a piecewise-affine (PWA) power-loss-dependent inductance behavioral model is proposed, for ferrite-core inductors used in switch-mode power supplies (SMPSs). The model expresses the inductance at steady-state as a function of easily-measurable quantities. The PWA formulation leads to a faster computation with respect to the arctangent models available in the literature and allows analytically computing the inductor current based on its voltage. The model is validated through experimental measurements on a buck converter, showing a reliable prediction of the steady-state inductor current, under different SMPS working conditions.

14:00 Sensitivity Analysis of Inductive Power Transfer Systems for Electric Vehicles Battery Charging

Giulia Di Capua, Nicola Femia and Kateryna Stoyka
D.I.E.M. - University of Salerno, Italy

This paper investigates the sensitivity of inductive power transfer systems for electric vehicles battery charging. The goal of the analysis is to assess the impact of harmonics on the transferred power and on the efficiency, in order to define the main specifications for design and calibration of relevant measurement systems. The first harmonic approximation models of a Series/Series system and a Series-Parallel/Series system is developed to perform the analysis with respect to the variations of main operating parameters and coils mutual coupling. The resulting model predictions are validated by comparison with PSIM simulations.

14:20 Realistic Cable Modeling for Low-Voltage Installations

Stefano Maranò[1], Yannick Maret[1], Matija Varga[1], Luca Ghezzi[2] and Agostino Butti[2]
[1]ABB, Switzerland R&D, [2]ABB Electrification, Italy

Numerical models of electrical cables are important to describe accurately signal propagation in electrical networks. We are interested in the modeling of cables used in low-voltage electrical networks. We observed that numerical cable models exhibit unrealistically sharp resonances and antiresonances. We propose an approach to generate cable models with realistic resonances and antiresonances by modifying the attenuation constant. The proposed approach is validated with VNA measurements performed on SPT-2 cable specimens of different lengths.

14:40 Analysis and Optimization of Power Supply Rejection (PSR) for Power Management Unit (PMU) Design in RFID Sensor applications

Jun Tan and Ralf Sommer
IMMS, Germany

This paper presents a methodology for analyzing and optimizing the power supply rejection (PSR) for a PMU in RFID sensor applications. Since RFID design is typically system-on-chip (SoC) that integrates multiple functions on a single chip, multi-frequency supply ripples can be observed. Since the supply ripple is a significant input noise for the sensors, the noise reduction is needed to achieve accurate sensor operations. Firstly, it is necessary to analyze the ripple frequencies from each source. Then, the conventional PMU for the calculation of transfer function is modeled to reveal the system behaviour. Since the crucial factor defining the overall PSR is explained, a system level optimization is given, that requires only a simple modification and can be applied to conventional PMU designs. The simulation results show that the system significantly reduces the input ripple after optimization with an improved PSR from 24 dB to -20 dB. Finally, the theory is applied to a fabricated CMOS design as a case study that achieves a PSR measurement of -26 dB from 400 Hz to 25 MHz.

SMACD Competition Event
EDA Competition: Part I **Wednesday, 13:20-15:00** *Room Auditoire CO2*
Chairs: Engin Afacan, *Kocaeli University, Turkey* and Fábio Passos, *Instituto de Telecomunicações, Portugal & Instituto de Microelectrónica de Sevilla, Spain*

13:20 IEEE CEDA

Prof. David Atienza
EPFL, Switzerland

13:30 Mixed-Signal Hardware Security Using MixLock: Demonstration in an Audio Application

Julian Leonhard[1], Marie-Minerve Louërat[1], Hassan Aboushady[1], Ozgur Sinanoglu[2] and Haralampos-G. Stratigopoulos[1]
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In this paper, we demonstrate a recently proposed security technique for mixed-signal circuits in the context of a real application. The security technique, called MixLock, is based on logic locking of the digital section of the mixed-signal circuit and can be used as a countermeasure for reverse engineering and counterfeiting. We demonstrate MixLock in an audio application, where the underlying Sigma-Delta ADC that digitizes the audio input is locked. We show the effect that locking has on the recorded audio quality based on a metric that counts the resultant glitches per second and by also providing a link where the interested reader can download and listen to output audio samples for locked and unlocked versions of the Sigma-Delta ADC.

14:00 Automated Parameter Extraction and SPICE Model Modification For Gate Enclosed MOSFETs Simulation

Boris Contreras, Gladys Ducoudray, Rogelio Palomera and Carlos Bernal
University of Puerto Rico at Mayaguez, Puerto Rico

This work focuses in using experimental measurements to extract the aspect ratio (W/L) for Gate-Enclosed or Annular MOSFETs. All measurements and calculations are performed with an automated virtual instrumentation (VI) environment developed in LabVIEW. The VI was capable of extracting threshold voltage and low field mobility, needed for W/L calculation. An extraction procedure for the body effect factor is also presented. For validation purposes, extracted parameters were compared with those provided by the foundry (MOSIS) using traditional rectangular transistors. The extracted W/L was validated by comparing to Giraldo's experimental method. The SPICE BSIM 3 model parameters provided by the foundry is then modified using the extracted parameters including the aspect ratio. With this modification better simulation results were obtained. They were compared to the experimental measurements for an annular MOSFET drain voltage vs drain current characteristic curves at different gate voltages, showing an improvement of 58% when compared to the original non modified SPICE model parameters.

14:30 Exploiting LabVIEW FPGA Socketed CLIP to Design and Implement Soft Core Based Complex Digital Architectures on PXI FPGA Target Boards

Luca Dello Sterpaio, Pietro Nannipieri, Antonino Marino and Luca Fanucci
University of Pisa, Italy

PXI FPGA Peripheral Modules by National Instruments are meant to be used in LabVIEW even without any previous knowledge of Hardware Description Languages (HDL) and let users to hardware accelerate their own test and measurement setups. However, designers fluent in HDL languages avoid such closed technology targets due to impossibility to include third party designs or the needed over effort to implement large and complex architectures into it, such as soft core based systems. In this paper a partially automated workflow to take advantage of the PXI environment while empowering advanced HDL engineers to implement complex architectures is presented with reference to a successful use case example.

SMACD Competition Event
EDA Competition: Part II **Wednesday, 15:20-16:20** *Room Auditoire CO2*
Chairs: Engin Afacan, *Kocaeli University, Turkey* and Fábio Passos, *Instituto de Telecomunicações, Portugal & Instituto de Microelectrónica de Sevilla, Spain*

15:20 TiDeVa: A Toolbox for the Automated and Robust Analysis of Time-Dependent Variability at Transistor Level

Pablo Saraza-Canflanca[1], Javier Díaz Fortuny[2], Rafael Castro Lopez[1], Elisenda Roca[1], Javier Martin Martinez[2], Rosana Rodriguez[2], Montserrat Nafria[2] and Francisco Fernandez[1]
[1]IMSE-CNM, CSIC and Universidad de Sevilla, Spain [2]Universitat Autònoma de Barcelona (UAB), Spain

Time-Dependent Variability has attracted increasing interest in the last years. In particular, phenomena such as Bias Temperature Instability, Hot Carrier Injection and Random Telegraph Noise can have a large impact on circuit reliability, and must be therefore characterized and modeled. For technologies in the nanometer range, these phenomena reveal a stochastic behavior and must be characterized in a massive manner, with enormous amounts of data being generated in each measurement. In this work, a novel tool with a user-friendly interface, which allows the robust and fullyautomated parameter extraction for RTN, BTI and HCI experiments, is presented.

15:50 Identification of EMI Induced Changes During the Design of ICs using a Post-Processing Framework

Dominik Zupan and Bernd Deutschmann
Institute of Electronics (IFE), Graz University of Technology, Graz, Austria

In this paper a post-processing framework is presented that can be applied during the design phase of integrated circuits. The aim of this work is to help designers to identify electromagnetic interference issues of their designs, already during the concept or design phase. The developed tool is mainly written in Python and therefore versatilely usable. In general it can be applied to a large range of potential issues, due to e.g. radio frequency interference, ESD (electrostatic discharge), etc., occurring in circuit design. However, this paper focuses on the investigation of changes that are introduced in a current regulator by injecting radio frequency interferences into specific circuit blocks. The main scripts are designed environment independent and can therefore be used for a broad range of simulators.

PRIME Technical Session
Analog Circuits and Sub-systems II **Wednesday, 15:20-16:40** *Room CO 123*
Chair: Olivier Pourchet, *Coilcraft*

15:20 A 0.3nV/√Hz Input-Referred-Noise Analog-Front-End for Weakly-Interacting-Massive-Particles (WIMPs) Acoustic Sensing in Bubbles-Chamber Detectors

Elia Arturo Vallicelli[1], Luca Gelmi[1], Roberto Bertoni[2], Walter Fulgione[1], Mattia Tambaro[1], Andrea Baschirotto[2], and Marcello De Matteis[1]
[1]University of Milano Bicocca, Italy [2]Istituto Nazionale di Fisica Nucleare, Italy

The Mosca-B-Detector (Materia OSCura a Bolle, dark matter bubble detector) is a geyser bubble chamber based on a superheated C3F8 volume in a closed vessel which aims to detect Dark Matter Weakly Interacting Massive Particles (WIMPs). When a particle interacts with the fluorine atoms, energy is released in small volume that acts as a nucleation site, producing a bubble and an acoustic signal, which are sensed by means of a set of ultrasound sensors and high-speed cameras. Each event, detected by threshold crossing approach, presents a specific acoustic signature (signal amplitude, duration and bandwidth) that can be used to separate the involved particles from background noise and thus detects an eventual WIMP interaction. However, the very low event rate (few events/day) along with weak signal amplitude (100 - 101 μV0-PEAK range) and small intrinsic sensor noise (2.3 nV/√Hz), forces strong constraints on the electronics noise to maximize the sensitivity of the detector to weak signals (thus minimizing false negatives/missed detections). This work presents the design of a 45 dB 0.3 nV/√Hz Input Referred Noise analog front-end specifically dedicated to bubble chamber detectors. The final 0.2 dB Noise Figure allows to set a 7-sigma threshold as low as 14μV (input-referred), thus allowing to observe the weakest events and thus maximize the detector sensitivity.

15:40 4-Channel Front-End Integrated Circuit For Readout of Large Area of SiPM under Liquid Argon

Alejandro David Martinez Rojas
Politecnico di Torino and INFN Torino, Italy

This paper presents the structure and transistor-level design of CMOS front-end amplifier for the readout of large area SiPM at LAr temperature (87 K). The front-end circuit, a trans- impedance amplifier and a summing amplifier, has been designed using a standard 110 nm CMOS technology, and the simulation results with the foundry PDK are included in this work. Each stage is implemented in a Folded Cascode Operational Trans- impedance Amplifier (OTA)

architecture with a power rail of +1.25 V and -1.25 V, a power consumption of 95 mW and an open-loop gain over 100 dB. The target sensor is a SiPM tile of 24 cm2 produced in the Darkside collaboration project, with 6 MΩ of quenching resistance and 6 nF/cm2 capacitance. For a single photoelectron (250 fC), the front-end can achieve a signal-noise ratio above 12 and a jitter better than 45 ns.

16:00 A Timing Pixel Front-End Design for HEP Experiments in 28 nm CMOS Technology

Lorenzo Piccolo
INFN, Italy

This work describes the design of a low-power low-jitter, analog front-end for timing-pixel radiations sensors. The circuit will provide the input stage for the front-end ASIC proposed for the TimeSpOT project that will be manufactured in a commercial 28 nm CMOS process. This front-end is designed to be part of 4D tracking detectors for future high data rate high energy physics experiments. This research aims at realizing 55 µm × 55 µm pixels with sub 100 ps resolution within less then 10 µW power consumption.

16:20 Exploring 3D Pixel Circuits for Small Pitch and High Brightness GaN Microdisplays.

Yoann Seauve, Margaux Vigier, Thomas Pilloix and Gilles Sicard
CEA Leti, France

Gallium nitride (GaN) based LEDs are a promising technology for microdisplays thanks to the brightness they can provide. However, they have not been widely adopted for this type of applications yet, partly due to the size and complexity of the associated driver circuits. In this paper, we demonstrate that despite the complexity of the driver circuits, a very small pixel pitch can be achieved thanks to CMOS 3D technology.

PRIME Technical Session
Digital Circuits and Emerging Technologies **Wednesday, 15:20-16:40** *Room CO 015*
Chair: Danilo Demarchi, *Politecnico di Torino, Italy*

15:20 A 48 mW 18 Gb/s Delay-Line Based 1:4 Demultiplexer in 45-nm RFSOI CMOS

Sami Rehman, Mahdi Khafaji, Corrado Carta and Frank Ellinger
TU Dresden, Germany

This paper presents the design and characterization of a new delay-line based demultiplexer (Demux). The Demux works by setting the delay of each delay-element in the delay-line equal to the period of the input symbol and the delay of the delay-line equal to the period of the sampling clock. Once the delay-line is sampled, each sampled output represents a unique symbol in the input symbol sequence. As opposed to the traditional tree architecture Demux, the proposed delay-line Demux dissipates power only in the delay-line. In addition to design simplicity, the delay-line Demux also offers power and area advantages over tree Demux when scaled to a higher channel count. Designed in 45-nm RFSOI CMOS, the Demux achieves 2.6 pJ/symbol of energy figure, which, to the best of the authors knowledge, is the best reported among inductor-less CMOS Demuxes.

15:40 A Fully Adaptive Lattice-based Notch filter for Mitigation of Interference in GPS

Syed Waqas Arif, Adem Coskun and Izzet Kale
University Of Westminster, United Kingdom

Intentional jammer broadcasting hop-frequency Continuous Wave Interference (CWI) signal present a major threat to the operation of the Global Navigation Satellite System (GNSS). Adaptive notch filtering provides an excellent countermeasure and deterrence against (CWI). This paper describes a comparative performance analysis of two different types of adaptive notch filtering algorithms for GPS specific application. These are 1) Direct form 2nd Order and 2) Lattice-Based adaptive notch filter. The AWGN and interference signal power is taken in a wide dynamic range to assess the performance of each individual adaptive algorithms. Signal to Nosie Ratio (SNR) is an important parameter for the evaluation of the functionality of the receiver under different conditions. Performance of each algorithm is determined under various conditions such as different, Jamming to Noise Density (J/N_0) versus effective SNR at the output of the correlator. A Fully Adaptive Lattice Notch Filter is proposed, which is able to simultaneously adapt both its coefficient to alter center frequency of notch along with the bandwidth of the notch. The filter demonstrated superior tracking ability and convergence speed than other counterpart. Along with that this paper also describes the complete modelling of GPS L1 signal in MATLAB.

16:00 A New Lightweight CSPRNG Implemented in a 0.18µm CMOS Technology

Miguel Garcia-Bosque, Guillermo Díez-Señorans, Adrián Pérez-Resa, Carlos Sánchez-Azqueta, Concepción Aldea and Santiago Celma
University of Zaragoza, Spain

In this work, a new Cryptographically Secure Pseudo-Random Number Generator (CSPRNG) has been proposed. This generator has been implemented in a 0.18 um technology and has been capable of generating sequences at a

high speed, using a small area and low power consumption. The output sequences generated by this system have been subjected to the NIST randomness tests proving that they are indistinguishable from a truly random sequence. Finally, other security-related aspects have been studied proving that the proposed generator is cryptographically secure.

16:20 Bistable Propagation of Monostable Molecules in Molecular Field-Coupled Nanocomputing

Yuri Ardesi, Luca Gnoli, Mariagrazia Graziano and Gianluca Piccinini
Politecnico di Torino, Italy

The Molecular Field-Coupling Nanocomputing is considered as one of the most promising technologies which are intended to outperform the current CMOS scenario. The information is encoded in the charge distribution of molecules and propagated thanks to intermolecular electrostatic interaction. Recent works have discussed the possibility of using monostable molecules to achieve extremely low power computation, encoding the information in the polarization of the molecule. Monostable molecule have been analysed as a single element, yet it is not obvious whether they can be used to propagate the information from molecule to molecule, or the information is lost after few molecules. In this work, we analyze from a theoretical point of view the information propagation in wires realized with monostable molecules. We define a parameter named ``bistable coefficient'' which directly links the molecule size, the molecule polarizability, and the intermolecular distance to the propagation of the information, providing a metric for the characterization of the bistable propagation. We define a Safe-Operating Area which can be used as a reference by chemists and technologists for the definition of a class of molecules which can be used for digital molecular Field-Coupled Nanocomputing.

SMACD Technical Session
Very large scale reliability **Wednesday, 13:20-15:00** *Room CO 124*
Chair: Maike Taddiken, *University of Bremen, Germany*

15:20 A new Method for the Analysis of Radiation-induced Effects in 3D VLSI Face-to-Back LUTs

Luca Sterpone, Ludovica Bozzoli, Corrado De Sio, Boyang Du and Sarah Azimi
Politecnico di Torino, Italy

In recent years, three-dimensional IC (3D IC) has gained much attention as a promising approach to increase IC performance due to their several advantages in terms of integration density, power dissipation and achievable clock frequencies. However, the reliability of 3D ICs regarding soft errors induced by radiation is not investigated yet. In this work, we propose a method for evaluating the sensitivity of 3D ICs to Single Event Transient induced by Heavy Ions. The flow starts with identifying the characteristics of the generated transient pulses with respect to the radiation profile and 3D layout of the design. Secondly, our method provides a Dynamic Error Rate using a Simulation-based Fault Injection environment. Experimental results achieved applying the approach on a 15nm 3D configurable Look-Up-Table (LUT) designed on two tiers demonstrated the feasibility of the method, showing the vulnerability characterization of four different functional configurations using eight different types of heavy ions.

15:40 A Fluctuation Model of a HfO2 RRAM Cell for Memory Circuit Designs

Feng Zhang[1], Linan Li[2], Qiang Huo[1], Cong Fang[2], Wenqiang Ba[2]
[1]Institute of Microelectronics, Chinese Academy of Sciences, China [2]School of Electronic and Information Engineering, Beijing Jiaotong University, China

A resistive random access memory device based on HfO2 with outstanding nonvolatility is fabricated. A dynamic Verilog-A model obeying the electrochemical metallization conductive filament mechanism is demonstrated. The fluctuation of conductive filament growth is added to this model, and the model is verified by DC voltage scanning. The simulation and experimental data are compared using data processing software. Experimental results verify the good electrical characteristics of the RRAM device. Modeling of the fluctuations of RRAM devices provides guiding significance to the design of peripheral circuits.

16:00 Long-Term Reliability Management For Multitasking GPGPUs

Zeyu Sun, Taeyoung Kim, Marcus Chow, Shaoyi Peng, Han Zhou, Hyoseung Kim, Daniel Wong and Sheldon Tan
University of California, Riverside, United States

This paper proposes long-term reliability management for spatial multitasking GPU architectures. Specifically, we focus on electromigration (EM)-induced long-term failure of the GPU's power delivery network. A distributed power delivery network model at functional unit granularity is developed and used for our EM analysis of GPU architectures. We use a recently proposed physics-based EM reliability model and consider the EM-induced time-to-failure at the GPU system level as a reliability resource. For GPU scheduling, we mainly focus on spatial multitasking, which allows GPU computing resources to be partitioned among multiple applications. We find that the existing reliability-agnostic thread block scheduler for spatial multitasking is effective in achieving high GPU utilization, but poor reliability. We develop and implement a long-term reliability-aware thread block scheduler in GPGPU-Sim, and compare it against existing reliability-agnostic scheduler. We evaluate several use cases of spatial multitasking and find that our proposed scheduler achieves up to 30% improvement in long-term reliability.

16:20 Dynamic Reliability Management for Multi-Core Processor Based on Deep Reinforcement Learning

Zeyu Sun, Han Zhou and Sheldon Tan
University of California, Riverside, United States

In this paper, we propose a new dynamic reliability management (DRM) approachwith deep reinforcement learning (DRL) for multicore processors considering device reliability eects (hard error) and transient error of signal (soft error). The proposed method is based on a recently proposed physics-based three-phase electromigration model and an exponential soft error model that considers dynamic voltage and frequency scaling (DVFS) eects. Applying DRL method can achieve better and exible control quality. Compared with the traditional Q-learning based method, DRL method has better scalability, lower memory and lower computational complexities. Experimental results show that the proposed method signicantly reduces memory footprint and computational time compared to the traditional Q-learning based method. Furthermore,we show that the DRL-based DRM method can save 53.50% more energy than the Q-learning based.

Thursday Morning, July 18th

PRIME Technical Session
Image and Data Processing **Thursday, 10:20-12:00** *Room CO 123*
Chair: Kemal Ozanoglu, *Dialog Semiconductor*

10:20 Efficient Architecture for Integral Image Computation on Heterogeneous FPGAs

Fanny Spagnolo, Pasquale Corsonello and Stefania Perri
University of Calabria - DIMES, Italy

Integral image (IIM) is an intermediate image representation, employed in several computer vision algorithms. Although only simple arithmetic operations are required to compute an IIM, the total number of additions increases quadratically with the input image size. For this reason, the design of hardware architectures able to accelerate the IIM computation receives a great deal of attention. Unfortunately, existing solutions are not appropriate for the integration within high-performance embedded systems, which are currently realized within modern heterogeneous CPU-FPGA System on Chips (SoCs). In this paper, we present a novel hardware architecture for accelerating the IIM computation. The proposed design outperforms existing competitors by parallelizing operations along both rows and columns of the input image. Experiments, conducted on a Zynq-7000 XC7Z020 SoC, demonstrate that the novel accelerator achieves a speed per computation unit up to 124 times higher than prior works, saving more than 70Mbits of on-chip memory resources for 1920×1080 frame resolutions.

10:40 Real-Time Neural Spikes Imaging by a 9375 sample / (sec pixel) 32x32 pixels Electrolyte-Oxide-Semiconductor Biosensor

Mattia Tambaro[1], Elia Arturo Vallicelli[1], David Tomasella[1], Andrea Baschirotto[1], Stefano Vassanelli[2], Marta Maschietto[2] and Marcello De Matteis[1]
[1]University of Milano-Bicocca, Italy [2]University of Padova, Italy

This paper presents a FPGA Real-Time Neural Spikes (RT-Neu) Imaging system that processes and detects in real-time the electrical activity of a neurons population taken from rat hippocampi on an Electrolyte-Oxide-Semiconductor (EOS) Multi Electrode Array (MEA) local matrix of 32x32 pixels. A demo video can be found at [ref] (password: rtneu). RT-Neu has been implemented on Xilinx Zynq-7000 ARM/FPGA SoC. RT-Neu receives the neural signals coming from a 9375 Sample/(sec·pixel) 32x32 pixels EOS Biosensor, filtering the single-pixel low-frequency offset/noise components and finally performing a multi-pixel signal processing (using a PCA-based correlation algorithm) to provide a final spatial map of the neural culture electrical activity. The correlation algorithm has been implemented to operate on multiplexed signals allowing to identify single neural Action Potentials (AP) with amplitudes as low as 215 μV0-PEAK.

11:00 DCNN for Tactile Sensory Data Classification based on Transfer Learning

Mohamad Alameh, Maurizio Valle, Ali Ibrahim and Gabriele Moser
Università degli Studi di Genova, Italy

Tactile data processing still an open challenge, in this paper we will demonstrate a method to achieve touch modality classification using pre-trained Convolutional Neural Network. The 3D tensorial tactile data generated by real human interaction on an electronic skin (E-Skin) were transformed into 2D images. Using CNN and Transfer Learning, the feasibility and efficiency of the proposed method, has been proven using a real tactile dataset, and by outperforming classification of the same problem in the literature.

11:20 Data Oriented Approximate K-Nearest Neighbor Classifier for Touch Modality Recognition

Hamoud Younes[1], Ali Ibrahim[2], Mostafa Rizk[1] and Maurizio Valle[2]
[1]Lebanese International University, Lebanon [2]University of Genoa, Italy

Approximate Computing Techniques offer a promising solution to reduce the hardware complexity and power consumption imposed when embedding machine learning algorithms. The reduction comes at the cost of some performance degradation. This paper presents an approximate machine learning classifier for touch modality recognition. Experimental results demonstrate that the use of software level approximation techniques reduce the execution time and memory usage up to 38% and 55% respectively, at the cost of accuracy loss less than 10% for our target application.

11:40 Smart imagers modeling and optimization framework for embedded AI applications

Luis Angel Cubero Montealegre, Arnaud Peizerat, Dominique Morche and Gilles Sicard
Université Grenoble Alpes - CEA, France

This work presents a framework for behavioral simulations of smart imagers with hardware and power constraints. The objective is to compare innovative imaging systems that would be composed of a specific image sensor and a dedicated image processing. For that purpose, a versatile imager model is presented and applied to a time-to-first-spike imager associated with two types of neural networks. Image classification is targeted to assess the system performance, namely the classification accuracy and data throughput. Simulation results depict/show the impact of different key-parameters helping in the choice of the final imaging system architecture.

PRIME Technical Session
Sensing and Biomedical Circuits II **Thursday, 10:20-12:00** *Room CO 015*
Chair: Sandro Carrara, *École polytechnique fédérale de Lausanne, Switzerland*

10:20 Multi-Target Electrolyte Sensing Front-End for Wearable Physical Monitoring

Ivan Ny Hanitra, Francesca Criscuolo, Sandro Carrara and Giovanni De Micheli
EPFL (Integrated Systems Laboratory), Switzerland

Wearable physiology is an expanding field, especially for sports applications that steadily require an accurate monitoring of the physical status of athletes. This work presents the co-design and the realization of an hardware front-end that enables multi-sensing of up to four endogenous electrolytes. A pH and temperature readout circuit are included for sensor calibration. The platform is validated with potassium and sodium ions monitoring. The hardware is remotely controlled by an user interface that configures the sensor panel and collects the biological data through a Bluetooth link. The sizes of the frontend circuit allows its integration into a headband, suitable for wearable monitoring in sweat.

10:40 Modelling of Implantable Photovoltaic Cell based on Human Skin Types

Jinwei Zhao, Kaung Oo Htet, Rami Ghannam, Muhammad Imran and Hadi Heidari
University of Glasgow, United Kingdom

Implantable electronic devices are emerging as important healthcare technologies due to their sustainable operation and low risk of infection. To overcome the drawbacks of the built-in battery in implantable devices, energy harvesting from the human body or another external source is required.. Energy harvesting using appropriately sized and properly designed photovoltaic cells enable implantable medical devices to be autonomous and self-powered. Among the challenges in using PV cells is the small fraction of incident light that penetrates the skin. Thus, it is necessary to involve such physical properties in the energy harvesting system design. Consequently, we propose a novel photodiode model that considers skin loss in different ethnic groups. Our physical simulations have been implemented using COMSOL and MATLAB. Circuit and system modelling has been performed using Cadence 180nm technology. Our results show that the transmittance of near infrared light is almost the same in three skin types: Caucasian, Asian and African. Maximum power delivery of 12 μW (African skin) and 14 μW (Caucasian and Asian skin) were achieved at 0.45 V. With the help of a power management unit, an output voltage of 1.8-2 V was achieved using the PV cells.

11:00 RF energy harvested sensory headwear for quadriplegic people

Alfiero Leoni[1], Giuseppe Piscitelli[2], Iolanda Ulisse[1], Mariachiara Ricci[2] and Vito Errico[2]
[1]University of L'Aquila, Italy [2]University of Roma Tor Vergata, Italy

In this work we present engineering optimization of our battery-operated sensory headwear, which uses an inertial measurement unit to detect the head movements and wireless transmits the acquired data. The manoeuvrability with the head, without the use of hands, makes it ideal for the autonomous use by people with reduced motor skills, such as quadriplegics, for home automation and direct control of actuators. 915MHz radio frequency energy harvester provide additional power to the system, thus increasing the usable time of the headwear and permitting the adoption of a smaller lightweight battery. The harvester, based on commercial chipset, has been conceived to operate with a custom loop antenna integrated on the headwear. In optimal condition, with a fixed RF feeder, an average efficiency as output to input power ratio, around 70% at 5dBm input power level, has been obtained.

11:20 A CMOS Analog Front-End for Implantable Pulmonary Artery Pressure Monitoring System

Mustafa Besirli, Kerim Ture, Diego Barrettino, Marco Mattavelli and Catherine Dehollain
Ecole Polytechnique Fédérale de Lausanne, Switzerland

This paper presents an energy-efficient analog front-end circuit to monitor the pulmonary artery pressure (PAP) with piezoresistive sensors. A low-power capacitively-coupled instrumentation amplifier (CCIA) is developed in order to boost the amplitude of the bridge sensor to the input range of the analog-to-digital converter (ADC). The 1/f noise and input-referred offset of the amplifier are eliminated by the chopping technique. Simulation results show that this CCIA with chopping technique achieves an input-referred noise density of 38.7 nV/√Hz and an input-referred offset voltage of 4 μV with a current consumption of 4.28 μA at 1.8 V voltage supply. This gives a noise-efficiency factor (NEF) of 3.1. Dual supply voltages are used to decrease the power consumption of the bridge sensor. The pressure range is selected to be between 0 and 125 mmHg and the bandwidth of the interface is set from DC to 400 Hz with an RC low pass filter (LPF). This low-noise, low-offset analog front-end circuit achieves an accuracy of 0.125 mmHg.

11:40 Quasi-Digital Biosensor-Interface for a Portable Pen to Monitor Anaesthetics Delivery

Simone Aiassa[1], Francesca Stradolini[2], Abuduwaili Tuoheti[1], Sandro Carrara[2] and Danilo Demarchi[1]
[1]Politecnico di Torino, Italy [2]Ecole Polytechnique Fédérale de Lausanne, Switzerland

Monitoring of patient response to the anaesthetic drugs is an attractive improvement for achieving a correct balance of sedation level, increasing the chance of success in the right procedure of anaesthesia. Nowadays, there are no commercial tools able to offer real-time monitoring of anaesthetics, indeed, there is still a lack in sensing technologies able to maintain high performances in long term monitoring within a portable miniaturised hardware system. To overcome these limitations, we are here presenting the innovative concept of a portable pen-device able to sense anaesthetic compounds over time. This study is based on an electrochemical sensor to be fully integrated into a complete pen-shaped point-of-care for the monitoring of anaesthesia delivery. The design of the system is based on a bio-inspired event-based approach that is guaranteeing low complexity, low power consumption and is therefore suitable to be scaled to fit the barrel of a pen. An exhaustive comparison between the proposed system and a lab instrument proves that the presented approach obtains comparable performances in terms of sensitivity and resolution with the ones obtained by expensive commercial instrumentation, meanwhile, the results show a 95% power consumption reduction and a 92% area decrease w.r.t. previously presented implementation.

SMACD Special Session — Thursday, 10:20-12:00 — *Room CO 124*
"MEMS & heterogeneous systems: Which design tools and methodologies are missing?"
Organizer/Chair: Prof. Ralf Sommer, *Technical Universtiy of Ilmenau, Germany*

10:20 Tutorial "Challenges in Modeling and Simulation of Inertial MEMS"

Prof. Jan Mehner
Chemnitz University of Technology, Germany

11:20 Parasitic Extraction Methodology for MEMS Sensors with Active Devices

Axel Hald[1], Robert Wolf[1], Johannes Seelhorst[1], Jürgen Scheible[2], Jens Lienig[2], Stefan Tibus[3] and Mike Schwarz[3]
[1]Automotive Electronics, Robert Bosch GmbH, Germany, [2]Reutlingen University, Robert Bosch Center for Power Electronics, Germany [3]Dresden University of Technology, Institute of Electromechanical and Electronic Design, Germany

Nowadays, the demand for a MEMS development/design kit (MDK) is even more in focus than ever before. In order to achieve a high quality and cost effectiveness in the development process for automotive and consumer applications, an advanced design flow for the MEMS (micro electro mechanical systems) element is urgently required. In this paper, such a development methodology and flow for parasitic extraction of active semiconductor devices is presented. The methodology considers geometrical extraction and links the electrically active pn-junctions to SPICE standard library models and finally extracts the netlist. An example for a typical pressure sensor is presented and discussed. Finally, the results of the parasitic extraction are compared with fabricated devices in terms of accuracy and capability.

11:40 Efficient Design and Layout of Capacitive 3D Accelerometer

Steffen Michael and Ralf Sommer
Ilmenau University of Technology, Germany

An approach for a mostly automated design and layout of capacitive accelerometers is presented, which permits the efficient synthesis of accelerometers up to 3 axes. The functionality of the hierarchical approach is shown using the example of a 3D accelerometer for tire-pressure monitoring systems (TPMS) using the open platform technology XMB10 from X-FAB.

SMACD Technical Session
Variability and Aging — Thursday, 10:20-12:00 — *Room CO 123*
Chair: Manuel Barragan, *TIMA Laboratory, France*

10:20 Experimental Characterization of Time-Dependent Variability in Ring Oscillators

Juan Nuñez[1], Elisenda Roca[1], Rafael Castro-Lopez[1], Javier Martin-Martinez[2], Rosana Rodriguez[2], Montserrat Nafria[2] and Francisco V. Fernandez[1]
[1]IMSE-CNM (CSIC/Universidad de Sevilla), Spain [2]Universitat Autònoma de Barcelona (UAB), Spain

Reliability in CMOS-based integrated circuits has always been a critical concern. In today's ultra-scaled technologies, a time-varying kind of variability has raised that, on top of the well-known time-zero variability, threatens to shorten the lifetime of integrated circuits, both analog and digital. Effects like Bias Temperature Instability and Hot Carriers Injection need to be studied, characterized and modeled to include, and, thus, mitigate, their impact in the design of CMOS integrated circuits. This paper presents an array-based integrated circuit whose purpose is precisely that: to

observe, quantify and characterize the impact of time-dependent variability effects in a specific kind of circuits: Ring Oscillators.

10:40 Charge-Based Model for Reliability Analysis Flow of Flip Flops under Process Variation and Aging

Maike Taddiken, Steffen Paul and Dagmar Peters-Drolshagen
University of Bremen, Germany

This paper analyzes the combined effects of process variation and aging, namely HCI and BTI, on the performance of Flip-Flops. To enable this evaluation, a stochastic reliability simulation flow which combines Monte Carlo simulations with degradation is presented. It makes use of a charged-based degradation aware transistor model incorporating both process variation and aging effects into a normal Spice simulation without the need of an additional aging simulator. The simulation flow enables the continuous evaluation of the changing stress conditions while keeping the simulation effort at a reasonable level. The analysis is performed on two different flip-flop architectures, a master slave flip-flop and a pulsed flip-flop, to determine the shift of timing performance distributions over time as well as the dependence on temperature.

11:00 Modeling the Dependencies between Circuit and Technology Parameters for Sensitivity Analysis using Machine Learning Techniques

Elena-Diana Şandru[1], Corneliu Burileanu[1], David Emilian[2], Andi Buzo[2] and Georg Pelz[2]
[1]University Politehnica of Bucharest, Romania [2]Infineon Technologies, Germany

The sensitivity of integrated circuit parameters regarding manufacturing process variation represents a very important ongoing topic in the semiconductor industry. Establishing the functional relationship between them at an early stage, i.e. simulation, would create an advantage in terms of circuit improvement and eventually high production yield. This paper presents a methodology for finding the influence of technology parameters (i.e. Process Control Monitor parameters) on device performance. The methodology is based on Machine Learning algorithms and Bayesian Optimization framework with the purpose of modelling the functional dependencies between technology and circuit parameters. The experimental results prove that the device performance is highly sensitive to technology parameters variation and this dependency can be modelled.

11:20 An IC Array for the Statistical Characterization of Time-Dependent Variability of Basic Circuit Blocks

Pablo Martín Lloret[1], Juan Núñez[1], Elisenda Roca[1], Rafael Castro Lopez[1], Javier Martin Martinez[2], Rosana Rodriguez[2], Montserrat Nafria[2] and Francisco Fernandez[1]
[1]IMSE-CNM (CSIC/Universidad de Sevilla), Spain [2]Universitat Autònoma de Barcelona (UAB), Spain

This paper presents an integrated circuit (IC) array whose purpose is to observe, quantify and characterize the impact of time-dependent variability effects, like aging, in several widely used digital and analog circuit blocks. With the increasing interest that this kind of mechanism has attracted in the last years, for its potential impact in the reliability of ultra-scaled integrated circuits, it is only relevant that appropriate measures are taken to find out how it can be included (and thus mitigated) in the design process of such integrated circuits. And, while substantial literature exists that covers the device level, time-dependent variability at circuit level has not been as equally studied. This work complements our previous efforts in providing a holistic approach to Reliability-Aware Design: from statistical characterization and modeling at device-level, to simulation, and into optimization-based design with reliability considerations, the array presented here provides one more step towards a thorough and accurate understanding of how time-dependent variability works at the circuit level.

11:40 Post-Silicon Validation of Yield-Aware Analog Circuit Synthesis

Engin Afacan[1], Gönenç Berkol[2] and Gunhan Dundar[3]
[1]Kocaeli University, Turkey [2]Eindhoven University of Technology, Netherlands [3]Bogazici University, Turkey

Analog/RF circuit design automation tools have become more popular in recent years. Conventionally, evolutionary algorithms are employed during circuit sizing and layout generation processes; thus, time to design can be considerably reduced. Furthermore, yield-aware analog circuit design automation tools have been developed by integrating variability analysis with the optimization. Previous works have mostly focused on improving the efficiency of optimization tools without sacrificing the accuracy. However, the accuracy of design automation tools is still argumentative since they are validated either at the pre- or post- layout level. But, in practice, post-silicon measurement is mandatory in order to verify the robustness of synthesis tools. To our best knowledge, there is no implementation and verification of yield-aware circuit sizing tools in the literature. In this study, a yield-aware circuit sizing tool is validated on silicon. For that purpose, two different OTA circuits were optimized using a yield-aware circuit sizing tool, a test chip was designed, tapedout, characterized, and results were compared with the results generated by the optimizer.

Thursday Afternoon, July 18th

PRIME Technical Session
Modeling, Optimization and Characterization **Thursday, 14:00-15:40** *Room CO 123*
Chair: Catherine Dehollain, *École polytechnique fédérale de Lausanne, Switzerland*

14:00 Performance Parameters Modeling and Simulation of Single-Photon Avalanche Diodes for Space LIDAR Applications.

Aymeric Panglosse[1], Philippe Martin-Gonthier[1], Olivier Marcelot[1], Cédric Virmontois[2], Olivier Saint-Pé[3] and Pierre Magnan[1]
[1]ISAE-SUPAERO, France [2]CNES - French government space agencie, France [3]AIRBUS Defense & Space, France

In this paper, we present a model to simulate accurately two main performance parameters of Single-Photon Avalanche Diodes (SPAD) in Complementary Metal-Oxide Semiconductor (CMOS) technology, the Photon-Detection-Probabilty (PDP) and the Dark-Count-Rate (DCR). The model development has been driven by the necessity to comply with the specifications of SPAD used for future space LIDAR applications. To evaluate these statistical parameters, the model is based on a combination of measurements to acquire data related to trap population, Technology CAD (TCAD) simulations and a Matlab routine.

14:20 Equivalent circuit extraction procedure from Nyquist plots for graphene-silicon solar cells

Ilaria Matacena
University of Naples Federico II Napoli, Italy

In this paper an automatic procedure to extract the equivalent circuit from impedance spectroscopy data is reported. The presented procedure is most suited for multilayer structures and has the advantage to cross the information deriving from impedance spectroscopy data, represented in the form of Nyquist plot, with C-V experimental data, adding physical constraints to the extracting procedure. Numerical and experimental tests have been performed on graphene-silicon solar cells, exhibiting good results.

14:40 Visualizations for Understanding SoC Behaviour

Dave McEwan[1], Marcin Hlond[2] and Jose Nunez-Yanez[1]
[1]University of Bristol, United Kingdom [2]UltraSoC Technologies Ltd, United Kingdom

This paper introduces a novel method of analysis for System-on-Chip (SoC) development building upon commonly used tools and techniques to approximate and automate the human process of investigation. Knowledge of the interactions between components within a SoC is essential for understanding how a system works so the presented method provides a way of visualizing these interactions. The mathematical basis for the method is explained and justified, then the method is demonstrated using two representative case studies. Visualizations from the case studies are used to exhibit the usefulness of the method for system optimization, monitoring, and validation.

15:00 System-Level Assessment of Dynamic Effects in GaN-based Power Converters

Andrea Minetto[1], Bernd Deutschmann[2], Oliver Häberlen[1] and Gilberto Curatola[1]
[1]Infineon Technologies Austria AG, Austria [2]Institute of Electronics, Graz University of Technology, Austria

Gallium nitride shows huge potential in power electronics applications. Nevertheless its implementation is still hindered by reliability issues and technology-related dynamic effects. A direct comprehension of their behavior in the final application is still missing. Hence, the goal of this work is to propose a novel methodology to analyse the role of these phenomena on the end application efficiency. These insights can thus lead to a system-level driven optimization of GaN technology. We propose a method based on T-CAD mixed-mode simulation and we give an example of its implementation in the analysis of a class-E power amplifier for wireless power transfer. Efficiency curve is extracted for different load resistance values. This is carried out for the device both in relaxed and in stressed conditions to evaluate the impact of buffer traps. It is demonstrated how the main degradation resides in the increased dynamic resistance while threshold voltage shift and output capacitance variations both play a minor role.

15:20 Minimum Energy Point in Constant Frequency Designs under Adaptive Supply Voltage and Body Bias Adjustment in 55nm DDC

Christoph Thomas Müller[1,2], Marc Pons[2], David Ruffieux[2], Jean-Luc Nagel[2], Stéphane Emery[2], Andreas Burg[1], Shuuji Tanahashi[3], Yoshitaka Tanaka[3] and Atsushi Takeuchi[3]
[1]EPFL, Switzerland [2]CSEM SA, Switzerland [3]Mie Fujitsu Semiconductor Limited , Japan

In this paper, we describe a systematic low-power design methodology for technologies that offer a strong body factor. Specifically, we explore both the body bias voltage and the supply voltage knobs in order to find the MEP (minimum energy point) for a constant target frequency. Our methodology accounts for process and temperature (PT) variations while charting the design space for a simple reference design. We then show how to scale the energy data of this

reference design to any arbitrary design. A case study of a 32bit RISC microprocessor achieves an energy estimation match of our significantly less complex estimation methodology within 1% of traditional signoff results.

PRIME Technical Session
MEMS and Piezoelectrical Sensors **Thursday, 14:00-15:40** *Room CO 123*
Chair: Patricia Desgreys, *University Paris-Saclay, France*

14:00 Perforated Paper-Based Piezoresistive Force Sensor

Yiğit Dağhan Gökdel, Kuter Erdil, Tuğçe Ayraç and Gökalp Akcan
İstanbul Bilgi University, Turkey

In this work, a paper-based disposable piezoresistive force sensor has been designed, fabricated and tested along with peripheral electronic circuit. Strathmore Bristol paper is employed as the substrate and it is coated with graphite and silver ink to form a perforated cantilever beam which constitutes the sensor part of the force sensing system. The proposed force sensing system can measure a force ranging to 24mN with a force resolution of 196μN. The implemented sensor has a sensitivity of 8.63mV/mN.

14:20 A feasibility study of AlN ultrasonic transducers fabrication using the multi-user PiezoMUMPs process for fingerprint scanning at GHz range

Jesus Yanez, Francesc Torres, Arantxa Uranga and Nuria Barniol
Universitat Autonoma de Barcelona, Spain

In this study, the feasibility of a piezoelectrical micromachined ultrasonic fingerprint sensor working at GHz range at CMOS-compatible voltage using the PiezoMUMPs process capabilities is explored analytically and through Finite Element Analysis. In addition to the advantages offered by ultrasonic fingerprint sensors based on MEMS technology, the all solid approach used here requires much lower driving voltage and provides higher operative frequency for improved axial resolution, overcoming some of the current limitations present in micromachined ultrasonic transducers. In this work we deal with the restrictions in the PiezoMUMPs process that arise due to the use of standard design rules that place constraints on the thicknesses, and materials that may be used, however, these inconveniences may be partially overcome by taking proper design considerations. Here we obtain output voltage in the mV range for an applied short pulse of 2 Vp at 1.6 GHz, showing the possibility to fabricate these piezoelectric micromachined ultrasonic transducers without requiring a customized process.

14:40 Design Considerations for a Digital Input MEMS Speaker Audio Amplifier with Energy Recovery

Markus Hänsler and Mario Auer
Graz University of Technology, Austria

The advances in MEMS technology offer now the possibility to manufacture loudspeakers, which need special drivers to achieve optimum performance. Driving capacitive loudspeakers (transducers) introduces a number of interesting challenges, which are addressed in this work. A digital amplifier, comparable to a class-D amplifier for electrodynamic loudspeakers is presented. The amplifier has a digital input and therefore also includes the A/D-conversion required for producing an analog output. In order to achieve a high efficiency the A/D-conversion is combined with a buck-boost converter and uses energy recovery to increase the efficiency. Using charge transfer efficient strategies for the design of such an amplifier will be given. The results are valid for capacitive loads in general and therefore useful for a wide range of problems, like MEMS drivers or switching control of power transistors. This article describes fundamental advantages of MEMS speaker based audio systems and the most important parameters for the required audio amplifier. A newly developed concept based on a non-inverting bidirectional buck boost converter will be used to derive the parameters as well as to explain the most important design criteria for an audio amplifier development for capacitive loads.

15:00 Mechanical Test Structures for the Determination of Normal Stress in Multilayer Freestanding MEMS-Membranes

Marvin Michel[1] and Holger Vogt[2]
[1]Fraunhofer, Germany [2]University Duisburg-Essen, Germany

Understanding the mechanical behavior of free standing membranes is a point of common interest for MEMS structures, where a certain distance or deflection of a cantilever or membrane refers directly to the detectors performance. A material system with different types of basic MEMS materials like doped silicon as well as a conducting and passivation layer was characterized. Mechanical stress was measured directly after deposition and at the freestanding membranes itself. It is found out, that the mechanical stress of the investigated material systems decreases up to two orders of magnitude due to relaxation between material deposition and releasing membranes from substrate.

15:20 Servo-Assisted Position-Feedback MEMS Inclinometer with Tunable Sensitivity

Alessandro Nastro, Marco Ferrari and Vittorio Ferrari

University of Brescia, Italy

A Micro Electro-Mechanical System (MEMS) inclinometer exploiting a double-actuator electrical servo-assisted position-feedback mechanism is presented. The mechanical position of the system is kept fixed thanks to a position-feedback loop that exploits a capacitive position sensor and two electrostatic force actuators. By adjusting specific loop parameters, the angle sensitivity can be finely tuned electrically. Experimental results show that the proposed system allows to tune the sensitivity up to 33.1 mV/deg. The obtained angle resolution, estimated at σ, is 40 mdeg. Allan deviation analysis for stability over time have been carried out, obtaining an optimal averaging cluster time of about 45 s.

SMACD Special Session *Room CO 124*

"Deep learning for analog EDA: Are we there yet?" **Thursday, 14:00-15:40**

Organizers/Chairs: Nuno Lourenço, *IT/IST, University of Lisbon, Portugal* and Mark Po-Hung Lin, *Department of Electrical Engineering, National Chung Cheng University, Taiwan*

14:00 Artificial Neural Networks as an Alternative for Automatic Analog IC Placement

Daniel Guerra, António Canelas, Ricardo Póvoa, Nuno Horta, Nuno Lourenço and Ricardo Martins

Instituto de Telecomunicações - Instituto Superior Técnico, Ulisboa, Portugal

In this paper, an exploratory research using artificial neural networks (ANNs) is conducted to automate the placement task of analog IC layout design. The proposed methodology abstracts the need to explicitly deal with topological constraints by learning reusable design patterns from validated legacy layout designs. The ANNs are trained on a dataset of an analog amplifier containing thousands of placement solutions for 12 different and conflicting layout styles/guidelines, and, used to output different placement alternatives, for sizing solutions outside the training set, at push-button speed. Ultimately, the methodology can offer the opportunity to reuse all the existent legacy layout information, either generated by layout designers or EDA tools.

14:20 Power to the Model: Generating Energy-Aware Mixed-Signal Models using Machine Learning

Martin Grabmann[1], Frank Feldhoff[2] and Georg Gläser[1]

[1]IMMS, GmbH, Germany [2]Department of Advanced Electromagnetics, Ilmenau University of Technology, Germany

Power consumption is a major concern in todays System-on-Chip (SoC) design and verification. While functional verification on system-level has recently be pushed to higher levels of abstraction using behavioral models, verifying power consumption still relies on time-consuming low-level simulations. The reason is that manually written models of Analog/Mixed- Signal (AMS) blocks and IP cores usually do not include transient power information because of the complex dependency that has to be captured for modeling it. This contribution presents a novel methodology for augmenting purely functional models of AMS blocks with information about their transient power consumption without manual interaction. This is realized through machine learning from simulations of the corresponding transistor-level representation. A feed forward time delay neural network (TDNN) is trained and afterwards automatically translated into a behavioral modeling language that is compatible to industrial circuit simulators. The applicability of our approach is presented in a case study.

14:40 Artificial Neural Network Assisted Analog IC Sizing Tool

Gamze İslamoğlu, Tuğberk Oğulcan Çakıcı, Engin Afacan and Gunhan Dundar

Bogazici University, Turkey

Some recent analog CAD tools include simulationbased circuit synthesizers that use evolutionary algorithms to find optimal circuit sizes. One important problem is the long execution time due to high number of simulations. This paper suggests the use of neural networks to determine circuit performance instead of simulations, which reduces execution time significantly. In our simulation-based circuit synthesizer, the data produced by preceding generations are not discarded as in conventional algorithms; they are used to train artificial neural networks inside the optimization loop. The simulator is then replaced by neural networks to estimate performance parameters. Up to 64.8% reduction in execution time was obtained with the proposed method.

15:00 Using Polynomial Regression and Artificial Neural Networks for Reusable Analog IC Sizing

Nuno Lourenço[1], Engin Afacan[2], Ricardo Martins[1], Fabio Passos[1,3], António Canelas[1], Ricardo Póvoa[1], Nuno Horta[1] and Gunhan Dundar[4]

[1]Instituto de Telecomunicações IST/UL, Portugal [2]Kocaeli University, Turkey [3]Instituto de Microelectronica de Sevilla, CNM, CSIC and Universidad de Sevilla [4]Bogazici University, Turkey

In this paper, the use of machine learning techniques to repurpose already available Pareto optimal fronts of analog integrated circuit blocks for new contexts (loads, supply voltage, etc.) is explored. Data from previously sized circuits is used to train models that predict both circuit performance under the new context and the corresponding device sizes. A two-model chain is proposed, where, in the first layer, a multivariate polynomial regression estimates the performance tradeoffs. The output of this performance model is then used as input of an artificial neural network that predicts the device sizing that corresponds to that performance. Moreover, the models are trained with optimized

sizing solutions, leading almost instantly to predicted solutions that are near optimal for the new context. The proposed methodology was integrated into a new framework and tested against a real circuit topology, with promising results. The model was able to predict wider and, in some cases, better, performance tradeoff, when compared to independent optimization runs for the same context, despite requiring 400 times fewer circuit simulations.

15:20 Efficient generation of data sets for one-shot statistical calibration of RF/mm-wave circuits

Florent Cilici[1], Gildas Leger[2], Manuel Barragan[1], Salvador Mir[1], Estelle Lauga-Larroze[3] and Sylvain Bourdel[3]
[1]TIMA Laboratory, France [2]Instituto de Microelectronica de Sevilla (IMSE-CNM-CSIC), Spain [3]RFICLab, France

Millimeter-wave circuits in current nanometric technologies are especially sensitive to process variations, which can seriously degrade the device behavior and reduce fabrication yield. To tackle this issue, conservative designs and large design margins are widely used solutions. Another approach consists in introducing variable elements, also called tuning knobs, to allow post-fabrication tuning. One-shot statistical calibration techniques take advantage of advanced machine learning regression tools to propose a set of tuning knobs values that enhance the circuit performance based on simple measurements. Training the regression models require a huge amount of data covering the device performances, the effect of the tuning knobs and the simple measurements that guide the regression. In this work, we propose an efficient method for generating such a data set that reduces noticeably the size of the required training set for an accurate calibration.

SMACD Technical Session
System-level methodologies — Thursday, 14:00-15:40 — *Room CO 016*
Chair: Shahed Reza, *Sandia National Laboratories, United States*

14:00 Noise leakage suppression in VCO-based ΣΔ-modulators excited by modulated signals

Dries Peumans, Piet Bronders and Gerd Vandersteen
Vrije Universiteit Brussel, Belgium

Oversampling data converters, such as the Sigma-Delta modulator, are widely used for analog-to-digital conversion. Proper evaluation of the in-band noise densities and the corresponding effective number of bits requires a post-processing step to adequately suppress the noise leakage. This suppression is traditionally achieved by windowing the digital output signal. Although windowing is effective for sinusoidal excitations, it is less optimal for the analysis of modulated signals. We propose a technique that not only accurately derives the in-band noise densities for these modulated signals, but also provides a measure for the in-band nonlinear distortions generated by the modulator. The performance of the technique is demonstrated on a Sigma-Delta modulator employing a voltage controlled oscillator for the internal quantiser.

14:20 Symbolic Top-down Design Methodology of a Quadrature Bandpass Delta Sigma Modulator

Oner Hanay and Renato Negra
RWTH Aachen University, Germany

This paper introduces a systematic top down design methodology for quadrature delta sigma modulators. The symbolic analyses of the modulator enables a systematic and mathematical design flow. Two different 3rd order feed-forward quadrature delta sigma modulators with a 3-level quantization are implemented. Where one is optimized to deliver best SNR in the signal band and the other designed to cancel signal and noise power at the image frequency. The calculated performance of the modulators in verified by a FPGA-based implementation and spectrum measurements. Both modulators are implemented on a FPGA. The measurements show great accuracy of the proposed design flow delivering \SI{60}{dB} and \SI{46}{dB} SNR in the passband. Furthermore, the symbolic design flow is used to calculate the effect of the quantization and mismatch of the coefficients which is conventionally done by time-consuming transient simulations.

14:40 PLL Real Number Modeling in SystemVerilog

Mina Louis, Mohamed Dessouky and Ashraf Salem
Mentor, A Siemens Business, Egypt

This paper discusses different techniques for the development of event-driven, analog functional models based on SystemVerilog for system-level verification. It leverages the recent introduction of additional real number capabilities in SystemVerilog to represent analog signals, known by Real Number Modeling (RNM). In addition to the introduction of composite user-defined net types that can carry multiple information, e.g. voltage, current, impedance, …. A Phase Locked Loop (PLL) model is considered as a vehicle to demonstrate the different proposed techniques. It is shown that using a pure SystemVerilog model, it is possible to achieve a comparable accuracy to Spice transistor-level simulation with a 27x simulation speedup.

15:00 Architectural Analysis of a Novel Closed-Loop VCO-Based 1-1 Sturdy MASH Sensor-to-Digital Converter

Elisa Sacco[1], Johan Vergauwen[2] and Georges Gielen[1]
[1]Katholieke Universiteit Leuven, Belgium [2]Melexis, Belgium

This paper presents the architectural concept and analysis of a novel VCO-based highly-digital closed-loop system employing a single VCO, which can achieve second-order quantization noise shaping thanks to the use of a second loop in 1-1 SMASH configuration, while still ensuring high linearity thanks to the feedback loop. The architecture improves upon the VCO-based closed-loop system, which only achieves inherent first-order noise shaping. The basic operating principle of the architecture is described at system level. Based on frequency-domain models, a theoretical analysis is presented, which derives the STF and the NTF for both architectures. State-variable-based simulation results are presented, which confirm the theoretical analysis and the SQNR improvement of the new architecture.

15:20 Modeling Power Supply Noise Effects for System-Level Simulation of ΔΣ -ADCs

Jonas Meier[1], Fabian Speicher[2], Christoph Beyerstedt[2], Tobias Saalfeld[1], Gregor Boronowsky[1], Ralf Wunderlich[1] and Stefan Heinen[1]
[1]IAS RWTH Aachen University, Germany [2]RWTH Aachen University, Germany

With the increasing integration density in modern designs new scenarios such as coupling and noise propagation need to be considered in top-level chip verification. Current state-of-the-art AMS simulation tools are not powerful enough for this task. Therefore an event-driven modeling approach using SystemVerilog and C++ is used to efficiently describe noise propagation through power supply in RF systems. Signals are represented in the Fourier domain using time-varying phasors to describe RF signals as equivalent baseband and noise as a spectrum with multiple frequency components. A ΔΣ-ADC for wireless applications is used as an example to show the model building process and possible system-level investigations.

SMACD Posters

SMACD Poster Session *On exhibition at Level 0 Hall*
Chair: Pablo Saraza-Canflanca, *IMSE, CNM, CSIC and Universidad de Sevilla, Spain*

Spiral Generation And Its Implication On Automatic Bi-Terminal Devices Circuits Drawing

Cristian Onete[1] and Maria Cristina Onete[2]
[1]NXP Semiconductors, Netherlands [2]Universite de Limoges, France

In this paper we investigate the connections between the Cycle Laplacian, the Hamiltonicity and Spirals as an initial step of automatic passive circuit drawing. A comparison between the related algorithms is provided. The new insights are based on the cycle description of planar graphs associated to passive circuits, contrary to the usual approach based on their node description.

Simulation Comparision of Frequency Estimation Methods Applied for Power Control in Renewable Energy Systems

Dariusz Kania and Józef Borkowski
Wrocław University of Science and Technology, Poland

This paper presents the simulation comparison of two Interpolated DFT frequency estimation methods in the control of a renewable energy system. The first method uses four points of the spectrum in calculations and MSD (Maximum Sidelobe Decay) time windows and the second method uses three points of the spectrum and Generalized MSD time windows. Simulations were performed for a modeled pure grid signal as well as signal distorted by Additive White Gaussian Noise and harmonic components in a very short estimation time. Both methods are very fast but the more accurate is the second method. The accuracy in real measurement conditions is in the order of 10-4 Hz/Hz or 10-3 Hz/Hz depending on the signal quality.

A Reliable and Fast ANN Based Behavioral Modeling Approach for GaN HEMT

Ahmad Khusro[1], Saddam Husain[1], Mohammad Hashmi[2], Medet Auyenur[2] and Abdul Quaiyum Ansari[1]
[1]Jamia Millia Islamia University, India [2]Nazarbayev University, Kazakhstan

The paper proposes an accurate, fast and advanced neural network approach to model the small signal behavior of GaN High Electron Mobility Transistor (HEMT). The presented approach makes use of the nonlinear autoregressive series-parallel and parallel architectures to model a 2x200μm device for a broad frequency range of 1GHz - 18GHz. A comparison is drawn between the two architectures based on the training algorithm, accuracy, convergence rate and number of epochs. An excellent agreement is found between the measured S-parameters and the proposed model for the complete broad frequency range. The proposed model can be embedded into computer aided design tool for an accurate and expedited design process of RF/microwave circuits and systems.

Baseband Equivalent Modelling Approach for Analog Linear Transfer Functions in Event-driven Simulations

Christoph Beyerstedt[1], Fabian Speicher[1], Jonas Meier[2], Ralf Wunderlich[1] and Stefan Heinen[1]
[1]RWTH Aachen University, Germany [2]IAS RWTH Aachen University, Germany

This paper presents a novel approach for baseband equivalent modelling of linear transfer functions in an event-driven simulation environment. The filter model allows fast simulations of in-band frequency dependent effects in RF transceivers. Needed parameters are calculated during runtime and the filter model is therefore not fixed for one specific RF frequency. The modelling approach was implemented in a SystemVerilog/C++ environment. Influences of a bandpass in a low noise amplifier on the bit error rate of a 2.4GHz receiver could be shown in a system simulations.

Hard and Soft Constraints for Multi-objective Analog IC Sizing Optimization

Nuno Lourenço[1], Ricardo Martins[1], António Canelas[1], Ricardo Póvoa[1], Nuno Horta[1] and Emmanuel Moutaye[2]
[1]Instituto de Telecomunicações, Instituto Superior Técnico – Ulisbon, Portugal [2]Thales Alenia Space, France

In this paper, the constraint handling of NSGA-II is modified to accommodate for both soft and hard constraints, by introducing the concept of soft-feasible solutions. In this context, softfeasible solutions are design points that fail to meet the hard constraints (original target specifications) but meet the soft constraints (acceptable relaxation for some of the hard constraints). This soft and hard constraint is a Designer centric definition and responds to a real-world need, since not all constraints have the same relevance and it can be hard to predict reasonable values beforehand. More, since analog IC sizing optimization is done on highly constrained search spaces, the proposed methodology increases the capability for the NSGA-II to retain the meaningful soft-feasible elements to augment diversity when hard-feasibility is difficult to achieve. The proposed methodology was implemented and tested on two circuit topologies, showing improvements of up to 31% on the average dominated hypervolume NSGA-II for difficult but existent target specifications. Moreover, when the target specifications are set to values impossible to be met by the topology, the proposed technique can obtain meaningful performance tradeoffs over the soft-feasible solutions.

FPGA Based Modelling of an ADPLL Network

Conor Dooley[1], Elena Blokhina[1], Brian Mulkeen[1] and Dimitri Galayko[2]
[1]University College Dublin, Ireland [2]LIP6 Lab, Sorbonne Université, France

This paper introduces and compares the implementation of a number of FPGA based ADPLL network prototyping architectures. Comparison is then made between the expected performance and role of each method as a development tool.

Self-improvement of OPAmp parameters using Q-Learning

Nobukazu Takai, Masafumi Fukuda and Masahiro Saruta
Gunma University, Japan

Q-Learning is one of the best ways to find action in certain situations through trials and errors. In this paper, we propose a novel method that finds element values of OPAmp satisfying specifications of a target circuit using Q-learning. In the proposed method, the relationship between "element value" and "circuit characteristic" is learned by Q-learning. From simulation results, we confirmed that the computer itself learned circuit design procedure, and autonomous design became possible.