Program

SMACD 2021 and PRIME 2021

18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) and
16th Conference on PhD Research in Microelectronics and Electronics (PRIME)

19 – 22 July 2021 | Online Event

www.smacd-conference.org
www.prime-conference.org

Fully Virtual Conference

Organized by

VDE ITG · IMMS · TECHNISCHE UNIVERSITÄT ILMENAU · RWTH AACHEN UNIVERSITY · Erfurt LANDESHAUPTSTADT THÜRINGEN Tourismus & Marketing

Technically Co-sponsored by

IEEE · CEDA IEEE Council on Electronic Design Automation · CAS IEEE CIRCUITS AND SYSTEMS SOCIETY

VDE

Welcome Message of the General Chairs

Dear PRIME & SMACD community and friends,

A warm welcome to all participants of this year's virtual event!

We are happy to confirm that the postponed 2020 edition of the 18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) and the 16th Conference on PhD Research in Microelectronics and Electronics (PRIME 2021) will take place from July 19 - July 22, 2021, as a virtual conference.

During these special times we want to offer our participants and particularly our PhD students a platform for an intensive scientific and professional exchange as well as to network with experts from industry and academia. We feel responsible to give especially our PhD students the possibility for publishing and presenting their submitted outstanding papers.

As in the year preceding the COVID 19 crisis, the two conferences enjoy a superior response from academia, industry, and scientific institutions. 211 authors from 21 countries had submitted 72 papers for the SMACD conference, and for the PRIME conference there were 69 topic proposals from 237 authors from 19 countries, in each case mainly from Europe. About two-thirds convinced the reviewers in each case, ensuring a diverse range of topics over the four days.

As SMACD2021 and PRIME 2021 are collocated and jointly organized, we have formed these papers into two presentation tracks with 14 sessions in total on Tuesday, Wednesday, and Thursday afternoon. On Monday afternoon and Wednesday morning eight tutorials covering hot topics in electronics and EDA are provided by experts from academia and industry.

All papers presented at both conferences will be made accessible in the conference proceedings and in IEEEXplore. We would like to express our thanks to all authors for their outstanding submissions and their patience during these days. Also, we want to thank the members of the Program and Scientific Committees for their competent evaluation of the submissions assuring the technical quality of the conference.

Likewise, we like to extend our gratitude to all committee members and the local organizers in Erfurt for their careful preparation of the virtual event and the Session Chairs for leading the sessions. Finally, I would like to thank all participants for providing the whole content of this year's online edition of SMACD 2021 and PRIME 2021. We wish you many interesting and enthusiastically presentations and let the conference be once again a successful forum for the exchange and networking of experienced scientists, PhD students, and industry in microelectronic and electronics.

Best regards, take care and stay healthy.

Ralf Sommer, SMACD 2021 Conference Chairman and host of the event and
Stefan Heinen, PRIME 2021 Conference Chairman

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SMACD 2021

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For reasons of safety we have decided to organize the SMACD and PRIME Conferences 2021 as an online event.

This was not an easy decision. However, it gives us greater planning security and the certainty that the conference will take place in any case. This way the authors, speakers, exhibitors and all guests will get to keep their trusted platform for exchange and networking on current topics again in 2021.

We look forward having you join us virtually!

We cordially invite you to join us for the virtual SMACD and PRIME 2021 conference from July 19th until July 22nd, 2021

SMACD 2021

18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design

The 2021 edition of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) was originally planned in Erfurt, Germany, but will be held virtually, as a forum devoted to modeling, simulation and synthesis for Analog, Mixed-signal, RF (AMS/RF) and multi-domain (nanoelectronics, biological, MEMS, optoelectronics, etc.) integrated circuits and systems. Experiences with modeling, simulation and synthesis techniques including machine-learning and artificial intelligence in diverse application areas are also welcomed. Objective technologies include CMOS, beyond CMOS, and, More-than-Moore such as MEMS, power devices, sensors, passives, etc.

SMACD 2021 is Technically Co-sponsored by IEEE, IEEE CEDA and IEEE CAS. The conference proceedings will be submitted for inclusion in IEEExplore.

PRIME 2021

16th Conference on PhD Research in Microelectronics and Electronics

PRIME has been established over the recent years as an important conference where PhD students and post-docs with less than one year post-PhD experience can present their research results and network with experts from industry, academia and research. PRIME 2021 will feature conference program reflecting the wide spectrum of research topics in Microelectronics and Electronics, building bridges between various research fields. In addition to the technical sessions, opportunities for the conference attendees will be the keynote talks, workshops, social events and conference proceedings will be submitted for IEEExplore. PRIME 2021 is seeking original papers in the areas given on the Call for Papers.

General Informations

Registration Fees

Conference and Tutorials

Students* full registration (IEEE/VDE member)	70 EUR
Students* full registration (Non-Member)	100 EUR
Author Students* (IEEE/VDE member)	120 EUR
Author Students* (Non-Member)	140 EUR
Regular full registration (IEEE/VDE member)*	170 EUR
Regular full registration (Non-Member)	200 EUR
Tutorial only registration	50 EUR

The conference fee includes admission to all conference sessions, the tutorials, and the conference proceedings.

* The reduced fees are only valid with the indication of the member card number (for VDE Members) or upload of the member card copy (for other organisations) and for student the upload of the student card copy during the online registration form. In case of missing certification the non member fees will apply.

Online registration

Important notice on author registration

- Authors are required to register by 22 May 2021 to ensure their paper is inserted in the programme and the conference proceedings.
- If no author is registered by 22 May 2021, the paper will be removed from the programme.
- Author registration can only cover the presentation of max. 2 papers.
- Please mention your paper ID when you register for the conference.

Payment of Conference Fee

Payment for registration, including bank charges and processing fees, must be made in Euro. The conference fee has to be fully paid in advance by credit card. Your registration can only be confirmed if VDE-Conference Services has recorded receipt of your full payment.

Cancellation

In case of cancellation, provided that written notice has been given to VDE-Conference Services before June 15, 2021, the registration fee will be fully refunded less a handling fee of EURO 30.00. After June 15, 2021, no refund will be made. Proceedings will then be sent to the registrant after the conference.

Contact

For all questions regarding the conference participation, changes in your conference registration, and payment methods please contact the

VDE Conference Service:
E:Mail: vde-conferences@vde.com
Phone: +49 69 63 08 477.

Welcome to Erfurt

My name is Matthias Gose,
I have been on the streets as a tour guide for 23 years.

I invite you on Wednesday, July 21st, at 5pm (CEST) to a virtual live tour through my hometown: the flower, cathedral and Luther city of Erfurt.

Around 1300 years of history come to life on the walk. From the time when the first monks evangelized the Franconian Empire, to the heyday of knighthood when Barbarossa was emperor, to the student Martin Luther, who became a monk and priest in Erfurt, through the Swedish period under Gustav Adolph von Wasa in the 30 Years War to the conquest of the City by the Archbishop of Mainz.

Horticulture and industrialization during the Wilhelminian era led Erfurt to a second boom in the 19th century. With a lot of luck, Erfurt survived the age of extremes in order to blossom again in full splendor in the 21st century as the state capital of Thuringia under the sign of the BUGA 2021.

Conference Topics

SMACD 2021

Modeling
- Compact modeling
- Performance and behavioral modeling
- Power and thermal modeling
- Reliability and variability modeling
- Multi-domain modeling (fluidic, bio, chemical, optical, mechanical)
- EMC & analog signal integrity
- RF/microwave/mm-wave modeling
- Linear and non-linear model order reduction
- Circuit & system theory and application
- Automated model generation

Simulation, verification and test
- Behavioral simulation
- Numerical and symbolic simulation methods
- Simulation and estimation methods of variability and yield
- Analysis of reliability effects (aging, electromigration, stress...)
- High-frequency simulation techniques
- Multilevel simulation techniques
- Multi-domain simulation
- Formal and functional verification
- Functional safety
- ESD

Synthesis
- Multilevel design methodologies
- Synthesis methods of multi-domain circuit and systems
- Physical synthesis
- High-frequency circuit and system design
- Low-power and energy-aware design techniques
- Parasitic-aware synthesis
- Variability-aware & reliability-aware design
- Performance monitors & self-healing techniques
- Test and design-for-test methods
- Optimization methods applied to circuit and system design
- Procedural design automation

Applications of modeling, simulation and synthesis in:
- Automotive
- Bio-electronics
- Security
- Internet-of-things
- Communications
- Renewable systems
- Energy management
- Engineering education

PRIME 2021

- Micro/Nanoelectronics
- Semiconductors
- Analog/Digital Signal Processing
- Computer Aided Design
- Analog/Digital/Mixed/RF IC Design
- Integrated Power ICs
- Sensors/Systems and MEMS
- Semiconductor Memories
- RF, Microwave and mm-wave Circuits
- VLSI and SoC Applications
- Visual Signal Processing
- Energy Harvesting
- Automotive Electronics
- Flexible Electronics
- Technical Trends & Challenges
- Biomedical Electronics

BarCamp

Do you ...

... miss the creative vibe of conference socials?

... have cool ideas but nowhere to talk about them?

... have more questions than answers?

... want to think outside of the box?

Then join us at the BarCamp!

The Concept

What to bring:

- Discussion topics
- Active Participation

How it works:

- Pitch your topic in the scheduling session
- Show your interest by voting for topics
- Schedule your topic in the agenda (If you get votes for your pitch!)
- Get a 1h time slot for your discussion topic
- Document your findings
- Have fun!

The BarCamp is shaped by participants like you!

Starting points for good sessions

- Have more questions than answers
- Stimulate discussions and let the crowd help you
- Show max. 1 slide

How to be part of the BarCamp

Submit a topic proposal to:

- Blog/Twitter/Talk about the BarCamp
- Bring your colleagues

The sessions will be held in breakout rooms and a Miro-Board will be provided.

Disclaimer

Attending the BarCamp might lead to the following conditions:

1. You create new ideas or project proposals
2. You have more concepts for publications than reviewers can handle
3. You connect with more collaborators than you can remember their names

The organizers are not responsible for late complications of novel research ideas or project proposals.

We are looking forward to your participation!

Your BarCamp@SMACD team
Anton, Christoph, Georg and Gregor

Registration Conditions

- Participation is free of charge for registered participants of the conference.
- For BarCamp only participation a 50,– € fee will be charged.

BARCAMP

Overview / Monday, July 19th

09:20 Short Opening

10:00 *Startup Coffee*

10:20 **BarCamp Scheduling I** p. 12

12:00 *Lunch Break*

Tutorials

13:00
- **Design Meets EDA: Gaps and Counter-measures in Analog/Mixed-Signal IC Design** p. 12
  a tutorial by Benjamin Prautsch
- **Quantum Computing: A Circuit Perspective** p. 13
  a tutorial by Lotte Geck

14:20 *Coffee Break*

14:40
- **Modelling Power Supply Noise in RF SoCs** p. 13
  a tutorial by Jonas Meier
- **High-Performance Flexible and Printed Electronics** p. 14
  a tutorial by Abhishek Singh Dahiya, Dhayalan Shakthivel

16:00 *Coffee Break*

16:20
- **On-Time RFIC Development with Fast EM Simulation and Integrated Design Flow** p. 15
  a tutorial by Fadoua Gacim
- **Metastable states in ECL- and CML designs and their consideration by design of TDCs with picoseconds resolutions** p. 15
  a tutorial by Gerald Kell and Daniel Schulz

17:40 Networking

Overview / Tuesday, July 20th

08:40 Opening Session

09:00 **Plenary Talk by Marco Seeland, TU Ilmenau** p. 16
Machine Learning Introduction

10:00 *Coffee Break*

10:20 **BarCamp Scheduling II** p. 16

10:40 **BC1** p. 16 | **BC2** p. 16 | **BC3** p. 16 | **BC4** p. 16

11:20 *Break*

11:40 **BC1** | **BC2** | **BC3** | **BC4**

12:20 *Lunch Break*

SMACD Technical Sessions | **PRIME Technical Sessions**

13:00
- **A1:** Competition (1) p. 17
- **B1:** Analog Circuit and Systems engineering p. 18
- **C1:** Digital Circuits and Subsystems p. 19
- **D1:** RF Circuits and Systems (1) p. 20

14:20 *Coffee Break*

14:40
- **A2:** Machine Learning SS p. 21
- **B2:** Behavioral Analysis p. 21
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- **D2:** Biomedical Circuits (1) p. 23

15:40 *Coffee Break*

16:00
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- **C3:** Data Converters (2) p. 25
- **D3:** Biomedical Circuits (2) p. 26

17:00 Sponsors Pitch and Get Together p. 26

Overview / Wednesday, July 21st

Tutorials

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11:20	*Break*			
11:40	**BC1**	**BC2**	**BC3**	**BC4**
12:20	*Lunch Break*			
	SMACD Technical Sessions		**PRIME Technical Sessions**	
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14:20	*Coffee Break*			
14:40	**A5:** Device Modelling (1) p. 32	**B5:** Optimization Methods p. 32	**C5:** Sensing Circuits (1) p. 33	Recruiting / Networking p. 33
15:40	*Coffee Break*			
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11:20	*Break*			
11:40	**BC1**	**BC2**	**BC3**	**BC4**
12:20	*Lunch Break*			
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14:20	*Coffee Break*			
14:40	**A8:** Complex System Analysis (2) p. 41	**B8:** Device Modelling (2) p. 41	**C8:** Circuits for Clock Generation and Optimization p. 42	**D6:** Analog Circuits and Qubit Interfaces p. 43
16:00	*Coffee Break*			
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Monday, July 19th 09:20–14:20

09:20–10:00 **Short Opening**

10:00–10:20 Startup Coffee

10:20–12:00 **BarCamp Scheduling I** *(further information on page 9)*

12:00–13:00 Lunch Break

Tutorials

13:00 ***Tutorial 1: Design Meets EDA: Gaps and Countermeasures in Analog/Mixed-Signal IC Design***
Chair: Georg Gläser, IMMS GmbH, Germany

Benjamin Prautsch *[1]; Reimund Wittmann [2]; Frank Schenkel [3]; Johannes Koelsch, Christoph Grimm [4]; Gunter Strube [5]*

[1] Fraunhofer Iis/Eas, Dresden, Germany; [2] Imst Gmbh, Kamp-Lintfort, Germany; [3] Muneda Gmbh, Unterhaching, Germany; [4] Tu Kaiserslautern, Kaiserslautern, Germany; [5] Blu Business Development, Gröbenzell, Germany

Along the path from specification to silicon, the design of analog/mixed-signal chips comprises a variety of challenges. They are of technological, methodological, organizational, communicational, and business nature. Additionally, large gaps are to be managed among the individual challenges. Still up to now, approaches such as the “four eye principle” are used even in industrial practice in order to handle them. However, steadily increasing system complexity makes this an end-of-range model. Instead, EDA support gets more and more relevant in order to tackle both problem-specific and overarching design challenges. Based on the well-known V-model, the tutorial will discuss the current design approach and discusses systematic alternatives comprising EDA, tools, tool interfaces, and usability aspects. With this, the design challenges can be tackled in order to stick with the market needs and tight design schedules.

Benjamin Prautsch received the Diploma degree in electrical engineering from the Dresden University of Technology in 2013 and is with Fraunhofer IIS/EAS since then. His interests are generator-based analog design automation as well as efficient and robust analog design flows. Since 2018 he is heading the group Advanced Mixed-Signal Automation and is responsible for generator-based analog design automation, design efficiency, and reuse methods. In this function, he has been developing these topics in various national and European projects (e.g. things2do, PRIME, Productive4.0, and currently AnastASICA) and he was involved in industrial design projects.

14:20–14:40 Coffee Break

Monday, July 19th 13:00–16:00
Tutorials

13:00 ***Tutorial 2: Quantum Computing: A Circuit Perspective***
Chair: Stefan Heinen, RWTH Aachen University, Germany

Lotte Geck

Forschungszentrum Jülich; Central Institute of Engineering, Electronics and Analytics (Zea) Electronic Systems (Zea-2), Nano- und Microelectronic Systems Germany

Quantum computing is an up and coming topic with a lot of attention not only from the scientific community but also increasing interest from industry. First, this talk introduces the topic from an electrical engineering point of view and explains why the possible use cases of a quantum computer make it so popular.

The underlying goal of the tutorial is to explain the two main types of circuits associated with a quantum computer, quantum circuits and specific (classical) circuits. For that the basic processing unit of a quantum computer, the so called qubit, is introduced first. With the qubits understood, quantum circuits can be addressed next. Here, the focus will be especially on understanding how such a circuit is similar or different to a classical circuit. Besides quantum circuits also a lot of classical electronics are necessary to realize a quantum computer. This talk will give an overview of the different kinds of classical electronics in a quantum computer and what circuit architectures are used in varying potential quantum computer implementations.

Lotte Geck received a M. Sc. degree in Electrical Engineering from the RWTH Aachen University in 2015. Afterwards she joined the Electronic Systems Institute (ZEA-2) of Forschungszentrum Jülich to pursue a PhD. Focusing on scalable control electronics for gallium-arsenide based quantum computers lead to new and interesting challenges for integrated circuits. The explorations of the quantum-classical interface also included a steep learning curve in quantum mechanics and a research stay at TU Delft further broadened the horizon. Currently Lotte is working at the ZEA-2 as a postdoc with a focus on modeling quantum processor systems.

14:20–14:40 Coffee Break

14:40 ***Tutorial 3: Modelling Power Supply Noise in RF SoCs***
Chair: Stefan Heinen, RWTH Aachen University, Germany

Jonas Meier

Integrated Analog Circuits and Rf Systems Laboratory; Rwth Aachen University, Germany

Todays integrated circuits (IC) incorporate more and more components to save area and increase reliability of the overall System on Chip (SoC). Yet the integration of analog, digital and RF systems on the same die suffers from various problems, one being the unwanted cross coupling, e.g. over power supply lines. Switching noise from digital circuits or high power ouput drivers propagate over the supply net to sensitive analog circuits and subsequently degrade their performance. Thus, these effects have to be taken into consideration early during the design and verification of mixed-signal ICs.

The simulation of an entire system such as an RF chip is not feasible on the transistor-level due to the very high computation effort that would be necessary. Event-driven simulation, widely used in digital circuit design, support the needed circuits sizes, but, even with the introduction of real number modeling, lack support for efficient description of analog or RF signal properties.

This presentation introduces a flexible framework, utilizing SystemVerilog user-defined data type (UDT) and net (UDN) in conjunction with the direct programming interface (DPI) to C++ to add the missing functionality. It is used to model a PLL testchip and investigate the influence of cross coupling through supply on the system performance.

Jonas Meier received the B.Sc. and M.Sc. degree in electrical engineering from RWTH Aachen University in 2013 and 2016, respectively, where he is currently working towards a Ph.D. degree in electrical engineering at the Chair of Integrated Analog Circuits and RF Systems. His research topic focuses on the integration and design methodologies needed for digital-centric RF Systems. His current research interests include advanced modeling and verification methods at chip-level for mixed-signal and RF systems as well as advances in PLL and transceiver designs.

16:00–16:20 Coffee Break

Tutorials

14:40 ***Tutorial 4: High-Performance Flexible and Printed Electronics***
Chair: Catherine Dehollain, EPFL, Switzerland

Abhishek S. Dahiya, Dhayalan Shakthivel, Yogeenth Kumaresan, Ravinder Dahiya [1]

[1] *Bendable Electronics & Sensing Technologies (Best) Group, James Watt School of Engineering, University of Glasgow*

The Printed Electronics (PE) devices and circuits are advantageous due to their ability to conform over different shapes and curvy surfaces which is needed for the advancement of numerous emerging applications including wearable systems, soft robotics, e-skin, bendable displays, and healthcare monitoring systems. This will also have an impact on the development of Internet of Things (IoT) concept where smart objects are required to be aware of and interactive with the unstructured environment. Additionally, PE systems are expected to revolutionise future electronics industry by providing cost-effective routes for processing diverse electronic materials at temperatures that are compatible with plastic substrates. Along with the flexible form factor, applications including IoT, smart healthcare etc. demands high device performance (fast data processing) leading to myriad machine-to-machine and/or human-to-machine connectivity at 5G communications. Accordingly, significant research efforts are on-going to manufacture electronic devices/systems with flexible form factor and high-performance. In this regard, printing of nanoscale inorganic structures have opened new avenues to achieve performances at par with silicon-based electronics.

In the first part of this tutorial, participants will gain an overview of various synthesis routes to obtain sub-100 nm inorganic semiconducting nanoscale materials (Nanowires (NWs), Nanoribbon (NRs) etc.) using bottom-up and top-down approaches. This includes wide variety of physical and chemical techniques such as metal assisted chemical etching (MACE), chemical vapour deposition (CVD) etc. The second part of this tutorial will bring together various printing techniques to integrate and assembly of grown nanoscale materials over flexible substrates. Potential capabilities and critical limitations of each printing technology will be highlighted, and possible solutions or alternatives will be discussed. The tutorial will also present some recent examples of high performance printed and flexible devices including transistors, sensors etc. using inorganic nanoscale materials.

Abhishek S. Dahiya is a research associate at the BEST group in the School of Engineering at University of Glasgow. He has received his Ph.D. from the GREMAN laboratory, Université François Rabelais de Tours, France in 2016. He performed his postdoctoral work at the GREMAN laboratory (2016-2017), the University of Bordeaux (ICMCB/CNRS) (2018-2019), and at the IES CNRS/Université de Montpellier (2019-2020) in France. He has published 28 high-impact research articles in leading journals and 1 US patent. His research interest covers synthesis of energy nanomaterials, nanofabrication, energy harvesting, printed and flexible electronics, and semiconductor device physics.

Dr. Dhayalan Shakthivel is a Researcher and ICURe entrepreneurial lead at the James Watt School of Engineering, University of Glasgow (UoG), UK. He has earned Ph.D in Materials Science, 2014, from the Indian Institute of Science (IISc), Bangalore. His research interests are growth and integration of semiconducting nanowires, kinetic studies of nanostructures growth, nanoscale crystal growth, Nano-pattering, electron microscopy, chemical vapour deposition (CVD) and nanowires based flexible electronics. He has developed kinetic models to probe key atomistic processes in the catalyst particle assisted growth of semiconducting NWs. His research works earned more than 35 publications in high impact journals, review articles, international conferences and 2 patents He has developed a non-chemistry specific automated CVD system for the growth of semiconducting nanostructures. His current research focused on semiconducting nanowires for flexible large area electronics towards the development of electronic-skin for robotics. He was a recipient of government of India-MHRD fellowship for Ph.D research. He received John Robertson Bequest award at the UoG.

16:00–16:20 Coffee Break

Monday, July 19th
Tutorials

16:20–17:40

16:20 ***Tutorial 5: On-Time RFIC Development with Fast EM Simulation and Integrated Design Flow***
Chair: Ralf Sommer, IMMS GmbH & TU Ilmenau, Germany

***Fadoua Gacim**; Anton Klotz*

Cadence Design Systems, Germany

In this tutorial, you'll see the new integration of the Cadence® EMX® Planar 3D Solver into the Electromagnetic Solver Assistant of the Cadence Virtuoso® Layout Suite EXL and how to leverage it in the RFIC design flow, with a power amplifier (PA) design as example. You'll learn how to perform fast and accurate EM analysis for selected passive components and nets in your design, while parasitic extraction for the rest of the design will be done in the Cadence Quantus™ Extraction Solution. Everything will be set up and driven from the Virtuoso Layout Suite EXL, keeping one golden schematic and one golden layout, without need of error-prone and time-consuming manual partitioning of the design into a block for parasitic extraction and a block for EM simulation. We will then demonstrate how to use the Cadence Spectre® X Simulator for post-layout simulation to predict accurate circuit performance.

Fadoua Gacim received a Ph.D degree from University of Caen-Normandie, France, in 2017 in collaboration with NXP semiconductors. She was in charge of modelling, characterization & optimization of substrate losses in IC design. She joined Cadence in 2018 and currently is Sr. Application engineer supporting Virtuoso-RF & Analog/mixed Signal Simulations.

17:40 Networking

16:20 ***Tutorial 6: Metastable states in ECL- and CML designs and their consideration by design of TDCs with picoseconds resolutions***
Chair: Georg Gläser, IMMS GmbH, Germany

Prof. Dr.-Ing. Gerald Kell, Daniel Schulz

Technische Hochschule Brandenburg; FB Informatik und Medien, Germany

The appearance of metastable states in flipflops by violations of setup- and hold times is a well known matter. In TDC circuits one cannot prevent metastabilities. In consequence, structural methods in practical designs, e.g. redundancies and multiple paths are required. Its real and practical function depends on the duration time of the metastabilities. There are some reasons that this durations are significantly less in SiGe- based ECL- and CML- structures in comparison to CMOS cells. In resume, we have characterized a lot of flipflop cells in the Common_ECL library to quantify the relevant duration of the metastable states. In result, the assigned VHDL models will show where is a metastability located in the structural design. After the defined duration, the model will switch to a random generated '1' or '0' value. This modelling concept can be a helpful tool to design fast TDC structures.

Gerald Kell was born 1954 in Berlin. His scientific career began with study of Electronic Technology 1975 – 1979 at the Humboldt University in Berlin (HUB) with the graduation as Dipl.-Ing. for electronics. He was a Research Associate at HUB since 1979, degree with Doctoral thesis 1985: Analog-Digital-Conversion and Digital Signal Processing. His research at HUB continued with precision measurement projects in manned spacecraft (TES, TEGRA), short time measurements and opto-electronic systems. In 1996, he co-founded of the PicoQuant GmbH Berlin, an enterprise for opto-electronic research and development. He was appointment as Professor for Digital Systems at the Brandenburg University of Applied Sciences (THB) in 2000. Core areas in teaching and research are hardware design for data processing and computer architectures. Since 2005 design of ultra fast integrated circuits in SiGe- technology, leading projects for fast data processing, time-to-digital converters (TDC) and computer interfaces. From 2016 – 2019 he was THB's vice president for research and technology transfer Since march 2020 he is professor emeritus.

17:40 Networking

Tuesday, July 20th 08:40–12:20

08:40–09:00 **Opening Session**
Chairs: Ralf Sommer, IMMS GmbH & TU Ilmenau; Stefan Heinen, RWTH Aachen University, Germany

09:00–10:00 ***Plenary Talk***
Chairs: Ralf Sommer, IMMS GmbH & TU Ilmenau, Germany

Machine Learning for the Design and Characterization of Microelectronic Systems

Marco Seeland
Ilmenau University of Technology, Software Engineering for Safety-Critical Systems, Department of Computer Science and Automation, Ilmenau, Germany

The design and characterization of microelectronic systems are substantially driven by experience and knowledge of design and test engineers. For the most part, such knowledge can neither be formally mapped nor used by methods of automation. Therefore, suboptimal solutions in complex analog or mixed analog / digital systems are often only recognized late. This causes additional effort ultimately resulting in high costs in design and validation of microelectronic systems after production. Meanwhile, machine learning algorithms achieved outstanding capabilities in areas such as natural language and image processing. Integrating learning algorithms into the design and characterization process of microelectronic structures, such techniques offer the potential for anomaly detection, data compression, and design optimization. The talk provides an overview on different application scenarios of using machine learning techniques for design and characterization of microelectronic systems. Learning models for the creation of behavioral predictions of system components, the automatic analysis of characterization data, and for anomaly detection in layout designs are discussed.

After receiving the M.Sc. degree in Technical Physics from the Technische Universität Ilmenau in 2012, and the Ph.D. degree in Physics in 2015, **Marco Seeland** fulfilled his long-standing passion and started as a postdoc researcher in the field of computer science. After joining the Software Engineering for Safety-critical Systems group at the Department of Computer Science and Automation, Technische Universität Ilmenau, he has been working in and leading several projects with a focus on data science and machine learning in different domains. His main research interest is development and application of neural networks for computer vision and pattern recognition in ecological bioinformatics to enable citizen science applications such as Flora Incognita.

10:00–10:20 Coffee Break

10:20–10:40 **BarCamp Scheduling II** *(further information on page 9)*

10:40–11:20 **BarCamp Sessions**			
BC1	**BC2**	**BC3**	**BC4**

11:20–11:40 Coffee Break

11:40–12:20 **BarCamp Sessions**			
BC1	**BC2**	**BC3**	**BC4**

12:20–13:00 Lunch

SMACD Technical Session *13:00-14:00*

A1 Competition (1)

Chair: Engin Afacan, Gebze Technical University, Turkey

A1.1 13:00

Trash or Treasure? Machine-learning based PCB layout anomaly detection with AnoPCB

Henning Franke [1], Paul Kucera [1], Julian Kuners [1], Tom Reinhold [2], Martin Grabmann [2], Patrick Mäder [1], Marco Seeland [2] and Georg Gläser [1]

[1] Technische Universität Ilmenau, Germany. [2] IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany

Designing PCBs requires experience and knowledgeabout bad designs, e.g. sensitive signals being influenced byaggressively switching ones in close proximity. Those interactionscan hardly be detected by formal checks and are usually treatedin review processes or by lengthy design iterations. An automatedway for identifying potentially harmful regions is still missing.This contribution introducesAnoPCB, a tool for automateddetection of such potentially harmful regions. Due to the lackof pre-classified data and tremendous potential for bad designchoices, AnoPCB is designed as unsupervised method and detectsdeviations from well-known design practices. In addition, wemade AnoPCB freely-available as plugin for the open-sourceKiCad PCB design environment. Instead of using top-downimagery, AnoPCB processes geometrical relationships and signalproperties in terms of layout slices containing category-basedsignal annotations. After training the anomaly detection on well-functional PCB layouts, our system is able to identify novel andpotentially anomalous design patterns in new PCB layouts. Wedemonstrate our approach using freely available PCB layoutsfrom the HackRF projects and showcase how novel designpatterns are detected by AnoPCB.

A1.2 13:20

A Deep Learning Toolbox for Analog Integrated Circuit Placement

António Gusmão [1,2], António Canelas [1], Nuno Horta [1,2], Nuno Lourenço [1] and Ricardo Martins [1]

[1] Instituto de Telecomunicações, Lisboa, Portugal.
[2] Instituto Superior Técnico – Universidade de Lisboa, Lisboa, Portugal

This paper presents a deep learning toolbox, DEEPPLACER, to assist designers during the layout design of analog integrated circuits. DEEPPLACER relies on a simple pair-wise device interaction circuit description, i.e., the circuits' topological constraints, to propose valid floorplan solutions for block-level structures, including topologies and deep technology nodes not used for its training, at push-button speed. Despite its automatic functionalities, the toolbox is focused on explainable artificial intelligence, involving the designer in the synthesis flow via filtering and editing options over the candidate floorplan solutions. This constant state of human-machine feedback environment turns the designer aware of the impact of each device's position change and inherent tradeoffs while suggesting subsequent moves, ultimately increasing the designers' productivity in this time-consuming and iterative task. Finally, DEEPPLACER is shown to instantly generate a floorplan with 61% better constraint fulfilment than a human designed solution.

A1.3 13:40

A Differential Evolution based Methodology for Parameter Extraction of Behavioral Models of Electronic Components

Gazmend Alia [1,2], Andi Buzo [1], Daniel Ludwig [1], Linus Maurer [2] and Georg Pelz [1]

[1] Infineon Technologies AG, Bundeswehr University Munich, Munich, Germany.
[2] Bundeswehr University Munich, Munich, Germany

Behavioral models of electronic components are crucial for system simulation, as they are quick to simulate and yet provide reliable information on the behavior of the original circuit. Parameter extraction of such models, i.e. calibrating the model to match the experimental characteristics of the device, is tedious work, as the number of such parameters can add up to tens of them. There are attempts in the literature to solve this problem with the help of optimization algorithms. However, when put to practice, new challenges arise due to the large number of devices to be calibrated, time restrictions and the wide variety of behavioral models. These challenges require novel techniques that ensure generality, speed and scalability. We address these challenges by proposing a fully automated flow, which includes the following novel features: an evolutionary algorithm, a smart sampling technique for reducing redundancy in the reference data, and a method for making use of the knowledge acquired in previous parameter extraction tasks. We tested the flow with a set of more than 200 Si-diodes and IGBT behavioral models with more than 50 parameters and 30 response curves to be calibrated. The results show that full automation of parameter extraction is possible, i.e. no human intervention is needed. Hundreds of Si-diodes and IGBT behavioral models are calibrated within 48 hours as compared to 1.5 years of manual work.

14:20–14:40 Coffee Break

SMACD Technical Session *13:00-14:20*

B1 Analog Circuit and System engineering

Chair: Helmut Graeb, Technical University of Munich, Germany

B1.1 13:00 Modeling and Optimization of Supply Sensitivity for a Time-Domain Temperature Sensor

Jun Tan, IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany

This paper presents a methodology for modeling and optimizing the supply sensitivity for a time-domain temperature sensor. Many modern System-on-Chip (SoC) designs integrate multiple functional blocks, such as sensors, power management units (PMU), and wired/wireless communication interfaces. Interference on the supply line between such blocks becomes critical, since it has a significant impact on sensor performance. Many state-of-the-art designs utilize supply sensitivity as a sensor parameter to describe the immunity to supply interference. Therefore, modeling and analysis of this parameter to optimize sensor performance are needed. This paper begins with the modeling of the common time-domain temperature sensor, while an instance of the model is precisely created with extracted parameters. Additionally, verification is performed by comparing the model with a transistor-level design. Finally, the optimization methodology for supply sensitivity improvement is discussed. The results show that the DC supply sensitivity is significantly reduced by a factor of 41. With the proposed methodologies, a further AC supply sensitivity can be analyzed and optimized, so that sensor performance in SoC designs can be improved.

B1.2 13:20 Noise behavior in current mirror circuit based on CNTFET and MOS Devices

Roberto Marani [1] and Anna Perri [2]

[1] National Research Council of Italy (CNR), Institute of Intelligent, Industrial Technologies and Systems for Advanced, Manufacturing (STIIMA), Bari, Italy. [2] Department of Electrical and Information Engineering, Electronic Devices Laboratory, Polytechnic University of Bari, Bari, Italy

In this paper we present a comparative analysis of noise performance of Carbon Nanotube Field Effect Transistors (CNTFETs) and MOSFET, through the design of a basic current mirror. For reference current of 1 µA and 10 µA the output static and dynamic characteristics are better in the case of CNTFET, but for all cases the output noise current is always higher for the CNTFET than for the MOS. The software used is Advanced Design System (ADS) which is compatible with the Verilog A programming language.

B1.3 13:40 A gm/ID Sizing Method for High-speed Multi-stage Operational Amplifiers with Feedforward-only Compensation

Qixu Xie, Guoyong Shi and Yaoyao Ye

Dept of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai, China

We present a gm/ID-based sizing method for multi stage operational amplifiers (Op Amps) with feedforward-only compensation. For this class of Op Amps, we have to take into account of the dominant parasitic capacitances in pole-zero analysis. The presented design method combines analytical design equations with the gm/ID tables to facilitate the calculation of the sizing parameters. To enhance the sizing accuracy, we propose to use a three-dimensional lookup table of gds/ID versus both gm/ID and VDS and the current-normalized parasitic capacitance lookup table, i.e., Cp,q/ID (p, q = D, G, S) versus gm/ID in sizing calculations. We verify by a case study that a high-speed three-stage Op Amp (attaining a GBW beyond 3 GHz) can be quickly sized using the TSMC 65nm CMOS technology.

B1.4 14:00 Hybrid Capacitor-less LDO with Switched-Mode Dead-Zone Control

Nellie Laleni, Andreas Tsiougkos and Vasilis Pavlidis

Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, Greece

A hybrid capacitor-less low-dropout regulator that includes switched-mode dead-zone control is proposed. Differently from the prior art, the combination of one digital and two analog low-dropout regulators effectively mitigates the oscillations of the output voltage within the dead-zone and reduces the overall power consumption. The digital part consists of an 1-bit comparator, shift registers and the PMOS array, and the analog part is constructed by an error amplifier and a pass transistor. In addition, an one-stage high gain amplifier without extra circuitry or an output capacitor is included ensuring that the hybrid LDO operates for load currents between 10 A - 10 mA, offering significant savings in area. The digital part is modeled using Verilog-A/AMS and the analog part and the output PMOS array of the digital part are designed using 180 nm X-fab CMOS technology.

14:20–14:40 Coffee Break

PRIME Technical Sessions ***13:00-14:20***

C1 Digital Circuits and Subsystems

Chair: Miguel Garcia-Bosque, University of Zaragoza, Spain

C1.1 13:00 Run-Time Adaptive Hardware Accelerator for Convolutional Neural Networks

Cristian Sestito [1], Fanny Spagnolo [1], Pasquale Corsonello [1] and Stefania Perri [2].

[1] Department of Informatics, Modeling, Electronics and System Engineering - University of Calabria, Italy.
[2] Department of Mechanical, Energy and Management Engineering - University of Calabria, Italy.

State-of-the-art Convolutional Neural Networks are characterized by heterogeneous convolutional layers to proper balance accuracy and computational complexity. Run-time adaptive convolution architectures able to process feature maps with kernels of various sizes and strides are highly desirable to achieve a favorable speed/power dissipation balance. This paper presents the design of an adaptive architecture able to manage efficiently convolutional layers with different running parameters. In order to guarantee high resources utilization for all the supported kernel sizes and strides, in contrast with existing competitors, the proposed design combines non-uniform basic blocks differently customized from each other. As a further nice characteristic, the hardware architecture here presented efficiently manages both odd and even kernel sizes, useful in models also requiring transposed convolutional layers. When accommodated within a Xilinx XC7Z045 FPGA SoC device, the proposed engine reaches a peak throughput of 217.2 GOPS and dissipates about 2.75 W at the 150 MHz clock frequency.

C1.2 13:20 Design and Analysis of a Leading One Detector-based Approximate Multiplier on FPGA

Salvatore Scarfone [1], Fabio Frustaci [1] and Stefania Perri [2].

[1] Department of Informatics, Modeling, Electronics and System Engineering - University of Calabria.
[2] Department of Mechanical, Energy and Management Engineering - University of Calabria.

In the context of error-tolerant applications, several approximate multipliers have been proposed to trade the energy consumption with the result accuracy. Unlikely, most of them are conceived for Application Specific Integrated Circuits and they can not be implemented on Field Programmable Gate Arrays due to their unique hardware structure. Among the others, the Leading One Detector-based approximate multipliers have attracted a lot of interest due to their efficiency. Nevertheless, a complete characterization of this kind of multipliers on Field Programmable Gate Arrays is still missing. This paper presents a thorough analysis of the approximate multiplier known as Dynamic Range Unbiased Multiplier when implemented on Field Programmable Gate Arrays, and it provides useful design guidelines to get the optimum energy-quality trade-off. Moreover, a simple approximation strategy is proposed to further increase the multiplier efficiency, leading to an energy reduction of up to 34% and a quality increase of up to 43% with respect to the conventional structure. Finally, the possibility of enhancing the referred approximate multiplier with a dynamically tuning of the energy-quality trade-off is analysed.

C1.3 13:40 Extending a RISC-V core with an AES hardware accelerator to meet IOT constraints

Anthony Zgheib, Olivier Potin, Jean-Baptiste Rigaud and Jean-Max Dutertre.

Mines Saint-Etienne, CEA-Tech, Centre CMP, F - 13541 Gardanne, France.

Internet of Things devices and applications are subject to strong constraints in terms of cost, code size and power consumption. This leads to difficulties in using resource-hungry encryption algorithms to ensure the confidentiality of the exchanged data. In this paper, we extend with a custom instruction the RISC-V open source Instruction Set Architecture (ISA) and integrate an Advanced Encryption Standard (AES) hardware accelerator to an IBEX RISC-V core. This is achieved for the sake of reducing its energy consumption, encryption time and code size with respect to purely AES software solutions. We consider a Field Programmable Gate Array implementation and ascertain its relevance for an Electrocardiography use case.

C1.4 14:00 Memristive Logic-In-Memory Implementations: A Comparison

Pietro Inglese, Elena Ioana Vatajelu and Giorgio Di Natale, TIMA Laboratory, France.

The technology evolution addresses the demand for faster computers. Despite the achieved speed-up in terms of memory and computation performances, the communication between the memories and the processor remains a bottleneck of today's computers. The Computation in Memory (CiM) paradigm aims at solving this problem by moving the computation directly inside the memory, eliminating thus the need for data transfer between memory and processor. Among the available CiM implementations, this study focuses on the Logic-in-Memory (LiM) solutions, i.e., digital operations to accelerate Boolean Logic. This work provides a comparison among the most prominent LiM solutions in terms of required memory resources (i.e., number of memristors) and number of operations.

14:20 – 14:40 Coffee Break

PRIME Technical Sessions ***13:00-14:20***

D1 RF Circuits and Systems (1)

Chair: Christopher Nardi, RWTH Aachen University, Germany

D1.1 13:00

A low-power 26.56-GHz LC-based DCO for multi-gigabit communication systems

Pablo Jiménez-Fernández [1], Óscar Guerra [1], Rocío Del Río [1], Alberto Rodríguez-Pérez [2] and Enrique Prefasi [2].

[1] Instituto de Microelectrónica de Sevilla, Spain. [2] KDPOF, Spain.

A voltage controlled oscillator (VCO) is one of the key building blocks in RF transceivers. By means of a Phase-Locked Loop (PLL) that controls the VCO, a clock signal at the desired frequency can be generated. Communications systems for multi-gigabit applications require high accuracy in the clock signal, so low phase noise of the VCO must be achieved. This paper presents the design of a 26.56-GHz digitally controlled VCO (DCO). The circuit is powered at 1.2 V and consumes 1.94 mW. Post-layout simulations based on a TSMC 65-nm CMOS RF process show a phase noise of -123.3 dBc/Hz at 10-MHz offset. By modelling the noise contributions of the digital PLL, a 242.84-fs rms jitter (integrated from 100 kHz to 100 MHz) has been estimated. The proposed DCO exhibits a FoM of -188.6 dBc/Hz at 1-MHz offset frequency.

D1.2 13:20

A Wide-Tuning-Range 55 GHz CMOS VCO on 22 nm FD-SOI Technology

Zoltán Tibenszky, Corrado Carta and Frank Ellinger.

Chair of Circuit Design and Network Theory, Technische Universität Dresden, Germany.

This paper presents the design and characterization of a low-power 55 GHz oscillator using complementary transistors. It has the highest continuous tuning range in its frequency band reported to date. The tuning range is 27.4 % and 30.8 % for supply voltages 0.8 V and 1.4 V, respectively. Its core and buffers consume in average 3 mW and 8 mW power, respectively, from a supply voltage of 1.2 V. The peak DC-to-RF efficiency is about 6 % for supply voltages above 1 V. The circuit was manufactured on a 22 nm FD-SOI CMOS technology, and requires a total silicon area of 0.012 mm2 .

D1.3 13:40

A Fully Integrated 28 GHz Class-J Doherty Power Amplifier in 130nm BiCMOS

Simone Veni [1], Michele Caruso [2], David Seebacher [2], Andrea Neviani [1] and Andrea Bevilacqua [1].

[1] University of Padova, Italy. [2] Infineon Technologies, Villach, Austria.

A SiGe BiCMOS Class-J Doherty power amplifier operating at 28 GHz is presented. The class-J operation is chosen to maximize the efficiency of the system without degradation in terms of bandwidth. A dynamic bias circuit is used to progressively turn on the auxiliary amplifier and improve the efficiency at back-off. Supplied by a 2.1 V supply, the power amplifier features a saturation power as high as 25 dBm, a peak power added efficiency equal to 25.5 %, and a gain equal to 13.6 dB. The PAE at the 6 dB power back-off (PBO) is 19.7 %.

D1.4 14:00

A Scalable CPW Circuit Model in Advanced CMOS Technologies for mm-Wave frequencies

Carla Moran Guizan [1], Peter Baumgartner [1] and Stefan Heinen [2].

[1] Intel Deutschland, Germany. [2] RWTH Aachen University, Germany.

This paper presents a physical circuit model for coplanar waveguide (CPW) transmission lines, scalable with line width and signal to ground spacing and suitable for circuit simulators such as SPICE. The circuit model components are fitted using EM simulation data, without the need to know materials and other stack up information that may be encrypted or hidden for the user. This is also helpful for complex layer stacks composed of many dielectric and conductive materials that are used in the latest CMOS technologies. The deviations of the transmission line main parameters, propagation constant and characteristic impedance, remain low for the mm-wave frequency band, from 20 GHz and up to 100 GHz. The scalability enables a fast circuit optimization.

14:20–14:40 Coffee Break

SMACD Technical Session *14:40-15:40*

A2 Machine Learning SS

Chair: Ralf Sommer, TU Ilmenau & IMMS GmbH, Germany

A2.1 14:40

Machine Learning in the Analog Circuit Simulation Loop

Petar Tzenov and Ahmed Sokar, Infineon Technologies AG, Neubiberg, Germany

This paper presents the software coupling of an analog circuit simulator (ACS) to a machine learning (ML) execution engine, in order to enable usage of ML models in circuit simulation context. This is achieved by interfacing Infineon's in-house simulator, TITAN, with the widely accepted machine learning framework TensorFlow (TF), via an easy to use Verilog-A API. Here we introduce the basic characteristics of this interface and present an application example for its usage in analog circuit behavioral modeling.

A2.2 15:00

Bringing Structure into Analog IC Placement with Relational Graph Convolutional Networks

António Gusmão [1,2], Nuno Horta [1,2], Nuno Lourenço [1] and Ricardo Martins [1]

[1] Instituto de Telecomunicações, Lisboa, Portugal.
[2] Instituto Superior Técnico – Universidade de Lisboa, Lisboa, Portugal

In this paper, disruptive research using modern embedding techniques and a deep learning (DL) model based on a relational graph convolutional network (R-GCN) encoder that automates the placement task of analog layout synthesis is conducted. The proposed methodology introduces structure in the input data, drastically reducing the total number of trainable parameters, leading to a smaller and more effective regression model. Moreover, its unsupervised training does not rely on expensive legacy layout data but only on sizing solutions. Experimental results show that the proposed R-GCN deep model generates placement solutions at push-button speed for multiple technology nodes and generalizes to circuit topologies not used in training. Moreover, the model outperforms other dense DL models while being 3000x smaller and producing solutions that compete with highly optimized analog designs.

A2.3 15:20

Machine Learning in Charge: Automated Behavioral Modeling of Charge Pump Circuits

Martin Grabmann [1], Christian Landrock [2] and Georg Gläser [1]

[1] IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany. 2X-FAB Global Services GmbH, Erfurt, Germany

Behavior models of Analog/Mixed-Signal (AMS) components are used in today's System-on-Chip (SoC) verification mainly for improving simulation speed. In addition, they can be used to enable verification scenarios including back-box intellectual properties (IP). Writing and maintaining such models is still time consuming and prevents widespread use. One class of essential building blocks are on-chip charge pumps (CP), which enable a variety of different features in SoCs e.g. embedded non-volatile memory solutions. This contribution presents a novel concept for automating the generation of grey-box behavior models of charge pump circuits using a Machine Learning (ML) approach. Compared to classical modeling approaches, it is not necessary to formulate an analytic description specific to the used circuit topology. The applicability of the approach is presented in a case study using a industrial charge pump design.

SMACD Technical Session *14:40-15:40*

B2 Behavioral Analysis

Chair: Georg Gläser, IMMS GmbH, Germany

B2.1 14:40

Verilog-A model development of a DC–DC boost controller with autonomous optimization

Davide Severin [1], Giovanni Capodivacca [1], Bernard Blaise Tchodjie Tchamabe [1], Andi Buzo [2] and Cristian-Vasile Diaconu [3]

[1] Infineon Technologies, Italy. [2] Infineon Technologies, Germany. [3] Infineon Technologies, Romania

Simulation time of wide schematic is often the root- cause of time-to-market worsening, especially during the design verification of large switchable circuit. To speed CPU-time up equivalent models can be used in place of the original modules, but they are often created for a specific project and requires a manual tuning of the specification. This contribution provides a methodology to develop Verilog-A equivalent models whose implementation is general, maintaining the physical coherence and parameterizing the internal properties. This large set of parameters is tuned with an autonomous Artificial Intelligence algorithm (GDE3) so that to achieve the required accuracy but reducing the human effort in optimization from some weeks down to a couple of days. The entire methodology has been applied to a DC–DC boost converter, decreasing the simulation time of an order of magnitude.

15:40 – 16:00 Coffee Break

B2.2 15:00
Analog Circuit Abstraction to SystemC-AMS Secured by Affine Forms
Ahmad Tarraf and Lars Hedrich
[1] *Institute for Computer Science, Goethe University Frankfurt, Germany*
Formal verification of analog circuits still suffers from a lot of challenges. The continuous nature of the variables along with the well-known state space explosion problem obstruct most verification approaches. Using behavioral abstraction, a circuit can be verified to some extent, however, the quality of the results is limited to the accuracy of the abstract model. To solve these problems, we propose an automated abstraction methodology that generates from transistor-level Spice netlists accurate models at the system level in SystemC-AMS. The models are deployed as hybrid automatons (HAs) with reduced complexities and linear system equations. Further, to compensate for modeling errors resulting from the abstraction technique, an extended version of the approach utilizes affine forms to generate models that produce bounded results during symbolic simulations.

B2.3 15:20
Simulating the impact of Random Telegraph Noise on integrated circuits
Pablo Saraza-Canflanca [1], Eros Camacho-Ruiz [1], Rafael Castro-Lopez [1], Elisenda Roca [1], Javier Martin-Martinez [2], Rosana Rodriguez [2], Montserrat Nafria [2] and Francisco Fernandez [1]
[1] *Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Sevilla, Spain.*
[2] *Electronic Engineering Department (REDEC) group, Universitat Autònoma de Barcelona (UAB) Barcelona, Spain*
This paper addresses the statistical simulation of integrated circuits affected by Random Telegraph Noise (RTN). For that, the statistical distributions of the parameters of a defectcentric model for RTN are experimentally determined from a purposely designed integrated circuit with CMOS transistor arrays. Then, these distribution functions are used in a statistical simulation methodology that, taking into account transistor sizes, biasing conditions and time, can assess the impact of RTN in the performance of an integrated circuit. Simulation results of a simple circuit are shown together with experimental measurements of a circuit with the same characteristics implemented in the same CMOS technology.

PRIME Technical Sessions ***14:40-15:40***

C2 **Data Converters (1)**
Chair: Alexander Meyer, RWTH Aachen University, Germany

C2.1 14:40
A 12-bit 100 MHz SAR ADC in 110-nm CMOS for MAPSs
Silvia Tedesco, INFN of Turin, Italy.
This paper presents a fully differential 12-bit SAR ADC developed for high-voltage CMOS sensors. The converter has been designed in compliance with low power consumption, high resolution and low material budget requirements. A merged capacitor switching method is employed to decrease power consumption and the capacitor array has been split up into two sub-DACs in order to reduce the area. The prototype has been implemented in a 110-nm CMOS technology. With a power supply of 1.2 V and a 100 MHz clock, simulations show an ENOB 9.87 of and a SFDR of 73.42 dB. The power consumption of the ADC is 513 uW while the Figure of Merit (FOM) results 54.8 fJ/conv-step. The final chip includes also a calibration engine to minimize the capacitor mismatch effect thus further improving the resolution.

C2.2 15:00
A Timing Skew Correction Technique in Time-Interleaved ADCs Based on a ΔΣ Digital-to-Time Converter
Gabriele Bè, Mario Mercandelli and Luca Bertulessi, Politecnico di Milano, Italy
This paper reviews state-of-the-art skew correction methods in time-interleaved (TI) analog-to-digital converters (ADCs) and introduces a novel mixed-signal skew correction technique based on dithering the control word of a digital-to-time converter (DTC), which significantly relaxes the stringent DTC resolution requirements. Simulation results of a 10 GS/s 8-bit 16-cores TI-ADC reveal that the proposed technique reduces the required DTC resolution by a factor of 4x and improves the spurious-free dynamic range (SFDR) by up to 10 dB with a negligible noise penalty.

C2.3 15:20
A low-noise high-speed comparator for a 12-bit 200-MSps SAR ADC in a 28-nm CMOS process
Luca Ricci, Luca Bertulessi and Andrea Bonfanti., Politecnico di Milano, Italy.
This paper presents a high-speed and low-noise comparator implemented in a 28-nm CMOS technology with a 0.9-V supply voltage. The comparator is designed for a 12-bit 200- MSps successive-approximation-register (SAR) analog-to-digital converter (ADC). Simulations show an input-referred noise of 163 uV and a reset-out delay of 110-ps for an input differential voltage of 100 uV. The energy per conversion is 595 fJ/conv and the Figure-of-Merit is 15.8 nJuV2, better than the state of the art.

15:40–16:00 Coffee Break

PRIME Technical Sessions ***14:40-15:40***

D2 Biomedical Circuits (1)

Chair: Catherine Dehollain, Ecole Polytechnique Federale de Lausanne, Switzerland

D2.1 14:40 A Sub-1µA Low-Power Low-Noise Amplifier with Tunable Gain and Bandwidth for EMG and EOG Biopotential Signals

Rafael Vieira [1], Ricardo Martins [1], Nuno Horta [1], Nuno Lourenço [1] and Ricardo Póvoa [1,2].

[1] Instituto de Telecomunicações, Lisboa, Portugal.

[2] Escola Superior Náutica Infante D. Henrique, Paço de Arcos, Portugal.

This paper presents the design of a low-power low noise amplifier for biomedical and healthcare applications of biopotential signals, focusing on electromyography (EMG) and electrooculography (EOG). The signals operate in different broad bands, yet follow an impulse shape transmission, being suitable to be applied and detected by the same receiver. The biopotential sensing amplifiers usually have a major impact in power and noise performance of an analog front end; hence the development of a low-noise amplifier with low-power consumption is of great importance. In this paper, the state-of-the-art amplifiers for biomedical applications are overviewed, and the proposed solution is presented. The proposed design has tunable cutoff frequency (FC) and gain, being adjustable for each type of signal. The circuit is designed in UMC 130 nm CMOS technology, supplied by 1.2 V, and consumes less than 1 µA. Post-layout simulation results show that, at the high FC of 2 kHz, the gain is 34 dB, presenting an input-referred noise of 1.476 µVrms corresponding to a noise efficiency factor (NEF) of 1.27. Whereas at the low FC of 20.91 Hz, the gain is 52.35 dB, the input-referred noise is 0.202 µVrms, and the NEF is 1.70.

D2.2 15:00 Transistor Downscaling toward Ultra-Low-Power, sub-100 µm^2 and sub-Hz Oscillators

Gian Luca Barbruni [1], Chiara Bielli [2], Danilo Demarchi [2] and Sandro Carrara [1].

[1] Ecole Polytechnique Federale de Lausanne, Switzerland. [2] Politecnico di Torino, Italy.

This paper analyses and discusses the feasibility of implementing sub-Hz range oscillators in ultra-low-power and ultra-miniaturised implants. The final aim is the Body Dust application, in which multiple freestanding smart cubes are wirelessly powered and freely to move in the human blood for bio-sensing purpose. That system requires an overall size smaller than 100 µm^2 and ultra-low power consumption. Two different CMOS technologies have been compared, analyzing the effect of transistor down-scaling in sub-Hz range oscillators. Four CMOS-based oscillators have been tested in both 0.18 µm and 28 nm technologies. The best result is the Schmitt Trigger-based timer implemented in FD-SOI 28 nm and combined with a ten stages frequency divider that oscillates at 122.5 mHz with a reduced area of 80 µm^2. The study demonstrate that the effect of transistor downscaling opens the possibility to reach a sub-Hz oscillator with both ultra-low-power and ultra-low-area consumption, so suitable for Body Dust application.

D2.3 15:20 Electronic solution to compensate the effects of the temperature and the humidity on the measurements of a capacitive sensor dedicated to an injection insulin pen

Sylvain Joly [1], Albrecht Lepple-Wienhues [1] and Catherine Dehollain [2].

[1] Valtronic Technologies, Switzerland. [2] Ecole Polytechnique Federale de Lausanne, Switzerland.

This article presents the climatic effects on a capacitive sensor device which measures drug volume inside an injection pen. The variations of the temperature and the humidity have a direct impact on the value of the capacitance. Therefore, experiments have been performed by modifying the temperature from 32°C to 22 °C at a constant relative humidity of 30%, inducing a variation of absolute humidity. The errors due to temperature and humidity induce a capacitance variation corresponding to a volume error of ~130µL That represents a dose error of 13 International Units (IU) of insulin. Two main approaches are presented in this paper. Firstly, the effect of water absorption is decreased by encapsulating the analog Printed Circuit Board (PCB). Secondly, reference electrodes are added to the system to correct the climatic variation by differential measurement. It will be shown that these two combined techniques have a beneficial effect on the measurements with a reduction of the error by 70%. The remaining error corresponds to a volume error of 40µL, equivalent to 4IU of insulin.

15:40–16:00 Coffee Break

Tuesday, July 20th 16:00–17:00

SMACD Technical Session *16:00-17:00*

A3 RF Systems (1)

Chair: Nuno Lourenço, Instituto de Telecomunicações, Portugal

A3.1 16:00

Frequency-Limited Reduction of RLCK Circuits via Second-Order Balanced Truncation

Olympia Axelou, Dimitrios Garyfallou and George Floros

Department of Electrical and Computer Engineering, University of Thessaly, Volos, Greece

Second-order formulation using susceptance elements has become very effective in modeling on-chip inductive couplings. Several prior works have proposed model order reduction techniques for RLCK circuits, mostly based on balanced truncation (BT) and moment matching, providing reduced-order models (ROMs) that can be simulated over the whole frequency range. However, in most applications, the ROMs are simulated only at specific frequency windows, which means that established methods usually provide models that may become unnecessarily large to achieve approximation over all frequencies. In this paper, we present a second-order frequency-limited approach for RLCK circuits, which may be combined with efficient low-rank Lyapunov solvers, leading to ROMs which are either smaller or exhibit better accuracy compared to an established second-order BT method. Experimental results on interconnect bus structures demonstrate the advantages of the proposed method.

A3.2 16:20

A Mixed Time-Frequency RF Simulation Technique Based on Numerical Time-Slot Partitioning

Jorge Oliveira [1,2]

[1] School of Technology and Management, Polytechnic of Leiria, Leiria, Portugal.
[2] Instituto de Telecomunicações, University of Aveiro, Aveiro, Portugal

The increasing complexity of RF architectures and the continuous push to profit from digital signal-processing techniques, have been addressing new challenges to circuit-level simulation. This paper describes the most relevant details of a time-frequency simulation technique specially conceived for the efficient numerical simulation of RF circuits whose stimuli are turned on and off for unknown periods of time, as is the case of RF circuits managing signals coded in some on-off digital scheme. The proposed technique is based on a time-slot partition stratagem with automatic switching between different numerical schemes (multitime envelope transient harmonic balance and time-step integration) along the simulation process, according to the on-off state of the circuits' stimuli. Simulation tests performed in an illustrative application example (a ASK/OOK transmitter used in low-power applications, as RFID or biomedical imaging) revealed significant gains in computational speed over commercial computer-aided design tools.

A3.3 16:40

Application of Asymmetric Crosstalk Harnessed Signaling on 3D Hexagonal Interconnect Arrays

Daniel Iparraguirre and José Delgado-Frías

[1] Intel Corporation, Hillsboro, OR, USA. [2] Washington State University, Pullman, WA, USA

This paper describes a novel application of the Asymmetric Crosstalk Harnessed Signaling (ACHS) on 3D routing environments, where interconnect wires are distributed across the two dimensions perpendicular to the routing direction. The ACHS scheme completely eliminates the common encoding mode that is part of the original CHS scheme. A fully 3D multi- stripline stackup containing a wiring bundle in a hexagonal wire arrangement is applied where channels are placed together. Simulation results, that include crosstalk and jitter effects, have shown a significant performance improvement of ACHS over the original CHS scheme.

17:00 Sponsors Pitch and Get Together

Tuesday, July 20th 16:00–17:00

SMACD Technical Session *16:00-17:00*

B3 Simulation Methods

Chair: Günhan Dündar, Bogazici University, Turkey

B3.1 16:00

Connecting Energy Storages from Tool Independent, Signal-flow Oriented FMUs

Meik Ehlert [1], Jan Michael [1], Christian Henke [1], Ansgar Trächtler [2], Matthias Kalla [3], Bakr Bagaber [3], Bernd Ponick [3] and Axel Mertens [3]

[1] Scientific Automation, Fraunhofer Institute for Mechatronic Systems, Design IEM, Paderborn, Germany.
[2] Heinz-Nixdorf-Institute, University of Paderborn, Paderborn, Germany.
[3] Institute for Drive Systems and Power Electronics, Leibniz Universität, Hannover

In cross-domain system simulation, models from a wide variety of tools are used. The FMI standard provides the possibility to connect these models as Functional Mockup Units. These so called FMUs have signal-flow oriented interfaces to each other. The interfaces can often be inconsistent due to missing knowledge of what kinds of energy storage are present in each model. The inconsistency leads to false simulation results. This article therefore presents design guidelines according to how energy storages can be distributed to different models of the electric drive technology. The goal here is to ensure correct numerical simulations. To validate these guidelines, a drive system is built from several FMUs and is compared against a topology-oriented reference.

B3.2 16:20

Adaptive Simulation with HDL Control Module for Frequency Converting Circuits

Zoltan Tibenszky, Martin Kreißig, Corrado Carta and Frank Ellinger

Technische Universität Dresden, Dresden, Germany

An adaptive simulator-independent method is presented, which reduces the simulation and post-processing time of transient simulations through the use of an intelligent sweep control implemented as a behavioural model. It is capable to effectively reduce the points to be simulated for determining the operation regions, or to find the local extrema of a continuous value performance parameter. It controls the variable sweeps based on real time simulation results, and delivers the circuit's performance parameters to be determined in a text file. This eliminates the often time consuming additional post-processing steps. The effectiveness of the proposed method is demonstrated for the case of a frequency divider verification, where it has led to a 10 times reduction in the simulation time, and eliminated any additional post-processing steps.

B3.3 16:40

Step Size Determination Approach for Aging Simulations in Analog Ics

Engin Afacan, Department of Electronics Engineering, Gebze Technical University

Simulation of time-dependent variations is quite complicated since the degradation is a function of time, where the time step directly affects the accuracy and the efficiency of the analysis. Commercial tools use a constant step count during simulations, in which choosing a large step count may degrade the efficiency whereas keeping it small may result in accuracy problems. To overcome this problem, a couple of different adaptive time-step approaches have been proposed in the literature. Nevertheless, they suffer from the initial workload during step count determination or some other accuracy problems. In this study, we present a two-level step count determination approach. At the first level, the step count induced estimation error can be promptly determined via an effective simulation strategy. At the second level, the error is fitted into a saturated power law model; thus, the efficient step count can be determined without any simulation effort. The proposed approach provides a remarkable save in computation time and can be used for all analog circuits without loss of generality.

PRIME Technical Sessions *16:00-16:40*

C3 Data Converters (2)

Chair: Alexander Meyer, RWTH Aachen University, Germany

C3.1 16:00

A 2GS/s 10-bit Time-Interleaved Capacitive DAC for Self-Interference-Cancellation Application

Mazyar Abedinkhan Eslami, Danilo Manstretta and Rinaldo Castello, Univerity of Pavia, Italy.

This article presents a 2-GS/s time-interleaved (TI) 10-bit capacitive digital-to-analog converter (CDAC) for self-interference-cancellation (SIC) application. There is option to test the design capable of working in TI or a single CDAC. By taking advantage low parasitic capacitance and equivalent parasitic capacitance at bottom and top plate of MIM capacitor, the split-capacitor technique is used without significant degradation in the linearity. The special architecture of the designed layout also relieves the local and radial oxide gradient error. The CDAC is designed in 28nm CMOS technology. If the CDAC works in stand-alone mode, followed by an additional anti-aliasing filter and the baseband input frequency equals 10.74 MHz, the ENOB, SFDR and THD at the output of the filter is equal to11.3-bit,76 dB and 76dB, respectively.

17:00 Sponsors Pitch and Get Together

C3.2 16:20 **Implementation of a Low Power Decimation Filter in a 180nm HV-CMOS Technology for a Neural Recording Front-End**

Markus Sporer, Nicolas Graber, Steffen Moll, Stefan Reich and Maurits Ortmanns, University of Ulm, Germany.

The design of decimation filters for Delta Sigma Converters is a rarely discussed topic though these filters are necessary for Delta Sigma modulator ADCs. In this work, we present a low-power decimation filter for a neural recording front-end. We show the applied design criteria and compare different filter structures to find the most efficient implementation. The decimation filter has been implemented and simulated in a 180 nm HV-CMOS process. It achieves a low power consumption of 6.4 µW at a supply voltage of 1.2 V. The filter has a 13 bit output running at a sampling rate of 22 kHz and requires an area of 460 µm x 210 µm. The input signal's SNDR degradation due to the filter is less than 2 dB.

PRIME Technical Sessions ***16:00-16:40***

D3 Biomedical Circuits (2)

Chair: Catherine Dehollain, Ecole Polytechnique Federale de Lausanne, Switzerland

D3.1 16:00 **A scalable spike detection method for implantable high-density multielectrode array**

Mattia Tambaro [1], Elia Arturo Vallicelli [2], Gerardo Saggese [3], Andrea La Gala [4], Marta Maschietto [1], Alessandro Leparulo [1], Antonio Strollo [3], Marcello De Matteis [4], Andrea Baschirotto [4] and Stefano Vassanelli [1].

[1] University of Padova, Italy. [2] INFN, Milan, Italy. [3] University of Naples "Federico II", Italy. [4] University of Milano - Bicocca, Italy.

High-density CMOS-based Multielectrode Arrays (MEA) provide thousands of channels to record extracellular electrical activity of neuronal networks. Such a high channels count generates an amount of data that is difficult to manage with long-term fully implantable neural interfaces, where power and data transmission are provided wirelessly. To overcome this limitation, a low resources digital signal processor able to reduce the amount of transmitted data to a relevant subset represented by the spiking activity is essential. Unfortunately, the resources required to detect spikes linearly grow with the number of channels, limiting the total amount of MEA pixels in these devices. This work presents a method, here called Spike Detection-by-Difference (SDD), to drastically reduce this limit, for real-time spike detection with an impact on resources and consumption independent from the total channels count. It exploits the high resolution of MEAs to separate the highly localized extracellular action potential from the large-scale local field potential. The SDD is compared with the standard spike detection approaches as the Threshold Crossing (TC) and the Nonlinear Energy Operator (NEO). The detection accuracy is compared for different spiking amplitudes on a synthetic dataset generated from real recordings, showing a detection accuracy of 90% for spikes as low as 45 µV, with a noise in the spikes frequency band from 300 Hz to 5 kHz of 10 µVrms. Furthermore, the resource consumption shows a reduction of the 91,5% respect to the TC and of 94% respect to the NEO on a 32x32 pixels matrix. This reduction can be further accentuated increasing the matrix size or reducing the number of columns.

D3.2 16:20 **Current-reuse Low-Power Single-Ended toDifferential LNA for Medical Ultrasound Imaging**

Olivia Mirea, Carsten Wulff and Trond Ytterdal.

NTNU: Norwegian University of Science and Technology, Trondheim, Norway.

We present a low power, low noise current-reuse fully differential OTA (Operational Transconductance Amplifier) -designed in 180 nm CMOS technology- having a very energy efficient architecture including a common-mode feedback which ensures the conversion from single-ended to differential with close to zero power - the power being used when the capacitors are reset, no power is consumed in active mode time, the amplifier being designed for an active time of 500 µs. The amplifier drives a capacitive load of 200 fF and achieves 50 µW, an input-referred noise of 20 nV/$\sqrt{\text{Hz}}$ and an input capacitance of 18 fF for a unity gain frequency (f_{ug}) of 280 MHz. Since this circuit can be designed for a large range of frequencies, we also investigate the way of optimizing a figure-of-merit (FOM).

17:00 Sponsors Pitch and Get Together

Wednesday, July 21st 08:40–10:00

Tutorials

08:40 ***Tutorial 7: Optimizing Neural Networks for embedded Hardware***
Chair: Georg Gläser, IMMS GmbH, Germany

Domenik Helms [2]*; Karl Amende* [3]*; Saqib Bukhari* [4]*; Thies Degraaff* [2]*; Alexander Frickenstein* [1]*; Frank Hafner* [4]*; Tobias Hirscher* [3]*; Sven Mantowsky* [4]*; Vijay Parsi* [4]*; Manoj-Rohit Vemparala* [1]

[1] *BMW Ag, Munich, Germany;* [2] *Offis E.v., Oldeburg, Germany;* [3] *Valeo, Kronach, Germany;* [4] *Zf Friedrichshafen Ag, Saarbrücken, Germany*

Neural networks are a pervasive technology, which is, however, still held back in the area of embedded systems by the high resource requirements, especially memory size, memory access time and power dissipation. In recent years, several different methods have been proposed to transform given neural networks in such a way that they can get by with much fewer resources while maintaining almost the same accuracy. This work reviews, categorizes and describes the state of the art in adapting and simplifying neural networks to make them better applicable to embedded systems. Even though we developed this study from a purely automotive context, the techniques described are also valid in other areas.

Domenik Helms works since 2001 in the area of embedded system's design automation. After focusing on non-functional aspects like power consumption, leakage currents and technology ageing of general embedded systems, he is now working on electronic design automation methods for non-functional aspects of embedded AI applications. His recent research interest is on optimization and estimation techniques for neural networks.

08:40 ***Tutorial 8: The essential role of procedural approaches in EDA***
Chair: Ralf Sommer, IMMS GmbH & TU Ilmenau, Germany

Dr.-Ing. Daniel Marolt*, Prof. Dr.-Ing. Jürgen Scheible*

Electronics & Drives, Department Electronic Design Automation; Reutlingen University, Germany

Electronic design automation approaches can be roughly divided into optimization algorithms and procedural approaches (aka generators). While the former have enabled a highly automated synthesis flow for digital ICs, the latter play a vital yet underestimated role in the analog domain. This paper introduces both automation strategies in comparison, thereby revealing two fundamentally different automation paradigms known as top-down and bottom-up automation. Then, with a focus on the latter, the history of procedural approaches is traced from their early beginnings until today's evolvements and future prospects to underline their practical importance and accentuate their scientific value, both in itself and in the overall context of EDA.

Daniel Marolt was born in Reutlingen, Germany, in 1984. He studied mechatronics at Reutlingen University, where he received the B.Eng. degree in 2008 and the M.Sc. degree in 2009. Since then, he has been working as an academic employee at the Robert Bosch Center for Power Electronics (rbz), receiving the Dr.-Ing. degree from the University of Stuttgart in 2018. He then stayed at the rbz, which is now named Electronics & Drives (E&D), currently acting as a research team leader. His research interest is focused on electronic design automation for full-custom analog circuit and layout design.

10:00–10:20 Coffee Break

Wednesday, July 21st 10:20–14:20

10:20–10:40 **BarCamp Scheduling II** *(further information on page 9)*

10:40–11:20 **BarCamp Sessions**

BC1	BC2	BC3	BC4

11:20–11:40 Coffee Break

11:40–12:20 **BarCamp Sessions**

BC1	BC2	BC3	BC4

12:20–13:00 Lunch

SMACD Technical Session ***13:00-13:40***

A4 Competition (2)
Chair: Engin Afacan, Gebze Technical University, Turkey

A4.1
13:00

Adaptive Test Bench Generation, Simulation and Parameter Extraction for AMS Circuitry

Alexander Meyer, Leon Weihs, Ralf Wunderlich and Stefan Heinen

Integrated Analog Circuits and RF Systems Laboratory, RWTH Aachen University, Aachen, Germany

This paper presents a novel semi-automatic test bench generation and parameter extraction workflow for analog-mixed signal circuitry. Specific test benches for a given circuit are automatically generated, simulated, and model parameters are extracted. By relying on a modular test bench structure, changes in the circuit's design or port list can be automatically considered, facilitating the overall verification process and avoiding errors during the parameter extraction phase. Hence, precise and pin-accurate models can be generated faster and more reliably. A first implementation of this workflow using Cadence's SKILL language is shown.

A4.2
13:20

Monitoring Analog Circuit Performance using Adaptive Filters and RSM-based Behavioral Models

Maike Taddiken, Steffen Paul and Dagmar Peters-Drolshagen

Institute of Electrodynamics and Microelectronics (ITEM.me), University of Bremen, Germany

This paper presents a concept for monitoring the performance of an analog circuit by using adaptive filters in combination with behavioral models. Digital calibration techniques based on adaptive filters are applied to monitor the circuit performance. The reference signal representing the ideal error-free circuit performance required by the filter is provided by a behavioral model based on Response Surface Modeling (RSM). Comparing the output signal of the circuit to the ideal reference signal results in a number of filter coefficients that are used to estimate the circuit performance. The shift of the filter coefficients over time is used to monitor the degradation of performance caused by aging. The monitoring approach is analyzed on a simulative basis with an amplifier in a 28nm process.

14:20–14:40 Coffee Break

SMACD Technical Session *13:00-14:20*

B4 Procedural design automation

Chair: Daniel Marolt, Reutlingen University, Germany

B4.1 13:00 Schematic Generation of Programmable Analog Neural Networks for Signal Proccessing

Florian Aul, Nikoletta Katsaouni, Lukas Krischker, Sascha Schmalhofer, Marcel H. Schulz and Lars Hedrich

[1] Institute for Computer Science, Goethe University Frankfurt, Germany.
[2] Institute for Cardiovascular Regeneration, Goethe University Frankfurt, Germany

This paper presents a methodology for generating analog neural networks (ANNs) from trained TensorFlow models using an intermediate description of the network. All needed circuitry and helper circuits are available in a block library provided for the operation in an energy efficient low power region. The weights of the ANN are programmable by the corresponding bitstream, which is also generated by the proposed approach. The feasibility of the approach is demonstrated with two examples, the larger being an ANN for arrhythmia detection of electrocardiograms (ECGs) with 2,570 neurons and 10,042 weights.

B4.2 13:20 Generators, Templates, and Code Generation for Flexible Automation of Array-Style Layouts

Benjamin Prautsch [1], Reimund Wittmann [2], Uwe Eichler [1], Uwe Hatnik [1] and Jens Lienig [3]

[1] Fraunhofer IIS/EAS, Institute for Integrated Circuits, Division Engineering of Adaptive Systems, Dresden, Germany.
[2] IMST GmbH, Kamp-Lintfort, Germany. [3] Dresden University of Technology, Dresden, Germany

The design of integrated circuits from the specification onward aims at the successful validation by silicon measurements. One key milestone in this process is the completion of the layout. This, however, can be very challenging as many iterations are usually necessary between schematic design and layout design due to parasitic effects. Thus, our work integrates declarative templates into procedural generator-based layout automation and incorporates automatic generator code creation from an input schematic. Using this flow, a schematic is translated into a reusable and executable design description, that allows automation of the layout with template-based flexibility and at generator-based execution speed. In addition, the template enables early and fast parasitic estimates. With our combined approach that is embedded into the design flow we contribute to analog layout automation by bridging the gap between generators and templates.

B4.3 13:40 Improvement of Simulation-Based Analog Circuit Sizing using Design-Space Transformation

Matthias Schweikardt and Jürgen Scheible

Electronics & Drives, Reutlingen University, Reutlingen, Germany

This paper presents an improvement in usability and reliability of simulation-based analog circuit sizing. Instead of using geometrical sizing parameters (width, length), a transformed design-space, consisting of electrical parameters (branch currents, efficiencies and speed) is utilized. This design-space is explored more efficiently by optimizers. Moreover, this design-space can be reduced without affecting the quality of the result. The method is illustrated on two application examples, a symmetrical and a miller operational amplifier. Sizing the circuits using the transformed design-space showed significant reduction in required circuit simulations (up to 11x faster), better convergence, without loss in quality.

B4.4 14:00 Machine Learning Based Procedural Circuit Sizing and DC Operating Point Prediction

Yannick Uhlmann [1], Michael Essich [2], Matthias Schweikardt [1], Jürgen Scheible [1] and Cristóbal Curio [2]

[1] Electronics & Drives, Reutlingen University, Reutlingen, Germany.
[2] Cognitive Systems, Reutlingen University, Reutlingen, Germany

This paper presents a machine learning powered, procedural sizing methodology based on pre-computed look-up tables containing operating point characteristics of primitive devices. Several Neural Networks are trained for 90 nm and 45 nm technologies, mapping different electrical parameters to the corresponding sizing of a primitive device. This moves the geometric sizing problem into the domain of circuit design experts, where the desired electrical characteristics are now inputs to the model. Analog building blocks or circuits are expressed as a sequence of function calls to these models, capturing the sizing strategy and intention of the designer in a procedural form, enabling reuse especially for technology migration. The methodology is applied to size two amplifiers and evaluated for two technology nodes, showing the versatility and efficiency of this approach.

14:20–14:40 Coffee Break

PRIME Technical Sessions *13:00-14:20*

C4 Automotive

Chair: Michael Hanhart, RWTH Aachen University, Germany

C4.1 13:00

Analog Baseband Filter and Variable-gain Amplifier for Automotive Radars in 22 nm FD-SOI CMOS

Andres Seidel [1], Songhui Li [1], Laszlo Szilagyi [1], Corrado Carta [1], Jens Wagner [1,2] and Frank Ellinger [1,2].

[1] Chair for Circuit Design and Network Theory, Technische Universität Dresden, Germany.
[2] CeTi, Center for Tactile Internet, Technische Universität Dresden, Germany.

This paper presents the design of an analog base- band for a 77 GHz automotive radar in 22 nm fully-depleted silicon on insulator (FD-SOI) CMOS. The baseband ranges from 0.13 MHz to 14 MHz and requires a steep low-pass filter to avoid aliasing. This is realized with an 8th order Butterworth low-pass filter. In order to achieve the specified gain requirements, a variable gain amplifier (VGA) with DC-offset cancellation is applied before the filter. Its dynamic range was maximized, the optimization strategy is presented. The performance of the baseband components was verified with laboratory measurements. The filter achieves a suppression of ≥ 35 dB at 28 MHz. A dynamic range of 45 dB and a maximum gain of 41 dB is measured for the VGA. In addition, a good agreement between simulation and measurement is obtained. With an area-optimized design of 0.032 mm², the baseband components are a fraction of the size compared to chains of similar radar systems.

C4.2 13:20

A Highly Linear High-Voltage Compliant Current Output Stage for Arbitrary Waveform Generation

Felix Schwarze, Florian Protze, Frank Ellinger and Christian Matthus.

Technische Universität Dresden, Germany.

In this paper, a highly linear high-voltage compliant current output stage is presented. The circuit enables the utilization of a conventional 8 bit low-voltage current-steering digital-to-analog converter in a high-voltage environment. Based on the improved active-feedback cascode current mirror topology, several adaptions were implemented to optimize the circuit towards high linearity and high bandwidth. The proposed circuit provides 167 MHz bandwidth, which to the authors' knowledge is the highest reported bandwidth for high-voltage compliant current mirrors. Moreover, with 0.49 LSB at 8 bit resolution it has, to the authors' knowledge, the highest reported linearity to date. Additionally, it is high-voltage compatible for output voltages of up to 60 V and provides the widest output current range of 10 mA maximum output current. At the same time, the power consumption of the utilized cascode control loop could be reduced by 92 % compared to the original topology.

C4.3 13:40

A RISC-V-based System on Chip for High-Speed Control in Safety-Critical 650 V GaN-Applications

Mike Richter [1], André Lüdecke [1], Yoon-Cue Lee [1], Alexander Stanitzki [1], Alexander Utz [1], Günter Grau [2], Holger Kappert [1] and Rainer Kokozinski [1].

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[2] advICo microelectronics GmbH, Recklinghausen, Germany.

In power electronics applications, Gallium Nitride (GaN)-based transistors generally offer benefits in efficiency and switching speed, but come at the cost of harder controllability and thus more complex control circuits. As a contribution towards easier and safer control for GaN-devices, we present a new system-on-chip (SoC) specifically dedicated to the control of GaN-based power modules. The main processing unit is compliant with the RISC-V specification and implements the RV32IMC instruction set. Major parts of a control algorithm may be performed by peripheral modules that reduce workload on the processor and enable low-latency reactions towards safety-critical events in the GaN-circuit. The output is generated by a PWM-unit that supports sub-nanosecond resolution. The processor achieves a benchmark score of 2.03 CoreMark per MHz. The SoC reacts to threshold violations on measurement inputs within 25 ns. Future steps will involve expanding the SoC with more safety features and the coupling of several SoCs for multiphase synchronization.

C4.4 14:00

An Approach to Online Wear Out Monitoring of PCB Interconnects in Safety-Critical Systems

Saeid Yazdani [1], Werner Wolz [1], Rainer Engelhardt [2], Christian Schott [1], Ulrich Heinkel [1] and Daniel Kriesten [3].

[1] TU Chemnitz, Germany. [2] Steinbeis GmbH, Chemnitz, Germany. [3] Hochschule Mittweida, Germany.

Online monitoring inside electronic control units (ECU) is mandatory for all safety-critical systems. Dedicated quality and safety monitoring structures will be described that support the early detection of health problems. Interconnect wear-out and delamination are major failure causes in printed circuit boards, and sensitive detector arrangements allow for the estimation of near-future fail situations. Countermeasures like pre-emptive service actions can keep the system safe without running into emergency situations (i.e. activating redundancy), and the number of system emergency states can be reduced. This paper suggests methods for online monitoring of wear-out detectors to increase reliability and safety.

14:20 – 14:40 Coffee Break

PRIME Technical Sessions *13:00-14:20*

D4 RF Circuits and Systems (2)

Chair: Lantao Wang, RWTH Aachen University, Germany

D4.1 13:00

Low Power High Linearity 14-23 GHz SiGe HBT Downconversion Mixer

Syed Sharfuddin Ahmed and Hermann Schumacher, University of Ulm, Germany.

This paper presents a low power, highly linear RF to IF down-conversion mixer operating at 14-23 GHz RF frequency in a 0.13m SiGe:C BiCMOS technology. The mixer is designed as a modified Gilbert cell topology where the RF transconductance stage is replaced by a passive input matching network thus reducing the supply voltage requirement and increasing linearity. The mixer consumes only 2.08 mW of power while exhibits a conversion gain of around -3 dB and a noise figure (NF) of <12 dB at the frequency of interest. The downconversion mixer has IP1dB of -5 dBm and IIP3 of +2 dBm. The results show that the presented down-conversion mixer can operate at low power while achieving comparable performance to state-of-the-art mixers at this frequency range.

D4.2 13:20

A Mixer-Embedded Low Noise Amplifier for Mixer-First Direct-Conversion Wake-Up Receivers

Christopher Nardi, Alexander Kronig, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany.

This paper presents the design of an integrated mixer-embedded low-noise amplifier (LNA) for mixer-first direct down-conversion wake-up receivers suited for IEEE 802.11ba. An efficient self-biased common gate-common source (CG-CS) coupling LNA with body coupling for improved noise figure (NF) was combined with three passive two-path mixers with capacitive load. This way, large decoupling capacitors can be avoided and antenna impedance matching without the need for external matching circuitry is achieved. Simulations show a high gain which can be varied between 52 dB and 16 dB, a NF of less than 9.4 dB and a current consumption of only 35 µA at 900 mV supply voltage. In its lowest gain setting, an IIP3 of -22 dBm is achieved. The structure is implemented in a 28 nm CMOS technology. Currently, only post-layout simulation data is available and a test die for collecting experiment data is being manufactured.

D4.3 13:40

Make Some Noise: Energy-Efficient 38 Gbit/s Wide-Range Fully-Configurable Linear Feedback Shift Register

Christoph Wagner [1], Georg Gläser [2], Thomas Sasse [1], Gerald Kell [3] and Giovanni Del Galdo [1,4].

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Compressed Sensing (CS) and Radio Detection and Ranging (RADAR) Systems require stimulus signals with properties similar to true random signals, but deterministic and reproducible in hardware. Therefore, Pseudo-Random Noise (PRN) sequences render ideal for this purpose. Especially mm-Wave systems require very high symbol rates and hence operating frequencies. Being able to choose a PRN signal is key to achieving good system performance by means of high operating frequency and energy consumption. For operating near the extreme limits of the technology, we propose an energy-efficient fully-configurable Linear Feedback Shift Register (LFSR) architecture with synchronous reset for PRN generation based on Positive Emitter Coupled Logic (PECL). By choosing a shift-register based multi-data-rate (MDR) structure, we shift the logic paths to a low-frequency domain. Further, we construct the register from small elementary slices with two levels of Power-Shut-Off (PSO) functionality for reducing the power consumption from 12% to 69%. We prove our architecture in 130nm SiGe BiCMOS technology, using transistor-level simulations and calibrated fab models. The register of length 24 is shown to operate correctly up to 38.5GHz, corresponding to 1/6 th of the process transition frequency. Our design draws 180mW to 510mW from a 2.50V supply at a die area of 0.10mm² (includes serializer).

D4.4 14:00

Every Clock Counts - 41 GHz Wide-Range Integer-N Clock Divider

Christoph Wagner [1], Georg Gläser [2], Gerald Kell [3] and Giovanni Del Galdo [1,4].

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[3] Technische Hochschule Brandenburg, Germany. [4] Fraunhofer IIS, Ilmenau, Germany.

Current clock divider architectures suffer from either inflexible divider ranges or slow performance due to long logic paths. When implementing Compressed Sensing (CS) signal acquisition for systems operating at mm-wave Radio Frequency (RF), both flexibility and operation at the limits of the technology node are required. We propose a configurable integer-N clock divider architecture with synchronous reset that satisfies this need. With a wide divider range of S = 8...1048583, an output duty cycle of 50 % is guaranteed for even, and approached for odd divider factors. The architecture is suited for operation with very high input clock frequencies, approaching the transit frequency of the technology. The key to construct our design is a serializer based approach, that enables the control logic to operate on two levels of lower frequencies. A symbol generator provides the output symbol stream. Internal clocks are derived directly from internal state vectors. In this way, the 20bit divider range is achieved with only 22 Flip Flops (FFs) (excluding the serializer) and no combinatory logic in the fastest clock domain. We demonstrate our architecture in 130nm SiGe BiCMOS technology using Positive Emitter Coupled Logic (PECL). We show that transistor-level simulation using calibrated fab models confirms successful operation up to 41.70 GHz which corresponds to ≈ 1/6 th of the process transition frequency. At a die area of 0.06 mm² (including serializer), our design draws ≈ 225 mW from a 2.50 V supply.

14:20 – 14:40 Coffee Break

SMACD Technical Session *14:40-15:20*

A5 Device Modelling (1)

Chair: Nicola Femia, University of Salerno, Italy

A5.1
14:40

A Compact Model for Scalable MTJ Simulation

Fernando García-Redondo [1], Pranay Prabhat [1], Mudit Bhargava [2] and Cyrille Dray [3]

[1] Arm Ltd, Cambridge, UK. [2] Arm Inc, Austin, USA. [3] Arm Ltd, La Paros, France

This paper presents a physics-based modeling framework for the analysis and transient simulation of circuits containing Spin-Transfer Torque (STT) Magnetic Tunnel Junction (MTJ) devices. The framework provides the tools to analyze the stochastic behavior of MTJs and to generate Verilog-A compact models for their simulation in large VLSI designs, addressing the need for an industry-ready model accounting for real-world reliability and scalability requirements. Device dynamics are described by the Landau-Lifshitz-Gilbert-Slonczewsky (s-LLGS) stochastic magnetization considering Voltage-Controlled Magnetic Anisotropy (VCMA) and the non-negligible statistical effects caused by thermal noise. Model behavior is validated against the OOMMF magnetic simulator and its performance is characterized on a 1-Mb 28nm Magnetoresistive-RAM (MRAM) memory product.

A5.2
15:00

A Quantitive Analysis of the Recovery Effect in Batteries from Datasheets

Alberto Bocca, Yukai Chen, Wenlong Wang, Alberto Macii, Enrico Macii and Massimo Poncino

Department of Control and Computer Engineering, Politecnico di Torino, Torino, Italy

Over the past decade, battery modeling using datasheets has been an intensive research topic due to the growing number of battery-powered devices. In this context, electronic designers who have to simulate and investigate the energy performance of circuits, need to have simple analytical or circuit-equivalent models that also characterize the non-ideal behavior of the battery used by their devices. One of the typical non-ideal discharge behaviors of certain batteries is the partial recovery of their energy after a current pulse; this is known as recovery effect. Consequently, the battery runtime is generally longer in the case of a battery operating at pulsed discharge current than at constant current of the same magnitude. This work aims to demonstrate how to analyze the recovery effect simply by considering the manufacturer's data. By applying the proposed method to the Energizer E91 alkaline cell, the results show that the absolute recovered energy, as additional available capacity, is greater the higher the battery current magnitude. In this case, the additional battery capacity can reach up to about 30% for medium currents. Besides, some direct experimental measurements validate the proposed methodology.

SMACD Technical Session *14:40-15:40*

B5 Optimization Methods

Chair: Francisco Fernandez, Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC and Universidad de Sevilla), Spain

B5.1
14:40

Surrogate-Assisted Multi-objective Differential Evolution based on Gaussian Process for Analog Circuit Synthesis

Sen Yin, Wenfei Hu, Ruitao Wang, Zhikai Wang, Jian Zhang and Yan Wang

Institute of Microelectronics, Tsinghua University, China

In this paper, A surrogate-assisted multi-objective differential evolution based on Gaussian process is proposed for analog circuit synthesis. NSGA-II-DE is used as the multi-objective optimizer and online Gaussian process surrogate model is constructed to prescreen the best two trial vectors according to non-dominated sorting and modified crowding distance. Only two instead of multiple designs are simulated by HSPICE in one generation. The efficiency of proposed approach is verified on two real-world circuits. Compared with two state-of-the-art multi-objective evolutionary algorithms, our method can achieve better Pareto front with much less number of simulations.

B5.2
15:00

A fast Structural Synthesis Algorithm for Op-Amps based on Multi-Threading Strategies

Inga Abel, Clara Kowalsky and Helmut Graeb

Technical University of Munich, Munich, Germany

This paper presents a method to speed up the structural synthesis of op-amps presented in [1]. Op-Amp topologies are created, sized and evaluated according to a given set of specifications. Three different types of op-amps are supported: single-output, fully-differential and complementary op-amps. The sizing and evaluation process is parallelized using multi-threading techniques. On a common computer the new algorithm needs less than eight hours to find all suitable topologies for a given set of specifications out of thousands of topologies compared to 22 h in [1]. The experimental results present the speed-up of the algorithm on seven different specification sets.

15:40–16:00 Coffee Break

B5.3 15:20 **An Essay on the Next Generation of Performance-driven Analog/RF IC EDA Tools: The Role of Simulation-based Layout Optimization**

Ricardo Martins [1], António Gusmão [1,2], António Canelas [1], Fábio Passos [1,3], Nuno Lourenço [1] and Nuno Horta [1,2]

[1] Instituto de Telecomunicações, Lisboa, Portugal. [2] Instituto Superior Técnico, Universidade de Lisboa, Portugal. [3] Dialog Semiconductors, Lisboa, Portugal

Despite the fact that analog and radio-frequency (A/RF) integrated circuit (IC) design automation has been intensively studied in the last few decades, only automatic circuit-level sizing methodologies have achieved a satisfactory level of maturity. Layout and its countless issues have challenged all automation attempts, and two limitative factors must be addressed to force their way into industrial environment: plug-and-play capabilities, and, accurate assessment of post-layout performance degradation. This paper brainstorms around the idea of developing the ultimate fully automatic "performance-driven" A/RF IC synthesis, by incorporating simulation-based layout optimization concepts in the flow. The essay is carried the Ponderous tool, a novel and highly integrated, but extremely computationally intensive, placement A/RF IC optimizer.

PRIME Technical Sessions ***14:40-15:40***

C5 Sensing Circuits (1)
Chair: Markus Sporer, University of Ulm, Germany

C5.1 14:40 **Experimental Investigation of Dielectric Loss Induced Noise in Charge Detection Systems for Cosmic Dust**

Sebastian Kelz, Markus Groezing and Manfred Berroth.

Institut für Elektrische und Optische Nachrichtentechnik, University of Stuttgart, Germany.

In this paper the influence of dielectric loss induced noise on a differential charge detection system for cosmic dust trajectory sensors is analyzed. For the sake of generality the distributed charge detector is replaced by compact capacitors with different dielectric materials. It is shown that for low-frequency high-impedance systems the selection of very low loss dielectric materials is of crucial importance to minimize the overall noise charge of the system.

C5.2 15:00 **Generalized comparison of the accessible emission limits of flash- and scanning LiDAR-systems**

Roman Burkard [1], Reinhard Viga [1], Jennifer Ruskowski [2] and Anton Grabmaier [1].

[1] University of Duisburg-Essen, Germany. [2] Fraunhofer IMS, Duisburg, Germany.

In the field of autonomous driving and human-robot collaboration applications the demand for three-dimensional imaging systems, that are reliable, small and low-cost, is rising. A promising technology to satisfy these demands are scanning or flash-based light detection and ranging (LiDAR)-systems, which differ mainly in the illumination of the field-of-view. A scanning LiDAR-system illuminates the field-of-view sequentially by deflecting a laser beam. In a flash LiDAR-system the laser beam is extended to illuminate the whole field-of-view with every emitted laser pulse. Both illumination principles are extensively treated in the recent literature separately and without the inclusion of the limits defined by the laser safety standard IEC 60825-1:2014. In this work a generalized model is derived from the standard. This model is able to determine the emission limits of the standard for both LiDAR-systems at the same time and it is used to compare the maximum output power and the intensities in the field-of-view for both LiDAR-systems.

C5.3 15:20 **A Mixed-Precision Binary Neural Network Architecture for Touch Modality Classification**

Hamoud Younes [1,2], Ali Ibrahim [1,2], Mostafa Rizk [2] and Maurizio Valle [1].

[1] University of Genova, Italy. [2] Lebanese International University, Bekaa, Lebanon

Binary Neural Networks (BNN) have been proposed to address the computational complexity and memory requirements of Convolutional Neural Networks (CNN). However, in most of the applications, BNNs suffer from severe accuracy loss due to the 1-bit quantization. In this paper, a Mixed-Precision Binary Weight Network (MP-BWN) is proposed as a compromise between CNN and BNN. Compared to traditional binary networks, MP-BWN offers better performance with an acceptable increase in the network size. MP-BWN achieves up to 99% reduction in both the number of operations and the network size compared to similar state-of-the-art solutions. When validated on a touch modality classification problem, the MP-BWN surpassed similar existing solutions by achieving a classification accuracy of 77.8%.

14:40 – 15:40 Recruiting/Networking

15:40 – 16:00 Coffee Break

Wednesday, July 21st 16:00–17:00

SMACD Technical Session *16:00-17:00*

A6 RF Systems (2)

Chair: Günhan Dündar, Bogazici University, Turkey

A6.1 16:00

A Phase Error Correction Algorithm for RF Energy Harvesters Using Two Antennas

Ali Dogus Güngördü, Didem Erol, Alican Çaglar and Mustafa Berke Yelten

Istanbul Technical University, Electronics and Communications Engineering, Istanbul, Turkey

In this study, a phase error correction algorithm is proposed for radio frequency (RF) energy harvesting through a fully differential RF-to-DC converter with two antennas. The system keeps one of the inputs as the reference and adjusts the phase of the other input. A 2-bit resolution is used to demonstrate how the concept works. The system aims to operate without an external battery. System-level simulation results prove that through the proposed concept, the efficiency of the harvester can be considerably boosted for an RF harvester with two antennas.

A6.2 16:20

Robust Design Methodology for RF LNA including Corner Analysis

Antonio Dionisio Martínez-Pérez [1], Francisco Aznar [2], Guillermo Royo [1], Pedro Martinez [1] and Santiago Celma [1]

[1] Group of Electronic Design (GDE), Universidad de Zaragoza, Zaragoza, Spain.
[2] Group of Electronic Design (GDE), Centro Universitario de la Defensa, Zaragoza, Spain

This work presents a design methodology of a competitive inductorless single-ended LNA in 65-nm standard CMOS technology. Instead of relying only on typical conditions, the method uses corners to find the optimal device sizing, anticipating variations on the implemented circuit, and hence, the design significantly improves its reliability, being able to fulfil specifications in a wider range of process deviations. Also, in addition to its robustness, the designed circuit is very effective, achieving a Noise Figure of 2.9 GHz at 5 GHz with a simple gm-enhanced common-gate amplifier thanks to a careful design window selection. The paper also describes the tradeoff-oriented design-window methodology that accomplishes the demanding specifications. Moreover, the authors provide a biasing strategy to offset the high process variability of the technology and statistical simulations show a 50 % reduction of failed samples due to process variations. The paper includes figures and statistical results from Montecarlo analysis for a more detailed description of the effect of the method and strategy employed on the complete design. Finally, a table compares the results with other similar circuits in the state-of-art.

A6.3 16:40

Event-Driven Modeling and Simulation of 5G NR-Band RF Transceiver in SystemVerilog

Chan Young Park and Jaeh Kim, Elelctrical and Computer Engineering Department, Seoul National University, Seoul, Korea

While baseband-equivalent real-number models (RNMs) are the current state-of-the-art for modeling RF transceivers in SystemVerilog, but their simulation speeds and accuracies are not adequate for predicting performance degradation due to DC offsets or high-order harmonic effects. This paper presents the models for a multi-standard, direct-conversion RF transceiver using XMODEL, for evaluating its system-level performance as well as verifying its digital controllers. The simulation results indicate that the presented models, including the digital configuration/calibration logic for the 5G sub-6GHz-band and mmWave-band transceiver, can deliver 30–1800× higher speeds than the baseband-equivalent RNMs while estimating the quadrature amplitude modulation signal constellation and error vector magnitude in the presence of non-idealities such as non-linearities, DC offsets, and I/Q imbalances.

17:00 Erfurt Video-Tour

Welcome to Erfurt!

I invite you on **Wednesday, July 21st, at 5pm (CEST)** to a virtual live tour through my hometown: the flower, cathedral and Luther city of Erfurt.

Around 1300 years of history come to life on the walk. From the time when the first monks evangelized the Franconian Empire, to the heyday of knighthood when Barbarossa was emperor, to the student Martin Luther, who became a monk and priest in Erfurt, through the Swedish period under Gustav Adolph von Wasa in the 30 Years War to the conquest of the City by the Archbishop of Mainz.

Horticulture and industrialization during the Wilhelminian era led Erfurt to a second boom in the 19th century. With a lot of luck, Erfurt survived the age of extremes in order to blossom again in full splendor in the 21st century as the state capital of Thuringia under the sign of the BUGA 2021.

My name is Matthias Gose, I have been on the streets as a tour guide for 23 years.

SMACD Technical Session *16:00-16:40*

B6 Complex System Analysis I

Chair: Jürgen Scheible, Reutlingen University, Germany

B6.1 16:00

An Efficient Modeling Approach for Large Ring Oscillator Based Ising Machines

Markus Graber, Nico Angeli and Klaus Hofmann

Integrated Electronic Systems Lab, Technical University of Darmstadt, Darmstadt, Germany

Using the Ising model for computation of optimization problems is getting more and more popular. A very promising approach is the use of electrical oscillators, often called Oscillator-based Ising machine (OIM), integrated on a single silicon die. A new modeling approach to handle the complexity of large networks during the design phase is proposed. The simulation runtime is significantly reduced while valuable design insight is provided. It helps to understand the relation between circuit level properties and Ising machine behaviour. It is easy to use and has minimal requirements on the circuit topology. All relevant properties used for the proposed modeling approach are extracted from a transistor-based implementation by a circuit simulator. Systems with large number of nodes can be fast and accurately analyzed and optimized for their computation ability.

B6.2 16:20

The Merging Technique to Simulate Synchronization Mode of Coupled Oscillators

Sergey Rusakov and Mark Gourary

IPPM, Russian Academy of Sciences, Moscow, Russia

New approach is applied to the analysis of synchronized Kuramoto oscillators. The approach is based on the technique of merging the oscillator models. This new technique provides computational efficiency due to the developed transformation of the pair of synchronized oscillators into single Kuramoto oscillator. Analytical expressions are derived that define the characteristics of merged oscillators, the transform of coupling functions and the sequence of merging operations. The results of numerical experiments are presented.

PRIME Technical Sessions *16:00-16:40*

C6 Sensing Circuits (2)

Chair: Markus Sporer, University of Ulm, Germany

C6.1 16:00

A CMOS SPAD pixel with an integrated mixed-signal rotatory TDC

Sergio Moreno, Victor Moro and Angel Dieguez, University of Barcelona, Spain

During the last century, much of the scientific discoveries and advances in the biological field have been derived from the exploration of fluorescence phenomena. This has been possible, in part, thanks to the development of a wide variety of measurement techniques accompanied by high-performance sensing devices. Among these are CMOS Single Photon Avalanche Diodes (SPADs) image sensors, which offer fast response and low fabrication costs. In this work we have developed a pixel with dimensions of 40 µm x 40 µm, which together with a 10 µm SPAD, allows to obtain a 5% fill-factor. In addition, it has an integrated Time-to-Digital Converter(TDC) with a programmable bin width from 170ps up to 1ns with a total measurement range of up to 72 ns.The pixel architecture will enable fluorescence lifetime measurements of organic and inorganic dyes. The photon arrival time will be used to generate a histogram.

C6.2 16:20

Germanium–InGaZnO heterostructured thin-film phototransistor with high IR photoresponse

Hichem Ferhati, Fayçal Djeffal and A Bendjerad, University of Batna, Algeria.

In this paper, the role of introducing Germanium (Ge)/IGZO heterostructure in enhancing the Infrared (IR) photodetection properties of thin-film phototransistor (Photo-TFT) is presented. Numerical models for the investigated device are developed using ATLAS device simulator. The influence of Ge photosensitive layer thickness on the sensor IR photoresponse is carried out. It is revealed that the optimized IR Photo-TFT based on p-Ge/IGZO heterojunction can offer improved IR responsivity of 4.1×102 A/W, and over 106 of sensitivity. These improvements are attributed to the role of the introduced p-Ge/IGZO heterostructure in promoting IR photodetection ability and improved separation and transfer mechanisms of photo-exited electron/hole pairs. The photosensor is then implemented in an optical inverter gate circuit in order to assess its switching capabilities. It is found that the proposed phototransistor shows an improved optical gain thus indicating its excellent performance. Therefore, providing high IR responsivity and low dark noise effects, the optimized Ge/IGZO IR Photo-TFT can be a potential alternative photosensor for designing optoelectronic systems with high-performance and ultralow power consumption

14:40 – 15:40 Recruiting/Networking

17:00 Erfurt Video-Tour

Thursday, July 22nd 09:00–12:20

09:00–10:00 ***Plenary Talk***

Chair: Ralf Sommer, IMMS GmbH & TU Ilmenau, Germany

Designing the Future of Automotive, Medical and Industrial – A Foundry Perspective on Challenges and Chances

Jörg Doblaski
CTO, X-Fab Global Services GmbH

The European microelectronics industry has a strong footprint in Automotive, Medical and Industrial markets, which are expected to grow significantly within the coming years. Driven by the transition towards connected, autonomous, shared and electric mobility, by the trend to personal medical devices and the needs of an aging society, as well as by the digital transformation of manufacturing, the requirements for microelectronic products are increasing, which calls for innovative solutions for IC manufacturing and design enablement and verification. The presentation is touching on process and device co-design challenges by using wafer scale CMOS and MEMS technologies in the development of system solutions. Using examples from automotive, medical and industrial, it will be shown how novel design technology can help to de-risk the design process, to reduce re-designs and time-to-market and to enable new applications.

Jörg Doblaski is Chief Technology Officer at X-FAB, and in this role responsible for the foundry's process technology development, design enablement and technical support. Prior to the CTO role, Jörg served in different engineering- and engineering management positions, with focus on the area of design support and design enablement. Jörg studied at the Technical University of Ilmenau, and holds a diploma degree in Electrical engineering and information technology.

10:00–10:20 Coffee Break

10:20–10:40 **BarCamp Scheduling II** *(further information on page 9)*

10:40–11:20 **BarCamp Sessions**			
BC1	**BC2**	**BC3**	**BC4**

11:20–11:40 Coffee Break

11:40–12:20 **BarCamp Sessions**			
BC1	**BC2**	**BC3**	**BC4**

12:20–13:00 Lunch

SMACD Technical Session *13:00-14:20*

A7 Wireless Power SS

Chair: Giulia Di Capua, University of Cassino and Southern Lazio, Italy

A7.1 13:00 Sensitivity analysis in dynamic WPT systems based on non-intrusive stochastic methods

Paul Lagouanelle [1,3], Giulia Di Capua [4], Nicola Femia [5], Fabio Freschi [3], Antonio Maffucci [4], Lionel Pichon [1] and Salvatore Ventre [4]

[1] Group of Electrical Eng., Paris, CNRS, CentraleSup´elec, Universit´e Paris-Saclay, Gif-sur-Yvette, France.
[3] Department of Energy, Politecnico of Torino, Turin, TO, Italy.
[4] Department of Electrical and Information Eng., University of Cassino and Southern Lazio, Cassino, FR, Italy.
[5] Department of Information and Electrical Eng. and Applied Math., University of Salerno, Fisciano, SA, Italy

The analysis of coil pairs mutual inductance is of great interest in the characterization, design and optimization of dynamic Wireless Power Transfer (WPT) systems for automotive applications. The objective of this paper is to show the use of non-intrusive stochastic methods to build accurate predictors of the mutual inductance. These methods are based on a polynomial-Chaos-Kriging metamodeling approach, which enables an accurate sensitivity analysis at system level. This approach is here applied to study the most influential spatial parameters in a dynamic WPT system, given different trajectories of the vehicle during its motion.

A7.2 13:20 Performance Analysis of IPT Systems for Electric Vehicles Dynamic Battery Charging

Giulia Di Capua [1], Luca De Guglielmo [2] and Nicola Femia [2]

[1] Department of Electrical and Information Eng., University of Cassino and Southern Lazio, Cassino, FR, Italy.
[2] Department of Information and Electrical Eng. and Applied Math., University of Salerno, Fisciano, SA, Italy

This paper investigates the joined influence of the vehicle trajectory, the coils mutual inductance, and the control strategy of transmitter and receiver power converter stages on the energy and efficiency performances of Inductive Power Transfer (IPT) systems for electric vehicles dynamic battery charging. A model based on normalized electric and magnetic variables is adopted to verify the maximum charge and energy efficiency of the IPT system, during the vehicle motion. The performances with respect to the control action implemented at the inverter and post-regulator stages and the vehicle nominal trajectory are also analyzed.

A7.3 13:40 Coil Geometry Modeling and Optimization for a Bidirectional Wireless Power Transfer System

Simon Nigsch, Falk Kyburz and Kurt Schenk

Institute for Energy Systems, Eastern Switzerland University OST, Buchs SG, Switzerland

The coil geometry and improvement of misalignment tolerance is a key challenge for the optimization of wireless power transfer (WPT) systems. In this paper a double-D shaped coil geometry is modeled and optimized for a bidirectional wireless power transfer system for electrical vehicles (EVs) with vehicle to grid (V2G) capabilities. With the new proposed winding configuration, the magnetic coupling is less sensitive to parking misalignments, which is helpful for a highly efficient battery charging system. Further efforts to reduce the amount of ferrite material helps to lower the weight and cost of the system without affecting the performance. In order to verify the effect of the winding geometry experimentally, a 3.6 kW hardware prototype was built.

A7.4 14:00 Impact of the Pad Geometry on System-Level Performance Indicators in WPT Systems for Electrical Vehicles

Antonio Maffucci [1], Salvatore Ventre [1] and Alberto Delgado Exposito [2]

[1] Dep. of Electrical and Information Engineering, Univ. of Cassino and Southern Lazio, Cassino, Italy.
[2] Centre of Industrial Electronics (CEI), Universidad Politécnica de Madrid, Madrid, Spain

This paper deals with the system-level optimization of resonant Inductive Power Transfer systems for dynamic recharging of electrical vehicles. Specifically, different shapes of transmitting and receiving coils are compared in terms of their impact on system-level performance indicators, such as the voltage gain and the resonant frequency. The impact is here associated to the variation of the coil coupling factor along the trajectory of the vehicle. As a case study, a dynamic real 85-kHz resonant IPT system is analyzed, whose reference coil geometry is rectangular. Alternative coil shapes (circular, rounded edges) are investigated, highlighting what are the best options for the the specific design optimization targets.

14:20 – 14:40 Coffee Break

SMACD Technical Session *13:00-14:20*

B7 Digital Circuit and System engineering
Chair: Rafael Castro Lopez, Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Spain

B7.1 13:00
RTL Implementation of MCMC-based Constraints Solver
Moemen Ahmed [1], Youssef Ahmed [1], Younan Nagy [1], Manar Adbel-Rahman [1], Khaled Salah [2], M. Watheq El-Kharashi [1], Ayub Khan [2]

[1] Department of computer and systems, faculty of engineering, Ain Shams University, Cairo, Egypt.
[2] Siemens Digital Industries Software, Fremont, USA.

Functional hardware verification is one of the most challenging areas in the hardware design cycle. With the increase in the complexity and size of the design, the time needed for verification becomes the largest part of the total design time. The most recent technique in practical verification is constrained random simulation. This method needs a solver to produce random input stimuli that satisfies a pre-defined set of input constraints. The efficiency of the overall verification process depends critically on the speed of the constraints solver and the distribution of the generated solutions. In this paper, we propose hardware acceleration for RTL constraints solver integrated with SystemVerilog. The solver is based on Markov Chains Monte Carlo methods.

B7.2 13:20
A study of SRAM PUFs reliability using the Static Noise Margin
Eros Camacho-Ruiz, Pablo Saraza-Canflanca, Rafael Castro-Lopez, Elisenda Roca, Piedad Brox and Francisco Fernandez

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC and Universidad de Sevilla), Sevilla, Spain

The use of SRAM cells as key elements in a Physical Unclonable Function (PUF) has been widely reported. An essential characteristic the SRAM cell must feature for a reliable PUF is stability, i.e., it must power up consistently to the same value. Different techniques to measure this stability (and thus improve the PUF reliability) have been reported, such as the Multiple Evaluation method and, more recently, the Maximum Trip Supply Voltage method, the latter using the Data Retention Voltage (DRV) concept. While experimental results have been reported, this paper sheds some light from a different perspective: simulation. In this sense, and using wellknown concepts like butterfly curves, static noise margin and voltage-transfer curves, an analysis is provided on why and how stability originates in the cell. Moreover, by simulating the butterfly curve behavior when the supply voltage scales down, it is possible to correlate DRV with stability, thereby confirming the correct theoretical foundation of the MTSV method.

B7.3 13:40
Design and Optimization of a Control Algorithm for a Digital Low-Dropout Regulator in System-on-Chip Applications
Benedikt Ohse [1] and Jun Tan [2]

[1] Ernst-Abbe-Hochschule Jena, Jena, Germany. [2] IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH), Ilmenau, Germany

The System-on-Chip (SoC) solutions have gained more importance in the field of microelectronics in the past years. The aim of this work is to develop an algorithm for a digital low-dropout regulator (DLDO) for a near-threshold / low supply voltage application. The developed LDO is fully synthesisable and has a high robustness. In the work, simulation models were developed for a combination of a SAR and a PID controller. In addition, research and optimizations were carried out regarding the phase shift for better control of the PID controller, the switching between the two algorithms and the stability of the digital LDO. The design is implemented in a commercial CMOS technology, with the input supply voltage from 0.85 V to 1.8 V. The input voltage range of the developed design ranges from 0.9 to 1.8 V and the power consumption is smaller as 10 µW at an operating voltage of 0.9 V. In order to achieve a trade-off between a fast settling for large transient and a low ripple at DC, a combined algorithm of a SAR and a PID controller is implemented. We have also optimised the performance for a wide input voltage range (0.9 V to 1.8 V), fast settling time (50 µs at 4 MHz, 1.2 V) and stable setting (0.79 V to 0.84 V at 4 MHz, 1.2 V). The clock and the power consumption are also reduced (average < 10 µW with 0.9 V VDC and 4 MHz, while the output power is between 10 µA and 320 µA using constant load.)

B7.4 14:00
A Differential Public PUF Design for Lightweight Authentication
Shengyu Duan [1,2] and Gaole Sai [3,4]

[1] School of Computer Engineering and Science, Shanghai University, China. [2] State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, China. [3] Guangdong Provincial Key Lab of Robotics and Intelligent System, Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China. [4] CAS Key Laboratory of Human-Machine Intelligence-Synergy Systems, Shenzhen Institutes of Advanced Technology, China

14:20–14:40 Coffee Break

Physical Unclonable Functions (PUFs) have emerged as a promising primitive to provide a hardware keyless security mechanism for integrated circuit applications. Public PUFs (PPUFs) address the crucial PUF vulnerability of requiring databases to store the secrete reference information. This paper investigates one of the PPUF families, differential PPUF (dPPUF), which exploits complexly interacted logic gates to create time gap between actual execution and simulation, and to prevent simulation attacks. Conventional dPPUFs have high costs. We observe the repressers have significant impact on the simulation time, but take a great proportion in current dPPUF structure. We thereby present a new represser network with specially designed interconnection and shared logic, to maintain a high circuit complexity and to reduce the area cost. We show the proposed dPPUF has similar resilience over simulation attacks as the conventional design. Area cost can be reduced by up to 44%, and thus the proposed design can be used for lightweight authentication.

PRIME Technical Sessions ***13:00-14:40***

C7 Power Circuits and Harvesting

Chair: Sebastian Kelz, University of Stuttgart, Germany

C7.1 13:00 Integrated Hysteretic Controlled Regulating Buck Converter with Capacitively Coupled Bootstrapping

Francarl Galea, Owen Casha, Ivan Grech, Edward Gatt and Joseph Micallef, University of Malta.

This paper presents the circuit design, layout implementation and simulations of an on-chip hysteretic regulating buck converter. All the high voltage transistors of the buck converter were implemented using 45V NMOS thin gate oxide layer transistors and are operated by means of a capacitively coupled bootstrap circuit. The circuit was implemented using the XFAB CMOS 0.35um high voltage technology and all the circuit blocks were designed using analogue electronic techniques, with the transistors operating in the sub-threshold region, in order to minimize power consumption. Simulations show that the control circuit of the hysteretic regulator consumes around 0.5uW, and the proposed buck converter operates at peak efficiency of 82%. The input voltage range of the regulator is from 1.5V to 45V and has a power range from 10uW to 200mW. The output regulated voltage is tunable via a feedback resistor and can be varied from 0.6V to 40V, with a dropout voltage of 1V.

C7.2 13:20 Single-Inductor Dual-Output Buck Converter with Charge Recycling

Kemal Ozanoglu and Gunhan Dundar, Bogazici University, Istanbul, Turkey.

This paper presents a novel switching topology for SIDO buck converters aiming to achieve charge recycling during sink/source operation. Two switching sequence options have been demonstrated for low load current (DCM) and high load current (CCM) profiles. Simulation results show that the proposed architecture can achieve sink/source operation by re-using the charge stored in the output capacitors with continuous conduction through the inductor, demonstrating that this topology promises to be a convenient solution for SIDO/SIMO switching converters where sink/source operation and high power efficiency are essential.

C7.3 13:40 Design of an integrated Maximum Power Point Boost Converter for PV Submodules

Léon Weihs, Michael Hanhart, Leo Rolff, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany.

The design constitutes an integrated boost controller with MPPT, targeting the optimization of power output of solar submodules, boosting system efficiency in partially shaded conditions compared to conventional PV panels. The negative impact on output power, caused by cell mismatch due to production and long-term degradation, can be minimized. The IC is designed for power throughputs up to 120W with an input voltage range of 7V - 24V and output voltages up to 50V. The converter operates at a switching frequency of 300kHz in current mode control and is internally compensated. During low irradiance, the controller changes to pulse-frequency operation to further increase efficiency. The MPPT utilizes a delta modulator, avoiding the need for high resolution ADCs. The sense structure dynamically adjusts the MPP measurement resistance, further increasing tracking efficiency.

C7.4 14:00 Design of a High PSRR Multistage LDO with On-Chip Output Capacitor

Jonas Zoche, Michael Hanhart, Jan Grobe, Léon Weihs, Leo Rolff, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany.

This paper proposes a high PSRR LDO design implemented in a 0.18 µm BCD technology using only on-chip capacitors. Multiple stages in series with PMOS pass transistors lead to high PSRR, small drop-out voltage, and low circuit complexity in comparison to designs relying on ripple feedforward. Without external capacitors, the presented auxiliary LDO does not increase the pin count while the multistage approach leads to low circuit complexity. Overall, 54 dB PSRR are achieved across corners up to 10 GHz with a quiescent current of 15.5 µA and 0.192 µm^2 chip area.

14:20 – 14:40 Coffee Break

PRIME Technical Sessions ***13:00-14:20***

D5 Devices and Reliability
Chair: Stefan Heinen, RWTH Aachen University, Germany

D5.1
13:00

Modeling Ni/β-Ga_2O_3 SBD interface properties

Madani Labed [1], Nouredine Sengouga [1], Afak Meftah [1], Jun Hui Park [2], Sinsu Kyoung [3], Hojoong Kim [2] and You Seung Rim [2].

[1] Laboratory of Semiconducting and Mettalic Materials, Biskra university.
[2] Department of Intelligent Mechatronics Engineering, and Convergence Engineering for Intelligent Drone.
[3] Research and Development, Powercubesemi Inc.

In this work, Ni/β-Ga_2O_3 Schottky diode deposited by electron-beam evaporation was studied. A detailed numerical simulation is carried out to reproduce the current-voltage measurement of Ni/β-Ga_2O_3 Schottky diode and extract the Ni/β-Ga_2O_3 interface properties. For more agreement between simulation and measurement the effect of Ni workfunction, Si-doped β-Ga_2O_3 surface electron affinity and traps concentration were studied.

D5.2
13:20

Performance assessment of a new low-cost RF sputtered Schottky diode based on a-Si/Ti structure

Hichem Ferhati, Fayçal Djeffal, A Bendjerad and A Benhaya, University of Batna, Algeria.

In this paper, a new efficient and low-cost Schottky Diode (SD) based on a-Si/Ti structure was elaborated using RF magnetron sputtering technique. An exhaustive investigation of structural and electrical properties was performed, where the sputtered device was characterized using X-ray diffraction (XRD) and Keithley (4200-SCS) to measure the current-voltage characteristics. Moreover, a comprehensive study regarding the impact of the Ti layers on the device characteristics is carried out. It was demonstrated that implementing Ti intermediate layers could induce depletion regions at the interfaces, leading to significantly enlarged voltage barrier height. Furthermore, the elaborated SD exhibits a rectification behavior providing an appropriate current with a favorable ideality factor. This is mainly due to the reduced series resistance of the multilayer structure as confirmed by electrical analysis. Therefore, the proposed SD structure based on Ti intermediate layers provides improved performance and can open a new route for the fabrication of promising alternative devices for microelectronic and sensing applications

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D5.3
13:40

Digitally Programmable Potentiometer Multistage Architecture with Switch Independent Linearity

Giorgiana Catalina Ilie [1,2], Cristian Tudoran [2], Otilia Neagoe [2], Gheorghe Pristavu [1] and Gheorghe Brezeanu [1].

[1] On Semiconductor, Romania. [2] University "Politehnica" of Bucharest, Romania.

This paper describes a multistage architecture for high resolution digitally programmable potentiometers. Its linearity characteristics dependence on switch's on-resistance is highly diminished. The proposed topology was implemented in a 0.18µm CMOS process and used in fabricating an 8-bit resolution digital potentiometer with I2C interface. The maximum measured values for its non-linearity errors are 0.25LSB for INL and 0.1LSB for DNL. A theoretical model for determining the non-linearity errors was developed for this architecture. It is proven that the linearity characteristics of the potentiometer are not affected by switches on-resistances. Moreover, the experimental non-linearity error values are attributed to deviations in unit resistances caused by process variations.

D5.4
14:00

Reliability Investigation of 0.18µm CMOS for OilField Applications

Yen Tran [1,2], Toshihiro Nomura [1], Mohamed Salim Cherchali [1], Claire Tassin [1], Yann Deval [2] and Cristell Maneux [2].

[1] Etudes et Production Schlumberger, Clamart, France. [2] Laboratoire IMS, Universite de Bordeaux, France.

We investigated the degradation due to BTI and HCI for 0.18um CMOS under extreme temperature operations (150°C and 210°C). The transistors have been applied dedicated DC bias and temperature conditions to investigate each intrinsic wear-out mechanism in specific severe environment for oilfield applications. The aging tests have been monitored up to 1000 hours. These results are preliminary used to develop equations reflecting aging laws to be included in commercial software tool for further investigation at logic circuit level.

14:20–14:40 Coffee Break

SMACD Technical Session *14:40-15:20*

A8 Complex System Analysis II

Chair: Jürgen Scheible, Reutlingen University, Germany

A8.1 14:40

A Probe Placement Method for Efficient Electromagnetic Attacks

Minmin Jiang and Vasilis Pavlidis

Advanced Processor Technologies group, Department of Computer Science, University of Manchester,Great Britain

Electromagnetic (EM) emissions have been explored as an effective means for non-invasive side-channel attacks. The leaked EM field from the memory bus when the data is loaded from the on-chip memory has received considerable attention in the literature. Meanwhile, off-chip memory buses gradually become the new attack target due to the relative ease of access in the modern systems in package technologies, such as 2.5-D integration where processing and memory chips are integrated, for example, on a silicon interposer. This paper, therefore, investigates EM snooping attacks on interposer-based off-chip memory buses. A gradient-search algorithm is proposed to locate fast (i.e. O(N)) the most efficient attack point. The effectiveness of the search algorithm and attack efficiency is evaluated on a 64-bit bus. It is demonstrated that at the optimal attack point, EM attacks can succeed with more than 10X fewer traces, compared to placing the probe to sub-optimal locations.

A8.2 15:00

Dealing with hierarchical partitioning in bottom-up design methodologies

F. Passos [1,2], Pablo Saraza-Canflanca [1], Rafael Castro Lopez [1], Elisenda Roca [1] and Francisco V. Fernandez [1]

[1] Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Sevilla, Spain.
[2] Instituto de Telecomunicações, Lisboa, Portugal

This paper deals with the expertise blend of circuit design and design methodology development required to successfully address hierarchical partitioning of analog, radio-frequency and mm-Wave circuits in bottom-up design methodologies. A set of guidelines is discussed for the optimal configuration of the bottom-up process that yields sound design results are obtained. These guidelines are demonstrated with two case studies.

SMACD Technical Session *14:40-15:20*

B8 Device Modelling (2)

Chair: Nuno Lourenço, Instituto de Telecomunicações, Portugal

B8.1 14:40

Organic Transistor Parameter Estimation and Accurate Modeling for Process Optimization

Rosalba Liguori, Gian Domenico Licciardo and Luigi Di Benedetto

Department of Industrial Engineering University of Salerno, Fisciano (SA), Italy

The development of accurate tools and models able to analyze and predict the electronic device properties is compulsory to promote the technological advancement and particularly to improve fabrication process in the case of unconventional materials. In this work the model proposed for the interpretation of the data obtained with the admittance spectroscopy technique is useful for investigating the causes of the property differences in organic thin film transistors fabricated with various gate dielectrics. The extracted parameters show that the use of the UV-cured copolymer PVP-co-PMMA as dielectric layer in a pentacene-based OTFT, instead of the as-deposited copolymer or the standard polymer PVP, reduces the ion diffusion through gate insulator and the density of trap states at the insulator-semiconductor interface, while improving the semiconductor structural order, therefore producing devices with lower and stable threshold voltage and lessened hysteresis.

B8.2 15:00

Bias Temperature Instability Characterization and Modelling for 0.18um CMOS under Extreme Thermal Stress Conditions

Yen Tran [1,2], Toshihiro Nomura [1], Mohamed Salim Cherchali [1], Claire Tassin [1], Yann Deval [2] and Cristell Maneux [2]

[1] Etudes et Production Schlumberger, Clamart, France. [2] Laboratoire IMS, Universite de Bordeaux, Talence, France

We investigated the significance of 0.18um CMOS degradation due to BTI under extreme temperature operations (150°C and 210°C). The transistors have been applied dedicated DC bias and temperature conditions to investigate the wear-out mechanism in specific severe environment for oilfield applications. The aging tests have been monitored up to 1000 hours. These results are preliminary used to develop equations reflecting aging laws to be included in commercial software tool for further investigation at logic circuit level.

16:00 – 16:20 Coffee Break

16:20 Award Ceremony & Closing Session

PRIME Technical Sessions ***14:40-16:00***

C8 Circuits for clock generation and optimization

Chair: Jonas Meier, RWTH Aachen University, Germany

C8.1 14:40

Skew and Jitter Performance in CMOS Clock Phase Splitter Circuits

Lorenzo Scaletti, Angelo Parisi and Luca Bertulessi, Politecnico di Milano, Italy.

This paper compares two different clock phase splitter architectures: the first is based on the standard XOR gate splitter topology, the other exploits the concept of phase interpolation. The comparison, supported by schematic simulations, shows that the phase interpolating splitter outperforms the XOR gate based topology with no penalty in power consumption. In particular, the output jitter is reduced by 15% while the skew between the output phases is reduced by about 80%. The phase interpolating splitter, implemented in 28nm CMOS, achieves jitter lower than 35fs with power consumption lower than 5mW at 1GHz input frequency in post-layout simulations. The skew between the generated output signals is always lower than 10ps.

C8.2 15:00

Entropy Analysis of RO-based Physically Unclonable Functions

Guillermo Diez-Senorans, Miguel Garcia-Bosque, Carlos Sanchez-Azqueta and Santiago Celma, University of Zaragoza, Spain.

In this paper we estimate the probability distribution of a ring oscillator based PUF (RO-PUF) operating under different digitization schemes (topologies) of compensated measuring, and we quantify their performance and security properties by means of the entropy and entropy-related metrics: entropy per bit ratio, entropy per oscillator ratio and the product of both. We have studied the most common digitization schemes for this type of systems, and we propose a new construction designed to overcome some flaws found in these. Each topology has been tested with a large set of frequencies obtained from an array of three-stages oscillators implemented in FPGA.

C8.3 15:20

On the Behavior of a Wide Set of Oscillators: PUFs or TRNGs?

Miguel Garcia-Bosque, Abel Naya, Guillermo Díez-Señorans, Carlos Sánchez-Azqueta and Santiago Celma, University of Zaragoza, Spain.

In this paper, a generic structure that includes previously studied oscillators (such as ring oscillators) as well as many other new oscillators has been studied to evaluate their suitability as TRNGs or PUFs. The studied structure consists of an array of n combinational logic blocks in a loop where the output of each block is a function of the output of the previous block and the feedback signal. To perform this analysis, a novel implementation has been proposed where, using a single implementation, we can make each block perform any possible 2-input function using some external configuration inputs. By analyzing all possible configurations of size equal or smaller than 7, we have concluded that none of them behave as an ideal TRNG and that ring oscillators present a behavior closest to the ideal one. Regarding their suitability for being used as PUFs, none of the polynomials have shown an ideal behavior but some of them present a higher reproducibility than the classical ring-oscillator PUF. Furthermore, we have noticed that, by increasing the length, we can find configurations with better PUF properties.

C8.4 15:40

A 55 MHz Integrated Crystal Oscillator with Chirp Injection Using a 28-nm Technology

Lantao Wang, Adrian Arnold, Jonas Meier, Markus Scholl, Ralf Wunderlich and Stefan Heinen, RWTH Aachen University, Germany.

This paper presents an integrated crystal oscillator to provide a 55 MHz reference frequency for applications such as phase-locked loops. The crystal oscillator uses a Pierce oscillator architecture and achieves a phase noise of -152 dBc/Hz at 1 kHz offset. A chirp frequency injection technique is also applied, achieving a start-up time of 300 us with 335 nJ energy consumption. The circuit is designed in a 28-nm technology, supplied by a 0.9 V voltage.

16:00 – 16:20 Coffee Break

16:20 Award Ceremony & Closing Session

PRIME Technical Sessions *14:40-16:00*

D6 Analog circuits and qubit interfaces

Chair: Lotte Geck, Forschungszentrum Jülich, Germany

D6.1 14:40

A Cryogenic High-Voltage Amplifier for Ion Traps

Michael Sieberer [1], Christoph Sandner [1] and Peter Hadley [2].

[1] Infineon Technologies, Villach, Austria. [2] Graz University of Technology, Austria.

Ion traps for quantum computers need high voltages to confine ions in an electrostatic potential. This work presents a high voltage current-feedback instrumentation amplifier, implemented in 130 nm-CMOS, that is fully functional at temperatures below 20 K and dissipates only 1.5 mW when powered with ±12 V. Since drain-extended MOS transistors cannot be used at cryogenic temperatures, high-voltage compliance is achieved by stacking low-voltage transistors. The high-frequency noise is below 8 nV/rt-Hz to avoid ion heating. Flicker noise and offset is reduced by chopping of the input gain stages.

D6.2 15:00

Cryogenic RF Transimpedance Amplifier in 22 nm SOI-CMOS for Control of a Qubit

Ricardo Heinen [1,2], Dennis Nielinger [1], Christian Grewing [1], Ralf Wunderlich [2] and Stefan Heinen [2].

[1] Forschungszentrum Jülich GmbH, Jülich, Germany. [2] RWTH Aachen University, Germany.

A cryogenic RF transimpedance amplifier (TIA) for signals around 20 GHz with millivolt amplitudes is presented in this paper. The TIA is part of an IC with a modulator system, where its primary application is to drive a semiconductor based spin qubit at temperatures around 100 mK. A 22 nm FDSOI CMOS technology is used for the circuit development. In post-layout simulations the TIA showed transimpedance magnitudes over 40 dBΩ and bandwidths larger than 1 GHz while dissipating less than 170 µW. Tuning options for the operating point and the frequency behavior where implemented to ensure functionality at cryogenic temperatures. The TIA performance allows to flip chip bond the modulator system in close vicinity to the qubit inside a dilution refrigerator. This setup can verify if the concept is feasible to upscale qubit numbers.

D6.3 15:20

A First Order-Curvature Compensation 5ppm/°C Low-Voltage & High PSR 65nm-CMOS Bandgap Reference with one-point 4-bits Trimming Resistor

Edoardo Barteselli [1], Luca Sant [2], Richard Gaggl [2] and Andrea Baschirotto [1].

[1] University of Milano - Bicocca, Italy. [2] Infineon Technologies, Villach, Austria.

Natural bandgaps produce 1.25V reference voltage that does not operate in low-voltage applications. This paper presents a current-mode bandgap reference circuit operating down to 1V supply (nominal = 1.2V) with low temperature coefficient, low power consumption, high Power-Supply-Rejection (PSR) and high performance robustness for industrial production in the consumer microphones field. The voltage reference is generated by the sum of two currents over a matched resistor: one current is proportional to VEB, the other one is proportional to VT. In 65nm node, a 600mV bandgap (BG) reference voltage consumes 5.2uW (4.3uA) at 1.2V supply. The simulated PSR is -91dB, -43dB and -29dB at DC, 1kHz and 10kHz respectively. Montecarlo simulations show a variation of 1% at 3sigma after 4-bits trimming over a temperature range between -40°C and 100°C without any high-order curvature compensation, performing 5ppm/°C temperature coefficient.

D6.4 15:40

Resource Efficient Sub-VT Level Shifter Circuit Design Using a Hybrid Topology in 28 nm

Saikat Chatterjee and Ulrich Rueckert, CITEC, Bielefeld University, Germany.

This paper presents a resource efficient level shifter circuit, which is capable of converting input voltages below subthreshold to above threshold voltages, making it suitable for ultra low power applications such as wireless sensor networks, biomedical implants, environmental sensors, to name a few. The proposed circuit topology has two stages. The first stage comprises of a Wilson current mirror, whereas the second stage has a cross coupled PMOS circuit. The two staged topology helps to overcome the challenges of deep nano process, when operated with ultra low input supply voltage. The circuit presented here, is implemented in 28nm FDSOI technology from ST Microelectronics. The proposed level shifter is capable of converting an input voltage as low as 150mV to 1V. The static power consumption is measured to be 100pW, when the circuit is operated with the minimum possible input supply and operational frequency of 500 kHz.

16:00 – 16:20 Coffee Break

16:20 Award Ceremony & Closing Session

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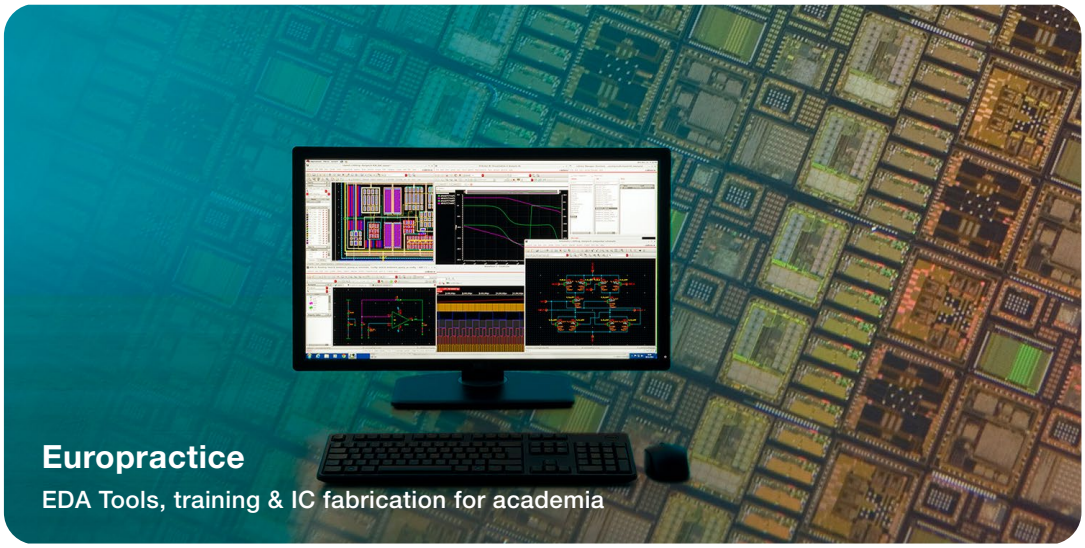

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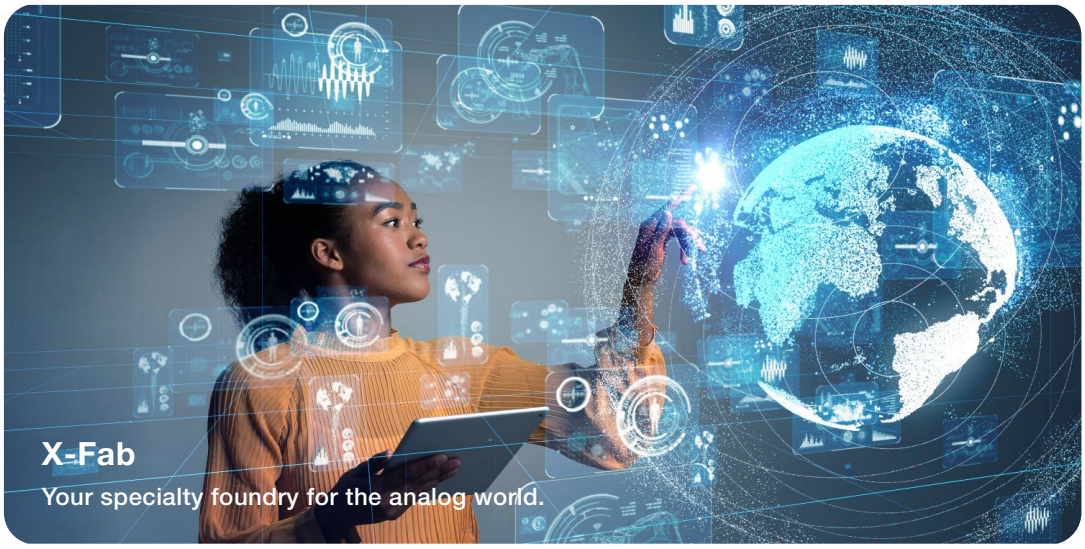

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