Nguyen Nguyen

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RESEARCH INTERESTS

My research interests lie at the intersection of low-power and energy-efficient integrated circuit design and advanced verification methodologies. I am particularly interested in exploring novel domain specific architectures that push the boundaries of energy efficient computation.

EDUCATION

University of Notre Dame | Notre Dame, IN — May 2026

Bachelor of Science, Electrical Engineering — *GPA: 3.623*

SKILLS

Verification: SystemVerilog (OOP, UVM), Bus Functional Models, Assertions, Constrained-Randomization, Coverage

Front-End Design: RTL Design (Verilog), Synthesis, STA

Back-End Design: Floorplanning, Place and Route, CTS, DRC, LVS

Automation & Scripting: C/C++, Python, Tcl, Shell, SKILL

Tools: Virtuoso, XCelium, VCS, Calibre, NC-Verilog, Vivado, ModelSim, Innovus, Genus, Stratus, KiCAD, Altium, LTSpice

EXPERIENCE

Research Assistant | Notre Dame, IN — May 2025 – Present

- Developed a UVM verification flow for ultra-low-power adiabatic MIPS processors, and implemented bus functional models with clock-phase-aware stimulus generation synced with adiabatic timing requirements.
- Implemented constrained-random and self-checking verification environment for block and system-level verification of adiabatic ALU achieving >95% functional coverage across key sequences.
- Built an automated verification infrastructure combining LLM-generated/feedbacked coverpoint writing with Python-based regression testing for post-processing and coverage reporting, significantly cutting setup time.

Research Assistant | Notre Dame, IN — August 2024 – April 2025

- Implemented reversible computing and logic principles such as Bennett clocking and split-rail charge recovery into 16-bit multicycle microarchitecture for MIPS ISA.
- Designed a library of standard cells for an adiabatic 16-bit MIPS microprocessor in SkyWater 90nm technology.
- Performed physical verification at partition level including scripting LVS batch runs with Shell and fixes with SKILL.

NDNano Undergraduate Research Fellow | Notre Dame, IN — January 2024 – August 2024

- Designed a test harness proof of concept on FPGA for post-silicon validation of adiabatic microprocessors.
- Developed a custom microprocessor-to-PC datapath, implementing an on-chip BRAM buffer and a UART transfer protocol, and PC-side data parsing and tabulation.

PROJECTS

Adiabatic GeMM Accelerator | Notre Dame, IN — May 2025 – August 2025

- Designed 4x4 adiabatic systolic array-based GeMM accelerator in SystemVerilog with Bfloat16 PEs and weight-stationary architecture for highly energy efficient matrix multiplication.
- Built an adiabatic scratchpad buffer to optimize input timing and results collection under adiabatic timing constraints, reducing active power dissipation by several orders of magnitude.

RNN Pick-up Line Generator | Notre Dame, IN May 2023 – July 2023

- Built a text-generating recurrent neural network using TensorFlow and a GRU architecture with multiple hidden layers and ~6 million parameters, trained on a dataset of over 10,000 graded pick-up lines.
- Optimized a deep learning model over 225 epochs by implementing regularization techniques like batch normalization, dropout, and L2 regularization, leading to a test loss of 1.7.
- Developed and trained a pick-up line classification model to score generated outputs in success percentage.

PUBLICATIONS

Presentations

- **Nguyen Nguyen**, "A UVM-Based Verification Approach for Adiabatic Microprocessors" NDNano Research Reviews, Notre Dame, IN, 2025.
- **Nguyen Nguyen**, "An FPGA-Based Test Harness for Post-Silicon Validation of an Adiabatic Microprocessor" NDNano Research Reviews, Notre Dame, IN, 2024.

TEACHING EXPERIENCE

Undergraduate Research Mentor | Notre Dame, IN August 2024 – Present

- Mentored multiple cohorts of 8+ undergrad students in digital IC design, accelerating their technical proficiency.
- Provided hands-on technical guidance in Design Verification flow, including testbench development, coverage analysis, and verification techniques.

RELATED COURSEWORK

EE 67062 Systems & Circuits for Machine Learning | Notre Dame, IN August 2025 – December 2025

- Developed a deep understanding of deep neural network (DNN), dataflow architectures, and the design of analog/mixed-signal and digital accelerators like the Google TPU.
- Analyzed and presented a paper on the role of hardware/software/model co-design in accelerating compressed ML models, focusing on how structured sparsity, quantization, and compiler optimizations enable efficient processing on specialized hardware.

High-Level Synthesis | Notre Dame, IN January 2025 – May 2025

- Proposed, designed, and verified a full-duplex UART controller in SystemC with baud rate control and error detection, completing the entire project lifecycle in just 2.5 weeks.
- Performed physical design including CTS and P&R using Cadence tools (Stratus, Genus, Innovus), exceeding all instructor PPA requirements and resulting in successful tapeout in TSMC 180nm technology.

Digital Integrated Circuits | Notre Dame, IN August 2024 – December 2024

- Designed a fan speed controller ASIC in Verilog with temperature sensor interface and multi-speed control logic.
- Synthesized the fan speed controller ASIC design using the eFabless digital chipIgnite flow in GF180nm technology, passing Multi-Project Wafer and Tapeout tests.

LICENSES AND CERTIFICATIONS

- Siemens SystemVerilog for Verification - v22.18

LEADERSHIP AND ACTIVITIES

- Strike Magazine Design Lead
- Chinese Cultural Society Merch Commissioner