

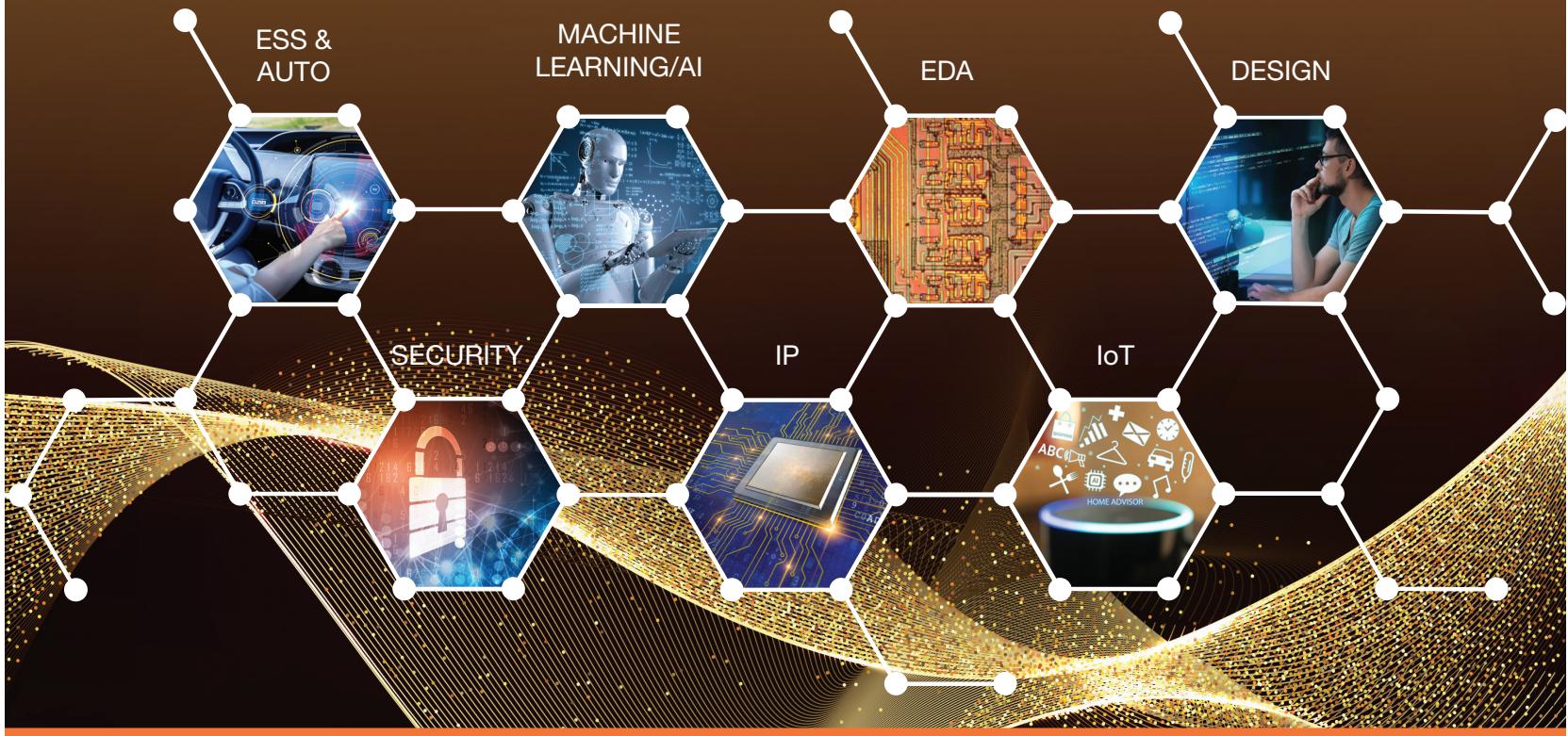


DESIGN AUTOMATION CONFERENCE

FROM CHIPS TO SYSTEMS – LEARN TODAY, CREATE TOMORROW

CONFERENCE PROGRAM & EXHIBITS GUIDE

JUNE 2-6, 2019 | LAS VEGAS, NV | LAS VEGAS CONVENTION CENTER



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GENERAL CHAIR'S WELCOME



Dear Colleagues,

Viva Las Vegas! Welcome to the 56th Design Automation Conference, back in town for the first time since 2001. Las Vegas bills itself as the entertainment capital of the world, and this week the city is also the design automation capital of the world!

DAC is a unique event that brings together the entire design and design automation ecosystem, from academic and industrial researchers, to designers, developers, vendors and educators. You're a part of that, so what should you do this week? Take advantage of DAC's unique character.

The DAC executive committee, along with the hundreds of volunteers who put the conference together, have once again brought you an excellent program with top quality research papers, great keynotes and invited talks, exciting panels, and valuable insights from design practitioners.

Beyond that, though, you should take advantage of all that DAC offers. Attend a presentation on a topic you don't know. DAC covers everything from emerging devices to cloud computing, so there's bound to be something. Find a new product or service. Ask questions. Attend our many social functions and meet up with old friends or make some new ones. And don't forget to take advantage of our location – there's always something going on in Las Vegas, and this week one of the highlights is DAC!

Enjoy the #56DAC!

Rob Aitken

ACM/SIGDA



IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION



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CONFERENCE INFORMATION

EXHIBIT HOURS

LOCATION: EXHIBIT HALLS N3 & N4

Monday, June 3	10:00am - 6:00pm
Tuesday, June 4	10:00am - 6:00pm
Wednesday, June 5	10:00am - 6:00pm

REGISTRATION HOURS

LOCATION: LAS VEGAS CONVENTION CENTER LEVEL 2

Friday, May 31 - Saturday June 1	8:00am - 6:00pm
Sunday, June 2 - Wednesday June 5	7:00am - 7:00pm
Thursday, June 6	7:00am - 5:00pm

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"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF).

All BOF meetings are held at the Las Vegas Convention Center Tuesday, June 4 from 7:00 - 8:30pm.

To arrange a BOF Meeting, please email Sophia Sun at sophia@dac.com

FIRST AID ROOM

First Aid and Security are located in the lobby area outside the DAC Exhibit Floor and have roving personnel around the entire perimeter of the facility. In case of emergencies dial from your phone 702-892-7400 which will connect you to the command center.

First Aid Room Hours:

Monday, June 3: 9:00am – 7:00pm

Tuesday, June 4: 9:00am – 7:00pm

Wednesday, June 5 : 9:00am – 6:00pm

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DAC NETWORKING OPPORTUNITIES

WELCOME RECEPTION

Sunday, June 2

6:00 - 7:30pm | Westgate Hotel - Ballroom A

Join fellow attendees for the first event to network and kick-off DAC 2019

NETWORKING RECEPTION

Monday, June 3

6:00 - 7:00pm | Exhibit Floor

Join us on the Exhibit Floor and enjoy snacks and beverages.

Thank you to our Reception Sponsor:



DESIGN INFRASTRUCTURE ALLEY RECEPTION

Monday, June 4

5:00 - 6:00pm | Design-on-Cloud Pavilion

Join us on the Exhibit Floor and enjoy snacks and beverages.

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Thank you to our Reception Sponsor:



NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Thank you to our Reception Sponsor:



Tuesday, June 4

6:00 - 7:00pm | Exhibit Floor

Join us on the Exhibit Floor to see Work-in-Progress posters and enjoy light snacks and beverages.

Wednesday, June 5

6:00 - 7:00pm | Level 2 Pre-Function Area

Join us in the Level 2 Lobby to see Work-in-Progress posters and enjoy light snacks and beverages.

Music courtesy of:



KEYNOTE PRESENTATIONS



KEYNOTE: SECURING THE BILLIONS OF DEVICES AROUND US

GALEN C. HUNT – *Distinguished Engineer and Managing Director - Microsoft Corporation, Redmond, WA*

Monday, June 3 | Time: 9:20 - 10:00am | Keynote Booth 1145

The next decade promises the democratization of connectivity to every device. Significant drops in the cost of connectivity mean that every form of electrical device—every child's toy, every household's appliances, and every DoD sensor—will become connected to the Internet. Tens of billions of these devices are controlled by microcontrollers, a class of device particularly ill-prepared for the security challenges of internet connectivity. What is required to secure these billions of devices? And, how can it be done economically enough to apply to every device? See page 18 for more details.



KEYNOTE: HORS D'OEUVRES FROM CHAOS

THOMAS DOLBY – *Musician, Producer & Innovator
- Johns Hopkins Univ., Baltimore, MD*

Tuesday, June 4 | 9:20 - 10:00am | Keynote Booth 1145

As a boy, what Thomas Dolby loved most about synthesizers was that (quote) “they did things I didn’t expect.” Just from fooling around with synths and samplers, never reading the owner’s manual (there was none!), he learned all that he knows about ‘real’ music and musical instruments. But his frustration today is that electronic music has not embraced the advances in AI and deep learning that are now become infused in filmmaking, videogames and virtual reality. Loops and samples, he says, are like “dumb Lego blocks that have no knowledge of each other”; yet schools of fish, murmurations of sparrows, and even world-class orchestral players watch and listen intently and make microsecond-grain, synaptic decisions, enabling them to think like a collective hive mind. Why then do synthesizers still have to behave like typewriters?

See page 30 for more details.



KEYNOTE: PRIORITIZING PLAY IN AN AUTOMATED AGE

JOHN COHN – *Massachusetts Institute of Technology & IBM Watson AI Lab, Cambridge, MA*

Wednesday, June 5 | 8:45 - 9:15am | Keynote Booth 1145

John Cohn is an IBM Fellow in the MIT-IBM Watson AI Research Group based in Cambridge, MA. John earned a BSEE at MIT, and a Ph.D in Computer Engineering from Carnegie Mellon University. He has authored more than 30 technical papers, contributed to four books and has more than 100 worldwide patents. In 2005 John was elected a Fellow of the IEEE.

John is active in education issues at a local, state and national level. He is so passionate about promoting STEM careers that he spent 59 days living and inventing in an abandoned steel mill as part of Discovery Channel’s technical survival show “The Colony”. John lives with his family in a restored 19th century schoolhouse in Jonesville Vermont and is eager to share his love of science and technology with anyone who will listen.

See page 54 for more details.

KEYNOTE PRESENTATIONS



KEYNOTE: FROM STUDENT PROJECT TO TACKLING THE MAJOR CHALLENGES IN REALIZING SAFE & SUSTAINABLE ELECTRIC VEHICLES

BAS VERKAIK – *Founder, SPIKE, Eindhoven, The Netherlands*

Wednesday, June 5 | 9:20 – 10:00am | Keynote Booth 1145

In 2014, a group of students from the Eindhoven University of Technology set a clear goal to ride around the world in 80 days on an electric motorcycle to show the world what electric vehicles were capable of. Since a suitable motorcycle to undertake such a tour didn't exist yet, the Dutch students decided to entirely develop it by themselves. A revolutionary vehicle was the result: 400 km range from a self-developed swappable and modular battery pack. After completing the 80-day world tour late 2016, the unique knowledge and experience gained in this project was made commercial by founding the spinoff SPIKE Technologies. SPIKE aims to accelerate the transition towards safe & clean mobility by designing & developing high quality powertrain components for electric vehicles. Among these components are SPIKE's battery solutions, that distinguish themselves due to their safety, performance and lifetime, while they can be produced very cost-efficiently due to their unique design. Until now, SPIKE has supported in the development of a wide variety of electric vehicles and recently established its own battery production facility in the Netherlands.

In his talk, Bas Verkaik will explain the complex design decisions that had to be made in developing the electric motorcycle and they now have to make every day to cope with the rapidly changing developments in the electric vehicle market.

See page 54 for more details.



KEYNOTE: REVERSE ENGINEERING VISUAL INTELLIGENCE

JAMES DICARLO, MD, PHD – *Massachusetts Institute of Technology, Cambridge, MA*

Thursday, June 6 | 9:20 – 10:00am | Room: N250

The brain and cognitive sciences are hard at work on a great scientific quest — to reverse engineer the human mind and its intelligent behavior. These fields are still in their infancy. Not surprisingly, forward engineering approaches that aim to emulate human intelligence (HI) in artificial systems (AI) are also still in their infancy. Yet the intelligence and cognitive flexibility apparent in human behavior are an existence proof that machines can be constructed to emulate and work alongside the human mind. And history suggests that these challenges of reverse engineering human intelligence will be solved by tightly combining the efforts of brain and cognitive scientists (hypothesis generation and data acquisition), and forward engineering aiming to emulate intelligent behavior (hypothesis instantiation and data prediction). As this approach discovers the correct neural network models, those models will not only encapsulate our understanding of complex brain systems, they will be the basis of next-generation computing and novel brain interfaces for therapeutic and augmentation goals (e.g., brain disorders).

In this session, I will focus on one aspect of human intelligence — visual object categorization and detection — and I will tell the story of how work in brain science, cognitive science and computer science converged to create deep neural networks that can support such tasks. These networks not only reach human performance for many images, but their internal workings are modeled after — and largely explain and predict — the internal workings of the primate visual system. Yet, the primate visual system (HI) still outperforms current generation artificial deep neural networks (AI), and I will show recent new clues that the brain and cognitive sciences can offer. More broadly, our species is at the beginning of its most important science and engineering quest — the quest to understand and emulate human intelligence — and I hope to motivate others to engage that frontier alongside us.

See page 75 for more details.

VISIONARY & SKY TALKS



VISIONARY TALK: GAME CHANGERS: HOW AUTOMATION HAS CHANGED THE GAMING INDUSTRY

Mark Yoseloff, Ph.D. — *Executive Director, UNLV Center for Gaming Innovation Univ. of Nevada, Las Vegas, NV*

Monday, June 3 | 9:00 – 9:20am | Keynote Booth 1145

Biography: Mark Yoseloff, Ph.D. is the Executive Director of the UNLV Center for Gaming Innovation. The Center is dedicated to teaching and mentoring the next generation of innovators in the gaming industry.

Dr. Yoseloff is the retired chairman of the board and CEO of Shuffle Master, Inc., a NASDAQ Global Markets Company. He is currently the CEO of High Roller Productions, LLC, the Managing Member of Well

Suited, LLC, a product creation company, and a Managing Member of Big Bet Gaming, LLC, a product distribution company

Dr. Yoseloff holds BA and MA degrees from the University of Pennsylvania and a doctorate in mathematics from Princeton University. He is the co-author of a college text entitled "Finite Mathematics" and holds well over 200 issued or pending patents throughout the world related to the gaming industry. See page 18 for more details.



SKY TALK: WHAT CAN EDA DO FOR QUANTUM COMPUTING AND WHAT CAN QC DO FOR EDA?

Leon Stok — *Vice President of IBM's Electronic Design Automation Group, Poughkeepsie, NY*

Monday, June 3 | 1:00 – 1:45pm | DAC Pavilion – Booth 871

Biography: Leon Stok is Vice President of IBM's Electronic Design Automation group. His team delivers world-class design

and verification flows and tools being used to design the world's largest supercomputers, IBM systemZ and Power systems. Prior to this he held positions as director of EDA and executive assistant to IBM's Senior Vice President of Technology and Intellectual Property and executive assistant to IBM's Senior Vice President of the Technology group. Leon Stok studied electrical engineering at Eindhoven University of Technology, the Netherlands, from which he graduated with honors in 1986. He obtained a Ph.D. degree from Eindhoven University in 1991. At IBM's Thomas J. Watson Research Center, Leon Stok pioneered logic synthesis, as part of the team that developed BooleDozer. Subsequently, he managed IBM's synthesis group and drove the first commercial application of physical synthesis by developing IBM's Placement Driven Synthesis tool. From

1999-2004 he led all of IBM's design automation research as the Senior Manager Design Automation at IBM Research. He drove key innovations in DFM using RRR (Radically Restrictive Rules) in static timing analysis using statistical timing and in large block physical synthesis. Dr. Stok has presented over sixty keynotes, invited talks and tutorials at major IEEE and ACM conferences worldwide and at many leading universities. Dr. Stok has published over sixty papers on many aspects of high level, architectural and logic synthesis, low power design, placement driven synthesis and on the automatic placement and routing for schematic diagrams. He holds 13 patents in EDA. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms. See page 20 for more details.

VISIONARY & SKY TALKS



SKY TALK: MARCH OF THE MACHINES – BUILDING ETHICAL AI

Carolyn Herzog – Arm, Ltd., San Jose, CA

Tuesday, June 4 | 1:00 – 1:45pm | DAC Pavilion – Booth 871

Biography: Carolyn Herzog has over 20 years of global business and legal experience. She has extensive expertise in cybersecurity and privacy, ethics and compliance, corporate governance, regulatory compliance, crisis management, stakeholder engagement, and strategic planning.

Carolyn is the Executive Vice President, General Counsel, Corporate Secretary and Chief Compliance Officer at Arm, the world's leading semiconductor IP company. At Arm, Carolyn leads a team of legal and public affairs professionals, and is responsible for all legal matters in the company. Prior to joining Arm, Carolyn was the VP, Chief Compliance Officer and Deputy General Counsel at Symantec Corporation, the global leader in cybersecurity, based in the company's headquarters in Mountain View, California. She held various roles at Symantec, leading the company through significant transformation in 3 major offices. Carolyn was instrumental in leading numerous acquisition integrations for Symantec and, notably, the company's sale of Veritas in 2016, creating a separate,

privately held company. As Head of Legal for the Europe, Middle East and Africa region, Carolyn was based in Symantec's European headquarters in the U.K. She joined Symantec through the AXENT Technologies acquisition in December 2000, where she successfully led the public company acquisition of AXENT by Symantec, as General Counsel. Carolyn had been based in the Washington DC area prior to moving to the UK, having worked in the international development arena, both in the non-profit sector and with The World Bank.

Carolyn has served on the European Board of the Association of Corporate Counsel, the Board for the National Cyber Security Alliance, and is an Advisory Board member to IPWatch System Corporation. She has been recognized as a Distinguished General Counsel by the Director's Roundtable, and an Attorneys Who Matter by Ethisphere Magazine.

Carolyn graduated from the University of Wisconsin, Madison with a JD and received her B.A. from Washington University in St. Louis. See page 38 for more details.



SKY TALK: THE MEMORY FUTURES

Gurtej S. Sandhu – Micron Technology, Inc., Boise, ID

Wednesday, June 5 | 1:00 – 1:45pm | DAC Pavilion – Booth 871

Biography: Gurtej Sandhu is Senior Fellow and Vice President at Micron Technology. In his current role, he is responsible for Micron's end-to-end R&D technology roadmaps and to drive cross-functional alignment across various departments and business units to proactively identify technology gaps and managing the engineering organization to resource and execute on developing innovative technology solutions for future memory scaling. Dr. Sandhu's responsibilities include leading several internal project teams worldwide and managing interactions with research consortia around the world. He has held several engineering and management roles and is actively involved with a broad range of process technologies for IC processing and has pioneered several process

technologies currently employed in mainstream semiconductor chip manufacturing.

Dr. Sandhu received a degree in electrical engineering at the Indian Institute of Technology, New Delhi, and a Ph.D. in physics at the University of North Carolina, Chapel Hill, in 1990. He holds over 1,300 U.S. patents and is recognized as one of the top inventors in the world. A Fellow of IEEE, he received the prestigious IEEE Andrew S. Grove Award in 2018 for outstanding contributions to solid-state devices and materials technology, as well as for leadership, originality, breadth, among other achievements. This competitive award is presented annually by the IEEE Board of Directors to an individual with pioneering achievements to the semiconductor technology. See page 60 for more details.

IN MEMORY

Joe Daniels | 1959 - 2018



The EDA industry suffered a tremendous loss with the sudden passing of Joe Daniels in November, 2018. Many of us crossed paths with him in some way or another during the nearly 40 years he spent as a consultant, technical writer and editor in the industry. Most of his contributions were in project development, coordination, and software and hardware technical writing and editing. He consulted with many companies and organizations in the industry over the years, and had long-standing relationships with the IEEE-Standards Association and Accellera Systems Initiative. He touched many of the standards in use today, as well as many currently in development, with his admirable editing skills for technical content, consistency, style, and formatting. Joe was involved in editing and documenting more than 20 standards including ALF, DPCS, IP-XACT, SystemC-AMS, SystemVerilog, UVM, Verilog, PSS, SCE-MI, SystemC CCI, just to name a few. We are fortunate to have known Joe and to be the beneficiaries of his many contributions to the EDA community.

Chuck Grindstaff, Siemens | 1957 - 2018



Former Siemens' PLM chief, Chuck Grindstaff passed away suddenly on Tuesday, October 23, 2018, at the age of 61. He won an Oscar award in 2004 for contributions to the evolution of digital audio editing technology. He presented a keynote at the 54th DAC in 2017. Chuck is a highly skilled PLM expert and left a permanent footprint in our industry. His humility, and his ability to listen and produce concise analyses serve as exemplary characteristics for all of us.

Stuart Sutherland | 1953 - 2018



Stuart Sutherland passed away the summer of 2018, shortly after DAC. Stu was known as the wizard and consultant in SystemVerilog and UVM Training. He was the president of Sutherland HDL, Inc., with over 25 years of experience as a world expert and educator in hardware design language. In addition to being a key technical contributor to the IEEE 1364 and IEEE 1800 standards, he was a technical editor in merging 1364 and SystemVerilog 3.0 from Accellera into IEEE 1800. The word "Herculean" might come close to describing his work. His efforts continued as editor through the most recent release of IEEE 1800. Stu was one of the premier independent Verilog educators in our industry as well as a prolific author of books and technical papers. He is the author of numerous papers and books which have left a marked technical legacy in his field. Stuart is survived by his wife of 37 years and their five children as well as ten grandchildren. He will be greatly missed but never forgotten.

2019 AWARDS

The 56th DAC will recognize success and excellence for the following individuals in the field of design automation of electronic systems.

2018 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ELECTRONIC SYSTEMS DESIGN

Thomas W. Williams, Consultant, Synopsys (retired), Synopsys Fellow

For Overall Impact on Electronics Industry through Contributions to Scan Design for Testability, Related Test Automation

ACM IEEE A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Edward B. Eichelberger, IBM (retired) IBM Fellow, IEEE Fellow
Thomas W. Williams, Consultant, Synopsys (retired), Synopsys Fellow

For the paper "A Logic Design Structure for LSI Testability," In Proc. of the 14th Design Automation Conference, 1977

2019 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

Iris Bahar - Professor of Engineering and Computer Science, Brown Univ.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Gia Douglass

DAC UNDER-40 INNOVATORS AWARD

The Under-40 Innovators Award is sponsored by Association for Computing Machinery (ACM), and the Institute of Electrical and Electronics Engineers (IEEE). The award will recognize the top five young innovators (nominees should be 40 years or younger in age as of June 1, 2019) who are movers and shakers in the field of design and automation of electronics.

SYSTEM DESIGN CONTEST WINNERS

HACK@DAC WINNERS

CEDA HONORS LAURENCE NAGEL FOR THE DONALD O. PEDERSON SOLID-STATE CIRCUITS AWARD AS KEY CONTRIBUTOR TO THE SPICE SIMULATOR CREATION

Laurence W. Nagel, President, Omega Enterprises Consulting

IEEE CEDA OUTSTANDING SERVICE AWARD

X. Sharon Hu, University of Notre Dame

For outstanding service to the EDA community as DAC General Chair in 2018.

IEEE FELLOW

Deming Chen, University of Illinois at Urbana- Champaign

For contributions to FPGA high-level synthesis

IEEE FELLOW

Hai (Helen) Li, Duke University

For contributions to neuromorphic computing system

IEEE FELLOW

Farinaz Koushanfar, University of California, San Diego

For contributions to hardware and embedded systems security, and to privacy-preserving computing

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

To Be Announced

2019 ACM TODAES BEST PAPER AWARD

Philipp Mundhenk, Andrew Paverd, Artur Mrowca, Sebastian Steinhorst, Martin Lukasiewycz, Suhaib A. Fahmy, and Samarjit Chakraborty,

"Security in Automotive Networks: Lightweight Authentication and Authorization," ACM Trans. Des. Autom. Electron. Syst. 22, 2, Article 25 (March 2017), 27 pages. DOI: <https://doi.org/10.1145/2960407>

ACM SIGDA DISTINGUISHED SERVICE AWARD

To Be Announced

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Jeyavijayan (JV) Rajendran, Texas A&M University

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

"Distributed Timing Analysis"

By Tsung-Wei Huang, Advisor: Martin D. F. Wong, University of Illinois at Urbana-Champaign

BEST RESEARCH PAPER NOMINEES

11.1 - Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search

Weiwen Jiang, Xinyi Zhang, Edwin Sha, Lei Yang, Qingfeng Zhuge, Yiyu Shi, Jingtong Hu
(see page 32)

31.1 - BRIC: Locality-based Encoding for Energy-Efficient Brain-Inspired Hyperdimensional Computing

Mohsen Imani, Justin L. Morris, John Messerly, Helen Shu, Yaobang Deng, Tajana Rosing
(see page 44)

40.1 - A 1.17 TOPS/W, 150fps Accelerator for Multi-face Detection and Alignment

Huiyu Mo, Leibo Liu, Wenping Zhu, Qiang Li, Hong Liu, Wenjing Hu, Yao Wang, Shaojun Wei
(see page 55)

51.2 - LithoGAN: End-to-end Lithography Modeling with Generative Adversarial Networks

Stephan Wei Ye, Mohamed Baker Alawieh, Yibo Lin, David Z. Pan
(see page 61)

54.1 - DREAMPlace: Deep Learning Toolkit-enabled GPU Acceleration for Modern VLSI Placement

Yibo Lin, Shounak Dhar, Wuxi Li, Haoxing Ren, Brucek Khailany, David Z. Pan
(see page 63)

DAC PAVILION - BOOTH 871



Thank you to our DAC Pavilion Sponsor:

Monday, June 3

FUNDAMENTAL SHIFTS IN THE ELECTRONICS ECOSYSTEM

Date: Monday, June 3 | Time: 10:30 - 11:15am | DAC Pavilion - Booth 871

SPEAKER:

Wally Rhines - Mentor, A Siemens Business, Wilsonville, OR

STRAIGHT TALK WITH TONY HEMMELGARN, SIEMENS DIGITAL INDUSTRIES SOFTWARE CEO

Date: Monday, June 3 | Time: 11:30am - 12:00pm | DAC Pavilion - Booth 871

MODERATOR:

Ed Sperling - Semiconductor Engineering, San Jose, CA

HEY ALEXA, WHO SHOULD I TALK TO ABOUT IMPLEMENTING LOW-POWER, ALWAYS-ON WAKE-UP APPLICATIONS?

Date: Monday, June 3 | Time: 2:00 - 2:45pm | DAC Pavilion - Booth 871

Event Type: DAC Pavilion | Keywords: IoT, Low Power, Emerging Technologies

Topic Area: Design, Embedded Systems & Software (ESS)

MODERATOR:

Brian Fuller - Arm, Ltd., San Jose, CA

ORGANIZER:

Jan Willis - Calibra Consulting, Menlo Park, CA

YOUNG UNDER 40 INNOVATORS AWARD PANEL

Date: Monday, June 3 | Time: 3:00 - 3:45pm | DAC Pavilion - Booth 871

MODERATOR:

Junko Yoshida - EE Times, Manhasset, NY

ORGANIZER:

Michelle Clancy - Cayenne Communication, Sunnyvale, CA

Topic of Discussion: Quantum Computing, AI and IOT: what do they have in common?

Please join EE Times editor Junko Yoshida for a lively discussion with the recipients of the 2019 Young Under 40 Innovator Award. Panelist will discuss the commonality between quantum computing, AI and IoT. The winners of the Young under 40 Innovators Award will be announced on Monday, June 3 during the opening session in the Keynote ballroom on the exhibition floor.

DAC BINGO

Date: Monday, June 3 | Time: 4:30 - 5:00pm | DAC Pavilion - Booth 871

Tuesday, June 4

THE STATE OF EDA: A VIEW FROM WALL STREET

Date: Tuesday, June 4 | Time: 10:30 - 11:15am | DAC Pavilion - Booth 871

SPEAKER:

Jay Vleeschhouwer - Griffin Securities, Inc., New York, NY

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud



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MYTH VS. REALITY: WHAT 5G IS SUPPOSED TO BE, AND WHAT IT WILL TAKE TO GET THERE

Date: Tuesday, June 4 || Time: 11:30am - 12:00pm || DAC Pavilion - Booth 871

MODERATOR:

Ed Sperling - Semiconductor Engineering, San Jose, CA

INCORPORATION OF SECURITY INTO CHIP DESIGN (DARPA)

Date: Tuesday, June 4 || Time: 2:00 - 2:45pm || DAC Pavilion - Booth 871

Keywords: Security & Privacy

SPEAKER: Serge Leef - Defense Advanced Research Projects Agency, Wilsonville, OR

ML/DL/AI FOR EDA: A MYTH OR A REALITY?

Date: Tuesday, June 4 || Time: 3:00 - 3:45pm || DAC Pavilion - Booth 871

Keywords: Implementation, Emerging Technologies || Topic Area: Design, EDA

MODERATOR:

Dr. Prith Banerjee - ANSYS, Inc., San Jose, CA

ORGANIZER:

Vic Kulkarni - ANSYS, Inc., San Jose, CA

DAC BINGO

Date: Tuesday, June 4 || Time: 4:30 - 5:00pm || DAC Pavilion - Booth 871

Wednesday, June 5

DEEP LEARNING MEETS SILICON - A PROGRESS REPORT ON TECHNOLOGY, APPLICATIONS, STARTUPS AND CHALLENGES

Date: Wednesday, June 5 || Time: 10:30 - 11:15am || DAC Pavilion - Booth 871

SPEAKER: Chris Rowen - Babblelabs, Inc., San Jose, CA

ELECTRONICS INNOVATION'S GREAT LEAP FORWARD: AN OVERVIEW OF THE JUMP PROGRAM

Date: Wednesday, June 5 || Time: 11:30am - 12:00pm || DAC Pavilion - Booth 871

ORGANIZER: Anand Raghunathan - Purdue Univ., Fort Wayne, IN

RISC-V OPPORTUNITIES AND CHALLENGES IN AN "OPEN" TECHNOLOGY SOCIETY

Date: Wednesday, June 5 || Time: 2:00 - 2:45pm || DAC Pavilion - Booth 871

MODERATOR: Ed Sperling - Semi Engineering

HACK@DAC - LIVE DEMO/MIRAI ATTACK

Date: Wednesday, June 5 || Time: 3:00 - 5:00pm || DAC Pavilion - Booth 871

ORGANIZER: Ahmad Reza Sadeghi - Technische Univ. Darmstadt

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

SUNDAY, JUNE 2

W1

WORKSHOP 1: STORAGE PROFILING, CONTAINERIZATION AND CLOUD FOR EDA

Time: 8:00am - 5:00pm || Room: N253 || Event Type: Workshop

Keywords: Emerging Technologies || Topic Area: EDA

ORGANIZER:

Derek Magill - *The Association of High Performance Computing Professionals, Austin, TX*

New and exciting IT infrastructure technologies are widely gaining adoption outside of EDA. This workshop focuses on some core capabilities needed by EDA companies in order to begin to embrace these new technologies. In this day-long course, we will cover:

Storage Profiling utilizing Ellexus (90 minutes)

- Tracing application dependencies in detail to provide a bill of materials showing all the locations a flow requires in order to run
- Collecting system-wide telemetry on storage performance of the above flow
- Finding applications that have I/O problems or what type of I/O patterns are likely to cause problems

How to size storage for Cloud for huge cost savings using Singularity Containers (90 minutes)

- Introduction to containers and Singularity containers specifically
- Performance and security considerations when selecting a container technology

- How to containerize an application for portability using Singularity EDA on AWS (60 minutes)

Running Scale-Out Engineering Workloads on the Cloud using Rescale (120 minutes)

- The attraction of running engineering workloads on the cloud is the promise of scale. However, running workloads at scale securely in the cloud often requires complicated set-up and development.
- This workshop will cover how to set-up and run a scale-out engineering workload on Rescale's turnkey platform.
- We will review how to monitor the job progress, set limits and budgets, and review results.

**Registered attendees are requested to bring their laptops to this workshop

SPEAKERS:

Rosemary Francis - *Ellexus, Cambridge, United Kingdom*

Gregory Kurtzer - *Sylabs.io, San Francisco, CA*

Richard Paw - *Rescale, Inc., San Francisco, CA*

Riaz Liyakath - *Rescale, Inc., San Francisco, CA*

W2

WORKSHOP 2: CEDA WORKSHOP ON CAD FOR SAFE AND SECURE ELECTRONIC SYSTEM DESIGN

Time: 8:00am - 5:00pm || Room: N255 || Event Type: Workshop

Keywords: Architecture & System Design, Test/Manufacturing/Reliability/Safety

Topic Area: Embedded Systems & Software (ESS), Security

ORGANIZERS:

Francesco Regazzoni - *Univ. of Lugano, Switzerland*

Marilyn Wolf - *Georgia Institute of Technology, Atlanta, GA*

Safe and secure electronic systems have become an important priority for industry, government, and consumers. Cyber-physical systems and Internet-of-Things (IoT) systems rely on safe and secure electronic systems. These systems are only as secure as the CAD tools used to create them. This workshop will explore the requirements on CAD systems for safety and security and the methodologies and algorithms required to satisfy these requirements.

Both the goals of safety/security and the best techniques to achieve these goals are rapidly evolving. Standards and certification are two complementary mechanisms for safe and secure system design.

Standards provide both goals and processes; certification is a regulatory process that is used in some domains. Externally-defined safety/security goals for CAD tools are relatively new; methodologies and algorithms to produce and use these tools are still evolving.

The workshop will draft a report identifying goals and research issues.

Topics of interest to the workshop include but are not limited to:

- Certification and validation of CAD tools.
- Secure design flows and design information integrity.
- Integrity of intellectual property.
- Attack models on electronic system hardware and software.
- CAD to secure against side channel attacks.
- Implications of existing security and safety standards on CAD.
- Embedded software design for safe and secure systems.
- Design of privacy-ensuring systems.
- Safe and secure CAD for cyber-physical control systems.
- Safe and secure CAD for wide-area IoT systems.

Participants may submit a 1-page white paper to wolf@ece.gatech.edu for participation as a poster and five-minute presentation.

SPEAKERS:

Marilyn Wolf - *Georgia Institute of Technology, Atlanta, GA*

Francesco Regazzoni - *Univ. of Lugano, Switzerland*

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

W3

WORKSHOP 3: GRAND CHALLENGES AND RESEARCH TOOLS FOR QUANTUM COMPUTING

Time: 8:00am - 12:00pm | **Room:** N257 | **Event Type:** Workshop | **Keywords:** Architecture & System Design, Emerging Technologies, Verification/Validation | **Topic Area:** Design, EDA

ORGANIZERS:

Diana Franklin - Univ. of Chicago, IL
Ali Javadi-Abhari - IBM T.J. Watson Research Center, White Plain, NY

We offer this workshop to grow an urgently needed community of computer science researchers for quantum computing. Speakers will be a combination of PIs from the EPiQC project, an NSF Expedition in computing, and researchers from IBM's quantum computing group. We will introduce and discuss areas of research in quantum computing where computer science contribution is most needed. We will also introduce an

end-to-end infrastructure for conducting quantum computing research based upon EPiQC's Scaffold tools and IBM's Qiskit tools. Participants will have the opportunity to run code on IBM's real quantum hardware through their cloud service, which will be exclusively reserved for the duration of the workshop.

SPEAKERS:

Diana Franklin - Univ. of Chicago, IL
Ali Javadi-Abhari - IBM T.J. Watson Research Center, White Plain, NY

W4

WORKSHOP 4: THE FOURTH INTERNATIONAL WORKSHOP ON DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS (DACP)

Time: 8:00am - 5:00pm | **Room:** N261 | **Event Type:** Workshop | **Keywords:** IoT, Automotive, Security & Privacy | **Topic Area:** Embedded Systems & Software (ESS), EDA

CHAIR:

Mohammad Al Faruque - Univ. of California, Irvine, CA

CO-CHAIR:

Chung-Wei Lin - National Taiwan Univ., Taiwan

ORGANIZERS:

Miroslav Pajic - Duke Univ., Durham, SC
Shiyan Hu - Michigan Technological Univ., Houghton, MI
Xin Li - Duke Univ., Durham, NC
Sandip Ray - Univ. of Florida, Gainesville, FL
Bei Yu - Chinese Univ. of Hong Kong
Umit Ogras - Arizona State Univ., Tempe, AZ
Huafeng Yu - Boeing, Ladson, SC
Qi Zhu - Northwestern Univ., Evanston, IL
Yier Jin - Univ. of Florida, Gainesville, FL
Bei Yu - Chinese Univ. of Hong Kong
Paul Bogdan - Univ. of Southern California, Los Angeles, CA
Phillip Brisk - Univ. of California, Riverside, CA
Dip Goswami - Eindhoven Univ. of Technology, Netherlands Antilles

Cyber-Physical Systems (CPS) are characterized by the strong interactions between cyber and physical components. CPS system examples include automotive and transportation systems, avionics systems, smart home, building and community, smart battery and energy systems, robotic systems, cyber-physical biochip, wearable devices, and so on. Due to the deeply complex intertwining among different components, CPS designs pose fundamental challenges in multiple aspects such as safety, performance, security, reliability, fault tolerance, extensibility, and energy consumption. Developing innovative design automation techniques, algorithms and tools is imperative to address the unique challenges in CPS design and operation, such as the fast increase of system scale and complexity, the close interactions with dynamic physical environment and human activities, the significant uncertainties in sensor readings,

the employment of distributed architectural platforms, and the tight resource and timing constraints. This workshop will present the state-of-the-art research results on the topic of design automation for CPS/IoT systems, introduce practical challenges and promising solutions in various industry sectors, and stimulate CAD researchers to participate in the interdisciplinary CPS/IoT research. In addition to the regular submissions, this workshop will also seek invited submissions/talks from high-profile experts in both academia and industry.

SPEAKERS:

Sanjit Seshia - Univ. of California, Berkeley, CA
Arquimedes Canedo - Siemens Corp., Princeton, NJ
Sukamo Mertoguno - Office of Naval Research, Scotts Valley, CA
Valeriy Sukharev - Mentor, A Siemens Business, Fremont, CA
Umit Ogras - Arizona State Univ., Tempe, AZ
Bei Yu - Chinese Univ. of Hong Kong
Xun Jiao - Villanova Univ., Villanova, PA
Wanli Chang - Univ. of York, United Kingdom
Pierluigi Nuzzo - Univ. of Southern California, Los Angeles, CA
Houssam Abbas - Oregon State Univ., Corvallis, OR
Francesco Regazzoni - Univ. of Lugano, Advanced Learning and Research Institute, Switzerland
Shivam Bhasin - Nanyang Technological Univ., Singapore
Miroslav Pajic - Duke Univ., Durham, SC
Muhammad Shafique - Technische Univ. Wien, Austria
Sandip Ray - Univ. of Florida, Gainesville, FL
Phillip Brisk - Univ. of California, Riverside, CA
Yier Jin - Univ. of Florida, Gainesville, FL

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

W5

WORKSHOP 5: BRIDGING THE GAP BETWEEN ARTIFICIAL TO NATURAL INTELLIGENCE

Time: 8:30am - 5:00pm | **Room:** N259 | **Event Type:** Workshop

Keywords: Architecture & System Design, Emerging Technologies, Analog & Mixed Signal | **Topic Area:** Machine Learning/AI, Design

ORGANIZERS:

Jae-sun Seo - Arizona State Univ., Tempe, AZ

Arijit Raychowdhury - Georgia Institute of Technology, Atlanta, GA

Despite tremendous progress in recent deep learning algorithms and hardware, there still exists three to four orders of energy efficiency gap between artificial and natural intelligence. Towards bringing this gap, up-to-date results of neuroscience needs to be abstracted to the algorithmic level, so that they can be implemented in engineering solutions. Based on understanding how the brain works, engineers from various disciplines need to collaborate on learning algorithms, knowledge representation, and architectures.

The objective of this workshop is to bring together researchers from across the JUMP (Joint University Microelectronics Program, funded by SRC and DARPA) community to discuss the most promising approaches towards the overarching goal of bridging the energy efficiency gap between artificial and natural intelligence. The workshop will explicitly focus on approaches that are well beyond today's deep neural networks and neural network accelerators.

Topics of interest will include bio-inspired network models and learning algorithms, neuro-mimetic devices and circuits, and hardware that embodies the information processing principles of the brain. Exemplary research efforts from both academia and industry will be presented. The workshop aims to establish a forum to discuss the current practices, as well as future research needs in the corresponding fields.

SPEAKERS:

Kaushik Roy - Purdue Univ., West Lafayette, IN

Laurent Itti - Univ. of Southern California, Los Angeles, CA

David Brooks - Harvard Univ., Cambridge, MA

Mike Davies - Intel Corp., Hillsboro, OR

Anand Raghunathan - Purdue Univ., West Lafayette, IN

Jae-sun Seo - Arizona State Univ., Tempe, AZ

Shimeng Yu - Georgia Institute of Technology, Atlanta, GA

Arijit Raychowdhury - Georgia Institute of Technology, Atlanta, GA

Geoffrey Burr - IBM Research, San Jose, CA

Suman Datta - Univ. of Notre Dame, Notre Dame, IN

W6

WORKSHOP 6: NIM - WORKSHOP ON NEAR- AND IN-MEMORY COMPUTING TRENDS

Time: 1:00 - 5:00pm | **Room:** N257 | **Event Type:** Workshop

Keywords: Emerging Technologies | **Topic Area:** Design, Machine Learning/AI

ORGANIZERS:

Valeria Bertacco - Univ. of Michigan, Ann Arbor, MI

David Brooks - Harvard Univ., Cambridge, MA

Near- and in-memory computing approaches are under intense exploration by researchers at the device, circuit, and architecture levels. This workshop will engage academic and industrialist to discuss current solutions, their applications and future trends in this space. The research span is quite broad covering a variety of topics and approaches. Because of the breadth of the research approach and the need to span multiple

layers of the technology stack, researchers at different levels often have difficulty comparing their approaches with others. The proposed workshop will bring together experts from multiple levels of the design stack, multiple institutions, and semiconductor companies to discuss a path forward in establishing the viability of in- and near-memory computing solutions over the next decade.

SPEAKERS:

Valeria Bertacco - Univ. of Michigan, Ann Arbor, MI

David Brooks - Harvard Univ., Cambridge, MA

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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SUNDAY, JUNE 2

DESIGN AUTOMATION SUMMER SCHOOL

Time: 7:30am - 6:00pm || Room: N250 || Event Type: Additional Meeting

Keywords: Architecture & System Design || Topic Area: EDA

The Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2019 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC. All the students receiving the fellowship (excluding the mentors) are required to attend DASS event.

For additional details go to: <http://www.sigda.org/dass>

Thank you to our Sponsors:



A. RICHARD NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Time: 7:30 - 9:00am || Room: N250 || Event Type: Additional Meeting

Topic Area: EDA

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation

Sunday, June 2

7:30 - 9:00am

Room: N250

Dr. Tom Williams Talk

Monday, June 3

3:00 - 4:00pm

Room: N249

Poster Presentation (colocated with the Ph.D. Forum)

Tuesday, June 4

7:00 - 9:00pm

Room: N246

Closing Session and Award Ceremony

Thursday, June 6

6:00 - 6:45pm

Room: N259

Thank you to our Corporate Sponsor:



ACM SIGDA/IEEE CEDA EARLY CAREER WORKSHOP AT DAC

Time: 8:30am - 6:00pm || Room: N254 || Event Type: Additional Meeting

Topic Area: Design, EDA

This workshop is for young and mid-career faculty and professionals in the fields related to electronic design automation (EDA). The workshop will start in the morning with an interactive session borrowing techniques from IMPROV to help you improve your soft skills (interpersonal, communication etc.) with others. This is followed by presentations and panel discussions by professionals discussing diverse topics such as navigating the various challenges to better succeed and thrive in your academic or industry

job, getting your projects funded and climbing academic and technical ladders, as well as improved cooperation between industry and academia research and development. In addition, the workshop will provide rich opportunities to closely interact and network with some of the established academicians, professionals, and funding officers in EDA related fields.

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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SUNDAY, JUNE 2

HACK@DAC FINAL COMPETITION

Time: 8:00am - 5:00pm | **Room:** N256 | **Event Type:** Additional Meeting

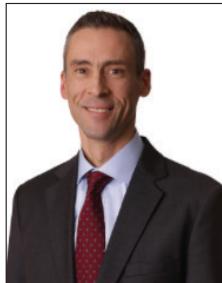
Keywords: Architecture & System Design, Contest | **Topic Area:** Security, Design

System-on-a-Chip (SoC) designers use third-party intellectual property (3PIP) cores and in-house IP cores to design SoCs. Trustworthiness of SoCs can be undermined by security bugs that are unintentionally introduced during the integration of the IPs. A security weakness, if discovered and exploited when the chips are in the field, can result in a compromise or bypass of one or more product security objectives. For example, an exploited security bug may lead to a deadlock or failure of the system, or create a backdoor through which an attacker can gain remote access to leak secrets from the system. The goal of this competition is to develop tools and methods for identifying security vulnerabilities in buggy SoCs.

In this 33-hour ordeal, the top scoring teams from phase I of the competition will compete live to find and report security bugs from an SoC that is released to them at the start of the day. These teams mimic the role of a security research team at the SoC integrator, as try to find the security vulnerabilities and report them back to the design team quickly, so they can be addressed before the SoC goes to market. The bug submissions from the participating teams are scored in real time by an expert team from industry and academia.

EDA OBSERVATIONS AND OUTLOOK: A WALL STREET PERSPECTIVE

Date: Sunday, June 2 | **Time:** 5:30 - 6:00pm | **Room:** Westgate Hotel - Ballroom B
Event Type: Additional Meeting



Richard F. Valera - Managing Director, Equity Research
Needham & Company,
New York, NY

This talk will explore the design software industry from the perspective of a Wall St. analyst.

Topics covered will include industry consolidation, growth rates, vertical market drivers, investment and public company stock performance.

WELCOME RECEPTION

Sunday, June 2

6:00 - 7:30pm | Westgate Hotel - Ballroom A

Join fellow attendees for the first event to network and kick-off DAC 2019

Music courtesy of:

methodics™

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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MONDAY, JUNE 3

OPENING SESSION & AWARDS PRESENTATION

Time: 8:45 - 9:00am | Keynote Booth 1145

Join us as we set the stage for the 56th DAC! DAC's Executive Committee will highlight the conference's events, and the award presentations will recognize success and excellence for individuals in the field of design automation of electronic systems.

2018 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ELECTRIC SYSTEMS DESIGN

Thomas W. Williams, Consultant, Synopsys (retired), Synopsys Fellow

For Overall Impact on Electronics Industry through Contributions to Scan Design for Testability, Related Test Automation

ACM IEEE A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

**Edward B. Eichelberger, IBM (retired) IBM Fellow, IEEE Fellow
Thomas W. Williams, Consultant, Synopsys (retired), Synopsys Fellow**

For the paper "A Logic Design Structure for LSI Testability," In Proc. of the 14th Design Automation Conference, 1977

2019 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

Iris Bahar - Professor of Engineering and Computer Science, Brown Univ.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Gia Douglass

DAC UNDER-40 INNOVATORS AWARD

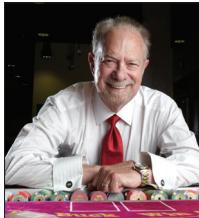
The Under-40 Innovators Award is sponsored by Association for Computing Machinery (ACM), and the Institute of Electrical and Electronics Engineers (IEEE). The award will recognize the top five young innovators (nominees should be 40 years or younger in age as of June 1, 2019) who are movers and shakers in the field of design and automation of electronics.

SYSTEM DESIGN CONTEST WINNERS

HACK@DAC WINNERS

VISIONARY TALK: GAME CHANGERS: HOW AUTOMATION HAS CHANGED THE GAMING INDUSTRY

Monday, June 3 | 9:00 – 9:20am | Keynote Booth 1145



In the last 30 years, automation has changed the operation of casinos to a greater extent than in the 3,000 year history of the industry. Beginning with a quick overview of what constitutes innovation, two very important examples of the application of automation to the industry will be given. These two innovations alone account for multi-billion dollar increases in revenue. Finally, several of

the latest trends in gaming innovation will be presented, with an open invitation to the audience to explore the application of automation in these areas.

SPEAKER:

Mark Yoseloff, Ph.D. - Executive Director, UNLV Center for Gaming Innovation, Univ. of Nevada, Nevada Las Vegas

KEYNOTE: SECURING THE BILLIONS OF DEVICES AROUND US

GALEN C. HUNT – Distinguished Engineer and Managing Director, Microsoft Corporation, Redmond WA

Time: 9:20 - 10:00am | Keynote Booth 1145



The next decade promises the democratization of connectivity to every device. Significant drops in the cost of connectivity mean that every form of electrical device—every child's toy, every household's appliances, and every DoD sensor—will become connected to the Internet. Tens of billions of these devices are controlled by microcontrollers, a class of device particularly ill-prepared for the security challenges of internet connectivity. What is required to secure these billions of devices? And, how can it be done economically enough to apply to every device?

Biography: Dr. Galen Hunt founded and leads the Microsoft team responsible for Azure Sphere. Their mission is to ensure that every IoT device on the planet is secure and trustworthy. Previously, Dr. Hunt pioneered technologies ranging from confidential cloud computing to light-weight container virtualization, type-safe operating systems, and video streaming. Dr. Hunt was a member of Microsoft's founding cloud computing team. Dr. Hunt holds over 100 patents, a B.S. degree in Physics from University of Utah and Ph.D. and M.S. degrees in Computer Science from the University of Rochester.

MONDAY, JUNE 3

DT1

IS YOUR AI-BASED EDA TOOL PRODUCTION-READY?

Time: 10:30am - 12:00pm || **Room:** N260 || **Event Type:** Designer Track

Keywords: Front-end Design, Back-end Design, Low Power || **Topic Area:** Machine Learning/AI, EDA

MODERATOR:

John Ellis - Silicon Integration Initiative, Inc., Austin, TX

ORGANIZER:

Leigh Anne Clevenger - Silicon Integration Initiative, Inc., Austin, TX

Artificial intelligence-based design automation algorithms tested in research studies show improved runtime and inference results over traditional EDA approaches. What does it take to move machine learning, deep learning, and reinforcement learning from research feasibility studies to production-worthy AI design automation tools?

For AI-based EDA tools, this panel discussion will explore the following:

- How do we feed the AI beast? What data is needed? Where does it come from and what relationships are required?
- What software platforms are available today to move research-level prototypes to production-level flows?

- Can research-level systems be successfully used in-house to improve hardware and software training and inference solutions? What criteria would necessitate a transition to production level?
- What I/O and data structure standards are needed to enable different AI engines for training and inference, shared AI models, and state-of-the-art visualization tools

PANELISTS:

Rhett Davis - North Carolina State Univ., Raleigh, NC

Leon Stok - IBM Systems Group, Poughkeepsie, NY

Ramy Iskander - Intento Design, Paris, France

Leigh Anne Clevenger - Silicon Integration Initiative, Inc., Austin, TX

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DT2

NEW FRONTIERS IN FORMAL AND STATIC VERIFICATION

Time: 10:30am - 12:00pm || **Room:** N262 || **Event Type:** Designer Track

Keywords: Verification/Validation, Front-end Design, Low Power || **Topic Area:** EDA, Design

CHAIR:

Maheshwar Chandrasekar - Synopsys, Inc., Sunnyvale, CA

Formal Verification continues to be one of the fastest-growing categories in EDA, with increasing recognition that it has hit a level of maturity where any modern design team needs to leverage it to stay competitive. The presentations in this session will help your team to stay abreast of the latest developments in formal and related technologies, and provide ideas to raise your design and validation process to the next level.

2.1 Stop Leaking Unverified Corner Cases

Wayne Yun - Advanced Micro Devices, Inc., Markham, ON, Canada

2.2 Bug Hunting for Deep Sequential Complex S/M using Formal

Nitin M. Mhaske, Synopsys, Inc., Austin, TX

Iain Singleton - Synopsys, Inc., Mountain View, CA

2.3 Achieving Sign-off Efficiently Via Static Verification Tools Customized for High-value Failure Modes

Akitsugu Nakayama, Masashi Shibata, Atsunori Machida, Katsumi Imamura, Yuji Yoshitani - Fujitsu Kyushu Network Technologies Ltd., Fukuoka, Japan

2.4 Unbounded Formal Verification of RISC-V CSRs with Interval Property Checking

Nicolae Tusinschi, Sven Beyer - OneSpin Solutions GmbH, Munich, Germany

2.5 CDC Handshake: Advanced Sign-off Methodology

Ramakrishna Rayaprolu - NVIDIA Corp., Santa Clara, CA

Vikas Sachdeva - Real Intent, Inc. Sunnyvale, CA

Prakash Mukre, Louis Caradillo, Vivek Gupta - NVIDIA Corp., Santa Clara, CA

2.6 Deadlock & Livelock Detection in Power Controllers using Under-constrained Formal Testbench

Ipsita Tripathi, Arumugam Velayoudame, Rahul Gupta, Vinay Garipelli - Qualcomm India Pvt. Ltd., Bangalore, India

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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MONDAY, JUNE 3

IP3

HOW PAM4 AND DSP ENABLE 112G SERDES DESIGN

Time: 10:30am - 12:00pm || **Room:** N264 || **Event Type:** IP Track

Keywords: Architecture & System Design, Analog & Mixed Signal || **Topic Area:** IP

CHAIR & ORGANIZER:

Eric Esteve - IP-nest, Marseille, France

Incredibly fast growing demand for bandwidth needed to support chip to chip and system to system communication is pushing the industry to develop very high speed SerDes, up to 112G (112 Gbps). In 2005, state of the art SerDes speed was 5 Gbps, moving to 10 Gbps in 2010 and 28 Gbps in 2014. New DSP-based techniques like Pulse Amplitude Modulation (PAM 4) enable the design of SerDes running at up to 112 Gbps. Join this session to hear the companies involved in very high speed SerDes IP design describe new architectures and techniques allowing them to reach data rates more than 20 times higher than in 2005.

3.1 How DSP is Killing the Analog in SerDes

Tony Pialis - AlphaWave IP Corp., Toronto, ON, Canada

3.2 Enabling 400G/800G Interconnects with 56G/112G PAM-4 PHY

Rita Horner - Synopsys, Inc., Mountain View, CA

3.3 Boosting the 112G Performance with PAM4 DSP

Rishi Chugh - Cadence Design Systems, Inc., San Jose, CA

Thank you to our IP Track Sponsor:



SKY TALK: WHAT CAN EDA DO FOR QUANTUM COMPUTING AND WHAT CAN QC DO FOR EDA?

Time: 1:00 - 1:45pm || **DAC Pavilion - Booth 871** || **Event Type:** SKY Talk



Though early in its development, quantum computing is now available on real hardware via the cloud through IBM Q. This radically new kind of computing holds open the possibility of solving some problems that are now and perhaps always will be intractable for “classical” computers.

As with any new technology there are a lot of open questions. What is the road to Quantum Advantage, e.g. the point where quantum computing shows demonstrable and significant advantage over classical computers and algorithms?

What is the status of Quantum computers today? How do we define a full system-metric to measure the performance of a Quantum System? This

Skytalk will answer these questions. We will discuss what we can do in EDA to improve the performance of Quantum Systems and describe the types of EDA problems where quantum computing might be applied.

SPEAKER:

Leon Stok - Vice President of IBM's Electronic Design Automation Group, Poughkeepsie, NY

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

MONDAY, JUNE 3

DT4

POWER BYTES DELIVERED

Time: 1:30 - 3:00pm || **Room:** N260 || **Event Type:** Designer Track

Keywords: Back-end Design, Low Power, Implementation || **Topic Area:** Design, EDA

CHAIR:

Badri Uppiliappan - Analog Devices, Inc., Norwood, MA

This session will begin with a journey into improving power analysis for large and complex multi-voltage, multi-chip; followed by deeper exploration of various aspects of building and analyzing power grid networks and electro-migration from signoff perspectives.

4.1 Efficient Multi Power Domain Analysis using IPD Flow

Jongyoon Jung - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Aniket Deshmukh - Cadence Design Systems, Inc., Seongnam-Si, Republic of Korea
Pawan D. Gandhi - Cadence Design Systems, Inc. & BITS Pilani, Noida, India
Naresh Kumar - Cadence Design Systems, Inc., Uttar Pradesh, India
Arvind Veeravalli, Ritika Govila - Cadence Design Systems, Inc., Bengaluru, India
Jeannette Sutherland - Cadence Design Systems, Inc., Austin, TX

4.2 3D Stacked (Foveros) SOC Power Delivery Analysis

Methodology for Predictable Silicon Success
Biswajit Patra, Ayan Roy Chowdhury - Intel Technology India Pvt. Ltd, Bangalore, India

4.3 Two Different Approaches of Power Integrity Analysis and Correlate with On-chip Measurement

Chee Kong Ung, Mizar Chang, Sean Hwang, Bihqui Tiang - MediaTek, Inc., Hsinchu City, Taiwan
PeiShen Wei, Ying-jiunn Lai, Chan Chiuan Lee - ANSYS, Inc., Taipei, Taiwan
Oscar Ou - MediaTek, Inc., San Jose, CA

4.4 Electro-migration Reliability Verification of Gate Level Blocks for High Performance Microprocessors in Presence of Self-heating

Nagu Dhanwada - IBM Corp., Poughkeepsie, NY
Leon Sigal - IBM Research, Yorktown Heights, NY
David Kadzov - IBM Systems Group, Williston, VT

4.5 A Multi-perspective Approach to IC Power Grid Development for 7nm Based Designs

Mahendrasing J. Patil, Ravi Teja Susarla, Surendra Boosam Kota - Intel Technology India Pvt. Ltd, Bangalore, India

4.6 Electromigration Signoff based on IR-drop Degradation Assessment

Valeriy Sukharev, Mentor, A Siemens Business, Fremont, CA
Armen Kekeyan - Mentor, A Siemens Business, Yerevan, Armenia
Jun-Ho Choy - Mentor, A Siemens Business, Fremont, CA
Farid N. Najm - Univ. of Toronto, ON, Canada

Thank you to our Designer Track Sponsor:



DT5

STOP WASTING YOUR VERIFICATION BUDGET - KNOW WHEN TO USE FORMAL

Time: 1:30 - 3:00pm || **Room:** N262 || **Event Type:** Designer Track

Keywords: Verification/Validation, Front-end Design || **Topic Area:** Design

CHAIR:

KiranKumar V.M. Achutha - Intel Corp., Bengaluru, India

ORGANIZER:

Roger Sabbagh - Oski Technology, Inc., Ottawa, ON, Canada

How would you verify that your PCIe receiver framer never confused payload data with framing tokens or packet header symbols? Imagine exhaustively testing every possible combination of payload data, packet lengths, modes, link widths and framing errors.

Or, how about verifying that your GPU shader sequencer always fetched, decoded and resolved dependencies between instructions correctly, for all possible types and sequences of instructions – all while simultaneously accounting for exceptions, configuration changes, stalls and control flow events?

What about verifying the correct ordering of register accesses across a CPU pipeline with aggressive out-of-order speculation in the presence of exceptions and flushes?

These are designs with too many corner case scenarios to cover with random or directed test cases. Formal verification is needed to solve hard problems like these. In this session, we present application specific verification challenges and examples of how formal verification has been used to develop practical solutions.

5.1 A Novel Approach to PCIe Receiver Framing Checks

Joe Keirouz - Broadcom Corp., San Jose, CA
Vigyan Singhal - Oski Technology, Inc., San Jose, CA

5.2 Formal Verification of a GPU Shader Sequencer

Vaibhav Tendulkar, Chirag Dhruv - Advanced Micro Devices, Inc., Santa Clara, CA
Ashutosh Prasad - Oski Technology, Inc., Gurgaon, India

5.3 Effective Formal Solutions to CPU Verification Challenges

Vikram Khosa - Arm, Ltd., Austin, TX

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

MONDAY, JUNE 3

IP6

FUTURE AI TRENDS FOR IP WITHIN THE AUTOMOTIVE INDUSTRY

Time: 1:30 - 3:00pm || **Room:** N264 || **Event Type:** IP Track

Keywords: Automotive, Architecture & System Design || **Topic Area:** IP

MODERATOR:

John Blyler - JB Systems, Portland, OR

ORGANIZER:

Nathan Mandelke - ChipEstimate.com, San Jose, CA

Artificial intelligence is quickly transforming and redefining the automotive industry in a multitude of ways. Over the past decade, we have seen such AI enhancements as driver assist, voice recognition, telecommunications (including Wi-Fi), cloud data connectivity, and autonomous cars. These advanced automotive features have created new opportunities and requirements for chip makers. From product innovation to compliance issues to various industry collaborations, IP innovation also comes with its various challenges. However, it not only can give automakers a competitive advantage, but also help a company stay ahead of the curve.

The future of AI in automotive is bright and seems to be limitless. Join this panel discussion about the impact of IP on the future direction of artificial intelligence in the automotive industry.

PANELISTS:

Dave Steer - Imagination Technologies Ltd., San Jose, CA

Charlie Janac - Arteris, Inc., San Jose, CA

Gordon Cooper - Synopsys, Inc., Mountain View, CA

Steve Brightfield - Wave Computing, Campbell, CA

Ali Osman Ors - NXP Semiconductors, Ottawa, ON, Canada

Thank you to our IP Track Sponsor:



INTEGRATE THE AWS CLOUD WITH RESPONSIVE XILINX MACHINE LEARNING AT THE EDGE

Time: 2:00- 4:00pm || **Room:** N261 || **Event Type:** Additional Meeting

Topic Area: IP

ORGANIZERS:

Naveen Purushotham - Xilinx, San Jose, CA

Kv Thanjavur Bhaaskar - Xilinx, San Jose, CA

Hugo A. Andrade, Xilinx - San Jose, CA

In this meeting, learn how to integrate FPGA based low-latency edge machine learning with an IoT enabled distributed control application that leverages the massive scale of AWS Cloud analytics, Xilinx Edge AI based machine learning model deployment, application provisioning, and system dashboards. Based on a distributed industrial control scenario,

you will work through a hands-on integration of AWS Cloud services through AWS Greengrass on Zynq Ultrascale+ and Amazon FreeRTOS on Xilinx Zynq-7000 platforms. After this workshop, you will have a concrete understanding of how a distributed industrial control system makes use of AWS edge and cloud services plus how they enable the evolutionary approach to these types of long-lived systems towards an edge-to-cloud collaboration exemplified through the integration of machine learning applications at the industrial edge.

IEEE CEDA/ACM SIGDA ADVANCING DIVERSITY IN EDA (DivEDA) FORUM

Time: 2:00 - 6:00pm || **Room:** N259 || **Event Type:** Additional Meeting

Topic Area: EDA

ORGANIZERS:

Chengmo Yang - Univ. of Delaware, Newark, DE

Ayse Coskun - Boston Univ., Boston, MA

The goal of the Advancing Diversity in EDA (DivEDA) event is to help facilitate women and underrepresented minorities (URM) to advance their careers in academia and industry, and hence, to help increase diversity in the EDA community. Through an interactive medium, our aim is to provide

practical tips to women and URM on how to succeed and overcome possible hurdles in their career growth, while at the same time, connecting senior and junior researchers to enable a growing diverse community, which will then help accelerate innovation in the EDA ecosystem and benefit societal progress.

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

MONDAY, JUNE 3

DT7

TINYML - ULTRA LOW POWER MACHINE LEARNING APPLICATIONS AND ARCHITECTURES

Time: 3:30 - 5:00pm || Room: N260 || Event Type: Designer Track

Keywords: Architecture & System Design, Front-end Design, Low Power

Topic Area: Design, Machine Learning/AI

CHAIR & ORGANIZER:

Ambar Sarkar - NVIDIA Corp., Santa Clara, CA

Machine learning represents a potent new computing model and is quickly spreading through almost every class of system - cloud, PC, mobile and IoT. But machine learning and deep neural networks have earned a reputation for huge computation loads, large memory footprint and high power. Can the industry find a way to adapt machine learning to the most power and cost sensitive applications?

This session explores the emerging concept of "Tiny ML" - hardware platforms, network structures, optimization methods and end applications that combine sophisticated learned inference models with minuscule power budgets. These systems, often aimed at power budgets as low as 1mW, carry great promise for smarter sensor swarms, autonomous systems with years of battery life and ubiquitous devices that add subtle intelligence to everyday interactions.

7.1 Ultra-low-power Command Recognition for Ubiquitous Devices

Chris Rowen - Babblelabs, Inc, Campbell, CA

7.2 Using Analog Computation in Flash Memory for Energy-efficient AI Inference

Manar El-Chammas - Mythic, Redwood City, CA

7.3 Microwatts, Kilobytes, Megahertz, and Cents: Solving Real World Problems for AI at the Mobile Edge

Scott Hanson - Ambiq Micro, Austin, TX

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DT8

TIME SPACE CONTINUUM

Time: 3:30 - 5:00pm || Room: N262 || Event Type: Designer Track

Keywords: Back-end Design, Implementation || Topic Area: Design, EDA

CHAIR:

Mike Kazda - IBM Systems and Technology Group, Poughkeepsie, NY

Improving timing closure by applying new perspectives to change the search space of solutions are some key messages that get explored in this session.

8.1 Coverage Improvement of Assertion based SDC Verification at Early Design Phase

Nozomi Yunokuchi - Renesas Electronics Corp., Kodaira-shi, Japan

Himanshu Bhatnagar - Excellicon Inc., Laguna Hills, CA

8.2 Design Optimization and Implementation Methodology using Cells with Different Diffusion Breaks

Jae Hoon Kim, Yongdeok Kim, Wootae Kim, Hyung-Ock Kim, Joonyoung Shin - Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea

Jaewon Lee - Samsung Semiconductor, Inc., Hwasung-si, Republic of Korea

Jung Yun Choi - Samsung Electronics Co., Ltd., Yong-in, Republic of Korea

8.3 An Advanced Method of Routing Optimization with 3D Coupling Aware to Improve Timing

Jialian Tang - Avera Semiconductor LLC & GLOBALFOUNDRIES, Shanghai, China

Baoguang Yan, Fengfeng Wu - Avera Semiconductor LLC & GLOBALFOUNDRIES, Beijing, China

Mike Trick - Avera Semiconductor LLC & GLOBALFOUNDRIES, Burlington, VT

8.4 Local Layout Effect Aware Design Methodology for Performance Boost below 10nm FinFET Technology

Jae Hoon Kim, Wootae Kim, Naya Ha, Hyung-Ock Kim, Sunik Heo, Hyunjeong Roh - Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea

Hayoung Kim - Siemens Corp., Hwaseong, Republic of Korea

Yonghwan Kim, Hyunwoo Kim, Jung Yun Choi - Samsung Electronics Co., Ltd., Yong-in, Republic of Korea

8.5 A Graph based Modelling of Multi Input Switching (MIS) in STA with Silicon Path Frequency Correlation

Amartya Mazumdar, Ulhas Kotha, Anshuman Seth - NVIDIA Corp., Bangalore, India

Tezaswi Raja - NVIDIA Corp., San Jose, CA

Reecha Jajodia, Jaison Kurien, Sarvesh Sharma - NVIDIA Corp., Bangalore, India

8.6 Tile-based Automated Pipeline Floorplanning

Greg Ford - Avera Semiconductor LLC, Santa Clara, CA

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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MONDAY, JUNE 3

IP9

POWER EFFICIENT IPs FOR AI

Time: 3:30 - 5:00pm || Room: N264 || Event Type: IP Track || Keywords: Emerging Technologies, Architecture & System Design || Topic Area: IP, Machine Learning/AI

MODERATOR:

Richard Nass - *Embedded Computing Design*, New York City, NY

ORGANIZER:

Farzad Zarrinfar - *Mentor, A Siemens Business*, Freemont, CA

Artificial intelligence (AI) is part of your future. A big boon to AI comes in the form of power-efficient IP that finds its way into SoCs developed for IoT Edge devices, as AI-based SoCs will have ability to make intelligent decisions and take independent action based on data collected and analysis performed by the IoT machine. New AI applications will be enabled by power-efficient IPs, enhancing functions like speech recognition, language translation, image recognition, machine learning

acceleration, and pattern matching. Join us for this lively discussion on the present and future of these new technologies.

PANELISTS:

Aditya Mukherjee - Microsoft Corporation, Mountain View, CA

Jay Hu - Dino-Lite Scopes, San Jose, CA

Art Swift - Wave Computing, Santa Clara, CA

Mike Li - NovuMind Inc., Santa Clara, CA

Chris Shore - Arm, Ltd., Cambridge, United Kingdom

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DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Time: 5:00 - 6:00pm || Exhibit Floor || Event Type: Designer and IP Track Poster

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Monday, June 3 from 5:00 to 6:00pm on the Exhibit Floor.

123.1 Accurately modeling ASIC memories in FPGA-based prototype systems

Juergen Jaeger - Cadence Design Systems, Inc., San Jose, CA

123.2 Signoff Abstarct Model (SAM) based Hierarchical Flow Verification using VC-LP

Susantha Wijesekara - Synopsys, Inc., Mountain View, CA
Chiragkumar D. Patel - Synopsys, Inc., Bengaluru, India
Nishant Patel - Synopsys, Inc., Mountain View, CA

123.3 Rapid IP and SOC Power Dissipation AnalysisBy Leveraging Emulation

Hojin Jo, Hyeongjin Kim, Jaewon Jeon, Hyunjae Woo, Changjun Choi, Youngsik Kim, Seonil B. Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea

123.4 Optimizing Threat Modelling to Create Robust IoT Security Solutions

Brian Clinton - Arm, Ltd., Dublin, Ireland

123.5 Early LVS - Paradigm Shift to LVS with Novel Methodology (LVS – Signoff Layout vs Schematic)

Karthik Kodakandla, MuraliMohan Thota - Texas Instruments India Pvt. Ltd., Bengaluru, India

123.6 Optimizing Hardware/Software Development for ARM Based Embedded Designs

Bill Neifert - Arm, Ltd., Acton, MA
Frank Schirrmeister - Cadence Design Systems, Inc., San Jose, CA

123.7 Systematic Power Routing Strategy To Meet Design Reliability Target for Ultra-low Power SoCs

Apurve Chawda, Vivek Joshi, Subhadeep Ghosh - Texas Instruments India Pvt. Ltd., Bangalore, India

123.8 An Effective Method to Accelerate Timing ECO for Large Scale Hierarchical DVFS Design

Jincheng Wang - Unisoc Communications, Inc., Hangzhou, China
Xiao Yong, Jianlin Li, Senhua Dong - Huada Empyrean Software Co., Ltd, Beijing, China

123.9 Get Higher Productivity and Smoother Tape-out by Smarter Disk Space Management

Jigar Savla - Juniper Networks, Inc. & Georgia Institute of Technology, Sunnyvale, CA

123.10 (BlueChip) . A Smarter EDA on the Cloud, using Machine Learning

Kerim Kalafala - IBM Corp., Hopewell Junction, NY
Steve Kurtz - IBM Corp., Austin, TX
Nicholai L'Esperance, Adisus Wheelock - IBM Corp., Burlington, VT

123.11 RTLarc – An RTL based Timing-arc Tool

Ankit K. Zalawadiya, Hariprasad T. T - Advanced Micro Devices, Inc., Bangalore, India

123.12 Fast and Accurate Moment LVF Characterization for Advanced Technology Nodes

Jongyoon Jung, Hyun-seung Seo, Naya Ha, Cheoljun Bae - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Vinayakam Subramanian, Krishnakanth Gilakamsetti - ANSYS, Inc., Bengaluru, India

123.13 vManager Robotization to Support Advance Regression Management

Ashutosh Rawal, Sivasankaran Maruthamuthu, Gokarakonda Sneha, Dinesh Pai - GLOBALFOUNDRIES, Bangalore, India

123.14 Timing Closure for an EPPGA IP Inside an SoC

Christopher Pelosi - Achronix Semiconductor Corp., Santa Clara, CA

123.15 In-design Power Grid and IR Drop Optimization for High Performance Arm CPUs

Sainarayanan Karatholuvu Suryanarayanan - Arm, Ltd., Bangalore, India
Seeram Chandrasekar, Vidyasagar Jampala, Vinay Krishnan - Cadence Design Systems, Inc., Bangalore, India

123.16 Advanced Low Power Debug using Static Techniques

Himanshu Bhatt - Synopsys India Pvt. Ltd., Bangalore, India
Archanna Srinivasan - Intel Corp., San Jose, CA

123.17 Current Flow Modelling in HDL for Mixed-signal Co-simulation Analysis

Lakshmanan Balasubramanian - Texas Instruments India Pvt. Ltd., Bengaluru, India
Vijaykumar Sankaran - Cadence Design Systems, India Pvt. Ltd., Bangalore, India
Sushmitha T G, Abhishek K, Sunita Tirlapur - KarMic Design Pvt. Ltd., Manipal, India

123.18 Multimodal CDC Analysis

Maël Rabé, Jean-Christophe Brignone - STMicroelectronics, Grenoble, France
Paras Mal Jain, Ankush Bagotra - Synopsys, Inc., Sunnyvale, CA

123.19 Machine Learning Based timing Arc Prediction for AMS Design

Eric Hsu, Ting Ku, George Kokai, Zuhaiib Sheikh, Tian Yang - NVIDIA Corp. & Huada Empyrean Software Co., Ltd, Santa Clara, CA

123.20 Accelerate your Verification using DFT Emulation: A Real Test-chip Showcasing Reduction in Verification Time from Weeks to Minutes

Jitendra Aggarwal - Arm, Ltd., Bangalore, India

123.21 Metric Driven Power Regression - A Methodology Based Metric Driven Approach for Power Regressions.

Mohammed Fahad, Qazi Faheem Ahmed, Tarak Parikh, Manish Kumar, Vishnu Kanwar, Neeraj Joshi, Amit Kumar, Nupur Shikha - Mentor, A Siemens Business, Noida, India

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Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

MONDAY, JUNE 3

DESIGNER/IP TRACK POSTER SESSION

123.22 Data Analytics Engine For Design Area Analysis And Tracking

Akshay Barapatre - Texas Instruments India Pvt. Ltd., Bangalore, India

123.23 Determining the Preferred Methodology for Timing Analysis and Signoff on Mixed Signal Designs in FinFET Technology Nodes

Krishnan-Talkad Sukumar, Hariprasad T. T - Advanced Micro Devices, Inc., Bangalore, India
David Newmark - Advanced Micro Devices, Inc., Austin, TX

123.24 Advances in Formal Connectivity Checking - A Case Study on a Multi-Billion-Gate SoC

Imtiyaz Ron - Xilinx Inc., San Jose, CA
Sasa Stamenkovic - OneSpin Solutions GmbH, San Jose, CA
Sergio Marchese - OneSpin Solutions GmbH, Bristol, United Kingdom

123.25 "River Fishing": Leverage Simulation Coverage to Drive Formal Bug Hunting

Ping Yeung, Joe Hupcey III - Mentor, A Siemens Business, Fremont, CA

123.26 Reliability Challenges of Advanced Semiconductor Technologies-A Designer's Perspective

Atul Bhargava - STMicroelectronics, Greater Noida, India
Abhay Apte - Cadence Design Systems, Inc., Noida, India

123.27 Enhanced-regression Techniques to Improve Layout Verification Coverage

Samichi S. Rajesh Karturi, Kumar Sayak, Kaushik Kumar Dhang - Intel Corp., Bangalore, India

123.28 Comprehensive Chip-Package-System (CPS) Electrostatic Discharge (ESD) Simulation

Junyong Deng - Unisoc Communications, Inc., Shanghai, China
Shuqiang Zhang, Yaliang Li - ANSYS, Inc., Shanghai, China

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NETWORKING RECEPTION

Time: 6:00 - 7:00pm || Exhibit Floor || Event Type: Networking

Join us on the Exhibit Floor and enjoy snacks and beverages.

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MONDAY TUTORIALS

T1

TUTORIAL 1: MODERN RECIPES FOR BREWING THE INEVITABLE METHODOLOGY FOR TODAY'S ICS: LOW POWER MIXED-SIGNAL DESIGN VERIFICATION

Time: 10:30am - 3:00pm || **Room:** N253 || **Event Type:** Monday Tutorial || **Keywords:** Low Power, Analog & Mixed Signal, Implementation || **Topic Area:** Design, EDA

ORGANIZERS:

Vijaykumar Sankaran - Cadence Design Systems, India Pvt. Ltd., Bengaluru, India

Lakshmanan Balasubramanian - Texas Instruments India Pvt. Ltd., Bengaluru, India

Venkatraman Ramakrishnan - Texas Instruments India Pvt. Ltd., Bengaluru, India

SPEAKERS:

Lakshmanan Balasubramanian - Texas Instruments India Pvt. Ltd., Bengaluru, India

Venkatraman Ramakrishnan - Texas Instruments India Pvt. Ltd., Bengaluru, India

Aswani Kumar Golla - Texas Instruments India Pvt. Ltd., Bengaluru, India

Zhong Fon - Cadence Design Systems, Inc., San Jose, CA

T2

TUTORIAL 2: EDA CHALLENGES OF 3D INTEGRATION: PHYSICAL LAYER TO MANYCORE CHIP DESIGN

Time: 10:30am - 12:00pm || **Room:** N255 || **Event Type:** Monday Tutorial
Keywords: Architecture & System Design, Low Power, Interconnect/Networking
Topic Area: EDA, Design

ORGANIZER:

Partha Pratim Pande - Washington State Univ., Pullman, WA

SPEAKERS:

Sung-Kyu Lim - Georgia Institute of Technology, Atlanta, GA

Gabriel Loh - Advanced Micro Devices, Inc., Bellevue, WA

Partha Pande - Washington State Univ., Pullman, WA

T3

TUTORIAL 3: TIMING CRITICAL SYSTEM DESIGN - PAST, PRESENT, AND FUTURE

Time: 10:30am - 12:00pm || **Room:** N257 || **Event Type:** Monday Tutorial
Keywords: Architecture & System Design, IoT, Automotive || **Topic Area:** Embedded Systems & Software (ESS), Autonomous Systems

MODERATOR:

Haibo Zeng - Virginia Polytechnic Institute and State Univ., Blacksburg, VA

ORGANIZER:

Jian-Jia Chen - Technische Univ. Dortmund, Germany

SPEAKERS:

Jian-Jia Chen - Technische Univ. Dortmund, Germany

Giorgio Buttazzo - Scuola Superiore Sant'Anna, Pisa, Italy

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

T4

TUTORIAL 4: MACHINE LEARNING IN DIGITAL IC DESIGN AND EDA: LATEST RESULTS AND OUTLOOK

Time: 10:30am - 12:00pm | **Room:** N252 | **Event Type:** Monday Tutorial

Keywords: Front-end Design, Back-end Design, Implementation | **Topic Area:** EDA, Machine Learning/AI

ORGANIZER:

Jiang Hu - Texas A&M Univ., College Station, TX

SPEAKERS:

Mark Ren - NVIDIA Corp., Austin, TX

Sreeram Chandrasekar - Cadence Design Systems, Inc., San Jose, CA

T5

TUTORIAL 5: DESIGNING APPLICATION SPECIFIC AI PROCESSORS

Time: 10:30am - 3:00pm | **Room:** N254 | **Event Type:** Monday Tutorial

Keywords: Emerging Technologies, Architecture & System Design, Any

Topic Area: Machine Learning/AI, Design

ORGANIZER:

Manish Pandey - Synopsys, Inc., Mountain View, CA

SPEAKERS:

Manish Pandey - Synopsys, Inc., Mountain View, CA

Claudionor Coelho - Google, Inc., CA

Zhiru Zhang - Cornell Univ., Ithaca, NY

T6

TUTORIAL 6: ANALOG IP MIGRATION AND VERIFICATION

Time: 1:30 - 5:30pm | **Room:** N255 | **Event Type:** Monday Tutorial | **Keywords:**

Analog & Mixed Signal, Back-end Design, Implementation | **Topic Area:** Design, EDA

ORGANIZER:

Michael Pronath - MunEDA GmbH, Unterhaching, Germany

SPEAKERS:

Michael Pronath - MunEDA GmbH, Unterhaching, Germany

Benjamin Prautsch - Fraunhofer IIS, Institutsteil EAS, Dresden, Germany

Hidekazu Kojima - Rohm, Kyoto, Japan

Russell Mohn - inPlay Technologies, Irvine, CA

Pierluigi Daglio - STMicroelectronics, Agrate, Italy

T7

TUTORIAL 7: REQUIREMENT-DRIVEN TESTING AND VERIFICATION FOR AUTONOMOUS CYBER-PHYSICAL SYSTEMS

Time: 1:30 - 3:00pm | **Room:** N257 | **Event Type:** Monday Tutorial

Keywords: Automotive, Verification/Validation, Test/Manufacturing/Reliability/Safety

Topic Area: Autonomous Systems, Embedded Systems & Software (ESS)

ORGANIZER:

Jyotirmoy V. Deshmukh - Univ. of Southern California, Los Angles, CA

SPEAKER:

Souradeep Dutta - Univ. Colorado, Boulder, CO

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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T8

TUTORIAL 8: HOW TO RUN ML ALGORITHMS ON THE EDGE

Time: 1:30 - 5:30pm || **Room:** N252 || **Event Type:** Monday Tutorial

Keywords: Emerging Technologies || **Topic Area:** Machine Learning/AI

ORGANIZERS:

Fei Sun - Facebook, Menlo Park, CA

Joe Spisak - Facebook, Menlo Park, CA

SPEAKERS:

Vin Sharma - Amazon Web Services, Inc., Palo Alto, CA

Manash Goswami - Microsoft Corporation, Mountain View, CA

Fei Sun - Facebook, Menlo Park, CA

T9

TUTORIAL 9: PRE-SILICON VERIFICATION & POST-SILICON VALIDATION: AN END-TO-END APPROACH WITH INDUSTRIAL APPLICATIONS

Time: 3:30 - 5:30pm || **Room:** N253 || **Event Type:** Monday Tutorial

Keywords: Verification/Validation, Test/Manufacturing/Reliability/Safety, Automotive
Topic Area: EDA, Design

ORGANIZER:

Clark Barrett - Stanford Univ., Stanford, CA

SPEAKERS:

Clark Barrett - Stanford Univ., Stanford, CA

Wolfgang Ecker - Infineon Technologies AG, Munich, Germany

Subhasish Mitra - Stanford Univ., Stanford, CA

T10

TUTORIAL 10: QUEST: QUANTUM COMPUTING- EDA, SECURITY AND TEST

Time: 3:30 - 5:30pm || **Room:** N254 || **Event Type:** Monday Tutorial

Keywords: Emerging Technologies, Security & Privacy, Test/Manufacturing/Reliability/Safety || **Topic Area:** EDA, Security

ORGANIZERS:

Swaroop Ghosh - Pennsylvania State Univ., State College, PA

Anupam Chattopadhyay - Nanyang Technological Univ., Singapore

Mathias Soeken - École Polytechnique Fédérale de Lausanne, Switzerland

Robert Wille - Johannes Kepler Univ. Linz, Austria

SPEAKERS:

Swaroop Gosh - Pennsylvania State Univ., State College, PA

Anupam Chattopadhyay - Nanyang Technological Univ., Singapore

Mathias Soeken - École Polytechnique Fédérale de Lausanne, Switzerland

Robert Wille - Johannes Kepler Univ. Linz, Austria

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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TUESDAY, JUNE 4

AWARDS PRESENTATION

Time: 9:00 - 9:20am || Keynote Booth 1145

Join us for the second award ceremony at DAC as we continue to recognize success and excellence for individuals in the industry.

CEDA HONORS LAURENCE NAGEL FOR THE DONALD O. PEDERSON SOLID-STATE CIRCUITS AWARD AS KEY CONTRIBUTOR TO THE SPICE SIMULATOR CREATION

Laurence W. Nagel, President, Omega Enterprises Consulting

IEEE CEDA OUTSTANDING SERVICE AWARD

X. Sharon Hu, University of Notre Dame

For outstanding service to the EDA community as DAC General Chair in 2018.

IEEE FELLOW

Deming Chen, University of Illinois at Urbana-Champaign

For contributions to FPGA high-level synthesis

IEEE FELLOW

Hai (Helen) Li, Duke University

For contributions to neuromorphic computing system

IEEE FELLOW

Farinaz Koushanfar, University of California, San Diego

For contributions to hardware and embedded systems security, and to privacy-preserving computing

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

To Be Announced

2019 ACM TODAES BEST PAPER AWARD

*Philipp Mundhenk, Andrew Paverd, Artur Mrowca,
Sebastian Steinhorst, Martin Lukasiewycz, Suhaib A. Fahmy,
and Samarjit Chakraborty,*

“Security in Automotive Networks: Lightweight Authentication and Authorization,” Vol. 22, Issue 2, March 2017

ACM SIGDA DISTINGUISHED SERVICE AWARD

To Be Announced

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Jeyavijayan (JV) Rajendran, Texas A&M University

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

“Distributed Timing Analysis”

By Tsung-Wei Huang, Advisor: Martin D. F. Wong, University of Illinois at Urbana-Champaign



KEYNOTE: HORS D'OEUVRES FROM CHAOS

**THOMAS DOLBY – Musician, Producer & Innovator,
Johns Hopkins Univ., Baltimore, MD**

Time: 9:20 - 10:00am || Keynote Booth 1145

As a boy, what Thomas Dolby loved most about synthesizers was that (quote) “they did things I didn’t expect.” Just from fooling around with synths and samplers, never reading the owner’s manual (there was none!), he learned all that he knows about ‘real’ music and musical instruments. But his frustration today is that electronic music has not embraced the advances in AI and deep learning that are now become infused in filmmaking, videogames and virtual reality. Loops and samples, he says, are like “dumb Lego blocks that have no knowledge of each other”; yet schools of fish, murmurations of sparrows, and even world-class orchestral players watch and listen intently and make microsecond-grain, synaptic decisions, enabling them to think like a collective hive mind. Why then do synthesizers still have to behave like typewriters?

Biography: Perhaps best known for blinding us with science, TED Music Director Thomas Dolby has always blurred the lines between composition and invention. As a London teenager, Tom Robertson was fascinated with the convergence of music and technology. His experiments with an assortment of keyboards, synthesizers and cassette players led his friends

to dub him “Dolby.” That same fascination later drove him to become an electronic musician and multimedia artist whose groundbreaking work fused music with computer technology and video. Two decades, several film scores, five Grammy nominations and countless live-layered sound loops later, it’s clear Dolby’s innovations have changed the sound of popular music. In the 1990s, Dolby re-created himself as a digital-musical entrepreneur, founding Beatnik, which developed the polyphonic ringtone software used in more than half a billion cell phones. Now back to touring and recording (after a 15-year hiatus), he’s using seriously retro technology — ’40s-era oscilloscopes and Royal Navy field-test equipment — to control his modern synthesizers, in shows that are at once nostalgic and cutting edge. From 2001 to 2012, Dolby served as TED’s Music Director, programming great music for the TED stage, assembling a wide variety of house bands and collaborations to play between speakers. In 2014, Dolby took on a new name: professor. He was named the Homewood Professor of the Arts at Johns Hopkins University, teaching the course “Sound on Film.”

TUESDAY, JUNE 4

CELUG: ASSOCIATION OF HIGH PERFORMANCE COMPUTING PROFESSIONALS

Time: 8:00am - 5:00pm || Room: N249 || Event Type: Additional Meeting

Topic Area: EDA, IP Technologies, Interconnects, Low Power & Reliability

Topic Areas: Design, IoT

ORGANIZERS:

Derek Magill - The Association of High Performance Computing Professionals, Austin, TX

Bob Van deer Kloot - Teradyne, Inc., North Reading, MA

EDA Licensing providers, ISVs, and Enterprise Customers will come together at an event colocated with the 55th ACM/EDAC/IEEE Design Automation Conference (DAC), June 24 - 28, 2018, at the Moscone Center in San Francisco, CA. CELUG (Centralized Enterprise Licensing Users

Group), the Association of High Performance Computing Professionals and the ESD Alliance are hosting this one-day event colocated at DAC 2018. This interactive event will focus on Enterprise Licensing roadmaps and private presentations, with presentations and panels addressing current and future challenges to making high technology tools and users more productive. This colocated event will bring Licensing Solution Providers and Independent Software Vendors together with Enterprise Customers from key industries for interactive, face-to-face meetings.

10

ALL THINGS FPGA!

Time: 10:30am - 12:00pm || Room: N252 || Event Type: Research Reviewed

Keywords: Architecture & System Design || Topic Area: EDA

CHAIR:

Tanvir Ahmed - Preferred Networks, Inc., Tokyo, Japan

CO-CHAIR:

Kaushik Vaidyanathan - Google, Inc., Mountain View, CA

This session presents design automation methodologies for FPGAs. The first paper proposes memory-access scheduling for emerging CPU-FPGA platforms. The next paper presents a novel thread-handling high-level synthesis technique, which is evaluated on FPGAs. The third paper presents allocation techniques for multi-FPGA platforms. The final paper examines a flat timing-driven placement flow for FPGAs.

10.1 LAMA: Link-aware Hybrid Management for Memory Accesses in Emerging CPU-FPGA Platforms

Liang Feng, Jieru Zhao, Tingyuan Liang - Hong Kong Univ. of Science and Technology, Hong Kong

Sharad Sinha - Indian Institute of Technology, Goa, India

Wei Zhang - Hong Kong Univ. of Science and Technology, Hong Kong

10.2 Thread Weaving: Static Resource Scheduling for Multithreaded High-level Synthesis

Hsuan Hsiao, Jason H. Anderson - Univ. of Toronto, ON, Canada

10.3 Exact and Heuristic Allocation of Multi-kernel Applications to Multi-FPGA Platforms

Junnan Shan, Mario R. Casu - Politecnico di Torino, Italy
Jordi Cortadella - Univ. Politècnica de Catalunya, Spain
Luciano Lavagno, Mihai T. Lazarescu - Politecnico di Torino, Italy

10.4 A Flat Timing-driven Placement Flow for Modern FPGAs

Timothy Martin, Dani Maarouf, Ziad Abuwaimer, Abeer Al-Hyari, Gary Grewal, Shawki Areibi - Univ. of Guelph, Guelph, Canada

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

11

APPROXIMATING SCHRODINGER'S NEURONS

Time: 10:30am - 12:00pm || **Room:** N253 || **Event Type:** Research Reviewed

Keywords: Architecture & System Design || **Topic Area:** Design, EDA

CHAIR:

Muzaffer Kal - Facebook, Redmond, WA

CO-CHAIR:

Vijay Ragunathan - Purdue Univ., West Lafayette, IN

This session has four papers that utilize approximate computing in deep neural network accelerators and GPGPUs. The first paper describes an FPGA-based neural network framework that automatically generates DNNs which are competitive with manually designed DNN models. The second paper improves neural network acceleration by cascading error propagation from multiple stages to reduce the overall output error. The third paper proposes a log quantization encoding technique to improve the accuracy of stochastic computing based neural network. The last paper proposes an approximate computing technique by memorizing data reuse in GPGPU applications.

***11.1 Accuracy vs. Efficiency: Achieving Both Through FPGA-implementation Aware Neural Architecture Search**

Weiwen Jiang, Xinyi Zhang - Univ. of Pittsburgh, PA

Edwin Sha - East China Normal Univ., Shanghai, China

Lei Yang - Univ. of California, Irvine, CA

Qingfeng Zhuge - East China Normal Univ., Chongqing, China

Yiyu Shi - Univ. of Notre Dame, Notre Dame, IN

Jingtong Hu - Univ. of Pittsburgh, PA

11.2 CANN: Curable Approximations for High-performance Deep Neural Network Accelerators

Muhammad Abdullah Hanif, Faiq Khalid, Muhammad Shafique - Vienna Univ. of Technology, Wien, Austria

11.3 Successive Log Quantization for Cost-efficient Neural Networks Using Stochastic Computing

Sugil Lee, Hyeonuk Sim, Jooyeon Choi, Jongeun Lee - Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea

11.4 ARGA: Approximate Reuse for GPGPU Acceleration

Daniel N. Peroni, Mohsen Imani - Univ. of California, San Diego, La Jolla, CA

Hamid Nejatollahi, Nikil Dutt - Univ. of California, Irvine, CA

Tajana Rosing - Univ. of California, San Diego, CA

12

DESIGNING EFFICIENT AND SAFE AUTONOMY

Time: 10:30am - 12:00pm || **Room:** N254 || **Event Type:** Research Reviewed

Keywords: Automotive || **Topic Area:** Autonomous Systems, Embedded Systems & Software (ESS)

CHAIR:

Qi Zhu - Northwestern Univ., Evanston, IL

CO-CHAIR:

Jyotirmoy Deshmukh - Univ. of Southern California, Los Angeles, CA

The session explores different approaches for designing autonomous systems according to their safety and resource-efficiency requirements. The first paper analyzes an autonomous driving software framework with respect to functional safety. Then, there are two papers which deal with the trade-off between resource-efficiency and control performance. One proposing a method ensuring system stability while optimizing distributed control functionalities and one dynamically choosing the control strategy of adaptive variable-rate tasks. The fourth paper proposes a memory-optimized matrix representation for being able to apply Bayesian MDPs on resource-constrained platforms.

12.1 Assessing the Adherence of Industrial Autonomous Driving Software to ISO-26262 Guidelines for Software

Hamid Tabani, Leonidas Kosmidis, Jaume Abella - Barcelona Supercomputing Center, Barcelona, Spain
 Guillem Bernat - Raptita Systems LTD, York, United Kingdom
 Francisco J. Cazorla - Barcelona Supercomputing Center, Barcelona, Spain

12.2 Tighter Dimensioning of Heterogeneous Multi-resource Autonomous CPS with Control Performance Guarantees

Debayan Roy - Tech. Univ. of Munich, Germany

Wanli Chang - Univ. of York, England, United Kingdom

Sanjoy Mitter - Massachusetts Institute of Technology, Cambridge, MA

Samarjit Chakraborty - Tech. Univ. of Munich, Germany

12.3 Dynamic Switching Speed Reconfiguration for Engine Performance Optimization

Chao Peng - National Univ. of Defense Technology, Changsha, China

Yecheng Zhao, Haibo Zeng - Virginia Polytechnic Institute and State Univ., Blacksburg, VA

12.4 A Memory-efficient Markov Decision Process Computation Framework Using BDD-based Sampling Representation

He Zhou, Sunil Khatri, Jiang Hu - Texas A&M Univ., College Station, TX

Frank Liu - IBM Research - Austin, TX

* Denotes best paper candidate

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

13

DESIGNS TO WEAR; DESIGNS TO REMEMBER

Time: 10:30am - 12:00pm || **Room:** N255 || **Event Type:** Research Reviewed

Keywords: Emerging Technologies || **Topic Area:** Design

CHAIR:

Ben Kerr - Google, Inc., Mountain View, CA

CO-CHAIR:

Harika Manem - Intel Corp., Hillsboro, OR

The demands of tomorrow's applications may be met with emerging technologies ranging from scaled embedded memories to large area electronics. The session begins with 5 nm design technology co-optimization (DTCO) for magnetic RAMs with vertical nanosheet transistors. Next, techniques to build a low latency architecture for phase change memories (PCM) are presented. After that, be ready for unexpected results regarding the effects of vibration on SSD performance. The session concludes with a presentation of an ultra-thin skin electronics platform for continuous skin-sensor-silicon interfacing.

13.1 Process, Circuit and System Co-optimization of Wafer Level Co-integrated FinFET with Vertical Nanosheet Selector for STT-MRAM Applications

Trong Huynh-Bao, Anabela Veloso, Sushil Sakhare, Philippe Matagne, Julien Ryckaert, Manu Perumkunnil, Davide Crotti, Farrukh Yasin, Alessio Spessot, Arnaud Furnemont, Anda Mocuta - IMEC, Leuven, Belgium

13.2 LL-PCM: Low-latency Phase Change Memory Architecture

Choungki Song - Univ. of Wisconsin, Madison, WI

Woo Young Cho - Samsung Electronics America, Inc., San Jose, CA

Jian Huang - Univ. of Illinois at Urbana-Champaign, IL

Myoungsoo Jung - Korea Advanced Institute of Science and Technology, Incheon, South Korea

Nam Sung Kim - Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea

13.3 What Does Vibration Do To Your SSD?

Janki S. Bhimani, Tirthak Patel, Devesh Tiwari, Ningfang Mi - Northeastern Univ., Boston, MA

13.4 Ultra-thin Skin Electronics for High Quality and Continuous Skin-sensor-silicon Interfacing

Leilai Shao - Univ. of California, Santa Barbara, CA

Sicheng Li - Hewlett Packard Enterprise, San Jose, CA

Ting Lei - Peking Univ., Beijing, China

Tsung-Ching Huang, Raymond Beausoleil - Hewlett Packard Enterprise, San Jose, CA

Zhenan Bao - Stanford Univ., Stanford, CA

Kwang-Ting Cheng - Hong Kong Univ. of Science and Technology, Clear Water Bay, Hong Kong

14

FROM CIRCUIT TO SYSTEM-LEVEL: TEST AND RELIABILITY WITH MACHINE LEARNING

Time: 10:30am - 12:00pm || **Room:** N257 || **Event Type:** Research Reviewed

Keywords: Test/Manufacturing/Reliability/Safety || **Topic Area:** EDA, Machine Learning/AI

CHAIR:

Benjamin Carrion Schaefer - Univ. of Texas at Dallas, TX

CO-CHAIR:

Srikanth Venkataraman - Intel Corp., Hillsboro, OR

The growing complexity of circuits and systems along with increasing quality and robustness requirements due to applications like automotive pose new challenges for test and reliability solutions. Machine learning provides a versatile tool-kit to explore solutions from the circuit to system-level. The first paper applies Bayesian optimization and to the problem of analog/ mixed-signal verification, while the second paper performs testability analysis using deep-learning. The next paper mitigates the problem of row-hammering using memory locality. Finally, the last paper of the session addresses the problem of predicting hardware failures at the system-level during runtime.

14.1 Enabling High-dimensional Bayesian Optimization for Efficient Failure Detection of Analog and Mixed-signal Circuits

Hanbin Hu, Peng Li, Jianhua Z. Huang - Texas A&M Univ., College Station, TX

14.2 High Performance Graph Convolutional Networks with Applications in Testability Analysis

Yuzhe Ma - Chinese Univ. of Hong Kong, Shatin, Hong Kong

Haoxing Ren, Brucek Khailany, Harbinder Sikka, Lijuan Luo, Karthikeyan Natarajan - NVIDIA Corp., Santa Clara, CA

Bei Yu - Chinese Univ. of Hong Kong, Shatin, Hong Kong

14.3 MRLoc: Mitigating Row-hammering Based on Memory Locality

Jung Min You, Joon-Sung Yang - Sungkyunkwan Univ., Suwon, Republic of Korea

14.4 System Level Hardware Failure Prediction Using Deep Learning

Xiaoyi Sun - Shanghai Jiao Tong Univ., Shanghai, China

Krishnendu Chakrabarty - Duke Univ., Durham, NC

Ruirui Huang, Yiqian Chen, Bing Zhao, Hai Cao - Alibaba Group Holding Limited, China

Yinhe Han - Chinese Academy of Sciences, Beijing, China

Xiaoyao Liang, Li Jiang - Shanghai Jiao Tong Univ., Shanghai, China

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TUESDAY, JUNE 4

15

REVOLUTIONARY COMPUTING OR HEURISTICS FOREVER?

Time: 10:30am - 12:00pm | **Room:** N259 | **Event Type:** Panel

Keywords: Architecture & System Design, Back-end Design, Front-end Design

Topic Area: EDA, Design

MODERATOR:

Giovanni De Micheli - École Polytechniquecole Polytechnique Fédérale de Lausanne, Switzerland

ORGANIZER:

Giovanni De Micheli - École Polytechniquecole Polytechnique Fédérale de Lausanne, Switzerland

Most EDA problems are computationally complex and thus unlikely to be solved exactly when above a given size. For decades, EDA researchers have proposed heuristic algorithms to achieve approximate solutions. In some cases such solutions have guaranteed properties, in some others, not. Most EDA tools and flows are based on such tools. As semiconductor technology downscaling slows down, a strong competitive edge stems from the tool quality, and it's ability to solve problems exactly or quasi-exactly on instances of size relevant enough for engineering design problems. At the same time, computer processing power and memory space are increasing at a fast pace, thus placing some exact solution to EDA problems within reach. Moreover, design companies as well as EDA providers are highly interested in the quality of the solutions.

Some large instances of the satisfiability problem (SAT) can be solved by specialized tools today. Smart mapping of design problems into SAT enables their efficient solutions. Moreover, the emergence of

reconfigurable hardware accelerators as co-processors paves the way to other way of solving problems exactly and in parallel way.

Recent computing approaches, such as quantum and memcomputing have shown the possibility to break the complexity barriers by using non-standard computational models and exploiting superposition. If the current (2018) results are confirmed and scale up, these computing models can revolutionize the algorithmic approach to problem solving and in particular the EDA world.

This panel is meant to debate the following controversy: Do we search for more heuristics leveraging Moore's Law scaling and expanding cloud compute/memory/storage capabilities or do we bet on revolutionary computing systems coupled with emerging specialized hardware – specifically, memcomputing and/or quantum computing?

PANELISTS:

Massimiliano Di Ventra - Univ. of California, San Diego, La Jolla, CA

Jason Cong - Univ. of California, Los Angeles, CA

Antun Domic - Stanford Univ., Standford, CA

Martin Roettler - Microsoft Research, Redmond, WA

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TUESDAY, JUNE 4

TRUST ME... IT'S SAFE..

DT16

Time: 10:30am - 12:00pm || Room: N260 || Event Type: Designer Track

Keywords: Verification/Validation, Automotive, System Security

Topic Area: Autonomous Systems, Security

MODERATOR:

Ann Steffora Mutschler - Semiconductor Engineering, San Jose, CA

ORGANIZERS:

Bryan Ramirez - Mentor, A Siemens Business, Wilsonville, OR

Jacob Wiltgen - Mentor, A Siemens Business, Denver, CO

Rebecca Granquist - Mentor, A Siemens Business, Wilsonville, OR

As companies strive for greater levels of autonomy, more capability will be required of automotive ICs, and the challenge of ensuring functional safety is exacerbated. The mass public trusts companies to deliver safe products to the market, but can industries deliver on that promise given the demand for rapid innovation and complexity within the automotive ecosystem and supply chain? The scope of functional safety extends beyond the product boundaries to systems of interlinked devices representing the complete transportation network. From IP to automobile, each product plays a role in the overall functional safety of the transportation network. New paradigms and methodologies are required to ensure functional safety across all levels of the automotive ecosystem.

T panel, we will explore the challenges of addressing functional safety as new technologies and tools are introduced.

Can we work together?

Safety has been commonly used as a marketing lever. Should safety continue to be viewed as a differentiator and data kept private?

- What sort of standardization is required to ensure functional safety beyond ISO26262 and SOTIF?
- Should safety reports, metrics, and audits be regulated?
- Should interfaces and V2X data models be standardized? Should industry engage in interoperability testing?
- What is the ethical responsibility of companies to share data (telemetry, accident, etc...) with competitors?

How do you validate and verify the autonomous driving ecosystem?

Autonomous vehicles will be required to operate independently (reactive) but the opportunity exists for enhanced functional safety with connectivity to infrastructure and cloud (proactive). The ISO26262 standard recommends safety analysis and testing to be performed as close as possible to the final product implementation. How does EDA enable verification in a V2X world?

- Is testing close to the final implementation (gate level) a reasonable and sustainable request given the trajectory of automotive ICs and systems?
- Are further levels of abstraction acceptable and to what degree? Can functional safety be closed in a digital representation (digital twin) or must physical testing be performed to supplement and validate the digital results?
- To support rapid development and deployment of machine learning algorithms, High Level Synthesis technologies are gaining traction. Can safety be "correct by construction" via HLS? Can fault testing be executed at that higher level of abstraction?

How much testing is enough for IC Functional Safety?

Functional correctness is about testing the positive space while verifying functional safety is about testing the larger negative space.

Today, functional safety verification continues to challenge even the most advanced verification teams.

- Current fault simulators leverage functional regressions and the completeness of a fault campaign is reliant on the quality of functional regression stimulus. How does a user know how much testing is enough and is current industry practice acceptable? How can formal and functional coverage metrics be used to aid and/or supplement fault simulations?
- Are traditional approaches to safety sufficient and if not, what new approaches are required to ensure safety across increasingly complex ICs? What techniques can be applied to make the safety workflow more efficient?

PANELISTS:

Ghani Kanawati - Arm, Ltd., Austin, TX

Yves Renard - ON Semiconductor, Brussels, Belgium

Nir Maor - Qualcomm Technologies, Inc., San Diego, CA

Mathieu Blazy-winning - NXP Semiconductors, Austin, TX

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TUESDAY, JUNE 4

17

IN-AND NEAR-MEMORY COMPUTING PARADIGMS

Time: 10:30am - 12:00pm || **Room:** N261 || **Event Type:** Special Session

Keywords: Architecture & System Design, Emerging Technologies

Topic Area: EDA, Embedded Systems & Software (ESS)

CHAIR:

Tulika Mitra - National Univ. of Singapore, Singapore

ORGANIZER:

Ethan Miller - Univ. of California, Santa Cruz, CA

The capacity of memory and storage devices is expected to increase drastically with adoption of the forthcoming memory and integration technologies. New memory technologies offer new trade-offs with respect to the relevant memory parameters and hence open the door for in-memory and near-memory computing paradigms. This special session enlightens these developments from various angles. The first talk discusses performing massively-parallel bulk operations in memory by exploiting the analog operational properties of DRAM, with low-cost changes as well as exploiting the logic layer in 3D-stacked memory technology in various ways to accelerate important data-intensive applications. The second talk presents a software-only implementation of Software-Defined Servers, allowing large in-memory virtual machines to be dynamically created that are larger than physical servers. Finally, the third talk focuses on bringing Near-Data Processing into Mainstream Heterogeneous Computing Systems by turning memory and storage devices into familiar heterogeneous distributed computing systems.

17.1 Enabling Practical Processing in and near Memory for Data-intensive Computing

Onur Mutlu - Eidgenössische Technische Hochschule Zürich, Switzerland

Saugata Ghose - Carnegie Mellon Univ., Pittsburgh, PA

Juan Gomez-Luna - Eidgenössische Technische Hochschule Zürich, Switzerland

Rachata Ausavarungnirun - Carnegie Mellon Univ., Pittsburgh, PA

17.2 Software-defined Servers

Ike Nassi - Univ. of California, Santa Cruz, CA

17.3 Practical Near-data Processing to Evolve Memory and Storage Devices into Mainstream Heterogeneous Computing Systems

Pankaj Mehra - Samsung Electronics Co., Ltd., San Jose, CA

Nam Sung Kim - Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea

DT18

EMBEDDED SYSTEMS, SECURITY, AND TOOL-CHAIN

Time: 10:30am - 12:00pm || **Room:** N262 || **Event Type:** Designer Track

Keywords: Architecture & System Design, System Security, IoT

Topic Area: Embedded Systems & Software (ESS), Security

CHAIR:

Natraj Ekambaram - NXP Semiconductors, Austin, TX

In this session, we explore methods to increase productivity for software and system development with cloud-based virtual environment and validation systems. For emerging technologies such as RISC-V, we will discuss tool chains and ecosystem support. We will also discuss lightweight encryption algorithms for IoT and side-channel attack simulation techniques for Crypto ICs.

18.1 Clouds, Containers, and your Simulations & Virtual Platforms

Jakob Engblom - Intel Corp., Stockholm, Sweden

18.2 A Novel Hardware and Software Architecture Sequencing & Validation Platform

Lashminarayanan Venkatesan, Raghav Tenneti, Preetika Tandon, Vishal Shah - NVIDIA Corp., Bengaluru, India

Edward Riegelsberger - NVIDIA Corp., Santa Clara, CA

18.3 RISC-V Software & Toolchain

Palmer Dabbelt - SiFive, Inc., San Mateo, CA

18.4 A Lightweight Hardware Architecture for IoT Encryption Algorithm

Khaled S. Mohamed - Mentor, A Siemens Business, Cairo, Egypt

18.5 Hybrid ADAS Development Environment for Architecture-specific Performance Estimation

Akira Takeda, Yuji Ishikawa, Tatsuya Mori, Takeshi Kodaka, Yuji Okuda, Takashi Yoshikawa - Toshiba Electronic Devices & Storage Corp., Kawasaki, Japan

18.6 A Full System Simulation Technique of Power-noise Side Channel Leakage in Cryptographic Integrated Circuits

Akihiro Tsukioka, Makoto Nagata - Kobe Univ., Kobe, Japan
Karthik Srinivasan, Shan Wan, Lang Lin, Ying-Shiun Li, Norman Chang - ANSYS, Inc., San Jose, CA

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TUESDAY, JUNE 4

IP19

OPEN SOURCE ISAS - WILL THE IP INDUSTRY FIND COMMERCIAL SUCCESS?

Time: 10:30am - 12:00pm || **Room:** N264 || **Event Type:** IP Track

Keywords: Emerging Technologies, Architecture & System Design, System Security

Topic Area: IP, Embedded Systems & Software (ESS)

MODERATOR:

Eric Dewannain - Broadcom Corp., San Jose, CA

ORGANIZER:

Randy Fish - UltraSoC Technologies Ltd., Cambridge, United Kingdom

In the past few years Open Source ISAs have generated an immense amount of interest in the semiconductor, IP, and systems industries. Advocates of open and well specified ISAs make a very compelling argument for driving the next generation of processing at all levels, server to edge. There are dozens of sources for acquiring processor IP, commercial and open source. There are commercial and open source development tools and infrastructure for supporting your own implementations. We have a plethora of papers about the promise of value. Where will there be real commercial success? Where are

the production implementations that use open source or commercial offerings? Will RISC-V and Open MIPS be drivers for the IP industry and will the IP industry be able to drive Open MIPS and RISC-V to a dominant position?

PANELISTS:

Emerson Hsiao - Andes Technology Corp., San Jose, CA

Jerry Ardizzone - Codasip Ltd., Campbell, CA

Steve Brightfield - Wave Computing, Campbell, CA

Kamakoti Veezhinathan - Indian Institute of Technology Madras, Chennai, India

Bobe Simovich - Broadcom Corp., San Jose, CA

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CEDA DISTINGUISHED SPEAKER LUNCHEON: SIMULATION TECHNOLOGIES FOR IMAGE SYSTEMS ENGINEERING

Date: Tuesday, June 4 || **Time:** 12:00 - 1:30pm || **Room:** N246

Event Type: Additional Meeting || **Keywords:** Verification/Validation, Architecture & System Design, Implementation, Emerging Technologies || **Topic Area:** EDA



The use of imaging systems has grown enormously over the last several decades; these systems are an essential component in mobile communication, medicine, and automotive applications. As part of this growth the complexity of imaging systems hardware, from optics to electronics, has increased dramatically, making software prototyping an essential tool for the design and evaluation of systems and components. I will describe several examples for image systems engineering

applications. This is a good moment to consider how academia and industry might combine to create an image systems simulation infrastructure that speeds the development of new systems for the many opportunities that will arise over the next few decades.

Biography: Brian A. Wandell is the first Isaac and Madeline Stein Family Professor at Stanford University. He joined the Psychology faculty in 1979 and is a member, by courtesy, of Electrical Engineering, and Ophthalmology. He is Director of the Center for Cognitive and Neurobiological Imaging, and Deputy Director of the Wu Tsai Neuroscience Institute. Wandell's research uses magnetic resonance imaging and software simulations for basic and applied research spanning human visual perception, brain development, and image systems simulations.

SPEAKER:

Prof. Brian A. Wandell - Stanford University, Stanford, CA

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TUESDAY, JUNE 4

SKY TALK: MARCH OF THE MACHINES – BUILDING ETHICAL AI

Time: 1:00 - 1:45pm || **DAC Pavilion - Booth 871** || **Event Type:** SKY Talk



As humans, our ethical and moral instincts are shaped by experience and circumstance. Our view of what is morally right or wrong is complicated by our emotional and instinctual responses related to past experience, family, friends, along with our cultural surroundings and actions that we have taken or learned in the past. While we may believe there are certain dark lines that cross the line of what is right and wrong, the difficulty of doing the right thing in extreme circumstances may

arise from people being unwilling to pay the price that the right action may require.

A robot would not suffer from the same ethical dilemma. Its response will be amoral, predetermined by its underlying software.

Humans created software structure on which the robot is built. Facing this future of AI, we must also face these ethical issues. The next generation of AI and the data revolution are upon us. We know that technology moves faster than regulation and that ethics influence law and regulation. In order for AI to be trusted and successful, the ethical dilemmas must be addressed, preferably within some common, recognizable framework. This framework must address cultural and regional differences while simultaneously accommodating the globalization of commerce and technology. This talk looks at the challenges and explores some possible ways forward.

SPEAKER:

Carolyn Herzog - Arm, Ltd., San Jose, CA

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20

EMBEDDED SOFTWARE MEETS EMERGING HARDWARE

Time: 1:30 - 3:00pm || **Room:** N252 || **Event Type:** Research Reviewed

Keywords: Architecture & System Design, Implementation || **Topic Area:** Embedded Systems & Software (ESS)

CHAIR:

Muhammad Shafique - Technische Univ. Wien, Vienna, Austria

CO-CHAIR:

Andreas Gerstlauer - Univ. of Texas at Austin, TX

This session discusses innovative embedded software design methods for efficient execution on constrained and heterogeneous emerging hardware. The first three papers address embedded GPU architectures, including efficient pruning for deep neural networks, a generalized tuning approach for approximate computing and lightweight design to boost mobile applications. The last paper exploits emerging non-volatile memories for improved transient computing.

20.1 HeadStart: Enforcing Optimal Inceptions in Pruning Deep Neural Networks for Efficient Inference on GPGPUs

Ning Lin - Chinese Academy of Sciences, Beijing, China

Hang Lu - Institute of Computing Technology, Beijing, China

Xin Wei - Chinese Academy of Sciences, Beijing, China

Xiaowei Li - Institute of Computing Technology, Beijing, China

20.2 GATE: A Generalized Dataflow-level Approximation Tuning Engine for Data Parallel Architectures

Seokwon Kang, Yongseung Yu - Hanyang Univ., Seoul, Republic of Korea

Hiho Kim - Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

Yongjun Park - Hanyang Univ., Seoul, Republic of Korea

20.3 LSIM: Ultra Lightweight Similarity Measurement for Mobile Graphics Applications

Yu-Chuan Chang, Wei-Ming Chen - National Taiwan Univ., Taipei, Taiwan

Pi-Cheng Hsiu, Yen-Yu Lin - Academia Sinica, Taipei, Taiwan
Tei-Wei Kuo - National Taiwan Univ., Taipei, Taiwan

20.4 Efficient State Retention Through Paged Memory Management for Reactive Transient Computing

Sivert T. Sliper, Domenico Balsamo - Univ. of Southampton, England

Nikos Nikoleris, William Wang - Arm, Ltd., Cambridge, United Kingdom

Alex S. Weddell, Geoff V. Merrett - Univ. of Southampton, England, United Kingdom

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21

FASTER COMPUTE IN SMARTER MEMORIES

Time: 1:30 - 3:00pm || **Room:** N253 || **Event Type:** Research Reviewed

Keywords: Architecture & System Design || **Topic Area:** Embedded Systems & Software (ESS)

CHAIR:

Vinay Chippa - Intel Corp., Hillsboro, OR

CO-CHAIR:

Jacques Pienaar - Google, Inc., Mountain View, CA

The emergence of in memory computing is one of the most exciting developments in recent times. This session offers solutions for problems across the near-memory computing stack, from estimating application performance on near-memory platforms, creating clever circuit optimizations for parallelizing complex DRAM operations, memory placement heuristics for improving the locality of graph algorithms to enabling neural training for low power AI edge devices.

21.1 NAPEL: Near-memory Computing Application Performance Prediction via Ensemble Learning

Gagandeep Singh - IBM Research - Zurich, Switzerland

Juan Gómez-Luna - Eidgenössische Technische Hochschule Zürich, Switzerland

Giovanni Mariani - IBM Research - Zurich, Switzerland

Geraldo Francisco De Oliveira - Eidgenössische Technische Hochschule Zürich, Switzerland

Stefano Corda - IBM Research - Zurich, Switzerland

Sander Stuijk - Eindhoven Univ. of Technology, Eindhoven, Netherlands

Onur Mutlu - Eidgenössische Technische Hochschule Zürich, Switzerland

Henk Corporaal - Eindhoven Univ. of Technology, Eindhoven, Netherlands

21.2 DREDGE: Dynamic Repartitioning During Dynamic Graph Execution

Andrew M. McCrabb, Eric Winsor, Valeria Bertacco - Univ. of Michigan, Ann Arbor, MI

21.3 ROC: DRAM-based Processing with Reduced Operation Cycles

Xin Xin, Youtao Zhang, Jun Yang - Univ. of Pittsburgh, PA

21.4 NV-BNN: An Accurate Deep Convolutional Neural Network Based on Binary STT-MRAM for Adaptive AI Edge

Chih-Cheng Chang, Ming-Hung Wu, Jia-Wei Lin, Chun-Hsien Li - National Chiao Tung Univ., Hsinchu, Taiwan

Vivek Parmar - Indian Institute of Technology Delhi, India

Heng-Yuan Lee, Jeng-Hua Wei, Shyh-Shyuan Sheu - Industrial Technology Research Institute, Chutung, Hsinchu, Taiwan

Manan Suri - Indian Institute of Technology Delhi, India

Tian-Sheuan Chang, Tuo-Hung Hou - National Chiao Tung Univ., Hsinchu, Taiwan

22

NO PEEKING AND POKING: SECURING YOUR DATA IN MEMORY AND STORAGE

Time: 1:30 - 3:00pm || **Room:** N254 || **Event Type:** Research Reviewed

Keywords: Security & Privacy || **Topic Area:** Security, Embedded Systems & Software (ESS)

CHAIR:

Ujjwal Guin - Auburn Univ., Auburn, AL

CO-CHAIR:

Jyotirmoy Deshmukh - Univ. of Southern California, Los Angeles, CA

This session has a healthy mix of solutions to security problems in the memory and storage segments. We will look at ideas covering memory isolation by leveraging existing debug infrastructure on the processors. Next up is a paper on Hybrid-Oblivious RAM that improves performance spanning memory and storage. This is also a good segue to a methodology for real time detection of emerging attacks such as ransomware on storage products. Finally, we look at a crash consistent, high performance non-volatile memory architecture.

22.1 No Compromises: Secure NVM with Crash Consistency, Write-efficiency and High-performance

Fan Yang, Youyou Lu, Youmin Chen, Haiyu Mao, Jiwu Shu - Tsinghua Univ., Beijing, China

22.2 In-process Memory Isolation using Hardware Watchpoint

Jinsoo Jang, Brent Byunghoon Kang - Korea Advanced Institute of Science and Technology, Daejon, Republic of Korea

22.3 H-ORAM: A Cacheable ORAM Interface for Efficient I/O Accesses

Liang Liu - Univ. of Pittsburgh, PA

Rujia Wang - Illinois Institute of Technology, Chicago, IL
Youtao Zhang, Jun Yang - Univ. of Pittsburgh, PA

22.4 RansomBlocker: a Low-overhead Ransomware-proof SSD

Jisung Park - Seoul National Univ., Seoul, Republic of Korea

Youngdon Jung - Daegu Gyeongbuk Institute of Science and Technology, Daegu, Republic of Korea

Jonghoon Won, Minji Kang - Seoul National Univ., Seoul, South Korea

Sungjin Lee - Daegu Gyeongbuk Institute of Science and Technology, Daegu, Republic of Korea

Jihong Kim - Seoul National Univ., Seoul, Republic of Korea

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

23

FIGHTING FOR ERROR RESILIENCY IN COMPUTING SYSTEMS

Time: 1:30 - 3:00pm || **Room:** N255 || **Event Type:** Research Reviewed

Keywords: Architecture & System Design || **Topic Area:** Embedded Systems & Software (ESS)

CHAIR:

Yanzhi Wang - Northeastern Univ., Boston, MA

CO-CHAIR:

Soonhoi Ha - Seoul National Univ., Seoul, Republic of Korea

Error resiliency has become key to design reliable systems that range from energy harvesting devices to 2-D and 3-D memories or full blown heterogeneous embedded systems. This track consists of four papers that target each of these computing systems. The first paper improves the accuracy of computations at back-end computing systems by performing optimal data refreshing from the edge to save energy. Then, the next two papers present the error emulation and correction for 2-D and 3-D memories, respectively. Finally, the last paper presents adaptive task remapping considering multi-layer reliability.

23.1 Transmit or Discard: Optimizing Data Freshness in Networked Embedded Systems with Energy Harvesting Sources

Zimeng Zhou - City Univ. of Hong Kong, Hong Kong

Chenchen Fu - Southeast Univ., Nanjing, China

Chun Jason Xue - City Univ. of Hong Kong, Hong Kong

Song Han - Univ. of Connecticut, Storrs, CT

23.2 FPGA-based Emulation of Embedded DRAMs for Statistical Error Resilience Evaluation of Approximate Computing Systems

Marco Widmer, Andrea Bonetti, Andreas Burg - École Polytechnique Fédérale de Lausanne, Switzerland

23.3 Adapting Layer RBERs Variations of 3D Flash Memories via Multi-granularity Progressive LDPC Reading

Yajuan Du, Yao Zhou - Wuhan University of Technology, Wuhan, China

Meng Zhang - Huazhong Univ. of Science & Technology, Wuhan, China

Wei Liu, Shengwu Xiong - Wuhan University of Technology, Wuhan, China

23.4 A Hybrid Agent-based Design Methodology for Dynamic Cross-layer Reliability in Heterogeneous Embedded Systems

Siva Satyendra Sahoo, Bharadwaj Veeravalli - National Univ. of Singapore

Akash Kumar - Technische Univ. Dresden, Germany

24

DESIGN-TIME OPTIMIZATION OF POWER, TEMPERATURE, AND ACCURACY

Time: 1:30 - 3:00pm || **Room:** N257 || **Event Type:** Research Reviewed

Keywords: Low Power, Back-end Design, Any || **Topic Area:** EDA, Design

CHAIR:

Dinesh Bhatia - Univ. of Texas at Dallas, TX

CO-CHAIR:

Younghyun Kim - Univ. of Wisconsin, Madison, WI

This session showcases opportunities for achieving power and energy efficiency ranging from new transistor technologies to accuracy trade-offs. The first paper provides a modeling tool to guide designers with early power estimations. The second paper assesses the impact of gate-level manipulations in approximate circuits on their computation accuracy. The third paper presents an in-depth analysis of the power and thermal implications of the NCFET technology. The final paper presents a circuit design technique to improve the energy efficiency of cache memories by adapting the signaling scheme used for data transmission at the interface.

24.1 PRIMAL: Power Inference using Machine Learning

Yuan Zhou - Cornell Univ., Ithaca, NY

Haoxing Ren, Yanqing Zhang, Ben Keller, Brucek Khailany - NVIDIA Corp., Austin, TX

Zhiru Zhang - Cornell Univ., Ithaca, NY

24.2 Partition and Propagate: an Error Derivation Algorithm for the Design of Approximate Circuits

Ilaria Scarabottolo, Giovanni Ansaloni - Univ. della Svizzera italiana, Lugano, Switzerland

George A. Constantinides - Imperial College London, United Kingdom

Laura Pozzi - Univ. della Svizzera italiana, Lugano, Switzerland

24.3 Performance, Power and Cooling Trade-offs with NCFET-based Many-cores

Martin Rapp, Sami Salamin, Hussam Amrouch - Karlsruhe Institute of Technology, Karlsruhe, Germany

Girish Pahwa, Yogesh Chauhan - Indian Institute of Technology Kanpur, India

Jörg Henkel - Karlsruhe Institute of Technology, Karlsruhe, Germany

24.4 STFL: Energy-efficient Cache Interface using Slow Transition Fast Level Signaling

Payman Behnam, Mahdi Bojnordi - Univ. of Utah, Salt Lake City, UT

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

25

IN-MEMORY COMPUTING FOR MACHINE LEARNING - FUTURE OR FALLACY?

**Time: 1:30 - 3:00pm || Room: N259 || Event Type: Panel || Keywords: Architecture & System Design, Analog & Mixed Signal, Emerging Technologies
Topic Area: Machine Learning/AI, Design**

MODERATOR:

Reetuparna Das - Univ. of Michigan, Ann Arbor, MI

ORGANIZER:

Valeria Bertacco - Univ. of Michigan, Ann Arbor, MI

Several flavors of memory-centric computing have evolved over the years. Back from 90s, Processing-in-Memory or Near-Memory architectures were born in form of logic units tightly fused to separate memory structures, to present day In-Memory architectures which repurpose memory structures to do computing. Further, these class of architectures has the added dimension of which memory technology to be used.

This panel will focus on the advantages and pitfalls of using memory-centric computing for AI. The champions are likely to make a case based

on data-movement benefits, area savings, parallelism, integration benefits, and efficiency. The other side is likely to make an against case based on precision, flavors of analog in-memory computing which introduce data conversion overheads, technology feasibility, and programmability.

PANELISTS:

Rangarajan Venkatesan - NVIDIA Corp., Santa Clara, CA
Nuwam Jayasena - Advanced Micro Devices, Inc., Santa Clara, CA
Vikas Chandra - Facebook, Mountainview, CA
Shekhar Borkar - Qualcomm Technologies, Inc., San Diego, CA
Engin Ipek - Univ. of Rochester, NY

DT26

PRODUCTIVITY IMPROVEMENTS IN VALIDATION AND DESIGN

**Time: 1:30 - 3:00pm || Room: N260 || Event Type: Designer Track
Keywords: Verification/Validation, Front-end Design, Automotive
Topic Area: EDA, Design**

CHAIR:

Soon Ee Ong - Intel Corp., Penang, Malaysia

With design complexity continuing to grow while budgets remain flat, it is only with a stream of constant productivity improvements that our industry can continue to grow. In this session we will see a variety of innovative ideas that enable us to increase the efficiency of our validation processes without a corresponding increase to design and validation resources.

26.1 Using PSS: An Automotive Case Study

Ben J. Sutton, Leo Matturi - Infineon Technologies UK Ltd., Bristol, United Kingdom

Dilip J. Kumar Shankar Dass, Balasubramanian Gopalakrishnan - Test and Verification Solutions, Bristol, United Kingdom

26.2 RamGen: Moving Memory from Physical to the Logical Domain

Jeffery B. Scott, Jonathan Sadowsky, Jigar Savla - Juniper Networks, Inc., Sunnyvale, CA

26.3 Scan Chain Recover and Chain Stitch for Function ECO

Tse-Wei Wu, Yu-Hsun Su, Chen-Yuan Kao, Min-Hsiu Tsai - Global Unichip Corp., Hsinchu, Taiwan

26.4 Connecting Verification Tools To Enhance Their Power

Raviv Gal, Avi Ziv - IBM Research - Haifa, Israel

26.5 Advanced Reset Design Methodology and Verification

Yong Lee, Changho Yang - SK hynix Inc., Sungnam, Republic of Korea

Hyobeen Park, Vikas Sachdeva - Real Intent, Inc. Sunnyvale, CA

26.6 'Time Slot Blade' : A Scheduling Mechanism to Avoid Transaction Level Race Condition

Soya Zhang, Chenghuan Li, Yunyang Song, Zhijun Fu - MediaTek, Inc., Hefei, China

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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27

HARDWARE SECURITY 2.0: TOWARDS NEXT-GENERATION SECURE AND INTELLIGENT CPUS AND SOCS

Time: 1:30 - 3:00pm || **Room:** N261 || **Event Type:** Special Session

Keywords: System Security, Hardware Security, IoT || **Topic Area:** Security

CHAIR:

Wolfgang Kunz - Technische Univ. Kaiserslautern, Germany

ORGANIZERS:

Lejla Batina - Radboud Univ. Nijmegen, The Netherlands
Nele Mentens - Katholieke Universiteit Leuven, Belgium

The capacity of memory and storage devices is expected to increase drastically with adoption of the forthcoming memory and integration technologies. New memory technologies offer new trade-offs with respect to the relevant memory parameters and hence open the door for in-memory and near-memory computing paradigms. This special session enlightens these developments from various angles. The first talk discusses performing massively-parallel bulk operations in memory by exploiting the analog operational properties of DRAM, with low-cost changes as well as exploiting the logic layer in 3D-stacked memory technology in various ways to accelerate important data-intensive applications. The second talk presents a software-only implementation of Software-Defined Servers, allowing large in-memory virtual machines to be dynamically created that are larger than physical servers. Finally, the third talk focuses on bringing Near-Data Processing into Mainstream Heterogeneous Computing Systems by turning memory and storage devices into familiar heterogeneous distributed computing systems.

27.1 Formal Verification of Security Critical Hardware-Firmware Interactions in Commercial SoCs

Sayak Ray, Nishant Ghosh, Ramya Jayaram Masti, Arun Kanuparthi, Jason M. Fung - Intel Corp., Hillsboro, OR

27.2 In Hardware We Trust – Gains and Pains of Hardware-assisted Security

Lejla Batina - Radboud Univ. Nijmegen, The Netherlands
Patrick Jauernig - Technische Univ. Darmstadt, Germany
Nele Mentens - Katholieke Universiteit Leuven, Belgium
Ahmad-Reza Sadeghi, Emmanuel Stafp - Technische Univ. Darmstadt, Germany

27.3 Protecting RISC-V against Side-channel Attacks

Elke De Mulder, Samatha Gummalla, Michael Hutter - Rambus Cryptography Research Devision, San Francisco, CA

DT28

SIMPLIFYING MACHINE LEARNING DEPLOYMENT FROM CLOUD TO EDGE TO END NODE

Time: 1:30 - 3:00pm || **Room:** N262 || **Event Type:** Designer Track

Keywords: IoT, Emerging Technologies, Architecture & System Design

Topic Area: Embedded Systems & Software (ESS), Machine Learning/AI

CHAIR:

Natraj Ekambaram - NXP Semiconductors, Austin, TX

ORGANIZER:

Markus Levy - NXP Semiconductors, San Jose, CA

For a variety of compelling reasons, there's a strong push to move machine learning from the cloud to the edge, where we are witnessing the intersection of artificial intelligence and systems design. However, for 'Edge AI' to become a mainstream reality, we must simplify the technology to a level that models can be trained and inference engines can be developed & deployed with a python script or pull-down menu, rather than burdening the developer with having to create complex mathematical algorithms. The goal of this track is to explore some of the capabilities and options to utilize neural networks and classical machine learning libraries in the modern era of programming that we call Software

2.0 - where programming is more about determining weights and parameters (e.g. typically known as training models), and the developer can take advantage of the growing number of open source resources.

28.1 Glow as a Machine Learning Compiler for Heterogeneous Hardware

Jordan Fix - Facebook, Menlo Park, CA

28.2 Open Source Implementations for Machine Learning at the Edge and End Node

Markus Levy - NXP Semiconductors, San Jose, CA

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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TUESDAY, JUNE 4

IP29

IP TO SECURE DEVICES IN A HOSTILE WORLD

Time: 1:30 - 3:00pm || Room: N264 || Event Type: IP Track

Keywords: System Security, Hardware Security, Security & Privacy || Topic Area: IP

CHAIR & ORGANIZER:

Henning Spruth - NXP Semiconductors, Austin, TX

With wired and wireless connectivity becoming a central feature of more and more everyday devices, security topics require correspondingly greater attention: communication needs to be protected against snooping, interception and tampering; the integrity of the device and its private keys needs to be ensured; its lifecycle needs to be managed; and in-field updates may be necessary to address future threat scenarios. This causes challenges both to the IP designer (to identify and implement the necessary security features) and the IP integrator (to ensure a system view on security and identify weakest links).

In this session, papers from IP providers highlight key topics regarding IP security.

29.1 IoT Security: It Starts with the Silicon

Pim Tuyts - Intrinsic ID, San Francisco, CA

29.2 Building a Complete IoT Security Solution with a Hardware Root of Trust

Ben Levine - Rambus Inc., San Francisco, CA

29.3 Is There A Hole In Your Security Stack?

Marco Ciaffi - Dover Microsystems, Boston, MA

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30

NEXT HOP IN NOC

Time: 3:30 - 5:30pm || Room: N252 || Event Type: Research Reviewed

Keywords: Interconnect/Networking, Architecture & System Design

Topic Area: EDA

CHAIR:

Umit Ogras - Arizona State Univ., Tempe, AZ

CO-CHAIR:

Tauhidur Rahman - Univ. of Massachusetts, Amherst, MA

This session presents six papers highlighting new directions in NoC research. Two papers present Machine Learning techniques for NoC design. One paper presents a novel technique to design secure NoCs. One paper goes into alignment issues in 3D NoCs. One paper presents a novel routing mechanism for bufferless NoCs. The final paper presents a reverse-engineered case study for Intel's Knights Landing.

30.1 ANN Based Admission Control for On-chip Networks

Boqian Wang, Zhonghai Lu - KTH Royal Institute of Technology, Stockholm, Sweden
Shenggang Chen - National Univ. of Defense Technology, Stockholm, Sweden

30.2 An Energy-efficient Network-on-chip Design using Reinforcement Learning

Hao Zheng, Ahmed Louri - George Washington Univ., Washington, DC

30.3 Lightweight Mitigation of Hardware Trojan Attacks in NoC-based Manycore Computing

Venkata Yaswanth Raparti, Sudeep Pasricha - Colorado State Univ., Fort Collins, CO

30.4 Sparse 3-D NoCs with Inductive Coupling

Michihiro Koibuchi - National Institute of Informatics, Tokyo, Japan
Lambert T. Leong - Univ. of Hawaii, Honolulu, HI
Tomohiro Totoki, Naoya Niwa, Hiroki Matsutani, Hideharu Amano - Keio Univ., Yokohama, Japan
Henri Casanova - Univ. of Hawaii, Honolulu, HI

30.5 Surf-Bless: A Confined-interference Routing for Energy-efficient Communication in NoCs

Peng Wang, Sobhan Niknam - Leiden Univ., Leiden, The Netherlands
Sheng Ma, Zhiying Wang - National Univ. of Defense Technology, Hunan, China
Todor Stefanov - Leiden Univ., Leiden, The Netherlands

30.6 Effect of Distributed Directories in Mesh Interconnects

Marcos Horro - Univ. of A Coruña, Spain
Mahmut T. Kandemir - Pennsylvania State Univ., State College, PA
Louis-Noël Pouchet - Colorado State Univ., Fort Collins, CO
Gabriel Rodríguez, Juan Touriño - Univ. of A Coruña, Spain

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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31

EMERGING TECHNOLOGIES MEET INTELLIGENT MACHINES

Time: 3:30 - 5:30pm || Room: N253 || Event Type: Research Reviewed

Keywords: Emerging Technologies, Architecture & System Design || Topic Area: Design

CHAIR:

Yingyezhe Jim - Facebook, San Jose, CA

CO-CHAIR:

Siddharth Joshi - Univ. of Notre Dame, Notre Dame, IN

This session highlights recent advances in emerging device technologies for hardware implementation of neural networks. The first two papers discuss novel coding techniques for hyper-dimensional and neuromorphic computing. The third paper presents a reconfigurable RRAM based CNN accelerator. The next two papers present fault-tolerant designs using non-reliable devices. Finally, the session concludes with an exciting paper on computing models with emerging devices.

***31.1 BRIC: Locality-based Encoding for Energy-efficient Brain-inspired Hyperdimensional Computing**

Mohsen Imani, Justin L. Morris, John Messerly, Helen Shu, Yaobang Deng, Tajana Rosing - Univ. of California, San Diego, La Jolla, CA

31.2 Fast and Efficient Information Transmission with Burst Spikes in Deep Spiking Neural Networks

Seongsik Park, Seijoong Kim, Hyekjun Choe, Sungroh Yoon - Seoul National Univ., Seoul, Republic of Korea

31.3 Deep-DFR: A Memristive Deep Delayed Feedback Reservoir Computing System with Hybrid Neural Network Topology

Kangjun Bai, Qiyuan An, Yang (Cindy) Yi - Virginia Polytechnic Institute and State Univ., Blacksburg, VA

31.4 A Fault-tolerant Neural Network Architecture

Tao Liu, Wujie Wen - Florida International Univ., Miami, FL

Lei Jiang - Indiana Univ., Bloomington, IN

Yanzhi Wang - Northeastern Univ., Boston, MA

Chengmo Yang - Univ. of Delaware, Newark, DE

Gang Quan - Florida International Univ., Miami, FL

31.5 A Configurable Multi-precision CNN Computing Framework Based on Single Bit RRAM

Zhenhua Zhu, Hanbo Sun - Tsinghua Univ., Beijing, China

Yujun Lin - Massachusetts Institute of Technology, Cambridge, MA

Guohao Dai - Tsinghua Univ., Beijing, China

Lixue Xia - Alibaba Group Holding Limited, China

Song Han - Massachusetts Institute of Technology, Cambridge, MA

Yu Wang, Huazhong Yang - Tsinghua Univ., Beijing, China

31.6 Noise Injection Adaption: End-to-End ReRAM Crossbar Non-ideal Effect Adaption for Neural Network Mapping

Zhezhi He, Jie Lin, Rickard Ewetz, Jiann-Shiun Yuan, Deliang Fan - Univ. of Central Florida, Orlando, FL

32

LEAKING LIKE A SIEVE: EXPLOITS AND MITIGATIONS FOR ARCHITECTURE SIDE CHANNELS

Time: 3:30 - 5:30pm || Room: N254 || Event Type: Research Reviewed

Keywords: Hardware Security || Topic Area: Security

CHAIR:

Nektarios Tsoutsos - Univ. of Delaware, Newark, DE

CO-CHAIR:

Tauhidur Rahman - Univ. of Alabama, Tuscaloosa, AL

If there is one thing that the recent flood of Spectre and Meltdown-style attacks has shown us, it is that computer architectures leak information like a sieve. This session uncovers new architectural security vulnerabilities, describes architectural mitigation techniques to patch these vulnerabilities, and presents security verification techniques to increase the security of modern architectures.

32.1 A Novel Covert Channel Attack using Memory Encryption Engine Cache

Youngkwang Han, John Kim - Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

32.2 Designing Secure Cryptographic Accelerators with Information Flow Enforcement: A Case Study on AES

Zhenghong Jiang, Hanchen Jin, Edward Suh, Zhiru Zhang - Cornell Univ., Ithaca, NY

32.3 SafeSpec: Banishing the Spectre of a Meltdown with Leakage-free Speculation

Khaled N. Khasawneh, Esmaeil Mohammadian Koruyeh, Chengyu Song - Univ. of California, Riverside, CA

Dmitry Evtyushkin - College of William & Mary, Williamsburg, VA

Dmitry Ponomarev - Binghamton, NY

Nael Abu-Ghazaleh - Univ. of California, Riverside, CA

32.4 SpectreGuard: An Efficient Data-centric Defense Mechanism Against Spectre Attacks

Jacob Fustos, Farzad Farshchi, Heechul Yun - Univ. of Kansas, Lawrence, KS

32.5 PAPP: Prefetcher-aware Prime and Probe Side-channel Attack

Daimeng Wang, Zhiyun Qian, Nael Abu-Ghazaleh, Srikanth V. Krishnamurthy - Univ. of California, Riverside, CA

32.6 HardScope: Hardening Embedded Systems Against Data-oriented Attacks

Thomas Nyman - Aalto Univ., Espoo, Finland

Ghada Dessouky, Shaza Zeitouni - Technische Univ. Darmstadt, Germany

Aaro Lehtikoinen, Andrew Paverd, N. Asokan - Aalto Univ., Espoo, Finland

Ahmad-Reza Sadeghi - Technische Univ. Darmstadt, Germany

* Denotes best paper candidate

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

33

DESIGN BETTER ANALOG -- FASTER!

Time: 3:30 - 5:30pm || Room: N255 || Event Type: Research Reviewed

Keywords: Analog & Mixed Signal, Back-end Design, Front-end Design || Topic Area: EDA

CHAIR:

Jongeon Lee - Ulsan National Institute of Science and Technology (UNIST)
Republlic of Korea

CO-CHAIR:

Sri Parameswaran - Univ. of New South Wales, Australia

The session contains the newest advances in analog circuit design automation covering a variety of topics. Faster approaches to the problem of analog circuit sizing and synthesis using multi-fidelity Bayesian optimization and sparse regression modeling are discussed in the first two papers. Then, a generative adversarial networks based approach is proposed to automate analog layout generation. Next, a digital-compatible flow including synthesis, placement, and implementation is proposed for the emerging class of time-domain computing circuits. Finally, the last two papers demonstrate faster analog simulations enabled by sparsifying reduced-order matrices and enabling exponential and quadratic input stimuli.

33.1 An Efficient Multi-fidelity Bayesian Optimization Approach for Analog Circuit Synthesis

Shuhan Zhang, Wenlong Lyu, Fan Yang, Changhao Yan, Dian Zhou, Xuan Zeng - Fudan Univ., Shanghai, China
Xiangdong Hu - Shanghai High Performance Integrated Circuit Design Center, Shanghai, China

33.2 Rethinking Sparsity in Performance Modeling for Analog and Mixed Circuits using Spike and Slab Models

Mohamed Baker Alawieh, Sinead A. Williamson, David Z. Pan - Univ. of Texas at Austin, TX

33.3 WellGAN: Generative-adversarial-network-guided Well Generation for Analog/Mixed-signal Circuit Layout

Biying Xu, Yibo Lin, Shaolan Li, Xiyuan Tang, Linxiao Shen, Nan Sun, David Z. Pan - Univ. of Texas at Austin, TX

33.4 Digital Compatible Synthesis, Placement and Implementation of Mixed-signal Time-domain Computing

Zhengyu Chen, Hai Zhou, Jie Gu - Northwestern Univ., Evanston, IL

33.5 A Rigorous Approach for the Sparsification of Dense Matrices in Model Order Reduction of RLC Circuits

Charalampos Antoniadis, Nestor Evmorfopoulos, Georgios Stamoulis - Univ. of Thessaly, Volos, Greece

33.6 Enabling Complex Stimuli in Accelerated Mixed-signal Simulation

Sara Divanbeigi, Evan Aditya, Zhongpin Wang - Univ. of Hannover, Germany
Markus Olbrich - Leibniz Univ. Hannover, Germany

34

WHAT HAPPENS IN LOGIC SYNTHESIS STAYS IN LOGIC SYNTHESIS

Time: 3:30 - 5:30pm || Room: N257 || Event Type: Research Reviewed

Keywords: Front-end Design || Topic Area: EDA

CO-CHAIR:

Younghyun Ki - Univ. of Wisconsin, Madison, WI

This session presents advances in traditional logic synthesis and emerging applications. Industrial strength synthesis flows show significant improvements to Engineering Change Order (ECO), incremental FPGA synthesis and scalability of core logic optimization. Innovative algorithms show how synthesis extends the state-of-the-art in cryptography, nanotechnology and quantum computing. The papers of this session demonstrate once again the central role of logic synthesis in present EDA and future computing.

34.1 Scalable Generic Logic Synthesis: One Approach to Rule Them All

Heinz Riener, Eleonora Testa, Winston J. Haaswijk - École Polytechnique Fédérale de Lausanne, Switzerland
Alan Mishchenko - Univ. of California, Berkeley, CA
Luca Amarù - Synopsys, Inc., Sunnyvale, CA
Giovanni De Micheli, Mathias Soeken - École Polytechnique Fédérale de Lausanne, Switzerland

34.2 Comprehensive Search for ECO Rectification Using Symbolic Sampling

Victor Kravets - IBM Research, Yorktown, NY
Nian-Ze Lee, Jie-Hong (Roland) Jiang - National Taiwan Univ., Taipei, Taiwan

34.3 Embedding Functions Into Reversible Circuits: A Probabilistic Approach to the Number of Lines

Niels Gleinig, Frances Ann Hubis, Torsten Hoefer - Eidgenössische Technische Hochschule Zürich, Switzerland

34.4 Disjoint-support Decomposition and Extraction for Interconnect-driven Threshold Logic Synthesis

Hao Chen, Shao-Chun Hung, Jie-Hong (Roland) Jiang - National Taiwan Univ., Taipei, Taiwan

34.5 Reducing the Multiplicative Complexity in Logic Networks for Cryptography and Security Applications

Eleonora Testa, Mathias Soeken - École Polytechnique Fédérale de Lausanne, Switzerland
Luca Amarù - Synopsys, Inc., Sunnyvale, CA
Giovanni De Micheli - École Polytechnique Fédérale de Lausanne, Switzerland

34.6 SMatch: Structural Matching for Fast Resynthesis in FPGAs

Rafael Trapani Possignolo, Jose Renau - Univ. of California, Santa Cruz, CA

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TUESDAY, JUNE 4

35

ARCHITECTURE, IP, OR CAD: WHAT'S YOUR PICK FOR SOC SECURITY

Time: 3:30 - 5:30pm || **Room:** N259 || **Event Type:** Panel || **Keywords:** Hardware Security, Verification/Validation, Architecture & System Design || **Topic Area:** Security

MODERATOR:

Swarup Bhunia - Univ. of Florida, Gainesville, FL

ORGANIZERS:

Jay Bhadra - Advanced Micro Devices, Inc., Austin, TX

Wen Chen - NXP Semiconductors, Austin, TX

System on Chips (SoCs) that serve as the backbone of IoT endpoint devices, need to protect the hardware itself against diverse physical attacks, as well as support building secure software, network, and systems. With trust issues arising from an untrusted supply chain and growing demand from the innovative application space, SoC vendors face unprecedented challenges to provide security assurance to device makers, developers and users. The security issues are varied and span all levels – from IPs to systems – and the solutions require significant

re-thinking. The panel, comprised of distinguished members of SoC industry, will debate on defining the right path to SoC security solution in the IoT age. A platform security architecture, an IP-centric security solution, or powerful CAD to accelerate time-to-security – what would make it tick? How to handle untrusted components? What would be the roles of metrics and standards in designing next-gen secure SoC?

PANELISTS:

Serge Leef - Defense Advanced Research Projects Agency, Washington DC

Yervant Zorian - Synopsys, Inc., Mountainview, CA

Eric Peeters - Texas Instruments, Dallas, TX

Ryan Kastner - Univ. of California, San Diego, CA

DT36

HACK@DAC: CATCH ME IF YOU CAN

Time: 3:30 - 5:00pm || **Room:** N260 || **Event Type:** Designer Track

Keywords: Contest, Hardware Security, Security & Privacy || **Topic Area:** Security, EDA

CHAIR:

Dan Holcomb - Univ. of Massachusetts, Amherst, MA

ORGANIZERS:

Jeyavijayan Rajendran - Texas A&M Univ., College Station, TX
Ahmad-Reza Sadeghi - Technische Univ. Darmstadt, Germany

System-on-a-Chip (SoC) designers use third-party intellectual property (3PIP) cores and in-house IP cores to design SoCs. Trustworthiness of such SoCs is undermined by security bugs unintentionally introduced during the integration of these IPs. Each SoC has its own defined usage scenario and corresponding security objectives. When exploited, a security weakness often results in compromise or bypass of at least one of the product security objectives. The goal of Hack@DAC is to develop practical and effective solutions and computer-aided tools to identify such vulnerabilities in buggy SoCs.

The winning teams of Hack@DAC are announced and awarded in this special session, and the teams also present their approaches in this session.

- 36.1** **Hardware and firmware security bugs and exploits for Hack@DAC**
- 36.2** **Finalist team 1 from 2019 Hack@DAC presents their approach Details To Be Determined**
- 36.3** **Finalist team 2 from 2019 Hack@DAC presents their approach Details To Be Determined**
- 36.4** **Finalist team 3 from 2019 Hack@DAC presents their approach Details To Be Determined**
- 36.5** **Finalist team 4 from 2019 Hack@DAC presents their approach Details To Be Determined**

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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TUESDAY, JUNE 4

37

UNLEASHING OPEN SOURCE EDA

Time: 3:30 - 5:30pm || **Room:** N261 || **Event Type:** Special Session
Keywords: Back-end Design, Front-end Design, Analog & Mixed Signal
Topic Area: EDA, Machine Learning/AI

CHAIR:

Noel Menezes - Intel Corp., Hillsboro, OR

ORGANIZER:

Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

The push towards open-source EDA has gathered considerable steam over the past few years. New activities in this arena have primarily been driven by academia through support from funding agencies, but there has also been considerable traction through engagement with industry. This session presents four talks that cover various aspects of open-source design with strong representation from academia and industry.. The first two talks will present perspectives from two one-year-old efforts on digital and analog layout tools, respectively. The last two talks present a “from the trenches” perspective: the third talk is a how-to presentation on the technical side of developing open source code, from a very strong contributor in the open-source community, while the fourth is a presentation that highlights engagement with users, and lessons learned, from one of the most experienced groups that is active in developing open-source tools.

37.1 Toward an Open-source Digital Flow: First Learnings from the OpenROAD Project

Tutu Ajayi - Univ. of Michigan, Ann Arbor, MI

Vidya A. Chhabria - Univ. of Minnesota, Minneapolis, MN

Mateus Fogaça - Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil

Soheil Hashemi - Brown Univ., Providence, RI

Abdelrahman Hosny - Brown Univ., Providence, RI

Andrew B. Kahng, Minsoo Kim - Univ. of California, San Diego, La Jolla, CA

Jeongsup Lee - Univ. of Michigan, Ann Arbor, MI

Uday Mallappa - Univ. of California, San Diego, La Jolla, CA

Marina Neseem - Brown Univ., Providence, RI

Geraldo Pradipta - Univ. of Minnesota, Minneapolis, MN

Sherief Reda - Brown Univ., Providence, RI

Mehdi Saligane - Univ. of Michigan, Ann Arbor, MI

Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

Carl Sechen - Univ. of Texas at Dallas, Dallas, TX

Mohamed Shalan - American Univ. of Cairo, Egypt

William Swartz - Univ. of Texas at Dallas, Dallas, TN

Lutong Wang - Univ. of California, San Diego, La Jolla, CA

Zhehong Wang - Univ. of Michigan, Ann Arbor, MI

Mingyu Woo, Bangqi Xu - Univ. of California, San Diego, La Jolla, CA

37.2 ALIGN: Open-source Analog Layout Automation from the Ground Up

Kishor Kunal, Meghna Madhusudan, Arvind K. Sharma - Univ. of Minnesota, Minneapolis, MN

Wenbin Xu - Texas A&M Univ., College Station, TX

Steven Burns - Intel Corp., Hillsboro, OR

Ramesh Harjani - Univ. of Minnesota, Minneapolis, MN

Jiang Hu - Texas A&M Univ., College Station, TX

Desmond Kirkpatrick - Intel Corp., Hillsboro, OR

Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

37.3 Essential Building Blocks for Creating an Open-source EDA Project

Tsung-Wei Huang, Chun-Xun Lin, Guannan Guo, Martin D F Wong - Univ. of Illinois at Urbana-Champaign, IL

37.4 Open-source EDA Tools and IP: A View from the Trenches

Elad Alon, Krste Asanovic, Jonathan Bachrach, Borivoje Nikolic - Univ. of California, Berkeley, CA

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TUESDAY, JUNE 4

DT38

SPRINT TO THE FINISH LINE

Time: 3:30 - 5:00pm || Room: N262 || Event Type: Designer Track
Keywords: Back-end Design, Implementation, Interconnect/Networking
Topic Area: Design, EDA

CHAIR:

Roman Schwarz - Avera Semiconductor LLC, Research Triangle Park, NC

New challenges calls for finding ways to get faster to design closure. Explore a variety of topics to improve the overall productivity of design flows including focus on bottlenecks with a different lens.

38.1 CTS Jitter: Analysis and Robustness Against Power Supply Noise

Palkesh Jain, Ashwath Prabhu, Mahesh Yatagiri, Dawuth Pathan - Qualcomm India Pvt. Ltd., Bangalore, India
Shuo Wang - Qualcomm Technologies, Inc., San Diego, CA

38.2 Hierarchical Coupled Noise Analysis using Timing Windows Derived from Required Arrival Times

Jason D. Morse, Patrick Williams - IBM Systems Group, Poughkeepsie, NY
Steven Washburn - IBM Corp., Poughkeepsie, NY

38.3 Ultra Low Power High Speed Clock Distribution- A Case for its usage in Energy Efficient Multi-lane PHY

Deepon Saha - Advanced Micro Devices, Inc., Bangalore, India
Milam Paraschou - Advanced Micro Devices, Inc., Fort Collins, CO
Thomas H. Likens, Justin Porter - Advanced Micro Devices, Inc., Austin, TX

38.4 Machine Learning Models for Improving Productivity in ASIC Design Flow

Joydip Das - Samsung Austin R&D Center, Austin, TX
Bowen Li - North Carolina State Univ., Cary, NC
Christopher Peura, Sneha Naidu, Rajesh Gupta, Ahsan Chowdhury, Aaron Lindner, Sandeep Srinivasan - Samsung Austin R&D Center, Austin, TX

38.5 A Hybrid Clock Tree with Multi-spine using Automated Design Methodology for Low Cost and Low Power Complex LSIs

Takashi Hasegawa, Maki Yajima, Makoto Fujiwara, Takanori Saeki - Sony LSI Design Inc., Atsugi, Japan

38.6 Analytical Approach to Optimize Routability in Consideration of Vias

YongDeok Kim, Yeon Gyeong Shin, Sangdo Park, Hyung-Ock Kim, Jung Yun Choi - Samsung Electronics Co., Ltd., Yong-in, Republic of Korea

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IP39

CHALLENGES WITH MEMORY AND SERDES TECHNOLOGIES WITH LATEST APPLICATION DOMAINS

Time: 3:30 - 5:00pm || Room: N264 || Event Type: IP Track

Keywords: Emerging Technologies, Analog & Mixed Signal || Topic Area: IP

CHAIR:

Chirag Dhruv - Advanced Micro Devices, Inc., San Jose, CA

This session focuses on advances and innovations in Memory technologies with latest application domains. The session also focuses on unique Serdes solutions as well as how security mitigation can be achieved with programmable solution. In this submitted paper session, authors from industry brings in unique ideas and views that they have developed by working through day to day challenges they have seen over years, and share their experience with industry.

39.1 OpenRAM Multiport Memory IP

Matthew R. Guthaus, Hunter Nichols, Michael Grimes, Jesse L. Cirimelli-Low, Jennifer Sowash - Univ. of California, Santa Cruz, CA

39.2 Advanced Memory Interfaces for High-performance Systems

Frank Ferro - Rambus Inc., Sunnyvale, CA

39.3 Memory Systems for AI and Leading-edge Applications

Steven Woo, Frank Ferro - Rambus Inc., Sunnyvale, CA

39.4 Super Testchip Methodology - Prototyping Testchips for SerDes IPs

Sangeetha Ramamurthy, Venkatasreekanth Prudvi - GLOBALFOUNDRIES, Bangalore, India

39.5 1Gbps to 112Gbps Multi-standard SerDes (MSS) IP Supporting Leading Edge NRZ And PAM Data Center Standards

Tony Pialis, - AlphaWave IP Corp., Toronto, ON, Canada
Clint Walker - AlphaWave IP Corp., Hood River, OR
Kent Orthner, Volkan Oktem - Achronix Semiconductor Corp., Santa Clara, CA

39.6 Implementing Strong and Programmable Security to Mitigate IoT Threats

Steve Singer - Rambus Inc., Sunnyvale, CA

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TUESDAY, JUNE 4

DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Time: 5:00 - 6:00pm || Exhibit Floor || Event Type: Designer and IP Track Poster

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Tuesday, June 4 from 5:00 to 6:00pm on the Exhibit Floor.

124.1 Machine Learning Techniques for Minimizing PVT Corner Analyses and Library Validation

Prateek Pendyala - Intel Technology India Pvt. Ltd, Bangalore, India
Akash Hegde - Carnegie Mellon Univ., Pittsburgh, PA
Suryansh Sahota - Intel Technology India Pvt. Ltd, Bangalore, India

124.2 Comprehensive Analog Layout Constraint Verification for Matching Devices

Hirokazu Kitamura, Saburo Hojo - Renesas Electronics Corp., Kodaira-shi, Japan
Kazuyuki Oya - Mentor, A Siemens Business, Shinagawa-ku, Japan
Toshiyuki Usui - Hitachi Ltd., Yokohama, Japan

124.3 Managing Electrical Reliability During Layout Implementation

Atul Bhargava, Akshita Mishra - STMicroelectronics, Greater Noida, India
Vishesh Kumar - Cadence Design Systems, India Pvt. Ltd., Noida, India

124.4 System Level Power – Thermal Analysis using Computational Fluid Dynamics (CFD) Simulation and Machine Learning

Wook Kim - Yunhyeok Im, Youngsang Cho, Joohee Choung - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Myunghoon Lee - ANSYS, Inc., Seoul-si, Republic of Korea
Varmsi Krishna Yaddanapudi - ANSYS, Inc., Bangalore, India

124.5 Solving IP Quality Challenges in Complex IP

Kalyani Challa, Curtis M. Webster - Synopsys, Inc., Mountain View, CA

124.6 Rapid Prototyping of Dynamic Voltage Drop using Combinations of Block Level Scenarios

Byunghyun Lee, Dongyoun Yi, Yongho Lee - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Mathew J. Kaipanatu - ANSYS, Inc., Bangalore, India
Rahul Rajan - ANSYS, Inc., San Jose, CA
Suresh K. Mantena, Sankar Ramachandran - ANSYS, Inc., Bangalore, India

124.7 Enabling Exhaustive Reset Verification in Intel Design

Rohit K. Sinha - Intel Technology India Pvt. Ltd, Bangalore, India

124.8 Hybrid Configurable Platform for HW&SW Co-development and Co-validation

Hyunjae Woo, Youngsik Kim, Seonil B. Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea

124.9 Pin FMEA of TPS65313 Device Using Analog Fault Simulation

Vijaykumar Sankaran - Cadence Design Systems, India Pvt. Ltd., Bengaluru, India

Tahsin Alim - Texas Instruments, Inc., Dallas, TX

Samir Camdzic - Texas Instruments, Inc., Freising, Germany

Tulong Yang - Texas Instruments, Dallas, TX

Chanakya K V, Sumit Kumar - Texas Instruments India Pvt. Ltd., Bengaluru, India

Victor Zhuk - Cadence Design Systems, Inc., San Jose, CA

Amit Bajaj - Cadence Design Systems, India Pvt. Ltd., Noida, India

Ayesha Chowdhury - Texas Instruments, Inc., Dallas, TX

124.10 A Low-power Triple-Vdd Dual-core Motion Estimation Chip Design and Implementation for a Wireless Panoramic Endoscopy

Ching-Hwa Cheng - Feng Chia Univ., Taichung, Taiwan

124.11 Customizing FPGA Implementation Flows for Domain-specific Applications

Chris Lavin, Alireza Kaviani - Xilinx Inc., San Jose, CA

124.12 A Continuous Microprocessor Delivery Pipeline using Feature based Development

Eduard Herkel, Gerrit Koch, Bodo Hoppe - IBM Deutschland Research & Development GmbH, Boeblingen, Germany

124.13 Low Power Validation of Heterogeneous SoCs Using Portable Stimulus Standard

Joydeep Maitra, Vikash K. Singh - Intel Technology India Pvt. Ltd, Bengaluru, India

124.14 A Transistor Level IR-drop based Method to Characterize an Accurate and Compact Model of an IP for SoC Level IR-EM Analysis

Paul Mathew, Shivaraj Byru - NXP Semiconductors, Noida, India

Anant Narain - ANSYS, Inc., Noida, India

Akarshan Arora - NXP Semiconductors, Noida, India

124.15 A Fast and accurate Solution To Verify Layout Efficiency And Reliability For Power Management IC(PMIC) Design

Xuan Wang - HiSilicon, Shanghai, China

Jie Cheng - ANSYS, Inc., Shanghai, China

Biran Li - HiSilicon, Shanghai, China

Hong Jia - ANSYS, Inc., Shanghai, China

124.16 A Smart RTL Linting Tool with Auto-correction

Khaled S. Mohamed - Mentor, A Siemens Business, Cairo, Egypt

124.17 Accurate and Correct-by-Construct Hold Margin Methodology for Standard cells

Gaurav K. Varshney, Rashmi Sachan, Tanvi Sharma - Texas Instruments India Pvt. Ltd., Bangalore, India

124.18 Congestion Aware Buffer Planner for Complex Design Structure

Mukesh D. Bagul, Vishal Rajvedi - GLOBALFOUNDRIES, Bangalore, India

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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TUESDAY, JUNE 4

DESIGNER/IP TRACK POSTER SESSION

124.19 Enhancing Functional Debug Capabilities using ALLSCAN Test Structures

Hardik Bhagat, Sreekanth Pai, Kavitha Shankar, Balaji Upputuri - GLOBALFOUNDRIES, Bangalore, India

124.20 Improve Hardware Assurance (HwA) using FPGA IP in your ASICs and SoCs

Raymond Nijssen, Quinn Jacobson - Achronix Semiconductor Corp., Santa Clara, CA

124.21 STA Compatible Netlist CDC Methodology

Ulhas Kotha, Pratik Suthar - NVIDIA Corp., Bangalore, India
Ankush Bagotra - Synopsys, Inc., Sunnyvale, CA
Ravindra Nibandhe - Synopsys India Pvt. Ltd., Karnataka, India

124.22 Application of Tempus Scope for Accelerated Timing Signoff

Tim Helvey - GLOBALFOUNDRIES, Rochester, MN
Parth Lakhya - Cyient, Pune, India
Jay Gaudani - GLOBALFOUNDRIES, Santa Clara, CA
Tim Sterczyk - Cyient, Ottawa, ON Canada

124.23 A Novel Methodology for Fast PDN Sign-off by Slicing Long-vectors

Udayakumar Yedakuppam - Infineon Technologies, Bengaluru, India
Soenke Grimpel - Infineon Technologies, Munich, Germany
Dileesh Jostin, Manali Khare - ANSYS, Inc., Bengaluru, India

124.24 Early-stage Power Check Methodology for IP Power Audit

Jinsuk Youn - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Jeongwon Kang - ANSYS, Inc., Seoul, Republic of Korea
Seonghoon Kim, Chul Rim, Naya Ha, Kyungtae Do, Jung Yun Choi - Samsung Electronics Co., Ltd., Yong-in, Republic of Korea

124.25 Configurable Multi-protocol AUTOSAR-based Secure Communication Accelerator

Ahmed Hamed - Mentor, A Siemens Business, Cairo, Egypt
Mona Safar, M. Watheq El-Kharashi - Ain Shams Univ., Cairo, Egypt
Ashraf Salem - Mentor, A Siemens Business, Cairo, Egypt

124.26 A Method to Build Clock Tree Comprehending Switching Activity to Address DVD in an SOC

Atul Garg - Texas Instruments India Pvt. Ltd., Bangalore, India
Venkatraman Ramakrishnan - Texas Instruments India Pvt. Ltd., Bangalore, India

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120**NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION****Time: 6:00 - 7:00pm || Exhibit Floor || Event Type: Work-In-Progress**

Join us on the Exhibit Floor to see Work-in-Progress posters and enjoy light snacks and beverages.

120.1 A Spectral Approach to Scalable Vectorless Thermal Integrity Verification

Zhiqiang Zhao, Zhuo Feng - Michigan Technological Univ., Houghton, MI

120.2 A Novel Design Framework for High-variation Carbon Nanotube-based Transistor Technology

Aporva Amarnath, Javad Bagherzadeh, Jielun Tan, Ronald Dreslinski - Univ. of Michigan, Ann Arbor, MI

120.3 Semi Supervised Learning of Multi-dimensional Analog Circuits

Rahul Dutta, Salahuddin Raju, Ashish James, Bruno Lecouat, Chemmada John Leo, Yong-Joon Jeon - Agency for Science, Technology and Research (A*STAR), Singapore
Balagopal Unnikrishnan - National Univ. of Singapore
Chuan-Sheng Foo - Institute for Infocomm Research, Singapore
Zeng Zeng, Kevin Chai Tshun Chuan, Vijay Ramaseshan Chandrasekha - Agency for Science, Technology and Research (A*STAR), Singapore

120.4 Boosting the Profitability of NVRAM-based Storage Devices via the Concept of Dual-chunking Data Deduplication

Shuo-Han Chen - Academia Sinica, Taipei, Taiwan
Min-Hong Shen - National Tsing Hua Univ., Hsinchu, Taiwan
Hsin-Wen Wei - Tamkang Univ., Taipei, Taiwan
Wei-kuan Shih - National Tsing Hua Univ., Hsin-chu, Taiwan

120.5 Memory Locking: An Automated Approach to Processor Design Obfuscation

Michael Zuzak, Ankur Srivastava - Univ. of Maryland, College Park, MD

120.6 Is Robust Design-for-security Robust Enough?: A Sensitization Attack on Locked Circuits with Restricted Scan Chain Access

Nimisha Limaye, Abhrajit Sengupta - New York Univ., New York City, NY
Mohammed Thari Nabeel, Ozgur Sinanoglu - New York Univ., Abu Dhabi, United Arab Emirates

120.7 Fast Thermal Modeling of Two-phase Vapor Chambers with Micropillar Wick Evaporators for Processor Cooling

Zihao Yuan - Boston Univ., Boston, MA
Geoffrey Vaartstra - Massachusetts Institute of Technology, Cambridge, MA
Prachi Shukla - Boston Univ., Boston, MA
Mostafa Abdelrehim, Sherief Reda - Brown Univ., Providence, RI
Evelyn Wang - Massachusetts Institute of Technology, Cambridge, MA
Ayse K. Coskun - Boston Univ., Boston, MA

120.8 Karna: A Security Aware EDA Flow for Improved Side-channel Attack Protection

Patanjali S. L. P. S. K., Prasanna Karthik Vairam, Chester D. Rebeiro, Kamakoti Veezhinathan - Indian Institute of Technology Madras, Chennai, Tamil Nadu, India

120.9 Converting Flip-flop to 3-phase Latch-based Designs

Huimei Cheng, Peter Beerel - Univ. of Southern California, Los Angeles, CA

120.10 Software/Hardware Codesign of the Post Quantum Cryptography Algorithm NTRUEncrypt Using High-level Synthesis and Register-transfer Level Design Methodologies

Farnoud Farahmand, Duc Tri Nguyen, Viet B. Dang, Ahmed Ferozpuri, Kris Gaj - George Mason Univ., Fairfax, VA

120.11 Pseudo Agent-based Multi-objective Hyperparameter Optimization for Efficient Neural Accelerator Design

Maryam Parsa, Aayush Ankit, Kaushik Roy - Purdue Univ., West Lafayette, IN

120.12 Performance Optimization of Dataflow Circuits

Lana Josipovic, Andrea Guerrieri, Paolo lenne - École Polytechnique Fédérale de Lausanne, Switzerland
Jordi Cortadella - Univ. Politècnica de Catalunya, Spain

120.13 Estimating the Circuit Deobfuscating Runtime Based on Graph Deep Learning

Zhiqian Chen - Virginia Polytechnic Institute and State Univ., Falls Church, VA
Gaurav S. Kolhe, Setareh Rafatirad - George Mason Univ., Fairfax, VA
Chang-Tien Lu - Virginia Polytechnic Institute and State Univ., Falls Church, VA
Sai Manoj Pudukotai Dinakarao, Houman Homayoun, Liang Zhao - George Mason Univ., Fairfax, VA

120.14 Enhancing Fault Tolerance of Neural Network for Security-critical Applications

Manaar Alam, Arnab Bag, Debapriya Basu Roy - Indian Institute of Technology Kharagpur, India
Dirmanto Jap - Nanyang Technological Univ., Singapore
Jakub Breier - UL, LLC, Singapore
Shivam Bhasin - Nanyang Technological Univ., Singapore
Debdeep Mukhopadhyay - Indian Institute of Technology Kharagpur, India

120.15 Efficient Reduction of Large Circuit Models Over Limited Frequency Windows

George Floros, Nestor Evmorfopoulos, George Stamoulis - Univ. of Thessaly, Volos, Greece

120.16 Dataflow Acceleration of Smith-waterman with Traceback for High Throughput Next Generation Sequencing

Konstantina Koliogeorgi - National Technical Univ. of Athens, Athens, Greece
Nils Voss, Sotiria Fytraki - Maxeler Technologies, Inc., United Kingdom
Sotirios Xydis - National Technical Univ. of Athens, Athens, Greece
Georgi Gaydadjiev - Maxeler Technologies, Inc., United Kingdom
Dimitrios Soudris - National Technical Univ. of Athens, Athens, Greece

120.17 High Speed Pseudo-write Assist Circuits for SRAM to Tackle High Metal Resistances in 7nm Technology and Beyond

Akash Bangalore Srinivasa, Arjunesh Namboothiri Madhavan, Sujit Kumar Rout, Paban Kumar Saha - Arm, Ltd., Bangalore, India

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WORK-IN-PROGRESS POSTER SESSION

120.18 3PXNet: Pruned-permuted-packed XNOR Networks for Edge Machine Learning

Wojciech Romaszkan, Tianmu Li, Puneet Gupta - Univ. of California, Los Angeles, CA

120.19 A Reconfigurable Layered-based Bio-inspired Smart Image Sensor

Pankaj Bhowmik, Md Jubaer Hossain H. Pantho, Sujan kumar Saha, Christophe Bobda - Univ. of Arkansas, Fayetteville, AR

120.20 Reducing the Read Energy of Reconfigurable SRAM with Finer-grained Data Feature Exploitation

Han Xu, Ziru Li, Fei Qiao, Qi Wei, Xinjun Liu, Huazhong Yang - Tsinghua Univ., Beijing, China

120.21 Enabling Energy-efficient 360-Degree Video Rendering on FPGA via Algorithm-architecture Co-design

Qiuyue Sun, Yawo A. Siatitse, Amir Taherin, Yuhao Zhu - Univ. of Rochester, Rochester, NY

120.22 Machine-learning Based Wire Delay Prediction on Tree and Non-tree Net Structures

Hsien-Han Cheng - National Chiao Tung Univ., Hsinchu, Taiwan
Iris Hui-Ru Jiang - National Taiwan Univ., Taipei, Taiwan
Oscar Ou - MediaTek, Inc., San Jose, CA

120.23 Power Optimization for Emerging NVM-based NVMe SSD Through Self Performance Training

Bo-Eok Seo, Joon-Sung Yang - Sungkyunkwan Univ., Suwon, South Korea

120.24 PVTMC: An All-digital Sub-picosecond Timing Measurement Circuit Based on Process Variations

Shuo Li - Univ. of Massachusetts, Amherst, MA
Xiaolin Xu - Univ. of Illinois at Chicago, IL
Wayne Burleson - Univ. of Massachusetts, Amherst, MA

120.25 Towards Hardware-based Stealthy Malware Detection

Hossein Sayadi, Yifeng Gao, Hosein Makrani, Sai Manoj P D, Setareh Rafatirad, Jessica Lin, Houman Homayoun - George Mason Univ., Fairfax, VA

120.26 Flexible Mining of Causal Relations from Hybrid System Traces

Antonio A. Bruto da Costa, Pallab Dasgupta - Indian Institute of Technology Kharagpur, India
Goran Frehse - ENSTA ParisTech, École Nationale Supérieure de Techniques Avancées, Palaiseau Cedex, France

120.27 Flipy: Efficient Pattern Redistribution for Enhancing MLC PCM Reliability and Storage Density

Muhammad Imran, Taehyun Kwon, Jung Min You, Joon-Sung Yang - Sungkyunkwan Univ., Suwon, Republic of Korea

120.28 EM-Aware Optimization for Multi-segment Power Grid Networks Considering Saturation Volume

Han Zhou, Zeyu Sun, Shuyuan Yu, Sheldon Tan - Univ. of California, Riverside, CA

120.29 Passive or Active: Determination of Cost-optimal Interposer Technology for Chiplet Integration

Dylan Stow, Itir Akgun, Yuan Xie - Univ. of California, Santa Barbara, CA

120.30 Projecting Future Power Trends in Die-stacked Memory

Dylan Stow - Univ. of California, Santa Barbara, CA
Amin Farmahini-Farahani, Sudhanva Gurumurthi, Michael Ignatowski - Advanced Micro Devices, Inc., Austin, TX
Yuan Xie - Univ. of California, Santa Barbara, CA

120.31 ApGAN: Approximate GAN for Robust Low-energy Learning from Imprecise Components

Arman Roohi, Shaahin Angizi, Shadi Sheikhfaal, Deliang Fan, Ronald F. DeMara - Univ. of Central Florida, Orlando, FL

120.32 Duery: Enabling Write-reduction Multi-version Index Scheme with Efficient Dual-range Query Over NVRAM

I-Ju Wang - National Tsing Hua Univ., Hsinchu, Taiwan
Tseng-Yi Chen - Yuan Ze Univ., Taoyuan, Taiwan
Shuo-Han Chen - Chinese Univ. of Hong Kong, Shatin, Hong Kong
Hsin-Wen Wei - Tamkang Univ., Taipei, Taiwan
Wei-kuan Shih - National Tsing Hua Univ., Hsin-chu, Taiwan

120.33 Agile SMT Based Place and Route for CGRAs with Restricted Routing Networks

Caleb Donovick, Makai Mann, Pat Hanrahan, Clark Barrett - Stanford Univ., Stanford, CA

120.34 A PVT-aware Voltage Scaling Method Targeting Energy Efficient FPGAs

Konstantinos Maragos, George Lentaris, Dimitrios Soudris - National Technical Univ. of Athens, Greece
Vasilis Pavlidis - Univ. of Manchester, United Kingdom

120.35 Small Delay Fault Diagnosis with Compacted Responses

Stefan Holst - Kyushu Institute of Technology, Iizuka, Japan
Eric Schneider - Univ. of Stuttgart, Germany
Michael A. Kochte - Consultant, Oslo, Norway
Xiaoqing Wen - Kyushu Institute of Technology, Iizuka, Japan
Hans-Joachim Wunderlich - Univ. of Stuttgart, Germany

120.36 Application of Topological and Lexicographic Boolean Satisfiability in On-track Bus Routing

He-Teng Zhang - National Taiwan Univ., Taipei, Taiwan
Masahiro Fujita - Univ. of Tokyo, Japan
Chung-Kuan Cheng - Univ. of California, San Diego, La Jolla, CA
Jie-Hong R. Jiang - National Taiwan Univ., Taipei, Taiwan

120.37 Soft Error Reliability Analysis of Autonomous Vehicles Software Stack

Felipe Rosa, Vitor Bandeira, Isadora Oliveira, Ricardo Reis - Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil
Luciano Ost - Loughborough Univ., Loughborough, United Kingdom

120.38 Dynamic Buffer Voltage Scaling for Energy-efficient Convolutional Neural Network

Minho Ha, Younghoon Byun, Youngjoo Lee, Sunggu Lee - Pohang Univ. of Science and Technology, Pohang, Republic of Korea

120.39 Defect Mitigation in Resistive Crossbars for Analog VectorMatrix Multiplication

Fan Zhang, Miao Hu - Binghamton Univ., Binghamton, NY

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

TUESDAY, JUNE 4

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Exhibit Floor || Event Type: Networking

Join us on the Exhibit Floor to see Work-in-Progress posters and enjoy snacks and beverages.

Thank you to our Reception Sponsor:



ACM SIGDA AND IEEE CEDA PH.D. FORUM

Time: 7:00 - 9:00pm || Room: N246 || Event Type: Additional Meeting

Topic Area: EDA

ORGANIZERS:

Helen Li - Duke Univ., Durham, NC
Umit Ogras - Arizona State Univ., Tempe, AZ
Rasit Topaloglu - IBM Corp., Hopewell, NY
Yiyu Shi - Univ. of Notre Dame, Notre Dame, IN

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community. Participation in the forum is highly competitive with acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

For more information, please visit the ACM SIGDA Ph.D. Forum website.

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WEDNESDAY, JUNE 5



KEYNOTE: PRIORITIZING PLAY IN AN AUTOMATED AGE

JOHN COHN – Massachusetts Institute of Technology & IBM Watson AI Lab, Cambridge, MA

Time: 8:45 – 9:15am | Keynote Booth 1145

Explore the critical role experimentation, failure, challenge, adventure and fun have played in the life and work of John Cohn, IBM Fellow at the MIT-IBM Watson AI Lab. Follow his path from EDA developer, to board room

to eating rats on reality TV! Find out how prioritizing play unlocks the gateway to creativity, innovation, invention and human potential, and how to avoid a homogenized existence in an automated age.



KEYNOTE: FROM STUDENT PROJECT TO TACKLING THE MAJOR CHALLENGES IN REALIZING SAFE & SUSTAINABLE ELECTRIC VEHICLES

BAS VERKAIK – SPIKE, Eindhoven, The Netherlands

Time: 9:20 - 10:00am | Keynote Booth 1145

In 2014, a group of students from the Eindhoven University of Technology set a clear goal to ride around the world in 80 days on an electric motorcycle to show the world what electric vehicles were capable of. Since a suitable motorcycle to undertake such a tour didn't exist yet, the Dutch students decided to entirely develop it by themselves. A revolutionary vehicle was the result: 400 km range from a self-developed swappable and modular battery pack. After completing the 80-day world tour late 2016, the unique knowledge and experience gained in this project was made commercial by founding the spinoff SPIKE Technologies. SPIKE aims to accelerate the transition towards safe & clean mobility by designing & developing high quality powertrain components for electric vehicles. Among these components are SPIKE's battery solutions, that distinguish themselves due to their safety, performance and lifetime, while they can be produced very cost-efficiently due to their unique design. Until now, SPIKE has supported in the

development of a wide variety of electric vehicles and recently established its own battery production facility in the Netherlands.

In his talk, Bas Verkaik will explain the complex design decisions that had to be made in developing the electric motorcycle and they now have to make every day to cope with the rapidly changing developments in the electric vehicle market.

Biography: Bas Verkaik holds a MSc degree in Sustainable Energy Technology at the Eindhoven University of Technology. As part of his study program, he was part of the STORM Eindhoven team from the beginning in 2014. This team of 23 students set a clear goal to ride around the world in 80 days, on an electric motorcycle. After finishing the unique 80-day world tour in 2016, Bas founded the STORM spinoff SPIKE Technologies, that is developing high quality components for electric vehicles.

40
REMEMBER TO LEARN!

Time: 10:30am - 12:00pm || Room: N252 || Event Type: Research Reviewed
Keywords: Analog & Mixed Signal, Architecture & System Design, Implementation
Topic Area: Design, Machine Learning/AI

CHAIR:

Kaushik Mazumdar - Advanced Micro Devices, Inc., Fort Collins, CO

CO-CHAIR:

Swagat Venkataram - IBM T.J. Watson Research Center, Yorktown Heights, NY

This session is all about using memory in various forms for machine learning applications. The first paper in the session describes the design of a smart dataflow to reduce the precious on-chip memory footprint and computational cost for face detection and alignment, while the second paper presents a generic error model for mixed-signal in-memory computation engines for deep learning inference. The third paper presents a novel memory cell leveraging emerging ferroelectric field-effect transistors for symmetric memory access, providing a means for efficient matrix operations. The last paper in the session presents a fast and reliable 6T SRAM-based in-memory computing architecture that distributes simultaneous wordline accesses to improve design margins and enable wide-voltage-range operation.

***40.1 A 1.17 TOPS/W, 150fps Accelerator for Multi-face Detection and Alignment**

Huiyu Mo, Leibo Liu - Tsinghua Univ., Beijing, China
 Wenping Zhu - Chinese Academy of Sciences, Beijing, China
 Qiang Li - Intel Corp., Beijing, China
 Hong Liu, Wenjing Hu, Yao Wang, Shaojun Wei - Tsinghua Univ., Beijing, China

40.2 Analog/Mixed-signal Hardware Error Modeling for Deep Learning Inference

Angad S. Rekhi - Stanford Univ., Stanford, CA
 Brian Zimmer, Nikola Nedovic - NVIDIA Corp., Santa Clara, CA
 Ningxi Liu - Univ. of Virginia, Charlottesville, VA
 Rangharajan Venkatesan - NVIDIA Corp., Santa Clara, CA
 Miaorong Wang - Massachusetts Institute of Technology, Cambridge, MA
 Brucek Khailany, William J. Dally, C. Thomas Gray - NVIDIA Corp., Durham, NC

40.3 A 3T/Cell Practical Embedded Nonvolatile Memory Supporting Symmetric Read and Write Access Based on Ferroelectric FETs

Juejian Wu, Hongtao Zhong - Tsinghua Univ., Beijing, China
 Kai Ni - Univ. of Notre Dame, Notre Dame, IN
 Yongpan Liu, Huazhong Yang, Xueqing Li - Tsinghua Univ., Beijing, China

40.4 A Fast, Reliable and Wide-voltage-range In-memory Computing Architecture

William A. Simon, Juan Galicia, Alexandre Levisse, Marina Zapater, David Atienza - École Polytechnique Fédérale de Lausanne, Switzerland

41
ZEROS IN NEURAL NETWORKS? STEP OUT PLEASE.

Time: 10:30am - 12:00pm || Room: N253 || Event Type: Research Reviewed
Keywords: Architecture & System Design, Low Power || Topic Area: Machine Learning/AI

CHAIR:

Norbert Wehn - Technische Univ. Kaiserslautern, Germany

CO-CHAIR:

Ashish Ranjan - IBM T.J. Watson Research Center, Yorktown Heights, NY

Taking advantage of sparse data and variable precision can provide a unique edge in energy efficiency when accelerating deep neural networks. In this session, we have four papers focusing on techniques for precision scaling and compute compression to realize maximum energy efficiency in both inference and training.

41.1 BitBlade: Area and Energy-efficient Precision-scalable Neural Network Accelerator with Bitwise Summation

Sungju Ryu, Hyunjun Kim, Wooseok Yi, Jae-Joon Kim - Pohang Univ. of Science and Technology, Pohang, Republic of Korea

41.2 Acceleration of DNN Backward Propagation by Selective Computation of Gradients

Gunhee Lee, Hannmin Park, Namhyung Kim, Joonsang Yu, Sujeong Jo, Kiyoung Choi - Seoul National Univ., Seoul, Republic of Korea

41.3 C3-flow: Compute Compression Co-design Flow for Deep Neural Networks

Matthew A. Sotoudeh - Univ. of California, Davis, CA
 Sara S. Baghsorkhi - Intel Corp., Santa Clara, CA

41.4 ABM-spConv: A Novel Approach to FPGA-based Acceleration of Convolutional Neural Network Inference

Dong Wang, Ke Xu, Qun Jia - Beijing Jiaotong Univ., China
 Soheil Ghiasi - Univ. of California, Davis, CA

* Denotes best paper candidate

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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HIDE AND SEEK: ENCRYPTION AND OBFUSCATION

Time: 10:30am - 12:00pm || **Room:** N254 || **Event Type:** Research Reviewed

Keywords: Hardware Security || **Topic Area:** Security

CHAIR:

Saverio Fazzari - Booz Allen Hamilton, Inc., McLean, VA

CO-CHAIR:

Michael Orshansky - Univ. of Texas at Austin, TX

This session presents methods and tools for quantum-resilient cryptography and piracy-resilient hardware. Come, learn about building theory and tool chains for securing post-quantum cryptography through speeding up the Gaussian sampling process, obfuscation-based countermeasures against circuit piracy and reverse-engineering, and non-volatile memories.

42.1 Pushing the Speed Limit of Constant-time Discrete Gaussian Sampling. A Case Study on Falcon Signature

Angshuman Karmakar - Katholieke Univ. Leuven, Belgium

Sujoy Sinha Roy - Univ. of Birmingham, United Kingdom

Frederik Vercauteren, Ingrid Verbauwhede - KU Leuven, Belgium

42.2 Full-lock: Hard Distributions of SAT Instances for Obfuscating Circuits using Fully Configurable Logic and Routing Blocks

Hadi Mardani Kamali, Kimia Zamiri Azar, Houman Homayoun, Avesta Sasan - George Mason Univ., Fairfax, VA

42.3 A Cellular Automata Guided Obfuscation Strategy For Finite-state-machine Synthesis

Rajit Karmakar - Indian Institute of Technology, Kharagpur, India
Suman Sekhar Jana, Santanu Chattopadhyay - Indian Institute of Technology Kharagpur, India

42.4 An Efficient Spare-line Replacement Scheme to Enhance NVM Security

Jie Xu, Dan Feng, Yu Hua, Fangting Huang, Wen Zhou, Wei Tong, Jingning Liu - Huazhong Univ. of Science & Technology, Wuhan, China

43

PREDICTABILITY IN COMMUNICATION AND COMPUTATION

Time: 10:30am - 12:00pm || **Room:** N255 || **Event Type:** Research Reviewed

Keywords: IoT, Architecture & System Design || **Topic Area:** Embedded Systems & Software (ESS)

CHAIR:

Shuo-Han Chen - Academia Sinica, Taipei, Taiwan

This session covers recent development of system design and analysis to improve the timing predictability in communication and computation. Specifically, the session covers 1) scheduling and analysis of parallel and OpenMP tasks in multiprocessor systems and 2) optimization of time division multiplexing NoC to improve time predictability.

43.1 Analyzing Parallel Real-time Tasks Implemented with Thread Pools

Daniel Casini, Alessandro Biondi, Giorgio Buttazzo - Scuola Superiore Sant'Anna, Pisa, Italy

43.2 Scheduling and Analysis of Parallel Real-time Tasks with Semaphores

Xu Jiang, Nan Guan - Hong Kong Polytechnic Univ., Hong Kong
Weichen Liu - Nanyang Technological Univ., Singapore

Maolin Yang - Univ. of Electronic Science and Technology of China, ChengDu, China

43.3 Real-time Scheduling and Analysis of Synchronous OpenMP Task Systems with Tied Tasks

Jinghao Sun - Northeastern Univ. of China, Shenyang China
Nan Guan - Hong Kong Polytechnic Univ., Hong Kong
Xiaoqing Wang, Chenhan Jin, Yaoyao Chi - Northeastern Univ. of China, Shenyang China

43.4 DCFNoC: A Delayed Conflict-free Time Division Multiplexing Network on Chip

Tomás Picornell, José Flích, Carles Hernández, José Duato - Univ. Politècnica de València, Spain

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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44

SPECIFY, SYNTHESIZE AND ASSERT!

Time: 10:30am - 12:00pm || Room: N257 || Event Type: Research Reviewed

Keywords: Verification/Validation || Topic Area: EDA

CHAIR:

Daniel Grosse - Univ. of Bremen, Germany

CO-CHAIR:

Prabhat Mishr - Univ. of Florida, Gainesville, FL

Manually writing assertions is time consuming and error prone. That's the reason specification mining and synthesis are so important. But pay attention, we cannot generate and synthesize tons of assertions. The first paper focuses on temporal specification mining. The second is about re-optimization of ASIC designs specified as behavioral descriptions for HLS to FPGAs. The third proposes an automatic synthesis technique for clock constraints specification language. Finally, the last paper presents an algorithm for dynamically selecting an effective subset of assertion monitors.

44.1 Learning Temporal Specifications from Imperfect Traces Using Bayesian Inference

Artur Mrowca, Martin Nocker, Sebastian Steinhorst, Stephan Günemann - Tech. Univ. of Munich, Germany

44.2 Accelerating FPGA Prototyping Through Predictive Model-based HLS Design Space Exploration

Shuangnan Liu, Francis Lau - Hong Kong Polytechnic Univ., Hong Kong
Benjamin Carrion Schaefer - Univ. of Texas at Dallas, Richardson, TX

44.3 Sample-guided Automated Synthesis for CCSL Specifications

Ming Hu, Tongquan Wei, Min Zhang - East China Normal Univ., Shanghai, China

Frederic Mallet - Université de Nice Sophia Antipolis, France
Mingsong Chen - East China Normal Univ., Shanghai, China

44.4 DHOOM: Reusing Design-for-debug Hardware for Online Monitoring

Neetu Jindal - Indian Institute of Technology Delhi, India
Sandeep Chandran - Indian Institute of Technology, Palakkad, India
Preeti Ranjan Panda, Sanjiva Prasad, Abhay Mitra, Kunal Singhal, Shubham Gupta, Shikhar Tuli - Indian Institute of Technology Delhi, India

45

CO-DESIGNING HARDWARE AND SOFTWARE FOR SECURE NEXT GENERATION PLATFORMS

Time: 10:30am - 12:00pm || Room: N259 || Event Type: Special Session

Keywords: Hardware Security, System Security, Security & Privacy

Topic Area: Security, Embedded Systems & Software (ESS)

CHAIRS:

Sri Parameswaran - Univ. of New South Wales, Sydney, Australia
Saibal Mukhopadhyay - Georgia Institute of Technology, Atlanta, GA

ORGANIZER:

Rainer Leupers - RWTH Aachen Univ., Aachen, Germany

Next generation platforms are expected to be intelligent and processing or communicating critical information. Hardware and software vulnerabilities in these platforms can be exploited to leak critical information or even to invoke denial of service attacks resulting in catastrophic consequences. Besides, hardware Trojans are showing up as major threats in such these platforms where a software-controlled hardware Trojan can invoke denial of service attack in these platforms at behest of an attacker. Over the years, researchers have looked deeply into the issues related to hardware

and software security. While there is an ongoing debate on whether hardware or software security is more important, we believe that both are equally important. In this special session, we bring together hardware and software security experts from academia and industry to discuss different ways to detect and prevent attacks on next generation platforms.

45.1 Security needs a Better Hardware-software Contract

Gernot Heiser - Univ. of New South Wales, Sydney, Australia

45.2 Untrusted Endpoints are Not an Option

Pim Tuyls - Intrinsic ID, Sunnyvale, CA

45.3 Ensuring System-level Security Through Hardware/Software Security Verification

Jason Oberg - Tortuga Logic, San Jose, CA

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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DT46

TECHNOLOGY TO ACCELERATE EMBEDDED SYSTEMS TIME TO MARKET/ INNOVATIVE SOLUTIONS TO FRONT-END POWER CHALLENGES

Time: 10:30am - 12:00pm || Room: N260 || Event Type: Designer Track

Keywords: Low Power, Front-end Design, Verification/Validation || Topic Area: EDA, Design

CHAIR:

Vivek Tiwari - Intel Corp., Sunnyvale, CA

This session consists of two mini-sessions provided by the ESS and Front End tracks. The first three papers, focusing on ESS, will provide examples of technology processes and design techniques that promote early system integration and reduce system complexity for safety critical systems. The second half of the session showcases innovative techniques for addressing key front-end challenges of low power design, including reset domain crossing, mixed-signal integration, and customized isolation cells.

46.1 Early SW Bring-up Methodology using Full-SoC Level Virtual Prototyping

Woojoo Kim, Jongmin Lee, Seonil B. Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea

46.2 Assessment of Hardware Based RTOS for Safety Critical System

Siaw Chen Lee, Soon Ee Ong - Intel Corp., Penang, Malaysia

46.3 Designing Power-efficient & Safe Autonomous Driving Devices: Using Custom Techniques to Quickly Identify/Fix Hotspots at RTL

Erez Iluz - Intel Corp., Haifa, Israel

46.4 Challenges of Tackling Reset Domain Crossing Verification in a Low Power SoC

Francis Chockalingam, Viral Gorasia - Broadcom Corp., Bangalore, India
Anup Gupta - Synopsys India Pvt. Ltd., Bangalore, India

46.5 Hierarchical Power Intent Driven Efficient Power Integration Methodology for Ultra Low Power Mixed-signal Soc

Aswani Kumar Golla, Venkatraman Ramakrishnan, Gaurav K. Varshney, Lakshmanan Balasubramanian - Texas Instruments India Pvt. Ltd., Bangalore, India

46.6 Improving Low Power Implementation Flow using Special NOR Isolation Cells

Aman Jain, Mohini Somvanshi - Seagate Technology, LLC, Pune, India

Thank you to our Designer Track Sponsor:



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MONOLITHIC 3D IC: BENEFITS, ARCHITECTURES, AND EDA TOOLS

Time: 10:30am - 12:00pm || Room: N261 || Event Type: Special Session

Keywords: Architecture & System Design, Interconnect/Networking, Emerging Technologies || Topic Area: EDA, Design

CHAIR:

Xiaoqing Xu - Arm, Ltd., Austin, TX

ORGANIZER:

Sung Kyu Lim - Georgia Institute of Technology, Atlanta, GA

Two key announcements made in 2018 on TSMC's Wafer-on-Wafer (WoW) technology and Intel's Foveros technology truly paved the way for upcoming commercial 3D IC products in logic applications. Unlike the currently popular micron-scale through-silicon-vias (TSVs) widely adopted in existing memory cube products, these emerging technologies, named monolithic 3D ICs, offer nano-scale inter-die vias for ultra-fine pitch interconnects that are essential in logic 3D ICs. Despite its manifold power, performance, area (PPA) benefits, however, the design complexity of logic monolithic 3D is orders of magnitude higher compared with memory cubes. This requires a paradigm shift in architecture and EDA solutions targeting monolithic 3D ICs. This session presents the current status and future prospect on PPA benefits of monolithic 3D ICs and the required innovations in architecture and EDA tools.

47.1 Monolithic 3D IC Value Proposition: Can This Technology extend Moore's and Dennard's Laws for Logic?

Vassilios Gerousis, Rwik Sengupta - Samsung Austin R&D Center, Austin, TX

47.2 Efficient System Architecture in the Era of Monolithic 3D: Dynamic Inter-tier Interconnect and Processing-in-Memory

Dylan Stow, Itir Akgun, Wenqin Huangfu - Univ. of California, Santa Barbara, CA

Xueqi Li - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

Gabriel H. Loh - Advanced Micro Devices, Inc., Bellevue, WA
Yuan Xie - Univ. of California, Santa Barbara, CA

47.3 RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs

Heechun Park, Kyungwook Chang, Bon Woong Ku, Jinwoo Kim, Edward Lee, Daehyun Kim - Georgia Institute of Technology, Atlanta, GA

Arjun Chaudhuri, Sanmitra Banerjee - Duke Univ., Durham, NC
Saibal Mukhopadhyay - Georgia Institute of Technology, Atlanta, GA

Krishnendu Chakrabarty - Duke Univ., Durham, NC

Sung Kyu Lim - Georgia Institute of Technology, Atlanta, GA

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DT48

THE GROWING UBIQUITY OF OPEN SOURCE HARDWARE AND SOFTWARE FOR EMBEDDED SYSTEMS

Time: 10:30am - 12:00pm || Room: N262 || Event Type: Designer Track

Keywords: IoT, Architecture & System Design, Emerging Technologies

Topic Area: Embedded Systems & Software (ESS), Design

CHAIR & ORGANIZER:

Natraj Ekambaram - NXP Semiconductors, Austin, TX

There are major open source hardware and software projects for embedded systems in industries as varied as IoT, home and industrial automation, drones, and automotive. For example, the Dronecode open source initiative is a platform with everything needed for a complete UAV solution including flight-controller hardware, autopilot software, ground control station, and developer APIs for enhanced/advanced use cases. Cloud providers like AWS provide open device development and starter kits. RISC-V is an open Instruction Set Architecture (ISA) creating its own open hardware and software ecosystem. In this session we will discuss how the open source momentum is changing the way the embedded industry works and collaborates.

Win a HoverGames Drone

Attend this session for a chance to win a new HoverGames drone kit from NXP, a member of Linux Foundation DroneCode.org. This kit uses NXP microcontrollers, sensors and interface components, and runs PX4 flight control software, which is the largest commercially deployed opensource flight stack. Modular and fully extensible, you can add IoT devices and

companion computers for R&D and educational purposes. Learn how to build your own drone and join HoverGames.com coding competitions to win prizes and implement solutions in a large, open source development project.

48.1 Comparing RISC-V Open Source Implementations

Charlie Hauck, Rishiyur Nikhil - Bluespec, Inc., Boston, MA

48.2 FreeRTOS for Microcontrollers and the IoT

Richard Barry - Amazon Development Center, San Jose, CA

48.3 Designing an Open Source Drone Solution that's Business Friendly

Iain Galloway - NXP Semiconductors, Austin, TX

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IP49

WANTED: ANALOG IP DESIGN METHODOLOGIES TO CATCH UP WITH DIGITAL TIME-TO-MARKET

Time: 10:30am - 12:00pm || Room: N264 || Event Type: IP Track

Keywords: Analog & Mixed Signal, Back-end Design || Topic Area: IP

CHAIR & ORGANIZER:

Paul Stravers - Synopsys, Inc., Eindhoven, The Netherlands

Digital design scaling yields 30-40% more transistors with every technology node. But what about the scaling of analog functions? It is common to integrate analog IP designed for node N-2 in a SoC targeting node N, resulting in suboptimal analog functionality. It appears that analog designers have failed to catch up with the aggressive times-to-market required in today's world. Possible solutions could be based on fast redesign or migration, as well as on innovative approaches to analog IP design. Whichever solution we choose, meeting the specification and the required quality criteria is mandatory!

In this session we invite a silicon vendor facing these challenges, describing real-world cases and sharing their expectations for faster IP development. In addition, we will have analog IP vendors talking about emerging solutions based on either faster migration or new design methodologies.

49.1 How to Resize Imager IP to Improve Productivity

Stephane Vivien - STMicroelectronics, Grenoble, France

49.2 Automated Analog Design from Architecture to Implementation

Saeid Ghafouri - Movellus, San Jose, CA

49.3 ID-Xplore: A Cognitive Software for Designing First-time Right Analog IP

Ramy Iskander - Intento Design, Paris, France

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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WEDNESDAY, JUNE 5

DOULOS LUNCH 'N' LEARN TUTORIAL: PYTHON FOR SCIENTIFIC COMPUTING AND DEEP LEARNING

Time: 12:15 - 1:15pm || Room: N246 || Event Type: Thursday is Training Day
Topic Area: EDA

Guaranteed places and lunch for pre-registrants only.

Pre-Registrants also receive a \$50 discount coupon to attend one Doulos main session on 'Thursday is Training Day'

REGISTER NOW!

As well as being a general-purpose programming and scripting language, Python has become one of the most popular languages for scientific computing and more recently for deep learning. Python is everywhere, and Python is cool. Python is easy to learn, and Python programs are

very readable, even by people who don't know Python. There are Python libraries available for doing pretty much anything.

In this tutorial you will learn enough to start using Python as a scripting language and you will become sufficiently familiar with Python to start making sense of the emerging libraries and frameworks used for deep learning, such as TensorFlow and Keras. This tutorial will show you some of the cool things you can do with Python right out-of-the-box!

You can learn more about the Python language and about Deep Learning in the morning and afternoon sessions on 'Thursday is Training Day'.

Thank you to our Sponsor:



THE MEMORY FUTURES

Time: 1:00 - 1:45pm || DAC Pavilion - Booth 871 || Event Type: SKY Talk



Without advances in how the world physically stores and retrieves data, today's most useful devices and algorithms would not exist. The dominant memory chip technologies such as NAND Flash and DRAM rode the wave of innovations in materials, process and device technologies to scale down the path of Moore's law. Although physical scaling is becoming increasingly difficult, the forces and market pull driving cost, power and density scaling are growing relentlessly. The amount of memory in systems for example is increasing geometrically while the power budget continues to decrease. In addition, the applications and resultant memory requirements continue to diversify and expand from traditional handheld devices and larger data centers.

A commitment to innovation and creativity at a system level design is required to meet demands of the data age. These innovations will help fuel the next generation of technologies such as self-driving cars, space exploration, artificial intelligence and machine learning, which sounded like science fiction not so long ago. Several technologies have been proposed over the years with no clear winner. Some of the critical factors which need to be considered for a successful implementation of a new technology include; why and when alternate memory technologies may be needed, what are the performance criteria and related requirements, and what needs to happen in the ecosystem to support a successful new technology. The result of this reality is that bottoms up development for a new memory technology may not feasible due to technical risks and cost and we must target application-specific solutions for new future markets.

Biography: Gurtej Sandhu is Senior Fellow and Vice President at Micron Technology. In his current role, he is responsible for Micron's end-to-end R&D technology roadmaps and to drive cross-functional alignment across various departments and business units to proactively identify technology gaps and managing the engineering organization to resource and execute on developing innovative technology solutions for future memory scaling. Dr. Sandhu's responsibilities include leading several internal project teams worldwide and managing interactions with research consortia around the world. He has held several engineering and management roles and is actively involved with a broad range of process technologies for IC processing and has pioneered several process technologies currently employed in mainstream semiconductor chip manufacturing.

Dr. Sandhu received a degree in electrical engineering at the Indian Institute of Technology, New Delhi, and a Ph.D. in physics at the University of North Carolina, Chapel Hill, in 1990. He holds over 1,300 U.S. patents and is recognized as one of the top inventors in the world. A Fellow of IEEE, he received the prestigious IEEE Andrew S. Grove Award in 2018 for outstanding contributions to solid-state devices and materials technology, as well as for leadership, originality, breadth, among other achievements. This competitive award is presented annually by the IEEE Board of Directors to an individual with pioneering achievements to the semiconductor

SPEAKER:

Gurtej S. Sandhu - Micron Technology, Inc., Boise, ID

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EFFICIENT, RESILIENT, ADAPTIVE IOT

Time: 1:30 - 3:00pm || **Room:** N252 || **Event Type:** Research Reviewed

Keywords: Emerging Technologies || **Topic Area:** Design

CHAIR:

Hai Zhou - Northwestern Univ. Evanston, IL

Internet of Things (IoT) has many applications, from building management, connected vehicles to smart cities. However, while evolving from centralized to distributed, sometimes constrained, systems, there are a wide range of challenges to be addressed, including, but not limited to, computation, storage, communication and networking. This session presents recent progress in systems and applications, including real-time mobile systems, reliability, energy efficient, and sensor drift.

50.1 MobiEye: An Efficient Cloud-based Video Detection System for Real-time Mobile Applications

Jiachen Mao, Qing Yang, Ang Li, Hai Li, Yiran Chen - Duke Univ., Durham, NC

50.2 Enabling File-oriented Fast Secure Deletion on Shingled Magnetic Recording Drives

Shuo-Han Chen, Ming-Chang Yang - Chinese Univ. of Hong Kong, Hong Kong
Yuan-Hao Chang, Chun-Feng Wu - Academia Sinica, Taipei, Taiwan

50.3 Enabling Failure-resilient Intermittently-powered Systems Without Runtime Checkpointing

Wei-Ming Chen - National Taiwan Univ., Taipei, Taiwan
Pi-Cheng Hsieh - Academia Sinica, Taipei, Taiwan
Tei-Wei Kuo - National Taiwan Univ., Taipei, Taiwan

50.4 Sensor Drift Calibration via Spatial Correlation Model in Smart Building

Tinghuan Chen - Chinese Univ. of Hong Kong, Shatin, Hong Kong, China
Bingqing Lin - Shenzhen Univ., Shenzhen, China
Hao Geng, Bei Yu - Chinese Univ. of Hong Kong, Shatin, Hong Kong

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SMARTER AND FASTER: MACHINE LEARNING AND NUMERICAL METHODS FOR SIMULATION

Time: 1:30 - 3:00pm || **Room:** N253 || **Event Type:** Research Reviewed

Keywords: Back-end Design, Test/Manufacturing/Reliability/Safety, Verification/Validation || **Topic Area:** EDA, Machine Learning/AI

CHAIR:

Ibrahim Elfadel - Khalifa Univ., Abu Dhabi, United Arab Emirates

CO-CHAIR:

Pingqiang Zhou - ShanghaiTech Univ., Shanghai, China

Simulation is vital for digital circuit design and manufacturing. This session will present recent exciting research to do faster simulations in a smarter way. In the first two papers, machine learning techniques (GANs, CNNs and other neural networks, random forests, etc.) have been explored for both lithography simulation and pre-routing timing prediction stages in the digital circuit design. The third paper introduces a general cache framework to speed up the generation of timing critical paths with a specific cone of logic. The fourth paper proposes improved spectral graph reduction techniques to accelerate the numerical analysis of graph-related simulation tasks.

51.1 Machine Learning-based Pre-routing Timing Prediction with Limited Pessimism.

Erick M. Carvajal Barboza, Nishchal Shukla - Texas A&M Univ., College Station, TX
Yiran Chen - Duke Univ., Durham, NC
Jiang Hu - Texas A&M Univ., College Station, TX

*51.2 LithoGAN: End-to-end Lithography Modeling with Generative Adversarial Networks

Wei Ye, Mohamed Baker Alawieh, Yibo Lin, David Z. Pan - Univ. of Texas at Austin, TX

51.3 A General Cache Framework for Efficient Generation of Timing Critical Paths

Kuan-Ming Lai - National Tsing Hua Univ., Hsinchu City, Taiwan
Tsung-Wei Huang - Univ. of Illinois at Urbana-Champaign, IL
Tsung-Yi Ho - National Tsing Hua Univ., Hsinchu, Taiwan

51.4 Effective-resistance Preserving Spectral Reduction of Graphs

Zhiqiang Zhao, Zhuo Feng - Michigan Technological Univ., Houghton, MI

* Denotes best paper candidate

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

52

SECURE AND PRIVATE EMBEDDED SYSTEM DESIGN

Time: 1:30 - 3:00pm || Room: N254 || Event Type: Research Reviewed

Keywords: Security & Privacy || Topic Area: Security, Embedded Systems & Software (ESS)

CHAIR:

Mimi Xie - Univ. of Pittsburgh, PA

CO-CHAIR:

Xue Lin - Northeastern Univ., Boston, MA

This session focuses on security and privacy of future embedded systems in the context of consumer privacy solutions and secure communication/computation. The session will first introduce smart-meter technologies for preserving consumer privacy against record disaggregation attacks. Then, a Hardware Security primitive based on debug facility will be presented that improves the run-time security of mobile devices. Later, this session will describe the realization of a private computing method applied at the scale of a modern microprocessor. This session will conclude by demonstrating that conservative quantum-secure encryption techniques can be energy-friendly through an improved ASIC multiplier hardware design.

52.1 Revisiting the ARM Debug Facility for OS Kernel Security

Jinsoo Jang, Brent Byunghoon Kang - Korea Advanced Institute of Science and Technology, Daejon, Republic of Korea

52.2 Low-overhead Power Trace Obfuscation for Smart Meter Privacy

Daniele Jahier Pagliari, Sara Vinco, Enrico Macii, Massimo Poncino - Politecnico di Torino, Italy

52.3 ARM2GC: Succinct Garbled Processor for Secure Computation

Ebrahim M. Songhori - Rice Univ., Houston, TX
M. Sadegh Riazi, Siam Umar Hussain - Univ. of California, San Diego, La Jolla, CA
 Ahmad-Reza Sadeghi - Technische Univ. Darmstadt, Germany
 Farinaz Koushanfar - Univ. of California, San Diego, La Jolla, CA

52.4 Filianore: Better Multiplier Architectures for LWE-based Post-quantum Key Exchange

Song Bian, Masayuki Hiromoto, Takashi Sato - Kyoto Univ., Kyoto, Japan

53

THOSE UNFORGETTABLE MEMORIES

Time: 1:30 - 3:00pm || Room: N255 || Event Type: Research Reviewed

Keywords: Emerging Technologies || Topic Area: Embedded Systems & Software (ESS)

CHAIR:

Darshana Jayasinghe - Univ. of New South Wales, Sydney, Australia

CO-CHAIR:

Ming-Chang Yang - Chinese Univ. of Hong Kong, Shatin, Hong Kong

Exciting research problems emerge as non-volatile memories inch closer to computation, forming main memories. Papers in this session address issues related to encoding for energy efficiency, 3D ReRam structures, path lookup efficiency aiding file system accesses, and wear-leveling driven allocation.

53.1 Adaptive Granularity Encoding for Energy-efficient Non-volatile Main Memory

Jie Xu, Dan Feng, Yu Hua, Wei Tong, Jingning Liu, Chunyan Li, Gaoxiang Xu - Huazhong Univ. of Science & Technology, Wuhan, China
 Yiran Chen - Duke Univ., Durham, NC

53.2 Magma: A Monolithic 3D Vertical Heterogeneous ReRAM-based Main Memory Architecture

Farzaneh Zokaei - Indiana Univ., Bloomington, IN
 Mingzhe Zhang - Institute of Computing Technology, Chinese Academy of Sciences, Chicago, IL
 Xiaochun Ye - Chinese Academy of Sciences, Beijing, China
 Dongrui Fan - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China
 Lei Jiang - Indiana Univ., Bloomington, IN

53.3 A Wear-leveling-aware Fine-grained Allocator for Non-volatile Memory

Xianzhang Chen - Chongqing Univ., Chongqing, China
 Qingfeng Zhuge - East China Normal Univ., Chongqing, China
 Qiang Sun - Chongqing Univ., Chongqing, China
 Edwin H.-M. Sha, Shouzhen Gu - East China Normal Univ., Shanghai, China
 Chaoshu Yang - Chongqing Univ., Chongqing, China
 Chun Jason Xue - City Univ. of Hong Kong, Hong Kong

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

54

IMAGINING NEW PLACEMENT APPROACHES

Time: 1:30 - 3:00pm || **Room:** N257 || **Event Type:** Research Reviewed
Keywords: Back-end Design, Implementation || **Topic Area:** EDA

CHAIR:

Matthew Berzins - Samsung Austin R&D Center, Austin, TX

CO-CHAIR:

Natarajan Viswanathan - Cadence Design Systems, Inc., San Jose, CA

Innovations in placement can dramatically speedup design closure and quality of results. Lowering the barrier to new EDA techniques by using deep learning hardware to speedup placement is the focus of the first paper. The next paper proposes a novel and universal approach to generating a smooth wire length model to speed up analytical placement.

Then we look at the complex interaction between standard cell and macro placement. Finally we examine automated FinFET standard cell layout for a 7nm process technology, considering metal zero (M0) routing and maximizing drain abutment to reduce area and minimize the need for fillers.

*54.1 DREAMPlace: Deep Learning Toolkit-enabled GPU Acceleration for Modern VLSI Placement

Yibo Lin, Shounak Dhar, Wuxi Li - Univ. of Texas at Austin, TX
 Haoxing Ren, Brucek Khailany - NVIDIA Corp., Austin, TX
 David Z. Pan - Univ. of Texas at Austin, TX

54.2 BiG: A Bivariate Gradient-based Wirelength Model for Analytical Circuit Placement

Fan-Keng Sun, Yao-Wen Chang - National Taiwan Univ.,
 Taipei, Taiwan

54.3 Routability-driven Mixed-size Placement Prototyping Approach Considering Design Hierarchy and Indirect Connectivity Between Macros

Jai-Ming Lin, Szu-Ting Li, Yi-Ting Wang - National Cheng Kung Univ., Tainan, Taiwan

54.4 NCTUcell: A DDA-aware Cell Library Generator for FinFET Structure with Implicitly Adjustable Grid Map

Yih-Lang Li, Shih-Ting Lin - National Chiao Tung Univ., Hsinchu, Taiwan
 Shinichi Nishizawa - Graduate School of Science and Engineering, Saitama University, Saitama, Japan
 Hong-Yan Su, Ming-Jie Fong - National Chiao Tung Univ., Hsinchu, Taiwan
 Oscar Chen - AnaGlobe Technology, Inc., Hsinchu, Taiwan
 Hidetoshi Onodera - Kyoto Univ., Kyoto, Japan

55

SHOULD WE TRUST AI FOR CYBERSECURITY?

Time: 1:30 - 3:00pm || **Room:** N259 || **Event Type:** Panel || **Keywords:** Security & Privacy, Emerging Technologies || **Topic Area:** Security, Machine Learning/AI

MODERATOR:

Jeyavijayan Rajendran - Texas A&M Univ., College Station, TX

ORGANIZERS:

Yier Jin - Univ. of Florida, Gainesville, FL
 Mark Tehranipoor - Univ. of Florida, Gainesville, FL
 Ahmad-Reza Sadeghi - Technische Univ. Darmstadt, Germany
 N Asokan - Aalto Univ., Aalto, Finland

Artificial Intelligence (AI), especially the Deep Neural Networks (DNN), has achieved great successes in various real-world applications ranging from facial/speech recognitions to medical image analyses. A recent trend combining AI techniques with cybersecurity challenges has resulted in various AI-powered cybersecurity solutions such as network intrusion detections and binary malware analyses. Although still at its early stage, AI-based cybersecurity approaches have become hot research topics and are believed to replace traditional solutions such as signature-based abnormality detection methods in the near future.

Nevertheless, many DNNs are vulnerable to adversarial example attacks. These carefully-crafted input examples can easily fool a DNN to output

incorrect classification results in the test stage. The advances in transfer learning make the problem even worse such that black-box attacks become possible and effective. Therefore, how to protect AI itself is an urgent research topic for both the AI community and the cybersecurity community.

In this panel, we try to address a seemingly ironic question: Shall we make AI robust and resilient enough first before we ever apply AI techniques in cybersecurity solutions and, if so, what are the challenges to develop secure AI techniques? However, if the answer is no, then why should we still trust AI-supported cybersecurity solutions while the underlying AI techniques are vulnerable to various attacks?

PANELISTS:

Rosario Cammarota - Intel Corp., Hillsboro, OR
 Farinaz Koushanfar - Univ. of California, San Diego, La Jolla, CA
 Jun Zhu - Tsinghua Univ., Beijing, China
 Bo Li - Univ. of Illinois at Urbana-Champaign, IL

* Denotes best paper candidate

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

DT56

SYSTEMC IN THE REAL WORLD

Time: 1:30 - 3:00pm | **Room:** N260 | **Event Type:** Designer Track

Keywords: Architecture & System Design, Verification/Validation, Front-end Design

Topic Area: Design, Design

CHAIR:

Mike Meredith - Cadence Design Systems, Inc., Bellevue, WA

ORGANIZER:

Mark Glasser - NVIDIA Corp., Santa Clara, CA

SystemC has been widely used for almost two decades as the medium of choice for building abstract, transaction-level models. Architects and designers use these high-level models for architectural exploration and coarse-grained performance or throughput modeling. In production flows it is important to incorporate the information contained in those abstract models into downstream, concrete portions of the flow. Connecting transaction-level modeling flows with RTL flows has long been ignored. In this session we attempt to rectify that by exploring interactions between

those two things. We look at how the two modeling environments can work together, each complimenting the other, to form flows that span the entire lifetime of a design from architectural exploration to coverage closure and timing closure.

56.1 Moving Up in the World

Stuart Swan - Mentor, A Siemens Business, San Jose, CA

56.2 Synchronizing Simulators, and Save and Restore!

David Black - Doulos , Austin, TX

Mark Burton - GreenSocs Ltd, Chalagnac, France

56.3 Multi-domain Simulation

Mark Glasser - NVIDIA Corp., Santa Clara, CA

Thank you to our Designer Track Sponsor:



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THE LUCK OF THE DRAW: DESIGNING TRUE RANDOM NUMBER GENERATORS FOR SECURITY

Time: 1:30 - 3:00pm | **Room:** N261 | **Event Type:** Special Session

Keywords: Hardware Security, Implementation, Test/Manufacturing/Reliability/Safety

Topic Area: Security, Design

CHAIR:

Aydin Aysu - North Carolina State Univ., Raleigh, NC

ORGANIZER:

Ingrid Verbauwheide - Katholieke Universiteit Leuven, Belgium

The generation of high quality true random numbers is essential in security applications, as well as in gambling and games. For secure communication, we also require these high quality TRNGs in embedded and IOT devices. Making them attack resistant and at the same time highly area and power efficient is a challenge.

In this special session we address the topic of TRNGs. Besides the coincidence that DAC is in Las Vegas, the capital of gambling, NIST has recently issued a new standard for the generation of TRNGs, the SP 800-90B, "Recommendation for the Entropy Sources Used for Random Bit Generation."

This session will have 3 invited presentations: the first one is a tutorial level introduction, the second one focuses on TRNGs in ASIC and the third one focuses on TRNGs for FPGAs.

57.1 True Random Number Generators for Security

John Kelsey - National Institute of Standards and Technology, Gaithersburg, MD

57.2 Implementing Random Number Generators in Commercial Silicon

David Johnston - Intel Corp., Hillsboro, OR

57.3 Random Numbers on FPGAs: Contradiction to the Deterministic Behavior

Ingrid Verbauwheide, Milos Grujic, Vladimir Rozic - Katholieke Universiteit Leuven, Belgium

Paper Title: Design Principles for True Random Number Generators for Security Applications

Authors: Milos Grujic, Vladimir Rozic - Katholieke Universiteit Leuven, Belgium

David Johnston - Intel Corp., Hillsboro, OR

John Kelsey - National Institute of Standards and Technology, Gaithersburg, MD

Ingrid Verbauwheide - Katholieke Universiteit Leuven, Belgium

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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DT58

EVERY JOULE COUNTS

Time: 1:30 - 3:00pm || **Room:** N262 || **Event Type:** Designer Track

Keywords: Back-end Design, Low Power, Implementation || **Topic Area:** Design, EDA

CHAIR:

Prashant Varshney - Microsoft Corporation, Sunnyvale, CA

Venture into this world where ardent fans of energy make every joule count in their hunt for savings – be it with a new way of power gating or substrate biasing, exploring the proper robustness of circuits and even designing automated cell design for analog cells. Rounding up the session is a deep look at what 3-Sigma really means!

58.1 Practical Implementation of Active Mode Power Gating Circuits

Insub Shin, Wook Kim, Kyungtae Do, Jung Yun Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea

58.2 A Novel Back Biasing Technique for Power Efficient SOC in FDSOI Technology Node

Koushik De, Abhishek Kumar Rai, Vikram Kuralla, Vivek Tiramareddi - INVECAS, Inc., Hyderabad, India

58.3 Activation-aware Slack Assignment (ASA) for Mode-wise Power Saving in High-end ISP

Jun Nagayama - Socionext, Inc., Yokohama, Japan
Yutaka Masuda - Osaka Univ., Suita, Japan
Masayuki Takeshige, Yoshimasa Ogawa - Socionext, Inc., Yokohama, Japan
Masanori Hashimoto - Osaka Univ., Suita, Japan
Yoichi Momiyama - Socionext, Inc., Yokohama, Japan

58.4 Novel Power-grid Design & Layout Strategy for SoC ESD-CDM Robustness

Villy V. Gohil, Karthik Kodakandla, Murali Mohan Thota, Subhadeep Ghosh - Texas Instruments India Pvt. Ltd., Bengaluru, India

58.5 Practical Cell Based Analog Design Methodology II (AnaCell)

Akira Suzuki, Yukichi Todoroki, Tomoyuki Kato, Masanori Kusano, Nobuto Ono, Kazuhiro Miura, Kazuyuki Kawauchi - Jedat, Inc., Tokyo, Japan
Takashi Ida, Yudai Abe, Yukiko Shibasaki, Anna Kuwana, Haruo Kobayashi - Gunma Univ., Kiryu, Japan

58.6 How Much Can One Trust Foundry's 3-Sigma PEX Corners?

Ning Lu - IBM Systems Group, Essex Junction, VT

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IP59

BEYOND MOORE'S LAW - NEW CHALLENGES WITH LOWER TECHNOLOGY NODES

Time: 1:30 - 3:00pm || **Room:** N264 || **Event Type:** IP Track || **Keywords:** Emerging Technologies, Implementation, Back-end Design || **Topic Area:** IP

CHAIR & ORGANIZER:

Chirag Dhruv - Advanced Micro Devices, Inc., Santa Clara, CA

The end of Moore's law may be upon us, but advanced nodes continue to present new challenges for IP Developers, suppliers, and consumers. Part of the industry has embraced 7nm node, while others are catching up to it. Exploration of 5nm technology node is already underway. As the technology nodes advance, we are faced with different challenges in terms of architecting efficiently for improved power and timing, physical design, increased complexity of designs due to higher amount of packing of transistors, etc.

In this session experts from IP development community, IP Consumers, and foundries share their experience with adoption of 7nm technology node, challenges they have encountered, and how they overcame those challenges.

59.1 New Design Solutions Keep Moore's Law Alive in N7 and Below. How to Find, and Stay in the Golden Path

Lluis Paris - Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA

59.2 IP Integration Challenges and Solutions in 7nm and Beyond

Raymond Nijssen - Achronix Semiconductor Corp., Santa Clara, CA

59.3 SOC Design Challenges on the Cutting Edge Technology Nodes

Karen Kwong, Donny Mota - Advanced Micro Devices, Inc., Markham, ON Canada

Thank you to our IP Track Sponsor:



Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

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NO MORE BETS: HIGH-LEVEL SYNTHESIS WINS ALL THE CHIPS

Time: 3:30 - 5:30pm || Room: N252 || Event Type: Research Reviewed

Keywords: Front-end Design || Topic Area: EDA

CHAIR:

Mahesh Iyer - Intel Corp., San Jose, CA

CO-CHAIR:

Sabya Das - Synopsys, Inc., Sunnyvale, CA

This session introduces novelties in High-Level Synthesis, approximate computing, hardware accelerator design and customized behavioral RISC processors. While High-Level Synthesis is widely used, there is still room to improve the quality of results. New methods based on graph morphing and SDC scheduling can help. Raising the level of abstraction also allows generation of multiple functionally equivalent designs with unique trade-offs. This is exploited to build different RISC-V processors and dedicated DNN hardware accelerators. Finally, an approximate computing functional unit design space explorer is presented.

60.1 Rapid Generation of High-quality RISC-V Processors from Functional Instruction Set Specifications

Gai Liu, Joseph Primmer, Zhiru Zhang - Cornell Univ., Ithaca, NY

60.2 autoAx: An Automatic Design Space Exploration and Circuit Building Methodology utilizing Libraries of Approximate Components

Vojtech Mrazek - Brno Univ. of Technology, Brno, Czech Republic
Muhammad Abdullah Hanif - Vienna Univ. of Technology, Vienna, Austria
Zdenek Vasicek, Lukas Sekanina - Brno Univ. of Technology, Brno, Czech Republic
Muhammad Shafique - Vienna Univ. of Technology, Vienna, Austria

60.3 Graph-morphing: Exploiting Hidden Parallelism of Non-stencil Computation in High-level Synthesis

Yu Zou, Mingjie Lin - Univ. of Central Florida, Orlando, FL

60.4 Overcoming Data Transfer Bottlenecks in FPGA-based DNN Accelerators via Layer-conscious Memory Management

Xuechao Wei, Yun Liang - Peking Univ., Beijing, China
Jason Cong - Univ. of California, Los Angeles, CA

60.5 High-level Synthesis of Resource-oriented Approximate Designs for FPGAs

Marcos T. Leipnitz, Gabriel L. Nazar - Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil

60.6 Improving Scalability of Exact Modulo Scheduling with Specialized Conflict-driven Learning

Steve Dai, Zhiru Zhang - Cornell Univ., Ithaca, NY

61

ET MEETS AI: EMERGING TECHNOLOGIES FOR ACCELERATING AI

Time: 3:30 - 5:30pm || Room: N253 || Event Type: Research Reviewed

Keywords: Emerging Technologies, Architecture & System Design, Low Power

Topic Area: Machine Learning/AI, Design

CHAIR:

Juergen Becker - Karlsruhe Institute of Technology, Karlsruhe, Germany

CO-CHAIR:

Xiaoqin Xu - Arm, Ltd.

Memory is the dominant cost factor in area, latency and power consumption of Neural Networks. Moreover, the memory cost increases exponentially with the dimensions of the neural networks. In this session papers explore emerging memory technologies such as RRAM and 3D die-stacked memory, and novel computing ideas such as stochastic computing to achieve low power consumption while improving performance and maintaining sufficient accuracy.

61.1 LAcc: Exploiting Lookup Table-based Fast and Accurate Vector Multiplication in DRAM-based CNN Accelerator

Quan Deng - National Univ. of Defense Technology, Changsha, Hunan, China

Youtao Zhang - Univ. of Pittsburgh, PA

Minxuan Zhang - National Univ. of Defense Technology, Changsha, China

Jun Yang - Univ. of Pittsburgh, PA

61.2 DRIS-3: Deep Neural Network Reliability Improvement Scheme in 3D Die-stacked Memory Based on Fault Analysis

Jae-San Kim, Joon-Sung Yang - Sungkyunkwan Univ., Suwon, Republic of Korea

61.3 X-MANN: A Crossbar Based Architecture for Memory Augmented Neural Networks

Ashish Ranjan, Shubham Jain, Jacob R. Stevens - Purdue Univ., West Lafayette, IN
Dipankar Das, Bharat Kaul - Intel Technology India Pvt. Ltd, Bangalore, India
Anand Raghunathan - Purdue Univ., West Lafayette, IN

61.4 On-chip Memory Technology Design Space Explorations for Mobile Deep Neural Network Accelerators

Haitong Li - Stanford Univ., Stanford, CA
Mudit Bhargava, Paul Whatmough - Arm, Ltd., Waltham, MA
H.-S. Philip Wong - Stanford Univ., Stanford, CA

61.5 SkippyNN: An Embedded Stochastic-computing Accelerator for Convolutional Neural Networks

Reza Hojabr, Kamyar Givaki, SM Reza Tayaranian - Univ. of Tehran, Iran
Parsa Esfahanian - Institute for Research in Fundamental Sciences, Tehran, Iran
Ahmad Khonsari - Univ. of Tehran, Tehran, Iran
Dara Rahmati - Shahid Beheshti Univ., Iran
M. Hassan Najafi - Univ. of Louisiana at Lafayette, LA

61.6 ZARA: A Novel Zero-free Dataflow Accelerator for Generative Adversarial Networks in 3D ReRAM

Fan Chen, Linghao Song, Hai Li, Yiran Chen - Duke Univ., Durham, NC

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

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ML FOR BLACK AND WHITE HATS

Time: 3:30 - 5:30pm || **Room:** N254 || **Event Type:** Research Reviewed

Keywords: Hardware Security || **Topic Area:** Security

CHAIR:

Xiaolin Xu - Univ. of Illinois at Chicago, IL

CO-CHAIR:

Selcuk Kose - Univ. of Rochester, NY

Machine learning provides a unique and powerful tool to both attack and defend hardware. This session highlights defensive and attacking techniques at the physical layer enhanced by machine learning algorithms. Specifically, the papers provide insight into side-channel detection, attacking split-manufactured ICs, mitigation of power analysis attacks, and leakage assessment for fault attack countermeasures.

62.1 X-DeepSCA: Cross-device Deep Learning Side Channel Attack

Debayan Das - Purdue Univ., West Lafayette, IN

Anupam Golder - Georgia Institute of Technology, Atlanta, GA

Josef Danial - Purdue Univ., West Lafayette, IN

Santosh Ghosh - Intel Corp., Hillsboro, OR

Arijit Raychowdhury - Georgia Institute of Technology, Atlanta, GA

Shreyas Sen - Purdue Univ., West Lafayette, IN

62.2 Attacking Split Manufacturing from a Deep Learning Perspective

Haocheng Li - Chinese Univ. of Hong Kong, Shatin, Hong Kong

Satwik Patnaik, Abhrajit Sengupta - New York Univ., New York City, NY

Haoyu Yang - Chinese Univ. of Hong Kong, Shatin, Hong Kong

Johann Knechtel - New York Univ., Abu Dhabi, United Arab Emirates

Bei Yu, Evangeline F. Y. Young - Chinese Univ. of Hong Kong,

Shatin, Hong Kong

Ozgur Sinanoglu - New York Univ., Abu Dhabi, United Arab Emirates

62.3 ALAFA: Automatic Leakage Assessment for Fault Attack Countermeasures

Sayandeep Saha, Nishok Kumar Sundaressan, Sikhar Patranabis, Debdeep Mukhopadhyay, Pallab Dasgupta - Indian Institute of Technology Kharagpur, India

62.4 ChipSecure: A 0.32 pJ/b Reconfigurable Analog eFlash-based Strong PUF in 55nm CMOS

Mohammad R. Mahmoodi, Hussein Nili, Shabnam Larimian, Xinjie Guo, Dmitri Strukov - Univ. of California, Santa Barbara, CA

62.5 Adversarial Attack Against Modeling Attack on PUFs

Sying-Jyan Wang, Yu-Shen Chen - National Chung Hsing Univ., Taichung, Taiwan

Katherine Shu-Min Li - National Sun Yat-sen Univ., Kaohsiung, Taiwan

62.6 RFTC: Runtime Frequency Tuning Countermeasure Using FPGA Dynamic Reconfiguration to Mitigate Power Analysis Attacks

Darshana Jayasinghe, Aleksandar Ignjatovic, Sri Parameswaran - Univ. of New South Wales, Sydney, Australia

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LET NATURE COMPUTE: FROM DNAS AND QBITS TO MICROFLUIDICS

Time: 3:30 - 5:30pm || **Room:** N255 || **Event Type:** Research Reviewed

Keywords: Emerging Technologies || **Topic Area:** Design

CHAIR:

Shreyas Sen - Purdue Univ., West Lafayette, IN

CO-CHAIR:

Swagath Venkataramani - IBM T.J. Watson Research Center

This sessions covers exciting opportunities for next-generation computing on emerging platform technologies. The first paper presents an end-to-end simulator for cross-layer design of ReRAM crossbar necessary for neuromorphic computing applications. The next two papers present advances in quantum computing. The fourth paper illustrates an approach to synthesize molecular reactions to compute support vector machines using radial basis function kernel. The fifth paper presents an in-memory computing platform based on SOT-MRAM to accelerate DNA sequence alignment computation. Finally the session concludes with a paper on the synthesis flow for micro-fluidic biochips.

63.1 Design Guidelines of RRAM based Neural-processing-unit: A Joint Device-circuit-algorithm Analysis

Wenqiang Zhang - Tsinghua Univ., Beijing, China

Xiaochen Peng - Arizona State Univ., Tempe, AZ

Huaqiang Wu, Bin Gao - Tsinghua Univ., Beijing, China

Shimeng Yu - Georgia Institute of Technology, Atlanta, GA

Youhui Zhang, Hu He, He Qian - Tsinghua Univ., Beijing, China

63.2 QURE: Qubit Re-allocation in Noisy Intermediate-scale Quantum Computers

Abdullah Ash-Saki, Mahabubul Alam, Swaroop Ghosh - Pennsylvania State Univ., University Park, PA

63.3 Mapping Quantum Circuits to IBM QX Architectures Using the Minimal Number of SWAP and H Operations

Robert Wille, Lukas Burgholzer, Alwin Zulehner - Johannes Kepler Univ. Linz, Austria

63.4 Computing Radial Basis Function Support Vector Machine using DNA via Fractional Coding

Xingyi Liu, Keshab K. Parhi - Univ. of Minnesota, Twin Cities, Minneapolis, MN

63.5 AlignS: A Processing-in-memory Accelerator for DNA Short Read Alignment Leveraging SOT-MRAM

Shaahin Angizi, Jiao Sun, Wei Zhang, Deliang Fan - Univ. of Central Florida, Orlando, FL

63.6 MiniControl: Synthesis of Continuous-flow Microfluidics with Strictly Constrained Control Ports

Xing Huang, Tsung-Yi Ho - National Tsing Hua Univ., Hsinchu, Taiwan

Wenzhong Guo - Fuzhou Univ., Fuzhou, China

Bing Li, Ulf Schlichtmann - Tech. Univ. of Munich, Germany

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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DEEP MANUFACTURING : DESIGN, DATA, AND MACHINE LEARNING

Time: 3:30 - 5:30pm || **Room:** N257 || **Event Type:** Research Reviewed

Keywords: Back-end Design, Test/Manufacturing/Reliability/Safety || **Topic Area:** EDA

CHAIR:

Sarvesh Bhardwaj - Mentor, A Siemens Business

CO-CHAIR:

Joydip Das - Samsung Austin R&D Center, Austin, TX

Deep learning opens the door to new approaches for Design for Manufacturing. The first four papers apply neural networks to hot-spot detection, sub-resolution assist feature generation, and layout test pattern generation. The fifth paper applies a novel Low Rank Tensor Approximation method to accurately estimate the probability of rare failure events. Meanwhile, progress in Directed Self-Assembly is enabled with a novel integer linear programming technique for Directed Self-Assembly.

64.1 Faster Region-based Hotspot Detection

Ran Chen - Chinese Univ. of Hong Kong, Shatin, Hong Kong
 Wei Zhong - Dalian Univ. of Technology, China
 Haoyu Yang, Hao Geng - Chinese Univ. of Hong Kong, Shatin, Hong Kong
 Xuan Zeng - Fudan Univ., Shanghai, China
 Bei Yu - Chinese Univ. of Hong Kong, Shatin, Hong Kong

64.2 Efficient Layout Hotspot Detection via Binarized Residual Neural Network

Yiyang Jiang, Fan Yang, Hengliang Zhu - Fudan Univ., Shanghai, China
 Bei Yu - Chinese Univ. of Hong Kong, Shatin, Hong Kong
 Dian Zhou - Univ. of Texas at Dallas, Richardson, TX
 Xuan Zeng - Fudan Univ., Shanghai, China

64.3 DeePattern: Layout Pattern Generation with Transforming Convolutional Auto-encoder

Haoyu Yang - Chinese Univ. of Hong Kong, Shatin, Hong Kong
 Piyush Pathak, Frank E. Gennari, Ya-Chieh Lai - Cadence Design Systems, Inc., San Jose, CA
 Bei Yu - Chinese Univ. of Hong Kong, Shatin, Hong Kong

64.4 GAN-SRAF: Sub-resolution Assist Feature Generation using Conditional Generative Adversarial Networks

Mohamed Baker Alawieh, Yibo Lin, Zaiwei Zhang, Meng Li, Qixing Huang, David Z. Pan - Univ. of Texas at Austin, TX

64.5 Meta-model Based High-dimensional Yield Analysis using Low-rank Tensor Approximation

Xiao Shi - Univ. of California, Los Angeles, CA
 Hao Yan, Qiancun Huang, Jiajia Zhang, Longxing Shi - Southeast Univ., Nanjing, China
 Lei He - Univ. of California, Los Angeles, CA

64.6 Novel Guiding Template and Mask Assignment for DSA-MP Hybrid Lithography Using Multiple BCP Materials

Yi-Ting Lin, Iris Hui-Ru Jiang - National Taiwan Univ., Taipei, Taiwan

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SECURE OPEN-SOURCE HARDWARE: HYPE OR REALITY?

Time: 3:30 - 5:30pm || **Room:** N259 || **Event Type:** Panel || **Keywords:** Hardware

Security, Architecture & System Design, Test/Manufacturing/Reliability/Safety

Topic Area: Security, Design

MODERATOR:

Ahmad-Reza Sadeghi - Technische Univ. Darmstadt, Germany

ORGANIZER:

Saverio Fazzari - Defense Advanced Research Projects Agency, Arlington, VA

Today's hardware designs are becoming more and more complex, featuring novel functionality in every iteration. In this context, Hardware Security plays a key role which has led to huge research and development efforts on designing and deploying Hardware Security architectures incorporating increasing number of security mechanisms. As a result, the Trusted Computing Base in hardware is not only constantly growing but is also typically highly proprietary through strict IP protection. Consequently, hardware platforms contain design and implementation flaws that are discovered after the fact and exploited by adversaries, as it has been repeatedly and impressively demonstrated in the recent years. Experience has also shown that patching Hardware Security bugs is not an adequate long-term solution.

On the other hand, the open-source community is advocating open hardware architectures (e.g., RISC-V) as an ultimate solution to establish

a transparent roadmap of developing hardware that enables the maxim of "Trust, but Verify". Indeed, we have already witnessed the popularity of the Linux kernel that spearheaded non-negligible and undeniable success stories in the software world.

As open hardware is quickly becoming a hot topic of research, academia and some enterprises have picked up this trend to "significantly" improve the current state of hardware design and security. While academic research follows the usual path of creating more conference papers and attract more funding, it seems questionable that semiconductor industry would ever be willing to adopt these solutions and open-source their entire hardware designs in the future.

In this panel experts from industry, government, and academia will discuss opportunities, promises and pitfalls of open-source models for improving the state-of-the-art or future hardware designs.

PANELISTS:

Eric Keiter - Sandia National Laboratories, Albuquerque, NM

Nele Mentens - Katholieke Universiteit Leuven, Belgium

Anand Rajan - Intel Corp., Hillsboro, OR

Jothy Rosenberg - Dover Systems, Waltham, MA

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

DT66

MACHINE LEARNING AND FRONT-END DESIGN

Time: 3:30 - 5:00pm || Room: N260 || Event Type: Designer Track

Keywords: Verification/Validation, Front-end Design, Emerging Technologies

Topic Area: Machine Learning/AI, EDA

CHAIR:

Vikas Sachdeva - *Real Intent, Inc., Sunnyvale, CA*

For those of us in the hardware design world, Machine Learning impacts us in two major ways: as a tool to help us design and validate, and as a new style of design we must support. In this session we will discuss new and innovative approaches in both these areas.

66.1 Improving Design Performance using Machine Learning in Synthesis

Gaurav K. Varshney, Akshi Tomar - *Texas Instruments India Pvt. Ltd., Bangalore, India*

66.2 High Confidence Early RTL Power Estimation with Machine Learning

Ajay S. Bist - *Intel Corp., Bangalore, India*
Mahesh G. Vutukuri - *Intel Technology India Pvt. Ltd, Bangalore, India*

Srinivas R. Jammula - *Intel Corp., Bengaluru, India*

66.3 Dedicated On-chip Network Hierarchies for Algorithm Acceleration

Kent Orthner, Travis Johnson - *Achronix Semiconductor Corp., Santa Clara, CA*

66.4 Virtual Methodology For Performance and Power Analysis of AI/ML SoC using Emulation

Vikas Singh, Debdutta Bhattacharya, Ayub Khan - *Mentor, A Siemens Business, Fremont, CA*

66.5 Arithmetic Datapath Design Exploration with Machine Learning

Mahesh G. Vutukuri - *Intel Technology India Pvt. Ltd, Bangalore, India*

Sreekanth Madgula, Ashutosh Garg - *Intel Corp., Folsom, CA*

66.6 Maximize TOPS (Tera Operations Per Second) per Watt for AI Chip using Early Power Analysis and Reduction

Ling Sun - *Iluvatar CoreX Inc., Shanghai, China*
Cheng Peng - *ANSYS, Inc., Shanghai, China*
Zhenhua Gan, Du Zhang - *Iluvatar CoreX Inc., Shanghai, China*

Thank you to our Designer Track Sponsor:



67

NEXT-GENERATION TIME-CRITICAL SYSTEMS

Time: 3:30 - 5:30pm || Room: N261 || Event Type: Special Session || Keywords: IoT, Architecture & System Design || Topic Area: Embedded Systems & Software (ESS), Design

CHAIR & ORGANIZER:

Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

The IoT revolution is rapidly ushering in myriad of new applications that need to interact with the physical environment in real time but are as prevalent as smartphones. Examples of such time-critical systems range from personal smart-drones, medical devices, robots to industrial IoT, in addition to the traditional real-time systems such as avionics, automotive, and spacecraft. All these emerging applications have irrefutable safety concerns associated with the failure to meet timing deadlines. Thus predictable response time of a computing system has become the first-class design target for diverse and everyday application scenarios rather than being relegated to only a selected few. This special session will introduce and explore the challenges, opportunities, and advancements to support the next-generation time-critical systems. The presentations will cover the entire spectrum of the design stack starting with high-level systems modeling to the overall system design process and finally to the underlying computer architecture.

67.1 Actors Revisited for Time-Critical Systems

Marten Lohstroh - *Univ. of California, Berkeley, CA*
Martin Schoeberl - *Technical Univ. of Denmark, Kongens Lyngby, Denmark*
Andrés Goen - *Technische Univ. Dresden, Germany*
Armin Wasicek - *Univ. of California, Berkeley, CA*
Christopher Gill - *Washington Univ., St. Louis, MO*
Marjan Sirjani - *Mälardalen Univ., Västerås, Sweden*
Edward Lee - *Univ. of California, Berkeley, CA*

67.2 Real-time Processing in the IoT - Why and How?

Lothar Thiele - *Eidgenössische Technische Hochschule Zürich, Switzerland*

67.3 Time Predictable Computing by Design: Looking Back, Looking Forward

Tulika Mitra - *National Univ. of Singapore*

67.4 Consolidation of High-integrity, High-performance, and Cyber-security Functions on a Manycore Processor

Benoit Dupont de Dinechin - *Kalray Corp., Grenoble, France*

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

WEDNESDAY, JUNE 5

DT68

WHEN ACCURACY MEETS POWER: 2019 DAC SYSTEM DESIGN CONTEST ON LOW POWER OBJECT DETECTION

Time: 3:30 - 5:00pm || Room: N262 || Event Type: Designer Track

Keywords: Architecture & System Design, Contest, Low Power || Topic Area: Machine Learning/AI, Embedded Systems & Software (ESS)

CHAIR:

Weiwen Jiang - Univ. of Pittsburgh, PA

ORGANIZERS:

Jingtong Hu - Univ. of Pittsburgh, PA

Jeff Goeders - Brigham Young Univ., Provo, UT

Philip Brisk - Univ. of California, Riverside, CA

Yanzhi Wang - Northeastern Univ., Boston, MA

Guojie Luo - Peking Univ., Beijing, China

This special session highlights the winning entries of the 2019 DAC System Design Contest on Low Power Object Detection (SDC). The contest started late last year. Contestants were required to implement object detection machine learning algorithms in either FPGA or GPU to achieve both high accuracy and low power. With Xilinx and Nvidia's sponsorship, contestants competed in two different categories: FPGA using Xilinx Ultra 96 and GPU using Nvidia TK2. All contestants used a large training dataset provided by DJI, a company renowned for drone technologies. The dataset contains over 14 GB of images with 100 different objects to detect. A hidden dataset was used to evaluate the performance of the designs in terms of accuracy and power. This year's contest attracted over 110 teams from more than 10 countries/regions. In this session, the SDC organizers will first introduce the background and statistics for this year's contest and announce the competition results. Then the top three teams in the FPGA and GPU category will present their designs.

68.1 Introduction to 2019 DAC System Design Contest: Dataset, Statistics and Discoveries

Jingtong Hu - Univ. of Pittsburgh, PA

Jeff Goeders - Brigham Young Univ., Provo, UT

Philip Brisk - Univ. of California, Riverside, CA

Yanzhi Wang - Northeastern Univ., Boston, MA

Guojie Luo - Peking Univ., Beijing, China

68.2 Third Place Winner Presentation: GPU Category

68.3 Second Place Winner Presentation: GPU Category

68.4 First Place Winner Presentation: GPU Category

68.5 Third Place Winner Presentation: FPGA Category

68.6 Second Place Winner Presentation: FPGA Category

68.7 First Place Winner Presentation: the FPGA Category

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IP69

OVERSEEING YOUR CHIP DESIGN TO IMPROVE EFFICIENCY

Time: 3:30 - 5:00pm || Room: N264 || Event Type: IP Track

Keywords: Emerging Technologies, Analog & Mixed Signal || Topic Area: IP

CHAIR:

Nathan Mandelke - Cadence Design Systems, Inc., San Jose, CA

This session focuses on how new technology is helping create a strategic value for companies by better oversight of the chip design process. In this session, authors will discuss new technologies and processes from deep learning and machine learning to qualifying and verifying IP blocks and how these processes are being adopted to improve the chip design process, resulting in cost savings and often a competitive advantage.

69.1 Reference-less, Real Time On-chip Clock Jitter Measurement IP

Ankur Bal, Rupesh Singh - STMicroelectronics, Greater Noida, India

69.2 Design and Evaluation of FPGA Fabric Optimized for Edge Compute and Machine Learning Inferencing Applications

Mike Fitton - Achronix Semiconductor Corp., Santa Clara, CA

69.3 Library Validation using Deep Learning

Srinivas Bodapati, Vidya Sagar Reddy Gopala - Intel Corp., Santa Clara, CA

69.4 Efficient Verification of High-level Synthesis IP

David Aerne - Mentor, A Siemens Business, Wilsonville, OR
Gagandeep Singh, Deepak Mehta - Mentor Graphics (India) Pvt. Ltd., Noida, India

69.5 The Importance of In-chip Monitoring Subsystems for the Optimisation, Reliability and Enhancement of FinFET Designs

Ramsay Allen, Stephen Crosher, Naseer Khan - Moortec Semiconductor Ltd., Plymouth, United Kingdom

69.6 Novel Approach in Differential CDC Analysis of Parameterized IP

Ashish Soni - STMicroelectronics, Greater Noida, India
Amit Goldie - Synopsys India Pvt. Ltd., Noida, India
Navneet Chaurasia - Synopsys, Inc., Noida, India
Anubhav Arora - STMicroelectronics, Greater Noida, India

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

WEDNESDAY, JUNE 5

DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Time: 5:00 - 6:00pm || Exhibit Floor || Event Type: Designer and IP Track Poster

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Wednesday, June 5 from 5:00 to 6:00pm on the Exhibit Floor.

125.1 Timing Constraint Generation and Management

Eric Foreman - IBM Systems and Technology Group, Essex Junction, VT
Nathan Buck, Robert Allen - IBM Corp., Essex Junction, VT

125.2 Dump, Convert and Replay: A Targeted Methodology to Mitigating Gate-level Power Simulations Effort

Ioannis Savvidis - Ericsson, Stockholm, Sweden

125.3 Fast and Accurate Incremental Power and Signal Integrity Analysis

Rotem Cohen, Anton Rozen - Mellanox Technologies, Kiryat Gat, Israel
Abhijith MV, Ramesh Agarwal, Sankar Ramachandran, - ANSYS, Inc., Bangalore, India,
Scott Johnson - ANSYS, Inc., Austin, TX

125.4 Synthetic Traffic Based Performance Verification

Seunghyun Song, Hyungtae Park, Hyunsun Ahn - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Sihyun Kim, Namho Heo - Synopsys, Inc., Seongnam-si, Republic of Korea
Seonil B. Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea

125.5 Sign-off Driven Design Closure for a Mixed-signal SOC

MuraliMohan Thota, Karthik Kodakandla, Atul Garg, Sanjana Sundaresh, Nagarjuna D. Ganji, Ajoy Mandal, Gaurav K. Varshney - Texas Instruments India Pvt. Ltd., Bangalore, India

125.6 Block Level Boundary Constraint Validation with Top Context

Patricia Fong - GLOBALFOUNDRIES, Santa Clara, CA

125.7 RISC-V Linux: Ports and Storms

Palmer Dabbelt - SiFive, Inc., San Mateo, CA

125.8 A 360 Degree View of UVM Events

Vikas Billa - Intel Technology India Pvt. Ltd, Hyderabad, India

125.9 Congestion Aware Incremental Scan Connections for ECO Flip Flops

Alok Chandra, Sandeep Prajapati - GLOBALFOUNDRIES, Bangalore, India
Sai V. Gudladona - Laksh Semiconductor Pvt. Ltd., Bangalore, India

125.10 Incremental Power Routing at Different Phases of Physical Design Flow

Jagadeeshwar Surigi - GLOBALFOUNDRIES, Bangalore, India

125.11 Data analytics and BQM for better early stage PI approach

Tian Zhuo, Qiuling Zeng - HiSilicon, Shanghai, China
xin yao, Yaliang Li - ANSYS, Inc., Shanghai, China

125.12 Faster PV Signoff Convergence in P&R using RTD

Satish K. Dinavahi - Qualcomm India Pvt. Ltd., Bangalore, India
Srinivas Velivala - Mentor, A Siemens Business, Wilsonville, OR
Gurpreet Singh Lamba - Mentor, A Siemens Business, Bangalore, India
Anukul Rangarajan - Qualcomm India Pvt. Ltd., Bangalore, India

125.13 A Rapid Timing Fixing Methodology Including Impact of Voltage Drop to Identify Real Timing Violations

Anil Yadav - STMicroelectronics, Greater Noida, India
Anant Narain - ANSYS, Inc., Noida, India

125.14 Hybrid Methodology- An Innovative Methodology for Hierarchical CDC Verification

Rohit K. Sinha, Ravichandra Sopanrao - Intel Technology India Pvt. Ltd, Bangalore, India

125.15 Power Grid Analysis For Huge Graphics Designs Using Big-data Elastic-compute Solution

Basavaraj Kanthi, Mohammed Farooq T A - Intel Corp., Bangalore, India
Srinivas Thota - Intel Corp., Folsom, CA, Anand Ananthanarayanan, Harikrishnan K - Intel Corp., Bangalore, India

125.16 Distributed Clock Useful Skew to Reduce Peak Current

Ryan Chen - Global Unichip Corp., Hsinchu City, Taiwan

125.17 Functional Safety on A-R-M CPUs

Jitendra Aggarwal - Arm, Ltd., Bangalore, India
Harish Narayanaswamy - Mentor, A Siemens Business, Bangalore, India

125.18 Machine Learning In-memory Computing Architecture using an Embedded Processor

Odin Shen - Arm, Ltd., Taipei City, Taiwan

125.19 Self-heating Aware Logic Cell Design and Optimization

Oskar Baumgartner, Markus Karner, Zlatan Stanojevic, Christian Kernstock - Global TCAD Solutions, Vienna, Austria

125.20 Timing Capture - Comprehensive Delay Calculation Flow for Programmable Devices

Nitin Navale, Sumukh Nanjangud - Xilinx Inc., San Jose, CA

125.21 Tackling the Increasing Challenge of IR drop & EM Fails in Advanced Technologies with a Push Button Solution

Anand Kumaraswamy - Avera Semiconductor LLC, Bangalore, India
Fady Fouad - Mentor, A Siemens Business, Cairo, Egypt
Gurpreet Singh Lamba - Mentor, A Siemens Business, Bangalore, India
Jeff Wilson - Mentor, A Siemens Business, Portland, OR
Sandeep Torgal - GLOBALFOUNDRIES, Bangalore, India

125.22 Update your SystemC to use Modern C++

David Black - Doulos, Austin, TX

125.23 Power Supply Noise Coupling Between Different Power Domains in a Large Programmable SoC

Dima Klokofov, Tony Luan, Anna Wong, Dawn M. Graves - Xilinx Inc., San Jose, CA
Venkata R. Nidamanuri, Chris Ortiz - ANSYS, Inc., San Jose, CA

125.24 SOC System Bus Performance Monitor (SPM)

Hyungtae Park, Seunghyun Song, Hyunsun Ahn, Jisu Yang - Samsung Electronics Co., Ltd., Gyeonggi-do, Republic of Korea
Sihyun Kim, Namho Heo - Synopsys, Inc., Seongnam-si, Republic of Korea
Seonil B. Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea

125.25 Advanced Chip Performance Monitoring by Tracking Critical Paths Which Reflects Real PVT Variation

Yonghwan Kim, Wook Kim, Sungwook Moon, Jung Yun Choi - Samsung Electronics Co., Ltd., Yong-in, Republic of Korea

Thank you to our Designer Track and IP Track Sponsors:



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NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Level 2 - Pre-Function Area || Event Type: Work-In-Progress

Join us in the Upstairs Pre-Function Area to see Work-in-Progress posters and enjoy light snacks and beverages.

121.1 Fast Simulation-based Fixed-point Refinement with Inferential Statistics

Justine Bonnot, Karol Desnos - Institut d'Électronique et de Télécommunications de Rennes, Rennes, France
Daniel Menard - Institut National des Sciences Appliquées de Rennes, France

121.2 Floating Point Configurable Approximate Multiplier

Chandan K. Jha, Sumit Walia, Gagan Kanojia, Joycee Mekie - Indian Institute of Technology Gandhinagar, India

121.3 Improving Ring ORAM Read Performance with Imbalance-aware Scheduling

Yuezhi Che, Ruija Wang - Illinois Institute of Technology, Chicago, IL

121.4 Inference Engine Benchmarking across Technological Platforms from CMOS to Post-CMOS

Xiaochen Peng - Georgia Institute of Technology, Atlanta, GA
Minkyu Kim - Arizona State Univ., Tempe, AZ
Xiaoyu Sun - Georgia Institute of Technology, Atlanta, GA
Shihui Yin - Arizona State Univ., Tempe, AZ
Titash Rakshit, Ryan M. Hatcher, Jorge A. Kittl - Samsung Semiconductor, Inc., Austin, TX
Jae-sun Seo - Arizona State Univ., Tempe, AZ
Shimeng Yu - Georgia Institute of Technology, Atlanta, GA

121.5 An Energy-efficient On-chip Learning Hardware Architecture for STDP based Sparse Coding

Heetak Kim, Hoyoung Tang, Jongsun Park - Korea Univ., Seoul, Republic of Korea

121.6 Exploring Communication Design Space in Optical Networks-on-chip: both Distance and Contention Matter

H. K. Luan Duong - Nanyang Technological Univ., Singapore
Mengquan Li - Chongqing Univ., Chongqing, China
Weichen Liu - Nanyang Technological Univ., Singapore

121.7 Zilean:Simplify the Complexity of Deploying Multiple NN-based Applications on a Single Machine

Lihui Jin, Chao Wang - Univ. of Science and Technology of China, Hefei, China

121.8 Microarchitecture-aware Code Generation for Deep Learning on Single-ISA Heterogeneous Multi-core Mobile Processors

Junmo Park - Seoul National Univ., Seoul, Republic of Korea
Yongin Kwon - Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea
Yongjun Park - Hanyang Univ., Seoul, Republic of Korea
Dongsuk Jeon - Seoul National Univ., Seoul, Republic of Korea

121.9 SPRoute: A Scalable Parallel Negotiation-based Global Router

Jiayuan He - Univ. of Texas at Austin, TX
Martin Burtscher - Texas State Univ., San Marcos TX
Rajit Manohar - Yale Univ., New Haven, CT
Keshav Pingali - Univ. of Texas at Austin, TX

121.10 A High Speed Multiply-accumulate (MAC) Unit: Case Studies on 3D Stacked FPGA and ASIC

Young Seo Lee, Kyung Min Kim - Korea Univ., Seoul, Republic of Korea
Sang Jun Nam, Young-Ho Gong - Samsung Electronics Co., Ltd., Suwon, Republic of Korea
Seon Wook Kim, Sung Woo Chung - Korea Univ., Seoul, Republic of Korea

121.11 PETs: Pin Level Error Checking and Correcting Architecture of DRAM with Toggling Sense Amplifier

Sangmok Jeong, Joon-Sung Yang - Sungkyunkwan Univ., Suwon, Republic of Korea

121.12 Buffer Protection using PUF-based Randomized Canaries

Asmit De, Aditya Basu, Swaroop Ghosh, Trent Jaeger - Pennsylvania State Univ., University Park, PA

121.13 Post-silicon Validation of the IBM POWER9 Processor

Tom Kolan - IBM Corp., Haifa, Israel
Hillel Mendelson, Vitali Sokhin - IBM Research - Haifa, Israel
Kevin Reick - IBM Systems and Technology Group, Austin, TX
Elena Tsanko - IBM Research - Haifa, Israel
Gregory A. Wetli - IBM Corp., Austin, TX

121.14 Acceleration of Sparse Winograd Convolution with Small-scale Systolic Arrays

Feng Shi, Haochen Li, Song-Chun Zhu, Jason Cong - Univ. of California, Los Angeles, CA

121.15 Runahead Activation: Exploiting Idleness Through DRAM-aware Speculation

Lavanya Subramanian, Anant Nori, Sreenivas Subramoney, Hong Wang - Intel Corp., Santa Clara, CA

121.16 LiveSim: A Fast, Hot-reload Simulator for HDLs

Haven B. Skinner, Rafael Trapani Possignolo, Jose Renau - Univ. of California, Santa Cruz, CA

121.17 Compact Modeling of I-V Characteristics, Temperature Dependency, Variations, and Noise of Integrated, Reproducible Metal-oxide Memristors

Hussein Nili, Adrien F. Vincent, Mirko Prezioso, Mohammad R. Mahmoodi - Univ. of California, Santa Barbara, CA
Irina Kataeva - DENSO CORP., Nisshin-Shi, Japan
Dmitri Strukov - Univ. of California, Santa Barbara, CA

121.18 Unified Testing and Security Framework for WiNoC-enabled Multicore Chips

Abhishek Vashist, Andrew Keats, Amlan Ganguly - Rochester Institute of Technology, Rochester, NY
Sai Manoj P. Dinakarao - George Mason Univ., Fairfax, VA

121.19 An All-digital, Bi-directional Adaptive Clocking Circuit and Its Application on a Wide-operating-range AVFS System in 28nm CMOS

Weivei Shan, Jiaming Xu, Shuai Zhang - Southeast Univ., Nanjing, China

121.20 A Novel Sensor Selection Method Based on Convolutional Neural Network for P300 Speller in Brain Computer Interface

Hongchang Shan, Todor Stefanov - Leiden Univ., Leiden, The Netherlands

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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WORK-IN-PROGRESS POSTER SESSION

121.21 No Need to be Subtle: Simple Physical Adversarial Examples against End-to-end Autonomous Driving Models

Adith J. Boloor - Washington Univ., St. Louis, MO
 Xin He - Univ. of Michigan, Ann Arbor, MI
 Christopher D. Gill, Yevgeniy Vorobeychik, Xuan Zhang - Washington Univ., Saint Louis, MO

121.22 Hawkware: Network Intrusion Detection Based on Behavior Analysis with ANNs on an IoT Device

Sunwoo Ahn, Hayoon Yi, Younghan Lee, Giyeol Kim, Yunheung Paek - Seoul National Univ., Seoul, Republic of Korea
 Yeongpil Cho - Soongsil Univ., Seoul, Republic of Korea

121.23 TIP: A Temperature Effect Inversion-aware System-on-chip Platform Targeting Ultra-low Power Operation

Kyuseung Han, Sukho Lee, Jae-Jin Lee - Electronics and Telecommunications Research Institute, Daejeon, Republic of Korea
 Woojoo Lee - Chung-Ang University, Seoul, Republic of Korea
 Massoud Pedram - Univ. of Southern California, Los Angeles, CA

121.24 QuSecNets: Quantization-based Defense Mechanism for Securing Deep Neural Network Against Adversarial Attacks

Faiq Khalid - Vienna Univ. of Technology, Vienna, Austria
 Hassan Ali, Hammad Ali Tariq - National University of Sciences and Technology, Islamabad, Pakistan
 Muhammad Abdullah Hanif, Semeen Rehman - Vienna Univ. of Technology, Vienna, Austria
 Rehan Ahmed - National University of Sciences and Technology, Islamabad, Pakistan
 Muhammad Shafique - Technische Univ., Wien, Austria

121.25 A Cost-effective, High-accuracy Two-stage Approximate Logarithmic Multiplier

HyunJin Kim - Dankook Univ., Yongin, Republic of Korea
 Min Soo Kim, Nader Bagherzadeh - Univ. of California, Irvine, CA

121.26 Improving Logic Optimization in Sequential Circuits Using Majority-inverter Graphs

Walter Lau Neto, Xifan Tang, Max D. Austin - Univ. of Utah, Salt Lake City, UT
 Luca Amarù - Synopsys, Inc., Sunnyvale, CA
 Pierre-Emmanuel Gaillardron - Univ. of Utah, Salt Lake City, UT

121.27 Characterizing Contention and Resource-sharing Levels in the NVIDIA's Xavier SoC

Hamid Tabani, Mikel Fernandez, Leonidas Kosmidis, Jaume Abella, Enrico Mezzetti, Francisco J. Cazorla - Barcelona Supercomputing Center, Barcelona, Spain

121.29 A Recursive Least-squares Approach to Partially Blind Calibration of a Pollution Sensor Network

Thomas Becnel, Tofigh Sayahi, Kerry Kelly, Pierre-Emmanuel Gaillardron - Univ. of Utah, Salt Lake City, UT

121.30 In Memory Computing for Floating Point Addition

Sina Sayyah Ensan, Seyedhamidreza Motaman, Swaroop Ghosh - Pennsylvania State Univ., University Park, PA

121.31 On the Analysis of the Execution Time Behaviour of Autonomous Driving Software

Hamid Tabani, Leonidas Kosmidis, Jaume Abella, Enrico Mezzetti, Francisco J. Cazorla - Barcelona Supercomputing Center, Barcelona, Spain

121.32 A 0.5V 140MHz 11.5 μ W/MHz Microcontroller Realized by Adaptive Body Bias Aware Implementation in 22FDX Technology

Sebastian Höppner, Holger Eisenreich, Dennis Walter, Andre Scharfe, Florian Schraut, Alexander Oefelein, Robert Niebsch, Heiner Bauer, Jörg Schreiter, Stefan Scholze, Georg Ellguth, Stephan Henker, Stephan Scherzer - RacilCs GmbH, Dresden, Germany
 Ulrich Hensel, Matthias Noßmann, Helmut Prengel - GLOBALFOUNDRIES, Dresden, Germany

121.33 RAreDPM: Reliability-aware Reinforcement Learning Based Multi-core Power Management

Sai Manoj Pudukotai Dinakarao - George Mason Univ., Fairfax, VA
 Muhammad Shafique - Technische Univ., Wien, Austria
 Houman Homayoun - George Mason Univ., Fairfax, VA

121.34 Leveraging LSTMs for Interference-aware Run-time System Predictability of Cloud Workloads

Dimosthenis Masouros, Sotirios Xydis, Dimitrios Soudris - National Technical Univ. of Athens, Athens, Greece

121.35 VCAM: Variation Compensation through Activation Matching for Analog Binarized Neural Networks

Jaehyun Kim, Chaeun Lee, Kiyoung Choi - Seoul National Univ., Seoul, Republic of Korea

121.36 Neksus: Interconnect for System-in-package Architectures

Vidushi Goyal, Xiaowei Wang, Valeria Bertacco, Reetu Das - Univ. of Michigan, Ann Arbor, MI

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm | Level 2 Pre-Function Area | Event Type: Networking

Join us on Level 2 Pre-Function Area to see Work-in-Progress posters and enjoy snacks and beverages.

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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LATE BREAKING RESULTS

Time: 6:00 - 7:00pm || Level 2 - Pre-Function Area || Event Type: LBR Poster Session

Please join us for the late breaking results poster session. All works have been accepted to be published in the proceedings as apart of our new LBR program this year.

100.1 Late Breaking Results: Authenticated Call Stack

Hans Liljestrand, Thomas Nyman - Aalto Univ., Espoo, Finland
Jan-Erik Ekberg - Huawei Technologies Co., Ltd., Espoo, Finland
N Asokan - Aalto Univ., Espoo, Finland

100.2 Late Breaking Results: United We Stand: A Threshold Signature Scheme for Identifying outliers in PLCs

Urbi Chatterjee, Pranesh Santikellur, Rajat Sadhukhan, Vidya Govindan, Debdeep Mukhopadhyay - Indian Institute of Technology Kharagpur, India
Rajat S. Chakraborty - Indian Institute of Technology, Kharagpur, India

100.3 Late Breaking Results: Improving Static Power Efficiency via Placement of Network demultiplexer over Control Plane of Router in Multi-NoCs

Sonal Yadav, Vijay Laxmi - Malaviya National Institute of Technology, Jaipur, India
Manoj Singh Gaur - Indian Institute of Technology, Jammu, India
Hemangee K. Kapoor - Indian Institute of Technology Guwahati, India

100.4 Late Breaking Results: How Secure are Deep Learning Algorithms from Side-channel based Reverse Engineering?

Manaar Alam, Debdeep Mukhopadhyay - Indian Institute of Technology Kharagpur, India

100.5 Late Breaking Results: Predicting DRC Violations Using Ensemble Random Forest Algorithm

Riadul Islam, Md Asif Shahjalal - Univ. of Michigan, Dearborn, MI

100.6 Late Breaking Results: Analog Circuit Generator based on Deep Neural Network Enhanced Combinatorial Optimization

Kourosh Hakhamaneshi, Kourosh Hakhamaneshi, Nick Werblun, Pieter Abbeel, Vladimir M. Stojanovic - Univ. of California, Berkeley, CA

100.7 Late Breaking Results: Distributed Timing Analysis at Scale

Tsung-Wei Huang, Chun-Xun Lin, Martin D.F. Wong - Univ. of Illinois at Urbana-Champaign, IL

100.8 Late Breaking Results: Towards Practical Record and Replay for Mobile Applications

Onur Sahin, Assel Aliyeva, Ayse K. Coskun, Manuel Egele, Hariharan Mathavan - Boston Univ., Boston, MA

100.9 Late Breaking Results: The Ping-pong Tunable Delay Line In A Super-resilient Delay-locked Loop

Zheng-Hong Zhang, Wei Chi, **Shi-Yu Huang** - National Tsing Hua Univ., HsinChu, Taiwan

100.10 Late Breaking Results: An Efficient Learning-based Approach for Performance Exploration on Analog and RF Circuit Synthesis

Po-Cheng Pan, Chien-Chia Huang, **Hung-Ming Chen** - National Chiao Tung Univ., HsinChu, Taiwan

100.11 Late Breaking Results: LODESTAR: Creating Locally-dense CNNs for Efficient Inference on Systolic Arrays

Bahar Asgari, Ramyad Hadidi, Hyesoon Kim, Sudhakar Yalamanchili - Georgia Institute of Technology, Atlanta, GA

100.12 Late Breaking Results: Robustly Executing DNNs in IoT Systems Using Coded Distributed Computing

Ramyad Hadidi, Jiashen Cao - Georgia Institute of Technology, Atlanta, GA
Michael S. Ryoo - Google, Inc., Mountain View CA
Hyesoon Kim - Georgia Institute of Technology, Atlanta, GA

100.13 Late Breaking Results: Visual Cortex Inspired Pixel-level Re-configurable Processors for Smart Image Sensors

Pankaj Bhowmik, Md Jubaer Hossain H. Pantho - Univ. of Arkansas, Fayetteville, AR
Christophe Bobda - Univ. of Florida, Gainesville, FL

100.14 Late Breaking Results: Efficient Circuits for Quantum Search over 2D Square Lattice Architecture

Shaohan Hu, Dmitri Maslov, Marco Pistoia, Jay Gambetta - IBM T.J. Watson Research Center, Yorktown Heights, NY

100.15 Late Breaking Results: SEDA - Single Exact Dual Approximate Adders for Approximate Processor

Chandan K. Jha, Joycee Mekie - Indian Institute of Technology Gandhinagar, India

100.16 Late Breaking Results: Merging Everything (ME): A Unified FPGA Architecture Based on Logic-in-memory Techniques

Xiaoming Chen, Longxiang Yin - Chinese Academy of Sciences, Beijing, China
Bosheng Liu - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China
Yinhe Han - Chinese Academy of Sciences, Beijing, China

100.17 Late Breaking Results: New Computational Results and Hardware Prototypes for Oscillator-based Ising Machines

Tianshi Wang, Leon Wu, Jaijeet Roychowdhury - Univ. of California, Berkeley, CA

100.18 Late Breaking Results: Internal Structure Aware RDF Data Management in SSDs

Renhai Chen, Qiming Guan, Guohua Yan, Zhiyong Feng - Tianjin Univ., Tianjin, China

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

THURSDAY, JUNE 6

DAC BEST PAPER AND PRESENTATION AWARDS

Time: 9:00 - 9:20am || Room: N250

Join us as DAC presents the Research Best Paper Award as well as the Designer and IP Track Best Presentation Awards.

BEST RESEARCH PAPER NOMINEES:

- 11.1 - Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search** (see page 32)
- 31.1 - BRIC: Locality-based Encoding for Energy-Efficient Brain-Inspired Hyperdimensional Computing** (see page 44)
- 40.1 - A 1.17 TOPS/W, 150fps Accelerator for Multi-face Detection and Alignment** (see page 54)
- 51.2 - LithoGAN: End-to-end Lithography Modeling with Generative Adversarial Networks** (see page 61)
- 54.1 - DREAMPlace: Deep Learning Toolkit-enabled GPU Acceleration for Modern VLSI Placement** (see page 63)

RESEARCH TRACK:

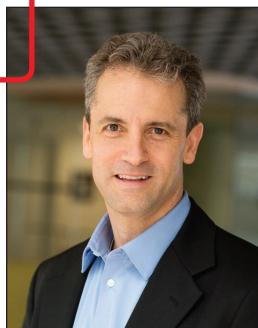
Best Research Paper

DESIGNER TRACK:

Best Presentation – Embedded Systems & Software
Best Presentation – Front-end Silicon Design
Best Presentation – Back-end Silicon Design

IP TRACK:

Best Presentation
Best Poster



KEYNOTE: REVERSE ENGINEERING VISUAL INTELLIGENCE

JAMES DICARLO, MD, PHD – Massachusetts Institute of Technology, Cambridge, MA

Time: 9:20 - 10:00am || Room: N250 || Event Type: Keynote

The brain and cognitive sciences are hard at work on a great scientific quest — to reverse engineer the human mind and its intelligent behavior. These fields are still in their infancy. Not surprisingly, forward engineering approaches that aim to emulate human intelligence (HI) in artificial systems (AI) are also still in their infancy. Yet the intelligence and cognitive flexibility apparent in human behavior are an existence proof that machines can be constructed to emulate and work alongside the human mind. And history suggests that these challenges of reverse engineering human intelligence will be solved by tightly combining the efforts of brain and cognitive scientists (hypothesis generation and data acquisition), and forward engineering aiming to emulate intelligent behavior (hypothesis instantiation and data prediction). As this approach discovers the correct neural network models, those models will not only encapsulate our understanding of complex brain systems, they will be the basis of next-generation computing and novel brain interfaces for therapeutic and augmentation goals (e.g., brain disorders).

In this session, I will focus on one aspect of human intelligence — visual object categorization and detection — and I will tell the story of how work in brain science, cognitive science and computer science converged to create deep neural networks that can support such tasks. These networks not only reach human performance for many images, but their internal workings are modeled after — and largely explain and predict — the internal

workings of the primate visual system. Yet, the primate visual system (HI) still outperforms current generation artificial deep neural networks (AI), and I will show recent new clues that the brain and cognitive sciences can offer. More broadly, our species is at the beginning of its most important science and engineering quest — the quest to understand and emulate human intelligence — and I hope to motivate others to engage that frontier alongside us.

Biography: James DiCarlo is a Professor of Neuroscience, and Head of the Department of Brain and Cognitive Sciences at the Massachusetts Institute of Technology. His research goal is to reverse engineer the brain mechanisms that underlie human visual intelligence. He and his collaborators have revealed how population image transformations carried out by a deep stack of neocortical processing stages -- called the primate ventral visual stream -- are effortlessly able to extract object identity from visual images. His team uses a combination of large-scale neurophysiology, brain imaging, direct neural perturbation methods, and machine learning methods to build and test artificial neural network models of the ventral visual stream and its support of cognition and behavior. Such an engineering-based understanding is likely to lead to new artificial vision and artificial intelligence approaches, new brain-machine interfaces to restore or augment lost senses, and a new foundation to ameliorate disorders of the mind.

70**EMERGING MEMORY IN EMERGING APPLICATIONS**

Time: 10:30am - 12:00pm || **Room:** N252 || **Event Type:** Research Reviewed
Keywords: Architecture & System Design || **Topic Area:** Embedded Systems & Software (ESS)

CHAIR:

Xiang Chen - George Mason Univ., Fairfax, VA

CO-CHAIR:

Jingtong Hu - Univ. of Pittsburgh, Pittsburgh, PA

In this session, four papers present recent advances on leveraging emerging NVMe in different computing platforms such as CPU, GPU and FPGA. Two papers presents how to integrate novel NVMe into GPUs. One paper discusses how to deploy NVMe on FPGA's BRAMs in a write-friendly way. The last paper presents a novel Skyrmiion-based racetrack memory and its novel applications in cache.

70.1 Efficient GPU NVRAM Persistence with Helper Warps

Sui Chen - Louisiana State Univ., Baton Rouge, LA
Faen Zhang - Ainnovation Technology Ltd., Beijing, China
Lei Liu - Chinese Academy of Sciences, Beijing, China
Lu Peng - Louisiana State Univ., Baton Rouge, LA

70.2 FlashGPU: Placing New Flash Next to GPU Cores

Jie Zhang, Miryeong Kwon - Yonsei Univ., InCheon-Si, Republic of Korea
Hyojong Kim, Hyesoon Kim - Georgia Institute of Technology, Atlanta, GA
Myoungsoo Jung - Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

70.3 Performance-aware Wear Leveling for Block RAM in Nonvolatile FPGAs

Shuo Huai, Weining Song, Mengying Zhao, Xiaojun Cai, Zhiping Jia - Shandong Univ., Qingdao, China

70.4 ZUMA: Enabling Direct Insertion/Deletion Operations with Emerging Skyrmiion Racetrack Memory

Zheng Liang, Guangyu Sun - Peking Univ., Beijing, China
Wang Kang, Xing Chen, Weisheng Zhao - Beihang Univ., Beijing, China

71**APPROXIMATE COMMON CORE MATH**

Time: 10:30am - 12:00pm || **Room:** N253 || **Event Type:** Research Reviewed
Keywords: Architecture & System Design || **Topic Area:** Design

CHAIR:

Mircea Stan - Univ. of Virginia, Charlottesville, VA

CO-CHAIR:

Swagath Venkataramani - IBM T.J. Watson Research Center, New York, NY

Much of the effort on approximate computing has focused on the design of foundational building blocks, namely arithmetic units. This session presents four papers on approximate designs for arithmetic units. The first two papers focus on improving the Pareto-frontier of approximate multiplier designs. The last two papers discuss both approximate and stochastic approaches to dividers and square roots.

71.1 ApproxLP: Approximate Multiplication with Linearization and Iterative Error Control

Mohsen Imani, **Alice Sokolova**, Ricardo A. Garcia, Andrew Huang - Univ. of California, San Diego, La Jolla, CA
Fan Wu - Univ. of California, Riverside, CA
Baris Aksanli - San Diego State Univ., San Diego, CA
Tajana Rosing - Univ. of California, San Diego, La Jolla, CA

71.2 Cooperative Arithmetic-aware Approximation Techniques for Energy-efficient Multipliers

Vasileios Leon, Konstantinos Asimakopoulos, **Sotirios Xydis**, Dimitrios Soudris, Kiamal Pekmestzi - National Technical Univ. of Athens, Greece

71.3 Approximate Integer and Floating-point Dividers with Near-zero Error Bias

Hassaan Saadat - Univ. of New South Wales, Sydney, Australia
Haris Javaid - Xilinx Inc., Singapore
Sri Parameswaran - Univ. of New South Wales, Sydney, Australia

71.4 In-stream Stochastic Division and Square Root via Correlation

Di Wu, Joshua San Miguel - Univ. of Wisconsin, Madison, WI

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

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LEARN YOUR LESSONS - MACHINE LEARNING AND SECURITY

Time: 10:30am - 12:00pm || **Room:** N254 || **Event Type:** Research Reviewed
Keywords: Security & Privacy, System Security || **Topic Area:** Security, Machine Learning/AI

CHAIR:

Christopher Harris - Auburn Univ., Auburn, AL

CO-CHAIR:

Aydin Aysu - North Carolina State Univ., Raleigh, NC

This session focuses on security in the context of machine learning. The first paper presents optimization techniques to modify the neural network parameters to disrupt function; The second paper leverages adversarial examples to enhance the security of speech recognition against eavesdropping; The third paper develops an adversarial example generator to circumvent the ML-based malware detector; The last paper proposes to better detect malware by re-purposing the embedded processor traces.

72.1 MASKER: Adaptive Mobile Security Enhancement Against Automatic Speech Recognition in Eavesdropping

Fuxun Yu, Zirui Xu - George Mason Univ., Fairfax, VA
Chenchen Liu - Clarkson Univ., Potsdam, NY
Xiang Chen - George Mason Univ., Fairfax, VA

72.2 Adversarial Attack on Microarchitectural Events based Malware Detectors

Sai Manoj Pudukotai Dinakarao, Sairaj Amberkar, Sahil Bhat, Abhijit Dhavle, Hossein Sayadi, Avesta Sasan, Houman Homayoun, Setareh Rafatirad - George Mason Univ., Fairfax, VA

72.3 Fault Sneaking Attack: A Stealthy Framework for Misleading Deep Neural Networks

Pu Zhao, Siyue Wang, Cheng Gongye, Yanzhi Wang, Yunsi Fei, Xue Lin - Northeastern Univ., Boston, MA

72.4 PREEMPT: PReempting Malware by Examining Embedded Processor Traces

Kanad Basu - New York Univ., Brooklyn, NY
Rana Elnagar, Krishnendu Chakrabarty - Duke Univ., Durham, NC
Ramesh Karri - New York Univ., Brooklyn, NY

73

GETTING THE MOST OF RESOURCE-CONSTRAINED SYSTEMS

Time: 10:30am - 12:00pm || **Room:** N255 || **Event Type:** Research Reviewed
Keywords: Verification/Validation, Implementation, Architecture & System Design
Topic Area: Embedded Systems & Software (ESS)

CHAIR:

Achim Rettberg - Hochschule Hamm-Lippstadt, Germany

CO-CHAIR:

Henri-Pierre Charles - CEA, Grenoble, France

This session presents innovations for the prediction-based resource allocation and scheduling. The first paper presents a harmonization and partitioning scheme for periodic real-time tasks. The second paper discusses a multi-resource allocation framework that integrates shared cache allocation with memory bandwidth regulation for virtualized CPUs. The third contribution takes advantage of workload prediction to improve the resource management efficiency. The last paper applies machine learning to find optimal task partitioning and mapping in heterogeneous architectures.

73.1 Workload-aware Harmonic Partitioned Scheduling of Periodic Real-time Tasks with Constrained Deadlines

Jiankang Ren, Xiaoyan Su - Dalian Univ. of Technology, Dalian, China
Guoqi Xie - Hunan Univ., Changsha, China
Chao Yu, Guozhen Tan, Guowei Wu - Dalian Univ. of Technology, Dalian, China

73.2 Holistic Multi-resource Allocation for Multicore Real-time Virtualization

Meng Xu - Apple, Inc., Cupertino, CA
Robert Gifford, Linh Thi Xuan Phan - Univ. of Pennsylvania, Philadelphia, PA

73.3 Runtime Resource Management with Workload Prediction

mina niknafs, Ivan Ukhov, Petru Eles, Zebo Peng - Linköping Univ., Linköping, Sweden

73.4 Code Mapping in Heterogeneous Platforms Using Deep Learning and LLVM-IR

Francesco Barchi, Gianvito Urgese, Enrico Macii, Andrea Acquaviva - Politecnico di Torino, Italy

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

74**ENERGY AND TEMPERATURE: RUN-TIME MANAGEMENT TO THE RESCUE****Time: 10:30am - 12:00pm || Room: N257 || Event Type: Research Reviewed****Keywords: Low Power, Architecture & System Design || Topic Area: EDA, Embedded Systems & Software (ESS)****CHAIR:**

Eli Bozorgzadeh - Univ. of California, Irvine, CA

CO-CHAIR:

Ronald Dreslinski - Univ. of Michigan, Ann Arbor, MI

This session focuses on run-time techniques to optimize energy and temperature. The first paper describes a method of automatically switching among energy-accuracy trade-off operating modes in an energy harvesting Internet-of-Things system. The second describes a scheduling method that considers availability and energy efficiency in solar-powered energy scavenging systems. The third describes methods to operate multiply accumulate units within tensor processing units at near the threshold voltage, then address resulting timing errors. The fourth paper describes a method to assign data/tasks to physical locations in three-dimensional stacked chip processor-in-memory systems to improve thermal and performance characteristics.

74.1 REAP: Runtime Energy-accuracy Optimization for Energy Harvesting IoT Devices

Ganapati Bhat, Kunal Bagewadi - Arizona State Univ., Tempe, AZ
Hyung Gyu Lee - Daegu University, Republic of Korea
Umit Y. Ogras - Arizona State Univ., Tempe, AZ

74.2 Tumbler: Energy Efficient Task Scheduling for Dual-channel Solar-powered Sensor Nodes

Yue Xu - Chongqing Univ., Chongqing, China
Hyung Gyu Lee - Daegu University, Republic of Korea
Yujuan Tan, Yu Wu, Xianzhang Chen, Liang Liang - Chongqing Univ., Chongqing, China
Lei Qiao - Beijing Institute of Technology, Beijing, China
Duo Liu - Chongqing Univ., Chongqing, China

74.3 GreenTPU: Improving Timing Error Resilience of a Near-threshold Tensor Processing Unit

pramesh pandey, Prabal Basu, Koushik Chakraborty, Sanghamitra Roy - Utah State Univ., Logan, UT

74.4 Thermal-aware Design and Management for Search-based In-memory Acceleration

Minxuan Zhou, Mohsen Imani, Saransh Gupta, Tajana Rosing - Univ. of California, San Diego, La Jolla, CA

75**EDA OPEN SOURCING: DAWN OF A GOLDEN AGE OR PIPE DREAM?****Time: 10:30am - 12:00pm || Room: N259 || Event Type: Panel || Keywords: Front-end Design, Back-end Design, Implementation || Topic Area: EDA, Design****MODERATOR:**

Leon Stok - IBM Corp., Yorktown Heights, NY

ORGANIZERS:

Noel Menezes - Intel Corp., Hillsboro, OR
Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

Open-source development is well established as a viable model for funding software development. Vibrant businesses and business models have developed around the “free” software that open sourcing provides. CAD itself has a rich history of successful open-sourcing starting with SPICE (in the seventies) and SIS (in the eighties) which were successfully used by the design houses that comprise the EDA customer base. In the last couple of decades, other than a few specific logic solvers, large-scale EDA open-source success stories have been hard to find. While arguments have been made, mostly by academics, that the commoditization of CAD tooling provides fertile ground, open-sourcing efforts have not succeeded at a large scale.

Recent government initiatives have jump-started interest in the latent CAD open-sourcing community. Several significant efforts have been funded some of which are represented in this special session. This panel will provide an opportunity for the open-source bigots to tell us why it will be different this time around while serving as a platform for the naysayers to tell us why “the more things change, the more they are the same.”

PANELISTS:

Andrew Kahng - Univ. of California, San Diego, La Jolla, CA
Andreas Olofsson - Defense Advanced Research Projects Agency, Arlington, VA
Shankar Krishnamoorthy - Synopsys, Inc., Mountain View, CA
Arun Subbiah - Intel Corp., Hillsboro, OR
Charles J. Alpert - Cadence Design Systems, Inc., Austin, TX

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

76**RELIABLE AND SECURE ML: CHALLENGES ACROSS H/W AND S/W STACKS**

Time: 10:30am - 12:00pm | **Room:** N261 | **Event Type:** Special Session
Keywords: Security & Privacy, Test/Manufacturing/Reliability/Safety, Emerging Technologies | **Topic Area:** Machine Learning/AI, Security

CHAIR:

Christos Kyrkou - Univ. of Cyprus, Nicosia, Cyprus

ORGANIZERS:

Theocharis Theocharides - Univ. of Cyprus, Nicosia, Cyprus
Muhammad Shafique - Technische Univ. Wien, Vienna, Austria

Machine Learning is the de-facto data analysis paradigm embedded within several computing devices, consumer electronics and cyber-physical systems. The need integrating real-time robust data analytics requires revolutionizing the way we design, implement, build and verify such systems. While the slight inaccuracy in some applications may not have severe consequences, in safety-critical applications such as autonomous driving and healthcare, a small error can lead to catastrophic effects. We therefore need to consider hardware and software architectures and methodologies that can produce reliable, robust and trustworthy results in the presence of faults (hardware and/or software), attacks (direct on the system or indirect in a location that affects the system itself) while also preserving security and privacy. The scope of this special session therefore is to bring together researchers and experts in security and robustness that will discuss ongoing and emerging challenges and opportunities for designing robust and reliable machine learning systems.

76.1 Building Robust Machine Learning Systems: Current Progress, Research Challenges, and Opportunities

Jeff (Jun) Zhang, Kang Liu - New York Univ., NY
Faiq Khalid, Muhammad Abdullah Hanif, Semeen Rehman - Vienna Univ. of Technology, Vienna, Austria
Theocharis Theocharides, Alessandro Artusi - Univ. of Cyprus, Nicosia, Cyprus
Muhammad Shafique - Technische Univ. Wien, Vienna, Austria
Siddharth Garg - New York Univ., Brooklyn, NY

76.2 Adversarial Machine Learning - An Industry Perspective

Jason Martin - Intel Corp., Hillsboro, OR

76.3 Adversarial Machine Learning Beyond the Image Domain

Giulio Zizzo, Chris Hankin, Sergio Maffei - Imperial College London, United Kingdom
Kevin Jones - Airbus S.A.S., Cardiff, United Kingdom

77**FASTER, LONGER, CHEAPER: METHODOLOGIES TO BUILD SYSTEMS**

Time: 1:30 - 3:00pm | **Room:** N252 | **Event Type:** Research Reviewed
Keywords: Architecture & System Design, Test/Manufacturing/Reliability/Safety
Topic Area: EDA

CHAIR:

Arnab Raha - Intel Corp., Santa Clara, CA

CO-CHAIR:

John Brunhaver - Arizona State Univ., Phoenix, AZ

In this session, the first paper mitigates challenging memory-access patterns in crypto-currency mining to make ASIC acceleration possible. The second paper quantifies the design implications of a chiplet-based design meant to reduce non-recurring design costs. The third paper evenly distributes tasks over a multi-core system in order to mitigate aging and maximizing aggregate available frequency during its lifetime. Finally, the fourth paper provides an accurate model for designing systems that are sped up by eliminating timing margin and robust to age-related timing degradation.

77.1 Memory-bound Proof-of-work Acceleration for Blockchain Applications

Kun Wu, Guohao Dai - Tsinghua Univ., Beijing, China
Xing Hu, Shuangchen Li, Xinfeng Xie - Univ. of California, Santa Barbara, CA
Yu Wang - Tsinghua Univ., Beijing, China
Yuan Xie - Univ. of California, Santa Barbara, CA

77.2 Architecture, Chip, and Package Co-design Flow for 2.5D Integration of Reusable IP Chiplets

Jinwoo Kim, Gauthaman Murali, Heechun Park, Eric Qin, Hyoukjun Kwon, Venkata Chaitanya Krishna Chekuri, Nihar Dasari, Arvind Singh, Minah Lee, Hakki M. Torun, Kallol Roy, Madhavan Swaminathan, Saibal Mukhopadhyay, Tushar Krishna, Sung Kyu Lim - Georgia Institute of Technology, Atlanta, GA

77.3 LifeGuard: A Reinforcement Learning-based Task Mapping Strategy for Performance-centric Aging Management

Vijeta Rathore - Nanyang Technological Univ., Singapore, Vivek Chaturvedi - Indian Institute of Technology Palakkad, India
Amit K. Singh - Univ. of Essex, United Kingdom
Thambipillai Srikanthan - Nanyang Technological Univ., Singapore
Muhammad Shafique - Technische Univ. Wien, Austria

77.4 Accurate Estimation of Program Error Rate for Timing-speculative Processors

Omid Assare, Rajesh Gupta - Univ. of California, San Diego, La Jolla, CA

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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78**HIGHLY EFFICIENT AI PROCESSING ON RESOURCE CONSTRAINED SYSTEMS**

Time: 1:30 - 3:00pm || **Room:** N253 || **Event Type:** Research Reviewed
Keywords: Architecture & System Design || **Topic Area:** Embedded Systems & Software (ESS)

CHAIR:

Ruija Wang - Illinois Institute of Technology, Chicago, IL

CO-CHAIR:

Noel Menezes - Intel Corp, Santa Clara, CA

This session offers stimulating insights to build high-efficiency AI systems in different embedded scenarios with comprehensive innovations at architecture, system, and run-time application levels. The first paper presents a fast design space exploration methodology to maximize utilization of neural processors. The second paper proposes a mechanism to reduce the LSTM network latency and energy consumption on edge devices. The third paper performs run-time reconfiguration of neural networks to satisfy embedded resource constraints. Finally, the fourth paper designs approximate ECG processing for edge devices.

78.1 Fast Performance Estimation and Design Space Exploration of Manycore-based Neural Processors

Jintaek Kang, Dowhan Jung, Kwanghyun Chung, Soonhoi Ha - Seoul National Univ., Seoul, Republic of Korea

78.2 E-LSTM: Efficient Inference of Sparse LSTM on Embedded Heterogeneous System

Runbin Shi, Junjie Liu - Univ. of Hong Kong
Shuo Wang, Yun Liang - Peking Univ., Beijing, China
Hayden So - Univ. of Hong Kong

78.3 ReForm: Static and Dynamic Resource-aware DNN Reconfiguration Framework for Mobile Devices

Zirui Xu, Fuxun Yu, Liang Zhao - George Mason Univ., Fairfax, VA
Chenchen Liu - Clarkson Univ., Potsdam, NY
Xiang Chen - George Mason Univ., Fairfax, VA

78.4 XBioSiP: A Methodology for Approximate Bio-signal Processing at the Edge

Bharath Srinivas Prabakaran, Semeen Rehman, Muhammad Shafique - Technische Univ. Wien, Austria

79**BUGS AND VULNERABILITIES: WE GOT YOU!**

Time: 1:30 - 3:00pm || **Room:** N254 || **Event Type:** Research Reviewed
Keywords: Verification/Validation || **Topic Area:** EDA

CHAIR:

Umair Siddique - BlackBerry Limited, Ottawa, Canada

CO-CHAIR:

Khaza Anuarul Hoque - Univ. of Missouri, Columbia MO

A mix of pre- and post-silicon techniques and methodologies to find bugs and vulnerabilities from gate level to software layers. The first paper describes a reverse engineering approach to verify multipliers. The second tackles cycle-accurate tracing of signals for post-silicon SoC. The third addresses equivalence checking for proving the correctness of firmware optimization. Finally, the fourth is about concolic testing for RISC-V system with peripherals.

79.1 RevSCA: Using Reverse Engineering to Bring Light into Backward Rewriting for Big and Dirty Multipliers

Alireza Mahzoon, Daniel Grosse, Rolf Drechsler - Univ. of Bremen, Germany

79.2 Temporal Tracing of On-chip Signals Using Timeprints

Rehab Massoud, Hoang M. Le - Univ. of Bremen, Germany
Peter Chini, Prakash Saivasan, Roland Meyer - Technische Univ. Braunschweig, Germany
Rolf Drechsler - Univ. of Bremen, Germany

79.3 ACCESS: HW/SW Co-equivalence Checking for Firmware Optimization

Michael Schwarz - Technische Universität Kaiserslautern, Germany
Raphael Stahl, Daniel Mueller-Gritschneider, Ulf Schlichtmann - Technische Univ. München, Germany
Dominik Stoffel, Wolfgang Kunz - Technische Universität Kaiserslautern, Germany

79.4 Early Concolic Testing of Embedded Binaries with Virtual Prototypes: A RISC-V Case Study

Vladimir Herdt, Daniel Grosse, Hoang M. Le, Rolf Drechsler - Univ. of Bremen, Germany

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

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HIGH PERFORMANCE AND ENERGY EFFICIENT ARCHITECTURES FOR IOT APPLICATIONS

Time: 1:30 - 3:00pm || Room: N255 || Event Type: Research Reviewed

Keywords: Architecture & System Design, IoT || Topic Area: Design, Embedded Systems & Software (ESS)

CHAIR:

Lixue Xia - Alibaba Group Holding Limited, Beijing China

CO-CHAIR:

Christian Pilato - Polytechnic Univ. of Milan, Italy

High-performance and energy-efficient architectures are crucial to the success of many emerging IoT applications. This session starts with a novel high-performance streaming accelerator for medical imaging device, followed by an energy-efficient architecture for low-power probabilistic inference. The next two papers present optimized designs for IoT personalization and lightweight neural networks.

80.1 Tetris: A Streaming Accelerator for Physics-limited 3D Plane-wave Ultrasound Imaging

Brendan L. West - Univ. of Michigan, Ann Arbor, Michigan

Jian Zhou - Arizona State Univ., Tempe, AZ

Ronald G. Dreslinski, J. Brian Fowlkes, Oliver Kripfgans - Univ. of Michigan, Ann Arbor, MI

Chaitali Chakrabarti - Arizona State Univ., Tempe, AZ

Thomas F. Wenisch - Univ. of Michigan, Ann Arbor, MI

80.2 ProbLP: A Framework for Low-precision Probabilistic Inference

Nimish Shah, Laura I. Galindez Olascoaga - MICAS, Electrical Engineering, KU Leuven, Heverlee, Belgium

Wannes Meert - DTAI, Computer Science, KU Leuven, Heverlee, Belgium

Marian Verhelst - MICAS, Electrical Engineering, KU Leuven, Heverlee, Belgium

80.3 An Optimized Design Technique of Low-bit Neural Network Training for Personalization on IoT Devices

Seungkyu Choi, Jaekang Shin, Yeongjae Choi, Lee-Sup Kim - Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

80.4 L-MPC: A LUT based Multi-level Prediction-correction Architecture for Accelerating Binary-weight Hourglass Network

Hong Liu, Leibo Liu - Tsinghua Univ., Beijing, China

Wenping Zhu - Chinese Academy of Sciences, Beijing, China

Qiang Li - Intel Corp., Beijing, China

Huiyu Mo, Shaojun Wei - Tsinghua Univ., Beijing, China

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STAYING AFLOAT: HOW TO NOT DROWN BY STREAMING DATA

Time: 1:30 - 3:00pm || Room: N257 || Event Type: Research Reviewed

Keywords: Architecture & System Design || Topic Area: Design

CHAIR:

Tulika Mitra - National Univ. of Singapore, China

Important emerging applications require continuous processing of large amounts of streaming data. These diverse works solve challenges in high-throughput data processing, using streaming accelerators, high-throughput memories and dynamic compilation. This session begins with domain specific accelerators for autonomous vision and line-speed data analytics. The second half of this session generalizes across domains, first with dynamic compilation for reconfigurable accelerators, and finally with transparently managed high-bandwidth memory.

81.1 eSLAM: An Energy-efficient Accelerator for Real-time ORB-SLAM on FPGA Platform

Runze Liu, Jianlei Yang - Beihang Univ., Beijing, China

Yiran Chen - Duke Univ., Durham, NC

Weisheng Zhao - Beihang Univ., Beijing, China

81.2 ShuntFlow: An Efficient and Scalable Dataflow Accelerator Architecture for Streaming Applications

Shijun Gong, Jiajun Li - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

Wenyan Lu, Guihai Yan, Xiaowei Li - Chinese Academy of Sciences, Beijing, China

81.3 A General Pattern-based Dynamic Compilation Framework for Coarse-grained Reconfigurable Architectures

Xingchen Man, Leibo Liu, Jianfeng Zhu, Shaojun Wei - Tsinghua Univ., Beijing, China

81.4 ReTagger: An Efficient Controller for DRAM Cache Architectures

Mahdi Bojnordi, Farhan Nasrulla - Univ. of Utah, Salt Lake City, UT

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

82

THE FUTURE OF AI: TO SPIKE OR NOT TO SPIKE?

Time: 1:30 - 3:00pm || **Room:** N259 || **Event Type:** Panel || **Keywords:** Emerging Technologies || **Topic Area:** Machine Learning/AI, Autonomous Systems

MODERATOR:

Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI

ORGANIZER:

Arijit Raychowdhury - Georgia Institute of Technology, Atlanta, GA

The current wave of AI is changing society and our lives in unprecedented ways. As we look at the challenges of the current hardware and software solutions that power deep neural networks, some key questions emerge. Should we move closer towards neuromorphic systems and borrow cues from the brain? Or should statistical techniques for data analysis take precedence? Will future AI systems use CPU/GPU/FPGAs and specialized accelerators, such as Google's TPU, in traditional deep neural networks; or are spiking neuromorphic engines, such as IBM's TrueNorth and Intel's Loihi, the right path forward? Further, emerging technologies: logic, memory and integration, are expected to play crucial roles in the next-generation of intelligent systems. This panel will feature experts in

AI systems as we discuss a wide range of issues in traditional/emerging technologies, circuit-design, architectures, algorithms and computational theory. We will debate whether spiking neural networks or traditional machine-learning algorithms, are expected to dominate the next decade of ubiquitous intelligence, continuous learning and extreme energy-efficiencies -- from the edge to the cloud.

PANELISTS:

Kaushik Roy - Purdue Univ., West Lafayette, IN

Mike Davies - Intel Corp., Hillsboro, OR

Brucek Khailany - NVIDIA Corp., Santa Clara, CA

Cliff Young - Google, Inc., Mountain View CA

83

RESILIENCE REVISITED - TOWARDS A SYSTEM PERSPECTIVE

Time: 1:30 - 3:00pm || **Room:** N261 || **Event Type:** Special Session

Keywords: Test/Manufacturing/Reliability/Safety, Architecture & System Design, Verification/Validation || **Topic Area:** Embedded Systems & Software (ESS), EDA

CHAIR:

Muhammad Shafique - Technische Univ. Wien, Vienna, Austria

ORGANIZER:

Ulf Schlichtmann - Tech. Univ. of Munich, Germany

In the wake of the upcoming age of autonomous driving, drone deliveries and Industry 4.0 automation, powerful computing platforms are increasingly deployed in safety-critical applications. The underlying complex electronics suffer from random hardware faults such as radiation-induced soft errors, which may cause a corruption of data or program execution. Hence, safety standards such as the ISO 26262 are introduced, which demand that the overall system must remain in a safe state even in the presence of such random faults.

There has been extensive research in the field of resilience of computing systems against the impact of soft errors. Yet, soft error resilience remains a major challenge in the design of future safety-critical systems. This session aims to present cutting-edge research results from this area with key insights from the viewpoint both of academia as well as industry.

83.1 Software Approaches for In-time Resilience

Aviral Srivastava - Arizona State Univ., Tempe, AZ

Moslem Dideban - Cadence Design Systems, Inc., Tempe, AZ

83.2 Cross-layer Resilience: Challenges, Insights, and the Road Ahead

Eric Cheng - Stanford Univ., Baltimore, MD

Daniel Mueller-Gritschneider - Tech. Univ. of Munich, Germany

Jacob Abraham - Univ. of Texas at Austin, TX

Pradip Bose, Alper Buyuktosunoglu - IBM Research, Yorktown Heights, NY

Deming Chen - Univ. of Illinois at Urbana-Champaign, IL

Hyungmin Cho - Hongik Univ., Seoul, Republic of Korea

Yanjing Li - Univ. of Chicago, IL

Uzair Sharif - Tech. Univ. of Munich, Germany

Kevin Skadron, Mircea Stan - Univ. of Virginia, Charlottesville, VA

Ulf Schlichtmann - Tech. Univ. of Munich, Germany

Subhasish Mitra - Stanford Univ., Palo Alto, CA

83.3 Increasing Soft Error Resilience by Software Transformation

Michael Werner, Moomen Chaari, Devarajegowda Keerthikumara

Wolfgang Ecker - Infineon Technologies AG, Munich, Germany

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

84

IMPERFECT IS THE NEW PERFECT: APPROXIMATE COMPUTING FOR DNNs**Time: 3:30 - 5:30pm || Room: N252 || Event Type: Research Reviewed****Keywords: Architecture & System Design || Topic Area: Machine Learning/AI****CHAIR:**

Mohammed Shafique - Vienna Univ. of Technology, Wien, Austria

CO-CHAIR:

Kaushik Vaidyanathan - Google, Inc., Mountain View CA

Papers in this session employ approximate computing to optimize the performance and energy of deep neural networks. The first two papers focus on new methods for quantization. The third and fourth papers eliminate computations in DNNs. The fifth paper alleviates the impact of timing errors on accuracy. The final paper heals the effect of memory errors due relaxed DRAM refreshes.

84.1 FlightNNs: Lightweight Quantized Deep Neural Networks for Fast and Accurate Inference

Ruizhou Ding, Zeye Liu, Ting-Wu Chin, Diana Marculescu, Ronald Blanton - Carnegie Mellon Univ., Pittsburgh, PA

84.2 BiScaled-DNN: Quantizing Long-tailed Data-structures with Two Scale Factors for Deep Neural NetworksShubham Jain - Purdue Univ., West Lafayette, IN
Swagath Venkataramani, Vijayalakshmi Srinivasan, Jungwook Choi, Kailash Gopalakrishnan, Leland Chang - IBM T.J. Watson Research Center, Yorktown Heights, NY**84.3 A None-sparse Deep Learning Accelerator that Explores the Computation Redundancy in Neural Networks**

Ying Wang, Shengwen Liang, Huawei Li, Xiaowei Li - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

84.4 On the Complexity Reduction of Dense Layers from O(N^2) to O(N logN) with Cyclic Sparsely Connected Layers

Seyed-Morteza Hosseini, Mark Horton, Hirenkumar S. Paneliya, Uttej Kallakuri, Tinoosh Mohsenin - Univ. of Maryland, Baltimore, MD

84.5 Sensitivity Based Error Resilient Techniques for Energy Efficient Deep Neural Network AcceleratorsWonseok Choi, Dongyeob Shin, Jongsun Park - Korea Univ., Seoul, Republic of Korea
Swaroop Ghosh - Pennsylvania State Univ., University Park, PA**84.6 St-DRC: Stretchable DRAM Refresh Controller with No Parity-overhead Error Correction Scheme for Energy-efficient DNNs**Duy-Thanh Nguyen - Kyung Hee Univ., Republic of Korea
Nhut-Minh Ho - National Univ. of Singapore
Ik-Joon Chang - Kyung Hee Univ., Republic of Korea

85

EMERGING NEURAL ACCELERATOR DESIGNS AND TECHNIQUES**Time: 3:30 - 5:30pm || Room: N253 || Event Type: Research Reviewed****Keywords: Architecture & System Design || Topic Area: Machine Learning/AI, Design****CHAIR:**

Shuo-Han Chen - Academia Sinica, Taipei City, Taiwan

CO-CHAIR:

Dimitrios Soudris - National Technical Univ. of Athens, Greece

This session presents six papers for emerging neural network accelerator designs with sparsity/co-design/scale-out techniques.

The first paper presents algorithm/hardware co-design for object detection. The second paper reports scale-out acceleration of lung nodule segmentation on a multi-FPGA platform. The third paper accelerates data centric graph traversal on FPGAs. Peregrine presents an LSTM accelerator that supports a wide range of sparsity. Systolic Cube work describes a CNN accelerator for video inputs that includes temporal domain data. The final paper presents context-aware CNN design for distributed system in collaborative computing.

85.1 FPGA/DNN Co-design: An Efficient Design Methodology for IoT Intelligence on the EdgeCong Hao, Xiaofan Zhang, Yuhong Li, Sitao Huang - Univ. of Illinois at Urbana-Champaign, IL
Jinjun Xiong - IBM Research, Yorktown Heights, NY
KYLE J. RUPNOW - Inspirit IoT, Inc., Wheeling, WV
Wen-mei Hwu, Deming Chen - Univ. of Illinois at Urbana-Champaign, IL**85.2 Scale-out Acceleration for 3D CNN-based Lung Nodule Segmentation on a Multi-FPGA system**Junzhong Shen, Deguang Wang, You Huang, Mei Wen - National Univ. of Defense Technology, Changsha, China
Chunyuan Zhang - National Aeronautics and Space Administration, Changsha, China**85.3 Dr. BFS: Data-centric Breadth-first Search on FPGAs**

Eric Finnerty, Zach Sherer, Yan Luo, Hang Liu - Univ. of Massachusetts, Lowell, MA

85.4 Peregrine: A Flexible Hardware Accelerator for LSTM with Limited Synaptic Connection PatternsJaeha Kung - Daegu Gyeongbuk Institute of Science and Technology, Daegu, Republic of Korea
Junki Park - Pohang Univ. of Science and Technology, Pohang, Republic of Korea
Sehun Park - Daegu Gyeongbuk Institute of Science and Technology, Daegu, Republic of Korea
Jae-Joon Kim - Pohang Univ. of Science and Technology, Pohang, Republic of Korea**85.5 Systolic Cube: A Spatial 3D CNN Accelerator Architecture for Low Power Video Analysis**Yongchen Wang, Ying Wang, Huawei Li - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China
Shi Cong - School of Microelectronics and Communication Engineering, Chongqing University, Beijing, China
Xiaowei Li - Chinese Academy of Sciences, Beijing, China**85.6 Context-aware Convolutional Neural Network over Distributed System in Collaborative Computing**

Jinhang Choi, Zeinab Hakimi, Philip W. Shin, Jack Sampson, Vijaykrishnan Narayanan - Pennsylvania State Univ., University Park, PA

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

86

EMERGING FLASH MEMORY AND RELIABILITY**Time: 3:30 - 5:30pm || Room: N255 || Event Type: Research Reviewed****Keywords: Architecture & System Design, Emerging Technologies****Topic Area: Embedded Systems & Software (ESS), Design****CHAIR:**

Weiwen Jiang - Chongqing Univ., Chongqing, China

CO-CHAIR:

Lei Yang - Chongqing Univ., Chongqing, China

As feature sizes shrunk and technologies shift, new issues and challenges come with emerging flash memory, in particular, reliability. The topics of this session are largely classified into two: i) low-level techniques with different access granularities and ii) approximation for better reliability/performance management. These approaches of this session control reliability of the underlying flash media while maximizing access performance at different levels of computing layers, ranging from systems to device controllers.

86.1 The Best of Both Worlds: On Exploiting Bit-alterable NAND Flash for Lifetime and Read Performance Optimization

Shuo-Han Chen, Ming-Chang Yang - Chinese Univ. of Hong Kong, Shatin, Hong Kong
Yuan-Hao Chang - Academia Sinica, Taipei City, Taiwan

86.2 WAS: Wear Aware Superblock Management for Prolonging SSD Lifetime

Shunzhuo Wang, Fei Wu - Huazhong Univ. of Science & Technology, Wuhan, China

Chengmo Yang - Univ. of Delaware, Newark, DE

Jiaona Zhou, Changsheng Xie, Jiguang Wan - Huazhong Univ. of Science & Technology, Wuhan, China

86.3 ASCache: An Approximate SSD Cache for Error-tolerant Applications

Fei Li, **Youyou Lu** - Tsinghua Univ., Beijing, China
Zhongjie Wu - Alibaba Group Holding Limited, Beijing China
Jiwu Shu - Tsinghua Univ., Beijing, China

86.4 Leveraging Approximate Data for Robust Flash Storage

Qiao Li - City Univ. of Hong Kong, Hong Kong
Liang Shi - East China Normal Univ., Shanghai, China
Jun Yang, **Youtao Zhang** - Univ. of Pittsburgh, PA
Chun Jason Xue - City Univ. of Hong Kong, Hong Kong

87

LAST BUT NOT LEAST: FROM ROUTING TO LAYOUT CLOSURE**Time: 3:30 - 5:30pm || Room: N257 || Event Type: Research Reviewed****Keywords: Back-end Design, Implementation || Topic Area: EDA****CHAIR:**

Wen-Hao Liu - Cadence Design Systems, Inc., Austin, TX

CO-CHAIR:

Myoungsoo Jung - Yonsei Univ., Seoul, Republic of Korea

The last mile of chip design closure, a nightmare or an opportunity? This session explores research frontiers in this area, with machine learning and advanced optimization techniques. This session first presents advancements on bus-based routing techniques, which guarantee routability while honoring similar topological constraints. Then, a recommender system is proposed to explore the best flow settings for the design closure from 14nm to 7nm industrial designs. To overcome the nightmare of routing closure in 10/7nm nodes, deep learning methodologies are introduced to mitigate routing congestions and improve pin accessibility. This session ends with a timing-driven dummy fill insertion study on layout finishing for manufacturing.

87.1 MARCH: MAze Routing Under a Concurrent and Hierarchical Scheme for Buses

Jingsong Chen, Jinwei Liu, Gengjie Chen, Dan Zheng, Evangeline F.Y. Young - Chinese Univ. of Hong Kong, Shatin, Hong Kong

87.2 A DAG-based Algorithm for Obstacle-aware Topology-matching On-track Bus Routing

Chen-Hao Hsu, Shao-Chun Hung, Hao Chen, Fan-Keng Sun, Yao-Wen Chang - National Taiwan Univ., Taipei, Taiwan

87.3 A Learning-based Recommender System for Autotuning Design Flows of Industrial High-performance Processors

Jihye Kwon - Columbia Univ., New York, NY
Matthew M. Ziegler - IBM T.J. Watson Research Center, Yorktown Heights, NY
Luca P. Carloni - Columbia Univ., New York, NY

87.4 Painting on Placement: Forecasting Routing Congestion Using Conditional Generative Adversarial Nets

Cunxi Yu, **Zhiru Zhang** - Cornell Univ., Ithaca, NY

87.5 Pin Accessibility Prediction and Optimization with Deep Learning-based Pin Pattern Recognition

Tao-Chun Yu, **Shao-Yun Fang** - National Taiwan Univ. of Science and Technology, Taipei, Taiwan
Hsien-Shih Chiu, **Kai-Shun Hu** - Synopsys Taiwan Co., Ltd., Taipei, Taiwan
Philip Hui-Yuh Tai - Synopsys, Inc., Mountain View, CA
Chin-Fang Cindy Shen - Synopsys Taiwan Co., Ltd., Taipei, Taiwan
Henry Sheng - Synopsys, Inc., Mountain View, CA

87.6 FIT: Fill Insertion Considering Timing

Bentian Jiang, **Xiaopeng Zhang**, **Ran Chen**, **Gengjie Chen**, **Peishan Tu**, **Wei Li**, **Evangeline F.Y. Young**, **Bei Yu** - Chinese Univ. of Hong Kong, Shatin, Hong Kong

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

88

IN CAD WE TRUST? THE QUESTION THAT DEFINES OUR TRUSTED MICROELECTRONICS FUTURE

Time: 3:30 - 5:00pm || Room: N261 || Event Type: Special Session

Keywords: Hardware Security, Test/Manufacturing/Reliability/Safety, Verification/Validation || Topic Area: Security, EDA

CHAIR:

Saverio Fazzari - Booz Allen Hamilton, Inc., Arlington, VA

ORGANIZERS:

Sandip Ray - Univ. of Florida, Gainesville, FL

Zhenkun Yang - Intel Corp., Hillsboro, OR

Security and trust of microelectronics have emerged as a major concern in the semiconductor industry due to the globalization of design, manufacturing, testing, and distribution process. Globalization and a complex supply chain promote a growing reliance on untrusted tools, components, intellectual property (IP) blocks, and people involved in the semiconductor life cycle, that can maliciously alter its desired function during field operation, e.g., through insertion of a hardware Trojan in a fabricated chip. The issue of hardware trust is inevitably plaguing security of electronic systems that build on these components. These security issues range from hidden backdoor, denial of service, privilege escalation, to reliability degradation. In this special session, we will cover the defining role of CAD in design, verification and deployment of trusted microelectronics, by combining views from academic, industry and government representatives.

88.1 The Metric Matters: The Art of Measuring Trust in Electronics

Jonathan Cruz, Prabhat Mishra, Swarup Bhunia - Univ. of Florida, Gainesville, FL

88.2 A Practical Application of Trust through Technology

Kenneth Plaks - Defense Advanced Research Projects Agency, Arlington, VA

88.3 Tool-based Approaches for Improving Microelectronics and Supply Chain Security

Yousef Iskander - Cisco Systems, Inc., Knoxville, TN

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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THURSDAY, JUNE 6

THURSDAY IS
TRAINING DAY

TRACK 1, PART I: HOW TO BUILD VERIFICATION ENVIRONMENTS IN SYSTEMVERILOG

Time: 10:15am - 1:15pm || **Room:** N260 || **Event Type:** Thursday is Training Day
Keywords: Verification/Validation || **Topic Area:** EDA

This session will teach the key SystemVerilog language skills needed to understand and build constrained random verification environments, as used by UVM. The emphasis will be on learning to apply the concepts of object-oriented programming to the creation of a re-usable test bench infrastructure. Language features will be taught using working code examples, which delegates can run immediately on the EDA Playground website and will be available to use and share after the class.

Topics to be taught include the object-oriented and constrained random language features of SystemVerilog, and more particularly how to use these language features to build a verification environment that includes a component hierarchy and transaction-level communication.

The knowledge taught in this session is an essential prerequisite to the afternoon session on UVM.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKER:

David C. Black - Doulos, Austin, TX

Thank you to our Sponsor:



TRACK 2, PART I - THE PYTHON LANGUAGE: BECOME A PYTHONEER!

Time: 10:15am - 1:15pm || **Room:** N262 || **Event Type:** Thursday is Training Day
Topic Area: EDA, Design

This session will teach attendees the basics of the Python programming language. Python has become enormously popular as a programming language because it is compact, elegant, productive, readable, and extensible. People often remark that a Python program looks like pseudocode, an English language description of what the code is meant to do. These attributes have led Python to be widely used as a general-purpose scripting language in EDA tool flows, for scientific computing and deep learning, for embedded software test, and even for digital hardware verification and system modeling.

People sometimes become very enthusiastic about Python because of its elegance as a programming language – so-called Pythoners. This session is your chance to become a Pythoneer, and to learn about some of the cool things you can do with Python right out-of-the-box!

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKER:

John Aynsley - Doulos, Ringwood, United Kingdom

Thank you to our Sponsor:



Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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THURSDAY, JUNE 6

THURSDAY IS
TRAINING DAY

TRACK 1, PART II: LEARN UVM USING THE EASIER UVM CODING GUIDELINES AND CODE GENERATOR

Time: 2:15 - 5:15pm || **Room:** N260 || **Event Type:** Thursday is Training Day

Keywords: Verification/Validation || **Topic Area:** EDA

This session will teach the basics of UVM, the Universal Verification Methodology for SystemVerilog, by taking advantage of Doulos' Easier™ UVM Coding Guidelines and Code Generator. All the main concepts of UVM will be taught using working code examples. By running the Easier™ UVM Code Generator on the EDA Playground website, delegates will be able to run UVM examples immediately, experiment with what they have learned, and share their examples with others after the class.

The session is aimed at hands-on engineers who want to start writing UVM code themselves and are looking for some specific advice on the best place to start, the right UVM features and coding idiom to use, and the pitfalls to avoid.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKER:

David C. Black - Doulos, Austin, TX

Thank you to our Sponsor:



TRACK 2, PART II - DEEP LEARNING FOR ELECTRONIC ENGINEERS

Time: 2:15 - 5:15pm || **Room:** N262 || **Event Type:** Thursday is Training Day

Topic Area: EDA, Machine Learning/AI

Deep learning is a very hot topic right now. Deep learning algorithms are proving effective in many existing applications such as image recognition, speech recognition, and natural language processing. Deep learning algorithms are opening the door to many totally novel applications and products, from smart homes to autonomous vehicles, from defense systems to medical systems.

Deep learning will impact DAC attendees in several ways, from the kinds of electronic product we design through to the algorithms used within EDA tools. The session will explain the background to deep learning, the technical jargon, and the main concepts you need to get started. Topics to be covered include basic machine learning algorithms for regression and classification, cost functions, basic neural network models, the distinction between machine learning and deep learning, the training and deployment of neural network models, an overview of the ecosystem including

common deep learning software libraries and frameworks, and how to get started with deep learning. The workshop includes access to working code examples and instruction on how to run them yourself.

This session assumes a basic knowledge of Python. Attendees with no prior knowledge of Python are recommended to attend the morning session The Python Language: Become a Pythoneer!

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKER:

John Aynsley - Doulos, Ringwood, United Kingdom

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COLOCATED CONFERENCES

2019 ACM/IEEE INTERNATIONAL WORKSHOP ON SYSTEM LEVEL INTERCONNECT PREDICTION (SLIP)

Date: Sunday, June 2 || Time: 8:30am - 6:00pm || Room: N249

Event Type: Colocated Conference || Keywords: Interconnect/Networking, Low Power, Architecture & System Design || Topic Area: EDA, Design

ORGANIZERS:

Selcuk Kose - Univ. of Rochester, Rochester, NY

Inna Partin-Vaisband - Univ. of Illinois at Chicago, IL

Mingsong Chen - East China Normal Univ., Shanghai, China

Weize Yu - Old Dominion Univ., Norfolk, VA

Ming-Chang Yang - Chinese Univ. of Hong Kong, Shatin, Hong Kong

Junlong Zhou - Nanjing Univ. of Science and Technology, Nanjing, China

Shantanu Dutt - Univ. of Illinois at Chicago, IL

Boris Vaishband - Univ. of California, Los Angeles, CA

The general technical scope of the workshop is the design, analysis, and optimization of interconnect and communication fabrics in electronic systems. A special emphasis is placed this year on predictive technologies and machine learning applications. The organizing committee invites original contributions in the form of papers, tutorials, panels, special session, and posters. We accept papers based on novelty and contributions to the advancement of the field. The accepted papers will be published in the ACM and IEEE digital libraries.

Technical topics include but are not limited to:

- Learning and predictive models for optimizing interconnect at various IC and system design stages
- System-level design for FPGAs, NoCs, reconfigurable systems
- Design, analysis, and optimization of power and clock networks
- Topologies and fabrics of multi- and many-core architectures
- Power consumption of interconnects
- Interconnect reliability
- Design-for-manufacturing (DFM) and yield techniques for interconnects
- High speed chip-to-chip interconnect design
- Design and analysis of chip-package interfaces
- 3D interconnect design and prediction
- Applications of interconnects to social, genetic, and biological systems
- Co-optimization of interconnect technology and chip design
- Emerging interconnect technologies in machine learning platforms & chips

<http://www.sliponline.org/>

THE 15TH INTERNATIONAL CONFERENCE ON EMBEDDED SOFTWARE AND SYSTEMS (ICESS)

Date: Sunday, June 2 || Time: 9:00am - 5:00pm || Room: N247

Event Type: Colocated Conference || Keywords: System Security, IoT, Emerging Technologies || Topic Area: Embedded Systems & Software (ESS)

ORGANIZER:

Qi Zhu - Northeastern Univ., Evanston, IL

The advancement of embedded software and systems, such as intelligent vehicles, industrial robots, wearable devices, and Internet-of-Things, has great societal and economic impacts. It is of utmost importance to ensure the safety, efficiency, and security of their design and implementation.

The IEEE International Conference on Embedded Software and Systems (ICESS) is a global forum for researchers and developers from academia, industry, and government to present and discuss emerging ideas and trends in embedded software and systems. The conference has a broad scope covering the design, implementation, optimization, and validation of embedded software and systems in various domains, with recent focus on cyber-physical systems, Internet-of-Things, embedded security, and autonomous software systems.

The ICESS 2019 is the next event of a series of highly successful international conferences on embedded software and systems, held in recent years as ICESS 2017 (Sydney, Australia), ICESS 2016 (Sichuan, China), ICESS 2015 (New York, USA), ICESS 2014 (Paris, France), ICESS 2013 (Sydney, Australia), ICESS 2012 (Liverpool, UK), ICESS 2011 (Changsha, China), ICESS 2010 (Bradford, UK), and ICESS 2009 (Hangzhou, China).

Accepted papers from the conference will be published by the IEEE Computer Society in the IEEE Proceedings. Selected papers, after further revisions, will be considered for publication in the Elsevier Journal of Software Architecture.

ADDITIONAL MEETINGS

DESIGN AUTOMATION SUMMER SCHOOL

Date: Sunday, June 2 | **Time:** 7:30am - 6:00pm | **Room:** N250 | **Event Type:** Additional Meeting | **Keywords:** Architecture & System Design | **Topic Area:** EDA

The Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2019 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC. All the students

receiving the fellowship (excluding the mentors) are required to attend DASS event.

For additional details go to: <http://www.sigda.org/dass>

Thank you to our Corporate Sponsor:



A. RICHARD NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Date: Sunday, June 2 | **Time:** 7:30 - 9:00am | **Room:** N250
Event Type: Additional Meeting | **Topic Area:** EDA

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation

Sunday, June 2
7:30 - 9:00am
Room: N250

Dr. Tom Williams Talk

Monday, June 3
3:00 - 4:00pm
Room: N249

Thank you to our DAC Sponsor:



Poster Presentation (colocated with the Ph.D. Forum)

Tuesday, June 4
7:00 - 9:00pm
Room: N246

Thank you to our Corporate Sponsor:



Closing Session and Award Ceremony

Thursday, June 6
6:00 - 6:45pm
Room: N259

Thank you to our Corporate Sponsor:

HACK@DAC FINAL COMPETITION

Date: Sunday, June 2 | **Time:** 8:00am - 5:00pm | **Room:** N256
Event Type: Additional Meeting | **Keywords:** Architecture & System Design, ContestTopic Area: Security, Design

System-on-a-Chip (SoC) designers use third-party intellectual property (3PIP) cores and in-house IP cores to design SoCs. Trustworthiness of SoCs can be undermined by security bugs that are unintentionally introduced during the integration of the IPs. A security weakness, if discovered and exploited when the chips are in the field, can result in a compromise or bypass of one or more product security objectives. For example, an exploited security bug may lead to a deadlock or failure of the system, or create a backdoor through which an attacker can gain remote access to leak secrets from the system. The goal of this competition is to develop tools and methods for identifying security vulnerabilities in buggy SoCs.

In this 33-hour ordeal, the top scoring teams from phase I of the competition will compete live to find and report security bugs from an SoC that is released to them at the start of the day. These teams mimic the role of a security research team at the SoC integrator, as try to find the security vulnerabilities and report them back to the design team quickly, so they can be addressed before the SoC goes to market. The bug submissions from the participating teams are scored in real time by an expert team from industry and academia.

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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ADDITIONAL MEETINGS

ACM SIGDA/IEEE CEDA EARLY CAREER WORKSHOP AT DAC

Date: Sunday, June 2 || Time: 8:30am - 6:00pm || Room: N254

Event Type: Additional Meeting || Topic Area: Design, EDA

This workshop is for young and mid-career faculty and professionals in the fields related to electronic design automation (EDA). The workshop will start in the morning with an interactive session borrowing techniques from IMPROV to help you improve your soft skills (interpersonal, communication etc.) with others. This is followed by presentations and panel discussions by professionals discussing diverse topics such as navigating the various challenges to better succeed and thrive in your academic or industry job, getting your projects funded and climbing academic and technical ladders, as well as improved cooperation between industry and academia research and development. In addition, the workshop will provide rich opportunities to closely interact and network with some of the established academicians, professionals, and funding officers in EDA related fields.

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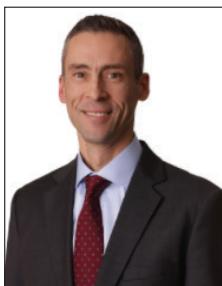
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EDA OBSERVATIONS AND OUTLOOK: A WALL STREET PERSPECTIVE

Date: Sunday, June 2 || Time: 5:30 - 6:00pm || Room: Westgate Hotel - Ballroom B

Event Type: Additional Meeting



Richard F. Valera - Managing Director, Equity Research Needham & Company, New York, NY

This talk will explore the design software industry from the perspective of a Wall St. analyst.

Topics covered will include industry consolidation, growth rates, vertical market drivers, investment and public company stock performance.

CADENCE LUNCHEON PANEL: CLOSING ANALOG AND MIXED-SIGNAL VERIFICATION IN 5G, HPC, AND AUTOMOTIVE

Date: Monday, June 3 || Time: 11:30am - 1:00pm || Room: Westgate Hotel - Paradise South || Event Type: Additional Meeting || Keywords: Analog & Mixed Signal Topic Area: EDA, Autonomous Systems

With 5G, high-performance computing, automotive, and other complex designs using images sensors, RFIC transceivers, and advanced nodes, verification across verticals poses the latest frontier of challenges looking for solutions. It is difficult to know when you are done with your electrical verification because 100% coverage is an evasive target and an acute

problem for analog and AMS types of designs. Customers are routinely forced to make tradeoffs among time to market, functional coverage, reliability tests, accounting for statistical variance, etc. Come to this luncheon and hear from industry luminaries who will share their solutions and their plans to reach their verification goals.

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

ADDITIONAL MEETINGS

STATIC SIGN OFF BEST PRACTICES FOR RTL DESIGN

Date: Monday, June 3 | Time: 1:30 - 2:30pm | Room: N250
Event Type: Additional Meeting | Topic Area: EDA, Design

Panelists will discuss their static sign off goals, the selected best practices and technologies they use to support those goals, and the results they have achieved in accelerating early functional verification and sign-off of digital designs.

Topics will include: Multimode & dynamic clock domain crossing (CDC) sign off, plus reset domain crossing sign off to eliminate metastability issues. Audience Q&A to follow panel discussion.

PANELISTS:

John Busco - NVIDIA Corp., Santa Clara, CA
Richard Ho - Google, Inc., San Francisco, CA
Seonil Brian Choi - Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea
Oren Katzir - Real Intent, Inc., Sunnyvale, CA

INTEGRATE THE AWS CLOUD WITH RESPONSIVE XILINX MACHINE LEARNING AT THE EDGE

Date: Monday, June 3 | Time: 2:00- 4:00pm | Room: N261 | Event Type: Additional Meeting | Topic Area: IP

ORGANIZERS:

Naveen Purushotham - Xilinx, San Jose, CA
Kv Thanjavur Bhaaskar - Xilinx, San Jose, CA
Hugo A. Andrade, Xilinx - San Jose, CA

In this meeting, learn in a hands-on workshop how to integrate FPGA based low-latency edge machine learning with an IIoT enabled distributed control application that leverages the massive scale of AWS Cloud analytics, Xilinx Edge AI based machine learning model deployment, application provisioning, and system dashboards. Based on a distributed

industrial control scenario, you will work through a hands-on integration of AWS Cloud services through AWS Greengrass on Zynq Ultrascale+ and Amazon FreeRTOS on Xilinx Zynq-7000 platforms. After this meeting, you will have a concrete understanding of how a distributed industrial control system makes use of AWS edge and cloud services plus how they enable the evolutionary approach to these types of long-lived systems towards an edge-to-cloud collaboration exemplified through the integration of machine learning applications at the industrial edge.

IEEE CEDA/ACM SIGDA ADVANCING DIVERSITY IN EDA (DivEDA) FORUM

Date: Monday, June 3 | Time: 2:00 - 6:00pm | Room: N259
Event Type: Additional Meeting | Topic Area: EDA

ORGANIZERS:

Chengmo Yang - Univ. of Delaware, Newark, DE
Ayse Coskun - Boston Univ., Boston, MA

The goal of the Advancing Diversity in EDA (DivEDA) event is to help facilitate women and underrepresented minorities (URM) to advance their careers in academia and industry, and hence, to help increase diversity in the EDA community. Through an interactive medium, our aim is to provide practical tips to women and URM on how to succeed and overcome

possible hurdles in their career growth, while at the same time, connecting senior and junior researchers to enable a growing diverse community, which will then help accelerate innovation in the EDA ecosystem and benefit societal progress.

For additional information and to view the agenda

Thank you to our DAC Sponsors:



Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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ADDITIONAL MEETINGS

DR. T.W. WILLIAMS TALK: ANOTHER INCONVENIENT TRUTH: SNAILS ARE MORE INTELLIGENT THAN US

Date: Monday, June 3 | Time: 3:00 - 4:00pm | Room: N249

Event Type: Additional Meeting | Topic Area: EDA, Design

In this talk, Dr. Williams will describe the problems with scaling and a number of possible solutions, including the latest alternative paths and their relative merits.

COOLEY'S DAC TROUBLEMAKER PANEL

Date: Monday, June 3 | Time: 3:00 - 4:00pm | Room: N250

Event Type: Additional Meeting | Topic Area: EDA, Design

MODERATOR:

John Cooley - Deepchip, Holliston, MA

Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

CELUG: ASSOCIATION OF HIGH PERFORMANCE COMPUTING PROFESSIONALS

Date: Tuesday, June 4 | Time: 8:00am - 5:00pm | Room: N249

Event Type: Additional Meeting | Topic Area: EDA, IP Technologies, Interconnects, Low Power & Reliability | Topic Areas: Design, IoT

ORGANIZERS:

Derek Magill - The Association of High Performance Computing Professionals, Austin, TX

Bob Van deer Kloot - Teradyne, Inc., North Reading, MA

EDA Licensing providers, ISVs, and Enterprise Customers will come together at an event colocated with the 55th ACM/EDAC/IEEE Design Automation Conference (DAC), June 24 - 28, 2018, at the Moscone Center in San Francisco, CA. CELUG (Centralized Enterprise Licensing Users

Group), the Association of High Performance Computing Professionals and the ESD Alliance are hosting this one-day event colocated at DAC 2018. This interactive event will focus on Enterprise Licensing roadmaps and private presentations, with presentations and panels addressing current and future challenges to making high technology tools and users more productive. This colocated event will bring Licensing Solution Providers and Independent Software Vendors together with Enterprise Customers from key industries for interactive, face-to-face meetings.

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

ADDITIONAL MEETINGS

CADENCE LUNCHEON PANEL: MACHINE LEARNING AND THE IMPACT ON THE DIGITAL DESIGN ENGINEER

Date: Tuesday, June 4 | **Time:** 11:30am - 1:00pm | **Room:** Westgate Hotel - Paradise South | **Event Type:** Additional Meeting | **Keywords:** Analog & Mixed Signal, Emerging Technologies | **Topic Area:** EDA, Machine Learning/AI

Much has been written, presented and debated about ML and its potential impact on the future. Yet there is no debating that ML technology is already shipping now inside production silicon that spans virtually every tech market segment. Today's design engineer is at the forefront of this revolution and during this panel you will have an opportunity to hear from

engineers who are paving the next-generation chip design path about the lessons they've learned implementing these new classes of architectures and how our digital design, implementation, and signoff tools are evolving in lockstep using machine learning techniques to continue delivering optimal silicon.

CEDA DISTINGUISHED SPEAKER LUNCHEON: SIMULATION TECHNOLOGIES FOR IMAGE SYSTEMS ENGINEERING

Date: Tuesday, June 4 | **Time:** 12:00 - 1:30pm | **Room:** N246
Event Type: Additional Meeting | **Keywords:** Verification/Validation, Architecture & System Design, Implementation, Emerging Technologies | **Topic Area:** EDA



The use of imaging systems has grown enormously over the last several decades; these systems are an essential component in mobile communication, medicine, and automotive applications. As part of this growth the complexity of imaging systems hardware, from optics to electronics, has increased dramatically, making software prototyping an essential tool for the design and evaluation of systems and components. I will describe several examples for image systems engineering

applications. This is a good moment to consider how academia and industry might combine to create an image systems simulation infrastructure that speeds the development of new systems for the many opportunities that will arise over the next few decades.

Biography: Brian A. Wandell is the first Isaac and Madeline Stein Family Professor at Stanford University. He joined the Psychology faculty in 1979 and is a member, by courtesy, of Electrical Engineering, and Ophthalmology. He is Director of the Center for Cognitive and Neurobiological Imaging, and Deputy Director of the Wu Tsai Neuroscience Institute. Wandell's research uses magnetic resonance imaging and software simulations for basic and applied research spanning human visual perception, brain development, and image systems simulations.

SPEAKER:

Prof. Brian A. Wandell - Stanford University, Stanford, CA.

SAMSUNG HBM ENABLING GUIDELINE

Date: Tuesday, June 4 | **Time:** 1:00 - 3:00pm | **Room:** Westgate Hotel - Ballroom F
Event Type: Additional Meeting | **Keywords:** Architecture & System Design, Test/Manufacturing/Reliability/Safety | **Topic Area:** Design, Machine Learning/AI

HBM is implemented as a part of SiP and it is new biz model in Samsung perspective because so far Samsung has discrete component and module pro biz. Samsung HBM has various application customer (HPC, AI, Network, Graphics) and more than 3 years HBM manufacturing experience. Based on this experience, Samsung found that HBM should be

consider from ASIC design. So, Samsung would like to share what is the key factors to implement HBM in SiP for whole process through design, verification, test.

Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

ADDITIONAL MEETINGS

ACM SIGDA AND IEEE CEDA PH.D. FORUM

Date: Tuesday, June 4 | Time: 7:00 - 9:00pm | Room: N246

Event Type: Additional Meeting | Topic Area: EDA

ORGANIZERS:

Helen Li - Duke Univ., Durham, NC
Umit Ogras - Arizona State Univ., Tempe, AZ
Rasit Topaloglu - IBM Corp., Hopewell, NY
Yiyu Shi - Univ. of Notre Dame, Notre Dame, IN

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community. Participation in the forum is highly competitive with

acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

For more information, please visit the ACM SIGDA Ph.D. Forum website.

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CADENCE LUNCHEON PANEL: OPTIMIZING VERIFICATION THROUGHPUT FOR ADVANCED DESIGNS IN A CONNECTED WORLD

Date: Wednesday, June 5 | Time: 11:30am - 1:00pm | Room: Westgate Hotel - Paradise South | Event Type: Additional Meeting | Keywords: Architecture & System Design, Low Power, Test/Manufacturing/Reliability/Safety | Topic Area: EDA

Verification throughput has become the key challenge for today's and next-generation advanced SoCs to be successful in a connected world. Users must run as many cycles as possible in return for their tool and man-power investment, employing smart verification practices to correct as many bugs as early as possible per dollar and day. This

panel will discuss these challenges in the context of advanced 5G, AI/ML, ADAS, mobile, and server designs and introduce state-of-the-art, efficient techniques to increase and scale bare performance of dynamic verification engines, explore how to connect different levels of abstraction, and introduce smart bug hunting techniques.

A. RICHARD NEWTON YOUNG FELLOW CLOSING SESSION

Date: Thursday, June 6 | Time: 6:00 - 6:45pm | Room: N259
Event Type: Additional Meeting

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Keynotes	SKY Talks	Research Sessions	Designer/IP Track Sessions	Panels	DAC Pavilion	Monday Tutorials
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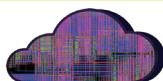
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DESIGN INFRASTRUCTURE ALLEY



DESIGN-ON-CLOUD THEATER SCHEDULE - Booth 1137

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Monday

Time	Presentation
10:00 - 10:45am	HPC Pros -- State of the Future
11:00 - 11:45am	Microsoft: Accelerating Silicon Design with Cloud and AI/ML
1:00 - 1:45pm	Cadence Design Systems, Inc: The 4 Questions to Ask When Creating a Cloud Strategy
2:00 - 2:45pm	Methodics, Inc.: Design Workflow Acceleration with Frictionless Cloud-bursting
3:00 - 3:45pm	Rescale: Cloud, what's Chip Design got to do with it? The Why, What, How, and What's Next of EDA on the Cloud
4:00 - 4:45pm	Google
5:00 - 6:00pm	Design Infrastructure Alley Reception

Tuesday

Time	Presentation
10:00 - 10:45am	Invited Session: Practical Cloud Advice from those that have already Adopted it
11:00 - 11:45am	Univa Corp: Taking EDA Clusters to the Extreme with HPC Cloud
1:00 - 1:45pm	ClioSoft, Inc.: Successfully Moving a Design Environment to the Cloud
2:00 - 2:45pm	IBM Corporation: Empowering the EDA Designer
3:00 - 3:45pm	Amazon Web Services: Cloud Best-practices for Semiconductor Design and Verification
4:00 - 4:45pm	Altair: Cloud for Cloud Pragmatists
5:00 - 5:45pm	Pure Storage, Inc.: Speed up Chip Design for Free (Almost)

Wednesday

Time	Presentation
10:00 - 10:45am	Google
11:00 - 11:45am	Si2 - Panel: OpenAccess DM6: A New Era Enabling Interoperable Cloud Design
1:00 - 1:45pm	Astera Labs: Revolutionizing Semiconductor Design Workflows with EDA on AWS
2:00 - 2:45pm	Invited Session: Doing EDA in the Cloud? Yes, it's possible!
3:00 - 3:45pm	Metrics Technology, Inc.: Verification Measurement and Optimization

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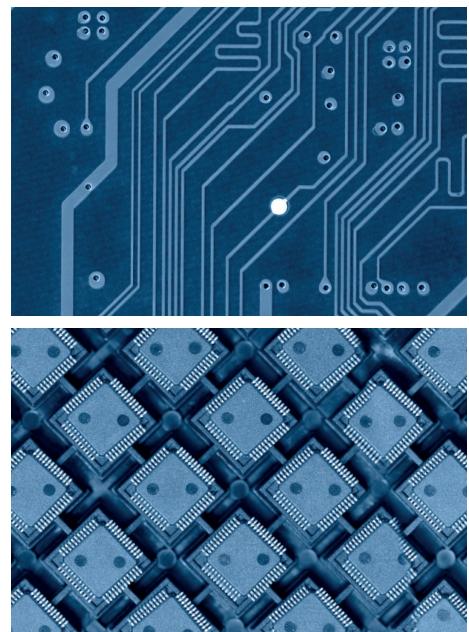


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Peggy Aycinena
Peggy Aycinena is a freelance journalist and Editor of EDA Confidential at www.aycinena.com. She can be reached at peggy at aycinena dot com.

Let's be honest about this. The reason the Electronic Design Process Symposium takes place eve in Monterey is because of the surf and sunshine. Otherwise, this conference would be so much appropriately located in Silicon Valley.

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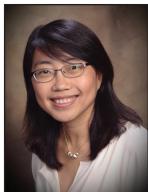
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