FINAL EXAMINATION REPORT
POWER ELECTRONICS
(TKE215204)

Compiled by :

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Lecturer :

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FAKULTAS TEKNIK UNIVERSITAS GADJAH MADA
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Task 1

Assigned to design a buck converter for step-down voltage conversion.

1. Key specifications of the buck converter
   - Input voltage (V_{in}) = 16V
   - Desired output voltage (V_{out}) = 8V
   - Switching frequency (f_{sw}) = 100kHz
   - Switching period (T_{sw}) = 10µs
   - Output power (P_{out}) = 20W
   - Output current (I_L) = 2.5A
   - Permissible inductor current ripple (ΔI_L) = 20% (0.5A)
   - Permissible output voltage ripple (ΔV_{out}) = 1% (0.08V)
   - Load (R) $= \frac{Vout^2}{Pout} = \frac{8^2}{20} = 3.2\Omega$
2. Suitable values for the inductor (L) and capacitor (C) to meet the design specifications
   - Duty Cycle

$$D = \frac{Vout}{Vin} = \frac{8}{16} = 0.5$$

   - Inductor calculation

$$L = \frac{Vout\,(1-D)}{\Delta I_L \cdot f_{sw}}$$

$$L = \frac{8\,(1-0.5)}{0.5 \cdot 100000}$$

$$L = \frac{4}{50000} = 80\mu H$$

   - Capacitor calculation

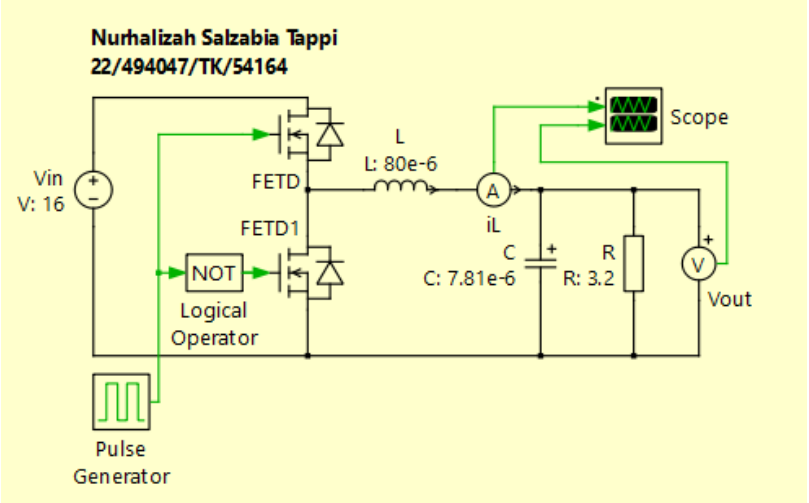
$$\Delta V_{out} = \frac{Vout\,(1-D)}{8LCfsw^2}$$

$$C = \frac{Vout\,(1-D)}{(8Lfsw^2)\Delta Vout}$$

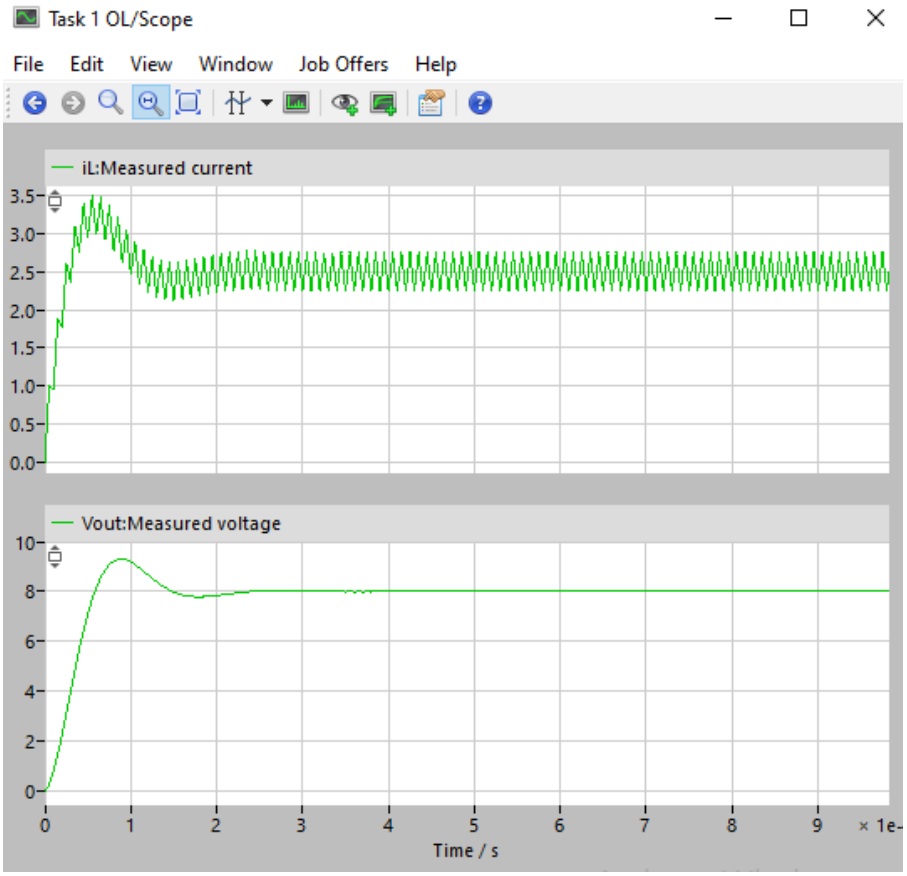
$$C = \frac{8\,(1-0.5)}{8 \cdot 80 \cdot 10^{-6} \cdot 100000^{2} \cdot 0.08}$$

$$C = \frac{4}{512000} = 7.81\mu F$$

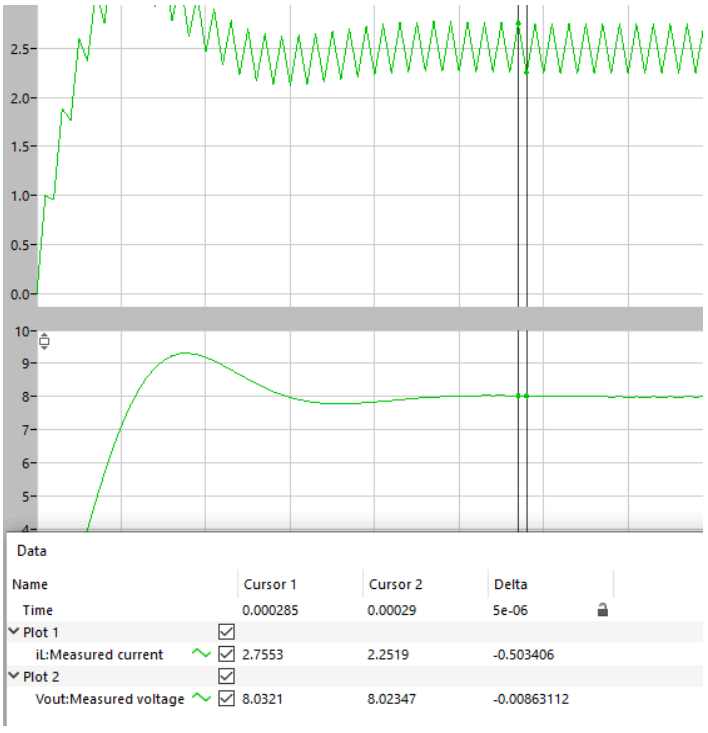
3. The open-loop operation of the buck converter without feedback control
   - Buck Converter Design



• Simulation



The open-loop buck converter simulation behaves as expected. With an input voltage of 16 V and an estimated duty cycle of 50%, the output voltage settles at approximately 8 V, which aligns well with theoretical calculations. The inductor current operates in Continuous Conduction Mode (CCM), reaching steady-state around 2.5 A with a typical ripple waveform. It shows a smooth transition after the initial inrush, indicating stable system dynamics.

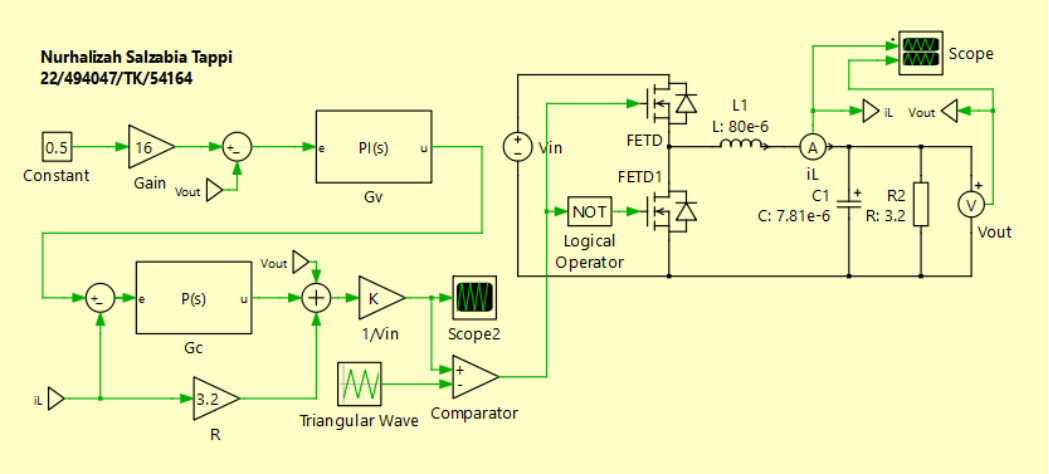


According to the design criteria, the permissible inductor current ripple is 20% of the average inductor current, which equals 0.5 A. From the simulation, the actual ripple remains within this limit, confirming that the inductor value is appropriate. Similarly, the permissible output voltage ripple is set to 1% of the output voltage, or 0.08 V. The observed voltage ripple in the simulation is small and remains below this threshold, demonstrating that the capacitor value is also well-chosen.

This confirms that the selected inductor and capacitor values are effective in suppressing ripple and maintaining stable operation, satisfying both performance and design constraints.

4. Cascaded control system for voltage regulation of the buck converter

• Complete block diagram of the control architecture.



• Calculations or tuning procedures for determining the control gains (e.g., Kp and Ki).

Outer Loop (Voltage Control)

$fbp = fsw/20 = 100000/20 = 5000Hz$

$fbi = fbp/10 = 5000/10 = 500Hz$

$Kp = 2\pi \cdot fbp \cdot C = 2\pi \cdot 5000 \cdot 7.81\times10^{-6} = 0.2453$

$Ki = 2\pi \cdot fbi \cdot Kp = 2\pi \cdot 500 \cdot 0.2453 = 770.47$

Inner Loop (Current Control)

$fbp = fsw/200 = 100000/200 = 500Hz$

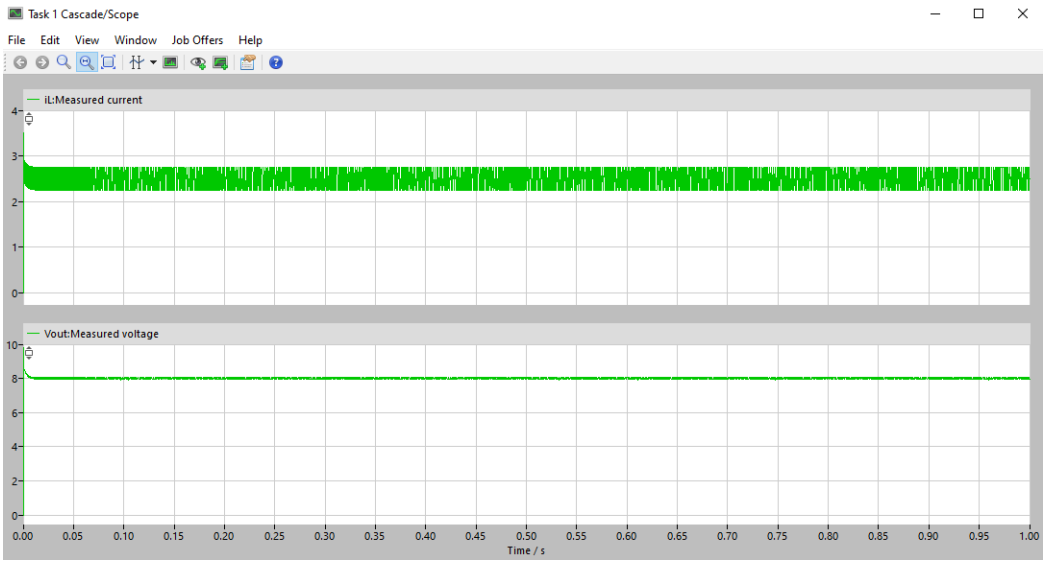
$fbi = fbp/10 = 500/10 = 50Hz$

$Kp = 2\pi \cdot fbp \cdot L = 2\pi \cdot 500 \cdot 80\times10^{-6} = 0.2513$

$Ki = 2\pi \cdot fbi \cdot Kp = 2\pi \cdot 50 \cdot 0.2513 = 78.98$

The gain values calculated using standard frequency-based formulas served as a good starting point. However, practical tuning based on simulation results was necessary to account for non-idealities and improve the performance of the closed-loop control system.

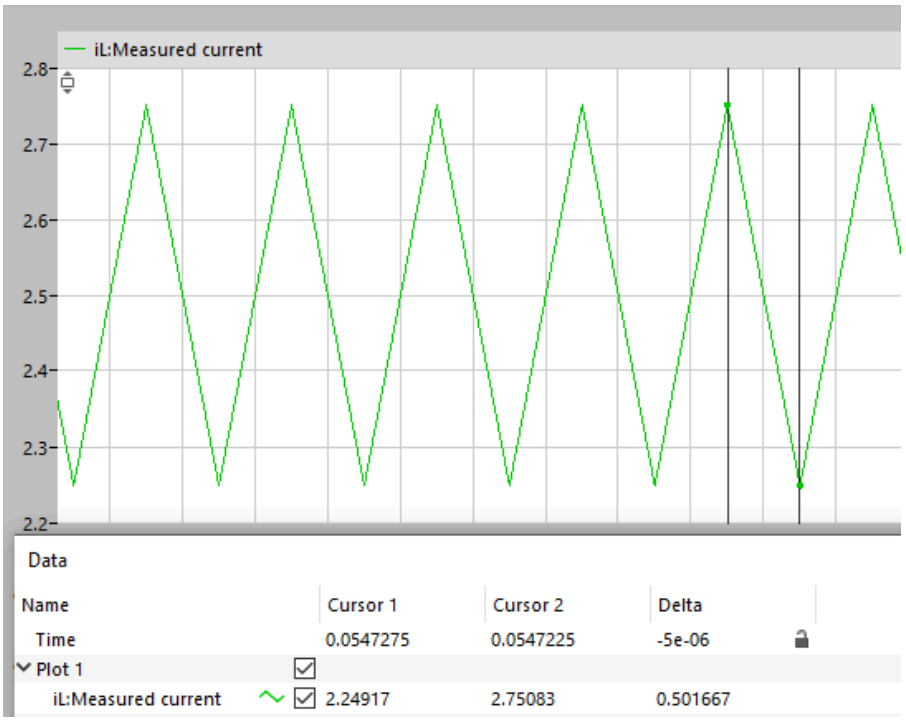
The final gain values that were used in the controller were those shown in the previous configuration screenshots, where the inner (current) loop used Kp = 0.2513 × 12 and the outer (voltage) loop used Kp = 0.2513 × 1 and Ki = 78.98 × 1. These tuned values provided better voltage regulation, a faster transient response, and minimal overshoot under various test conditions, ensuring stability and accuracy of the buck converter system.



The simulation of the closed-loop buck converter using a cascaded control system shows that the output voltage is well-regulated and stable. The control architecture consists of two loops: an outer voltage loop and an inner current loop, each implemented using a PI controller. The voltage controller adjusts the current reference based on the voltage error, while the current controller ensures that the actual inductor current closely follows this reference.

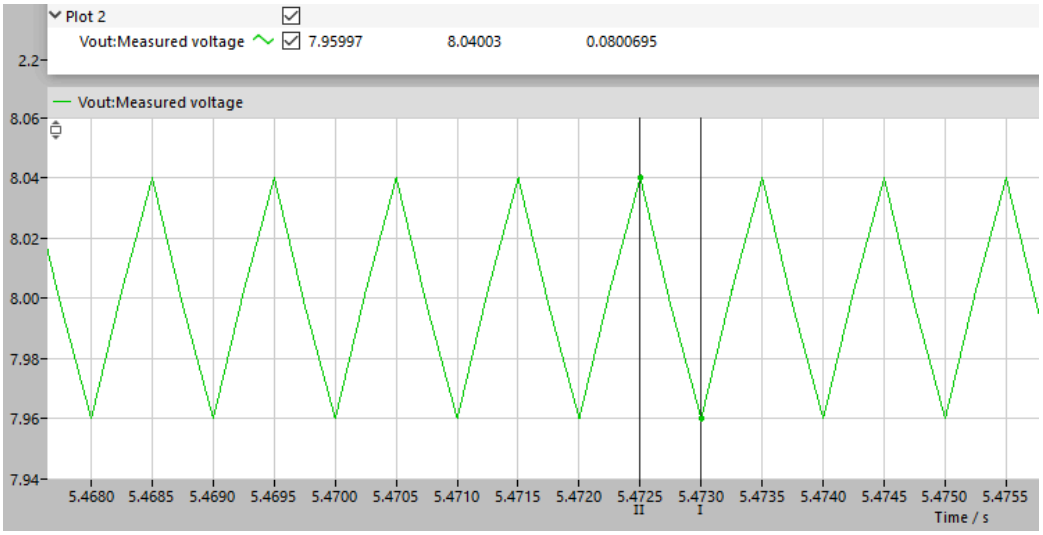
From the simulation, it can be observed that the output voltage maintains a constant level with minimal ripple, and the inductor current remains stable without any significant overshoot or oscillation. This indicates that the system is operating in Continuous Conduction Mode (CCM) and that the control gains (Kp and Ki) have been properly tuned. Overall, the cascaded control system successfully improves voltage regulation, suppresses ripple, and enhances the dynamic response of the buck converter, fulfilling the intended design objectives.

5. Plot the inductor current waveform and verify that the ripple meets your design criteria.



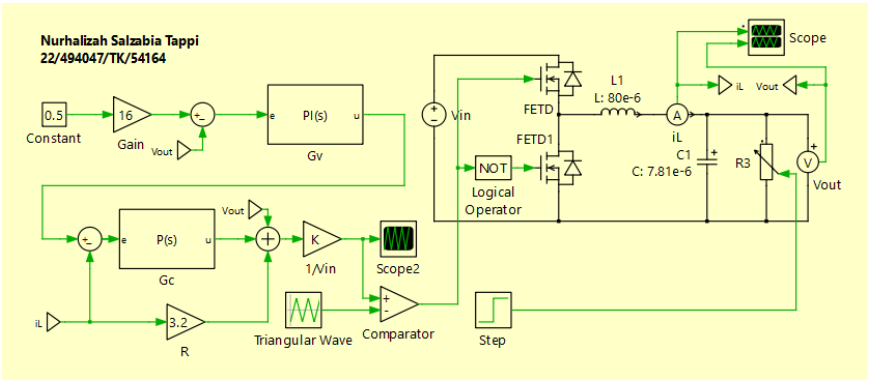
The inductor current varies between approximately 2.249 A and 2.750 A, resulting in a peak-to-peak ripple of 0.501 A. This corresponds to exactly 20% of the average current, which meets the specified ripple allowance of 20% (0.5 A). Therefore, the inductor selection is verified to be appropriate for maintaining current stability.

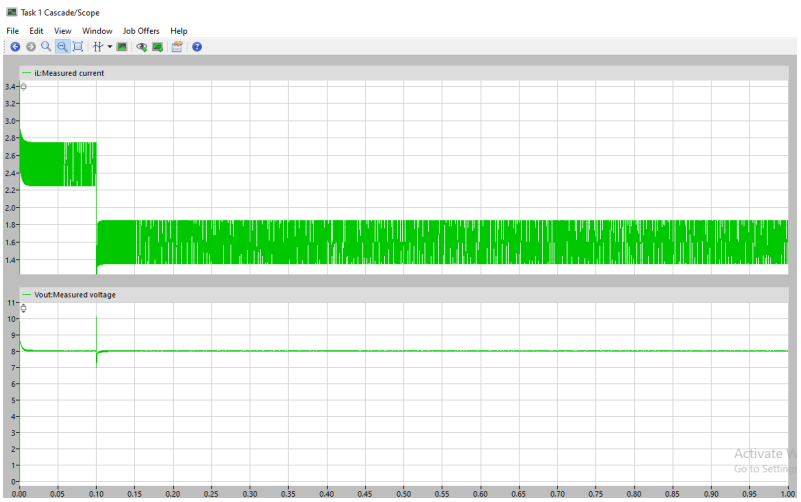
6. Plot the output voltage waveform and verify that the ripple is within the allowable range.



The output voltage waveform shows a variation between 7.960 V and 8.040 V, producing a ripple of approximately 0.080 V. This matches the allowable output voltage ripple of 1% of 8 V (0.08 V), as specified in the design. The capacitor used in the circuit effectively suppresses voltage fluctuations, ensuring a clean and stable output.

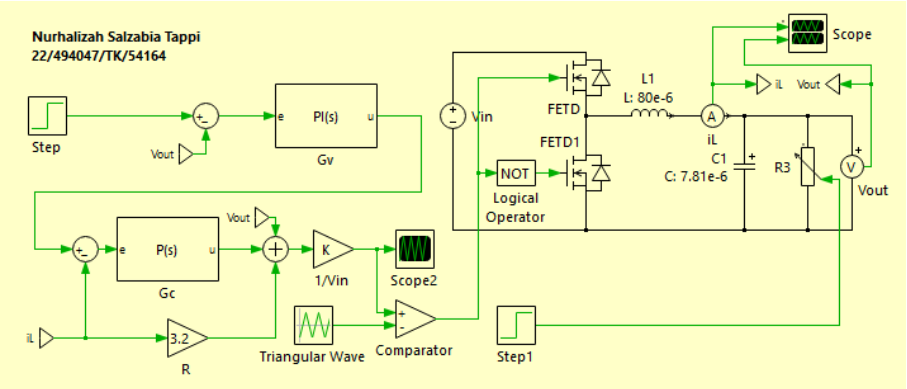
7. Simulate a sudden load change and analyze the converter's dynamic response. Demonstrate how the controller maintains stability and restores regulation.

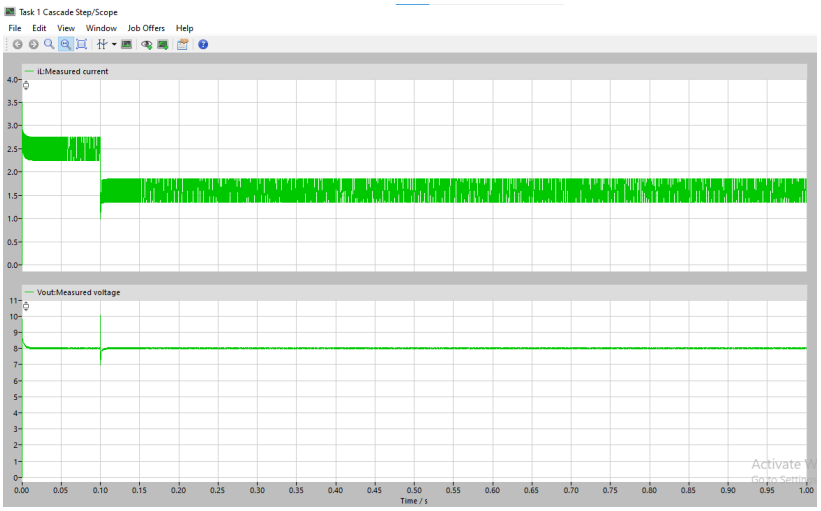




The system is designed to observe the dynamic response of a buck converter under a sudden load change, while maintaining a constant voltage reference. The voltage reference is provided by a constant block, meaning the desired output voltage does not change during the simulation. However, a step block is used to trigger a change in the load condition. For example, by switching from one load resistance to another. This change causes a sudden increase or decrease in the output current demand. When this occurs, the output voltage initially deviates from the desired setpoint due to the disturbance. However, the controller uses a PI (Proportional-Integral) control strategy, quickly detects the error and adjusts the PWM duty cycle to restore the voltage to its target value. From the simulation waveform, we can see that the current increases after the load change, while the voltage undergoes a brief transient before stabilizing again. This demonstrates that the controller is effective in maintaining regulation and ensuring system stability even when the load varies abruptly.

8. Simulate the system response to a step change in the voltage reference. Show how effectively the controller tracks the new reference value





A step block is connected to the voltage reference input, meaning that the desired output voltage changes at a specific time during the simulation. This simulates a scenario where the user or system changes the voltage setpoint. For example, increasing the desired output from 8 V to a higher value. The controller must now adjust the duty cycle of the PWM signal in real time to achieve and maintain the new target voltage. The waveform shows a step response in the output voltage, with a smooth transition and minimal overshoot, followed by stabilization at the new voltage level. This indicates that the PI controller performs well in tracking the new reference with good dynamic characteristics, fast response time, low overshoot, and stable steady-state operation. It proves the controller's effectiveness in not just regulating voltage under fixed conditions, but also adapting quickly to new demands.

Task 2

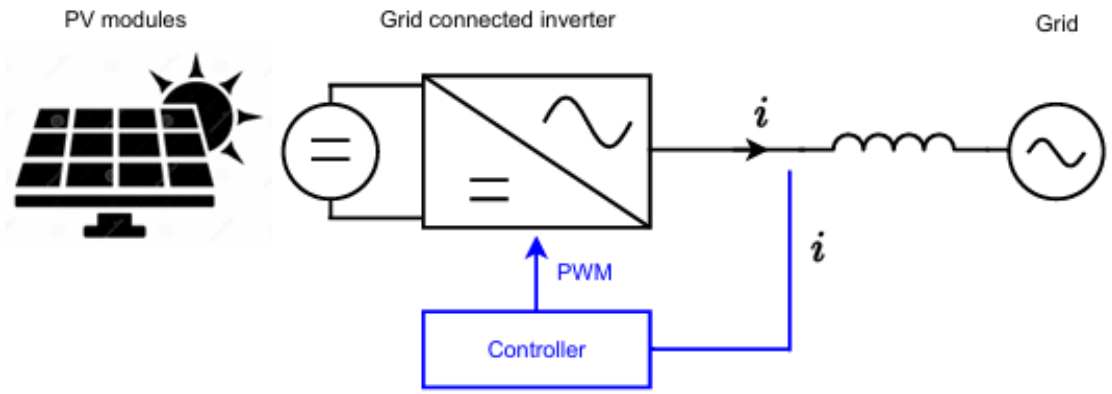


Figure 1: PV grid connected inverter

Assigned to design a PV grid-connected inverter system as illustrated in Figure 1. The task includes determining the inverter and PV module specifications, selecting system components, and designing a control strategy to regulate both active and reactive power injected into the grid.

1. Configuration of the photovoltaic (PV) array. Specify key parameters such as module voltage, current, and how modules are arranged (series/parallel).
   - Target Power = 2.7kW
   - Maximum Power (P_{mp}) /module = 300W
   - Voltage at Max Power (V_{mp}) /module = 38V
   - Open-Circuit Voltage (V_{oc}) /module = 46V
   - Current at Max Power (I_{mp}) /module = 7.89A
   - Modules Arrangement = Series
   - Required Modules = 9
2. The PV module configuration and its rating such as voltage and current.

   $V_{mp} = 9 \cdot 38 = 342V$

   $V_{ov} = 9 \cdot 46 = 414V$

   $I_{mp} = 7.89A$ (series)

   $P_{tot} = 2.7kW$
3. The specifications of the inverter.
   - DC-link voltage

     $Vpeak(ph) = \sqrt{2} \times 220 = 311V$

     $DClink = 1.2 \times Vpeak(ph) \approx 375 - 400V$
   - AC output voltage

     Target = Grid connect, 3 phase system

     Standard in Indonesia regions = 380V – 50Hz

     Phase voltage = $380/\sqrt{3}$ = 220Vrms
   - Power rating

     From PV array (2.7kW), chosen power rating 3kW.

• Semiconductor devices used

IGBT

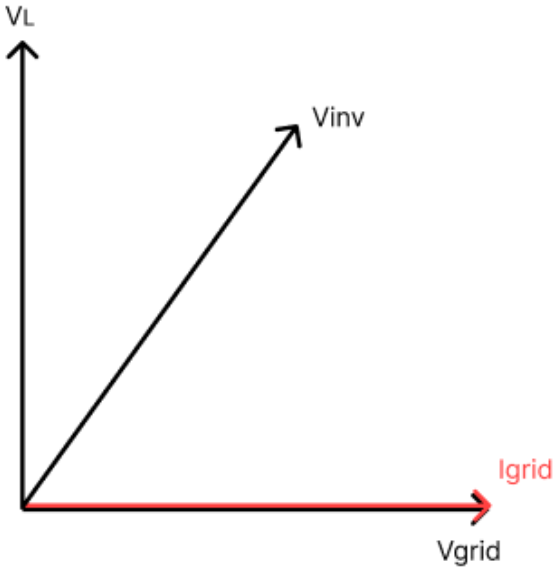
• Modulation strategy Justify your choices with technical reasoning and/or references.

SVPWM (Space Vector PWM)

4. Calculate the value of the inductor (L) connecting the inverter to the grid (three-phase voltage of 380 V. Support your answer with a phasor (vector) analysis diagram showing voltage and current relationships.

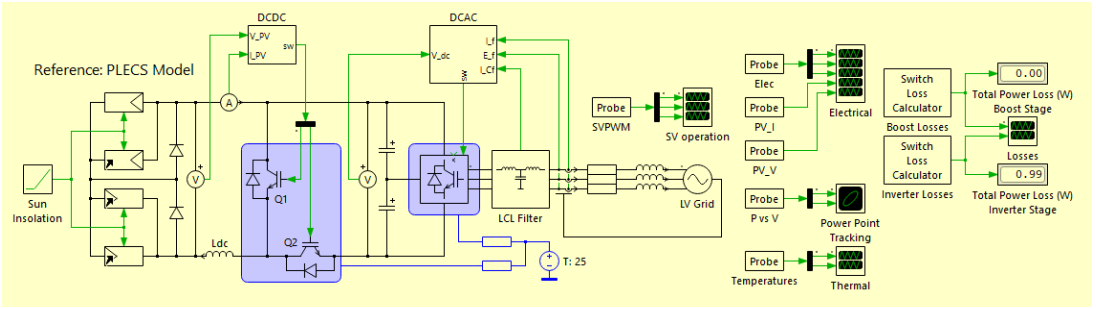
$$V_{ph} = V_{LL}/\sqrt{3} = 380/\sqrt{3} = 219.4Vrms$$

$$L = \frac{\Delta V}{2\pi f I} = \frac{10}{2\pi(50)(7.89)} = 4.03mH$$



5. Design a control system capable of regulating both active and reactive power.

• Present your control design using block diagrams.



• Explain the method used to determine controller gain parameters.

The most common and practical approach is frequency-domain tuning based on system modeling.

$$R = 0.1$$

$$fsw = 10000$$

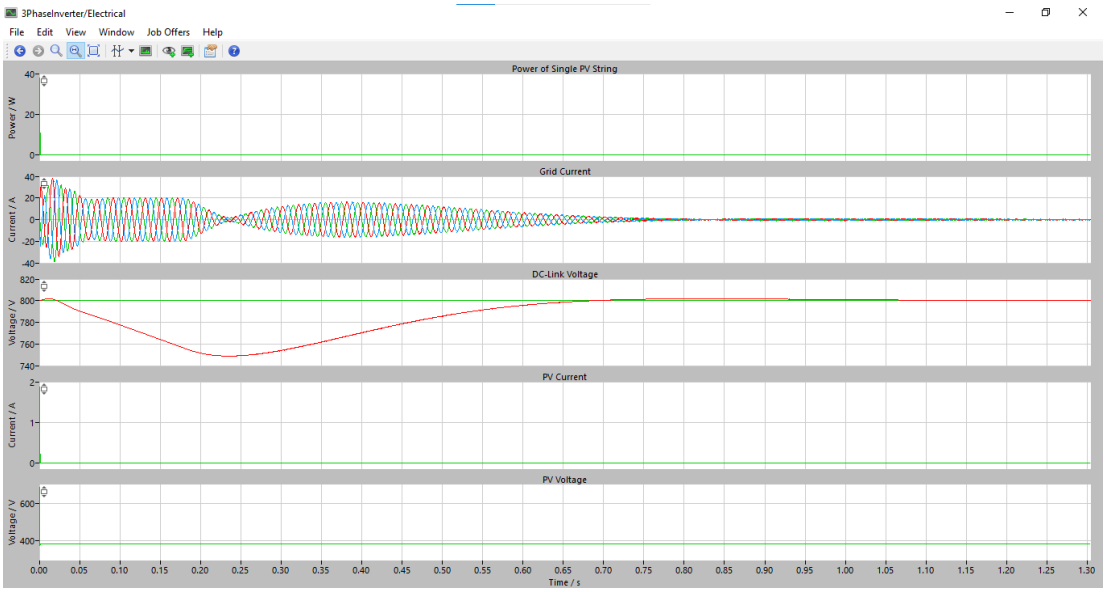
$$\omega_c = fsw(1/10) = 1000rad/s$$

$$T_i = 1/\omega_c = 0.001s$$

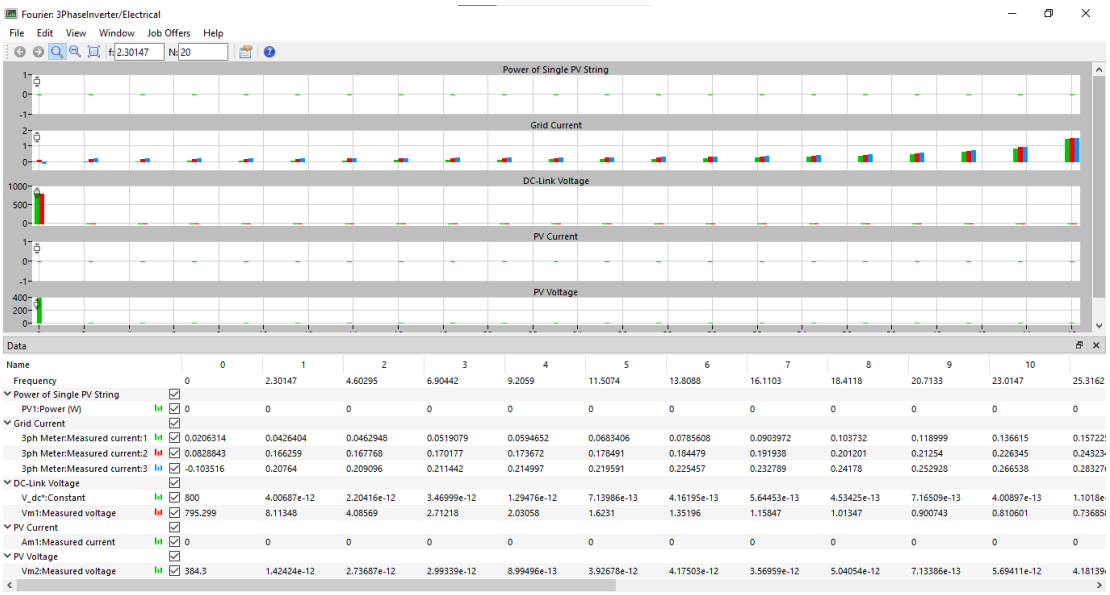
$$K_p = L/Ti = (4.03 \times 10^{-3})/0.001 = 4.03$$

$$K_i = R/Ti = 0.1/0.001 = 100$$

6. Simulate and plot inverter currents in the dq-reference frame.



7. Plot the inverter output voltage (phase and line) in both time domain and frequency domain. Perform FFT analysis on the time-domain waveform to evaluate harmonic content.



Name	0	1	2	3	4	5	6	7	8	9	10
Frequency	0	2.30147	4.60295	6.90442	9.2059	11.5074	13.8088	16.1103	18.4118	20.7133	23.0147
Power of Single PV String											
PV1:Power (W)	0	0	0	0	0	0	0	0	0	0	0
Grid Current											
3ph Meter:Measured current:1	0.0206314	0.0426404	0.0462948	0.0519079	0.0594652	0.0683406	0.0785608	0.0903972	0.103732	0.118999	0.136615
3ph Meter:Measured current:2	0.0828843	0.166259	0.167768	0.170177	0.173672	0.178491	0.184479	0.191938	0.201201	0.21254	0.226345
3ph Meter:Measured current:3	-0.103516	0.20764	0.209096	0.211442	0.214997	0.219591	0.225457	0.232789	0.24178	0.252928	0.266538
DC-Link Voltage											
V_dc*:Constant	800	4.00687e-12	2.20416e-12	3.46999e-12	1.29476e-12	7.13986e-13	4.16195e-13	5.64453e-13	4.53425e-13	7.16509e-13	4.00897e-13
Vm1:Measured voltage	795.299	8.11348	4.08569	2.71218	2.03058	1.6231	1.35196	1.15847	1.01347	0.900743	0.810601
PV Current											
Am1:Measured current	0	0	0	0	0	0	0	0	0	0	0
PV Voltage											
Vm2:Measured voltage	384.3	1.42424e-12	2.73687e-12	2.99339e-12	8.99496e-13	3.92678e-12	4.17503e-12	3.56959e-12	5.04054e-12	7.13386e-13	5.69411e-12

8. Analyze the system behavior under overmodulation conditions.

Overmodulation occurs when the modulation index mam_ama exceeds the linear range of the PWM technique. It is when the amplitude of the reference voltage exceeds the carrier signal in sinusoidal PWM or when the reference vector exceeds the hexagon boundary in SVPWM. In the setup, this condition can be intentionally introduced by increasing the amplitude of the reference voltage signal