

TBR Designs

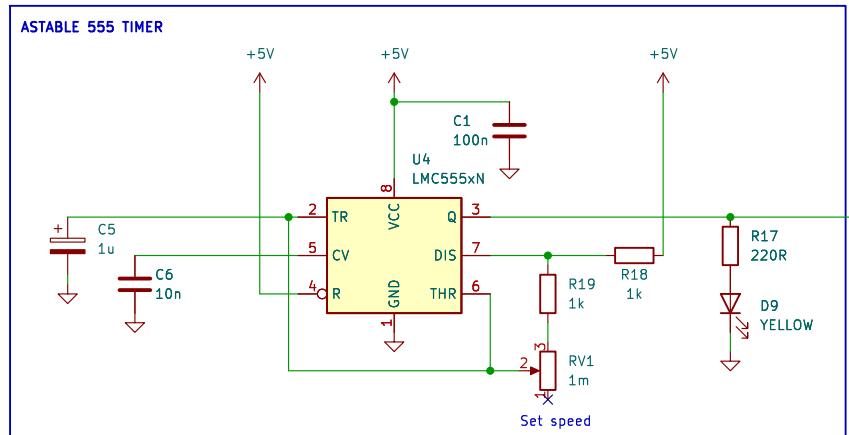
Sheet: /
File: 8-bit-cpu.kicad_sch

Title: 8-bit CPU

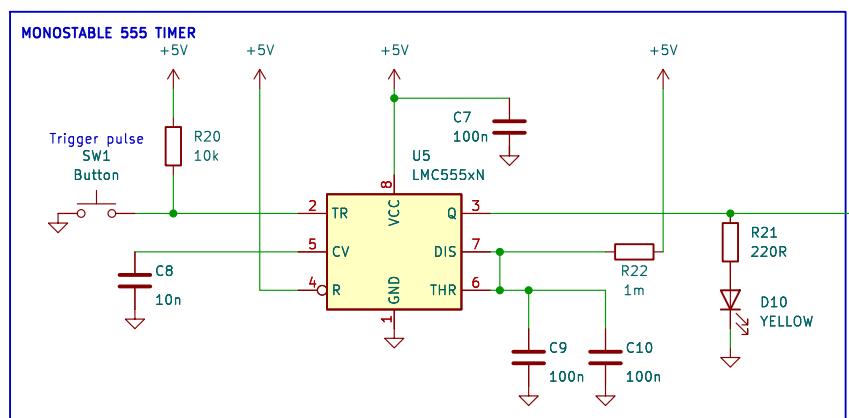
Size: A3 | Date: 2023-11-28
KiCad E.D.A. kicad 7.0.9

Rev: 1.0

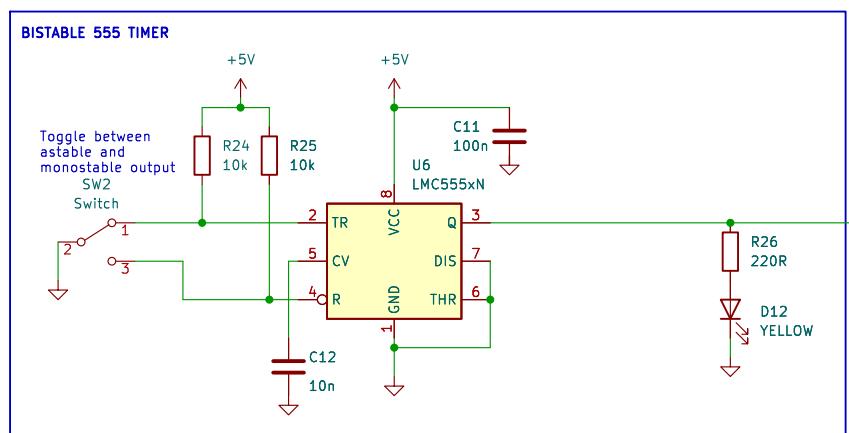
Id: 1/21



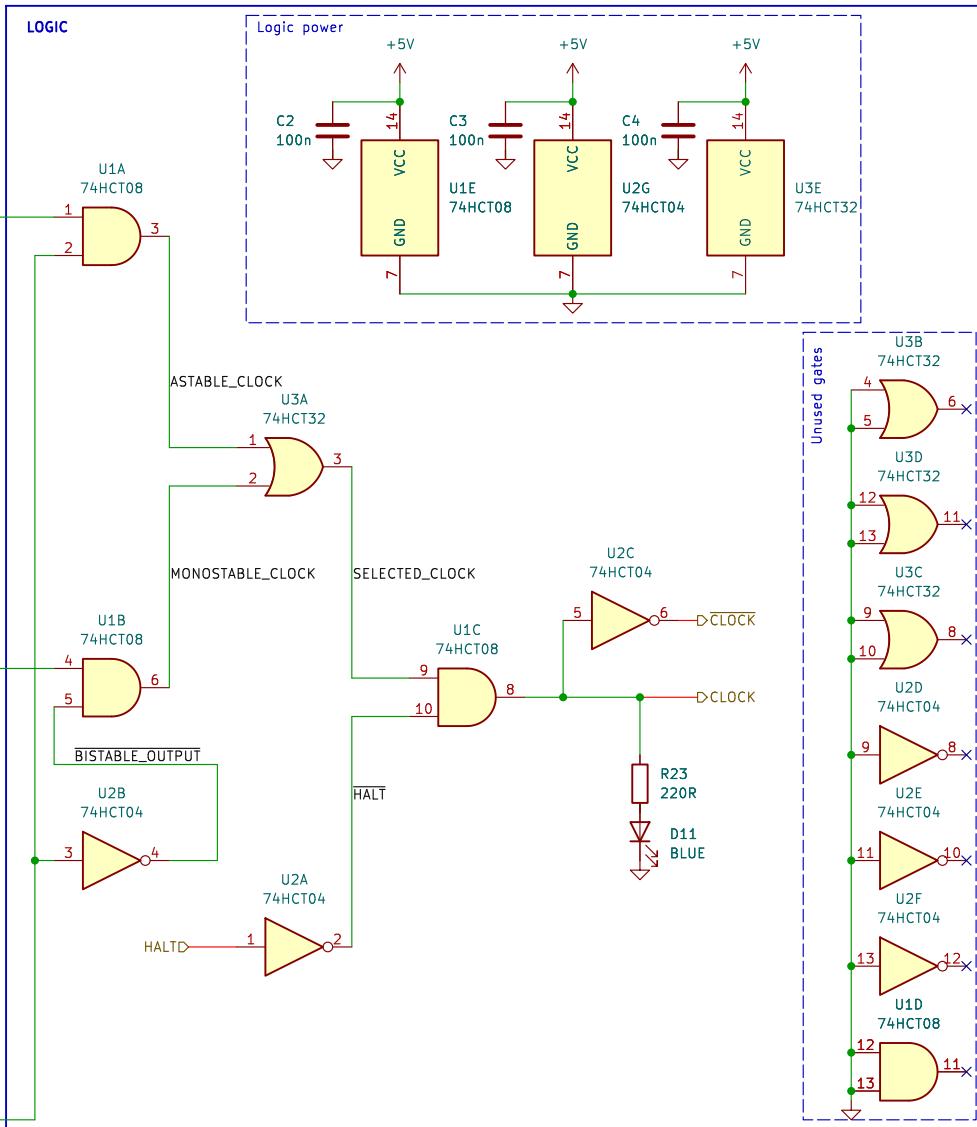
ASTABLE_OUTPUT



MONOSTABLE_OUTPUT



BISTABLE_OUTPUT



Provides a clock pulse and inverted clock pulse.
Speed can be set with the potentiometer.
Manual pulse can be chosen with the switch and pulsed with the button.
If HALT is HIGH no pulse is outputted.

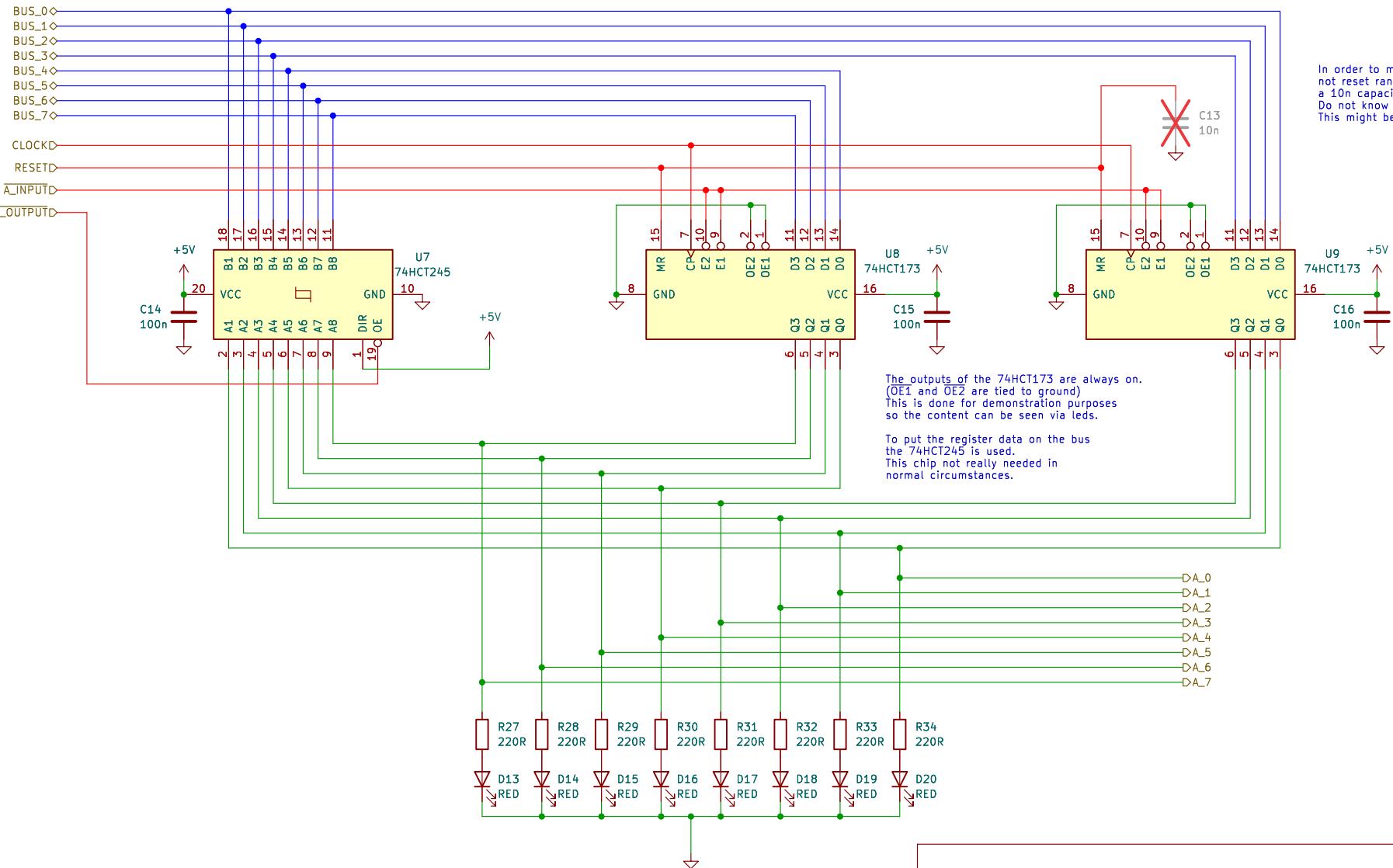
TBR Designs

Sheet: /Clock/
File: clock.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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Rev: 1.0
Id: 2/21



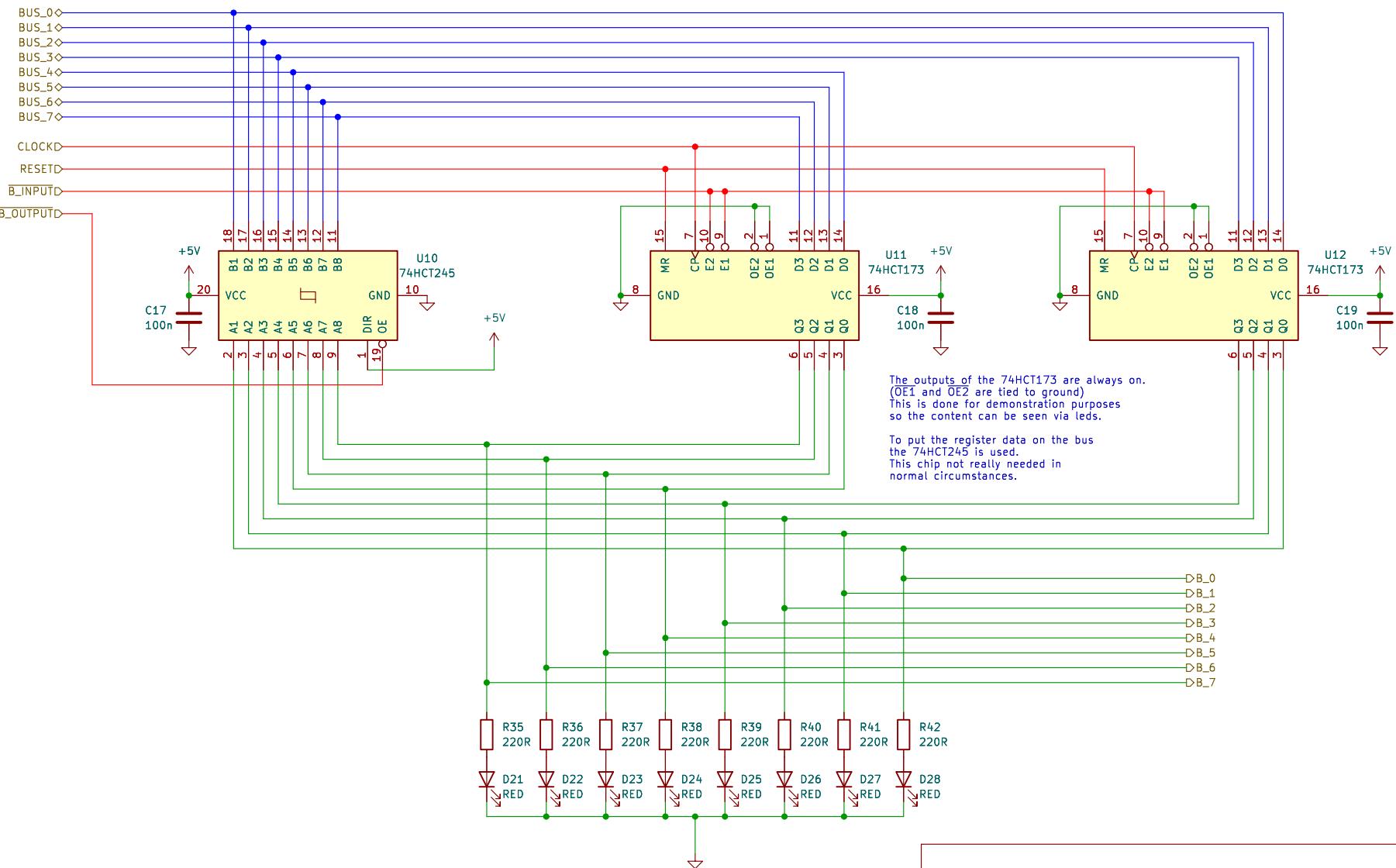
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Sheet: /A register/
File: a-register.kicad_sch

Title: 8-bit CPU

Size: A4 | Date: 2023-11-28
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Rev: 1.0
Id: 3/21



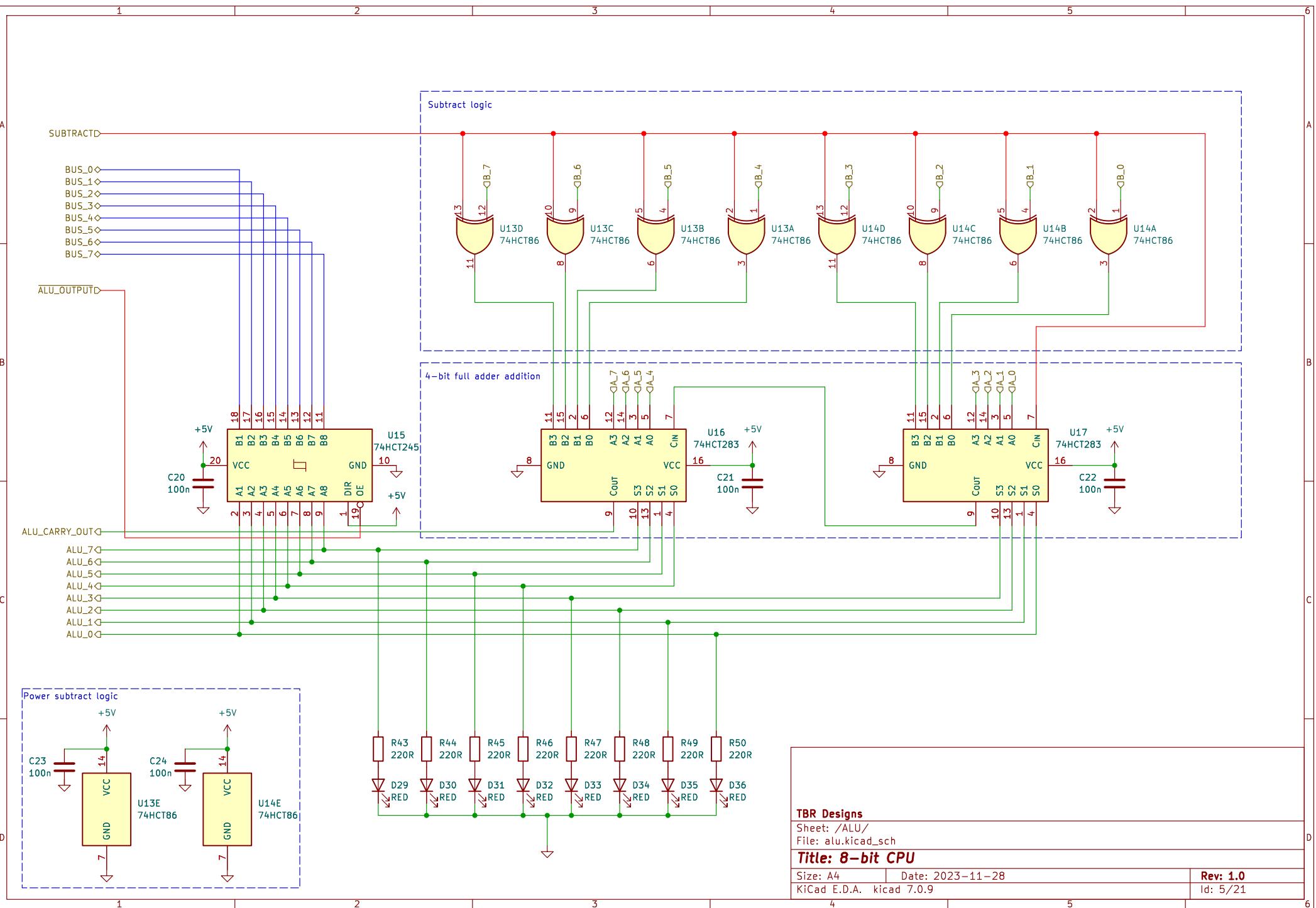
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Sheet: /B register/
File: b-register.kicad_sch

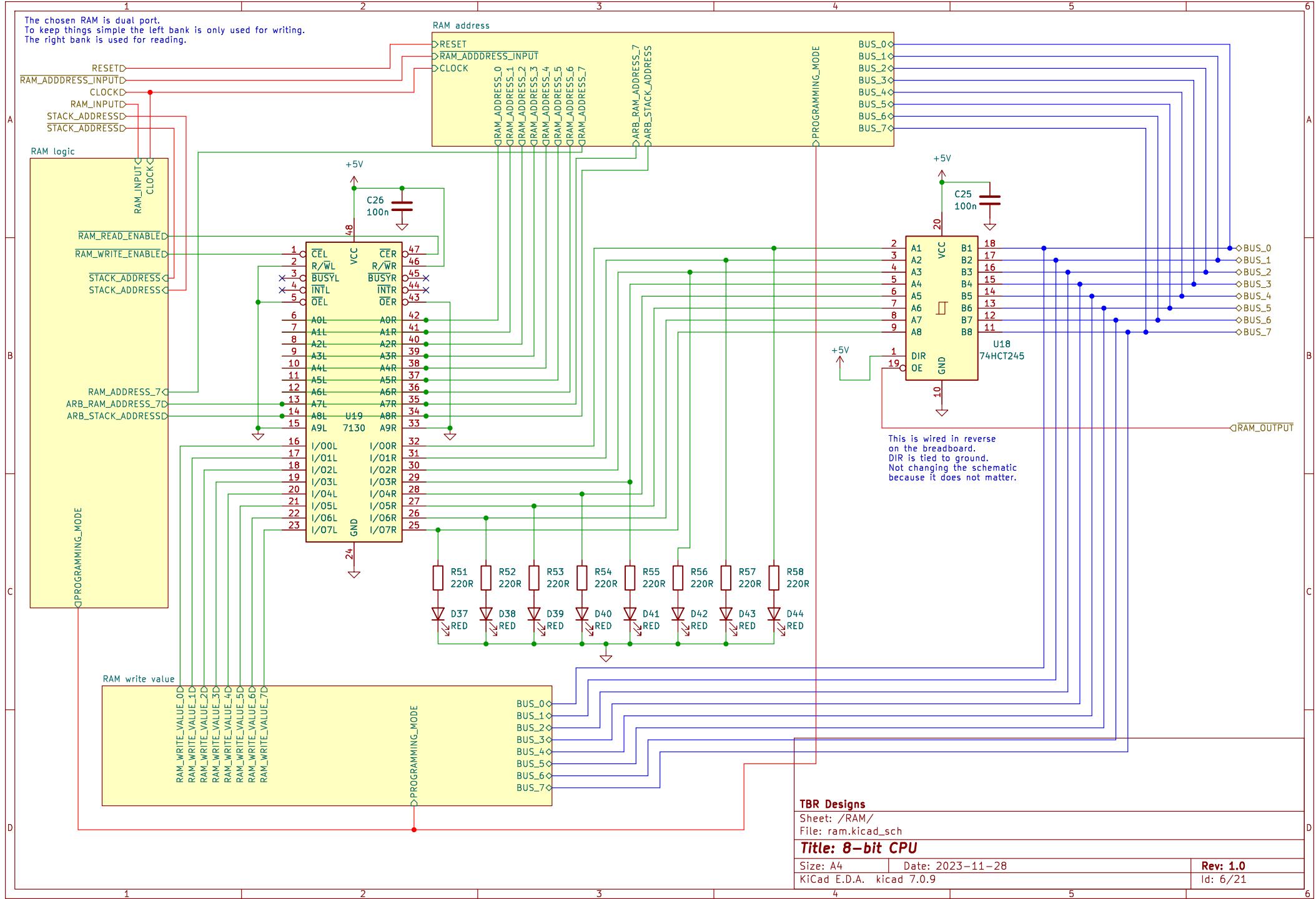
Title: 8-bit CPU

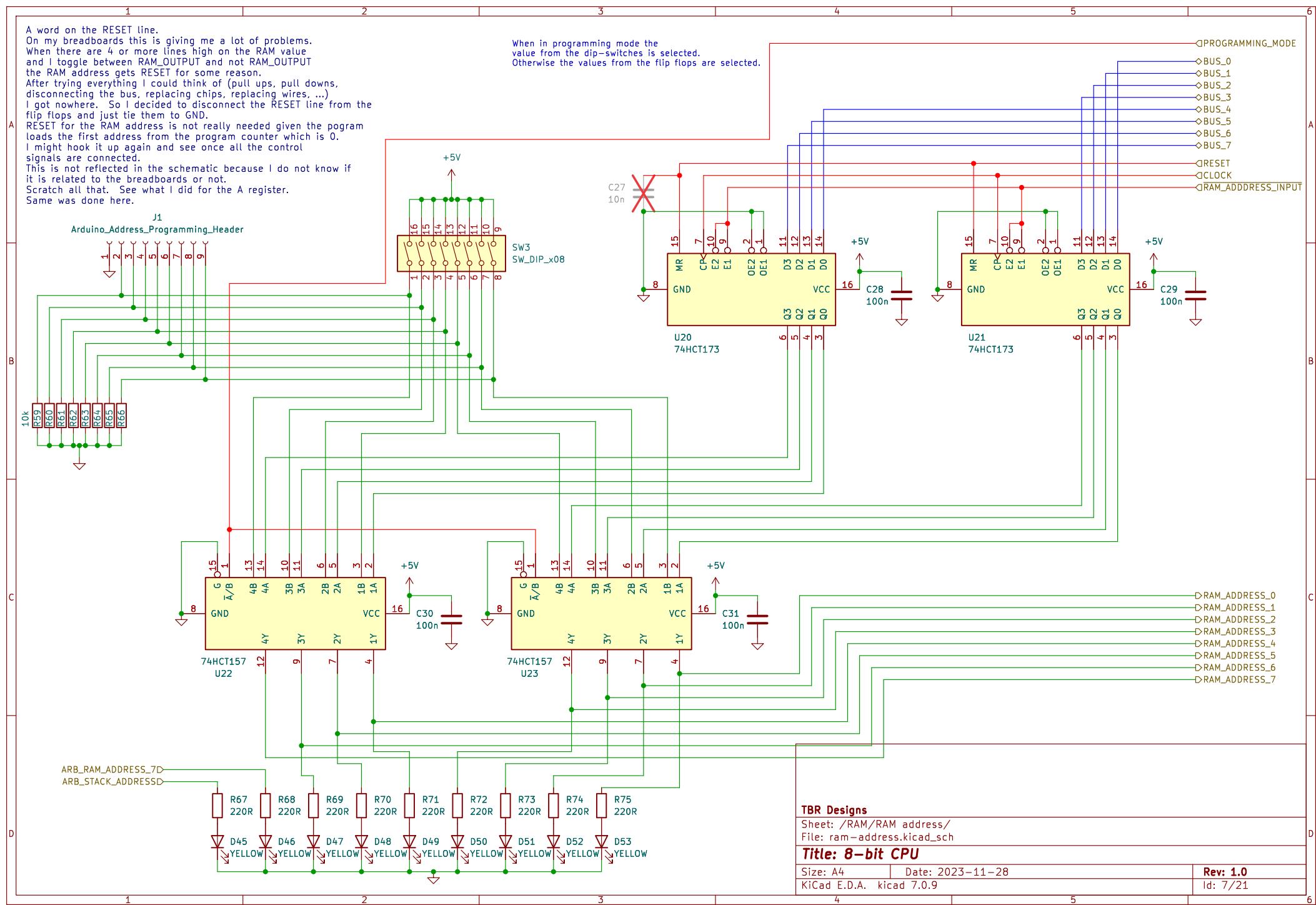
Size: A4 | Date: 2023-11-28
KiCad E.D.A. kicad 7.0.9

Rev: 1.0
Id: 4/21



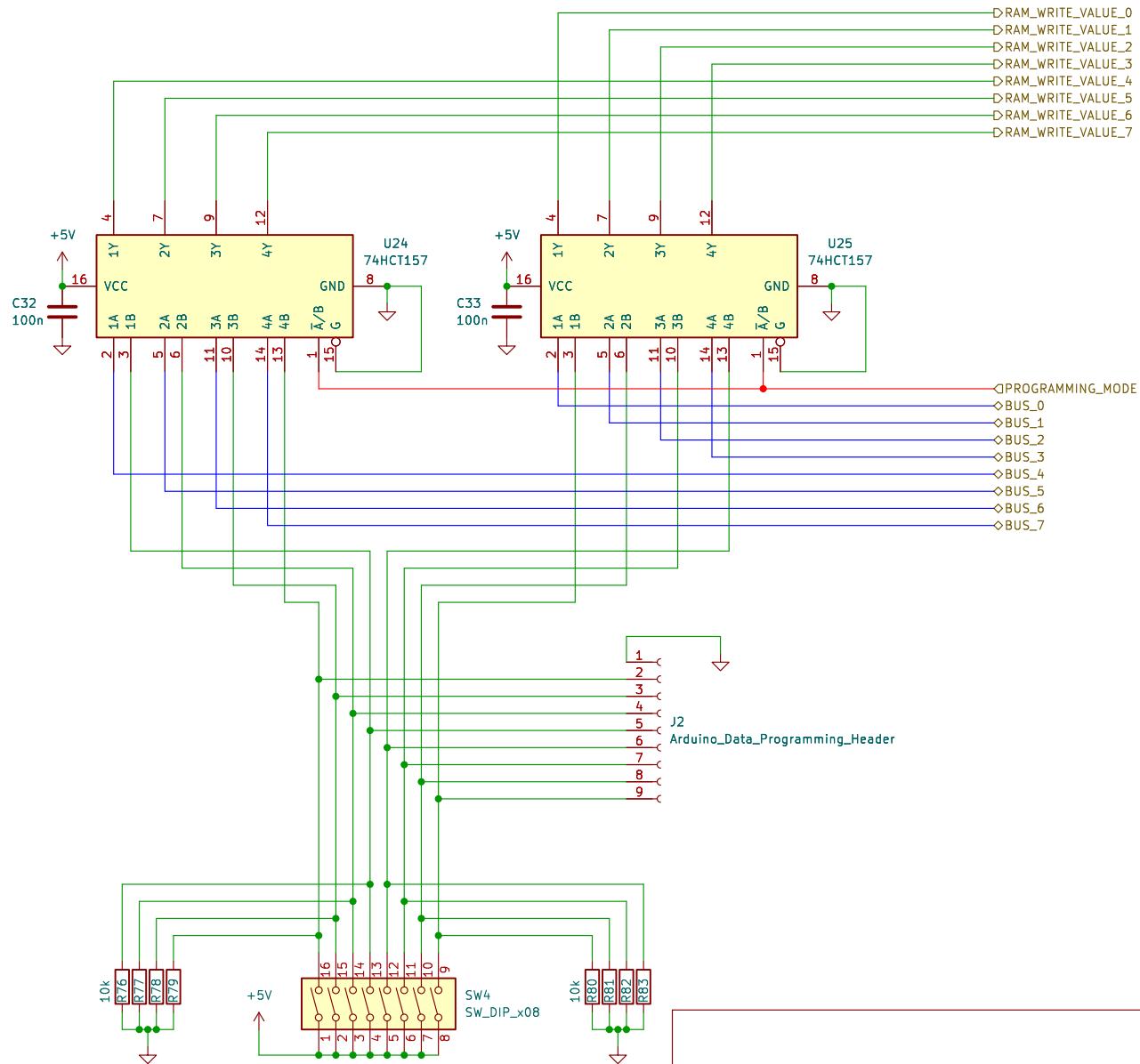
The chosen RAM is dual port.
To keep things simple the left bank is only used for writing.
The right bank is used for reading.





1 2 3 4 5 6

When in programming mode the value from the dip-switches is selected. Otherwise the value from the bus is selected.



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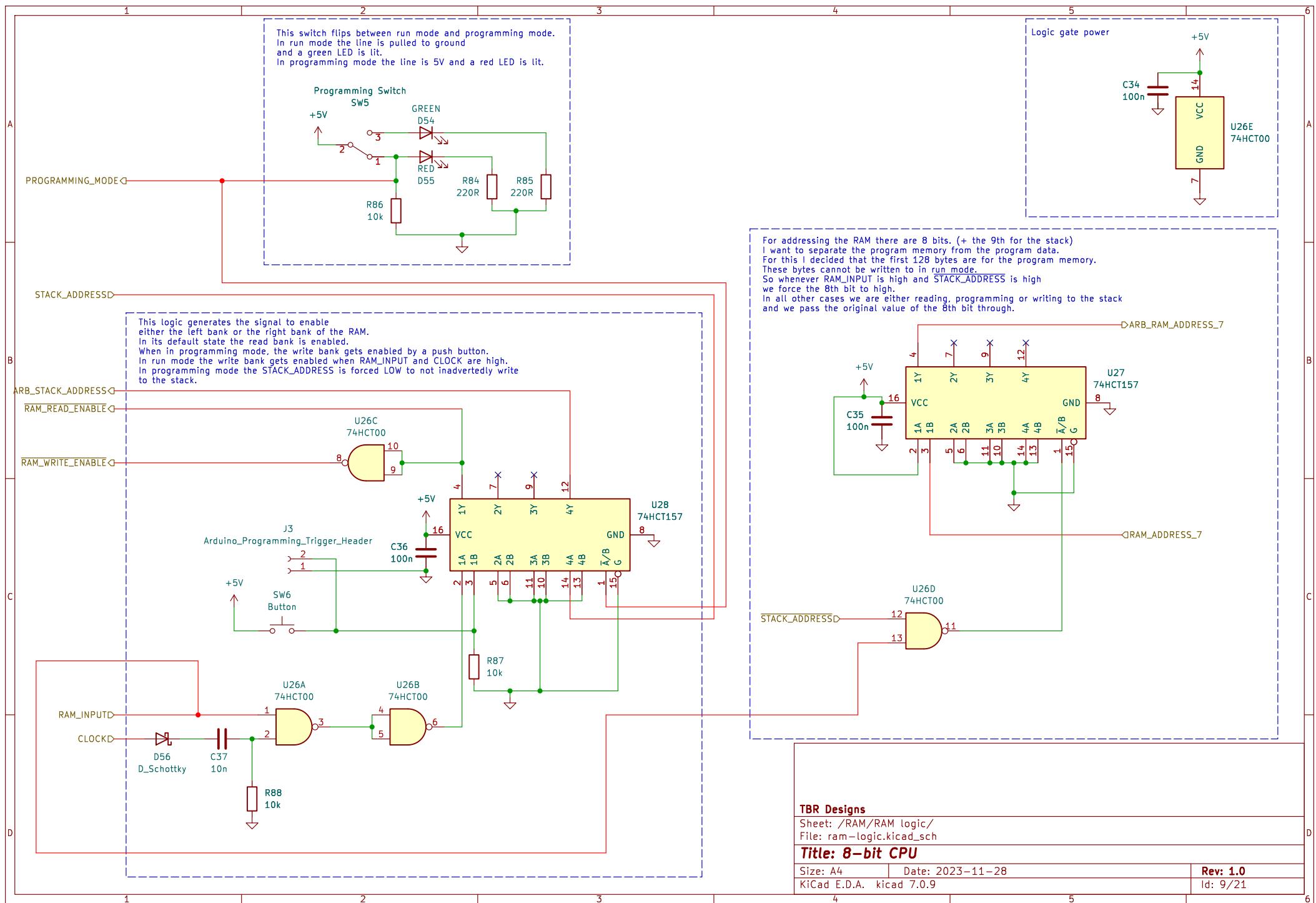
Sheet: /RAM/RAM write value/
File: ram-write-value.kicad_sch

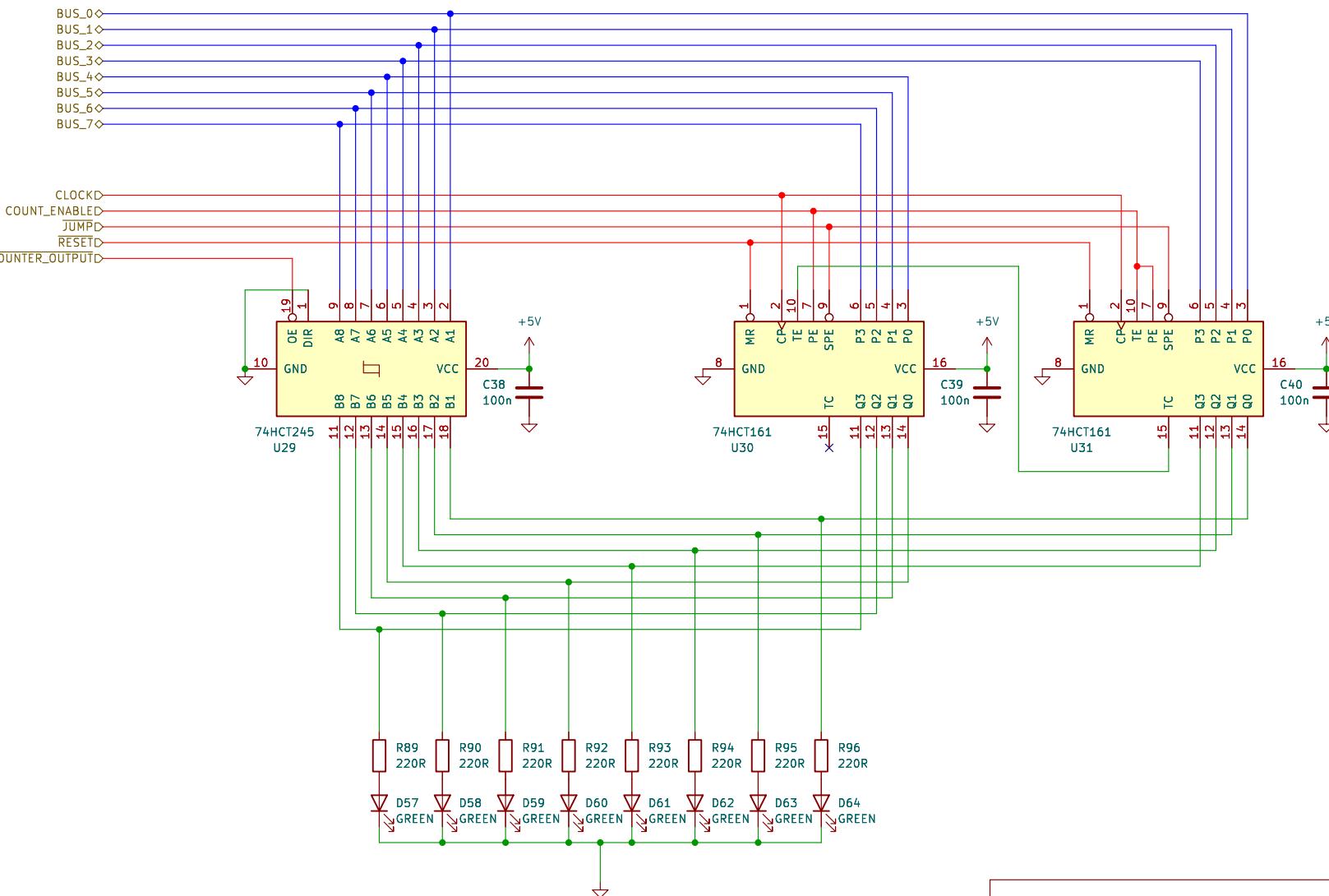
Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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Rev: 1.0
Id: 8/21

1 2 3 4 5 6





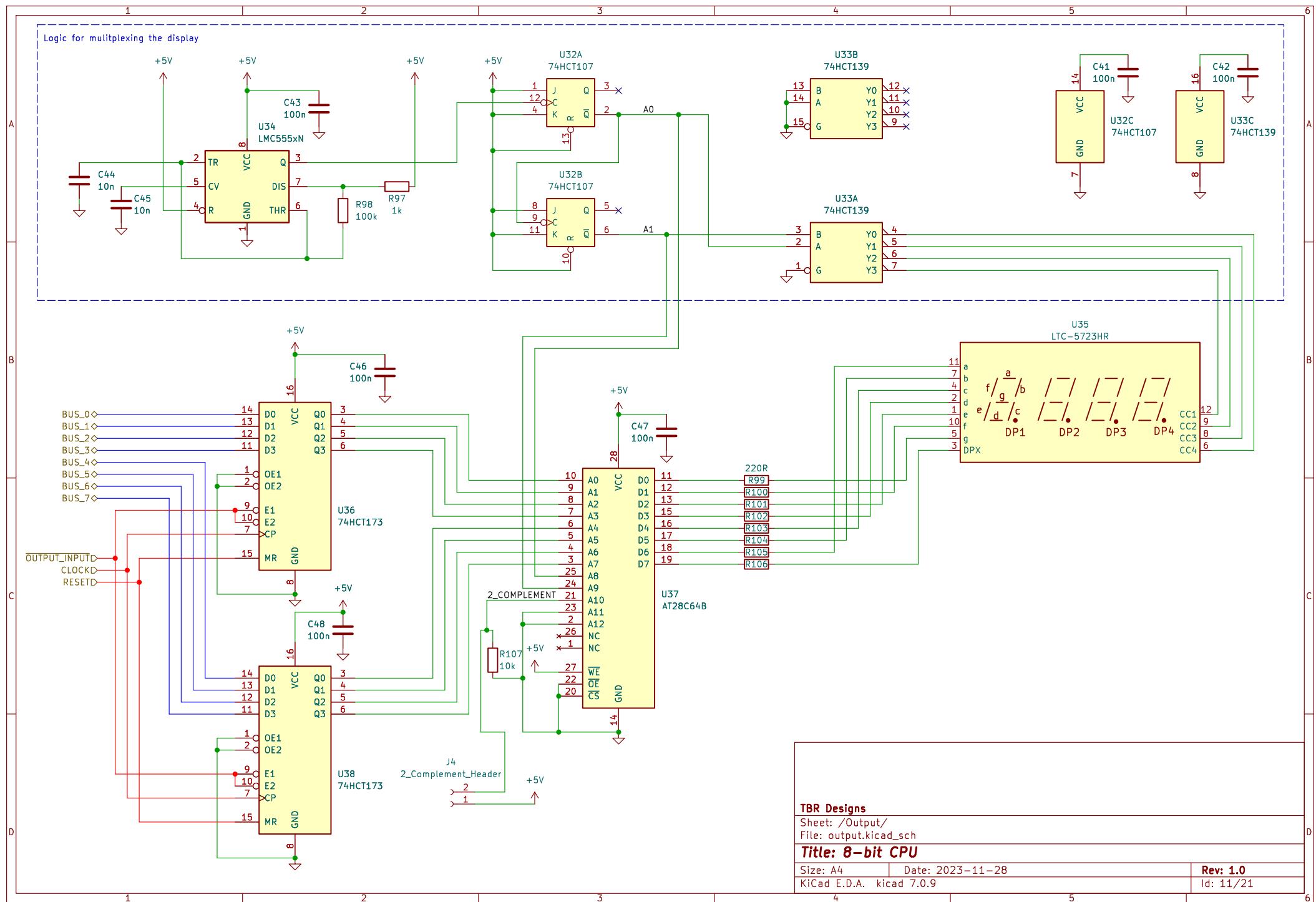
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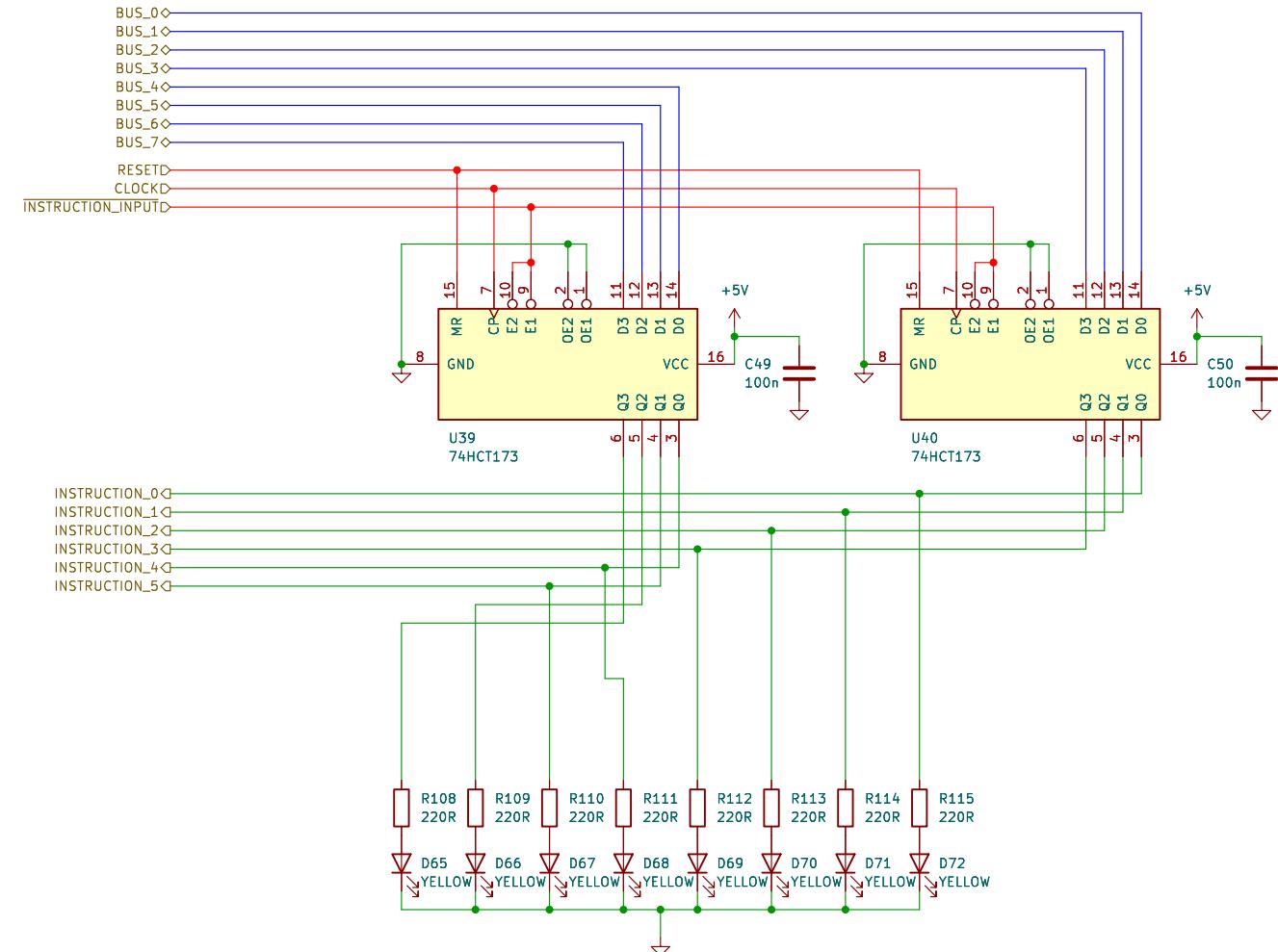
Sheet: /Program Counter/
File: program-counter.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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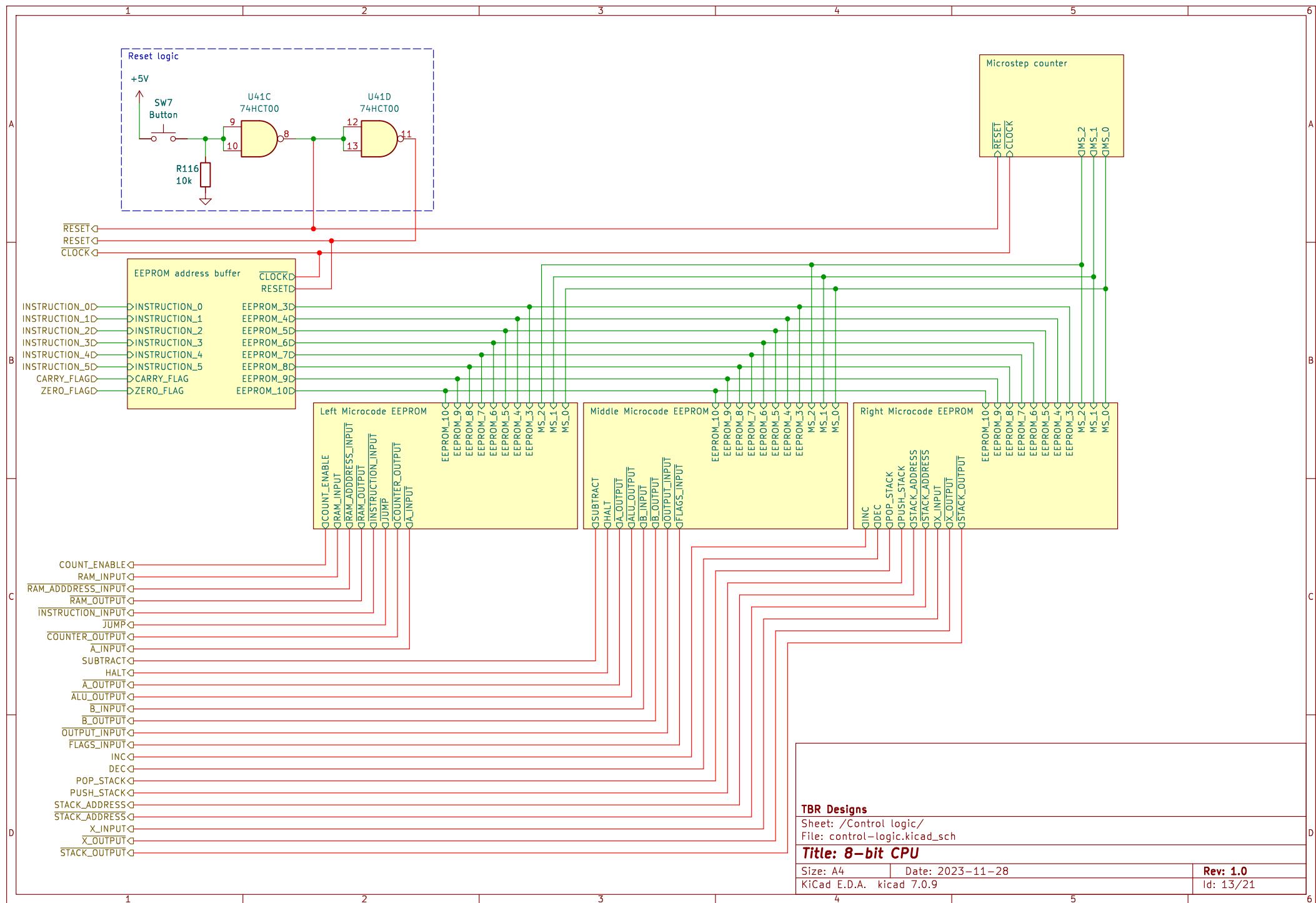
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Sheet: /Instruction register/
 File: instruction-register.kicad_sch

Title: 8-bit CPU

Size: A4 | Date: 2023-11-28
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This address buffer triggers on the inverted CLOCK.
 I had to include this because during an address transition the outputs of the EEPROM's are undefined.
 They vary wildly and random actions were triggered briefly.
 Making the address change on the inverted CLOCK seems to solve this issue because all of the other logic is triggered on the CLOCK.

A

A

B

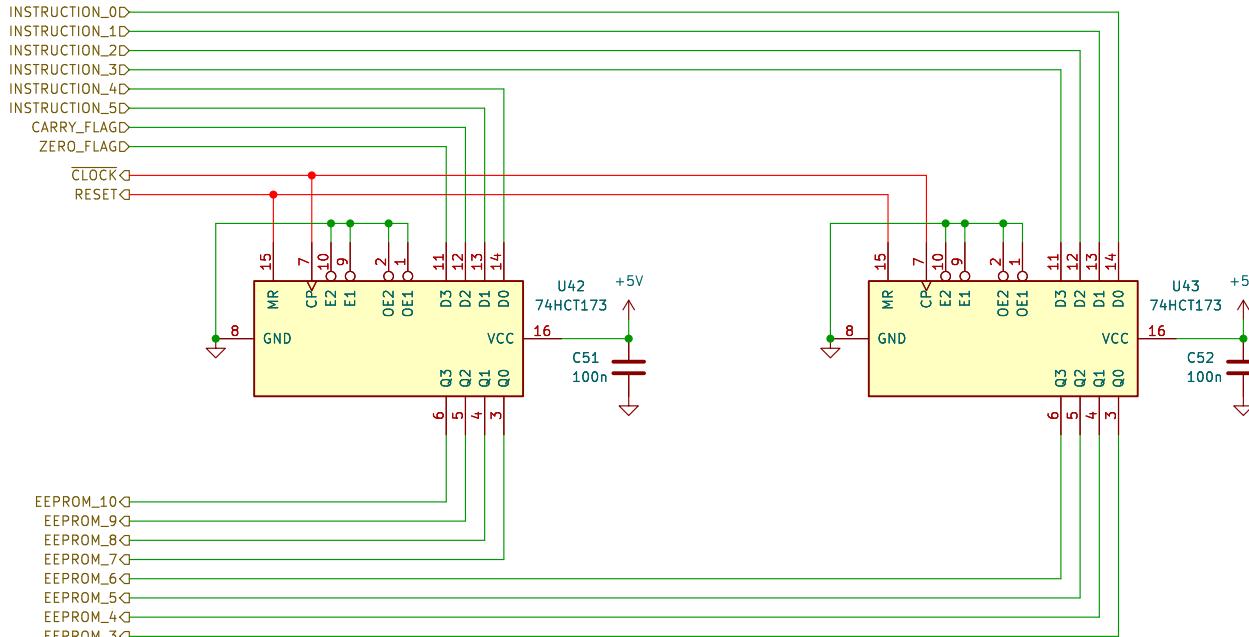
B

C

C

D

D



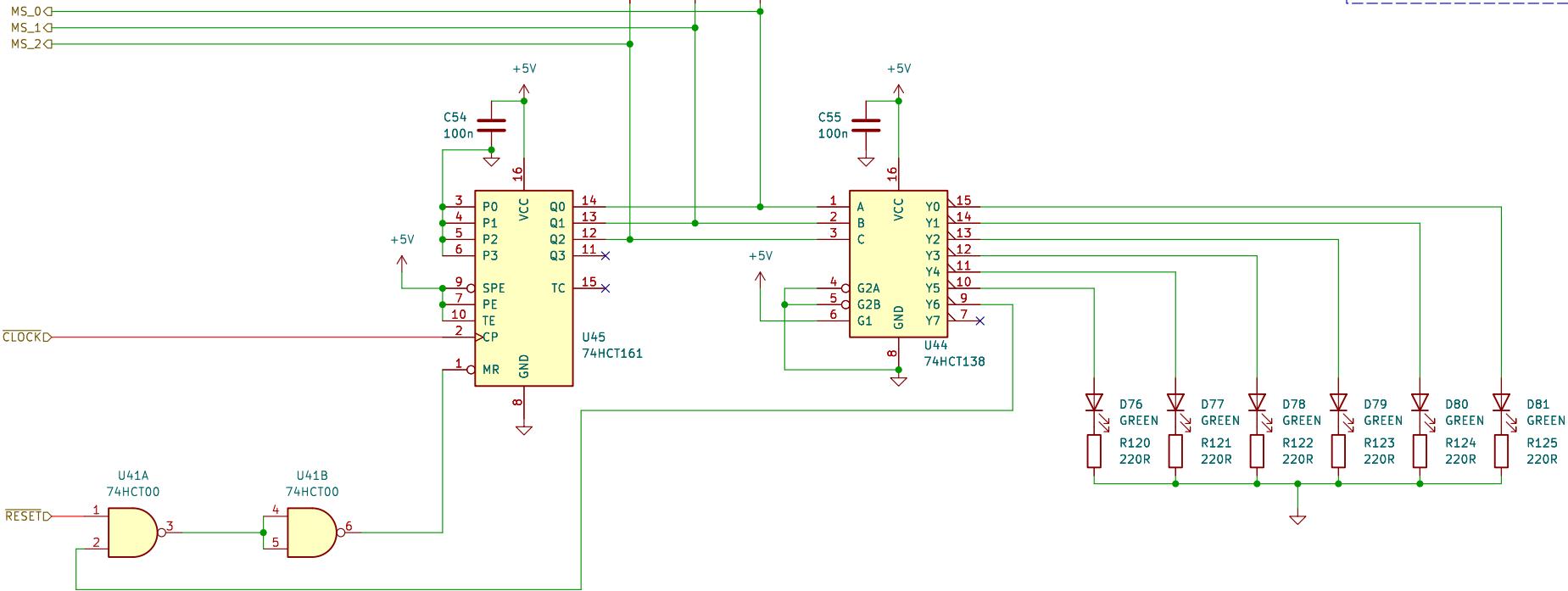
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Sheet: /Control logic/EEPROM address buffer/
 File: eeprom-address-buffer.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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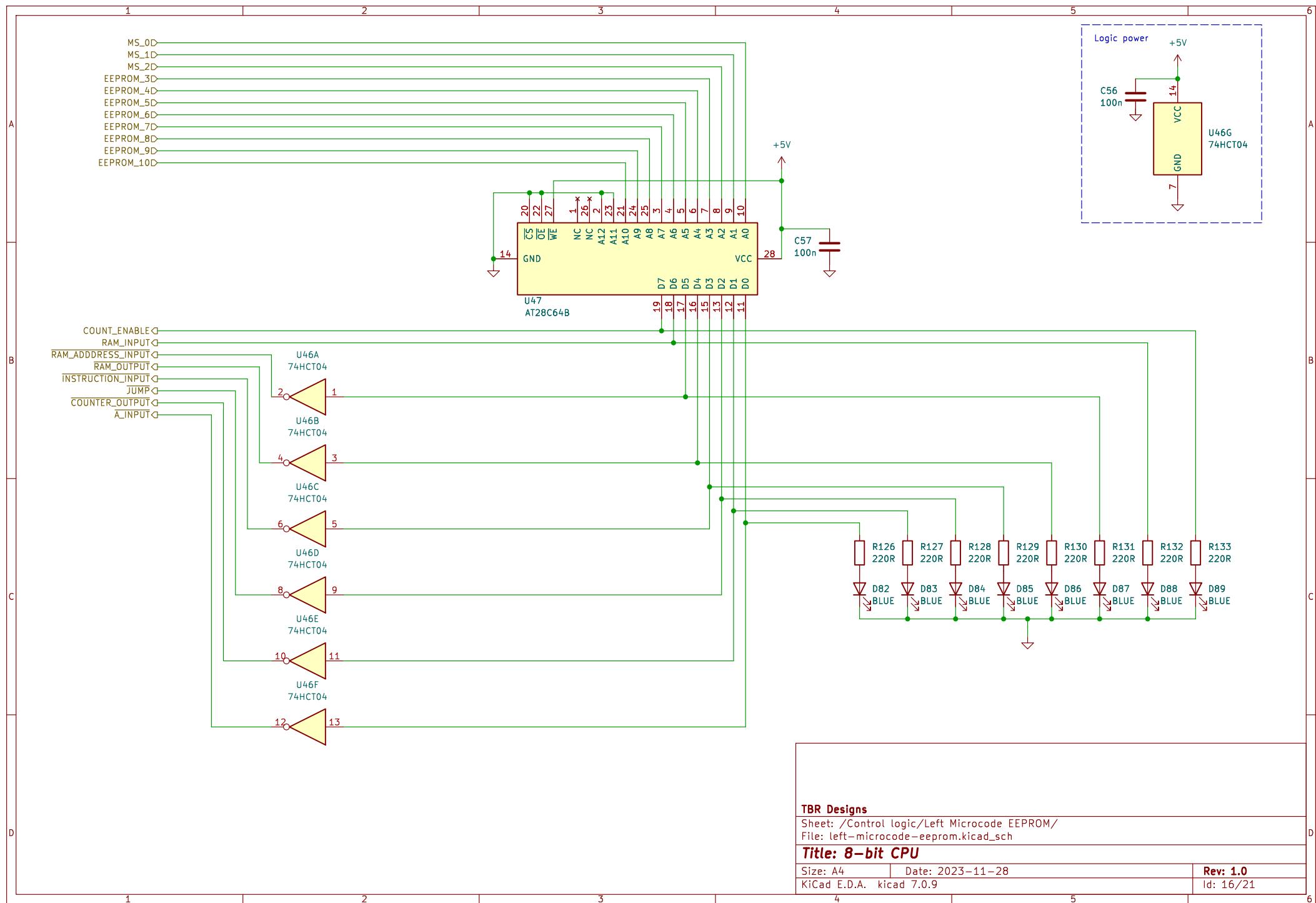
TBR Designs

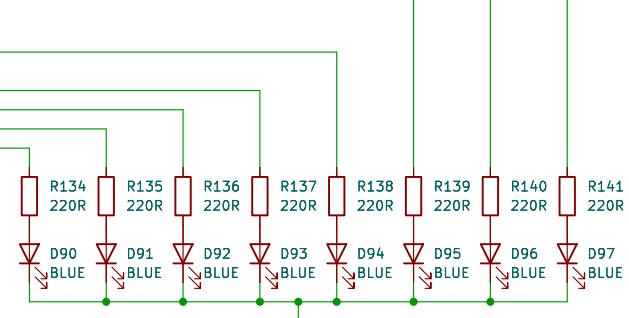
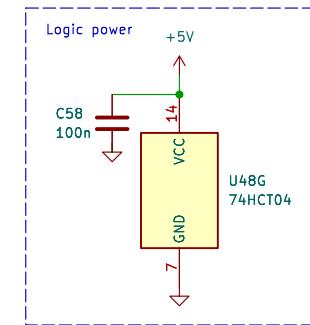
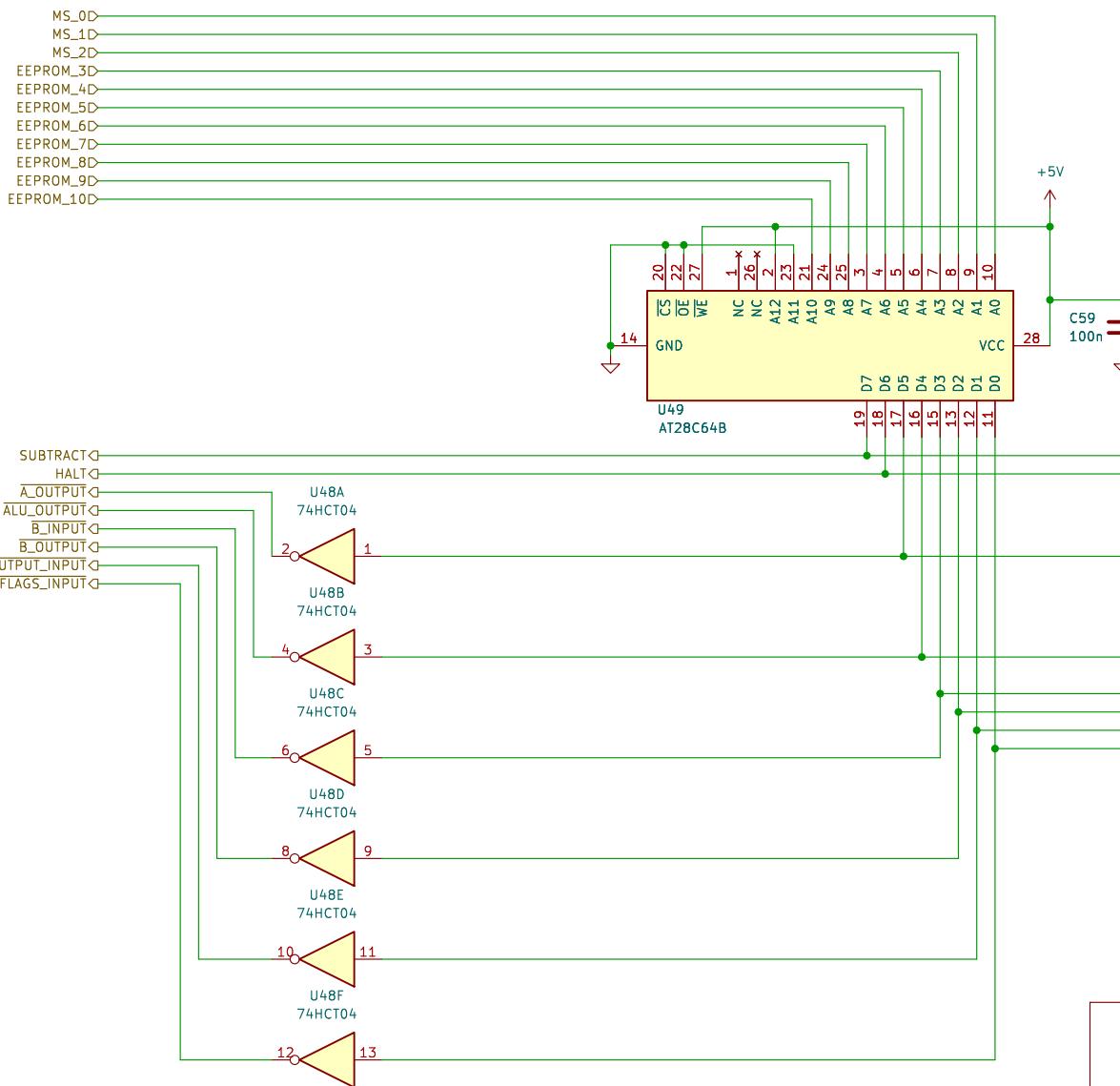
Sheet: /Control logic/Microstep counter/
File: microstep-counter.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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Rev: 1.0
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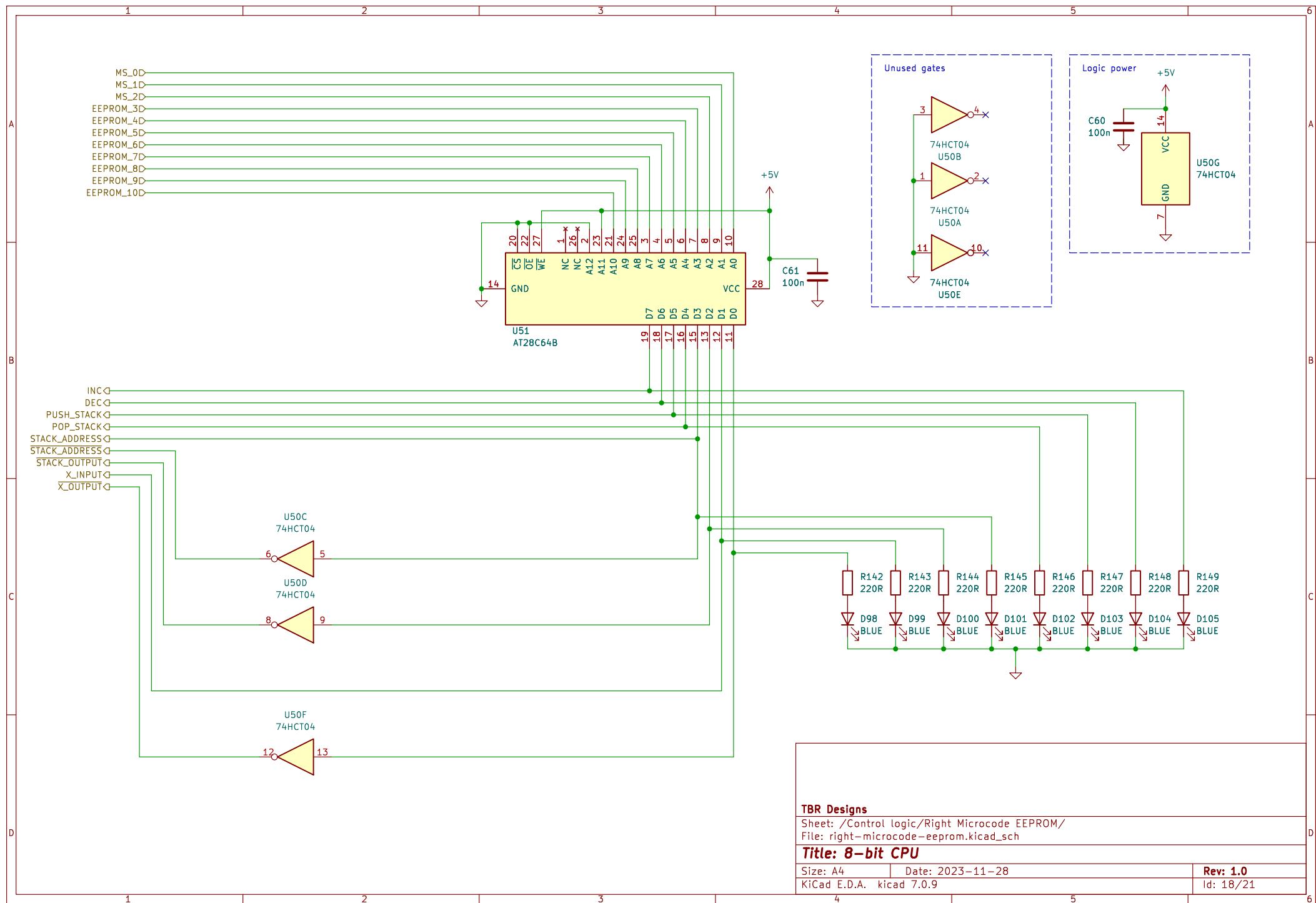
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Sheet: /Control logic/Middle Microcode EEPROM/
File: middle-microcode-eeprom.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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Rev: 1.0
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Sheet: /Control logic/Right Microcode EEPROM/
File: right-microcode-eeprom.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
KiCad E.D.A. kicad 7.0.9

Rev: 1.0
Id: 18/21

