Mapping of instruction names

Schematic name	Code name	Active low	
RAM_ADDRESS_IN PUT	Ral	Υ	
RAM_INPUT	RI	N	
RAM_OUTPUT	RO	Υ	
INSTRUCTION_INPUT	II	Υ	
JUMP	J	Υ	
COUNTER_OUTPU T	СО	Υ	
COUNTER_ENABL E	CE	N	
A_INPUT	Al	Υ	
A_OUTPUT	AO	Υ	
ALU_OUTPUT	AIO	Υ	
SUBTRACT	S	N	
B_INPUT	ВІ	Υ	
B_OUTPUT	во	Υ	
OUTPUT_INPUT	OI	Υ	
FLAGS_INPUT	FI	Υ	
HALT	HLT	N	

Micro code ROM layout

		Ins	tructi	on cod	e		Step		Flags		Left		Direct			To inv	verters	ers		Mic	ldle	Di	rect		7	Γο inv	erters			Rig	ht	Dir	ect	To inverters						
										CF	ZF			CE RI	Ral	RO	II	J	СО	Al			s	HLT	AO	AIO	ВІ	во	OI	FI			?	?	?	?	?	?	?	?
	A8	A7	A6	A5 A4	A3	A2	2 A1	Α0	A 9	A10	A11	A12	D7 D6	Y 5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y 5	Y4	Y 3	Y2	Y1	Y0	A11	A12	D7	D6	Y 5	Y 4	Y3	Y2	Y1	Y0	
NOP Is also the start of each	0	0	0	0 0	0	0		0	X	X	0	0	1	1	1	1		1		0	1									1	0									
instruction						_									·	·					•									·										
LDA	0	0	0	0 0	1	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
						0		1	Х	Х	0	0	1	1	1					0	1									1	0									
						1	0	0	Х	Х	0	0			1				1	0	1									1	0									
ADD	0	0	0	0 1	0	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
Add what is						0	1	1	Х	Х	0	0	1	1	1					0	1									1	0									
at memory address to A						1	0	0	Х	Х	0	0			1					0	1					1				1	0									
						1	0	1	Х	Х	0	0							1	0	1				1				1	1	0									
SUB	0	0	0	0 1	1	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
Subtract what						0	1	1	Х	Х	0	0	1	1	1					0	1									1	0									
is at memory address from						1	0	0	Х	Х	0	0			1					0	1					1				1	0									
Α						1	0	1	Х	Х	0	0							1	0	1	1			1				1	1	0									
STA	0	0	0	1 0	0	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
						0	1	1	Х	Х	0	0	1	1	1					0	1									1	0									
						1	0	0	Х	Х	0	0	1							0	1			1						1	0									
LDI Load direct	0	0	0	1 0	1	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
into A						0	1	1	Х	Х	0	0	1		1				1	0	1									1	0									
JMP	0	0	0	1 1	0	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
Jump to address						0	1	1	х	Х	0	0		1			1			0	1									1	0									
JC	0	0	0	1 1	1	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
Jump to address if						0	1	1	0	Х	0	0	1							0	1									1	0									
carry out						0	1	1	1	Х	0	0			1		1			0	1									1	0									
JZ	0	0	1	0 0	0	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
Jump to address if						0	1	1	Х	0	0	0	1							0	1									1	0									
zero						0	1	1	Х	1	0	0			1		1			0	1									1	0									
LDB	0	0	1	0 0	1	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
						0	1	1	Х	Х	0	0	1	1	1					0	1									1	0									
						1	0	0	Х	Х	0	0			1					0	1					1				1	0									
STB	0	0	1	0 1	0	0	1	0	Х	Х	0	0		1				1		0	1									1	0									
						\vdash	1	1	Х	Х	0	0	1		1					0	1									1	0									

	Instruction code			Step			Step		Flags		Left		Direct		To inverters					Middle		Direct		To inverters						Right		Dir	ect	To inverters							
										CF	ZF			CE	RI	Ral	RO	II	J	СО	Al			s	HLT	AO	AIO	ВІ	во	OI	FI			?	?	?	?	?	?	?	?
	A8	A7	A6	A 5	A 4	А3	A2	A1	A0	A 9	A10	A11	A12	D7	D6	Y 5	Y4	Y 3	Y2	Y 1	Y0	A11	A12	D7	D6	Y 5	Y4	Y 3	Y2	Y1	Y0	A11	A12	D7	D6	Y 5	Y 4	Y 3	Y2	Y 1	Y0
							1	0	0	Х	Х	0	0		1							0	1						1			1	0								
LDIB	0	0	1	0	1	1	0	1	0	Х	Х	0	0			1				1		0	1									1	0								
Load direct into B							0	1	1	Х	Х	0	0	1			1					0	1					1				1	0								
OUT	0	0	1	1	0	0	0	1	0	Х	Х	0	0	1								0	1			1				1		1	0								
OUTB	0	0	1	1	0	1	0	1	0	Х	Х	0	0	1								0	1						1	1		1	0								
HLT	0	0	1	1	1	1	0	1	0	Х	Х	0	0									0	1		1							1	0								