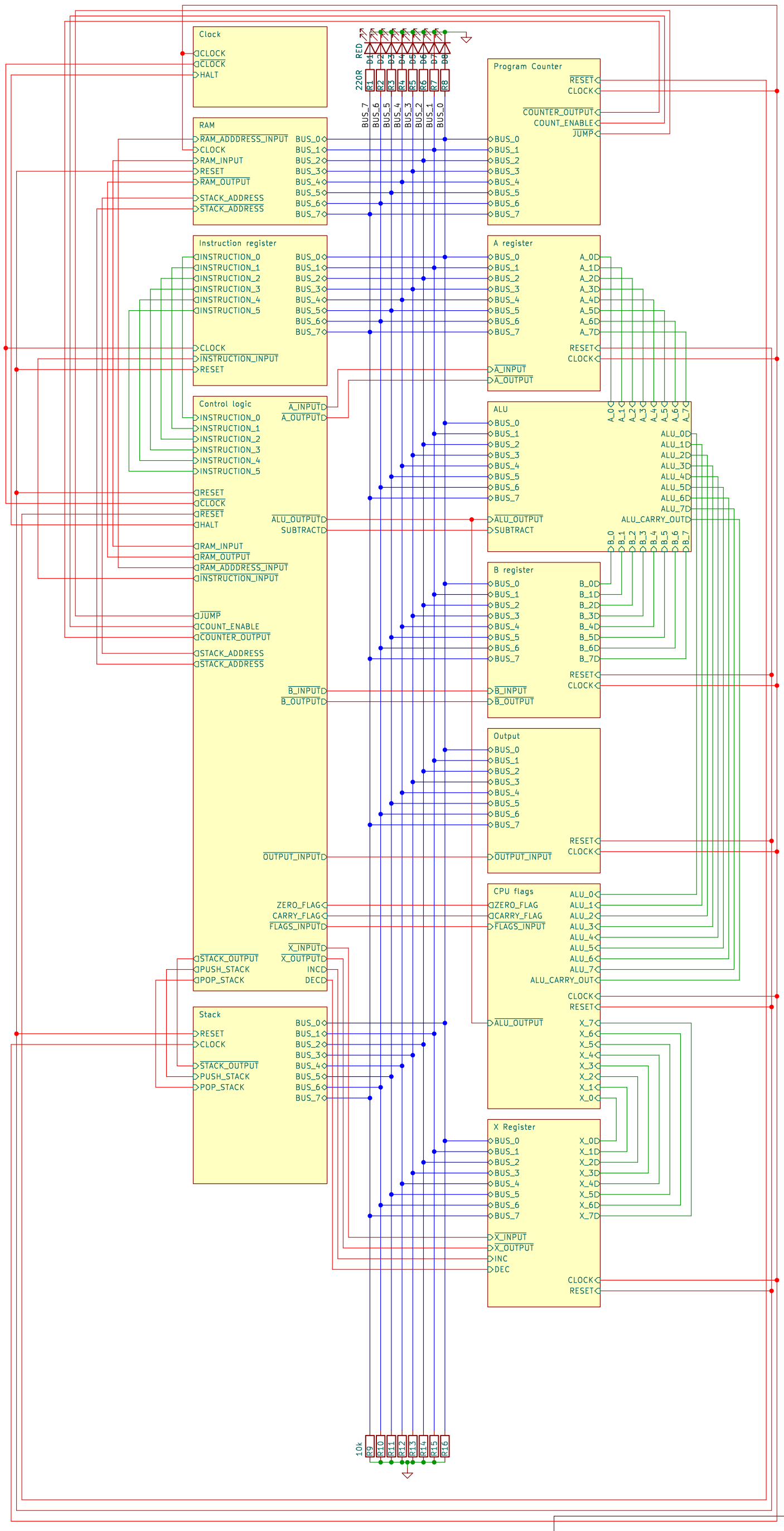


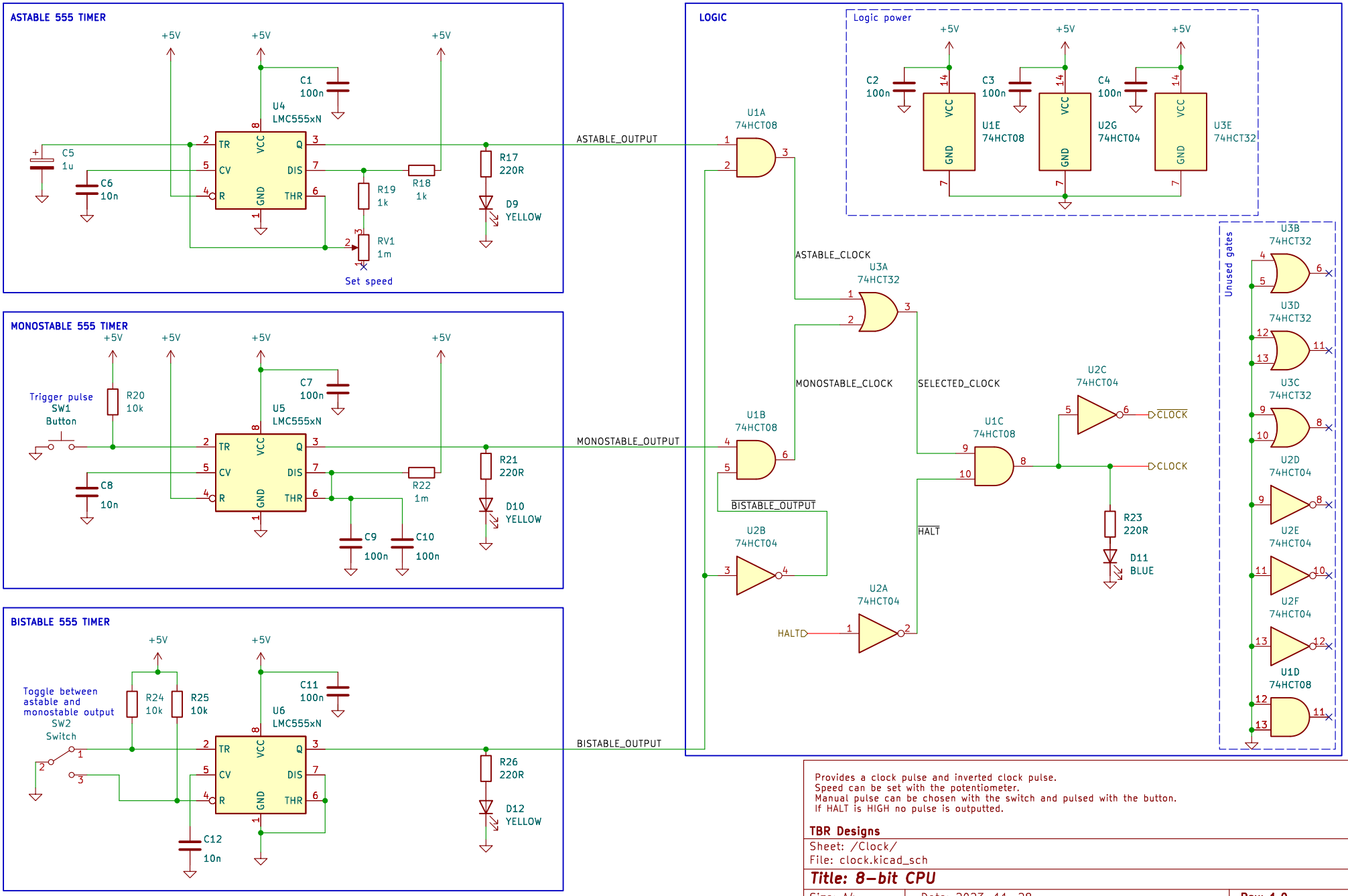
TBR Designs

Sheet: /

File: 8-bit-cpu.kicad_sch

Title: 8-bit CPU

Size: A3	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 1/20



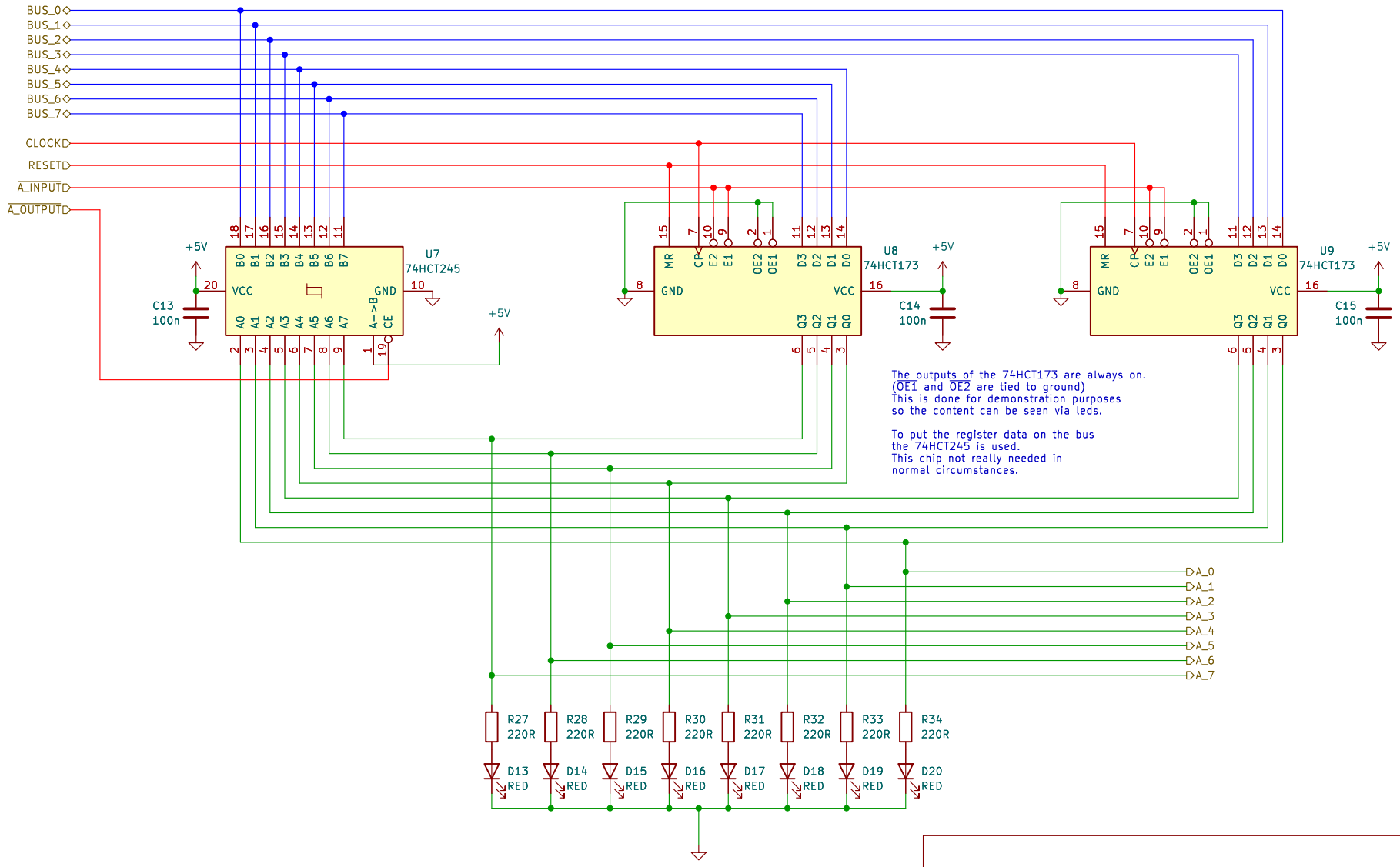
Provides a clock pulse and inverted clock pulse.
Speed can be set with the potentiometer.
Manual pulse can be chosen with the switch and pulsed with the button.
If HALT is HIGH no pulse is outputted.

TBR Designs

Sheet: /Clock/
File: clock.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 2/20



The outputs of the 74HCT173 are always on.
(OE1 and OE2 are tied to ground)
This is done for demonstration purposes
so the content can be seen via leds.

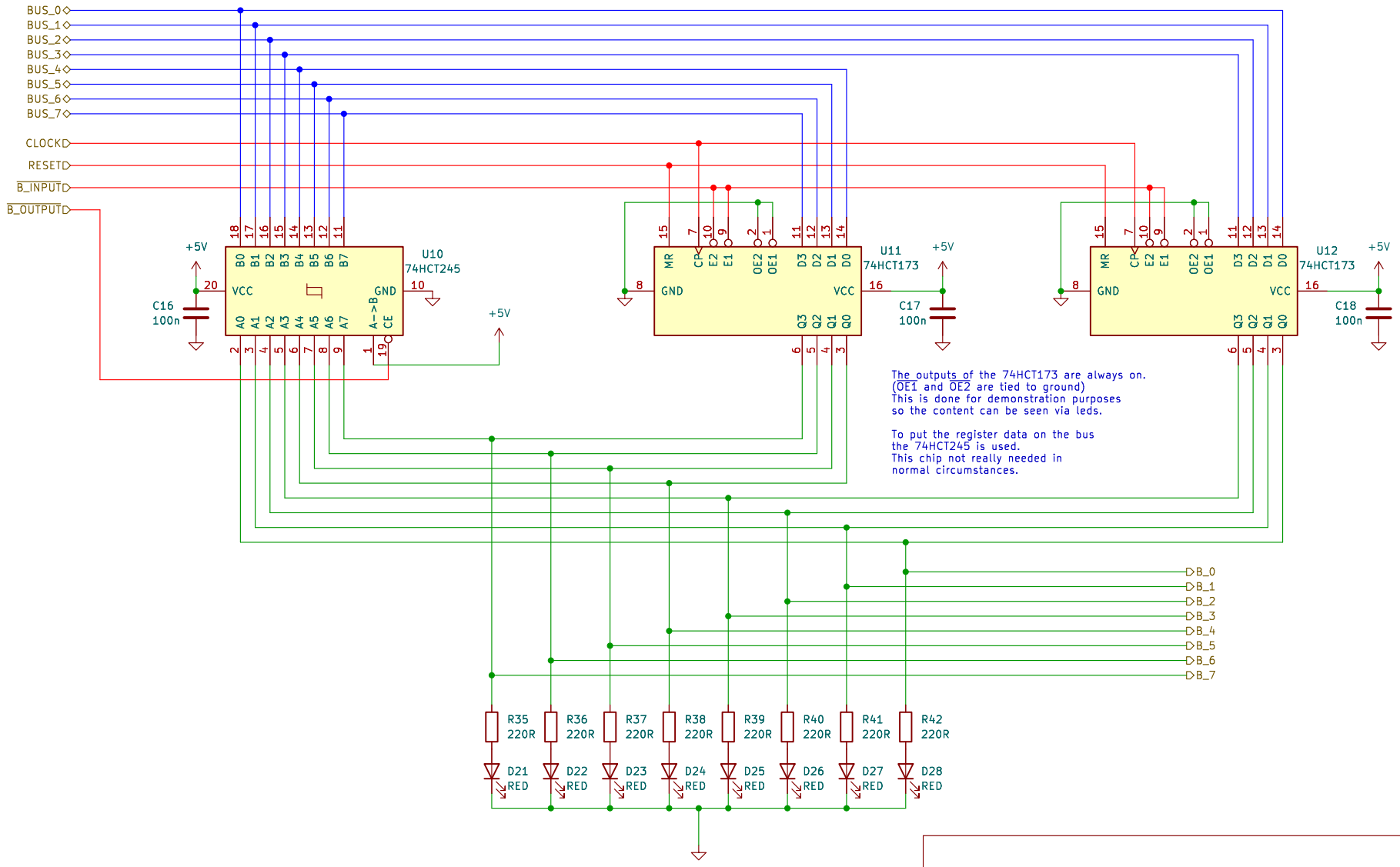
To put the register data on the bus
the 74HCT245 is used.
This chip not really needed in
normal circumstances.

TBR Designs

Sheet: /A register/
File: a-register.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 3/20

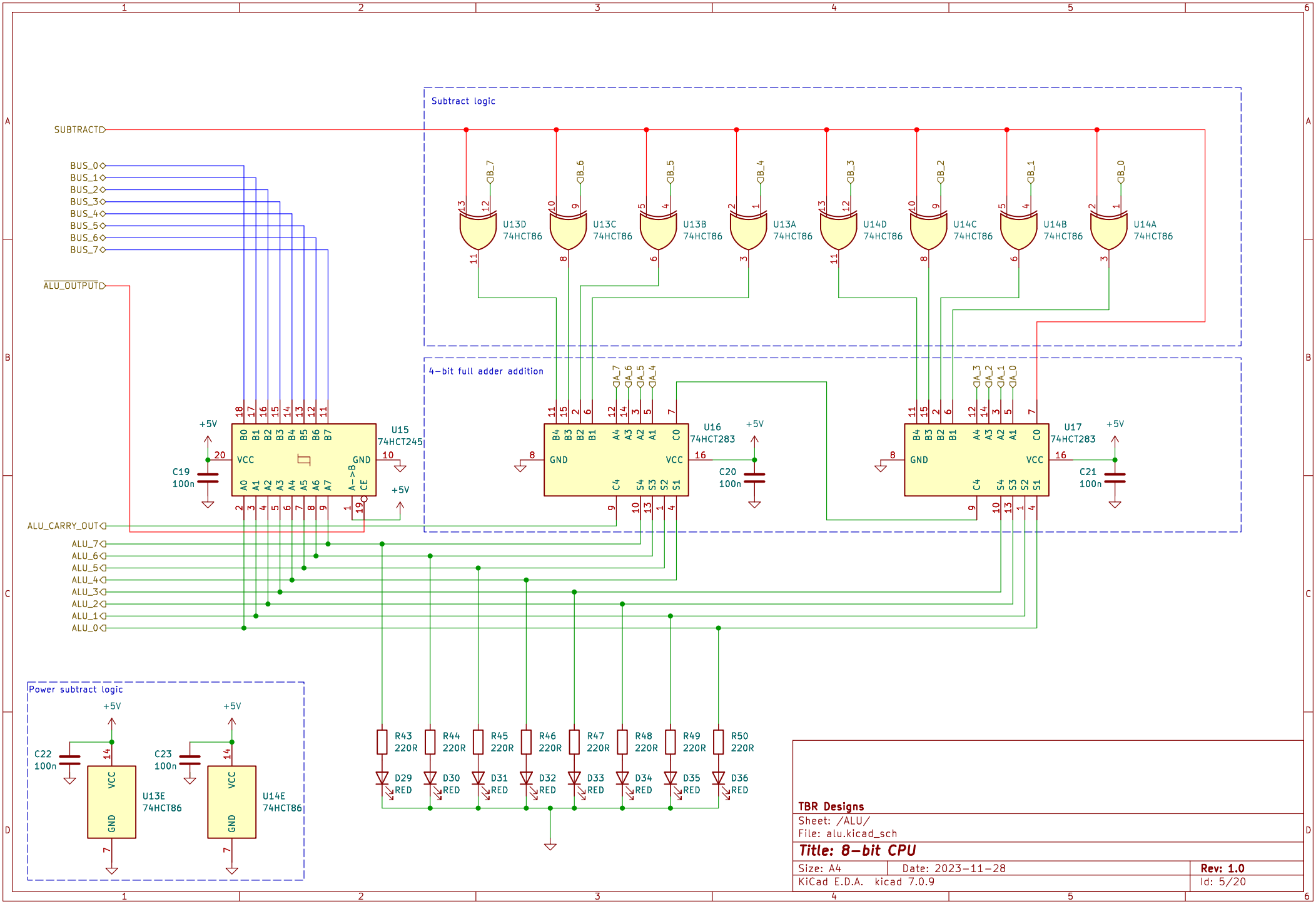


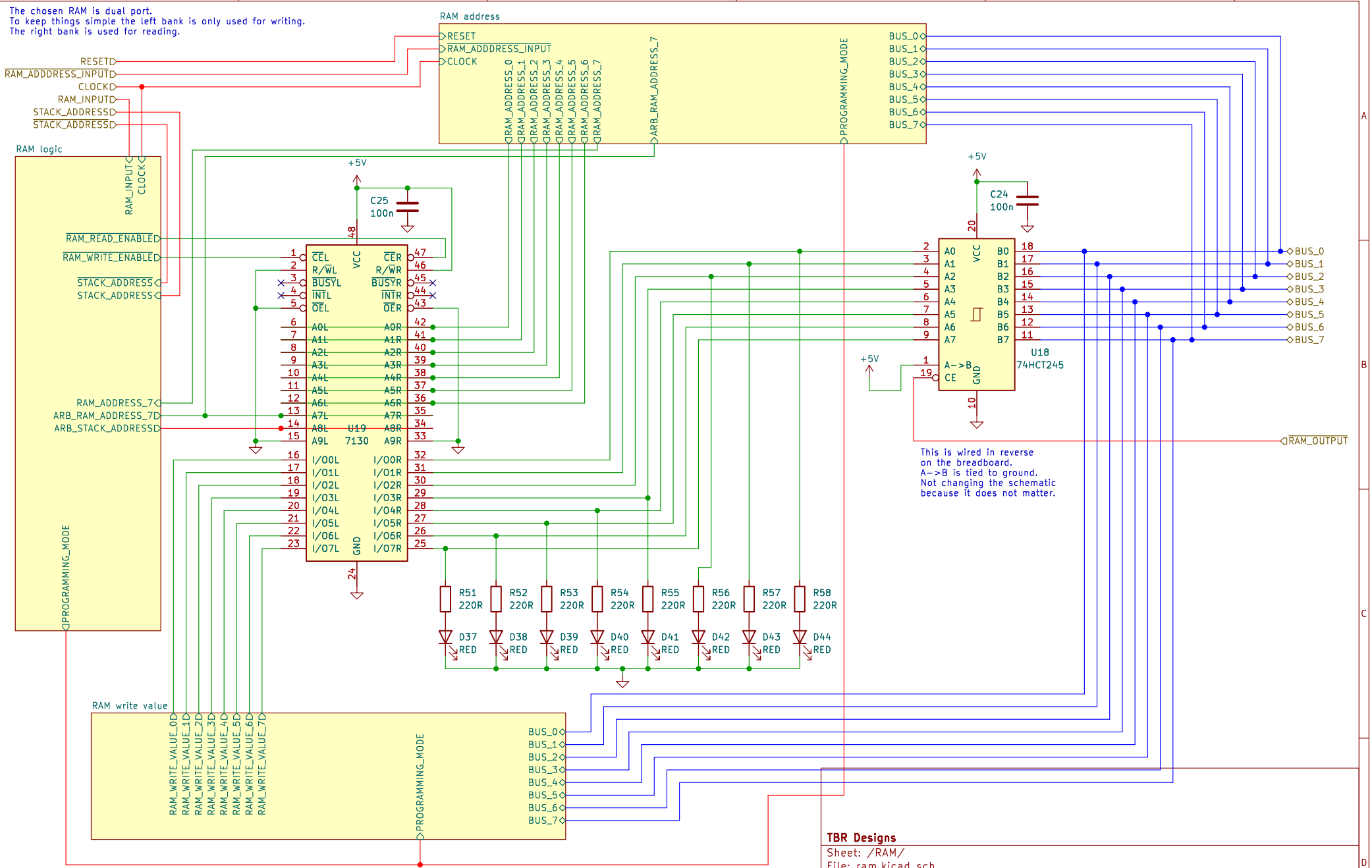
TBR Designs

Sheet: /B register/
File: b-register.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 4/20

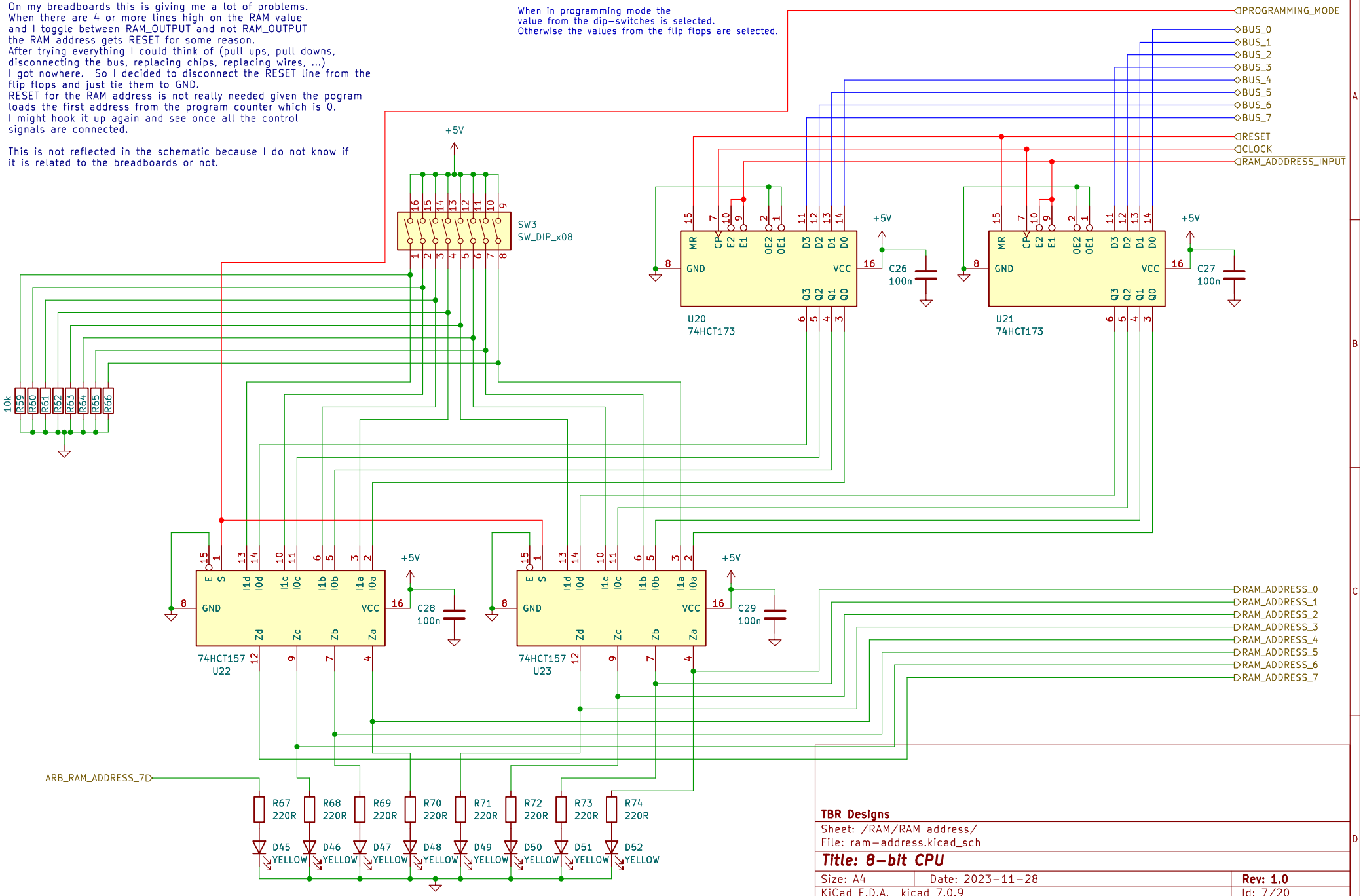

Subtract logic
4-bit full adder addition
Power subtract logic
SUBTRACT
BUS_0
BUS_1
BUS_2
BUS_3
BUS_4
BUS_5
BUS_6
BUS_7
ALU_OUTPUT
ALU_CARRY_OUT
ALU_7
ALU_6
ALU_5
ALU_4
ALU_3
ALU_2
ALU_1
ALU_0
U13D 74HCT86
U13C 74HCT86
U13B 74HCT86
U13A 74HCT86
U14D 74HCT86
U14C 74HCT86
U14B 74HCT86
U14A 74HCT86
U15 74HCT245
U16 74HCT283
U17 74HCT283
U13E 74HCT86
U14E 74HCT86
C19 100n
C20 100n
C21 100n
C22 100n
C23 100n
+5V
R43 220R
R44 220R
R45 220R
R46 220R
R47 220R
R48 220R
R49 220R
R50 220R
D29 RED
D30 RED
D31 RED
D32 RED
D33 RED
D34 RED
D35 RED
D36 RED
TBR Designs
Sheet: /ALU/
File: alu.kicad_sch
Title: 8-bit CPU
Size: A4
Date: 2023-11-28
Rev: 1.0
KiCad E.D.A. kicad 7.0.9
Id: 5/20


The chosen RAM is dual port.
To keep things simple the left bank is only used for writing.
The right bank is used for reading.
RAM address
RESET
RAM_ADDDRESS_INPUT
CLOCK
RAM_ADDRESS_0
RAM_ADDRESS_1
RAM_ADDRESS_2
RAM_ADDRESS_3
RAM_ADDRESS_4
RAM_ADDRESS_5
RAM_ADDRESS_6
RAM_ADDRESS_7
ARB_RAM_ADDRESS_7
PROGRAMMING_MODE
BUS_0
BUS_1
BUS_2
BUS_3
BUS_4
BUS_5
BUS_6
BUS_7
RAM_INPUT
STACK_ADDRESS
RAM logic
RAM_READ_ENABLE
RAM_WRITE_ENABLE
ARB_RAM_ADDRESS_7
ARB_STACK_ADDRESS
+5V
C25
100n
C24
100n
U19
7130
U18
74HCT245
A->B
CE
VCC
GND
RAM_OUTPUT
This is wired in reverse
on the breadboard.
A->B is tied to ground.
Not changing the schematic
because it does not matter.
R51 220R
R52 220R
R53 220R
R54 220R
R55 220R
R56 220R
R57 220R
R58 220R
D37 RED
D38 RED
D39 RED
D40 RED
D41 RED
D42 RED
D43 RED
D44 RED
RAM write value
RAM_WRITE_VALUE_0D
RAM_WRITE_VALUE_1D
RAM_WRITE_VALUE_2D
RAM_WRITE_VALUE_3D
RAM_WRITE_VALUE_4D
RAM_WRITE_VALUE_5D
RAM_WRITE_VALUE_6D
RAM_WRITE_VALUE_7D
TBR Designs
Sheet: /RAM/
File: ram.kicad_sch
Title: 8-bit CPU
Size: A4
Date: 2023-11-28
Rev: 1.0
KiCad E.D.A. kicad 7.0.9
Id: 6/20

A word on the RESET line.
On my breadboards this is giving me a lot of problems.
When there are 4 or more lines high on the RAM value
and I toggle between RAM_OUTPUT and not RAM_OUTPUT
the RAM address gets RESET for some reason.
After trying everything I could think of (pull ups, pull downs,
disconnecting the bus, replacing chips, replacing wires, ...)
I got nowhere. So I decided to disconnect the RESET line from the
flip flops and just tie them to GND.
RESET for the RAM address is not really needed given the pogram
loads the first address from the program counter which is 0.
I might hook it up again and see once all the control
signals are connected.

This is not reflected in the schematic because I do not know if
it is related to the breadboards or not.

When in programming mode the
value from the dip-switches is selected.
Otherwise the values from the flip flops are selected.



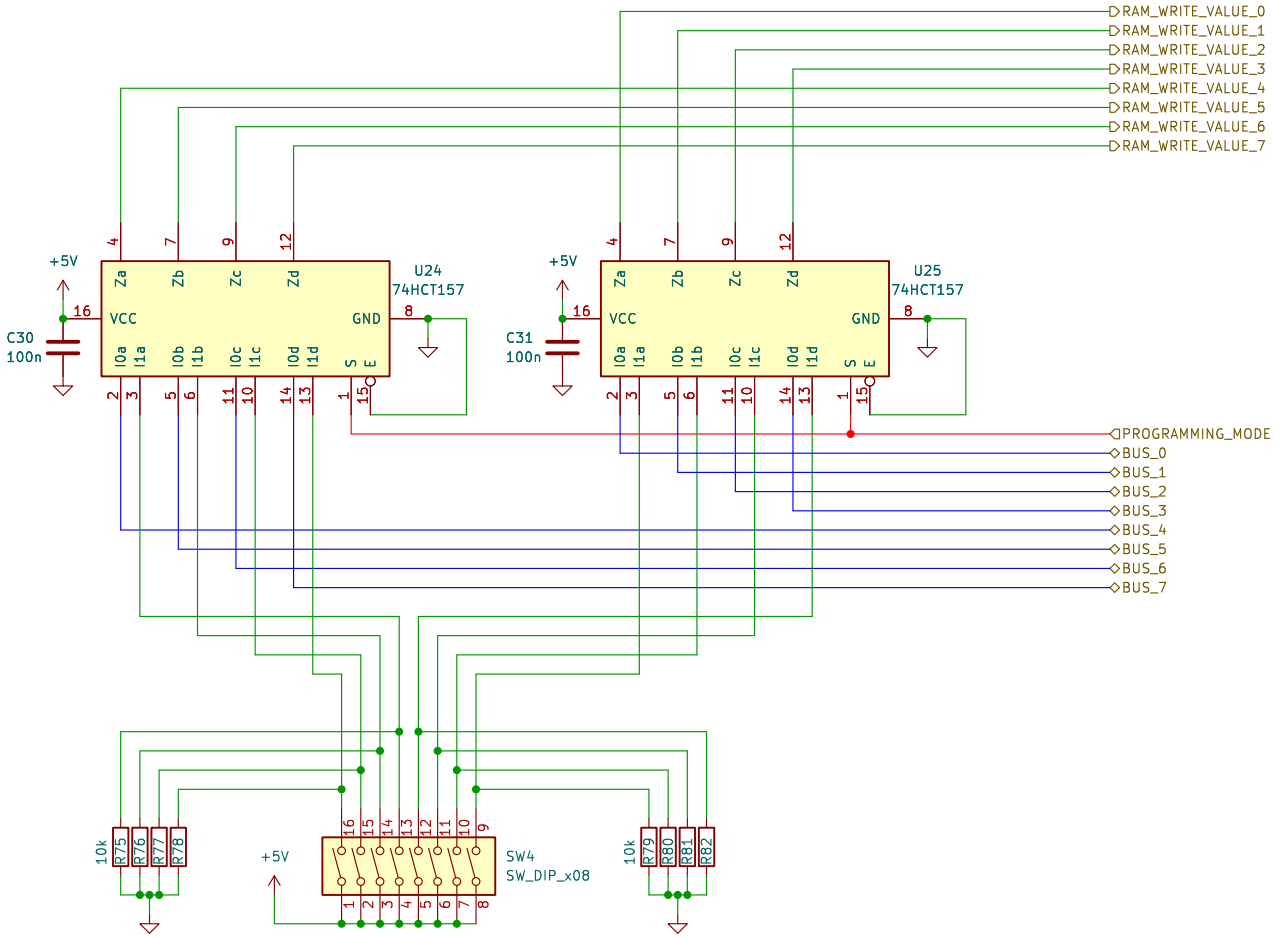
TBR Designs

Sheet: /RAM/RAM address/
File: ram-address.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 7/20

When in programming mode the
value from the dip-switches is selected.
Otherwise the value from the bus is selected.

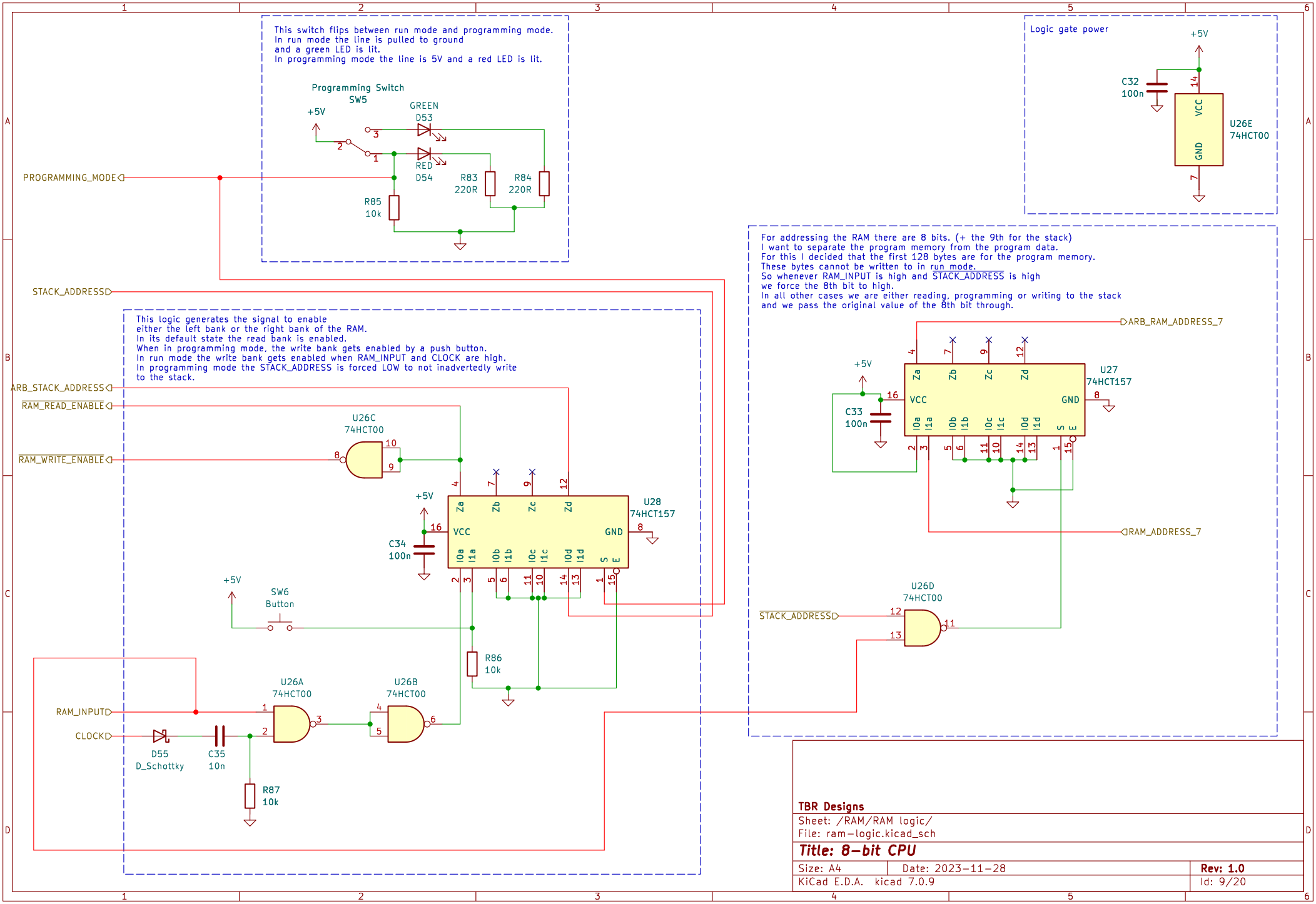


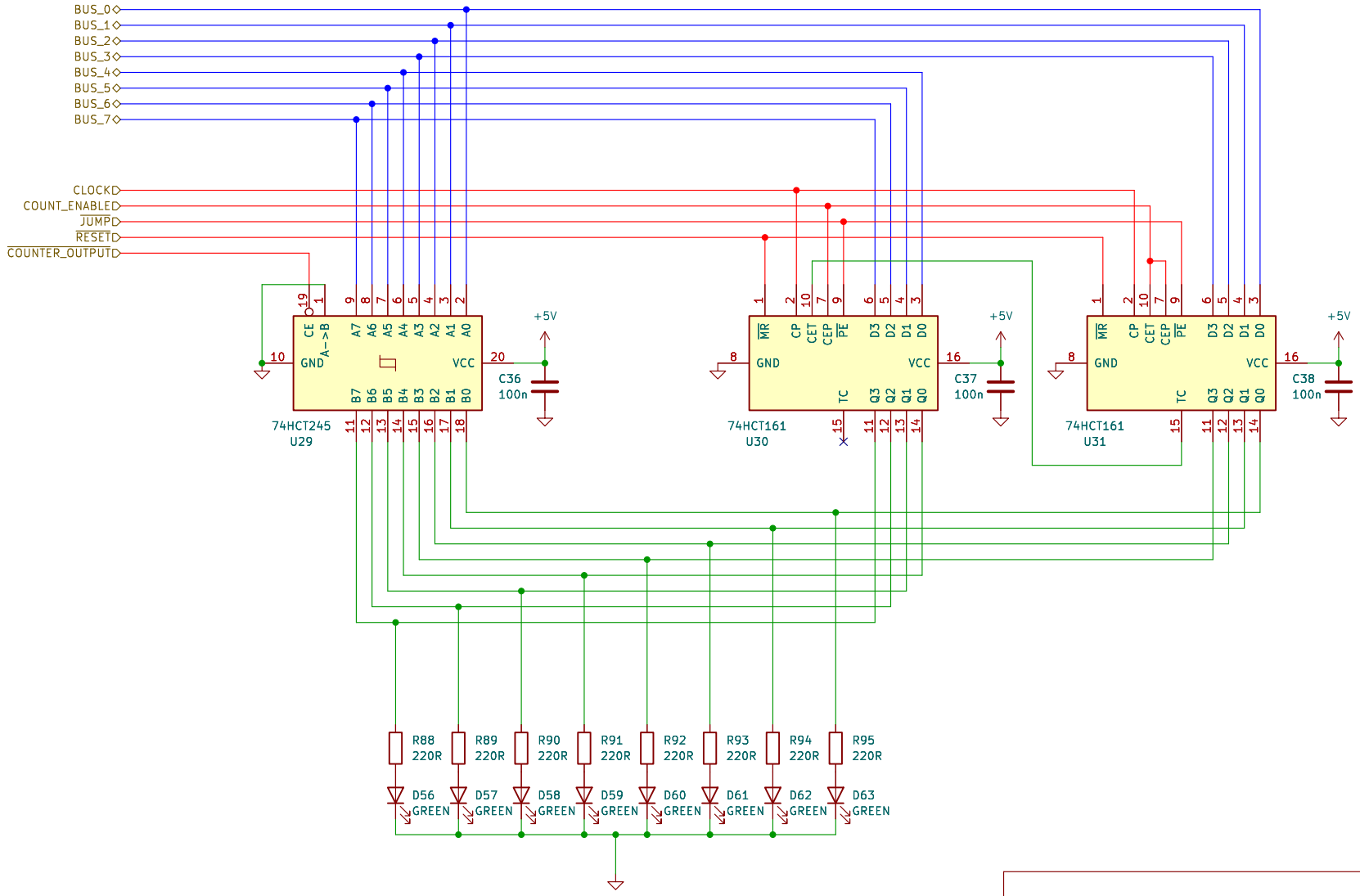
TBR Designs

Sheet: /RAM/RAM write value/
File: ram-write-value.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 8/20


This switch flips between run mode and programming mode.
In run mode the line is pulled to ground
and a green LED is lit.
In programming mode the line is 5V and a red LED is lit.
Programming Switch
SW5
+5V
GREEN
D53
RED
D54
R83
220R
R84
220R
R85
10k
PROGRAMMING_MODE
Logic gate power
+5V
C32
100n
U26E
74HCT00
VCC
GND
STACK_ADDRESS
This logic generates the signal to enable
either the left bank or the right bank of the RAM.
In its default state the read bank is enabled.
When in programming mode, the write bank gets enabled by a push button.
In run mode the write bank gets enabled when RAM_INPUT and CLOCK are high.
In programming mode the STACK_ADDRESS is forced LOW to not inadvertedly write
to the stack.
ARB_STACK_ADDRESS
RAM_READ_ENABLE
RAM_WRITE_ENABLE
U26C
74HCT00
U28
74HCT157
C34
100n
SW6
Button
R86
10k
U26A
74HCT00
U26B
74HCT00
RAM_INPUT
CLOCK
D55
D_Schottky
C35
10n
R87
10k
For addressing the RAM there are 8 bits. (+ the 9th for the stack)
I want to separate the program memory from the program data.
For this I decided that the first 128 bytes are for the program memory.
These bytes cannot be written to in run mode.
So whenever RAM_INPUT is high and STACK_ADDRESS is high
we force the 8th bit to high.
In all other cases we are either reading, programming or writing to the stack
and we pass the original value of the 8th bit through.
ARB_RAM_ADDRESS_7
U27
74HCT157
C33
100n
RAM_ADDRESS_7
U26D
74HCT00
STACK_ADDRESS
TBR Designs
Sheet: /RAM/RAM logic/
File: ram-logic.kicad_sch
Title: 8-bit CPU
Size: A4
Date: 2023-11-28
Rev: 1.0
KiCad E.D.A. kicad 7.0.9
Id: 9/20



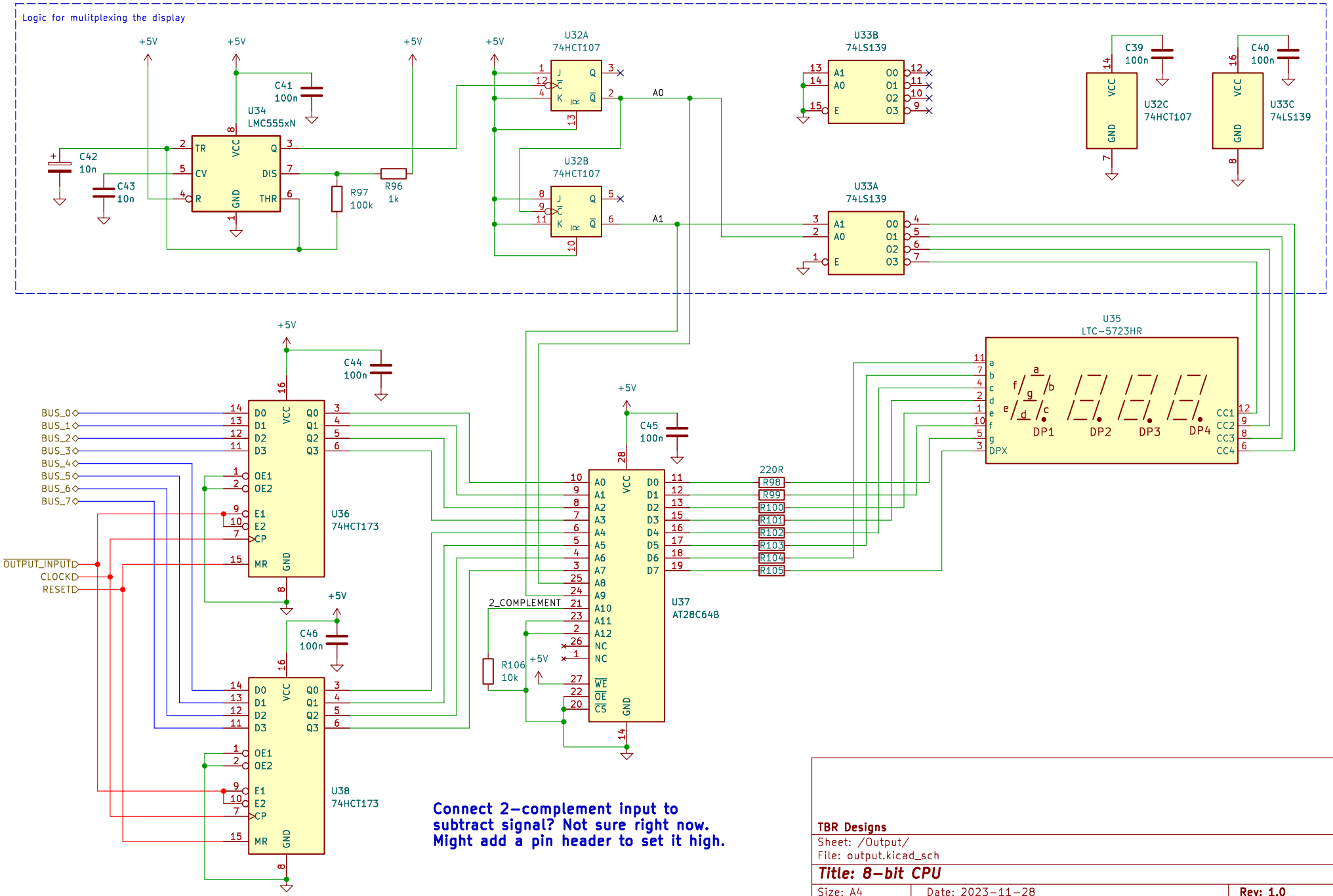
TBR Designs

Sheet: /Program Counter/

File: program-counter.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 10/20



Connect 2-complement input to subtract signal? Not sure right now. Might add a pin header to set it high.

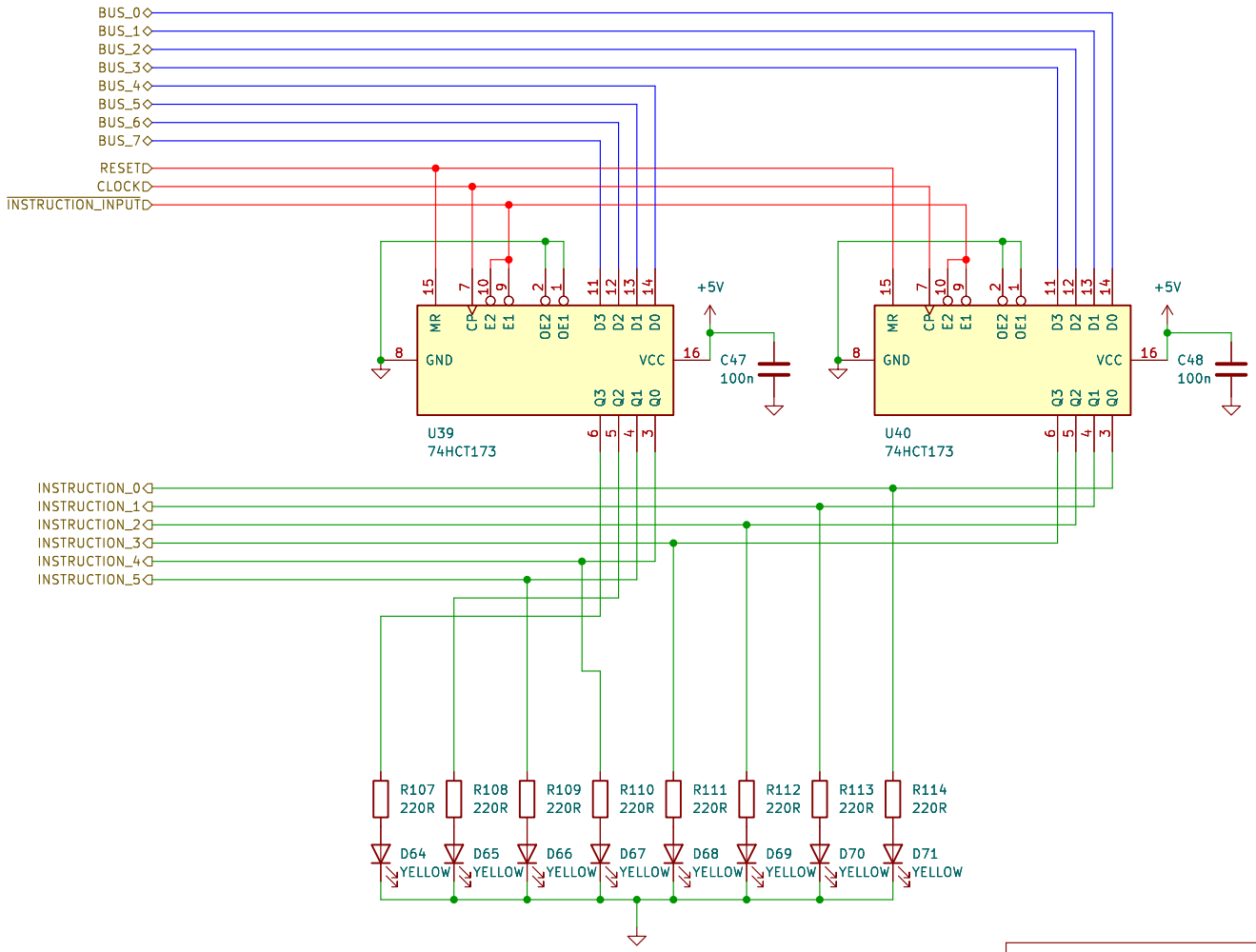
TBR Designs

Sheet: /Output/

File: output.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 11/20

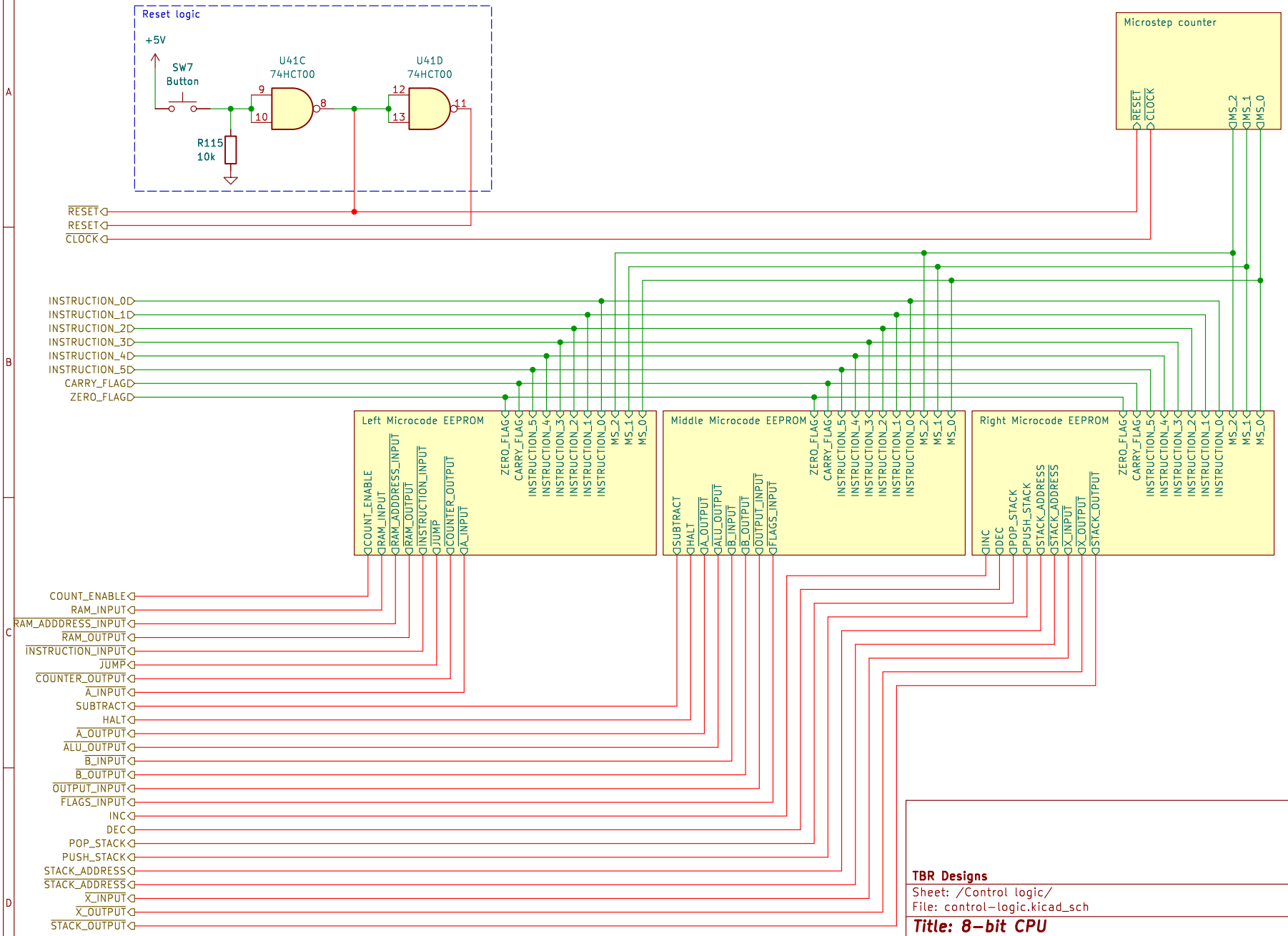


TBR Designs

Sheet: /Instruction register/
File: instruction-register.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 12/20



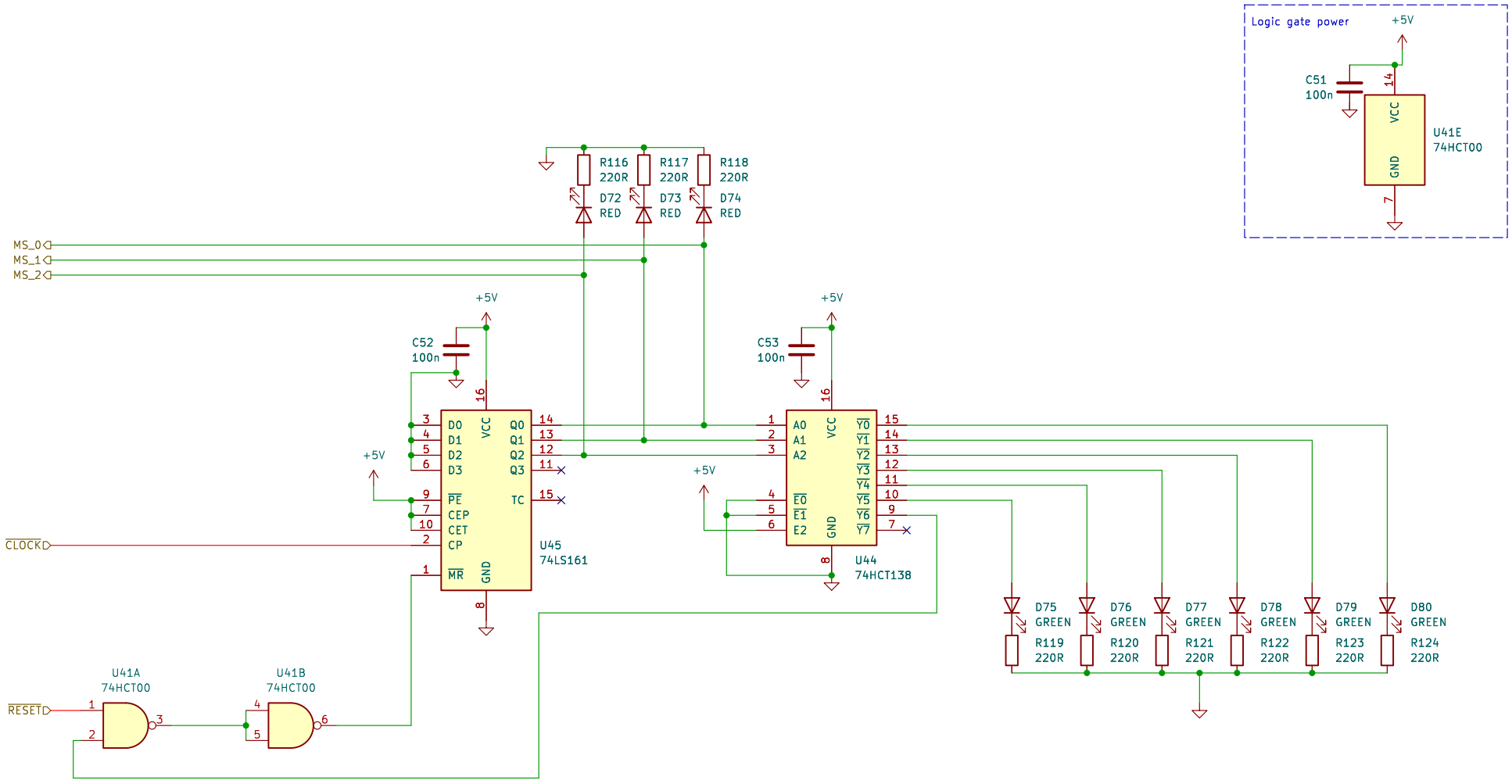
TBR Designs

Sheet: /Control logic/

File: control-logic.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 13/20



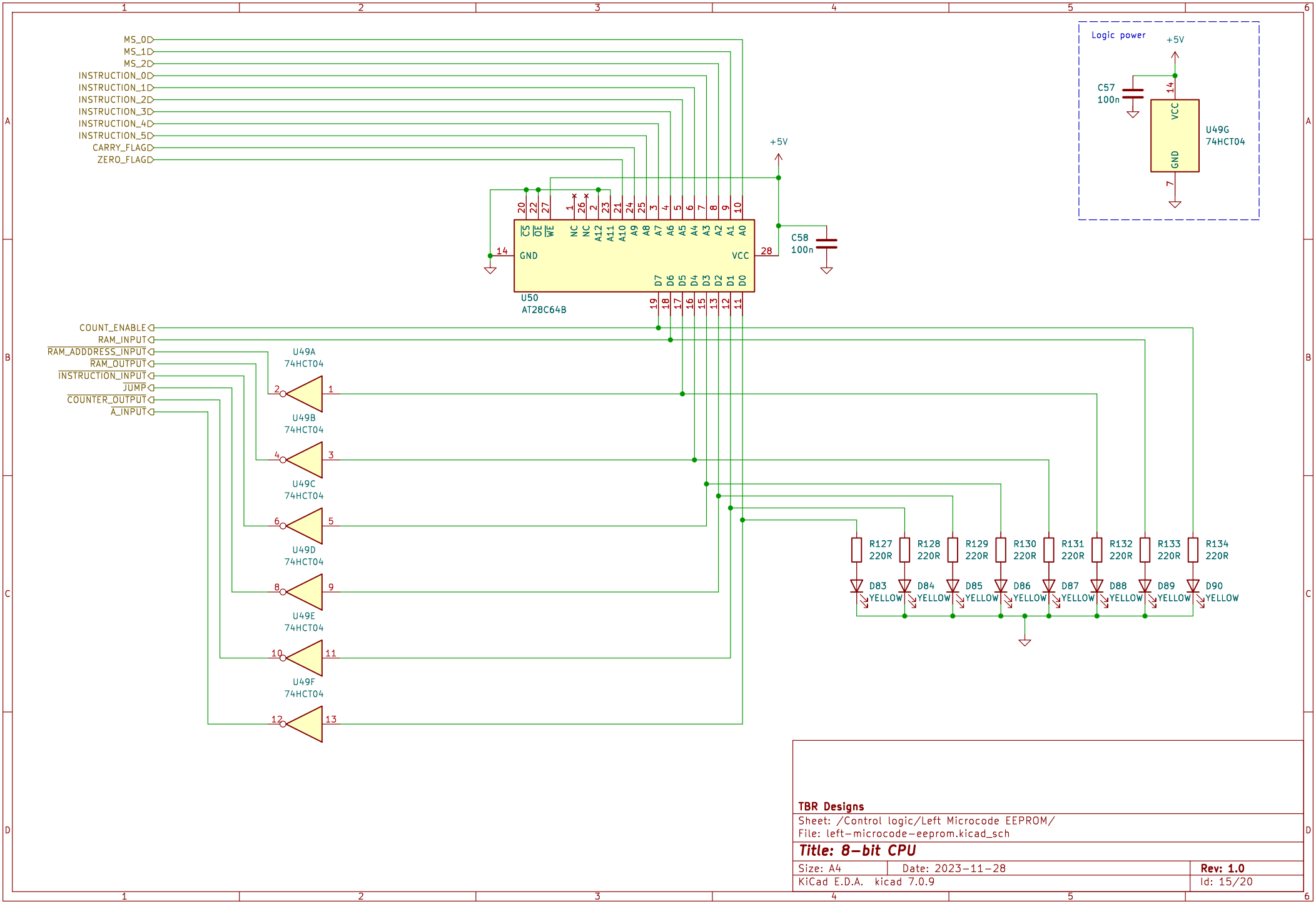
TBR Designs

Sheet: /Control logic/Microstep counter/

File: microstep-counter.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 14/20

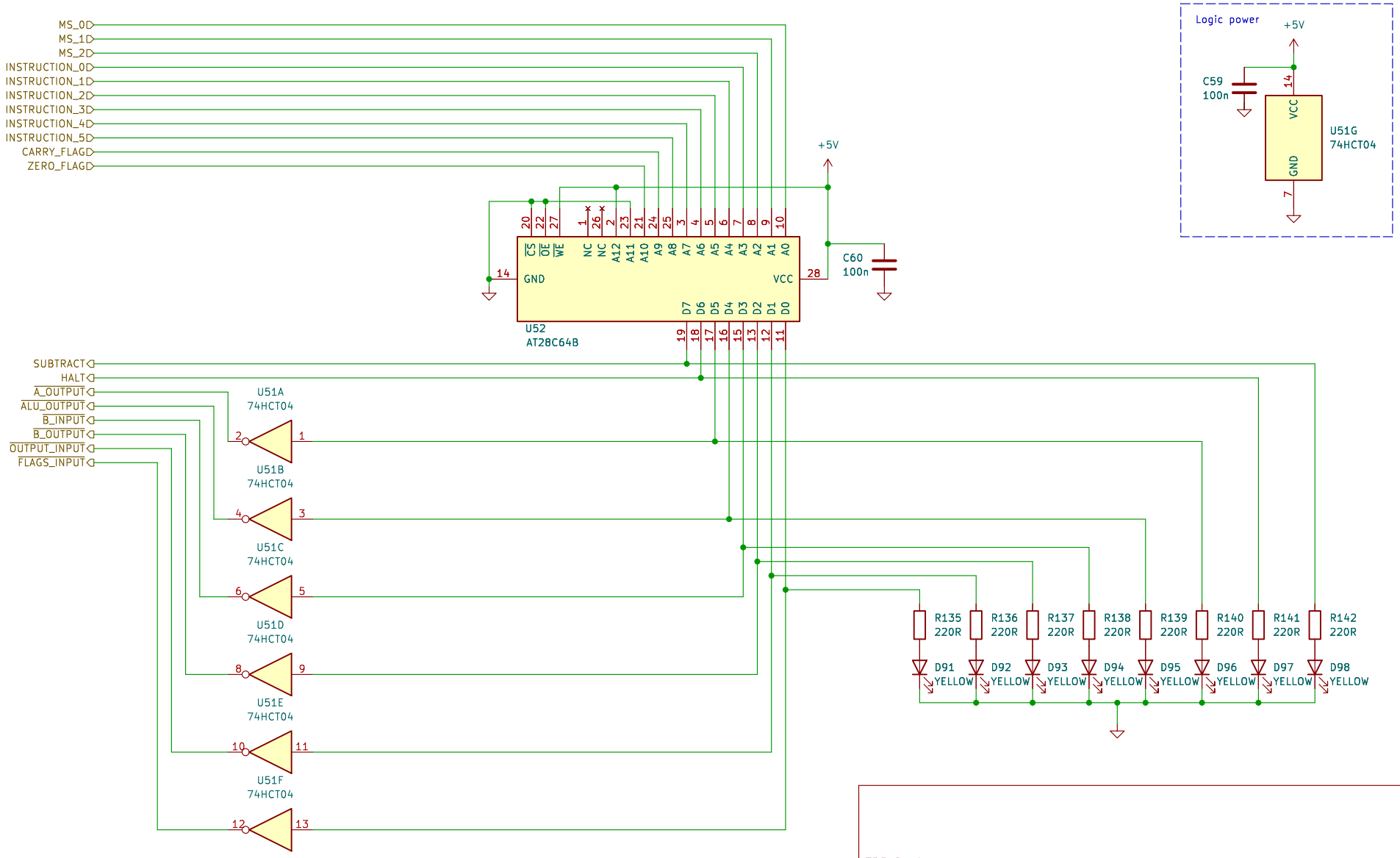


TBR Designs

Sheet: /Control logic/Left Microcode EEPROM/
File: left-microcode-eeprom.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 15/20

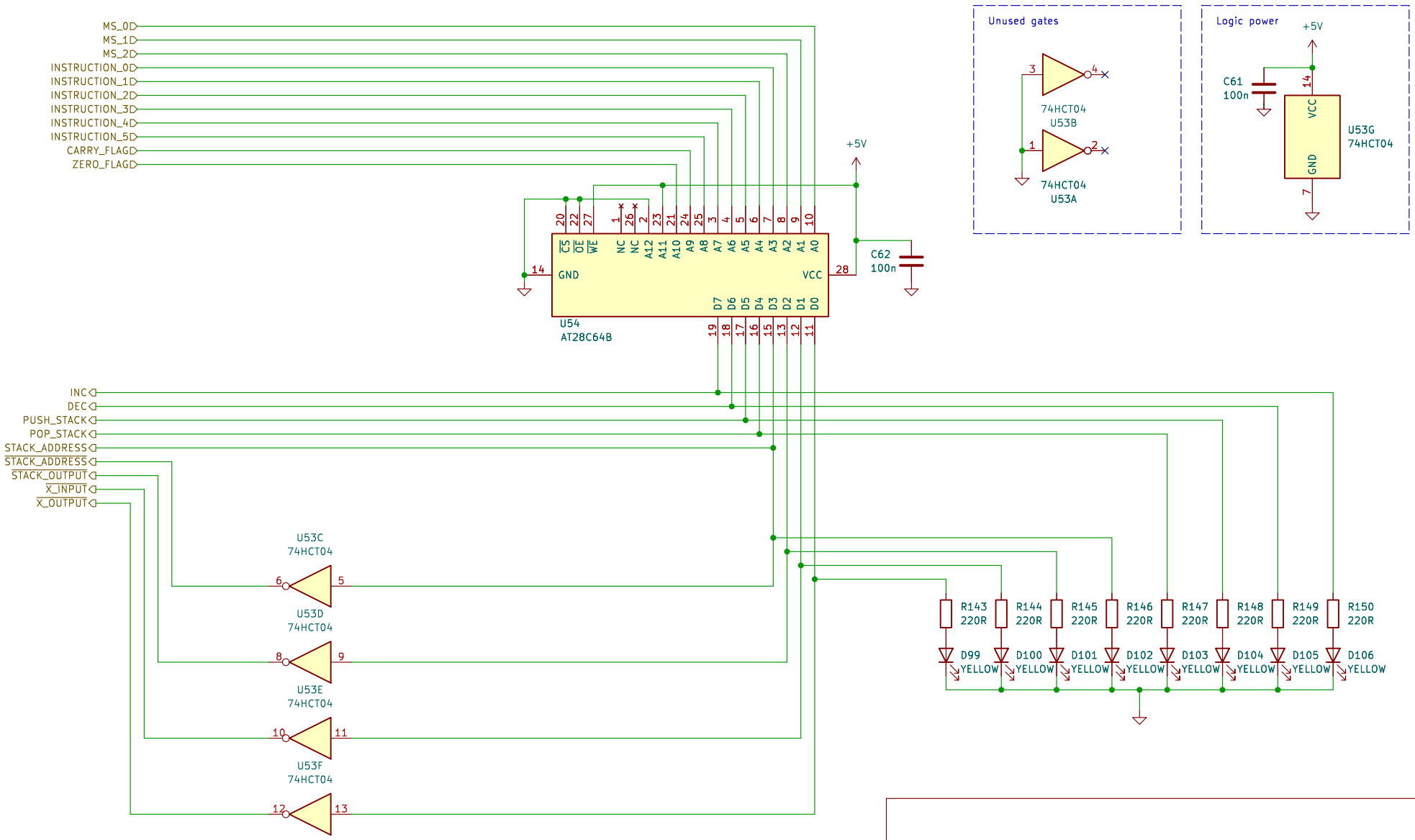


TBR Designs

Sheet: /Control logic/Middle Microcode EEPROM/
File: middle-microcode-eeprom.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 16/20

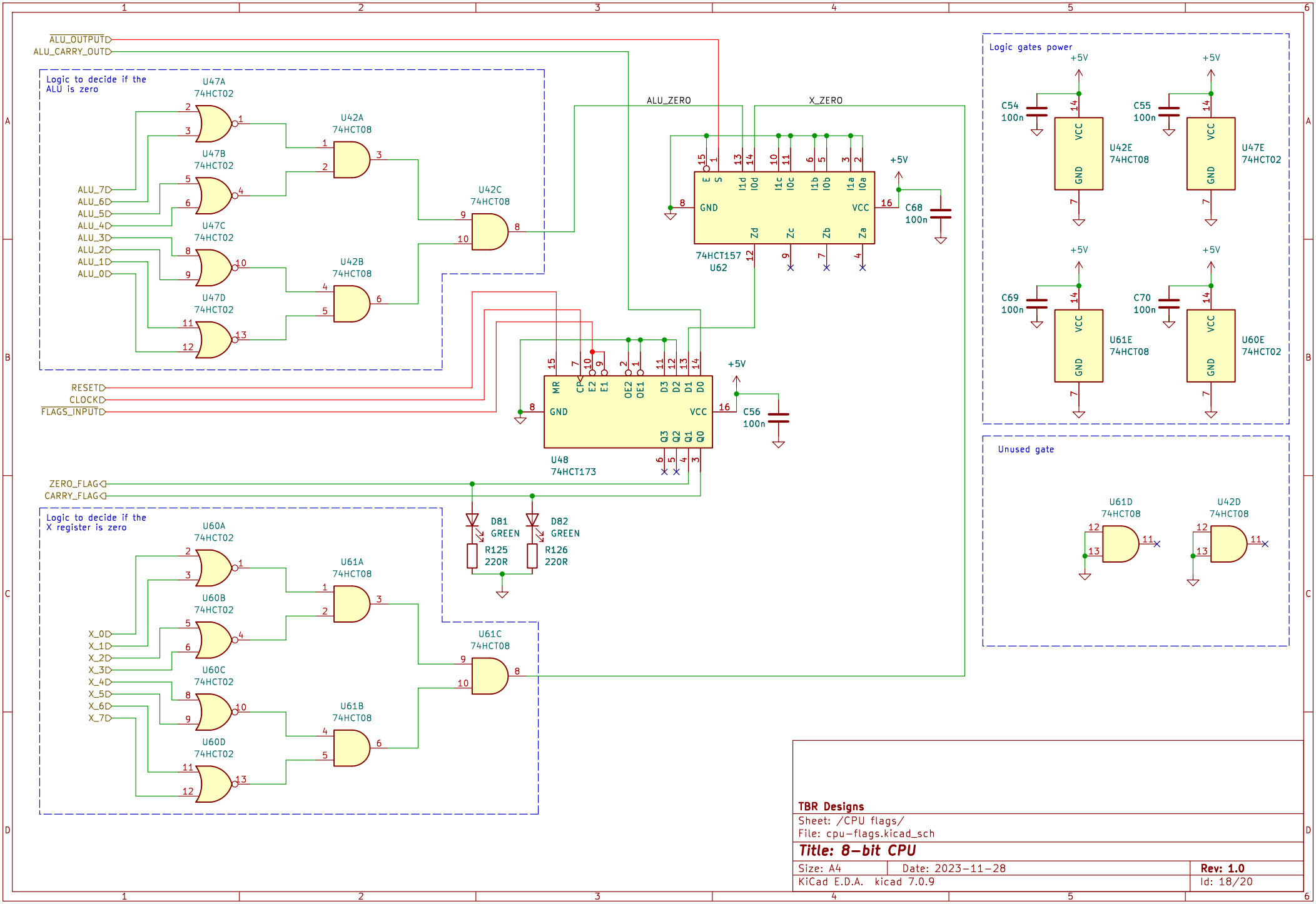


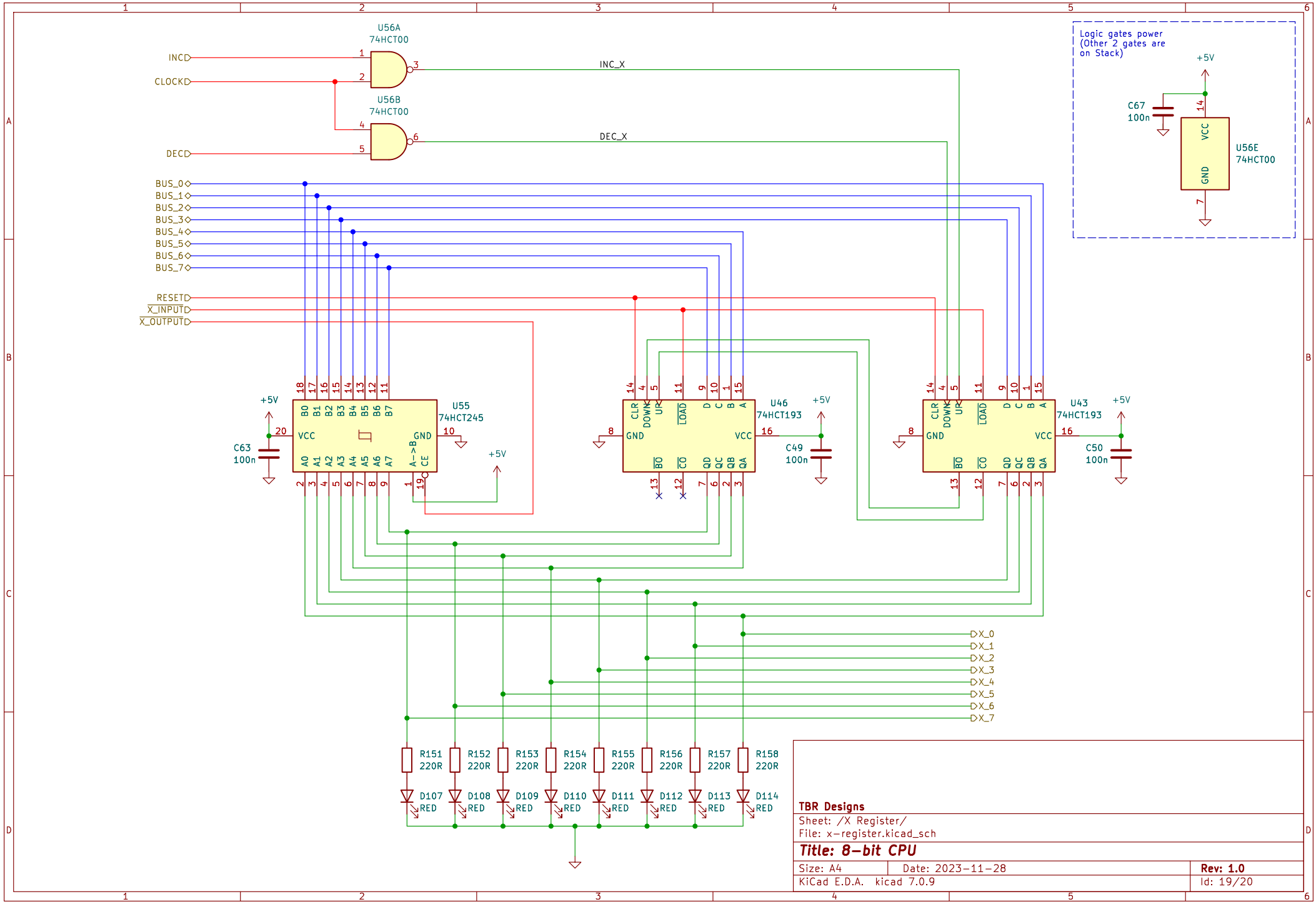
TBR Designs

Sheet: /Control logic/Right Microcode EEPROM/
File: right-microcode-eeprom.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 17/20


ALU_OUTPUT
ALU_CARRY_OUT
Logic to decide if the ALU is zero
U47A 74HCT02
U47B 74HCT02
U47C 74HCT02
U47D 74HCT02
U42A 74HCT08
U42B 74HCT08
U42C 74HCT08
ALU_7
ALU_6
ALU_5
ALU_4
ALU_3
ALU_2
ALU_1
ALU_0
ALU_ZERO
X_ZERO
E S I1d I0d I1c I0c I1b I0b I1a I0a
GND VCC
Zd Zc Zb Za
74HCT157 U62
+5V
C68 100n
RESET
CLOCK
FLAGS_INPUT
MR CP E2 E1 OE2 OE1 D3 D2 D1 D0
GND VCC
Q3 Q2 Q1 Q0
U48 74HCT173
C56 100n
ZERO_FLAG
CARRY_FLAG
D81 GREEN
D82 GREEN
R125 220R
R126 220R
Logic to decide if the X register is zero
U60A 74HCT02
U60B 74HCT02
U60C 74HCT02
U60D 74HCT02
U61A 74HCT08
U61B 74HCT08
U61C 74HCT08
X_0
X_1
X_2
X_3
X_4
X_5
X_6
X_7
Logic gates power
C54 100n
C55 100n
C69 100n
C70 100n
U42E 74HCT08
U47E 74HCT02
U61E 74HCT08
U60E 74HCT02
VCC GND
Unused gate
U61D 74HCT08
U42D 74HCT08
TBR Designs
Sheet: /CPU flags/
File: cpu-flags.kicad_sch
Title: 8-bit CPU
Size: A4
Date: 2023-11-28
Rev: 1.0
KiCad E.D.A. kicad 7.0.9
Id: 18/20



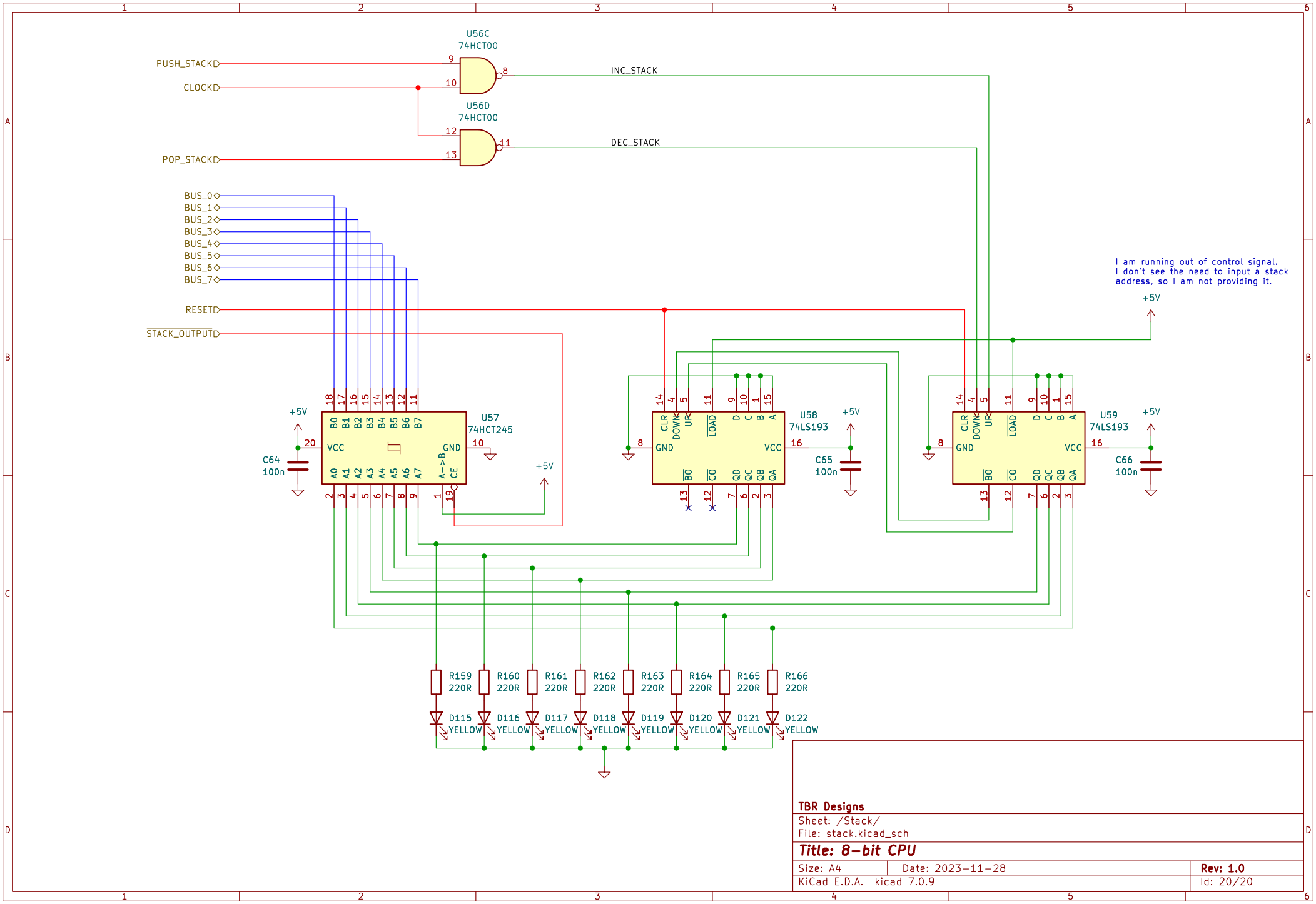
TBR Designs

Sheet: /X Register/

File: x-register.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 19/20



TBR Designs

Sheet: /Stack/

File: stack.kicad_sch

Title: 8-bit CPU

Size: A4	Date: 2023-11-28	**Rev: 1.0**
KiCad E.D.A. kicad 7.0.9		Id: 20/20