

TBR Designs

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File: 8-bit-cpu.kicad_sch

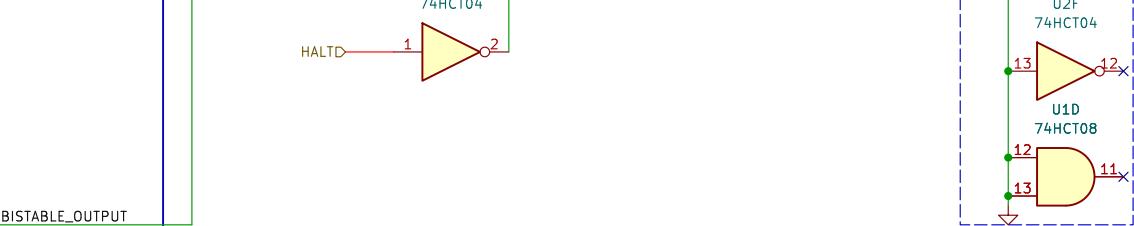
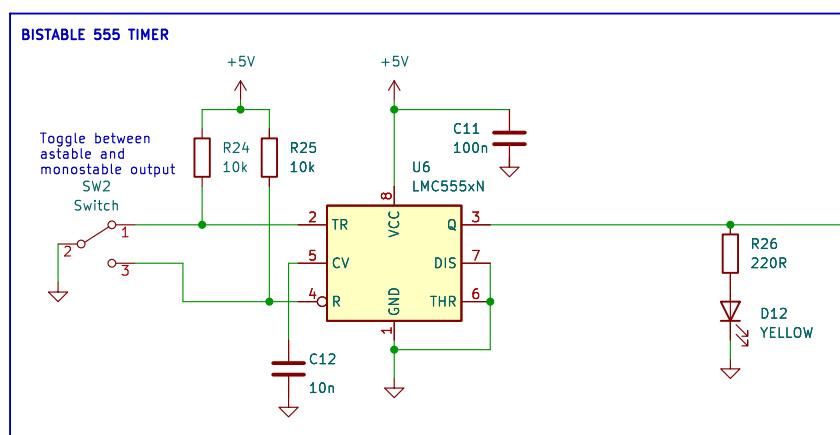
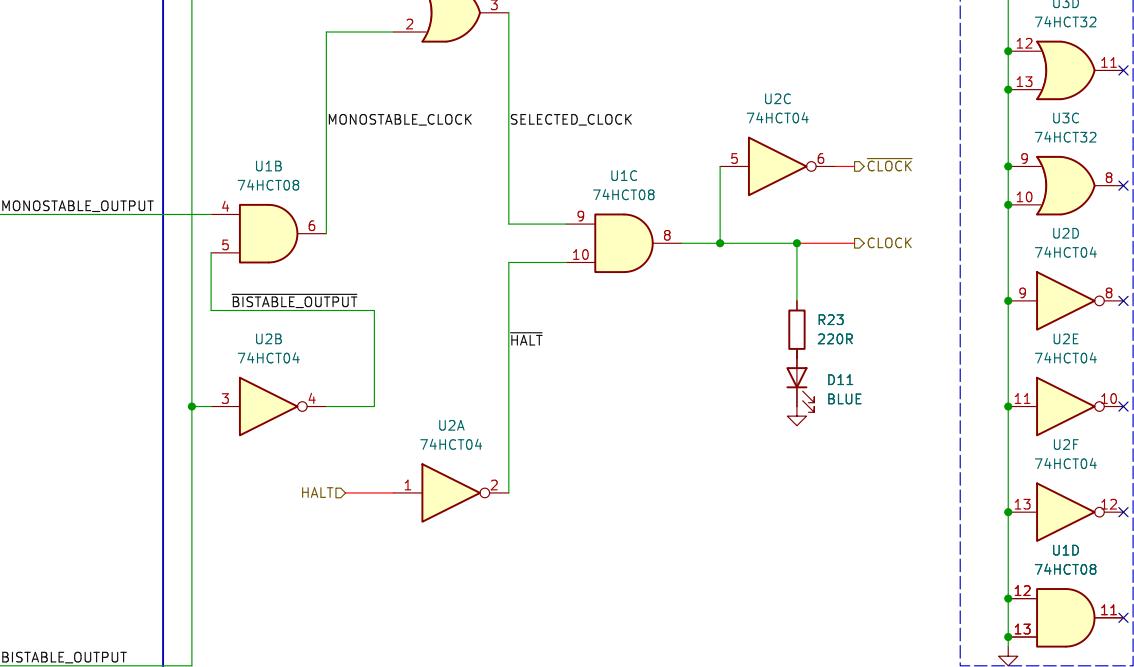
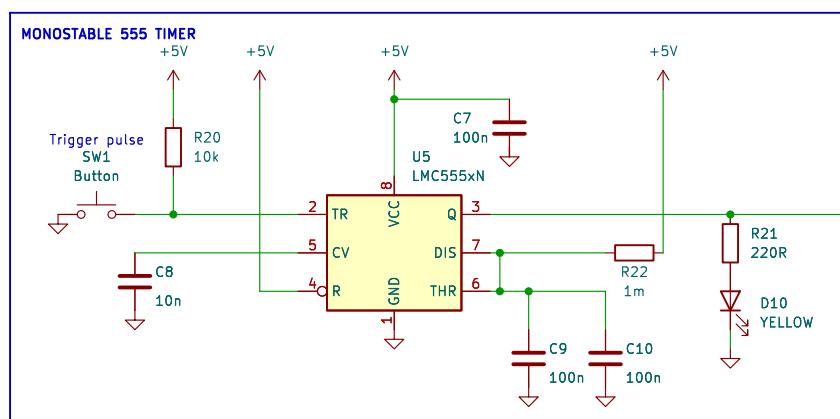
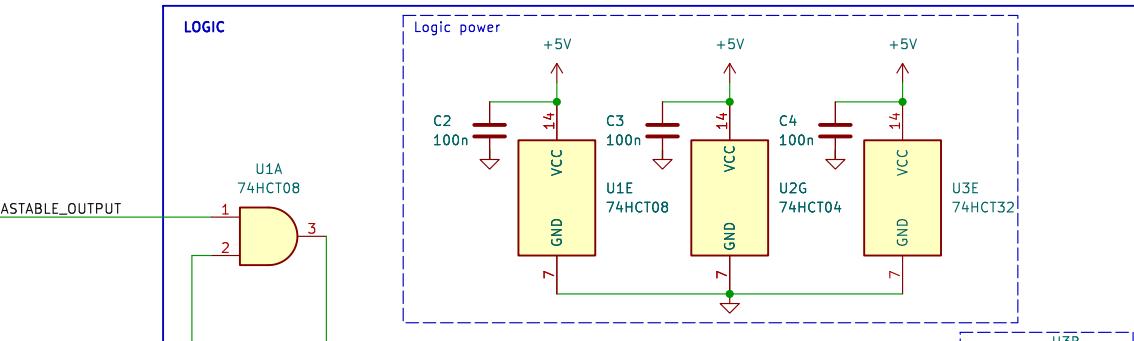
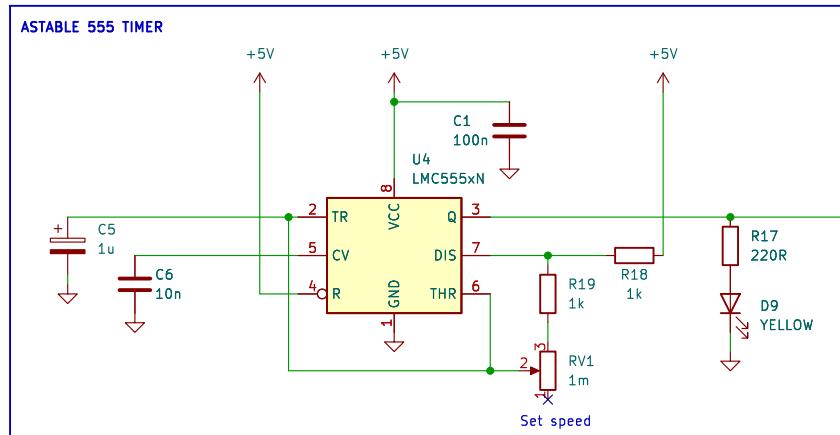
Title: 8-bit CPU

Size: A3 | Date: 2023-11-28

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Rev: 1.0

Id: 1/21



Provides a clock pulse and inverted clock pulse.
Speed can be set with the potentiometer.
Manual pulse can be chosen with the switch and pulsed with the button.
If HALT is HIGH no pulse is outputted.

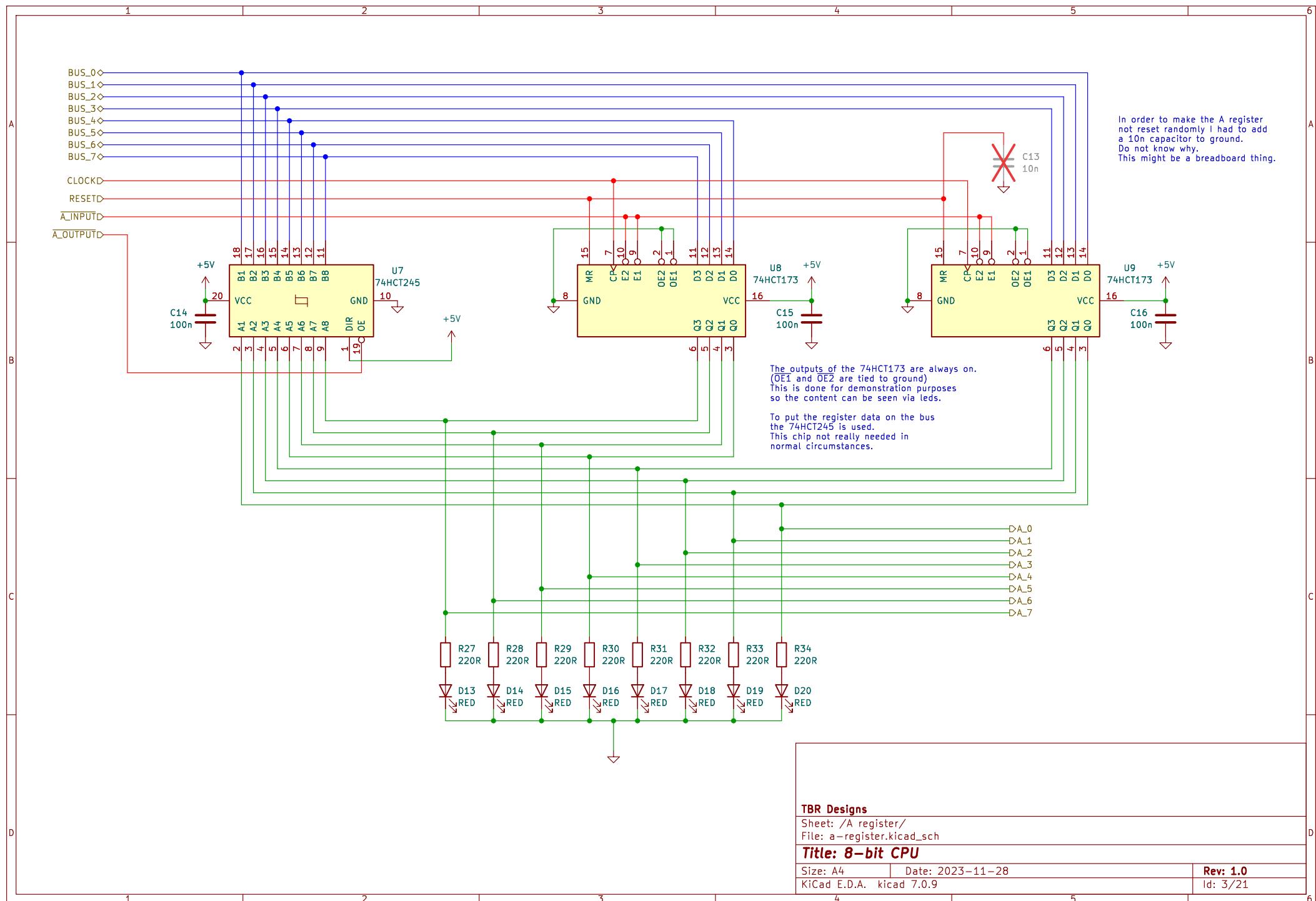
TBR Designs

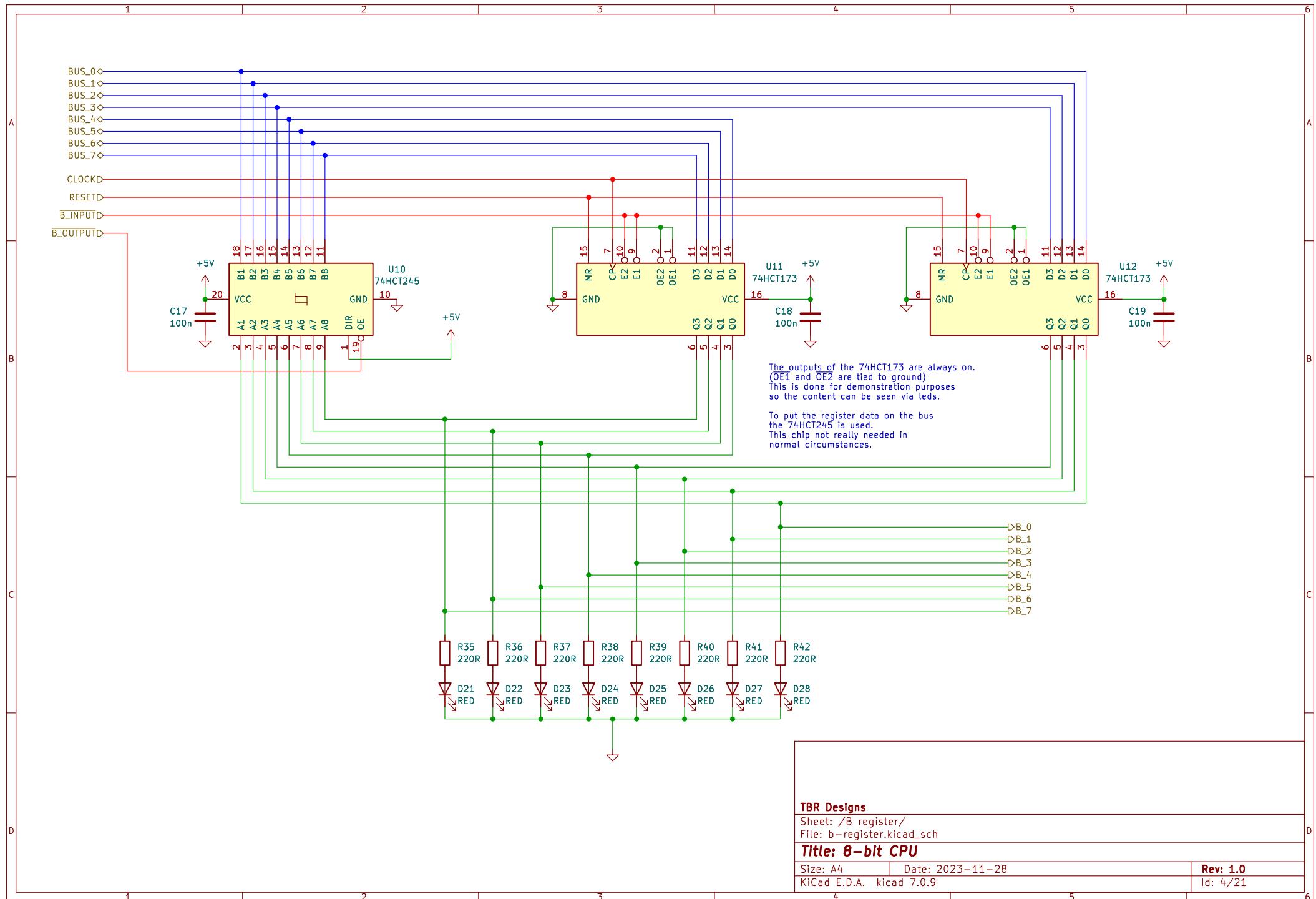
Sheet: /Clock/
File: clock.kicad_sch

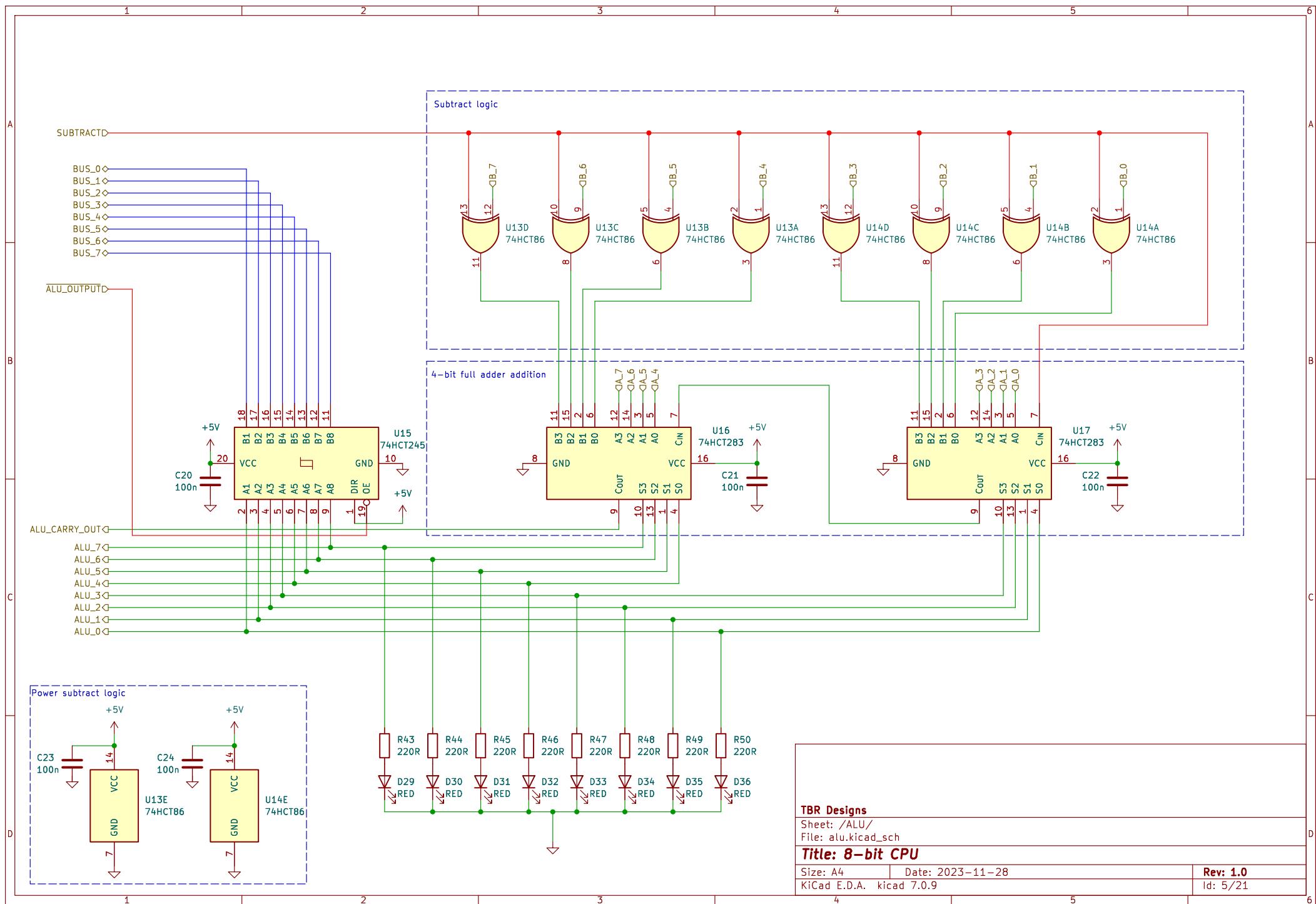
Title: 8-bit CPU

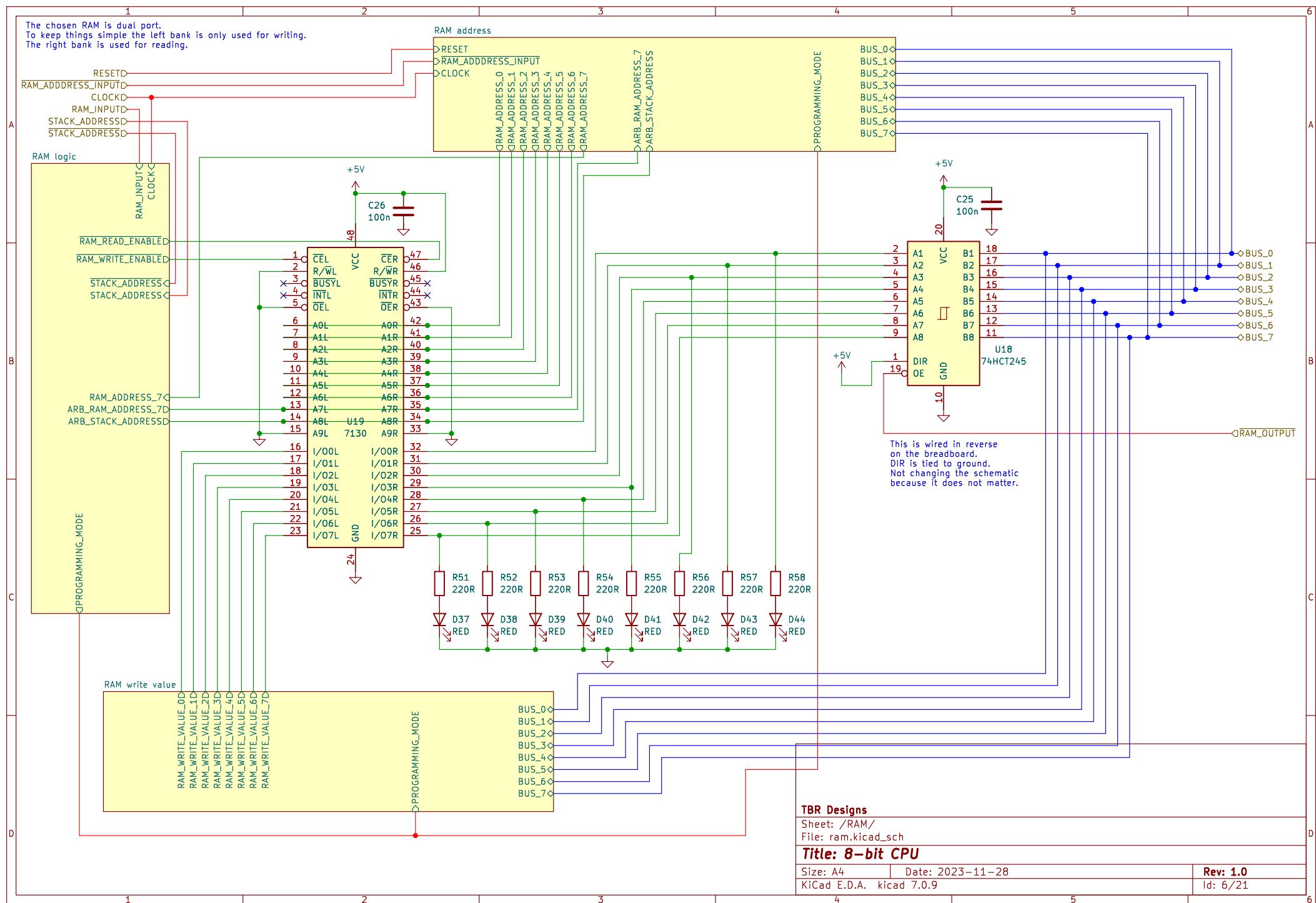
Size: A4 | Date: 2023-11-28
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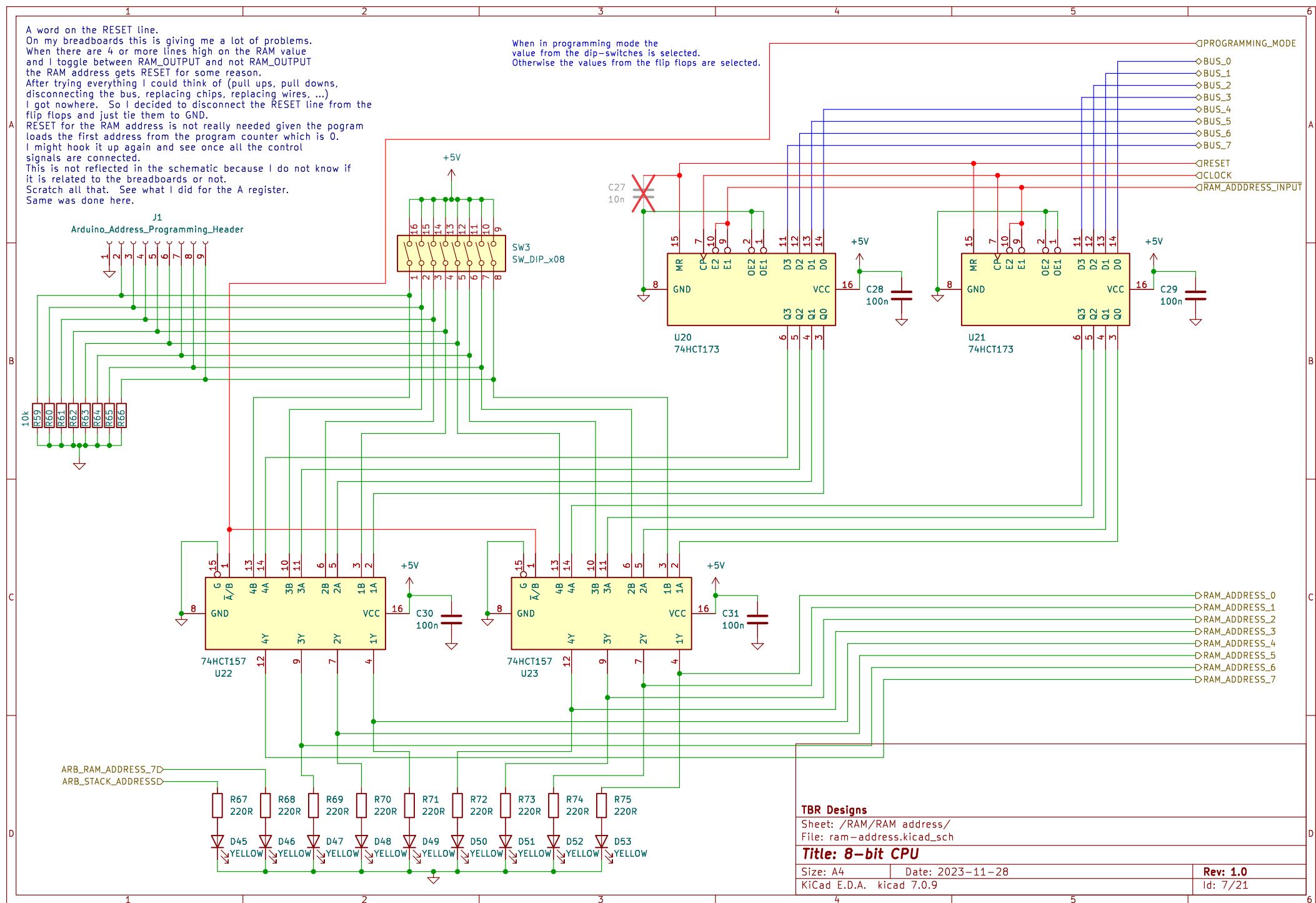
Rev: 1.0
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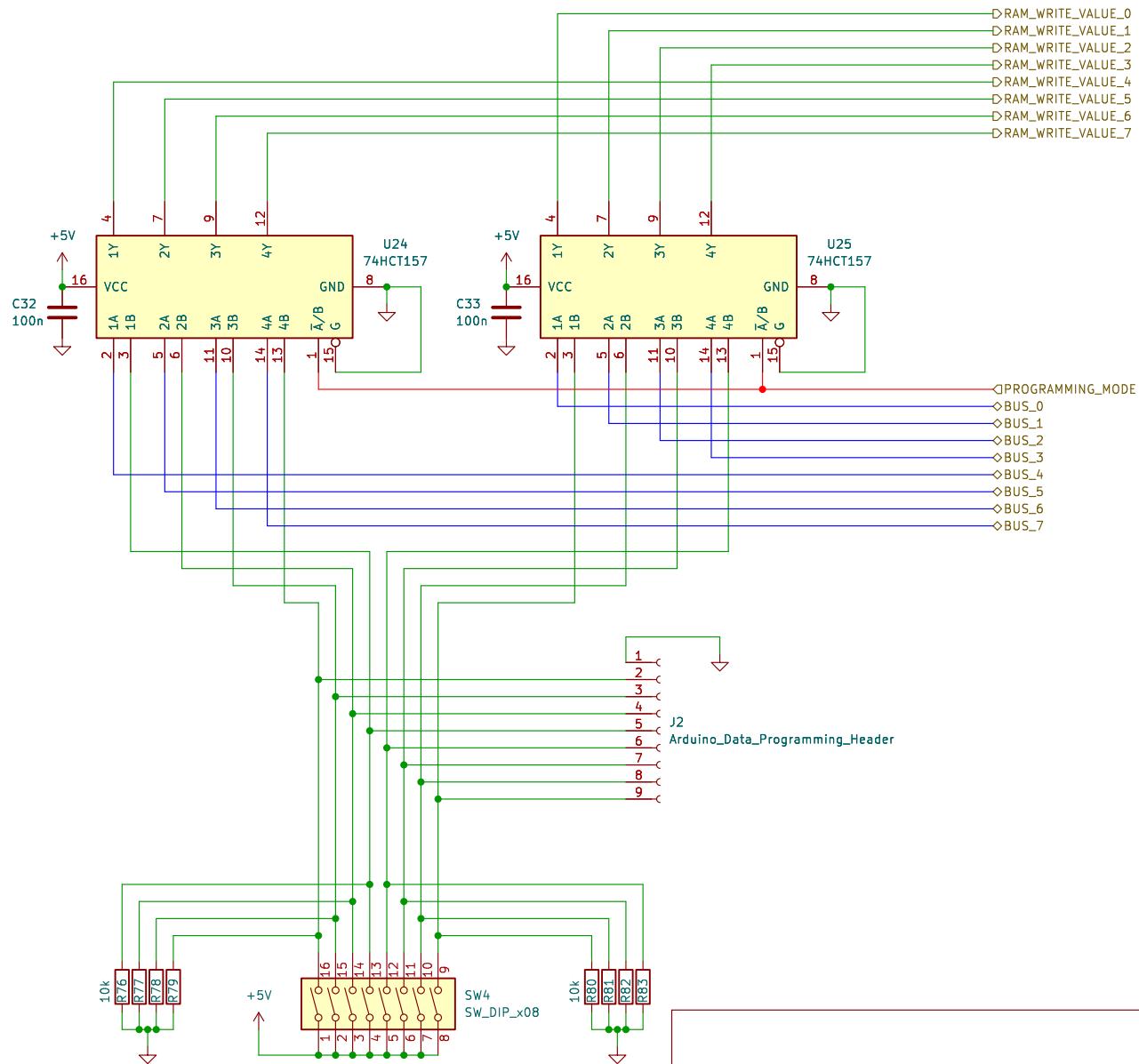








When in programming mode the value from the dip-switches is selected. Otherwise the value from the bus is selected.



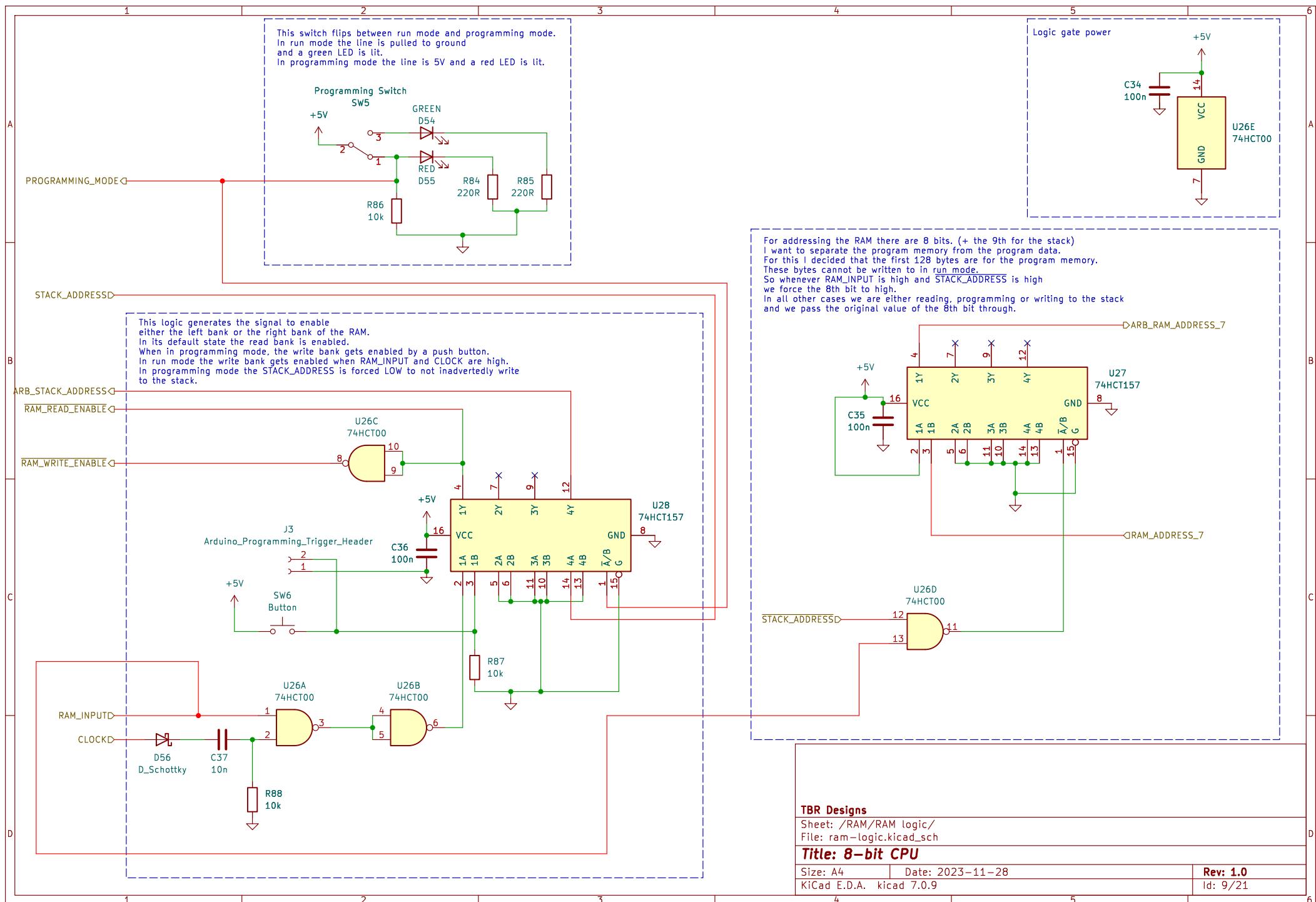
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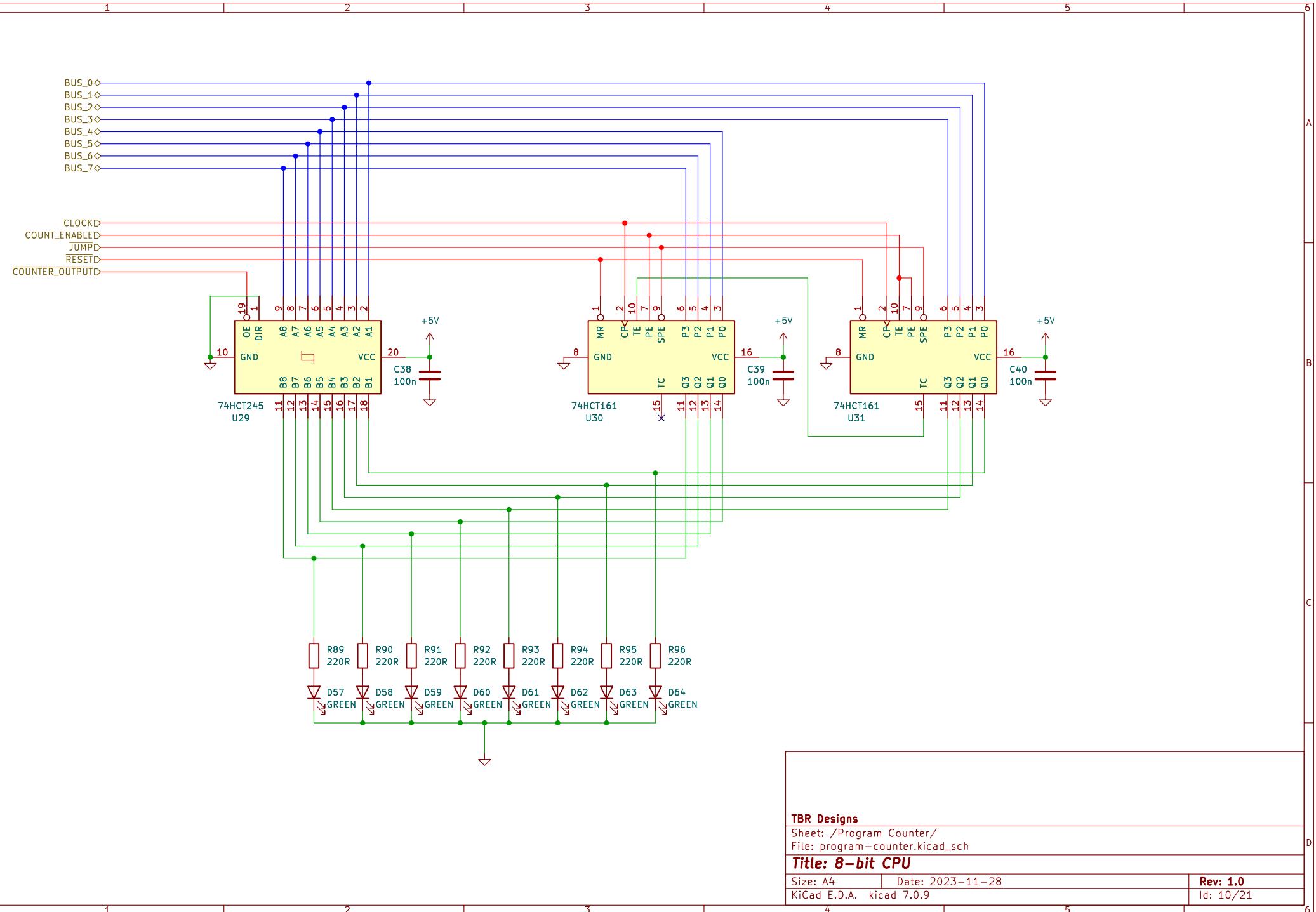
Sheet: /RAM/RAM write value/
File: ram-write-value.kicad_sch

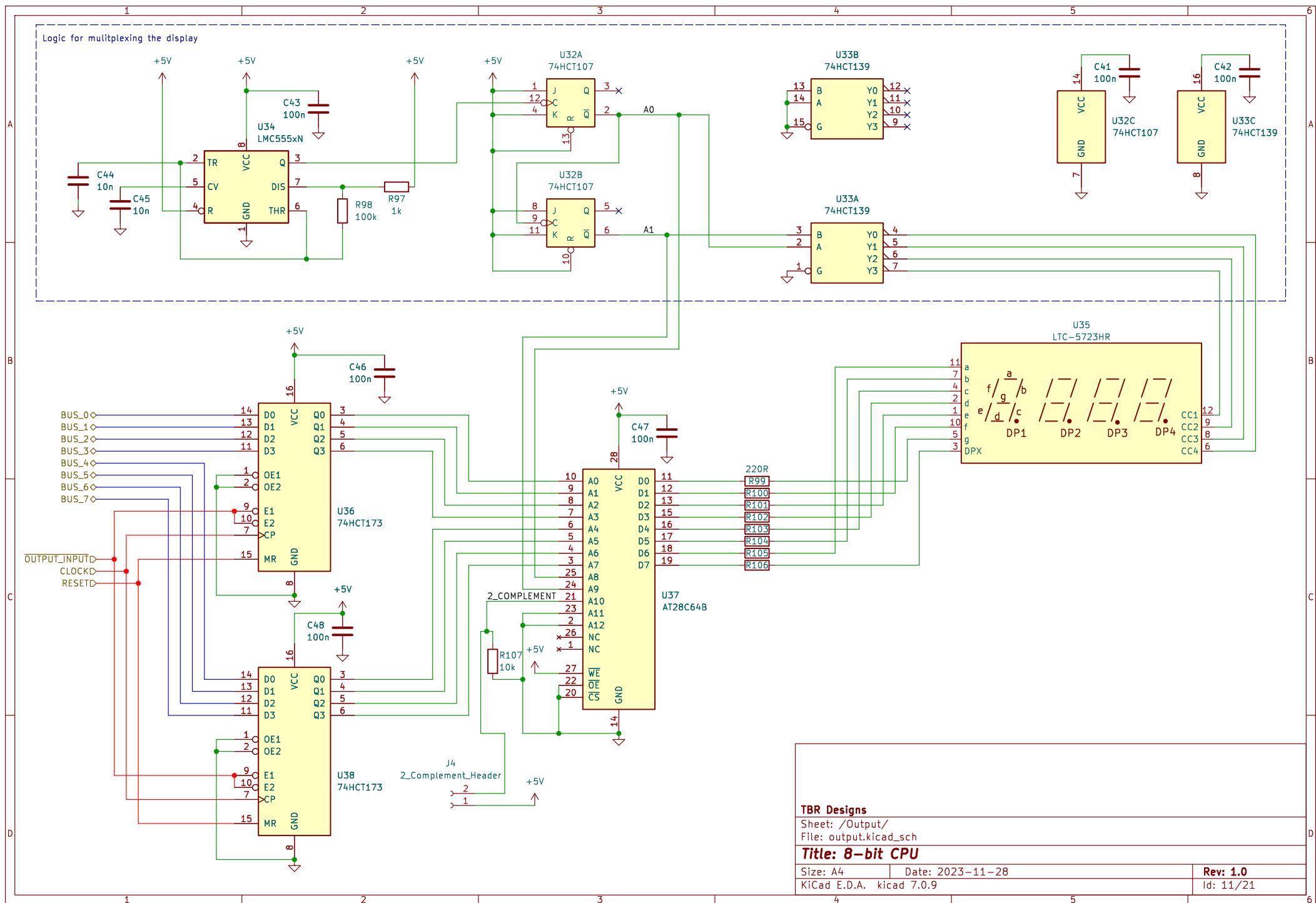
Title: 8-bit CPU

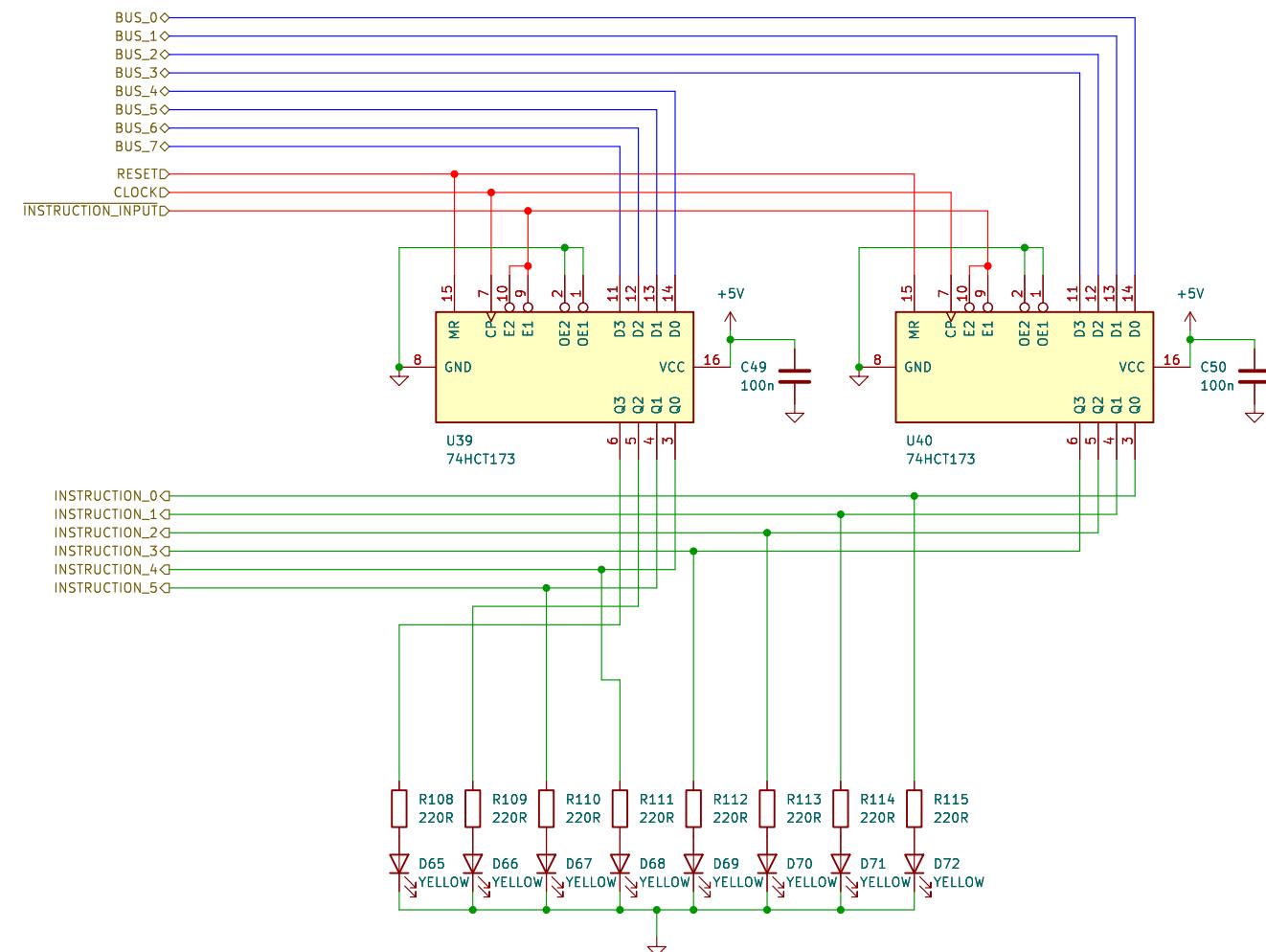
Size: A4 Date: 2023-11-28
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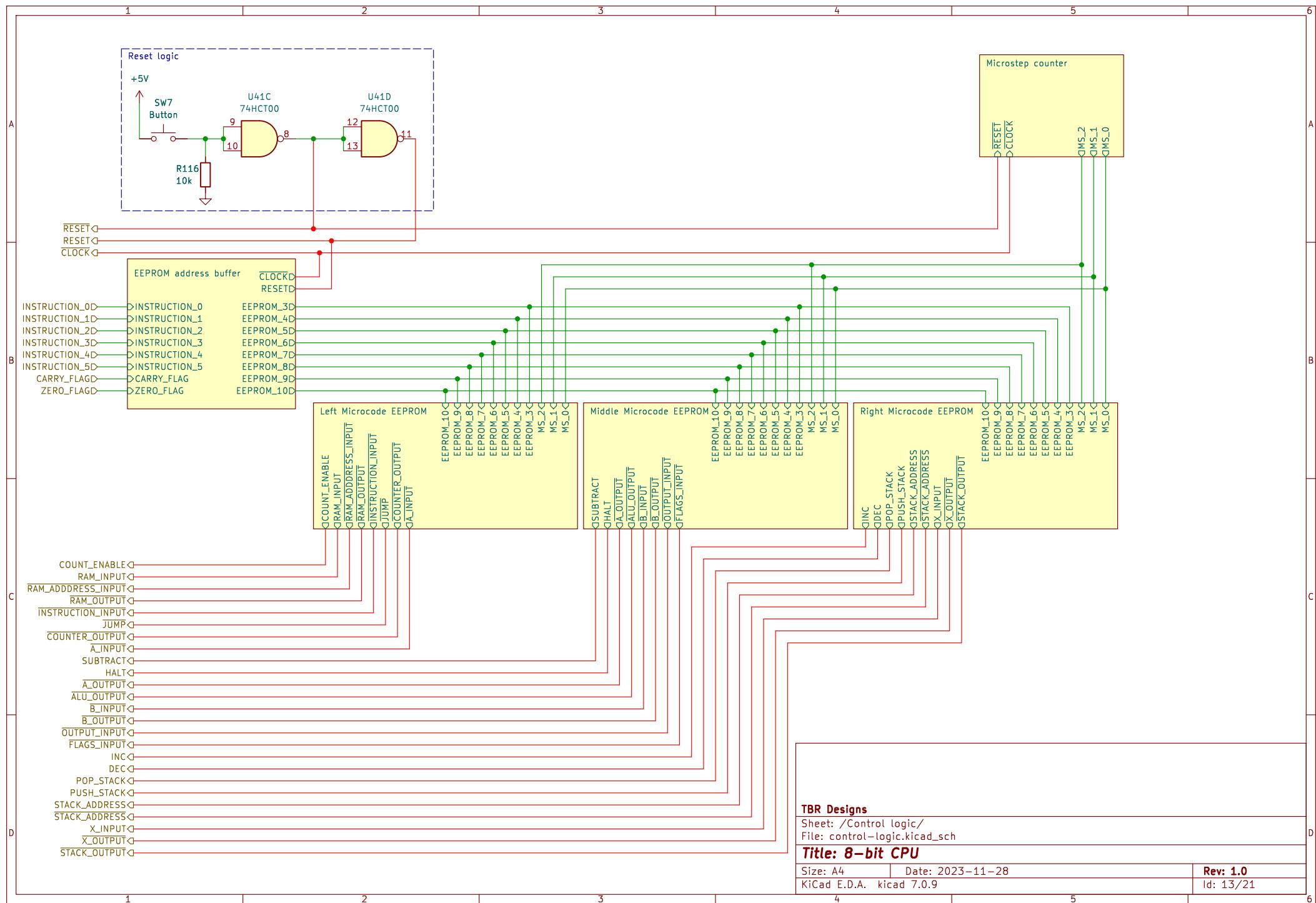
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Sheet: /Instruction register/
File: instruction-register.kicad_sch

Title: 8-bit CPU

Size: A4 | Date: 2023-11-28
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This address buffer triggers on the inverted **CLOCK**. I had to include this because during an address transition the outputs of the EEPROM's are undefined. They vary wildly and random actions were triggered briefly. Making the address change on the inverted **CLOCK** seems to solve this issue because all of the other logic is triggered on the **CLOCK**.

A

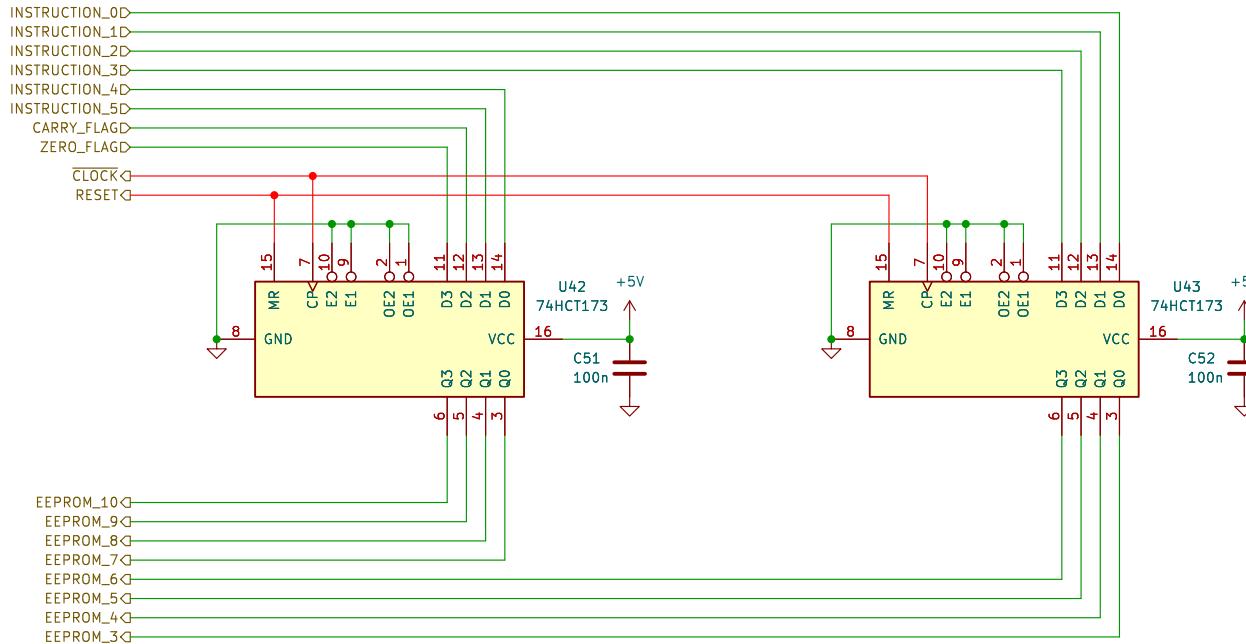
A

B

B

1

C



TBR Design

Sheet: /Control logic/EEPROM address buffer/
File: eeprom-address-buffer.kicad_sch

Title: 8-bit CPU

Size: A4 Date: 2023-11-28
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