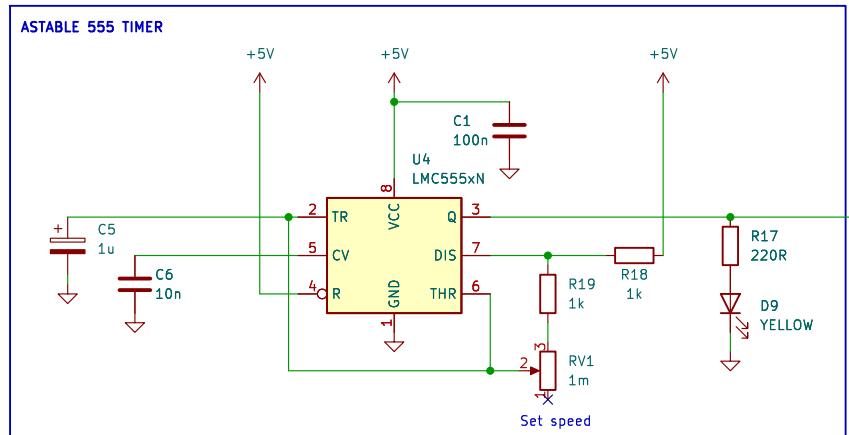


#### TBR Designs

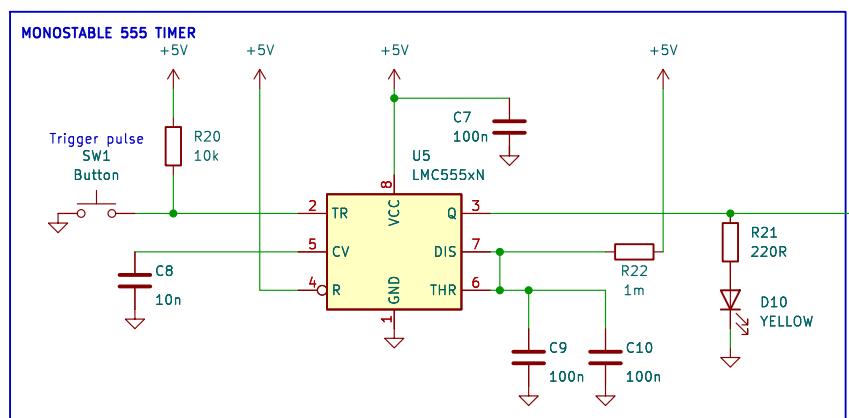
Sheet: /  
File: 8-bit-cpu.kicad\_sch  
**Title: 8-bit CPU**

Size: A3 | Date: 2023-11-28  
KiCad E.D.A. kicad 7.0.9

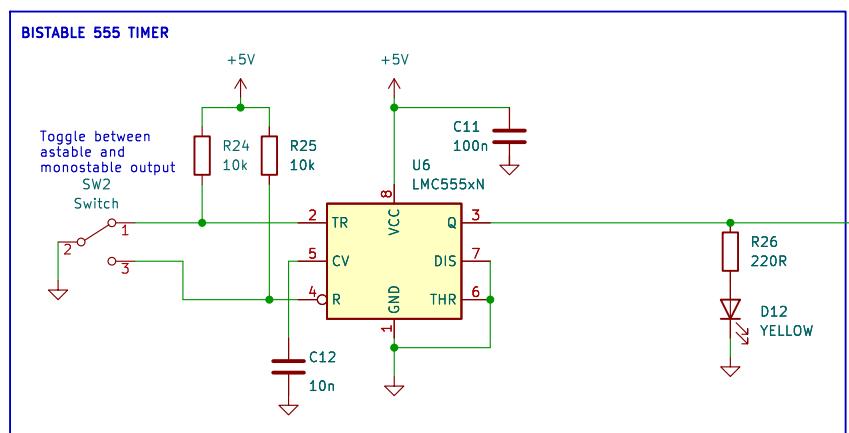
Rev: 1.0  
Id: 1/21



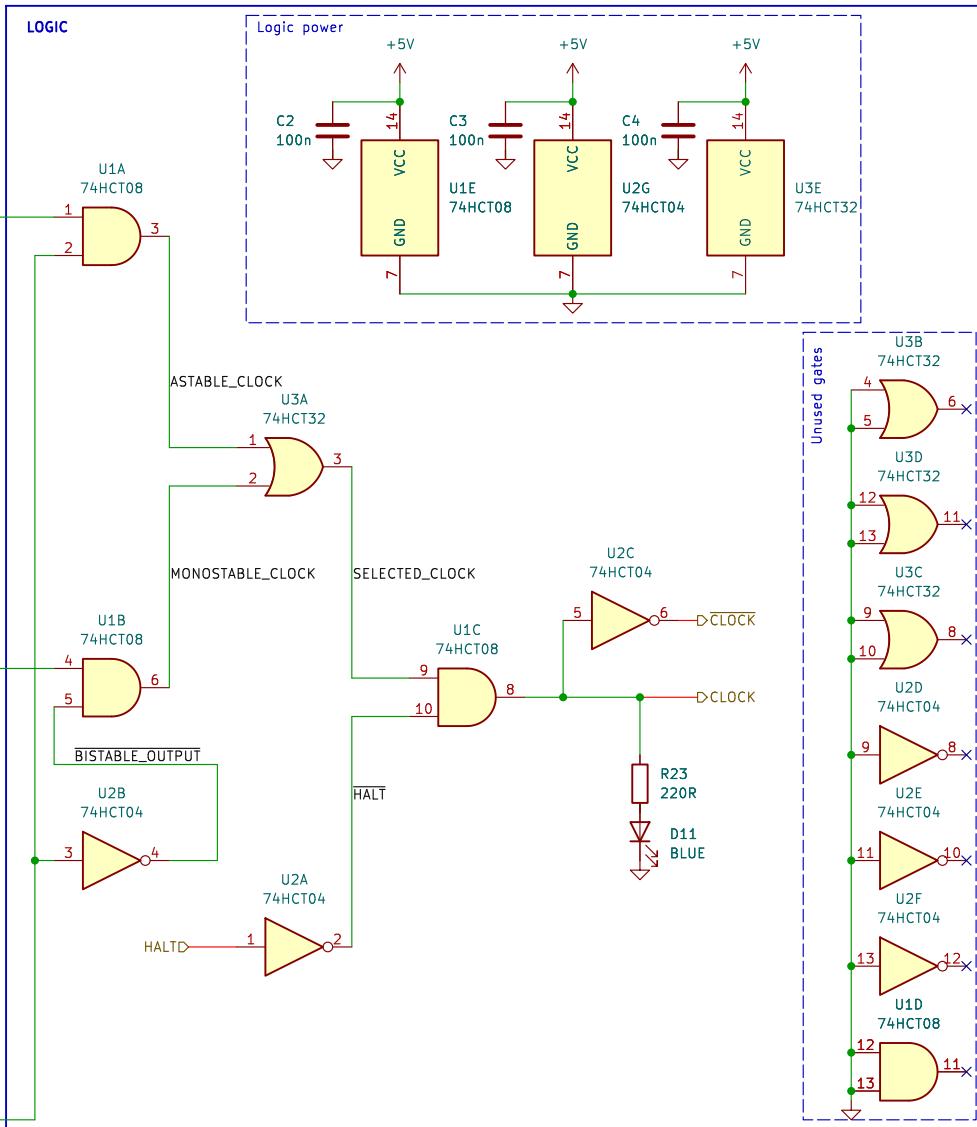
ASTABLE\_OUTPUT



MONOSTABLE\_OUTPUT



BISTABLE\_OUTPUT



Provides a clock pulse and inverted clock pulse.  
Speed can be set with the potentiometer.  
Manual pulse can be chosen with the switch and pulsed with the button.  
If HALT is HIGH no pulse is outputted.

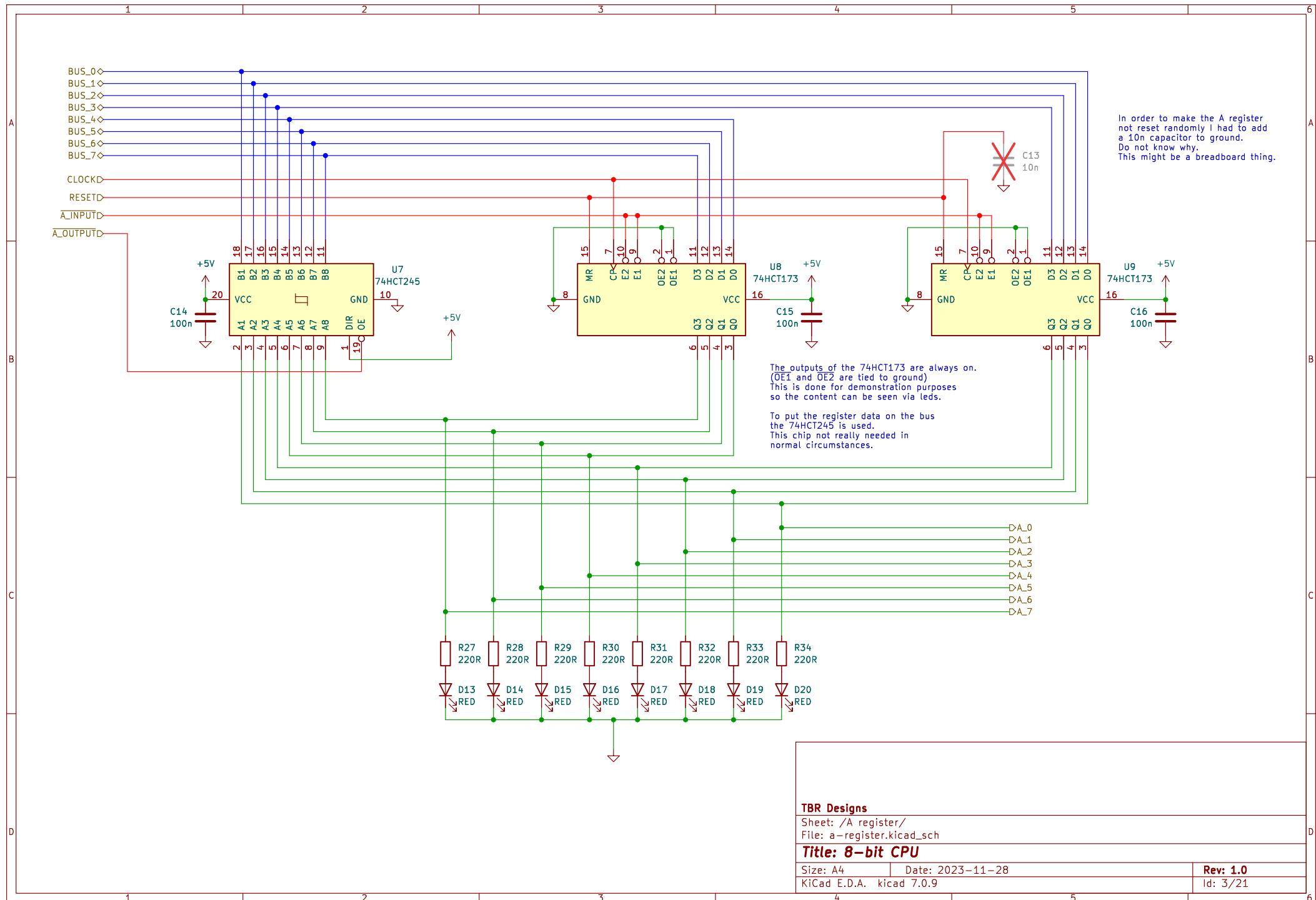
#### TBR Designs

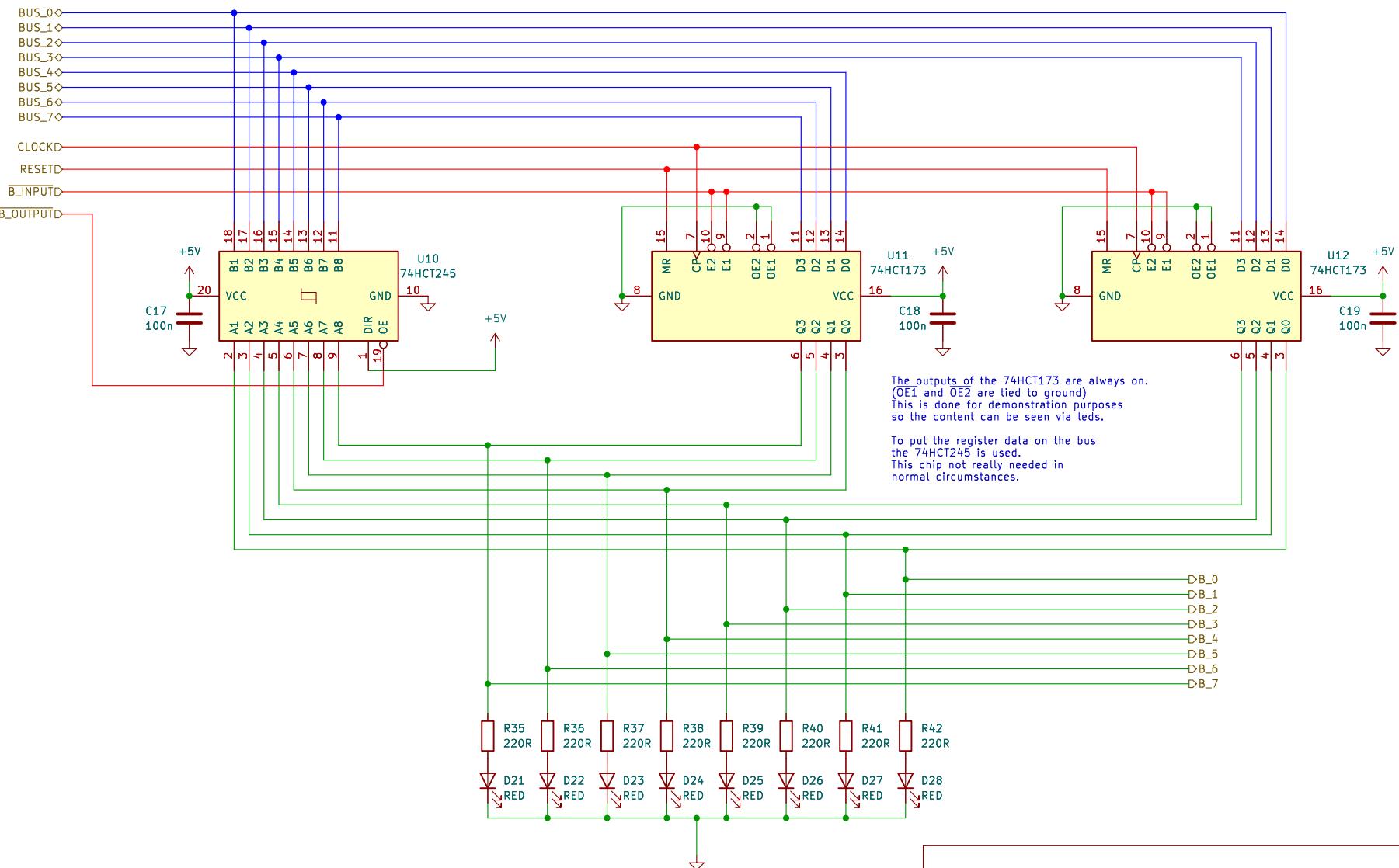
Sheet: /Clock/  
File: clock.kicad\_sch

**Title: 8-bit CPU**

Size: A4 Date: 2023-11-28  
KiCad E.D.A. kicad 7.0.9

Rev: 1.0  
Id: 2/21





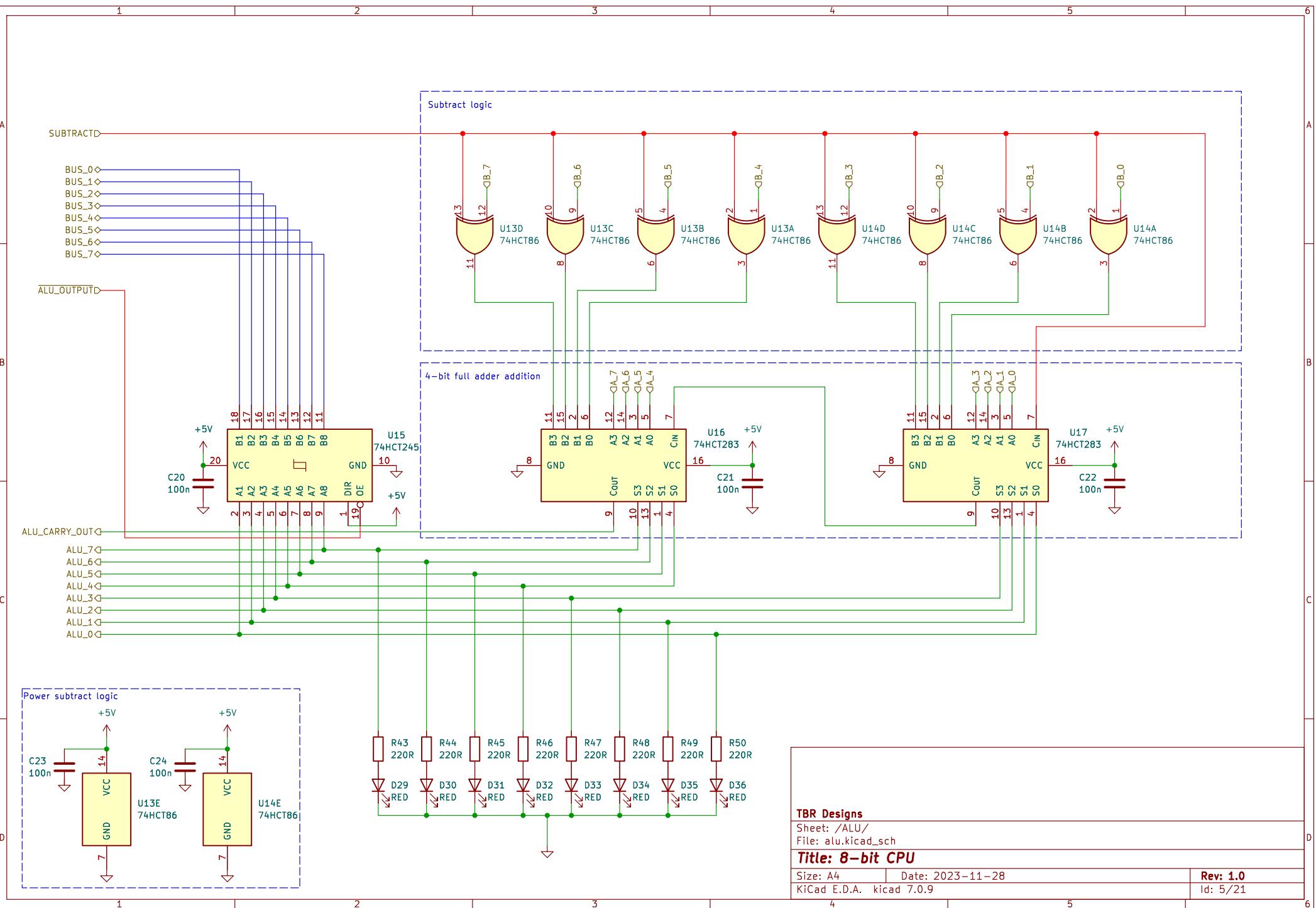
#### TBR Designs

Sheet: /B register/  
File: b-register.kicad\_sch

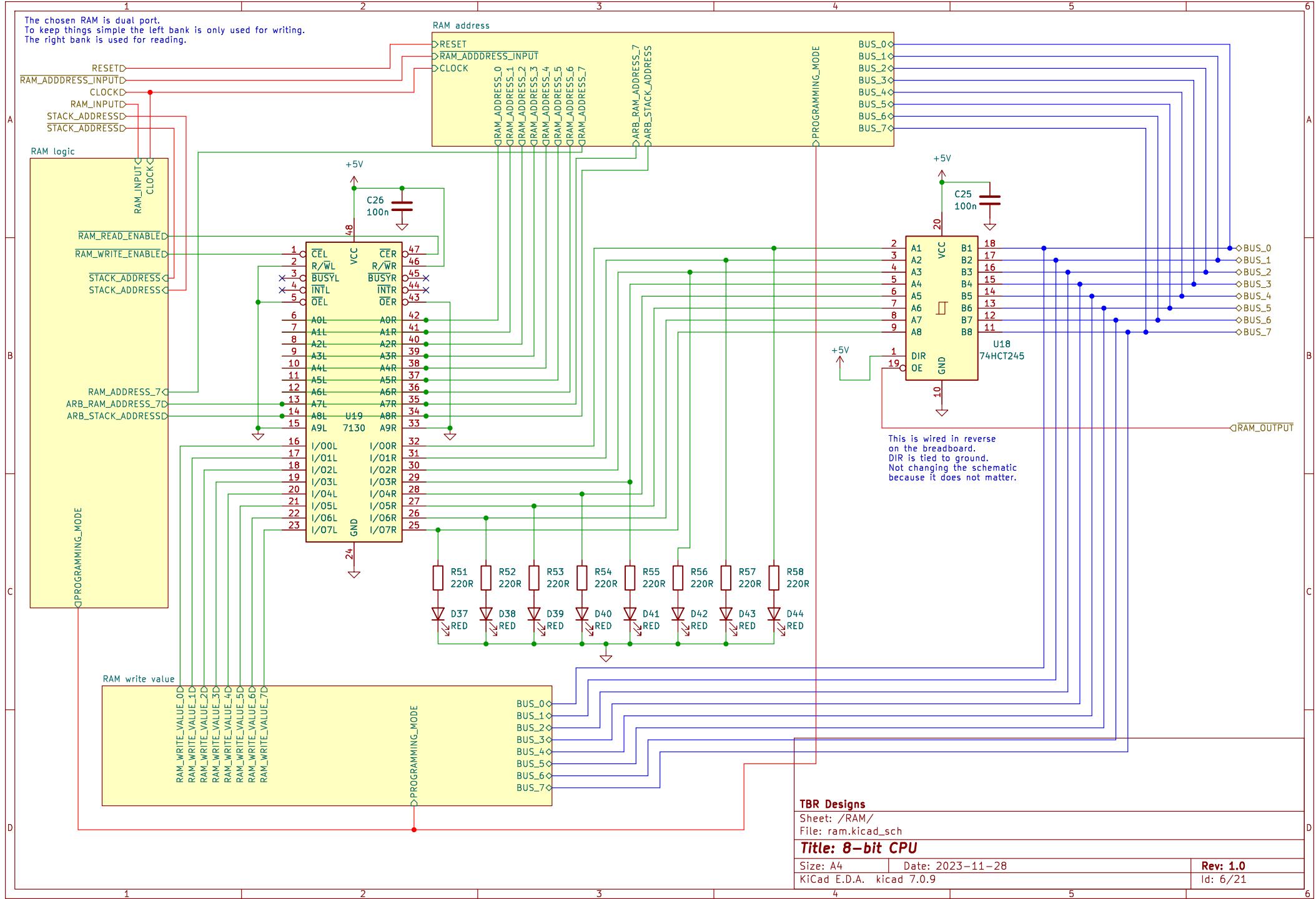
**Title: 8-bit CPU**

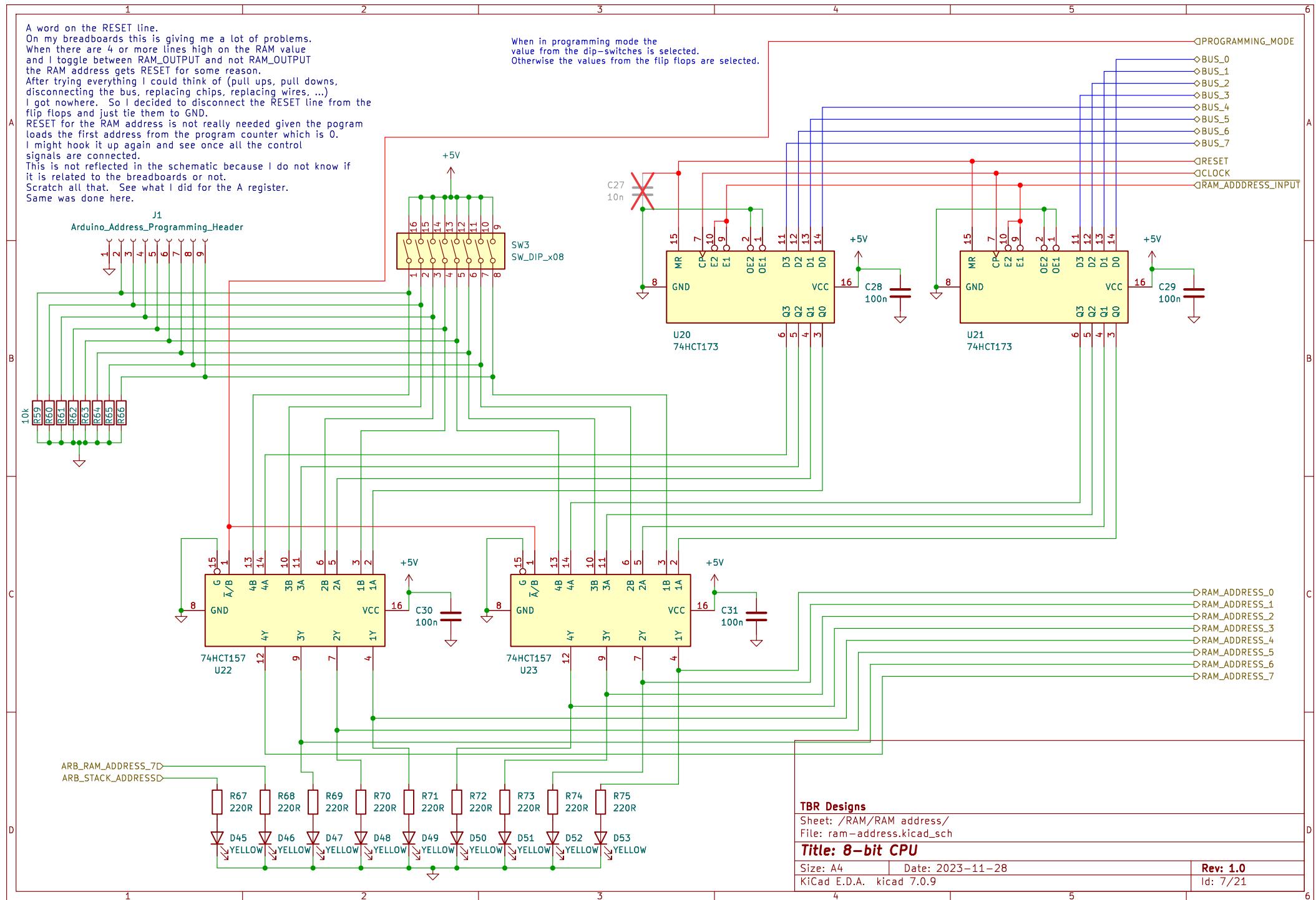
Size: A4 | Date: 2023-11-28  
KiCad E.D.A. kicad 7.0.9

**Rev: 1.0**  
Id: 4/21



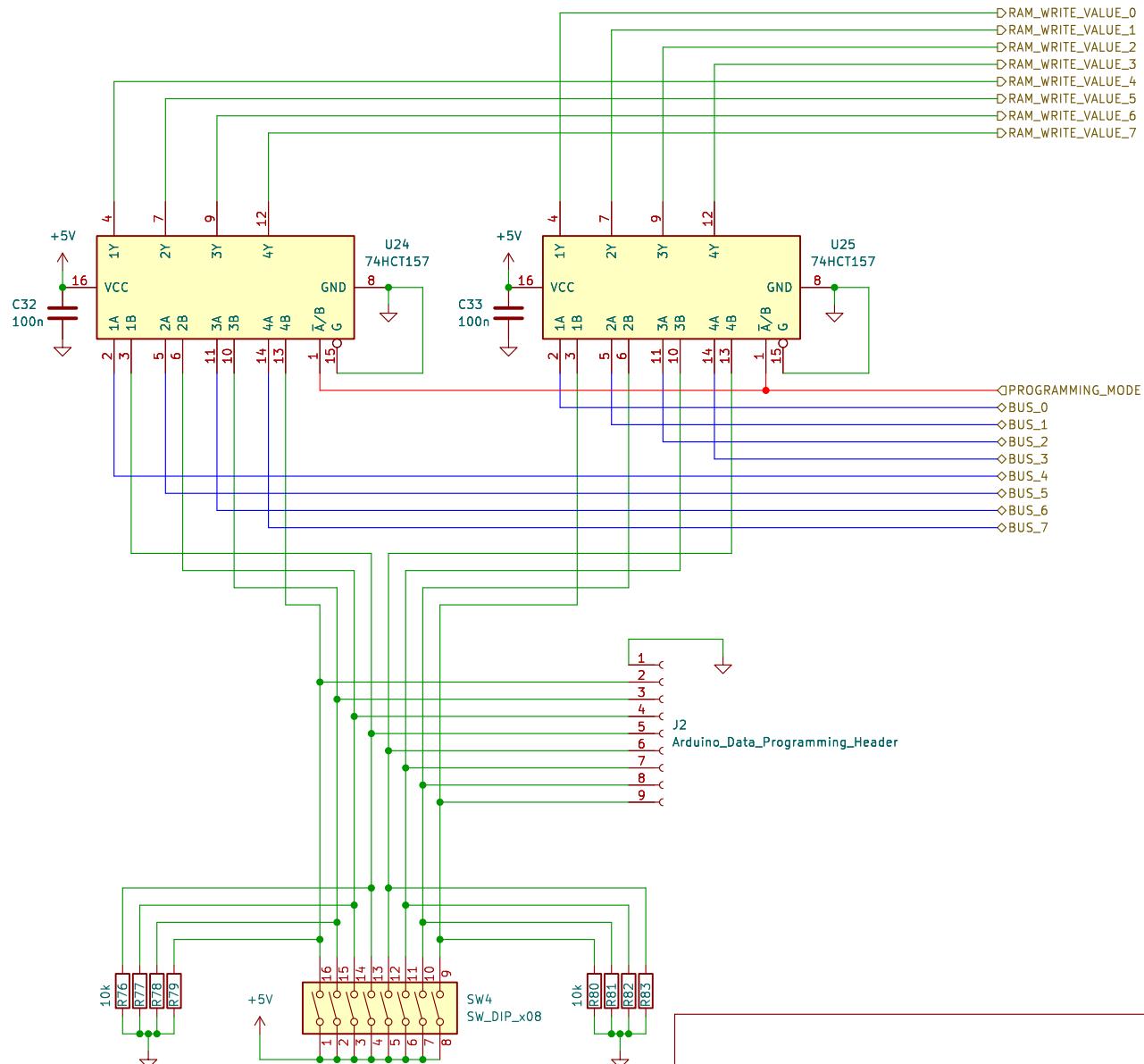
The chosen RAM is dual port.  
To keep things simple the left bank is only used for writing.  
The right bank is used for reading.





1 2 3 4 5 6

When in programming mode the value from the dip-switches is selected.  
Otherwise the value from the bus is selected.



#### TBR Designs

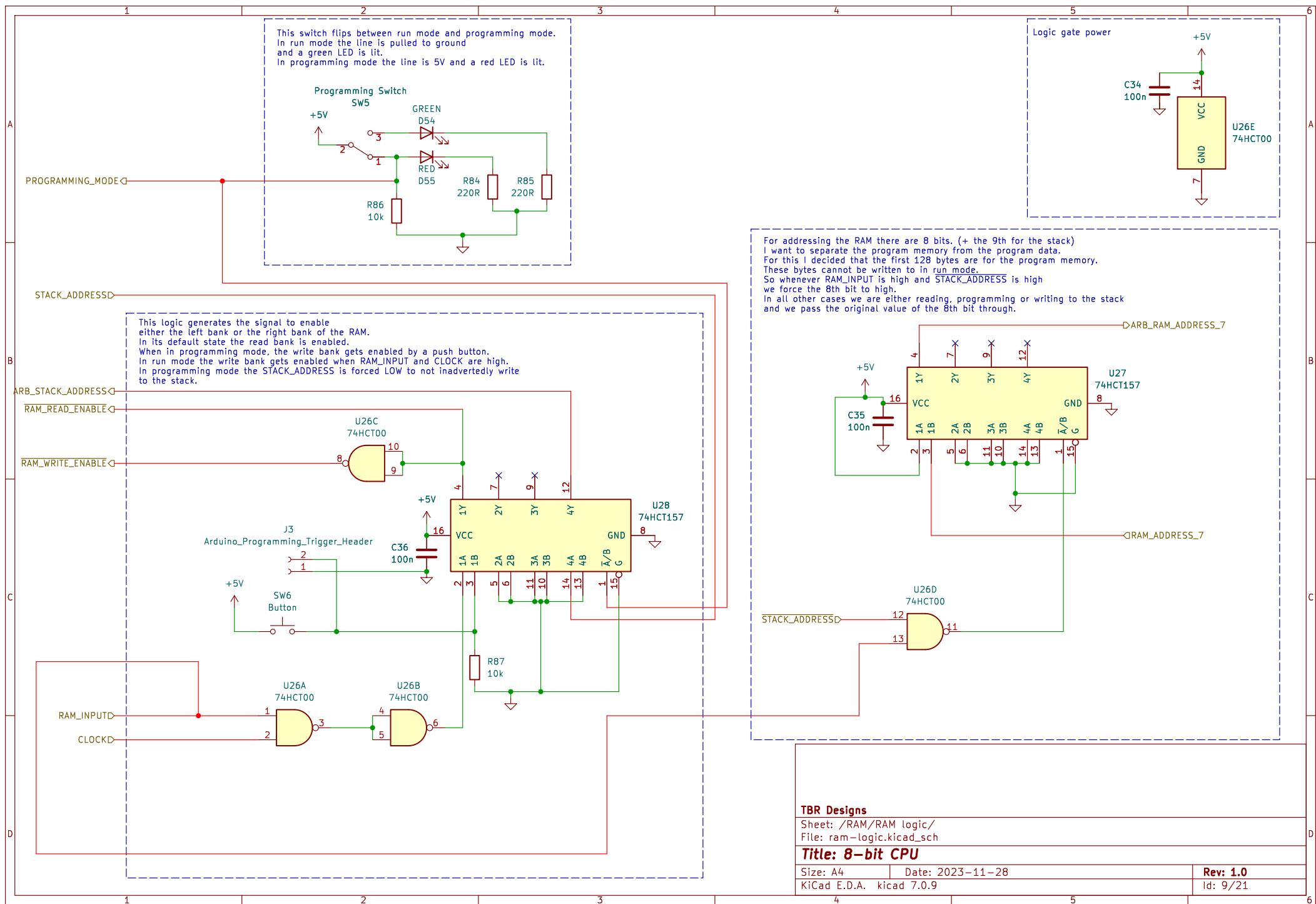
Sheet: /RAM/RAM write value/  
File: ram-write-value.kicad\_sch

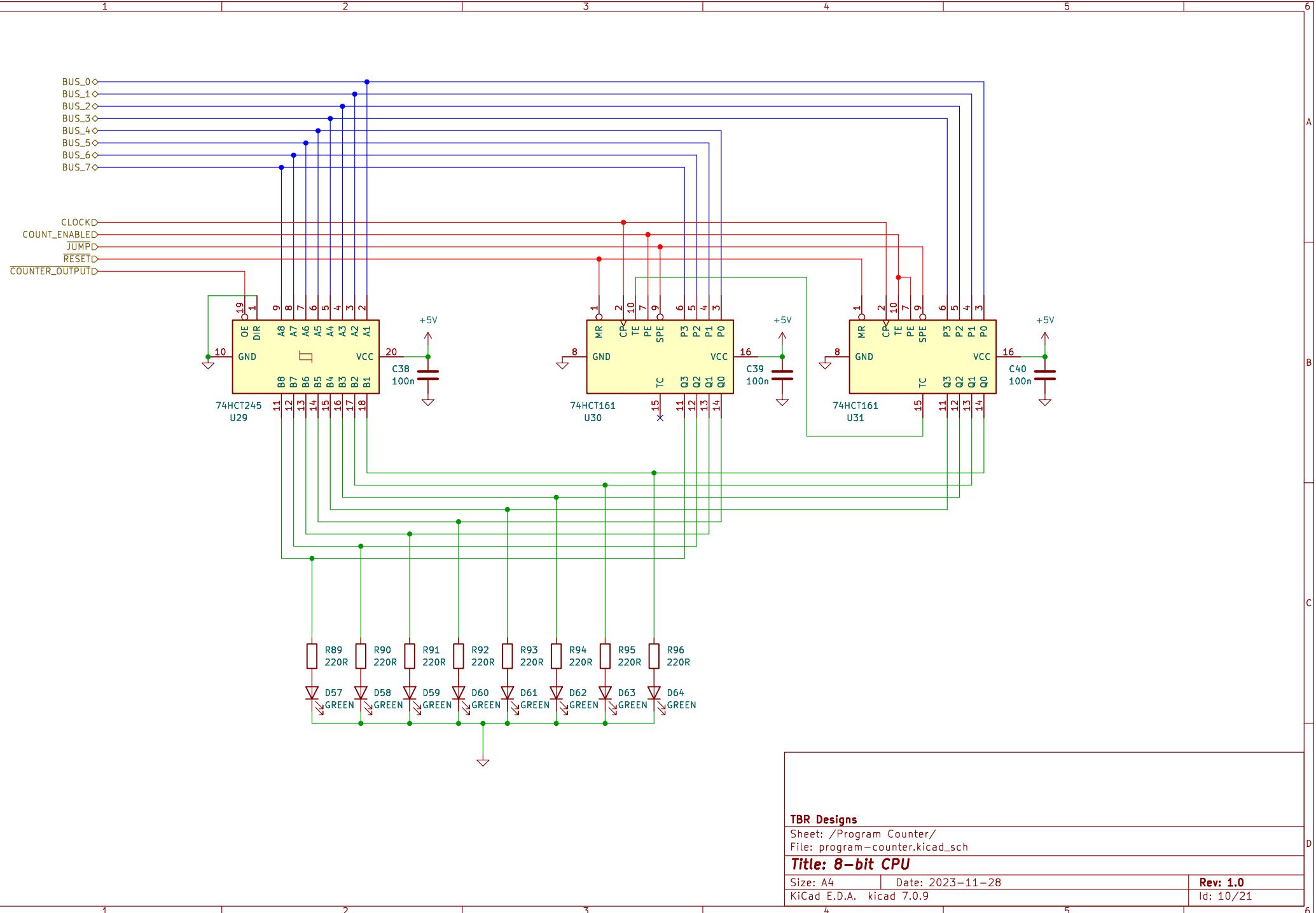
**Title: 8-bit CPU**

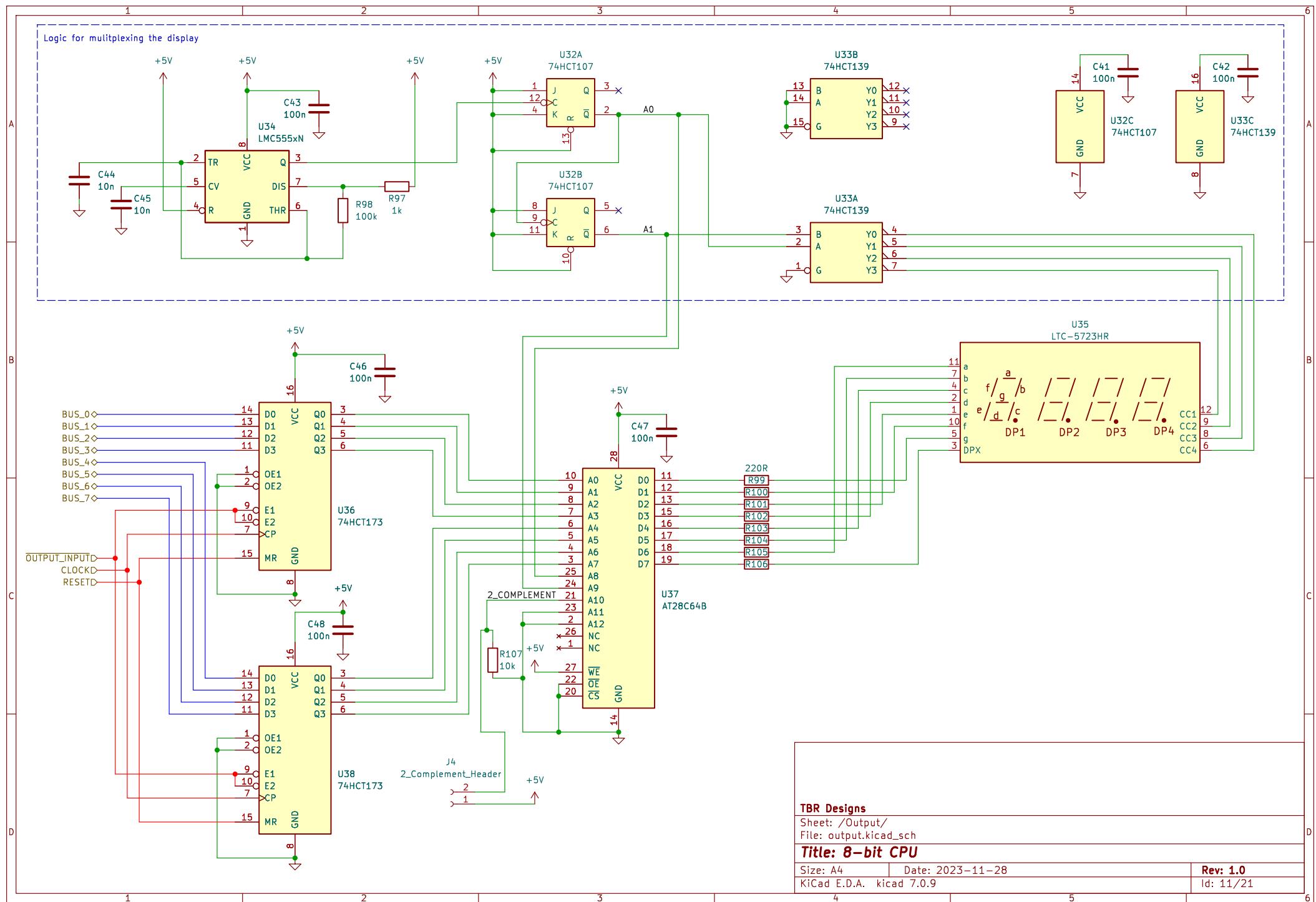
Size: A4 Date: 2023-11-28  
KiCad E.D.A. kicad 7.0.9

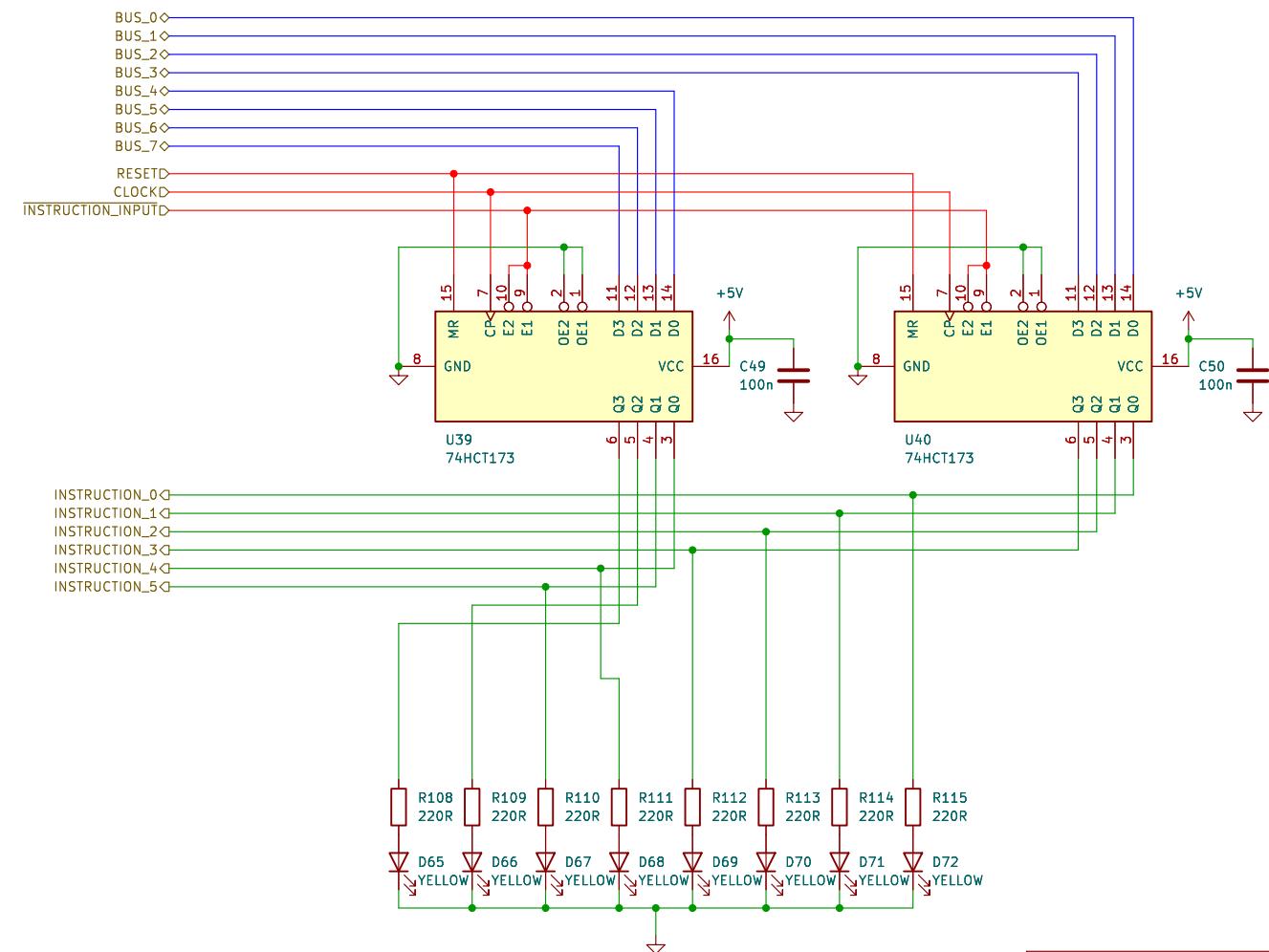
Rev: 1.0  
Id: 8/21

1 2 3 4 5 6









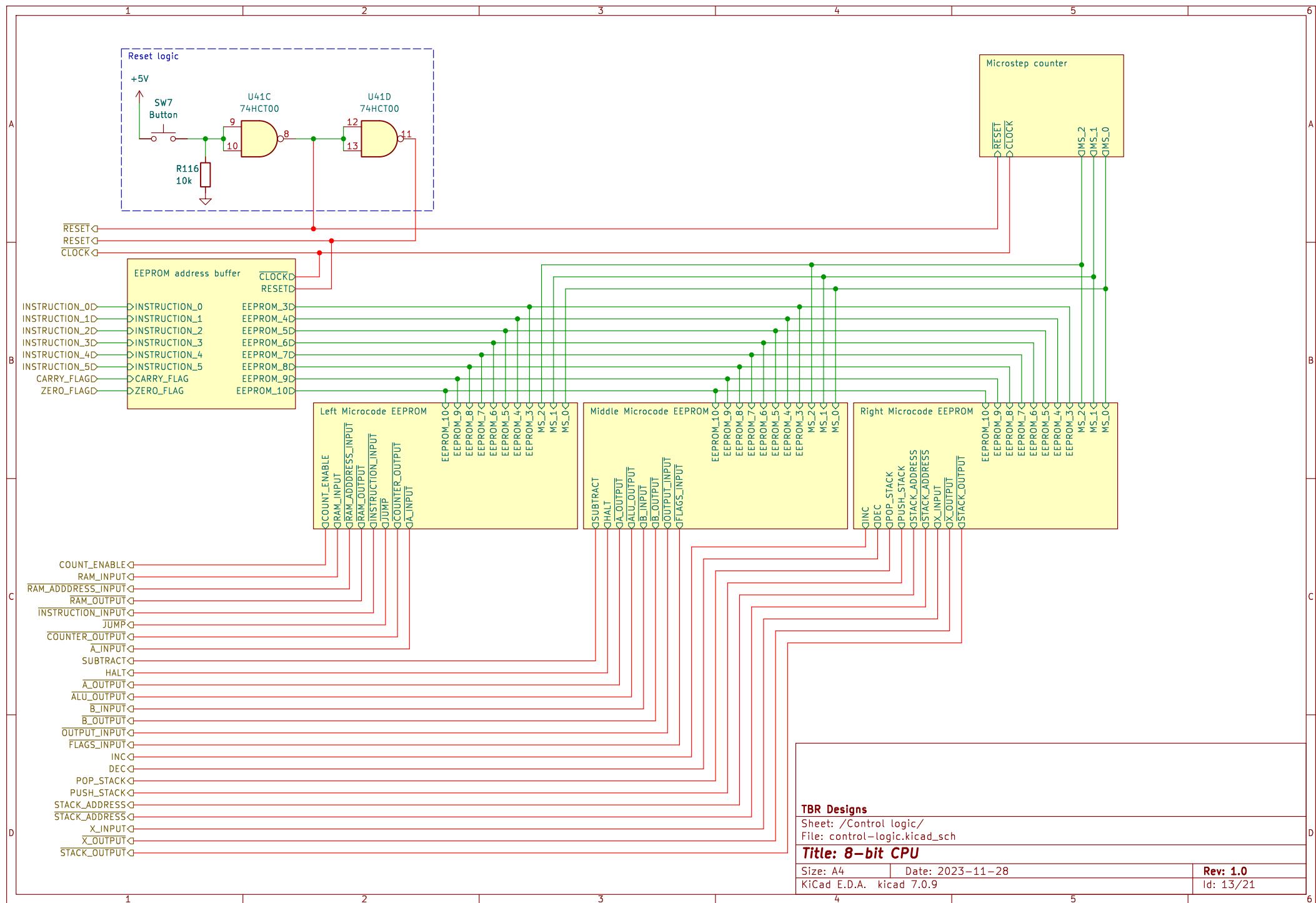
#### TBR Designs

Sheet: /Instruction register/  
 File: instruction-register.kicad\_sch

**Title: 8-bit CPU**

Size: A4 | Date: 2023-11-28  
 KiCad E.D.A. kicad 7.0.9

**Rev: 1.0**  
 Id: 12/21



This address buffer triggers on the inverted CLOCK.  
 I had to include this because during an address transition the outputs of the EEPROM's are undefined.  
 They vary wildly and random actions were triggered briefly.  
 Making the address change on the inverted CLOCK seems to solve this issue because all of the other logic is triggered on the CLOCK.

A

B

C

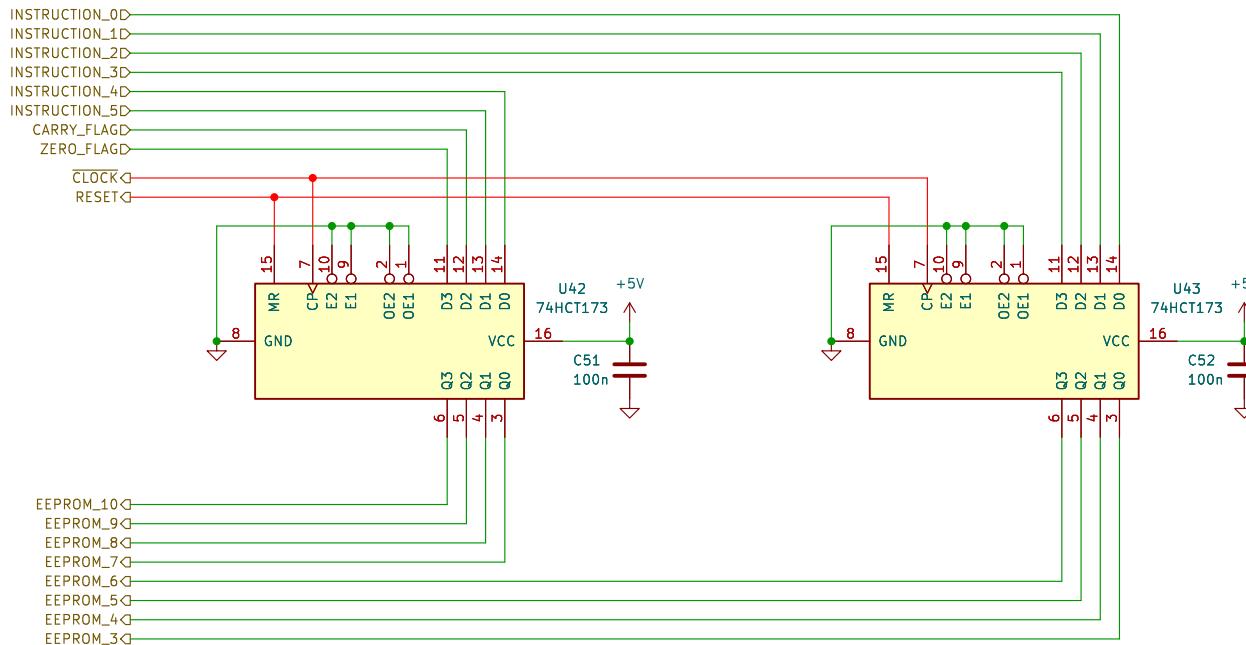
D

A

B

C

D



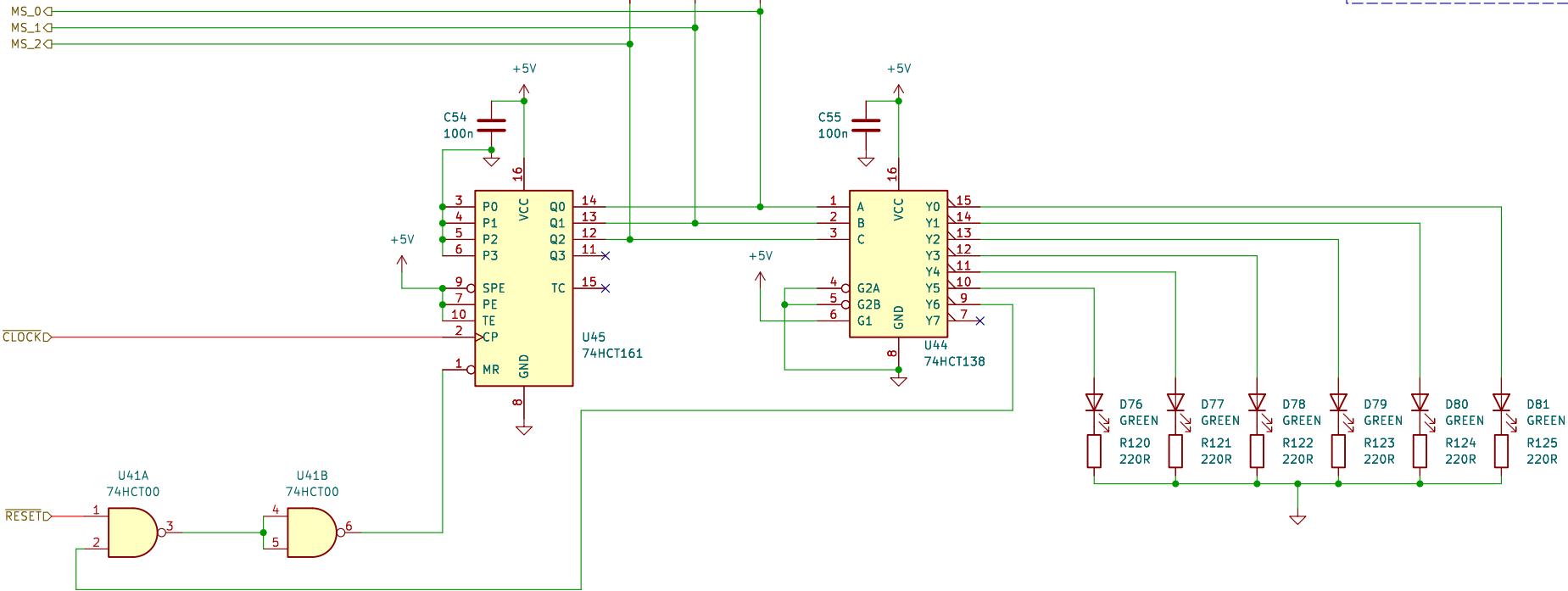
#### TBR Designs

Sheet: /Control logic/EEPROM\_address\_buffer/  
 File: eeprom-address-buffer.kicad\_sch

#### Title: 8-bit CPU

Size: A4 | Date: 2023-11-28  
 KiCad E.D.A. kicad 7.0.9

Rev: 1.0  
 Id: 14/21



### TBR Designs

Sheet: /Control logic/Microstep counter/  
File: microstep-counter.kicad\_sch

**Title: 8-bit CPU**

Size: A4 Date: 2023-11-28  
KiCad E.D.A. kicad 7.0.9

Rev: 1.0  
Id: 15/21

