Micro code EEPROM layout

	Instruction code						Step			Flags		Left		Direct		To inverters						Middle		Direct		To inverters						Right		Direct					To inverters		
										CF	ZF			CE	RI	Ral	RO	II	J	CO	AI			S	HLT	AO	AIO	BI	BO	OI	FI			INC	DCR	SUP	SDN	SA	SO	XI	XO
	A8	A7	A6	A5	A4	A3	A2	A1	A0	A9	A10	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0
NOP Is also the start of each instruction	0	0	0	0	0	0	0	0	0	X	X	0	0			1				1		0	1									1	0								
							0	0	1	X	X	0	0	1			1	1				0	1									1	0								
LDA	0	0	0	0	0	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0				1				1	0	1									1	0								
ADD Add what is at memory address to A	0	0	0	0	1	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0				1					0	1					1				1	0								
							1	0	1	X	X	0	0								1	0	1				1				1	1	0								
SUB Subtract what is at memory address from A	0	0	0	0	1	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0				1					0	1					1				1	0								
							1	0	1	X	X	0	0								1	0	1	1			1				1	1	0								
STA	0	0	0	1	0	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0		1							0	1			1						1	0								
LDI Load direct into A	0	0	0	1	0	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1			1				1	0	1									1	0								
JMP Jump to address	0	0	0	1	1	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0				1		1			0	1									1	0								
JC Jump to address if carry out	0	0	0	1	1	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	0	X	0	0	1								0	1									1	0								
							0	1	1	1	X	0	0				1		1			0	1									1	0								
JZ Jump to address if zero	0	0	1	0	0	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	0	0	0	1								0	1									1	0								
							0	1	1	X	1	0	0				1		1			0	1									1	0								
LDB	0	0	1	0	0	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0				1					0	1					1				1	0								
STB	0	0	1	0	1	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								

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										CF	ZF			CE	RI	Ral	RO	II	J	CO	AI			S	HLT	AO	AIO	BI	BO	OI	FI			INC	DCR	SUP	SDN	SA	SO	XI	XO
	A8	A7	A6	A5	A4	A3	A2	A1	A0	A9	A10	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0
							1	0	0	X	X	0	0		1							0	1						1			1	0								
LDIB Load direct into B	0	0	1	0	1	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1			1					0	1					1				1	0								
OUT	0	0	1	1	0	0	0	1	0	X	X	0	0									0	1			1				1		1	0								
OUTB	0	0	1	1	0	1	0	1	0	X	X	0	0									0	1						1	1		1	0								
OUTX	0	0	1	1	1	0	0	1	0	X	X	0	0									0	1							1		1	0								1
HLT	0	0	1	1	1	1	0	1	0	X	X	0	0									0	1		1							1	0								
LDX	0	1	0	0	0	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0				1					0	1									1	0							1	
STX	0	1	0	0	0	1	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1		1	1					0	1									1	0								
							1	0	0	X	X	0	0		1							0	1									1	0								1
LDIX	0	1	0	0	1	0	0	1	0	X	X	0	0			1				1		0	1									1	0								
							0	1	1	X	X	0	0	1			1					0	1									1	0							1	
PSH	0	1	0	0	1	1	0	1	0	X	X	0	0			1						0	1									1	0					1	1		
							0	1	1	X	X	0	0		1							0	1			1						1	0			1		1			
POP	0	1	0	1	0	0	0	1	0	X	X	0	0									0	1									1	0				1				
							0	1	1	X	X	0	0			1						0	1									1	0					1	1		
							1	0	0	X	X	0	0				1				1	0	1									1	0					1			
PSHB	0	1	0	1	0	1	0	1	0	X	X	0	0			1						0	1									1	0					1	1		
							0	1	1	X	X	0	0		1							0	1						1			1	0			1		1			
POPB	0	1	0	1	1	0	0	1	0	X	X	0	0									0	1									1	0				1				
							0	1	1	X	X	0	0			1						0	1									1	0					1	1		
							1	0	0	X	X	0	0				1					0	1					1				1	0					1			
JSR	0	1	0	1	1	1	0	1	0	X	X	0	0			1						0	1									1	0					1	1		
							0	1	1	X	X	0	0		1					1		0	1									1	0			1		1			
							1	0	0	X	X	0	0			1				1		0	1									1	0								
							1	0	1	X	X	0	0				1		1			0	1									1	0								
RTS	0	1	1	0	0	0	0	1	0	X	X	0	0									0	1									1	0				1				
							0	1	1	X	X	0	0			1						0	1									1	0					1	1		
							1	0	0	X	X	0	0				1		1			0	1									1	0					1			
							1	0	1	X	X	0	0	1								0	1									1	0								

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										CF	ZF			CE	RI	Ral	RO	II	J	CO	AI			S	HLT	AO	AIO	BI	BO	OI	FI			INC	DCR	SUP	SDN	SA	SO	XI	XO
	A8	A7	A6	A5	A4	A3	A2	A1	A0	A9	A10	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0	A11	A12	D7	D6	Y5	Y4	Y3	Y2	Y1	Y0
INCX	0	1	1	0	0	1	0	1	0	X	X	0	0									0	1									1	0	1							
							0	1	1	X	X	0	0									0	1								1	1	0								
DECX	0	1	1	0	1	0	0	1	0	X	X	0	0									0	1									1	0		1						
							0	1	1	X	X	0	0									0	1								1	1	0								
										X	X	0	0									0	1									1	0								
										X	X	0	0									0	1									1	0								
										X	X	0	0									0	1									1	0								