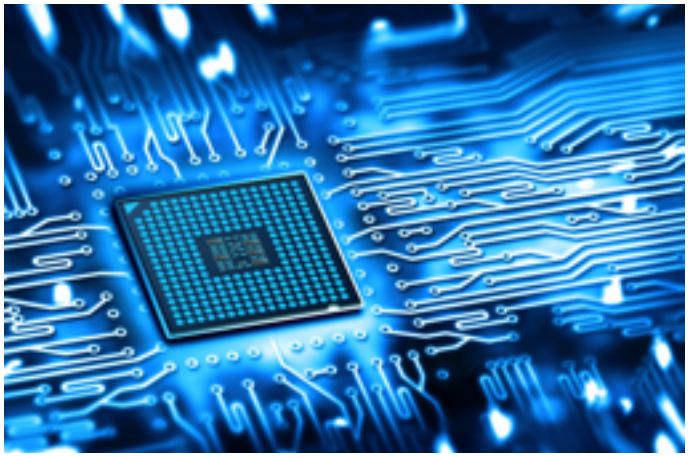
SCHOOL OF COMPUTING
SESSION 2018/2019 SEMESTER 2

SCSR 1013

SECTION-03

DIGITAL LOGIC PROJECT



FINAL REPORT

4-BITS XEROX MACHINE

Group Members: Ridwan bin Monjur (A18CS3026)

Nurul Ismat Tanni (A18CS4052)

Meghla Mehnaz Rose (A18CS3017)

Li Zhaosong(A18CS3069)

Lecturer: Dr. Marina Md Arshad

Submission Date: 18th May, 2019 (Saturday)

DEDICATION AND ACKNOWLEDGEMENT

"Alone we can do so little; together we can do so much." – Helen Keller.

“Talent wins games, but teamwork and intelligence win championships." – Michael Jordan.

Being firm believers of these wise words, we would like to acknowledge the merits of team-work first. If not for togetherness, this wouldn't be possible. The one person without whom we wouldn't be a team in the first place is Ms. Marina Binti Md Arshad, our Digital Logic lecturer. Therefore, we would sincerely like to thank her for her endeavours and always pushing us to think outside the box. She has guided us through every step and was always there when we needed her cooperation. We are indeed so very grateful for her guidance. All the lecturers, along with Ms Marina has given us a fulfilling university experience.

Last, but not the least, we would like to thank our family and friends who constantly support us to get through all adversities. Nonetheless, without them we wouldn’t be where we are.

Needless to say, this is dedicated to our family, friends and all our lecturers, specially Ms. Marina Binti Md Arshad.

Nurul's Family

Li's Family

Rose's Family

Ridwan's Family

TABLE OF CONTENTS

CONTENTS ***PAGE NUMBER***

OUR GOALS

The project incorporates few objectives that were needed to be fulfilled. It was a step-by-step procedure. At our first day, 7th May, 2019, our aim was to type the code, compile it, burn it and at last test it. The simple xerox machine controller implemented 3 different components on a single PLD device. They are count-up counter, comparator, input switches and decoder (Pattern detector)—Clock enabler. This was part 1: 2-bit Xerox Machine Circuit testing.

The description of the first part functions are described below:

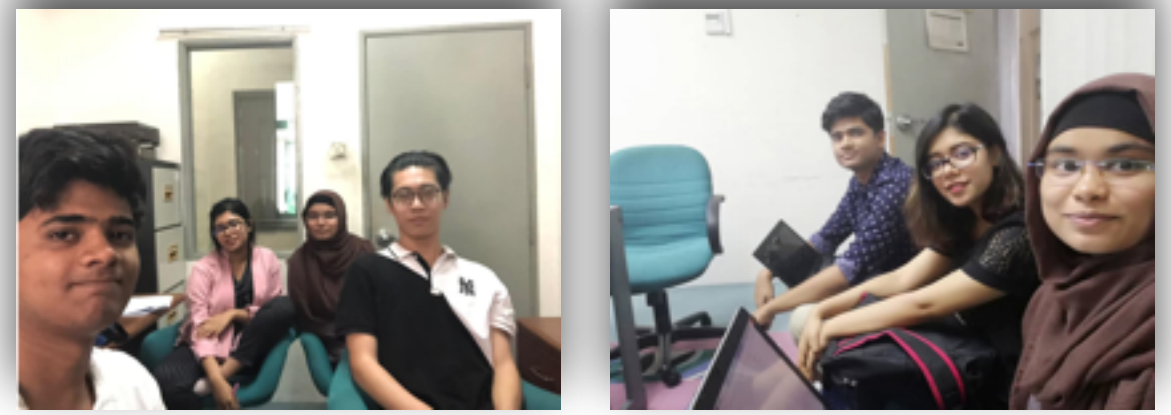
- *Input switches*-It is needed to enter the user's required number of copies. It will be connected to the comparator to be compared with the count-up counter.
- *Comparator*-The comparator compares the input number of copies of paper if it is equal to the current number of printed pages.
- *Count-up counter*-This is needed to count up the number of pages needed to copy. The counter will send the output to the comparator until it matches with the number entered. A 3-bits counter was created and built with aid of the state diagram, truth table and K-map and then finally an equation was obtained.
- *Clock Enabler/disabler*-Clock enabler/disabler is needed to stop the process of the counter or to saturate the counter. It is needed to check if all the requirements are satisfied by the comparator or not. It can also check if the start button is on or off.

Next, part 2 comprised of the xerox machine enhancement in DEEDS stimulator. We implemented the design using DEEDS software. Furthermore, we had to extend the design with the other components, such as encoder, comparator etc.

INTRODUCTION

After being assigned to our respective groups, we first discussed our ideas in our activity room. And, that very day started working in our block diagram. (It will be provided in the up-coming pages). After that, we went to Ms Marina with our draft diagram and she helped us correct it and enhance it in order to have a more eligible and efficient one. In the upcoming pages we will be describing all our procedures—from state diagrams to K-Map. And, how we landed in our final result.

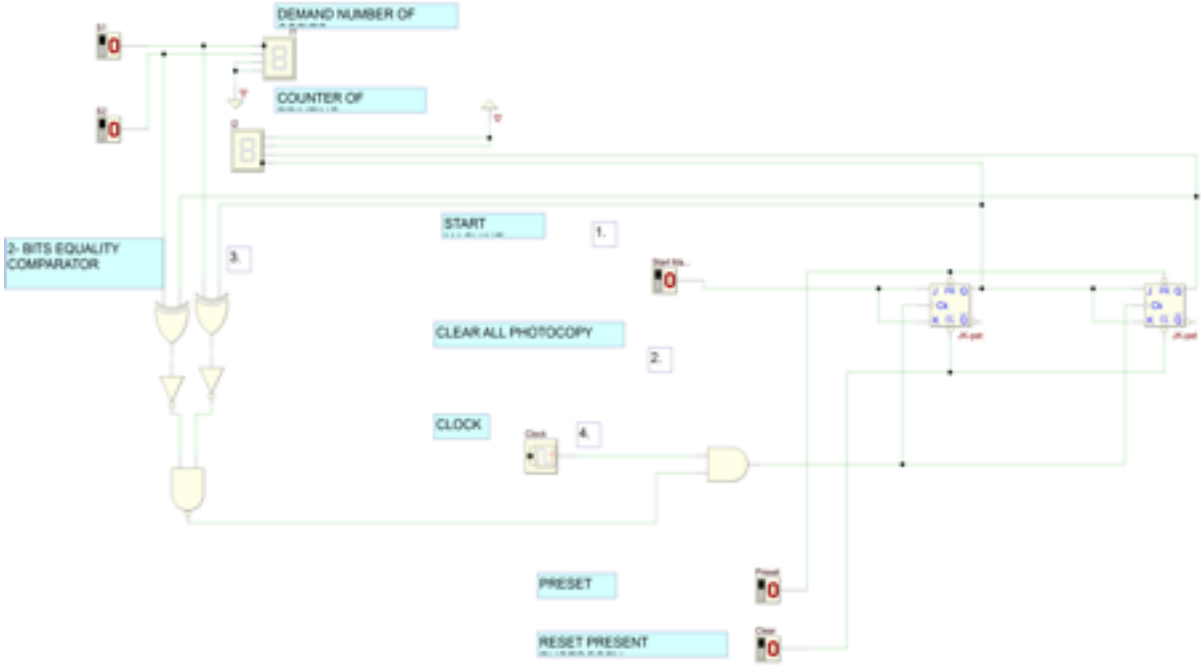
Our method of working was doing all the steps together with every member's consent. However, we also used our strengths and divided a few tasks that way. Ridwan and Li, being good at technicals, brought the ideas in the form of K-map and state diagrams. While Nurul and I(Rose), improvised on what they did and used our decorative skills to write the group report. Ridwan and Li helped too in that as well. Even though tasks were divided, we all helped each other when needed.



Pictures of us during discussion and consultation

DEEDS DIAGRAM

Fig. 1 V: Screenshot of the 2-bits Deeds Diagram



4-BIT DESIGN WITH K-MAP AND EQUATIONS

Present State				Next State				JK Transition Table							
Q3	Q2	Q1	Q0	Q3 +	Q2 +	Q1 +	Q0 +	J3	K3	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

J3

Q3Q2 \ Q1Q0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

0111
1111

J3=Q2Q1Q0

J2

Q3Q2 \ Q1Q0	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

0011
0111
1111
1011

J2=Q1Q0

J1

Q3Q2 \ Q1Q0	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	1	X	X
10	0	1	X	X

0001
0101
1101
1001
0011
0111
1111
1011

J1=Q0

J0

Q3Q2 \ Q1Q0	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

J0=1

K3

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

0111
1111

K3=Q2Q1Q0

K2

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	0	1	0
10	X	X	X	X

0011
0111
1111
1011

K2=Q1Q0

K1

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	0
10	X	X	1	0

0001
0101
1101
1001
0011
0111
1111
1011

K1=Q0

K0

Q3Q2 \ Q1Q0	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

K0=1

ENHANCEMENT

4-BITS XEROX MACHINE:

Design of enhanced functions:

1. **Enhanced function 1:**

Password [Binary encoder (3 to 8)]

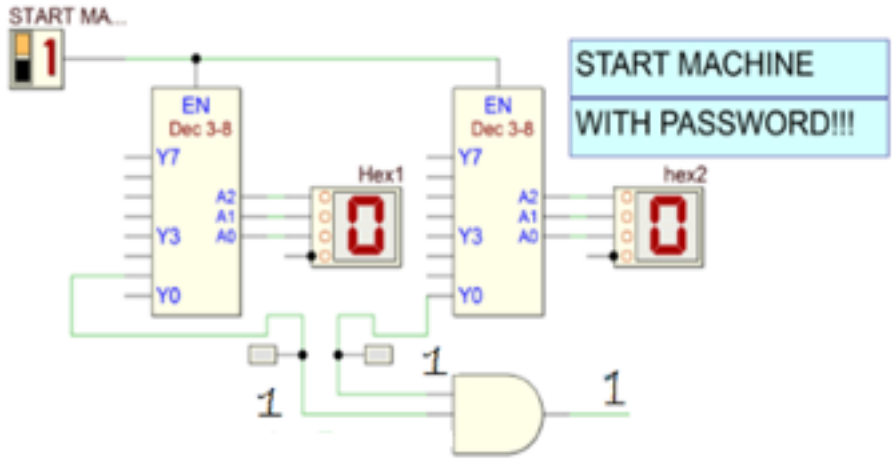
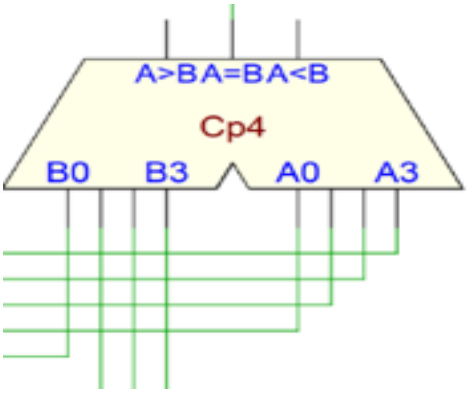


Fig.: Password

- Two hex- digits input the 2-digit hex password.
- Password is set ‘2 0‘ at the moment. (not ‘1 0’!)
- If the right password is inputted only, LED lights to show the password is correct and 2 input bits of 1 is output into the clock enabler.



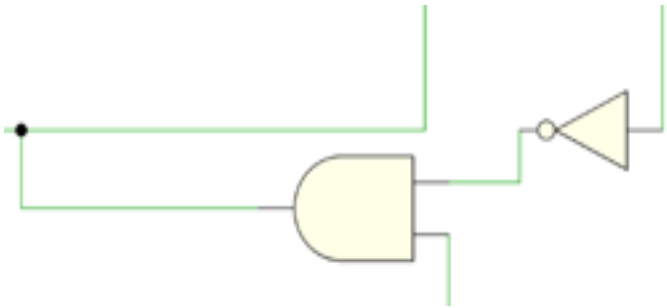
2. Identical comparators and counters (give HIGH logic output):

1) Comparator 1 for Counter 1: compares number of **sets of photocopy** with the count by Counter1.

2) Comparator 2 for Counter 2: compares **number of pages of photocopy for each set** with the count by Counter2.

3) Enhanced function 3: Two Clock Enablers

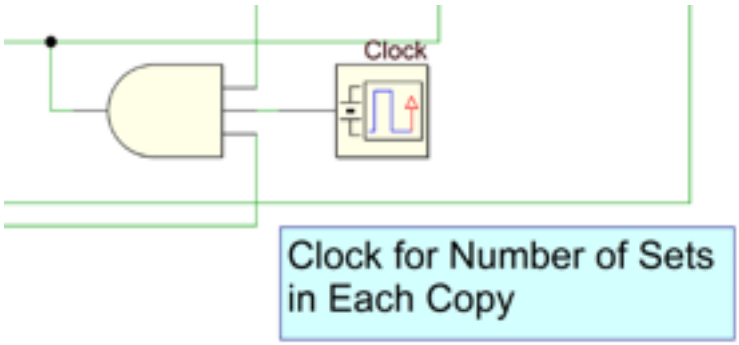
1) Clock enabler 1/ Clock enabler for Counter 1 (Number of sets)



- This clock is **not** driven by a clock generator**.** It is driven by the '1' / HIGH output of the AND.

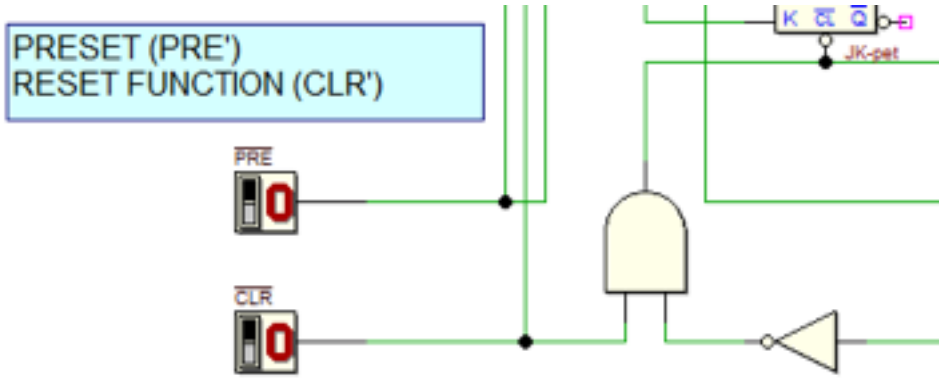
- Bottom wire into the AND gate comes from the **Comparator 2.** If the number of pages for each set of photocopy are same as user inputted, then Comparator 2 gives '1' / HIGH logic. This HIGH logic increments **Counter 2**.
- Top wire into the AND gate comes from the **comparator** 1 (for number of sets).
    - There is a NOT gate which means if Comparator 1 gives HIGH output, it will stop the clock *because NOT inverses the HIGH output to LOW output.*
    - Comparator 1 gives HIGH output if all the number of sets have been completed.
    - If number of sets of photocopy is completed, the task is over, so we want to stop it now by the NOT gate.

2) Clock enabler 2/ Clock enabler for Counter 2 (Number of pages for each set)



- Bottom wire into the AND gate comes from the **password,** giving logic '0'/ stopping clock for **Counter 2 (Number of pages for each set)** if password fails**.**
- Top wire into the AND gate comes from the **comparator** 1 (for number of sets), which stops clock if number of sets equal.

4. **Enhanced Function 3: Clear counter2 when one set of photocopy is completed.**



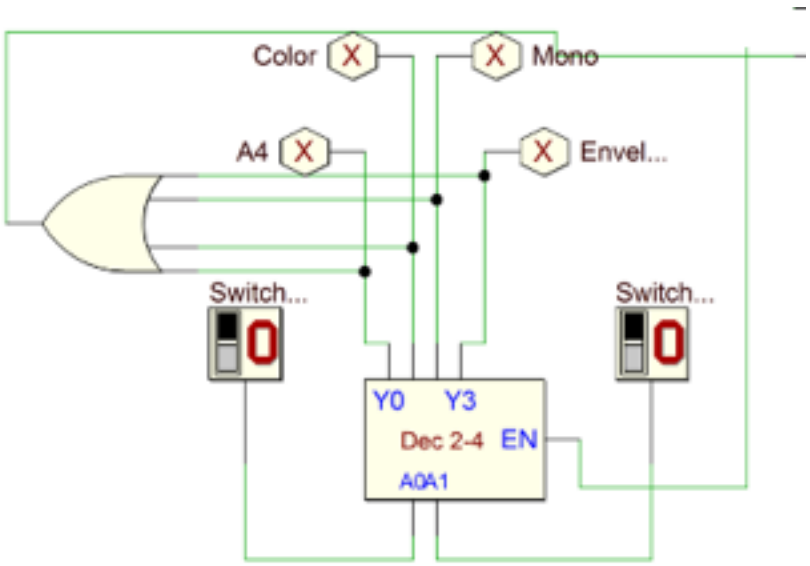
When RESET=1:

1) Left wire is coming from RESET switch (‘1’ at moment).

2) Right wire is coming from **Comparator2.** When one set of photocopy is completed, it gives ‘1’/HIGH output. We inverse it, so ‘0’ goes into the AND.

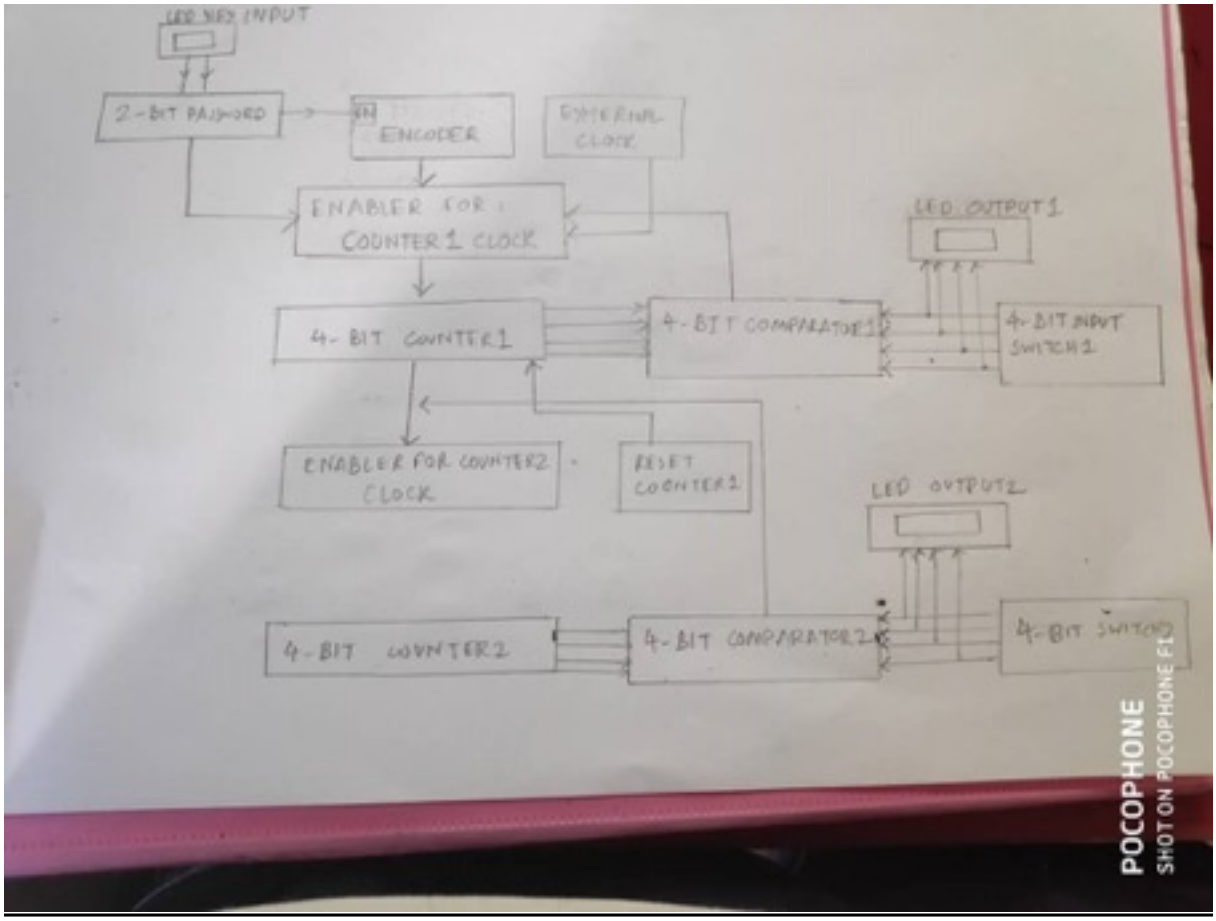
3) AND gives RESET=0. So, counter resets.

4) Enhanced Function 4: Type of Photocopy

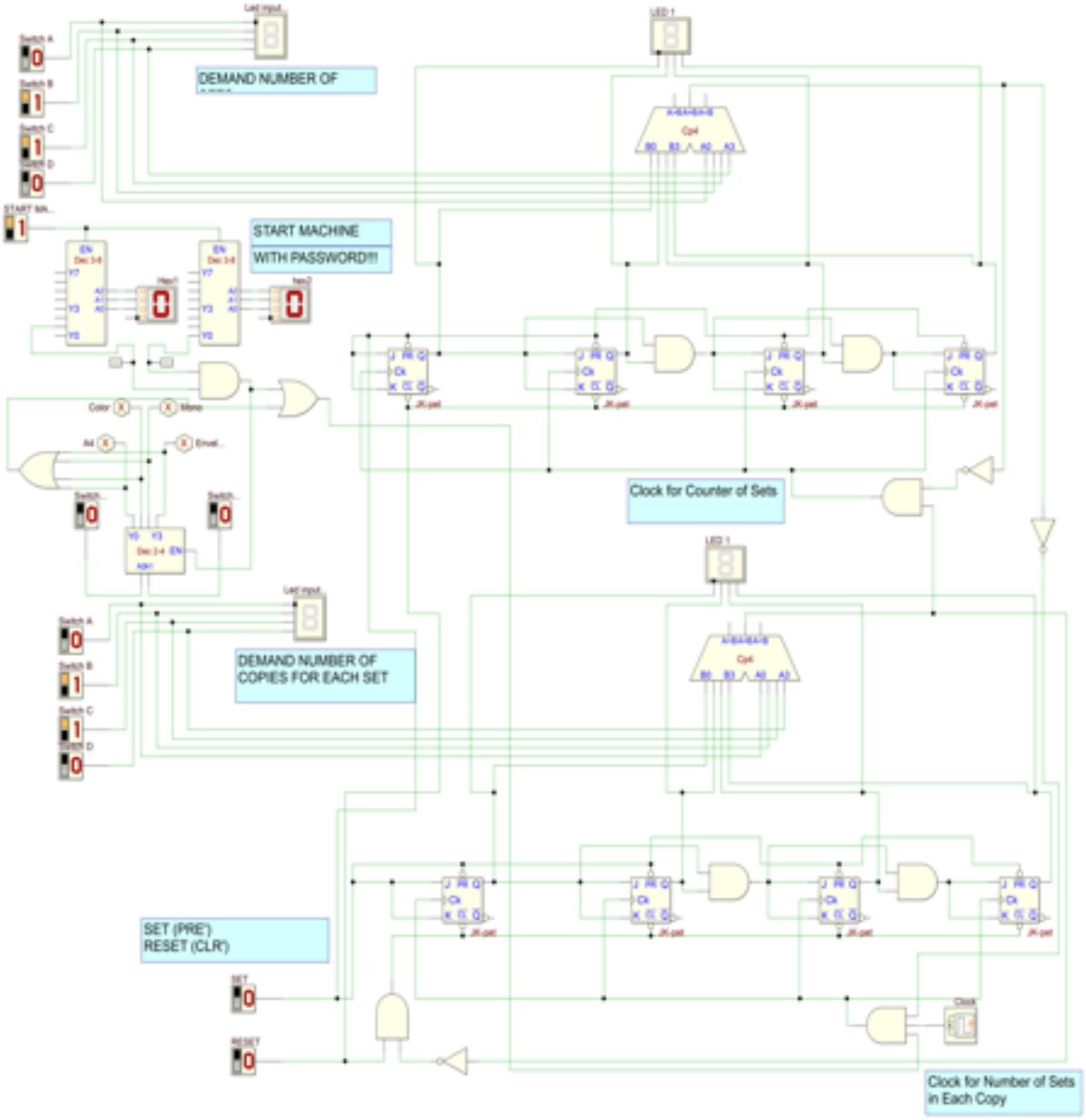


User can choose any of the two paper types and any of the two colour options.

BLOCK DIAGRAM



FINAL DEEDS CIRCUIT



INSTRUCTIONS OF USING THE MACHINE:

1. Switch on START MACHINE.
2. Switch on

   PRE'=1

   CLR'=1
3. Set Password: '2 O' i.e. Left hex digit should be '2'
4. (Optional) Choose your photocopy type: a) Colour or Mono? AND b) A4 or A3?
5. Choose the number of sets and number of pages for each set.
6. Enjoy! Just press the clock.

REFERENCES

- Digital Fundamentals by Thomas L. Floyd, 11 edition
- Fundamentals of Logic Design, Sixth Edition, Charles H. Roth, Larry L. Kenney
- Digital Logic, School of Computing, Faculty of Engineering, University Teknologi Malaysia
- https://www.electronics-tutorials.ws
- https://www.allaboutcircuits.com/textbook/digital/chpt-10/j-k-flip-flop/
- https://electronics.stackexchange.com/questions/323093/what-is-the-difference-between-enable-and-clock-in-flip-flops
- Marina, M. A. (2017). Report Format: REPORT for DIGITAL LOGIC PROJECT. Johor: Marina Md Arshad, Department of Computer Science, Faculty of Computing.

Appendices

Software used;

• DEEDS software.

• Win CULP.

• Wellon.

Lab hours: 5 hours

Project group members:

- Meghla Mehnaz Rose
- Ridwan Bin Monjur
- Nurul Ismat Tanni
- Li Zhaosang

Project supervisor:

Miss Marina Binti Mad Arshad.