United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam Trimester: Summer 2024

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 30 Duration: 1 hour 45 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (6 Marks)

Transfer of bus control from processor to device takes **200 ns**. Transfer of bus control from device to processor takes **300 ns**.

a.	If one of the input/output devices employs **DMA** in **Burst** Mode and takes **20,000,500 ns** to transfer **2048 bytes** of data. Find the data transfer rate of the device in **KB/s**.	[3]
b.	Suppose, you are transferring **2048 bytes** of data in both Burst Mode and Cycle Stealing Mode. For the **first half** of the bytes, you use Burst Mode and for the **rest half**, you use Cycle Stealing Mode. Assume that in Cycle Stealing Mode, data is transferred 4 bytes at a time. How long will it take to transfer a total block of 2048 bytes? (Use the data transfer rate found from (a))	[3]

Question 2: Answer all the questions. (6 Marks)

a.	Suppose, execution of a signed addition instruction **(7A34H + 4DC2H)** occurred. What would be the values of the sign flag (SF), parity flag (PF), carry flag (CF), and overflow flag (OF)?	[4]
b.	If some microprocessor has a 24 bit address bus, 8 bit data bus, and its total memory is segmented into 128 KB sized blocks; how many segments should be present in the memory?	[2]

Question 3: Answer all the questions. (6 Marks)

a.	CS = E47BH, DS = 4C18H, BX = 0100H, BP = 0F20H To access the physical address in the **Data Segment**, what should be the value of I) the **segment register** if the offset register holds the value of B290H. II) the **offset register** if the segment register holds the value of 3C2FH. **Justify whether your answer is valid or not.** III) Find the last physical address of the given **Code Segment**.	[3]

b.	RAM[A] has a **data bus** of 32 bits, while RAM[B] has an **address bus** of 20 bits and a **data bus** of 8 bits. Both RAMs have the same total memory capacity. Determine the **width of the address bus** of RAM[A], and calculate the **total memory capacity** for both RAMs.	[3]

Question 4: Answer all the questions. (6 Marks)

a.	**Draw the diagram** of a microprocessor with a 18-bit address bus and 8-bit data bus interfaced to 4 KB RAM system using the **partial decoding method**. Each RAM chip has a 10-bit address bus and 8-bit data bus. Provide the corresponding **address range** (starting and end address) as well.	[3]
b.	What modifications are needed to implement the same system as described in part (a) using the **full decoding method**? **Draw** only the **modified part**. **Compare** both methods (partial and full decoding) for this case, and determine which method is better and why.	[3]

Question 5: Answer all the questions. (6 Marks)

a.	In an **8086 microprocessor**, CS = 0080 H , IP = 00FF H , Flag Register = FFFF H Describe the **sequence** of **events** that the 8086 microprocessor will execute when it encounters a **software interrupt** based on the given values. Also, show the **stack contents** during this process.	[4]
b.	The memory addresses for Overflow Interrupt and Floating Point Error in the vector table are (10 H - 13H) and (40 H - 43H) respectively. Which interrupt has a **higher priority** and why?	[2]