United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Final-Term Exam Trimester: Fall 2024

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 40 Duration: 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (10 Marks) [CO3]

Global Descriptor Table	
Index	**Address**
045 H	Base: BE308810, Limit: 78BD7H, Access: 54H, G = 1
1A3 H	Base: BFE4DBB8, Limit: 3345AH, Access: 1FH, G = 0
2F6 H	Base: B66125A3, Limit: CC32FH, Access: 8AH, G = 1
4D1 H	Base: B2B2ACFF, Limit: F56A9H, Access: 27H, G = 1
6B4 H	Base: B61310BD, Limit: 50AEAH, Access: 53H, G = 0
A29 H	Base: B4DF02F6, Limit: C5072H, Access: 49H, G = 0

Local Descriptor Table	
Index	**Address**
045 H	Base: A584718E, Limit: 0FAE1H, Access: F9H, G = 0
1A3 H	Base: A872A2F3, Limit: 29FDBH, Access: 0DH, G = 0
2F6 H	Base: AFF3B41C, Limit: 53027H, Access: B8H, G = 1
4D1 H	Base: ABA461B6, Limit: C31ABH, Access: 62H, G = 0
6B4 H	Base: A56DC418, Limit: E6357H, Access: 54H, G = 1
A29 H	Base: A61C994D, Limit: 694CCH, Access: 14H, G = 1

Part of the descriptor table for an **80386 microprocessor** is given above. For a segment register value of **35A1 H**, determine the followings:

a.	Which entry, table and requested privilege level are selected?	**[3]**
b.	Starting and Ending address of the segment.	**[2]**
c.	For an **offset** value of **158C0 H**, determine the physical address.	**[1]**
d.	Has the segment been accessed?	**[1]**
e.	Segment type (**CS/DS/SS/ES**).	**[2]**
f.	Is the descriptor defined or undefined?	**[1]**

Question 2: Answer all the questions. (10 Marks) [CO5]

a.	The NXP Kinetis Series offers a 24 bit ADC on a 5.0 V reference system and a 12 bit DAC with I2C interface. i. Calculate the analog voltage if the ADC reading is **8300608.** ii. During the digital to analog programming, you need to call **analogWrite(1760)**. Calculate the duty cycle and draw the corresponding duty cycle diagram.	**[2+2]**
b.	What is the primary difference between **SPI** and **I2C** protocols? Suppose in a particular I2C communication, the **Master (index - CH)** receives a **4 byte data (from characters: 'uGrad')** from a **Slave (index - 7H)**. Draw the corresponding sequence diagram. **ASCII** codes for **'A'** and **'a'** are **65 and 97 respectively**.	**[1+3]**

c.	Suppose you want to design a **real-time traffic monitoring system** for an intersection. The system requires processing multiple sensor inputs (traffic cameras, speed detection sensors) and adjusting traffic signal timings dynamically to optimize traffic flow. The system can be built using either a **Raspberry Pi (microprocessor-based system) or Arduino (microcontroller-based system)**. **Which platform would be more suitable** and **why?**	**[2]**

Question 3: Answer all the questions. (10 Marks) **[CO3]**

a.	Consider the following fetch cycle in an 8086 BIU: [Fetch, Fetch, Fetch, Fetch, Fetch, Fetch,Fetch, Fetch] When the one instruction is being executed, **four instructions** are fetched and saved in the instruction queue. If the **1st** instruction is a **'MOV <address>'**, the **3rd** is a **'JUMP <5th instruction address>'** and **4th** instruction is a **'JUMP <7th instruction address>'** instruction, then **draw** the corresponding **BIU and EU's cycle.**	**[4]**
b.	Draw the timing diagram for **IO Write** operation of microprocessor "808x" showing the activities of $\overline{Mem/IO}$, *Address-Data bus (AD0 - AD15, A16 - A19),* $\overline{ALE}$*, WR, RD,* $\overline{DEN}$*,* $\overline{DT/R}$ in each clock cycle. **[Observe the pins carefully]**	**[4]**
c.	What is the advantage of **paging technique**?	**[2]**

Question 4: Answer all the questions. (10 Marks) **[CO4]**

RAM Content

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	0000 0010
3H			BH	0110 0100
4H			CH	0000 0101
5H			DH	0000 0001
6H			EH	1000 0101
7H			FH	0100 0010

Opcode Table

Mnemonic	Opcode
HLT	1101
OUT	1001
SUB	1100
ADD	1110
LDA	1010

Initially, the value of the **Accumulator Register is 1H, the B Register is 3H, and the Output Register is 4H**.

a.	Write the **assembly code** for the following expression using **RAM content**. $3 + 5 - 2 - 1$	**[4]**
b.	Find out the values of the **Accumulator register, B register and Output Register** after executing **each** instruction **written in (a)**.	**[3]**
c.	Write the control words for Execution T-states (**T4, T5, T6**) to perform the **ADD instruction** using the controller sequence below. **CON** = $S_U\overline{E_U}\,C_p\;E_p \quad L_M C_E \overline{L_I}\,\overline{E_I} \quad L_A\overline{E_A}\,\overline{L_B}\,\overline{L_O}$ **[Observe the pins carefully]**	**[3]**