United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam Trimester: Spring 2025

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 30 Duration: 1 hour 30 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (7.5 Marks)

Transfer of bus control from processor to device takes **0.2 µs(microseconds)**. Transfer of bus control from device to processor takes **0.4 µs(microseconds)**.

a.	If one of the input/output devices employs DMA in **Cycle Stealing Mode** and takes **62,960,800 ns** to transfer some data at a transfer rate of **96 KB/s** with **8 Bytes** of data being transferred at once, find out the **total size** of the data to be transferred **in Bytes**.	**[4]**
b.	Suppose, you will be transferring the total data (*found from (a)*) now in both Burst Mode and Cycle Stealing Mode. For the first **one-third** of the bytes, you use **Burst Mode** and for **the rest**, you use **Cycle Stealing Mode**. Assuming that cycle stealing mode transfers **8 Bytes** at a time and both modes use **96 KB/s** transfer rate, how long will it take to transfer the whole data?	**[3.5]**

Question 2: Answer all the questions. (7.5 Marks)

a.	Execution of a signed addition instruction **(76DAH + 3867H)** occurred. What would be the values of the sign flag (SF), parity flag (PF), auxiliary flag (AF), carry flag (CF), and overflow flag (OF)? **Provide a brief explanation for your answer.**	**[5.5]**
b.	State **two** differences between the Primary memory and Secondary memory.	**[2]**

Question 3: Answer all the questions. (7.5 Marks)

a.	**CS = 25A1 H, DS = 4132 H, SS = 3123 H, ES = 5132 H** **IP = 2451 H, SI = 134B H, SP = 2354 H** I) Find how many **physical address slots** exist that are **overlapping** between **Code segment and Stack segment**? II) Can the **Data Segment** be placed after the **Stack Segment** without overlapping with the **Extra Segment**? **Explain with mathematical reasoning.**	**[2.5+ 2.5]**

b.	**RAM X** has **two third times** the capacity of **RAM Y**. The total memory capacity of **both RAMs combined is 15 MB**. If **RAM X** has a **22-bit address bus**, determine the size of its **data bus**.	**[2.5]**
Question 4: Answer all the questions. (7.5 Marks)		
a.	You need to design a system where a microprocessor with a **18-bit address bus** and **16-bit data bus** is interfaced to a **48 KB RAM** system using **Linear decoding**. Each RAM chip has a **12-bit address bus** and a **16-bit data bus**. **Draw a block diagram showing the microprocessor, RAM chips, and linear decoding logic**. **Provide the 3rd, 5th and 7th address of the last three RAM chips.**	**[4+ 3.5]**