United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Final-Term Exam Trimester: Fall 2023

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 40 Duration: 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (10 Marks)

Local Descriptor Table	
Index	**Address**
002 H	Base: C238000A, Limit: F175FH, Access: 02H, G = 0
014 H	Base: C38400A0, Limit: E9806H, Access: C1H, G = 1
126 H	Base: C9560A00, Limit: 85642H, Access: FEH, G = 0
158 H	Base: C002A00E, Limit: 2A043H, Access: B4H, G = 1
275 H	Base: C85200EF1, Limit: AB00FH, Access: D1H, G = 1
344 H	Base: C60401A1, Limit: 0FFFFH, Access: A0H, G = 0

Global Descriptor Table	
Index	**Address**
002 H	Base: D7210111, Limit: 01234H, Access: 05H, G = 1
014 H	Base: D3270011, Limit: 98765H, Access: F1H, G = 0
126 H	Base: D3741000, Limit: 1524CH, Access: 11H, G = 1
158 H	Base: D6590B00, Limit: FB000H, Access: B2H, G = 0
275 H	Base: D6870010, Limit: 0AF0EH, Access: FEH, G = 1
344 H	Base: D655000B, Limit: D015CH, Access: 07H, G = 1

Part of the descriptor table for an **80386 microprocessor** is given above. For a segment register value of **930H**, determine the followings:

a.	Which entry, table and requested privilege level are selected?	[3]
b.	Starting and ending address of the segment.	[2]
c.	For an offset value of **12ACDH**, determine the physical address.	[1]
d.	Segment type (CS/DS/SS/ES).	[1]
e.	Is access to the segment granted? Why or why not ?	[2]
f.	Is the descriptor defined or undefined?	[1]

Question 2: Answer all the questions. (10 Marks)

a.	In **'X' microcontroller**, **11 bits** digital to analog (**DAC**) resolution is set. During the digital to analog conversion programming, you have called "**analogWrite (1535)**" instruction. Calculate the **duty cycle**. **Draw the duty cycle diagram.** Consider the **system voltage is 7V.**	[2+2]
b.	UIU is planning to implement an **Advanced Access Control system** for enhanced campus security. Employees and students will utilize **RFID cards** for entry and exit. Another plan is to create **an automated module to calculate attendance, performance and efficiency of the students.** Now, "X" suggested using **Raspberry pi for the Advanced Access Control System** and **Arduino for the other module.** Do you think the suggestion was right? Write **Yes or No** and then **give reasons for your answer.**	[1+2]

c.	In a microcontroller-based system a master device, **Master (index:2H)** receives **3 byte data (char 'M&m')** from the **slave (index: D2H)** using **I^2C**. **Draw** the corresponding **sequence diagram.** (Assume that I^2C uses **10 bit addressing** for slave address, **ASCII value of '&' is 38, 'D' is 68, '2' is 50, 'M' is 77 and 'm' is 109**)	[3]

Question 3: Answer all the questions. (10 Marks)

a.	Consider the following fetch cycle in an 8086 BIU: [Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch] When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the **2nd** instruction is a **'JUMP <5th instruction address>'**, the **5th** is a **'JUMP <7th instruction address>'** and **6th** instruction is a **'MOV <address>'** instruction, then **draw** the corresponding **BIU and EU's cycle.**	[4]
b.	**Draw** the timing diagram for **IO Read** operation of microprocessor "**808x**" showing the activities of Mem/$\overline{IO}$, Address-Data bus (AD_0 - AD_{15}, AD_{16} - AD_{19}), $\overline{ALE}$, WR, RD, DEN, $\overline{DT}$/R in each clock cycle. **[Observe the pins carefully]**	[4]
c.	What is the **page fault**? What happens when a page fault occurs?	[1+1]

Question 4: Answer all the questions. (10 Marks)

RAM Content

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	0000 0100
3H			BH	0010 0100
4H			CH	0000 0011
5H			DH	0000 0010
6H			EH	0001 0011
7H			FH	0000 0101

Opcode Table

Mnemonic	Opcode
HLT	1110
OUT	0101
SUB	0100
ADD	0110
LDA	1001

a.	Write **the assembly code** for the below expression using the **RAM content:** $5 \times 4 - 2 \times 3$ **Hints: Multiplication can be done by addition**	[3]
b.	Fill-up the **RAM content table** with the instructions **machine code.** (**Start from 0H**). Use the opcode given in the **opcode table**.	[3]
c.	Explain what changes you have to make in **SAP-1** architecture to perform the instruction **OUTB** (Load the content of memory address to B register and show its value in the binary display). Also, Write the control words for execution T-states (T4, T5, T6) to perform the instruction using the given controller sequence. **CON** = $\overline{C_P E_P} L_M CE \; L_I E_I \overline{L_A} E_A \; S_U \overline{E_U} L_B L_O$ [**Observe the pins carefully**]	[4]