United International University **(UIU)**

Dept. of Computer Science & Engineering **(CSE)**

Final-Term Exam: Trimester: Summer 2023

Course Code:CSE 4325; Course Title: Microprocessors & Microcontrollers
Total Marks: 40**; Duration:** 2 hours
Answer all the questions

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question-1: Answer all the questions: **[10 Marks]**

Local Descriptor Table	
Index	**Address**
002 H	Base: C238000A, Limit: F175FH, Access: 02H, G = 0
014 H	Base: C38400A0, Limit: E9806H, Access: C1H, G = 1
126 H	Base: C9560A00, Limit: 85642H, Access: FEH, G = 0
158 H	Base: C002A00E, Limit: 2A043H, Access: B4H, G = 1
275 H	Base: C85200EF1, Limit: AB00FH, Access: D1H, G = 1
344 H	Base: C60401A1, Limit: 0FFFFH, Access: A0H, G = 0

Global Descriptor Table	
Index	**Address**
002 H	Base: D7210111, Limit: 01234H, Access: 05H, G = 1
014 H	Base: D3270011, Limit: 98765H, Access: F1H, G = 0
126 H	Base: D3741000, Limit: 1524CH, Access: 11H, G = 1
158 H	Base: D6590B00, Limit: FB000H, Access: B2H, G = 0
275 H	Base: D6870010, Limit: 0AF0EH, Access: FEH, G = 1
344 H	Base: D655000B, Limit: D015CH, Access: 07H, G = 1

Part of the descriptor table for an **80386** microprocessor is given above. For a segment register value of **AC6H** , **determine** the followings:

i) Which entry,table and requested privilege level are selected? **[3]**
ii) Starting and ending address of the segment. **[2]**
iii) For an offset value of **C051B H**, determine the physical address. **[1]**
iv) Segment type (CS/DS/SS/ES). **[1]**
v) Is access to the segment granted? Why or why not ? **[2]**
vi) Is the descriptor defined or undefined? **[1]**

Question-2: Answer all the questions: **[10 Marks]**

a) Draw the timing diagram for memory **Read** operation of microprocessor 8086 showing the activities of Mem/IO, Address-Data bus (AD), ALE,$\overline{WR}$, $\overline{Rd}$, $\overline{DEN}$, DT/$\overline{R}$ in each clock cycle. **[4]**

b) Consider the following fetch cycle in an 8086 BIU:

[Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch]

When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the 2nd instruction is a **'MOV <address>'** instruction and the 5th is a **'JUMP <7th instruction address>'**, then ***draw*** the corresponding BIU and EU's cycle.
[2+2]

c) Describe the **clock skew** phenomenon. **[2]**

Question-3: Answer all the questions: **[10 Marks]**

a) Write the assembly code for the below expression using the RAM content:

$$27 + 25 \times 2 - 35 = ?$$ **[3]**

[Multiplication can be done by addition]

b) Fill-up the RAM content table with the instructions machine code. (Start from 0H). Use the opcode given in the opcode table: **[4]**

RAM Content :

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	
3H			BH	01100100
4H			CH	00011011
5H			DH	00011001
6H			EH	00010100
7H			FH	00100011

Opcode Table:

Mnemonic	Opcode
HLT	1000
OUT	0001
SUB	0011
ADD	0100
LDA	1100

c) What are the values of **Accumulator** registers after executing each instruction programmed in the RAM. [Initially Accumulator = 0H]. **[3]**

Question-4: Answer all the questions: **[10 Marks]**

a) Your microprocessor lab wants to add a new experiment. The main idea of the experiment is to process raw video data for security purposes. You have two options- Raspberry Pi or Arduino board to implement this. Explain which board you will use and why. **[3]**

b) In a microcontroller board, 12 bits digital to analog (DAC) resolution is set.During the analog to digital conversion programming, you have called the "analogWrite(1023)" instruction. **Calculate the duty cycle. Draw the duty cycle diagram. Consider system voltage 12V.** **[1+2]**

c) What does **UART** stand for? Draw a simplified UART interface. **[2]**

d) Write 1 advantage and 1 disadvantage of **SPI** communication. **[2]**