United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam Trimester: Fall 2024

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 30 Duration: 1 hour 30 minute(s)

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (6 Marks)		
	Transfer of bus control from processor to device takes **600 ns**. Transfer of bus control from device to processor takes **400 ns**.	
a.	If one of the I/O devices employs DMA in **cycle stealing mode** and takes **120512 µs (micro seconds)** to transfer a total **3072 bytes** of data. The I/O device has a data transfer rate of **25 KB/s**. How many bytes are transferred at a time in this mode?	**[3]**
b.	Shafiq, a student of the Microprocessor and Microcontroller course, stated that sending **3072 bytes** of data in **burst mode** would have been faster but could lead to a significant problem. Do you agree with **Shafiq's statement?** Justify your answer **mathematically** and explain the significant problem mentioned.	**[1+2]**
Question 2: Answer all the questions. (6 Marks)		
a.	Suppose the **AX register contains 6F24H and the BX register contains 4213H**. Determine the values of the **SF** and **OF** after executing **each of the following instructions sequentially**. **Provide a brief explanation for your answer.** I. ADD AX, BX II. SUB AX, BX	**[2+2]**
b.	Briefly explain **one** disadvantage of **memory mapped I/O**.	**[2]**
Question 3: Answer all the questions. (6 Marks)		
a.	CS = 1437H, DS = 2153H I) Find the last physical address of **Code Segment.** II) Find the last physical address of **Data Segment.** III) Find **how many** physical address slots exist that are **overlapping between both segments**?	**[3]**

b.	A DRAM has a **data bus** of 24 bits, while an SRAM has an **address bus** of 24 bits and a **data bus** of 6 bits. Both the RAMs have the same total memory capacity. Determine the **width of the address bus** of the DRAM, and calculate the **total memory capacity** for both RAMs in **megabytes (MB)**.	**[2+1]**
Question 4: Answer all the questions. (6 Marks)		
a.	You need to design a system where a microprocessor with a **20-bit address bus** and **16-bit data bus** is interfaced to a **192 KB RAM** system using **full decoding**, starting from address **80000H**. Each RAM chip has a **14-bit address bus** and a **16-bit data bus**. **Draw a block diagram showing the microprocessor, RAM chips, and full decoding logic**. Ensure the first RAM **starts at 80000H**. **Provide the second address and the second-last address of the first three RAM chips.**	**[3+3]**
Question 5: Answer all the questions. (6 Marks)		
a.	If **007EH** and **007FH** memory locations contain **CS=0080H** for an interrupt instruction in the Interrupt Vector Table, find the corresponding Interrupt (INT) number.	**[4]**
b.	Write the sequence of events that take place when a software interrupt instruction is executed.	**[2]**