UIU QUESTION BANK

MID-TERM QUESTION SOLUTIONS

MICROPROCESSORS AND MICROCONTROLLERS

CSE 4325

SOLUTION BY

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UPDATED TILL ***FALL 2024***

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1. Transfer of bus control from processor to device takes **600 ns**. Transfer of bus control from device to processor takes **400 ns**.

1. a) If one of the I/O devices employs DMA in **cycle stealing mode** and takes **120512 µs (micro seconds)** to transfer a total **3072 bytes** of data. The I/O device has a data transfer rate of **25 KB/s**. How many bytes are transferred at a time in this mode?

Solution:

Let,

x bytes data transferred at a time.

Here,

$25\ KB$ data transferred in $1\ s$

$\therefore 25 \times 2^{10}\ B$ data transferred in $1\ s$

$\therefore 1\ B$ data transferred in $\frac{1}{25 \times 2^{10}}\ s$

$\therefore x\ B$ data transferred in $\frac{1 \times x}{25 \times 2^{10}}\ s$

$$= \frac{x \times 10^9}{25 \times 2^{10}}\ ns$$

According to questions,

$$\left(600\ ns + \frac{x \times 10^9}{25 \times 2^{10}}\ ns + 400\ ns\right) \times \frac{3072}{x} = 120512 \times 10^3\ ns$$

or, $\frac{600 \times 3072}{x} + \frac{x \times 10^9 \times 3072}{25 \times 2^{10} \times x} + \frac{400 \times 3072}{x} = 120512000$

or, $\frac{1843200}{x} + 120000000 + \frac{1228800}{x} = 120512000$

or, $\frac{1843200 + 1228800}{x} = 120512000 - 120000000$

or, $\frac{3072000}{x} = 512000$

or, $x = \frac{3072000}{512000}$

$\therefore x = 6$

$\therefore$ 6 bytes are transferred at a time in this mode

1. b) Shafiq, a student of the Microprocessor and Microcontroller course, stated that sending 3072 bytes of data in **burst mode** would have been faster but could lead to a significant problem. Do you agree with **Shafiq's statement**? Justify your answer **mathematically** and explain the significant problem mentioned.

Solution:

Here, $120512\ \mu s$ required for Cycle Stealing Mode.

For Burst Mode,

$25\ KB$ data transferred in $1\ s$

$\therefore 25 \times 2^{10}\ B$ data transferred in $1\ s$

$\therefore 1\ B$ data transferred in $\dfrac{1}{25 \times 2^{10}}\ s$

$\therefore 3072\ B$ data transferred in $\dfrac{1 \times 3072}{25 \times 2^{10}}\ s$

$$= \frac{3072 \times 10^9}{25 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Burst Mode} = \left(600 + \frac{3072 \times 10^9}{25 \times 2^{10}} + 400\right) ns$$
$$= 120001000\ ns$$
$$= 120001\ \mu s$$

Since $120001\ \mu s > 120512\ \mu s$, therefore Burst Mode would be more faster.

In Cycle Stealing Mode, after transferring one byte of data, releases control of the system buses and lets the CPU process an instruction and then requests access again to the bus for transfers another byte of data. On the other hand, in Burst Mode, once it is granted access to the system buses, it transfers all bytes of data in the memory data block before releasing control of the buses back to the CPU.

By continually obtaining and releasing control of the system buses, the Cycle Stealing Mode essentially interleaves instruction and data transfers. On the other hand, some important instructions could be missed while sending big data block in Burst Mode, which can create significant problem.

Therefore, statement of Shahiq is valid.

2. a) Suppose, the **AX register contains 6F24H and BX register contains 4213H**. Determine the values of **SF** and **OF** after executing **each of the following instructions sequentially. Provide a brief explanation for your answer.**

I. ADD AX, BX

II. SUB AX, BX

Solution:

I. ADD AX, BX

$$\begin{array}{r} 6\text{F}24H \\ +\ 4213H \\ \hline \text{B}137H \end{array} \qquad \begin{array}{r} 0110\ \ 1111\ \ 0010\ \ 0100 \\ +\ 0100\ \ 0010\ \ 0001\ \ 0011 \\ \hline 1011\ \ 0001\ \ 0011\ \ 0111 \end{array}$$

Here,

SF = 1 (MSB of result is 1)

OF = 1 (The result of addition of two positive number should be also a positive number, but our result is negative)

II. SUB AX, BX

[P.T.O]

$$\begin{array}{r} B137H \\ -\ 4213H \\ \hline 6F24H \end{array} \qquad \begin{array}{r} 1011\ 0001\ 0011\ 0111 \\ -\ 0100\ 0010\ 0001\ 0011 \\ \hline 0110\ 1111\ 0010\ 0100 \end{array}$$

Here,

SF = 0 (MSB of result is 0)

OF = 1 (Subtracting a positive number from a negative number is equivalent of addition of two negative number. The result of addition of two negative number should be also a negative number, but our result is positive)

2. b) Briefly explain **one** disadvantage of **memory mapped I/O**.

Solution:

In memory-mapped I/O, the microprocessor does not use the M / IO control pin. Instead, the microprocessor uses an unused address pin to distinguish between memory and I/O. In memory mapped I/O, the most significant bit (MSB) of the address can be used to distinguish between I/O and memory.

MSB = 1; I/O port selected
MSB = 0; memory location is selected

This reduces the micro-processor memory by 50%.

3. a) CS = 1437H, DS = 2153H

I) Find the last physical address of **Code Segment**.
II) Find the last physical address of **Data Segment**.
III) Find **how many** physical address slots exist that are **overlapping between both segments**?

Solution:

I) For Code Segment,

$$\begin{aligned} \text{First Physical Address} &= CS \times 10H + 0 \\ &= 1437H \times 10H \\ &= 14370H \end{aligned}$$

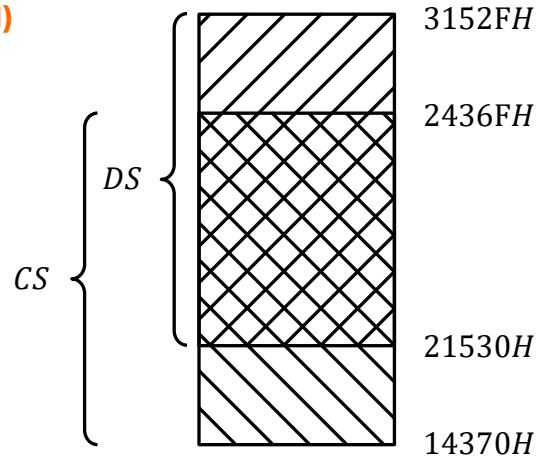
$$\begin{aligned} \therefore \text{Last Physical Address} &= 14370H + FFFFH \\ &= 2436FH \end{aligned}$$

II) For Data Segment,

$$\begin{aligned} \text{First Physical Address} &= DS \times 10H + 0 \\ &= 2153H \times 10H \\ &= 21530H \end{aligned}$$

$$\begin{aligned} \therefore \text{Last Physical Address} &= 14370H + FFFFH \\ &= 3152FH \end{aligned}$$

III)



From figure,

We can see,

$$\text{Overlapped Slots} = 2436\text{F}H - 21530H$$
$$= 2\text{E}3\text{F}H$$

$\therefore 2\text{E}3\text{F}H$ physical address slots exist that are overlapping between both segments.

3. b) A DRAM has a **data bus** of 24 bits, while an SRAM has an **address bus** of 24 bits and a **data bus** of 6 bits. Both RAMs have the same total memory capacity. Determine the **width of the address bus** of the DRAM, and calculate the total **memory capacity** for both **RAMs in megabyts (MB)**.

Solution:

Here,

$DRAM$ Data Bus $= 24\ bit$

$SRAM$ Address Bus $= 24\ bit$

$SRAM$ Data Bus $= 6\ bit$

$DRAM$ Address Bus $= ?$

Let,

$DRAM$ Address Bus $= n$

According to questions,

$DRAM$ Memory Capacity $= SRAM$ Memory Capacity

or, $2^n \times 24 = 2^{24} \times 6$

or, $2^n = \dfrac{2^{24} \times 6}{24}$

or, $n = \log_2\left(\dfrac{2^{24} \times 6}{24}\right)$

$\therefore n = 22\ bit$

Now,

Memory Capacity of both RAM $= (2^{24} \times 6)\ bit$

$$= \frac{2^{24} \times 6}{8 \times 2^{10} \times 2^{10}}\ KB$$
$$= 12\ MB$$

$\therefore$ The width of the address bus of DRAM is 22 bit and the total memory capacity for both RAMs is 12 MB.

4. a) You need to design a system where a microprocessor with a **20-bit address bus** and **16-bit data bus** is interfaced to a **192 KB RAM** system using **full decoding**

starting from address **80000H**. Each RAM chip has a **14-bit address bus** and a **16-bit data bus. Draw a block diagram showing the microprocessor, RAM chips, and full decoding logic.** Ensure the first RAM **starts at 80000H**.
Provide the second address and the second-last address of the first three RAM Chips.

Solution:

For Microprocessor,

Address Bus, $AB = 20\ bit$
Data Bus, $DB = 16\ bit$

For RAM,

Address Bus, $AB = 14\ bit$
Data Bus, $DB = 16\ bit$

Now,

$$\text{RAM Size} = (2^{14} \times 16)\ bit$$
$$= \frac{2^{14} \times 16}{8 \times 2^{10}}\ KB$$
$$= 32\ KB$$

$\therefore$ Total RAM Needed $= \left\lceil \frac{192}{32} \right\rceil = 6$

$\therefore 3:8$ decoder is needed to implement it in full decoding method.

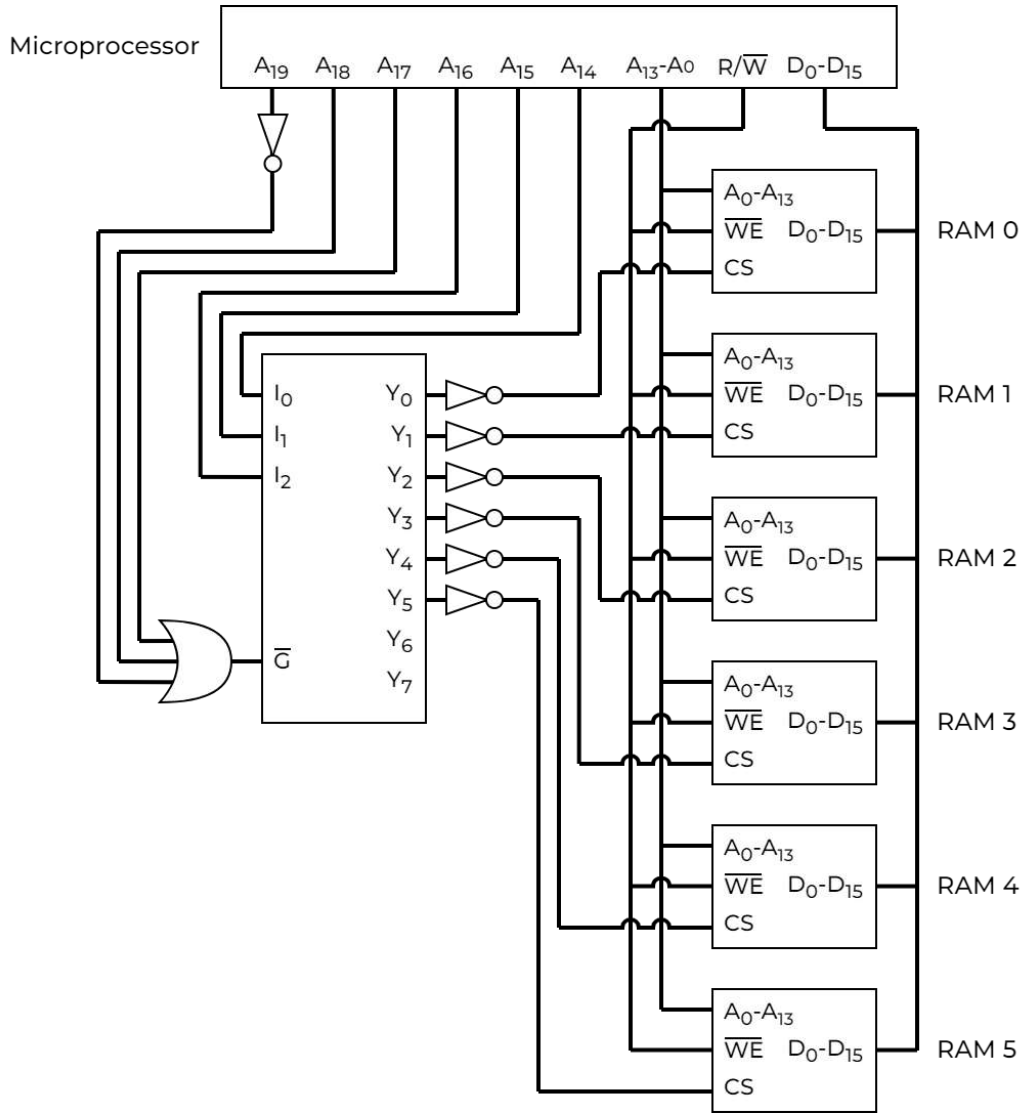
Here,

Given starting,

$$80000\ H \quad \rightarrow \quad 1000\ 0000\ 0000\ 0000\ 0000$$

The diagram has been drawn below:

[P.T.O]



The second address and the second-last address of the first three RAM Chips has been written below:

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	$A_{13} \dots A_0$	Hex	RAM
1	0	0	0	0	0	0000 ... 0001	80001 H	0
1	0	0	0	0	0	1111 ... 0000	83FFE H	
1	0	0	0	0	1	0000 ... 0001	84001 H	1
1	0	0	0	0	1	1111 ... 1110	87FFE H	
1	0	0	0	1	0	0000 ... 0001	88001 H	2
1	0	0	0	1	0	1111 ... 1110	8BFFE H	

5. a) If **007EH** and **007FH** memory locations contain **CS=0080H** for an interrupt instruction in the Interrupt Vector Table, find the corresponding Interrupt (INT) number.

Solution:

Here,

$PA \text{ of } CS(H) = 007\text{F}H$
$PA \text{ of } CS(L) = 007\text{E}H$

$\therefore PA \text{ of } IP(H) = 007\text{E}H - 1H = 007\text{D}H$
$\therefore PA \text{ of } IP(L) = 007\text{D}H - 1H = 007\text{C}H$

We know,

$$PA \text{ of } IP(L) = INT \text{ Number} \times 4H$$

$$\therefore INT \text{ Number} = \frac{INT \text{ Number}}{4H}$$
$$= \frac{007\text{C}H}{4H}$$
$$= 1\text{F}H$$

CS(H) = $007\text{F}H$
CS(L) = $007\text{E}H$
IP(H) = $007\text{D}H$
IP(L) = $007\text{C}H$

$\therefore$ Corresponding Interrupt (INT) number is $1\text{F}H$.

5. b) **Write the sequence of events that take place when a software interrupt instruction is executed.**

Solution:

The sequence of events that takes place when a software interrupt instruction is executed has been described below:

1. Push flag register onto the stack.
2. Both the interrupt (IF) and trap flag (TF) are set to 0. This disables the INTR pin and the trap or single-step feature.
3. The contents of the current code segment (CS) register are pushed onto the stack.
4. The contents of the current instruction pointer (IP) register are pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both code segment (CS) and instructor pointer (IP) so that, the next instruction executes at the interrupt service procedure address by the interrupt service.

Summer 2024

1. Transfer of bus control from processor to device takes **200 ns**. Transfer of bus control from device to processor takes **300 ns**.

1. a) If one of the input/output devices employs **DMA** in **Burst** Mode and takes **20,000,500 ns** to transfer **2048 bytes** of data. Find the data transfer rate of the device in **KB/s**.

Solution:

According to questions,

$$200\ ns + x + 300\ ns = 20000500\ ns$$
$$\text{or, } x = 20000500\ ns - (200 + 300)\ ns$$
$$\text{or, } x = 20000000\ ns$$
$$\therefore x = 0.02\ s$$

Now,

$0.2\ s$ required for transfer data of $2048\ B$

$$\therefore 1\ s \text{ required for transfer data of } \frac{2048}{0.02}\ B$$
$$= 102400\ B$$
$$= \frac{102400}{1024}\ KB$$
$$= 100\ KB$$

∴ Data transfer rate of the device is 100 KB/s.

1. b) Suppose, you are transferring **2048 bytes** of data in both Burst Mode and Cycle Stealing Mode. For the **first half** of the bytes, you use Burst Mode and for the **rest half**, you use Cycle Stealing Mode. Assume that in Cycle Stealing Mode, data is transferred 4 bytes at a time. How long will it take to transfer a total block of 2048 bytes? (Use the data transfer rate found from (a)).

Solution:

Here,

$$\text{Transferred data in each half} = \frac{2048}{2}\ B = 1024\ B$$

For first half in Burst Mode,

$100\ KB$ data transferred in $1\ s$

$$\therefore 100 \times 2^{10}\ B \text{ data transferred in } 1\ s$$
$$\therefore 1\ B \text{ data transferred in } \frac{1}{100 \times 2^{10}}\ s$$
$$\therefore 1024\ B \text{ data transferred in } \frac{1 \times 1024}{100 \times 2^{10}}\ s$$
$$= \frac{1024 \times 10^9}{100 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Burst Mode} = \left(200 + \frac{1024 \times 10^9}{100 \times 2^{10}} + 300\right) ns$$
$$= 10000500\ ns$$

For second half in Cycle Stealing Mode,

$100\ KB$ data transferred in $1\ s$

$\therefore 100 \times 2^{10}\ B$ data transferred in $1\ s$

$\therefore 1\ B$ data transferred in $\frac{1}{100 \times 2^{10}}\ s$

$\therefore 4\ B$ data transferred in $\frac{1 \times 4}{100 \times 2^{10}}\ s$

$$= \frac{4 \times 10^9}{100 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Cycle Stealing Mode} = \left(200 + \frac{4 \times 10^9}{100 \times 2^{10}} + 300\right) \times \frac{1024}{4}\ ns$$
$$= 10128000\ ns$$

Now,

Total time needed = Burst Mode time + Cycle Stealing Mode time
$$= (10000500 + 10128000)\ ns$$
$$= 20128500\ ns$$

2. a) Suppose, execution of a signed addition instruction **(7A34H + 4DC2H)** occurred. What would be the values of the sign flag (SF), parity flag (PF), carry flag (CF), and overflow flag (OF)?

Solution:

$$\begin{array}{r} 7A34H \\ +\ 4DC2H \\ \hline C7F6H \end{array} \qquad \begin{array}{r} 0111\ 1010\ 0011\ 0100 \\ +\ 0100\ 1101\ 1100\ 0010 \\ \hline 1100\ 0111\ 1111\ 1001 \end{array}$$

Here,

SF = 1 (MSB of result is 1)
PF = 1 (Even number of '1's in lower 8 bit of result)
CF = 0 (No carry out of MSB)
OF = 1 (The result of addition of two positive number should be also a positive number, but our result is negative)

2. b) If some microprocessor has a 24 bit address bus, 8 bit data bus, and its total memory is segmented into 128 KB sized blocks; how many segments should be present in the memory?

Solution:

Here,

No of slot $= 2^{AB} = 2^{24}$
Size of each slot $= DB = 8\ bit$

Now,

$$\text{Total memory} = (2^{24} \times 8)\ bit$$
$$= 2^{24}\ B$$
$$= \frac{2^{24}}{2^{10}}\ KB$$
$$= 2^{14}\ KB$$

$$\therefore \text{Number of segments} = \frac{2^{14}\ KB}{128\ KB} = 128$$

∴ 128 segments should be present in the memory.

3. a) CS = E47BH, DS = 4C18H, BX = 0100H, BP = 0F20H

To access the physical address in the **Data Segment**, what should be the value of

I) the **segment register** if the offset register holds the value of B290H.

II) the **offset register** if the segment register holds the value of 3C2FH. **Justify whether your answer is valid or not.**

III) Find the last physical address of the given **Code Segment**.

Solution:

For Data Segment,

$$\text{Physical Address} = DS \times 10H + BX$$
$$= 4\text{C}280H$$

I) $\text{Physical Address} - \text{Offset} = 4\text{C}280H - \text{B}290H$
$$= 40\text{FF}0H$$

(Valid as there are 0 at last)

$$\therefore \text{Sagment} = \frac{40\text{FF}0H}{10H}$$
$$= 40\text{FF}H$$

II) Physical Address = Sagment × $10H$ + Offset

$\therefore$ Offset = Physical Address − Sagment × $10H$
$$= 4\text{C}280H - 3\text{C}2\text{F}H \times 10H$$
$$= \text{FF}90H$$

(Valid as it is non-negative and under 16 bit)

III) For Code Segment,

$$\text{First Physical Address} = CS \times 10H + 0$$
$$= \text{E}74\text{B}H \times 10H$$
$$= \text{E}74\text{B}0H$$

$$\therefore \text{Last Physical Address} = \text{E}74\text{B}0H + \text{FFFF}H$$
$$= \text{F}74\text{AF}H$$

3. b) RAM[A] has a **data bus** of 32 bits, while RAM[B] has an **address bus** of 20 bits and a **data bus** of 8 bits. Both RAMs have the same total memory capacity. Determine the **width of the address bus** of RAM[A], and calculate the total **memory capacity** for both RAMs.

Solution:

Here,

$RAM[A]$ Data Bus $= 32\ bit$
$RAM[B]$ Address Bus $= 20\ bit$
$RAM[B]$ Data Bus $= 8\ bit$
$RAM[A]$ Address Bus $= ?$

Let,

$RAM[A]$ Address Bus $= n$

According to questions,

$RAM[A]$ Memory Capacity $= RAM[B]$ Memory Capacity

or, $2^n \times 32 = 2^{20} \times 8$

or, $2^n = \dfrac{2^{20} \times 8}{32}$

or, $n = \log_2\left(\dfrac{2^{20} \times 8}{32}\right)$

$\therefore n = 18\ bit$

Now,

$$\text{Memory Capacity of both RAM} = (2^{20} \times 8)\ bit$$
$$= \frac{2^{24} \times 8}{8 \times 2^{10}}\ KB$$
$$= 1024\ KB$$
$$= 1\ MB$$

∴ The width of the address bus of RAM[A] is 18 bit and the total memory capacity for both RAMs is 1 MB.

4. a) **Draw the diagram** of a microprocessor with a 18-bit address bus and 8-bit data bus interfaced to 4 KB RAM system using the **partial decoding method**. Each RAM chip has a 10-bit address bus and 8-bit data bus. Provide the corresponding **address range** (starting and end address) as well.

Solution:

For Microprocessor,

Address Bus, $AB = 18\ bit$
Data Bus, $DB = 8\ bit$

For RAM,

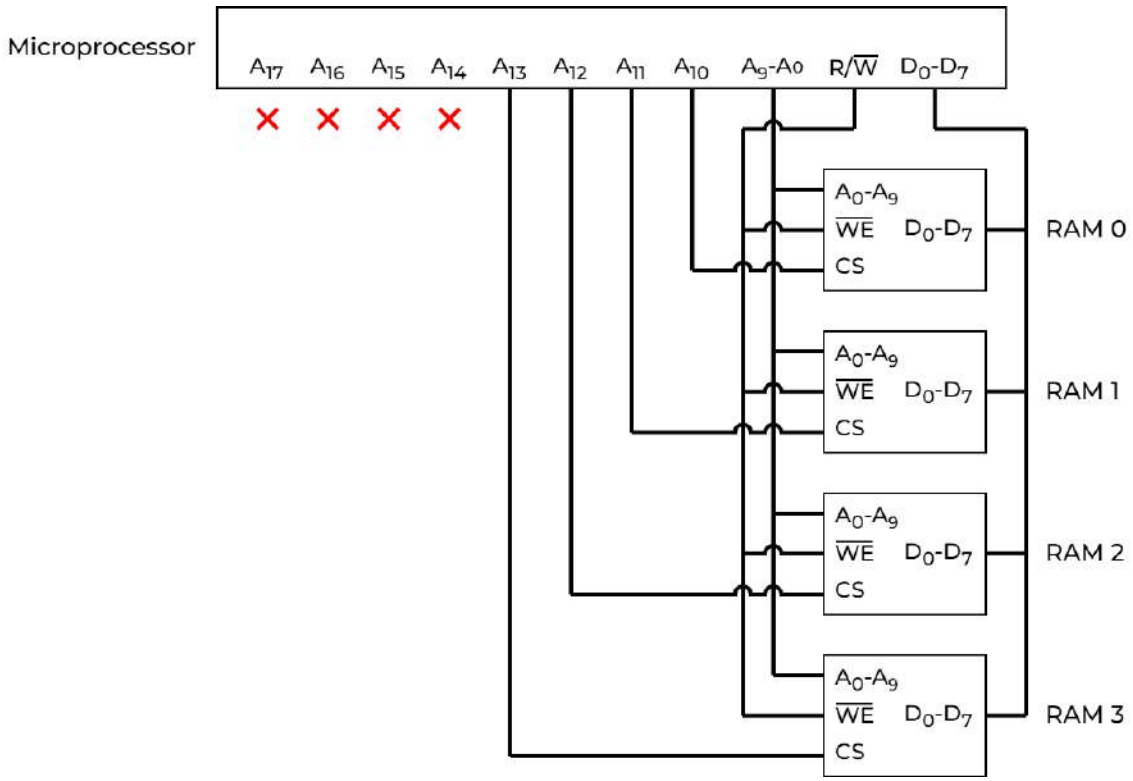
Address Bus, $AB = 10\ bit$
Data Bus, $DB = 8\ bit$

Now,

$$\text{RAM Size} = (2^{10} \times 8)\ bit$$
$$= \frac{2^{10} \times 8}{8 \times 2^{10}}\ KB$$
$$= 1\ KB$$

$\therefore$ Total RAM Needed $= \left\lceil \frac{4}{1} \right\rceil = 4$

The diagram has been drawn below:



Address Mapping:

A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	$A_9 \dots A_0$	Hex	RAM
0	0	0	0	0	0	0	1	0 … 0	00400 H	0
0	0	0	0	0	0	0	1	1 … 1	007FF H	
0	0	0	0	0	0	1	0	0 … 0	00800 H	1
0	0	0	0	0	0	1	0	1 … 1	00BFF H	
0	0	0	0	0	1	0	0	0 … 0	01000 H	2
0	0	0	0	0	1	0	0	1 … 1	013FF H	
0	0	0	0	1	0	0	0	0 … 0	02000 H	3
0	0	0	0	1	0	0	0	1 … 1	023FF H	

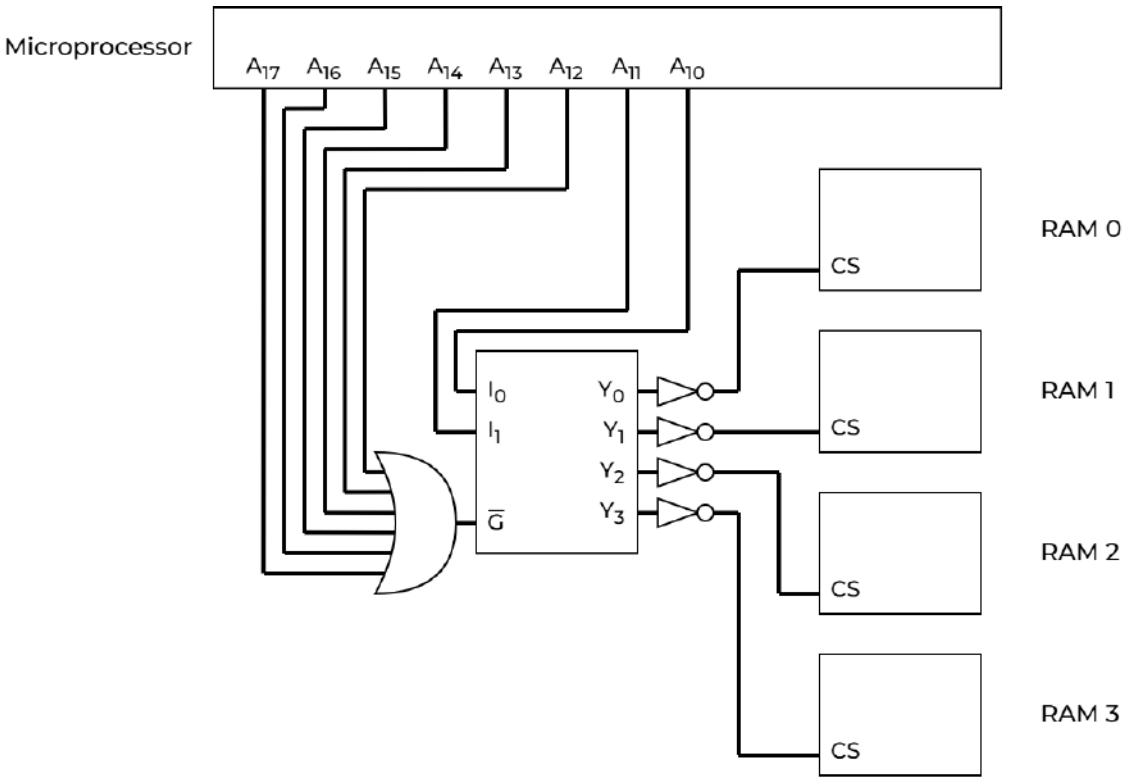
4. b) What modifications are needed to implement the same system as described in part (a) using the **full decoding method**? Draw only the **modified part**.

Compare both methods (partial and full decoding) for this case, and determine which method is better and why.

Solution:

For full decoding method, $2:4$ decoder is needed.

The modified part has been drawn below:



Comparison of partial and full decoding methods:

- Waste of address space in partial decoding occur, but in full decoding no waste of address space.
- Address map is not contiguous in partial decoding, it is sparsely distributed, but in full decoding address map is contiguous.
- Data collision for hardware fault may occur in partial decoding, but in full decoding data collision is not occur.
- Memory foldback (address not unique for memory locations) and it wastes memory space for partial decoding but in full decoding each memory location has unique address.
- For full decoding more hardware needs compare to partial decoding.

Therefore, from the comparison, we can say that full decoding is better method.

5. a) In an **8086 microprocessor**,
CS = 0080 H , IP = 00FF H , Flag Register = FFFF H
Describe the **sequence** of **events** that the 8086 microprocessor will execute when it encounters a **software interrupt** based on the given values. Also, show the **stack contents** during this process.

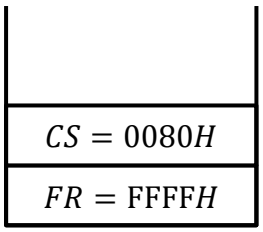
Solution:

Sequence of event has been described below:

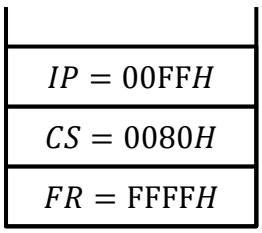
1. Push flag register ($\mathrm{FFFF}H$) onto the stack.
2. Both the interrupt (IF) and trap flag (TF) are set to 0. This disables the INTR pin and the trap or single-step feature.
3. The contents of the current code segment resister ($CS = 0080H$) are pushed onto the stack.
4. The contents of the current instruction pointer resister ($IP = 00\mathrm{FF}H$) are pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both code segment ($CS = 0080H$) and instructor pointer ($IP = 00\mathrm{FF}H$) so that, the next instruction executes at the interrupt service procedure address by the interrupt service.

Stack contents:

Pushing $FF = \mathrm{FFFF}H$



Pushing $CS = 0080H$



Pushing $IP = 00\mathrm{FF}H$

5. b) The memory addresses for Overflow Interrupt and Floating Point Error in the vector table are (10 H - 13H) and (40 H - 43H) respectively. Which interrupt has a **higher priority** and why?

Solution:

We know,

$$PA \text{ of } IP(L) = INT \text{ Number} \times 4H$$

For Overflow Interrupt,

$$PA \text{ of } IP(L) = 10H$$
$$\therefore INT \text{ Number} = \frac{10H}{4H} = 4H$$

For Floating Point Error,

$$PA \text{ of } IP(L) = 40H$$
$$\therefore INT \text{ Number} = \frac{40H}{4H} = 10H$$

Since number of Overflow Interrupt has lower, therefore Overflow Interrupt has a higher priority.

1. Transfer of bus control from processor to device takes **300 ns**. Transfer of bus control from device to processor takes **200 ns**.

1. a) If one of the input/output devices employs **DMA** in **cycle stealing** mode and takes **12564000 ns** to transfer **512 bytes** of data. If data is transferred 4 bytes at a time, what is the data transfer rate of the device in **KB/s**?

Solution:

According to questions,

$$(300 + x + 200) \times \frac{512}{4} = 12564000$$

$$\text{or, } x = \left(12564000 \times \frac{4}{512}\right) - (300 + 200)$$

$$\text{or, } x = 97656.25\ ns$$

$$\text{or, } x = \frac{97656.25}{10^9}\ s$$

$$\therefore x = 0.00009765625\ s$$

Now,

$0.00009765625\ s$ required for transfer data of $4\ B$

$\therefore 1\ s$ required for transfer data of $\frac{4}{0.00009765625}\ B$

$$= 40960\ B$$

$$= \frac{40960}{2^{10}}\ KB$$

$$= 40\ KB$$

∴ Data transfer rate of the device is 40 KB/s.

1. b) Suppose, you are transferring **8192 bytes** of data. Which mode (**burst mode/cycle stealing mode**) will be faster to transfer this data? Assume that in cycle stealing mode, data is transferred **4 bytes at a time**. (Use the data transfer rate found from(a))

Solution:

For Burst Mode,

$40\ KB$ data transferred in $1\ s$

$\therefore 40 \times 2^{10}\ B$ data transferred in $1\ s$

$\therefore 1\ B$ data transferred in $\frac{1}{40 \times 2^{10}}\ s$

$\therefore 8192\ B$ data transferred in $\frac{1 \times 8192}{40 \times 2^{10}}\ s$

$$= \frac{8192 \times 10^9}{40 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Burst Mode} = \left(300 + \frac{8192 \times 10^9}{40 \times 2^{10}} + 200\right) ns$$
$$= 200000500\ ns$$

For Cycle Stealing Mode,

$40\ KB$ data transferred in $1\ s$

$\therefore 40 \times 2^{10}\ B$ data transferred in $1\ s$

$\therefore 1\ B$ data transferred in $\frac{1}{40 \times 2^{10}}\ s$

$\therefore 4\ B$ data transferred in $\frac{1 \times 4}{40 \times 2^{10}}\ s$

$$= \frac{4 \times 10^9}{40 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Cycle Stealing Mode} = \left(300 + \frac{4 \times 10^9}{40 \times 2^{10}} + 200\right) \times \frac{8192}{4}\ ns$$
$$= 201024000\ ns$$

Therefore, burst mode will be faster to transfer this data.

2. a) Suppose, execution of a signed substractional instruction **(8000H - 0001H)** occurred, What would be the value of carry flag (CF), sign flag (SF), parity flag (PF), overflow flag (OF)?

Solution:

$$\begin{array}{r} 8000\text{H} \\ -\ 0001\text{H} \\ \hline 7FFF\text{H} \end{array} \qquad \begin{array}{r} 1000\ 0000\ 0000\ 0000 \\ -\ 0000\ 0000\ 0000\ 0001 \\ \hline 0111\ 1111\ 1111\ 1111 \end{array}$$

Here,

CF = 0 (No carry out of MSB)
SF = 0 (MSB of result is 0)
PF = 1 (Even number of '1's in lower 8 bit of result)
OF = 1 (Subtracting a positive number from a negative number is equivalent of addition of two negative number. The result of addition of two negative number should be also a negative number, but our result is positive)

2. b) Proof mathematically, the maximum size of a segment is **64KB** in an 8086 microprocessor.

Solution:

We know,

For 8086 microprocessor,
Offset size $= 16\ bit$

So,
Memory for address location of segment $= 2^{16}\ bit$
Size of each location of segment $= 8\ bit$

Now,

$$\begin{aligned}\text{Size of a segment} &= (2^{16} \times 8)\ bit \\ &= 2^{16}\ Byte \\ &= \frac{2^{16}}{2^{10}}\ KB \\ &= 2^{6}\ KB \\ &= 64\ KB\end{aligned}$$

∴ The maximum size of a segment is 64KB in an 8086 microprocessor. (Proven)

3. a) SS = 2526H BX = 0020H BP = 1105H CS = A231H

To access the physical address in the **Stack Segment**, what should be the value of

I) the **segment register** if the offset register holds the value of 3C5AH.

II) the **offset register** if the segment register holds the value of 213AH. **Justify whether your answer is valid or not.**

III) Find the first and last physical address of the given **Code Segment**.

Solution:

For Stack Segment,

$$\begin{aligned}\text{Physical Address} &= SS \times 10H + BP \\ &= 2526H \times 10H + 1105H \\ &= 26365H\end{aligned}$$

I) $\text{Physical Address} - \text{Offset} = 26365H - 3\text{C5A}H$
$= 2270\text{B}H$

(Invalid as there are no 0 at last)

II) $\text{Physical Address} = \text{Segment} \times 10H + \text{Offset}$

∴ $\text{Offset} = \text{Physical Address} - \text{Segment} \times 10H$
$= 26365H - 213\text{A}H \times 10H$
$= 4\text{FC}5H$

(Valid as it is non-negative and under 16 bit)

III) For Code Segment,

$$\begin{aligned}\text{First Physical Address} &= CS \times 10H + 0 \\ &= \text{A}231H \times 10H \\ &= \text{A}2310H\end{aligned}$$

∴ $\text{Last Physical Address} = \text{A}2310H + \text{FFFF}H$
$= \text{B}230\text{F}H$

3. b) RAM[A] has a **data bus** of 16 bits and RAM[B] has an **address bus** of 17 bits. Both RAMs have a total memory capacity of 128KB. What is the **address bus** width of RAM[A] and **data bus** width of RAM[B]?

Solution:

Here,

$RAM[A]$ Data Bus $= 16\ bit$
$RAM[B]$ Address Bus $= 17\ bit$
Both RAM memory Capacity $= 128\ KB$
$= 128 \times 2^{10} \times 8\ bits$
$RAM[A]$ Address Bus $= ?$
$RAM[B]$ Data Bus $= ?$

For $RAM[A]$,

$$2^{AB} \times 16 = 128 \times 2^{10} \times 8$$

$$\text{or, } 2^{AB} = \frac{128 \times 2^{10} \times 8}{16}$$

$$\text{or, } AB = \log_2\left(\frac{128 \times 2^{10} \times 8}{16}\right)$$

$$\therefore AB = 16\ bit$$

For $RAM[B]$,

$$2^{17} \times DB = 128 \times 2^{10} \times 8$$

$$\text{or, } DB = \frac{128 \times 2^{10} \times 8}{2^{17}}$$

$$\therefore DB = 8\ bit$$

∴ Address bus width of RAM[A] and data bus width of RAM[B] are respectively 16 bit and 8 bit.

4. a) **Draw the diagram** of a microprocessor with a 20-bit address bus and 8-bit data bus interfaced to 8 KB RAM system using the **full decoding method**. Each RAM chip has a 11-bit address bus and 8-bit data bus. Draw the circuit to address memory range **58000H – 59FFFH**. Provide the **address mapping** as well.

Solution:

For Microprocessor,

Address Bus, $AB = 20\ bit$
Data Bus, $DB = 8\ bit$

For RAM,

Address Bus, $AB = 11\ bit$
Data Bus, $DB = 8\ bit$

Now,

$$\text{RAM Size} = (2^{11} \times 8)\ bit$$
$$= \frac{2^{11} \times 8}{8 \times 2^{10}}\ KB$$
$$= 2\ KB$$

$$\therefore \text{Total RAM Needed} = \left\lceil \frac{8}{2} \right\rceil = 4$$

$\therefore 2:4$ decoder is needed to implement it in full decoding method.

Here,

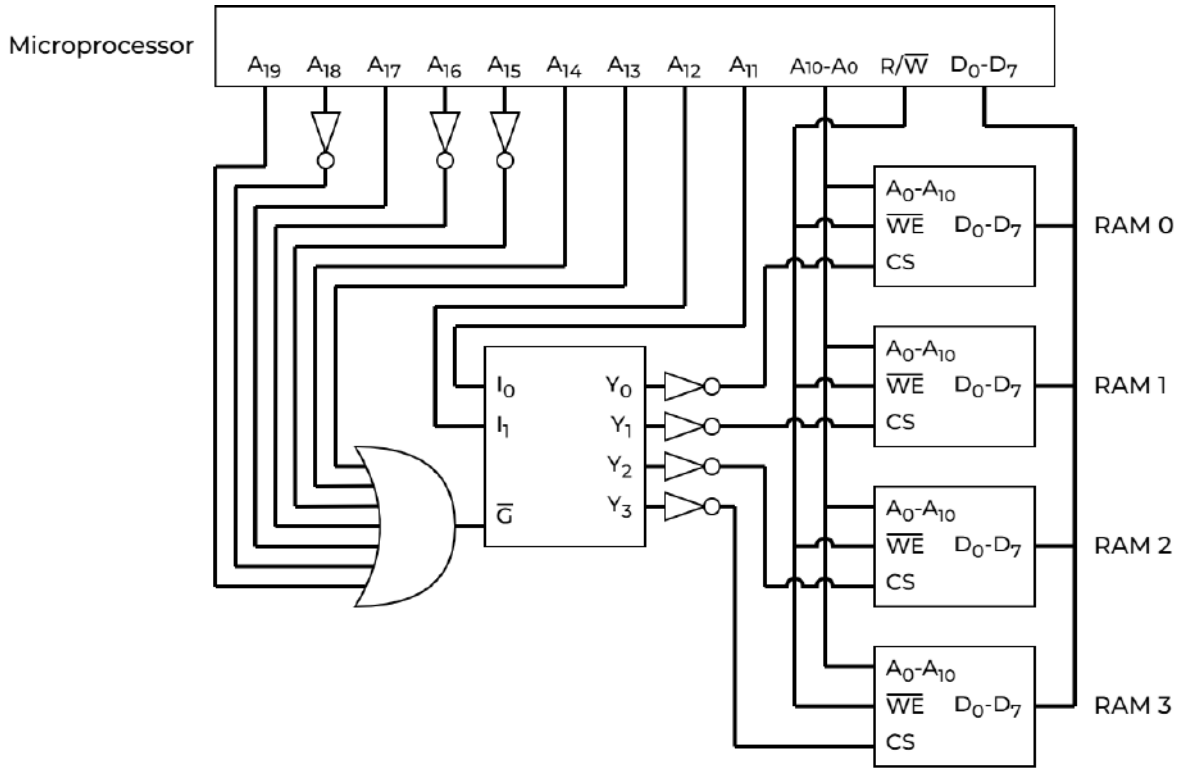
Given address memory range,

$$58000\,H \downarrow 59FFF\,H$$

$$\underbrace{0101\ 100}_{\text{Fixed Part}}\ \underbrace{0\ 0}_{\text{Decoder Input}}\ \underbrace{000\ 0000\ 0000}_{\text{Address Bus}}$$

$$\underbrace{0101\ 100}_{\text{Fixed Part}}\ \underbrace{1\ 1}_{\text{Decoder Input}}\ \underbrace{111\ 1111\ 1111}_{\text{Address Bus}}$$

The diagram has been drawn below:



Address Mapping:

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	$A_{10} \dots A_0$	Hex	RAM
0	1	0	1	1	0	0	0	0	0 … 0	58000 H	0
0	1	0	1	1	0	0	0	0	1 … 1	587FF H	
0	1	0	1	1	0	0	0	1	0 … 0	58800 H	1
0	1	0	1	1	0	0	0	1	1 … 1	58FFF H	
0	1	0	1	1	0	0	1	0	0 … 0	59000 H	2
0	1	0	1	1	0	0	1	0	1 … 1	597FF H	
0	1	0	1	1	0	0	1	1	0 … 0	59800 H	3
0	1	0	1	1	0	0	1	1	1 … 1	59FFF H	

5. a) In the interrupt vector table, the **upper byte of CS** for the ultrasonic motion detector is in the physical address **0036BH**, and the **upper byte of IP** for the fire alarm sensor is in the physical address **001E5H**.

I) Determine each sensor's interrupt number in hexadecimal.

II) If both sensors send interrupt signals to the microprocessor at the same time, which one will be executed first and why?

Solution:

I) We know,

PA of $IP(L) = INT$ Number $\times 4H$

For ultrasonic motion detector,

PA of $CS(H) = 0036BH$

$\therefore PA$ of $IP(L) = 00368H$

$$\therefore INT \text{ Number} = \frac{00368H}{4H}$$

$$= \text{DA}H$$

For fire alarm sensor,

PA of $IP(H) = 001\text{E}5H$

$\therefore PA$ of $IP(L) = 001\text{E}4H$

$$\therefore INT \text{ Number} = \frac{001\text{E}4H}{4H}$$

$$= 79H$$

For ultrasonic sensor,

CS(H) = $0036BH$
CS(L) = $0036AH$
IP(H) = $00369H$
IP(L) = $00368H$

For fire alert system

CS(H) = $001\text{E}7H$
CS(L) = $001\text{E}6H$
IP(H) = $001\text{E}5H$
IP(L) = $001\text{E}4H$

II) Since INT number of fire alarm sensor interrupt is lower, therefore fire alarm sensor Interrupt has a higher priority than $\text{DA}H$ and it will be executed first.

5. b) If there are a total 128 interrupts in an 8086 microprocessor then what will be the size of the interrupt vector table?

Solution:

We know,

Size of 1 interrupts $= 8 \times 4\ bits$

$$= 4\ Bytes$$

$\therefore$ For 128 interrupts,

Size of Interrupt Vector Table $= 4 \times 128\ Bytes$

$$= 512\ Bytes$$

$\therefore$ Size of the interrupt vector table will be 512 byte.

1. Transfer of bus control from processor to device takes **100 ns**. Transfer of bus control from device to processor takes **200 ns**.

1. a) If one of the input/output devices employs **DMA** in **burst** mode and takes 10000300 ns to transfer 1536 bytes of data, what is the data transfer rate of the device in KB/s?

Solution:

According to questions,

$$100 + x + 200 = 10000300$$
$$\text{or, } x = 10000300 - (100 + 200)$$
$$\text{or, } x = 10000000 \ ns$$
$$\text{or, } x = \frac{10000000}{10^9} \ s$$
$$\therefore x = 0.01 \ s$$

Now,

$0.01 \ s$ required for transfer data of $1536 \ B$

$$\therefore 1 \ s \text{ required for transfer data of } \frac{1536}{0.01} \ B$$
$$= 153600 \ B$$
$$= \frac{153600}{2^{10}} \ KB$$
$$= 150 \ KB$$

∴ Data transfer rate of the device is 150 KB/s.

1. b) Suppose, you are transferring 1536 bytes of data in both burst mode and cycle stealing mode. For the first **one-third** of the bytes, you use **burst mode** and for the rest **two-third**, you use **cycle stealing mode**. Assume that in cycle stealing mode, data is transferred **4 bytes at a time**. How long will it take to transfer a block of 1536 bytes? (Use the data transfer rate found from(a))

Solution:

Here,

$$\text{Transferred data in first one-third time} = 1536 \times \frac{1}{3} \ B = 512 \ B$$
$$\text{Transferred data in rest two-third time} = 1536 \times \frac{2}{3} \ B = 1024 \ B$$

For first one-third time in Burst Mode,

$150 \ KB$ data transferred in $1 \ s$

$$\therefore 150 \times 2^{10} \ B \text{ data transferred in } 1 \ s$$
$$\therefore 1 \ B \text{ data transferred in } \frac{1}{150 \times 2^{10}} \ s$$

$$\therefore 512\ B \text{ data transferred in } \frac{1 \times 512}{150 \times 2^{10}}\ s$$
$$= \frac{512 \times 10^9}{150 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Burst Mode} = \left(100 + \frac{512 \times 10^9}{150 \times 2^{10}} + 200\right) ns$$
$$= 3333633.333\ ns$$

For rest two-third time in Cycle Stealing Mode,

$$150\ KB \text{ data transferred in } 1\ s$$
$$\therefore 150 \times 2^{10}\ B \text{ data transferred in } 1\ s$$
$$\therefore 1\ B \text{ data transferred in } \frac{1}{150 \times 2^{10}}\ s$$
$$\therefore 4\ B \text{ data transferred in } \frac{1 \times 4}{150 \times 2^{10}}\ s$$
$$= \frac{4 \times 10^9}{150 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Cycle Stealing Mode} = \left(100 + \frac{4 \times 10^9}{150 \times 2^{10}} + 200\right) \times \frac{1024}{4}\ ns$$
$$= 6743466.667\ ns$$

Now,

$$\text{Total time needed} = \text{Burst Mode time} + \text{Cycle Stealing Mode time}$$
$$= (3333633.333 + 6743466.667)\ ns$$
$$= 10077100\ ns$$

2. a) Suppose, execution of a signed additional instruction (6BCDH+5234H) occurred, What would be the value of zero flag (ZF), sign flag (SF), parity flag(PF), overflow flag(OF)?

Solution:

$$\begin{array}{r} 6BCD\text{H} \\ +\ 5234\text{H} \\ \hline BE01\text{H} \end{array} \qquad \begin{array}{r} 0110\ 1011\ 1100\ 1101 \\ +\ 0101\ 0010\ 0011\ 0100 \\ \hline 1011\ 1110\ 0000\ 0001 \end{array}$$

Here,

ZF = 0 (Non-zero result)
SF = 1 (MSB of result is 1)
PF = 0 (Number of '1's in lower 8 bit of result is not even)
OF = 1 (The result of addition of two positive number should be also a positive number, but our result is negative)

2. b) Describe in short the four general purpose registers of the 8086 microprocessor.

Solution:

The 8086 microprocessor has four general-purpose registers, each 16 bits wide, and they can be used for a variety of operations. These registers are described below:

AX (Accumulator Register): Used for arithmetic, logic, and data transfer operations.

BX (Base Register): Primarily used as a base pointer for memory addressing.

CX (Count Register): Used as a counter for loop and iterative operations.

DX (Data Register): Used in operations requiring two registers, such as division and multiplication. Also used for I/O operations to specify port numbers.

3. a) Suppose the address 79E4H : 2A8CH has an instruction. To access this instruction, what should be the value of

I) the **segment register** if the offset register holds the value of 5A3CH.
II) the **segment register** if the offset register holds the value of 5A2DH.
II) the **offset register** if the segment register holds the value of 2679H.

Justify whether your answer is valid or not.

Solution:

For $79\text{E}4H : 2\text{A}8\text{C}H$,

$$\begin{aligned}\text{Physical Address} &= \text{Segment} \times 10H + \text{Offset} \\ &= 79\text{E}4H \times 10H + 2\text{A}8\text{C}H \\ &= 7\text{C}8\text{C}\text{C}H\end{aligned}$$

I) $$\begin{aligned}\text{Physical Address} - \text{Offset} &= 7\text{C}8\text{C}\text{C}H - 5\text{A}3\text{C}H \\ &= 76\text{E}90H\end{aligned}$$

(Valid as there are 0 at last)

$$\therefore \text{Sagment} = \frac{76\text{E}90H}{10H}$$
$$= 76\text{E}9H$$

II) $$\begin{aligned}\text{Physical Address} - \text{Offset} &= 7\text{C}8\text{C}\text{C}H - 5\text{A}2\text{D}H \\ &= 76\text{E}9\text{F}H\end{aligned}$$

(Invalid as there are no 0 at last)

III) $\text{Physical Address} = \text{Segment} \times 10H + \text{Offset}$

$$\begin{aligned}\therefore \text{Offset} &= \text{Physical Address} - \text{Segment} \times 10H \\ &= 7\text{C}8\text{C}\text{C}H - 2679H \times 10H \\ &= 5613\text{C}H\end{aligned}$$

(Invalid since it is higher than 16 bits)

3. b) RAM[A] has a **data bus** of 32 bits and RAM[B] has an **address bus** of 26 bits. Both RAMs have a total memory capacity of 128 MB. What is the **address bus** width of RAM[A] and **data bus** width of RAM[B]?

Solution:

Here,

$RAM[A]$ Data Bus $= 32\ bit$
$RAM[B]$ Address Bus $= 26\ bit$
Both RAM memory Capacity $= 128\ MB$
$= 128 \times 2^{10} \times 2^{10} \times 8\ bits$
$RAM[A]$ Address Bus $= ?$
$RAM[B]$ Data Bus $= ?$

For $RAM[A]$,

$$2^{AB} \times 32 = 128 \times 2^{10} \times 2^{10} \times 8$$

or, $2^{AB} = \dfrac{128 \times 2^{10} \times 2^{10} \times 8}{32}$

or, $AB = \log_2\left(\dfrac{128 \times 2^{10} \times 2^{10} \times 8}{32}\right)$

$\therefore AB = 25\ bit$

For $RAM[B]$,

$$2^{26} \times DB = 128 \times 2^{10} \times 2^{10} \times 8$$

or, $DB = \dfrac{128 \times 2^{10} \times 2^{10} \times 8}{2^{26}}$

$\therefore DB = 16\ bit$

$\therefore$ Address bus width of RAM[A] and data bus width of RAM[B] is respectively 25 bit and 16 bit.

4. a) **Draw the diagram** of a microprocessor with a 20-bit address bus and 8-bit data bus interfaced to 28 KB RAM system using the **full decoding method**. Each RAM chip has a 13-bit address bus and 8-bit data bus. Provide the corresponding address range (starting address and end address) for the system.

Solution:

For Microprocessor,

Address Bus, $AB = 20\ bit$
Data Bus, $DB = 8\ bit$

For RAM,

Address Bus, $AB = 13\ bit$
Data Bus, $DB = 8\ bit$

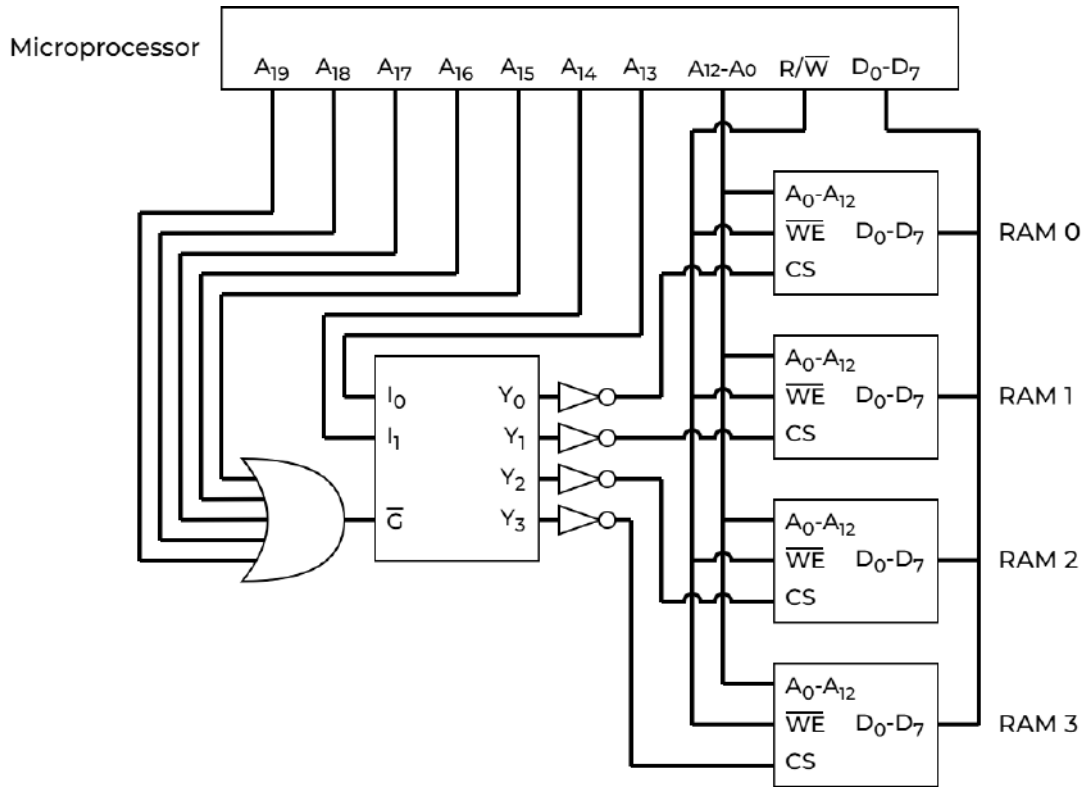
Now,

RAM Size $= (2^{13} \times 8)\ bit$
$= \dfrac{2^{13} \times 8}{8 \times 2^{10}}\ KB$
$= 8\ KB$

$\therefore$ Total RAM Needed $= \left\lceil \dfrac{28}{8} \right\rceil \approx 4$

$\therefore 2:4$ decoder is needed to implement it in full decoding method.

The diagram has been drawn below:



Address Mapping:

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	$A_{12} \dots A_0$	Hex	RAM
0	0	0	0	0	0	0	0 … 0	00000 H	0
0	0	0	0	0	0	0	1 … 1	01FFF H	
0	0	0	0	0	0	1	0 … 0	02000 H	1
0	0	0	0	0	0	1	1 … 1	03FFF H	
0	0	0	0	0	1	0	0 … 0	54000 H	2
0	0	0	0	0	1	0	1 … 1	05FFF H	
0	0	0	0	0	1	1	0 … 0	06000 H	3
0	0	0	0	0	1	1	1 … 1	07FFF H	

4. b) Modify the circuit of (a) to address memory range B0000H – B6FFFH. Draw the diagram as before and provide the modified address range. **You need only draw the part of the diagram that goes through any modification**.

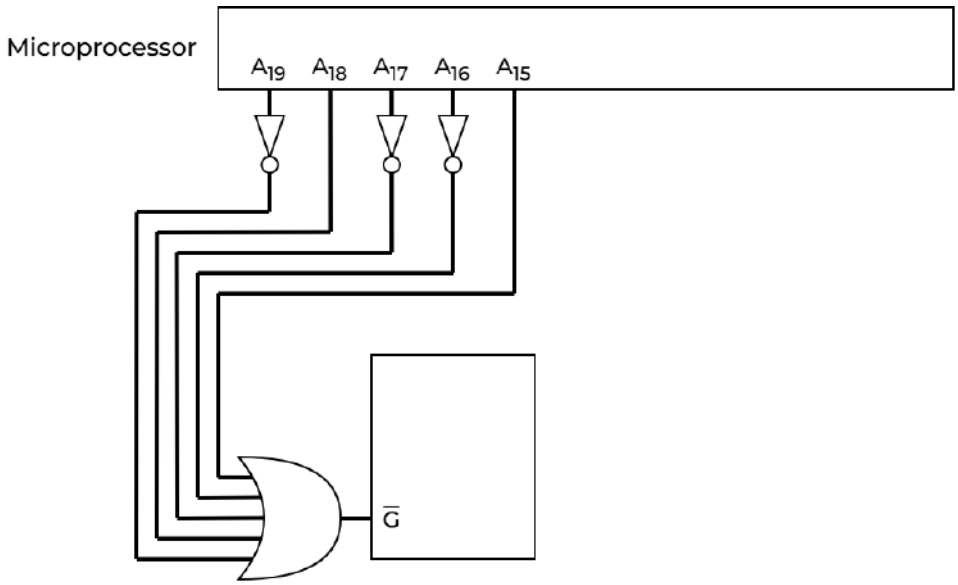
Solution:

Here,
Given address memory range,

[P.T.O]

$$\begin{array}{c} \text{B0000}\,H \\ \downarrow \\ \text{B6FFF}\,H \end{array} \qquad \begin{array}{c} 1011\ \ 0\ \ \ 00\ \ \ 0\ \ 0000\ \ 0000\ \ 0000 \\ \downarrow \quad\ \downarrow \qquad\qquad\ \downarrow \\ \underbrace{1011\ \ 0}_{\text{Fixed Part}}\ \ \underbrace{11}_{\text{Decoder Input}}\ \ \underbrace{0\ \ 1111\ \ 1111\ \ 1111}_{\text{Address Bus}} \end{array}$$

Here we can see that given address memory range does not cover the all memory addresses. However, the modified diagram has been drawn below:



5. a) Calculate the memory location of **CS** and **IP** for the interrupt **INT EH** in the interrupt vector table.

Solution:

We know,

$$\begin{aligned} PA \text{ of } IP(L) &= INT \text{ Number} \times 4H \\ &= \text{E}H \times 4H \\ &= 38H \end{aligned}$$

Now,

$$\begin{aligned} &PA \text{ of } IP(L) = 38H \\ \therefore\ &PA \text{ of } IP(H) = 38H + 1H = 39H \\ \therefore\ &PA \text{ of } CS(L) = 39H + 1H = 3\text{A}H \\ \therefore\ &PA \text{ of } CS(H) = 3\text{A}H + 1H = 3\text{B}H \end{aligned}$$

CS(H) = 3BH
CS(L) = 3AH
IP(H) = 39H
IP(L) = 38H

5. b) What is the sequence of events that takes place when a software interrupt instruction is executed?

Solution:

The sequence of events that takes place when a software interrupt instruction is executed has been described below:

6. Push flag register onto the stack.
7. Both the interrupt (IF) and trap flag (TF) are set to 0. This disables the INTR pin and the trap or single-step feature.

8. The contents of the current code segment (CS) register are pushed onto the stack.
9. The contents of the current instruction pointer (IP) register are pushed onto the stack.
10. The interrupt vector contents are fetched, and then placed into both code segment (CS) and instructor pointer (IP) so that, the next instruction executes at the interrupt service procedure address by the interrupt service.

5. c) Explain the function of **"IRET"** in interrupt service procedure.

Solution:

The IRET (Interrupt Return) instruction in the 8086 microprocessor is used at the end of an Interrupt Service Routine (ISR) to return control to the program that was interrupted. It restores the processor state to what it was before the interrupt occurred.

1. Transfer of bus control from processor to device takes **100 ns**. Transfer of bus control from device to processor takes **150 ns**.

1. a) If one of the input/output devices employs **DMA** in **burst** mode and takes 10000250 ns to transfer 512 bytes of data, what is the data transfer rate of the device in KB/s?

Solution:

According to questions,

$$100 + x + 150 = 10000250$$
$$\text{or, } x = 10000250 - (100 + 150)$$
$$\text{or, } x = 10000000\ ns$$
$$\text{or, } x = \frac{10000000}{10^9}\ ns$$
$$\therefore x = 0.01\ s$$

Now,

$0.01\ s$ required for transfer data of $512\ B$

$$\therefore 1\ s \text{ required for transfer data of } \frac{512}{0.01}\ B$$
$$= 51200\ B$$
$$= \frac{102400}{2^{10}}\ KB$$
$$= 50\ KB$$

∴ Data transfer rate of the device is 50 KB/s.

1. b) Suppose, you are transferring 512 bytes of data in both burst mode and cycle stealing mode. For the first half of the bytes, you use burst mode and for the rest half, you use cycle stealing mode. Assume that in cycle stealing mode, data is transferred 2 bytes at a time. How long will it take to transfer a block of 512 bytes? (Use the data transfer rate found from (a))

Solution:

Here,

$$\text{Transferred data in each half} = \frac{512}{2}\ B = 256\ B$$

For first half in Burst Mode,

$50\ KB$ data transferred in $1\ s$

$$\therefore 50 \times 2^{10}\ B \text{ data transferred in } 1\ s$$
$$\therefore 1\ B \text{ data transferred in } \frac{1}{50 \times 2^{10}}\ s$$
$$\therefore 256\ B \text{ data transferred in } \frac{1 \times 256}{50 \times 2^{10}}\ s = \frac{256 \times 10^9}{50 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Burst Mode} = \left(100 + \frac{256 \times 10^9}{50 \times 2^{10}} + 150\right) ns$$
$$= 5000250\ ns$$

For second half in Cycle Stealing Mode,

$50\ KB$ data transferred in $1\ s$

$\therefore 50 \times 2^{10}\ B$ data transferred in $1\ s$

$\therefore 1\ B$ data transferred in $\frac{1}{50 \times 2^{10}}\ s$

$\therefore 2\ B$ data transferred in $\frac{1 \times 2}{50 \times 2^{10}}\ s$

$$= \frac{2 \times 10^9}{50 \times 2^{10}}\ ns$$

$$\therefore \text{Time needed for Cycle Stealing Mode} = \left(100 + \frac{2 \times 10^9}{50 \times 2^{10}} + 150\right) \times \frac{256}{2}\ ns$$
$$= 5032000\ ns$$

Now,

Total time needed = Burst Mode time + Cycle Stealing Mode time
$$= (5000250\ + 5032000)\ ns$$
$$= 10032250\ ns$$

2. a) **Suppose, execution of a signed additional instruction (4F37H + 3012H) occurred, what would be the value of zero flag (ZF), sign flag (SF), parity flag (PF), overflow flag (OF), carry flag (CF)?**

Solution:

$$\begin{array}{r} 4F37H \\ +\ 3012H \\ \hline 7F49H \end{array} \qquad \begin{array}{r} 0100\ 1111\ 0011\ 0111 \\ +\ 0011\ 0000\ 0001\ 0010 \\ \hline 0111\ 1111\ 0100\ 1001 \end{array}$$

Here,

ZF = 0 (Non-zero result)
SF = 0 (MSB of result is 0)
PF = 0 (Number of '1's in lower 8 bit of result is not even)
OF = 0 (Result of addition of two positive number is also positive)
CF = 0 (No carry out of MSB)

2. b) **Name one advantage of using memory segmentation in a microprocessor.**

Solution:

One significant advantage of using memory segmentation in a microprocessor is efficient use of memory. Memory segmentation divides the memory into smaller, logical segments (such as Code, Data, Extra, and Stack), allowing efficient organization and utilization of memory. It enables microprocessors to access larger

memory spaces than their native address width, as segment registers or similar mechanisms extend the addressable range.

3. a) DS = 34A9H, BX = 8722H, BP = 45E4H

To access the physical address in the data segment (DS), what should be the value of

I) the segment register if the offset register holds the value of 7B85H.
II) the segment register if the offset register holds the value of 45D2H.
II) the offset register if the segment register holds the value of 7D92H.

Justify whether your answer is valid or not.

Solution:

For Data Segment,

$$\text{Physical Address} = DS \times 10H + BX$$
$$= 34A9H \times 10H + 8722H$$
$$= 3D1B2H$$

I) $\text{Physical Address} - \text{Offset} = 3D1B2H - 7B85H$
$$= 3562DH$$

(Invalid as there are no 0 at last)

II) $\text{Physical Address} - \text{Offset} = 3D1B2H - 45D2H$
$$= 38BE0H$$

(Valid as there are 0 at last)

$$\therefore \text{Segment} = \frac{38BE0H}{10H}$$
$$= 38BEH$$

III) $\text{Physical Address} = \text{Segment} \times 10H + \text{Offset}$

$\therefore \text{Offset} = \text{Physical Address} - \text{Segment} \times 10H$
$$= 3D1B2H - 7D92H \times 10H$$
$$= -4076EH$$

(Invalid since result is negative)

3. b) RAM[A] has a data bus of 8 bits and RAM[B] has a data bus of 16 bits. Both RAMs have a total memory capacity of 128 MB. What is the address bus width of each RAM?

Solution:

Here,

$RAM[A]$ Data Bus $= 8\ bit$
$RAM[B]$ Data Bus $= 16\ bit$
Both RAM memory Capacity $= 128\ MB$
$$= 128 \times 2^{10} \times 2^{10} \times 8\ bits$$
$RAM[A]$ Address Bus $= ?$

$RAM[B]$ Address Bus = ?

For $RAM[A]$,

$$2^{AB} \times 8 = 128 \times 2^{10} \times 2^{10} \times 8$$

$$\text{or, } 2^{AB} = \frac{128 \times 2^{10} \times 2^{10} \times 8}{8}$$

$$\text{or, } AB = \log_2\left(\frac{128 \times 2^{10} \times 2^{10} \times 8}{8}\right)$$

$$\therefore AB = 27\ bit$$

For $RAM[B]$,

$$2^{AB} \times 16 = 128 \times 2^{10} \times 2^{10} \times 8$$

$$\text{or, } 2^{AB} = \frac{128 \times 2^{10} \times 2^{10} \times 8}{16}$$

$$\text{or, } AB = \log_2\left(\frac{128 \times 2^{10} \times 2^{10} \times 8}{16}\right)$$

$$\therefore AB = 26\ bit$$

∴ Address bus width of RAM[A] and RAM[B] is respectively 27 bit and 26 bit.

4. a) **Draw the diagram of a microprocessor with 20-bit address bus and 8-bit data bus interfaced to 28 KB RAM system using the full decoding method. Each RAM chip has a 12-bit address bus and 8-bit data bus. Provide the corresponding address range (starting address and end address) for the system.**

Solution:

For Microprocessor,

Address Bus, $AB = 20\ bit$
Data Bus, $DB = 8\ bit$

For RAM,

Address Bus, $AB = 12\ bit$
Data Bus, $DB = 8\ bit$

Now,

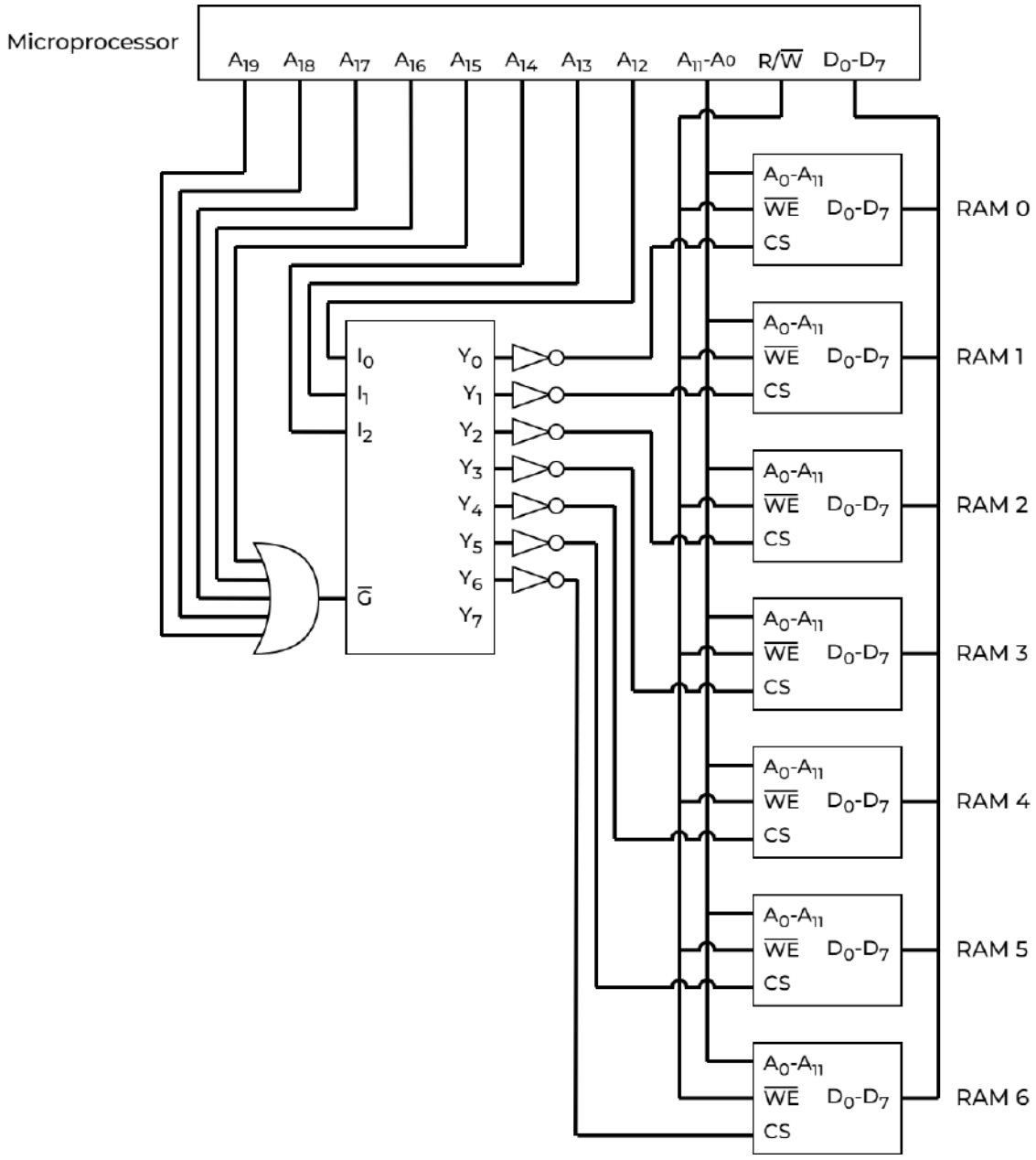
$$\text{RAM Size} = (2^{12} \times 8)\ bit$$
$$= \frac{2^{12} \times 8}{8 \times 2^{10}}\ KB$$
$$= 4\ KB$$

$$\therefore \text{Total RAM Needed} = \left\lceil \frac{28}{4} \right\rceil = 7$$

∴ $3:8$ decoder is needed to implement it in full decoding method.

The diagram has been drawn below:

[P.T.O]



Address Mapping:

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	$A_{11} \dots A_0$	Hex	RAM
0	0	0	0	0	0	0	0	0 … 0	00000 H	0
0	0	0	0	0	0	0	0	1 … 1	00FFF H	
0	0	0	0	0	0	0	1	0 … 0	01000 H	1
0	0	0	0	0	0	0	1	1 … 1	01FFF H	
0	0	0	0	0	0	1	0	0 … 0	02000 H	2
0	0	0	0	0	0	1	0	1 … 1	02FFF H	
0	0	0	0	0	0	1	1	0 … 0	03000 H	3
0	0	0	0	0	0	1	1	1 … 1	03FFF H	
0	0	0	0	0	1	0	0	0 … 0	04000 H	4
0	0	0	0	0	1	0	0	1 … 1	04FFF H	

0	0	0	0	0	1	0	1	0 ... 0	05000 H	5
0	0	0	0	0	1	0	1	1 ... 1	05FFF H	
0	0	0	0	0	1	1	0	0 ... 0	06000 H	6
0	0	0	0	0	1	1	0	1 ... 1	06FFF H	

4. b) Modify the circuit of (a) to address memory range 50000H – 56FFFH. Draw the diagram as before and provide the modified address range. You need only draw the part of the diagram that goes through any modification

Solution:

Here,

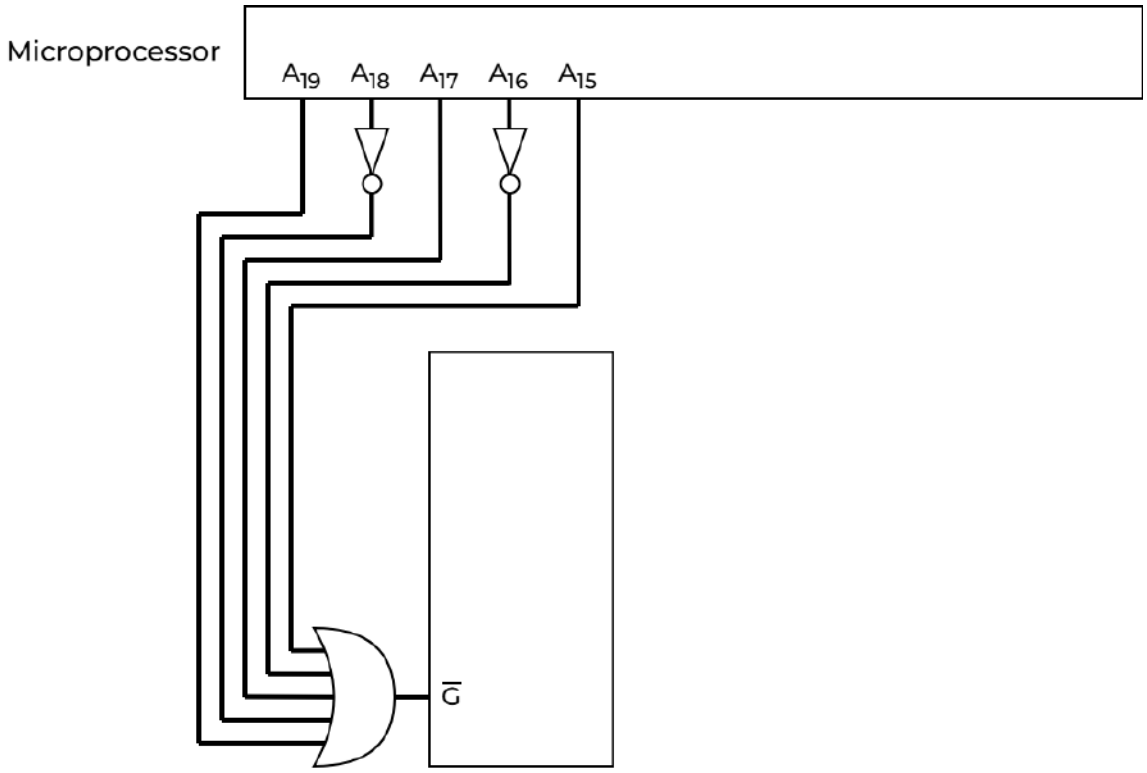
Given address memory range,

$$50000\ H \downarrow 56FFF\ H$$

$$0101\ 0\ 000\ 0000\ 0000\ 0000 \downarrow 0101\ 0\ 110\ 1111\ 1111\ 1111$$

Fixed Part | Decoder Input | Address Bus

The modified diagram has been drawn below:



5. a) If there are a total of 32 Interrupt types in a microprocessor and the address bus has width of 12 bits, what is the ending address of the interrupt vector table if the starting address is 000H.

Solution:

We know,

1 interrupt take = 4 address slot

$\therefore$ 32 interrupt take $= 4 \times 32$ address slot
$= 128$ address slot
$= 80H$ address slot

Here,
Starting Address $= 000H$

$\therefore$ Ending Address $= 000H + 80H - 1H$
$= 07FH$

$\therefore$ Ending address of the interrupt vector table is $07FH$.

5. b) **Mention names of some address registers used in 8086 microprocessor. What do stack pointer and instruction pointer point to?**

Solution:

Some commonly used address registers in the 8086 microprocessor are: Base Pointer (BP), Stack Pointer (SP), Instruction Pointer (IP), Source Index (SI), Destination Index (DI) and etc.

Stack Pointer (SP): Points to the top of the stack in the stack segment (SS). It is automatically updated during push and pop operations to track the topmost stack element.

Instruction Pointer (IP): Points to the offset address of the next instruction to be executed in the code segment (CS). It ensures sequential execution by fetching the next instruction unless altered by jumps, calls, or interrupts.

5. c) **What are the sequence of events that takes place when an interrupt instruction is executed.**

Solution:

The sequence of events that takes place when a software interrupt instruction is executed has been described below:

1. Push flag register onto the stack.
2. Both the interrupt (IF) and trap flag (TF) are set to 0. This disables the INTR pin and the trap or single-step feature.
3. The contents of the current code segment (CS) register are pushed onto the stack.
4. The contents of the current instruction pointer (IP) register are pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both code segment (CS) and instructor pointer (IP) so that, the next instruction executes at the interrupt service procedure address by the interrupt service.