United International University (UIU)
Dept. of Computer Science & Engineering (CSE)
Final-Term Exam Trimester: Spring 2024
Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers
Total Marks: 40 Duration: 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (10 Marks)

Global Descriptor Table	
Index	**Address**
3H	Base: A1270000, Limit: 0FFFFH, Access right: 05H, G = 1
4H	Base: A2370000, Limit: 0FFFFH, Access right: F1H, G = 0
5H	Base: A3470000, Limit: 0FFFFH, Access right: 11H, G = 1
6H	Base: A4570000, Limit: 0FFFFH, Access right: B2H, G = 1
7H	Base: A5670000, Limit: 0FFFFH, Access right: FEH, G = 1
8H	Base: A6770000, Limit: 0FFFFH, Access right: 07H, G = 0

Local Descriptor Table	
Index	**Address**
3H	Base: B1270000, Limit: 0FFFFH, Access right: 02H, G = 1
4H	Base: B2370000, Limit: 0FFFFH, Access right: C1H, G = 0
5H	Base: B3470000, Limit: 0FFFFH, Access right: FEH, G = 1
6H	Base: B4570000, Limit: 0FFFFH, Access right: C2H, G = 1
7H	Base: B5670000, Limit: 0FFFFH, Access right: D1H, G = 1
8H	Base: B6770000, Limit: 0FFFFH, Access right: A0H, G = 0

Part of the descriptor table for an **80386 microprocessor** is given above. For a segment register value of **28H**, determine the followings:

a.	Which entry, table and requested privilege level are selected?	[3]
b.	Starting and ending address of the segment.	[2]
c.	For a physical address of **A351BC12**, determine the offset.	[1]
d.	Segment type (CS/DS/SS/ES).	[1]
e.	Is access to the segment granted? Why or why not ?	[2]
f.	What is the descriptor privilege level?	[1]

Question 2: Answer all the questions. (10 Marks)

a.	The **10-bit Analog-to-Digital Converter (ADC)** of the Arduino on a **5V** system. If the **ADC report as a value is 434** then what will be the **analog voltage**? In a microcontroller where a **12-bit digital-to-analog (DAC)** resolution is configured, the **"analogWrite(x)"** instruction is invoked for digital-to-analog conversion programming, resulting in a calculated **duty cycle** of **75%**. Given a system voltage of **5V,** what is the value of **x**?	[2+2]
b.	When planning a **home security system** comprising a **central monitoring unit** and multiple **sensor nodes** distributed throughout the property, how would you decide whether to use a	[1+2]

	microcontroller or a **microprocessor** for each component? Provide reasoning for your choice of component for both the central monitoring unit and the sensor nodes.	
c.	A microcontroller-based system has a master device: **"Master" (index: 20H)** and three slave devices: "Slave 1" (index: 58H), "Slave 2" (index: 29H), "Slave 3" (index: 7AH). Now, in I2C data transfer protocol, Master receives **2-byte data (from char "UIU")** from **Slave 3**. Draw the corresponding sequence diagram. **The ASCII value of 'U' is 85, and the ASCII value of 'I' is 73.**	[3]

Question 3: Answer all the questions. (10 Marks)

a.	Consider the following fetch cycle in an 8086 BIU: [Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch] When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the **1st** instruction is a **'MOV <address>'**, the **2nd** is a **'JUMP <6th instruction address>'** and **5th** instruction is a **'MOV <address>'** instruction, then **draw** the corresponding **BIU and EU's cycle.**	[4]
b.	**I.** What is the function of the '**READY**' pin in an **8086 microprocessor**? **II.** While doing a **memory read** operation, the **DEN** pin was kept active while sending an address and **ALE** was active while sending data. Do you think the operation would have been completed successfully? If not describe **the problem** and also **the solution**.	[2+2]
c.	What is **paging**? Describe in short.	[2]

Question 4: Answer all the questions. (10 Marks)

RAM Content

Address	Content		Address	Content
0H	1010 1010		8H	XXXX XXXX
1H	1100 1100		9H	XXXX XXXX
2H	1110 1110		AH	0010 0000
3H	1100 1111		BH	0110 0100
4H	1111 XXXX		CH	0000 1010
5H	1001 XXXX		DH	0001 1001
6H	XXXX XXXX		EH	0000 0101
7H	XXXX XXXX		FH	0001 1011

Opcode Table

Mnemonic	Opcode
HLT	1001
OUT	1111
SUB	1100
ADD	1110
LDA	1010

a.	Write **the assembly code** for the instructions stored in **RAM address (0H - 5H).**	[4]
b.	What are the values of the **Accumulator register** after executing each instruction programmed in the **RAM**. [**Initially Accumulator = 0H**]	[3]
c.	If a **256x16 RAM chip** is used in **SAP-I architecture**, then what would be the size of the **Program counter, Input and MAR register, Instruction register, Accumulator register, B register and Output register**. Describe with proper logic.	[3]