UIU QUESTION BANK

FINAL QUESTION SOLUTIONS

MICROPROCESSORS AND MICROCONTROLLERS

CSE 4325

SOLUTION BY

NURUL ALAM ADOR

*UPDATED TILL **FALL 2024***

nurulalamador.github.io/**UIUQuestionBank**

Index

1.

Global Descriptor Table	
Index	**Address**
045 H	Base: BE308810, Limit: 78BD7H, Access right: 54H, G = 1
1A3 H	Base: BFE4DBB8, Limit: 3345AH, Access right: 1FH, G = 0
2F6 H	Base: B66125A3, Limit: CC32FH, Access right: 8AH, G = 1
4D1 H	Base: B2B2ACFF, Limit: F56A9H, Access right: 27H, G = 1
6B4 H	Base: B61310BD, Limit: 50AEAH, Access right: 53H, G = 0
A29 H	Base: B4DF02F6, Limit: C5072H, Access right: 49H, G = 0

Local Descriptor Table	
Index	**Address**
045 H	Base: A584718E, Limit: 0FAE1H, Access right: F9H, G = 1
1A3 H	Base: A872A2F3, Limit: 29FDBH, Access right: 0DH, G = 0
2F6 H	Base: AFF3B41C, Limit: 53027H, Access right: B8H, G = 1
4D1 H	Base: ABA461BC, Limit: C31ABHH, Access right: 62H, G = 0
6B4 H	Base: A56DC418, Limit: E6357H, Access right: 54H, G = 1
A29 H	Base: A61C994D, Limit: 694CCH, Access right: 1AH, G = 1

Part of the descriptor table for an **80386 microprocessor** is given above. For a segment register value of **35A1 H**, determine the followings:

1. a) Which entry, table and requested privilege level are selected?

Solution:

$$\text{Segment Register} = 35A1H \rightarrow \underbrace{0011\ 0101\ 1010\ 0}_{\text{Descriptor Index}}\ \underbrace{0}_{\text{TI}}\ \underbrace{01}_{\text{RPL}}$$

Entry = $0110\ 1011\ 0100 \rightarrow 6B4H$
Table = $0 \rightarrow$ Global Descriptor Table
Requested Privilege Level = 01

1. b) Starting and ending address of the segment.

Solution:

We know,

$$\text{Starting Address} = \text{Base Address} = B61310BDH$$

$$\text{Ending Address} = \text{Base Address} + \text{Limit} = B61310BDH + 50AEAH$$

$= \text{B6181BA7}H$

1. c) For an **offset** value of **158C0 H**, determine the physical address.

Solution:

We know,

$$\begin{aligned}\text{Physical Address} &= \text{Base Address} + \text{Offset}\\ &= \text{B61310BD}H + 158\text{C0}H\\ &= \text{B614697D}H\end{aligned}$$

∴ Physical Address is $\text{B614697D}H$.

1. d) Has the segment been accessed?

Solution:

Access Right = $53H$ →

0	1	0	1	0	0	1	1
P	DPL		S	E	ED/C	R/W	A

Since $A = 1$, therefore the segment has been accessed.

1. e) Segment type **(CS/DS/SS/ES)**.

Solution:

Since $E = 0$ and $ED = 0$, therefore this is data segment (DS).

1. f) Is the descriptor defined or undefined?

Solution:

Since $P = 0$, therefore the descriptor is undefined.

2. a) The NXP Kinetis Series offers a 24 bit ADC on a 5.0 V reference system and a 12 bit DAC with I2C interface.

- **i.** Calculate the analog voltage if the ADC reading is **8300608**.
- **ii.** During the digital to analog programming, you need to call **analogWrite(1760).** Calculate the duty cycle and draw the corresponding duty cycle diagram.

Solution:

i. We know,

$$\frac{\text{Resolution of the } ADC}{\text{System Voltage}} = \frac{ADC \text{ Reading}}{\text{Analog Voltage}}$$

$$\text{or, } \frac{2^{24}-1}{5} = \frac{8300608}{\text{Analog Voltage}}$$

$$\text{or, } \frac{5}{2^{24}-1} \times 8300608 = \text{Analog Voltage}$$

$\therefore$ Analog Voltage $= 2.47$

$\therefore$ Analog Voltage is 2.47 V.

ii. We know,

$$\text{Resolution of the } DAC = 2^n - 1$$
$$= 2^{12} - 1$$
$$= 4095$$

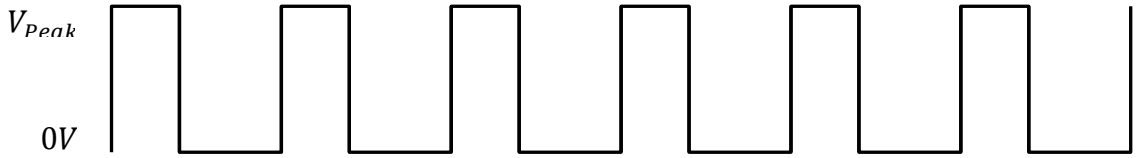
$4095 \rightarrow 100\%$ call duty

$\therefore 1 \rightarrow \frac{100}{4095}\%$ call duty

$\therefore 1760 \rightarrow \frac{100 \times 1760}{4095}\%$ call duty

$= 43\%$ call duty

$\therefore$ Duty cycle is 43%. Duty cycle diagram has been drawn below:



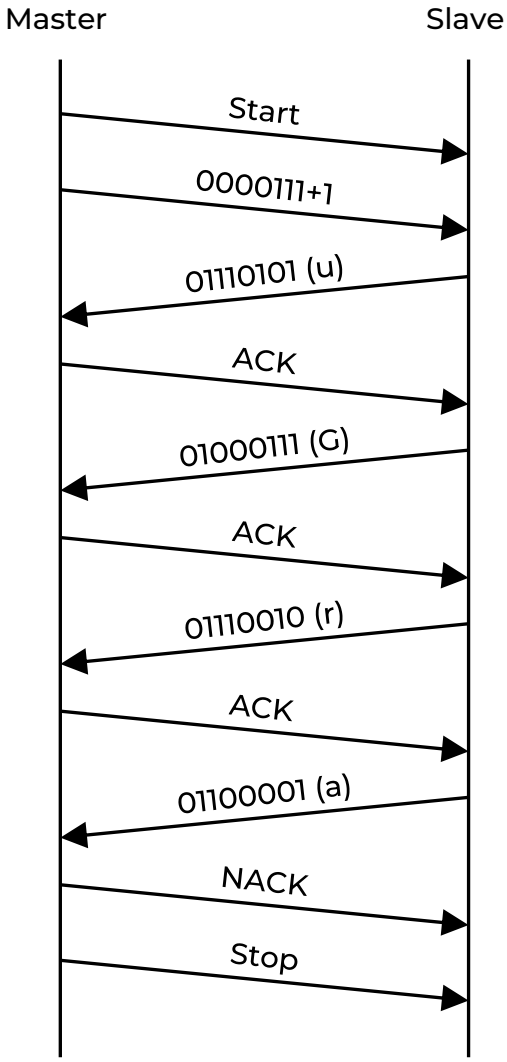
2. b) What is the primary difference between **SPI** and **I2C** protocols? Suppose in a particular I2C communication, **Master (index - CH)** receives **4 byte data (char - 'uGrad)** from **Slave (index - 7H)**. Draw the corresponding sequence diagram. **ASCII** codes for **'A'** and **'a'** are **65 and 97 respectively**.

Solution:

SPI (Serial Peripheral Interface) is a three-wire based full-duplex communication system and, on the other hand, I2C (Inter-Integrated Circuit) is half-duplex and it is two-wire based. This is one of the primary difference between SPI and I2C protocols.

Corresponding sequence diagram has been drawn below:

[P.T.O]



Here,

u → 117
G → 71
r → 114
a → 97

2. c) Suppose you want to design a **real-time traffic monitoring system** for an intersection. The system requires processing multiple sensor inputs (traffic cameras, speed detection sensors) and adjusting traffic signal timings dynamically to optimize traffic flow. The system can be built using either a **Raspberry Pi (microprocessor-based system) or Arduino (microcontroller-based system)**. **Which platform would be more suitable** and **why**?

Solution:

Since there are highly software based operations and multitasking (like camera, speed detection, traffic signal adjustment, etc.) is required for this traffic monitoring system, therefore Raspberry Pi (microprocessor-based system would be more suitable for this project.

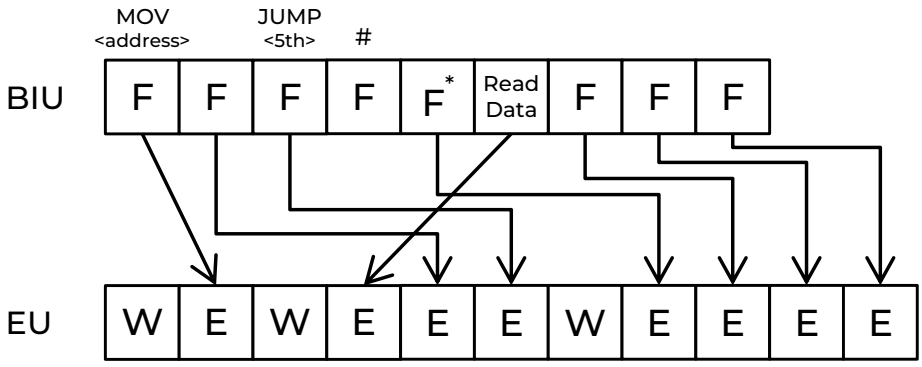
3. a) Consider the following fetch cycle in an 8086 BIU:

[Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch]

When the one instruction is being executed, **four instructions** are fetched and saved in the instruction queue. If the 1st instruction is a **'MOV <address>'**, the **3rd** is a **'JUMP <5th instruction address>'** and **4th** instruction is a **'JUMP <7th instruction address>'** instruction, then **draw** the corresponding **BIU and EU's cycle.**

Solution:

BIU and EU's cycle has been drawn below:

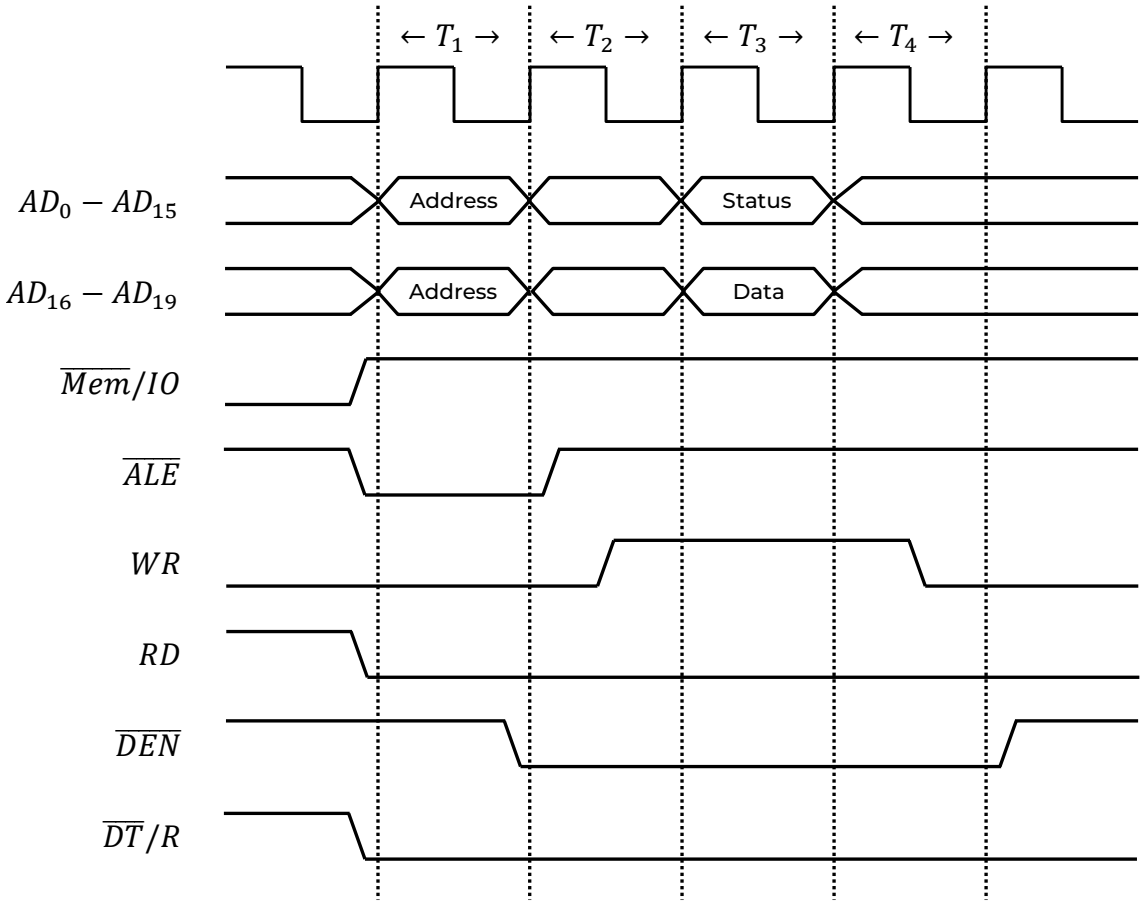


= Discard

3. b) Draw the timing diagram for **IO Write** operation of microprocessor "808x" showing the activities of $\overline{Mem}/IO$, Address-Data bus ($AD_0 - AD_{15}$, $AD_{16} - AD_{19}$), $\overline{ALE}$, WR, RD, $\overline{DEN}$, $\overline{DT}/R$ in each clock cycle. **[Observe the pins carefully]**

Solution:

The timing diagram has been drawn below:



3. c) What is the advantage of **paging technique**?

Solution:

The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time.

Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Whenever the other pages of task are required for execution, they may be fetched from the secondary storage. Thus paging mechanism provides an effective technique to manage the physical memory for multitasking systems.

4. RAM Content

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	0000 0010
3H			BH	0110 0100
4H			CH	0000 0101
5H			DH	0000 0001
6H			EH	1000 0101
7H			FH	0100 0010

Opcode Table

Mnemonic	Opcode
HLT	1101
OUT	1001
SUB	1100
ADD	1110
LDA	1010

Initially, the value of the **Accumulator Register is 1H, the B Register is 3H, and the Output Register is 4H.**

4. a) Write the **assembly code** for the below expression using the **RAM content**.

$$3 + 5 - 2 - 1$$

Solution:

Given,

$3 + 5 - 2 - 1$

Assembly Code:

```
ADD  AH
ADD  CH
SUB  AH
SUB  DH
OUT
HLT
```

Here,

$AH \rightarrow 2$
$CH \rightarrow 5$
$DH \rightarrow 1$

4. b) Find out the values of the **Accumulator register, B register and Output Register** after executing **each** instruction **written in (a)**.

Solution:

Accumulator register value after each execution has been shown below:

Instruction	AX	BX	OUT
Initially	$1H$	$3H$	$4H$
ADD AH	$3H$	$2H$	$4H$
ADD CH	$8H$	$5H$	$4H$
SUB AH	$6H$	$2H$	$4H$
SUB DH	$5H$	$1H$	$4H$
OUT	$5H$	$1H$	$5H$
HLT	$0H$	$0H$	$0H$

4. c) Write the control words for Execution T-states (**T4, T5, T6**) to perform the **ADD instruction** using the controller sequence below.

CON $= S_U\ \overline{E_U}\ C_p\ E_p \quad L_M\ C_E\ \overline{L_I}\ \overline{E_I} \quad L_A\ \overline{E_A}\ \overline{L_B}\ \overline{L_O}$

Solution:

Control words for the instruction ADD has been written below:

T4: CON $= 0100\ \ 1010\ \ 0111$
$= 4\text{A}7H$

Instruction Register → Bus
Bus → MAR

T5: CON $= 0100\ \ 0111\ \ 0101$
$= 475H$

MAR → Bus
Bus → B Register

T6: CON $= 0000\ \ 0011\ \ 1111$
$= 03\text{F}H$

Operation of Addition
Adder/Subtractor → Bus
Bus → Accumulator Register

Summer 2024

1.

Local Descriptor Table	
Index	**Address**
500H	Base: B56700, Limit: 0129H, Access right: 92H
501H	Base: B23900, Limit: 0129H, Access right: FFH
502H	Base: B11C00, Limit: 0C12H, Access right: D1H
503H	Base: B67800, Limit: 0560H, Access right: A0H

An **80286 microprocessor** is executing a segment in protected mode and a portion of its descriptor table is given above. If the current physical address produced by this processor is **B123ABH**, then determine the followings:

1. a) Find out the **descriptor (index number)** of which this physical address belongs to.

Solution:

For index 500H,

$$\begin{aligned}\text{Base} &= \text{B}56700\text{H}\\ \text{End} &= \text{Base} + \text{Limit}\\ &= \text{B}56700H + 0129H\\ &= \text{B}56829H\end{aligned}$$

$\therefore \text{B}123ABH$ does not belong in this range.

For index 501H,

$$\begin{aligned}\text{Base} &= \text{B}23900H\\ \text{End} &= \text{Base} + \text{Limit}\\ &= \text{B}23900H + 0\text{F}10H\\ &= \text{B}24810H\end{aligned}$$

$\therefore \text{B}123ABH$ does not belong in this range.

For index 502H,

$$\begin{aligned}\text{Base} &= \text{B}11\text{C}00H\\ \text{End} &= \text{Base} + \text{Limit}\\ &= \text{B}11\text{C}00H + 0\text{C}12H\\ &= \text{B}12812H\end{aligned}$$

$\therefore \text{B}123ABH$ belongs in this range.

$\therefore$ Descriptor (index number) is $502H$.

1. b) For an offset value of **2D4H**, determine the **physical address**.

Solution:

We know,

$$\begin{aligned}\text{Physical Address} &= \text{Base Address} + \text{Offset}\\ &= \text{B11C00}H + \text{2D4}H\\ &= \text{B11ED4}H\end{aligned}$$

$\therefore$ Physical Address is $\text{B11ED4}H$.

1. c) Segment type **(CS/DS/SS/ES)**.

Solution:

Access Right = $28H$ →

1	1	0	1	0	0	0	1
P	DPL		S	E	ED/C	R/W	A

Since E = 0 and ED = 0, therefore this is data segment (DS).

1. d) Has the segment been accessed?

Solution:

Since A = 1, therefore the segment has been accessed.

1. e) What is the descriptor privilege level?

Solution:

Since DPL = 10, therefore descriptor privilege level is 10.

1. f) Is the descriptor defined or undefined?

Solution:

Since P = 1, therefore the descriptor is defined.

2. a) Suppose, you are using a device which uses an **"N" bit ADC** on a **5v system**. This system converts an analog voltage of **3V** into a digital value of **2457**. **Find out the value of "N"**. If we want to reduce **quantization error**, should we increase or decrease the value of **"N"**? **Give an explanation for your answer**.

Solution:

We know,

$$\frac{\text{Resolution of the } ADC}{\text{System Voltage}} = \frac{ADC \text{ Reading}}{\text{Analog Voltage}}$$

or, $\frac{2^N - 1}{5} = \frac{2457}{3}$

$$\text{or, } 2^N = \frac{2457 \times 5}{3} + 1$$

$$\text{or, } N = \log_2\left(\frac{2457 \times 5}{3} + 1\right)$$

$$\therefore N = 12$$

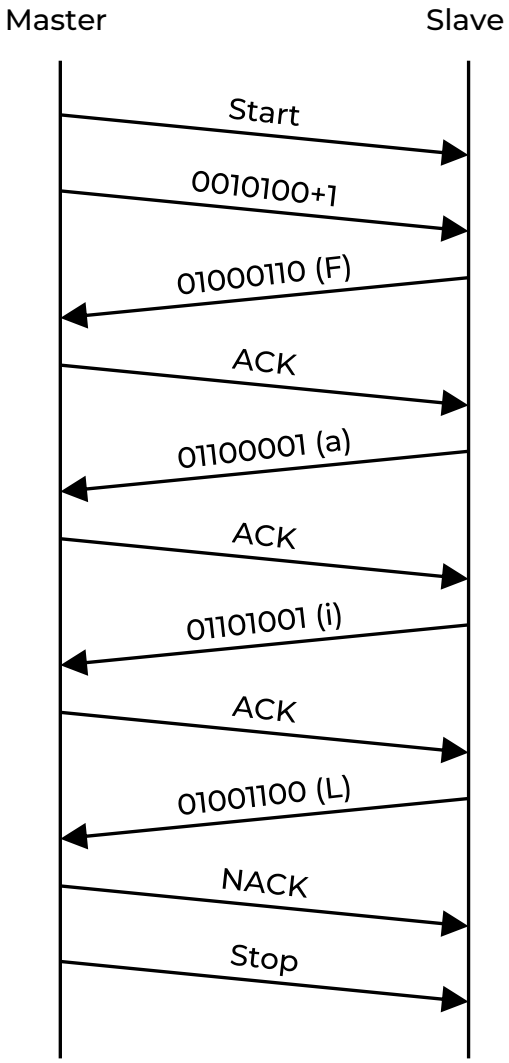
To reduce quantization error, we should increase value of N (number of bits). More bits in an ADC increase the number of possible digital values, reducing the error.

2. b) Why is **I2C** called a **handshaking protocol**? In a particular communication in I2C, **Master (index - 10H)** receives **4 byte data (char - 'FaiL')** from **Slave (index - 14H)**. Draw the corresponding sequence diagram. **ASCII** codes for **'A'** and **'a'** are **65 and 97 respectively**.

Solution:

I2C is called a handshaking protocol because it uses ACK (acknowledge) and NACK (negative acknowledge) bits to ensure reliable communication.

Corresponding sequence diagram has been drawn below:



Here,

F → 70
a → 97
i → 105
L → 76

2. c) Design a **Smart Irrigation System** that automates water pumps based on soil moisture levels while sending data to a server for real-time monitoring.

For example, when soil moisture drops below 50%, the pump automatically activates, and it turns off once the moisture reaches 55%. The system can be built using either a **Raspberry Pi (microprocessor-based system) or Arduino (microcontroller -based system)**. **Which platform would be more suitable?**

Solution:

Since this project is based on one specific work and it is mainly hardware related work, therefore Arduino (microcontroller-based system) would be suitable for this Smart Irrigation System project.

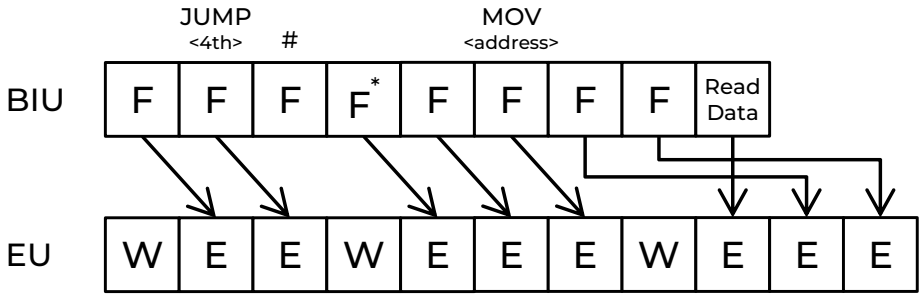
3. a) Consider the following fetch cycle in an 8086 BIU:

[Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch]

When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the **2nd** instruction is a **'JUMP <4th>'**, the **3rd** is a **'JUMP <6th instruction address>'** and **6th** instruction is a **'MOV <address>'** instruction, then **draw** the corresponding **BIU and EU's cycle**.

Solution:

BIU and EU's cycle has been drawn below:



= Discard

3. b) **I.** What is **'Wait State'** in an **8086 microprocessor**? Which **pin** is used to **insert 'Wait States'** into the timing of an **8086 microprocessor**?

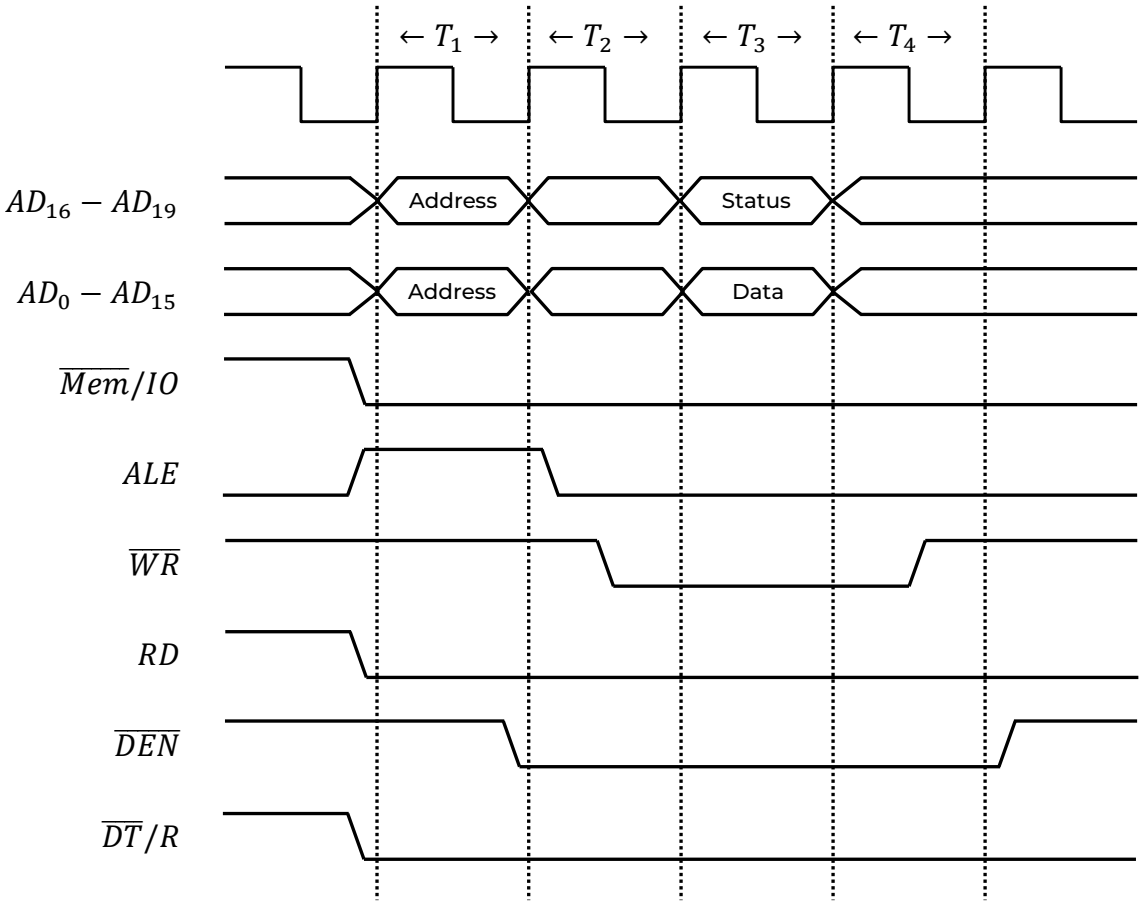
II. Draw the timing diagram for **Memory Write** operation of microprocessor "808x" showing the activities of $\overline{Mem}/IO$, Address-Data bus ($AD_0 - AD_{15}$, $AD_{16} - AD_{19}$), ALE, $\overline{WR}$, RD, $\overline{DEN}$, $\overline{DT}/R$ in each clock cycle. **[Observe the pins carefully]**

Solution:

I. A wait state is a situation in which a computer processor is waiting for the completion of some event before resuming activity. READY pin is used to insert 'Wait States' into the timing of an 8086 microprocessor.

II. The timing diagram has been drawn below:

[P.T.O]



3. c) When does **page fault** occur in the paging mechanism?

Solution:

Paging is one of the memory management techniques used for virtual memory multitasking operating system. If the page required by the processor is not in the main memory, then page fault occurs. There are two possible reasons for a page fault: either the page does not exist or the page was not prepared for load.

4. RAM Content

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	
3H			BH	0000 1000
4H			CH	0000 0010
5H			DH	0000 0001
6H			EH	0000 0110
7H			FH	0000 0011

Opcode Table

Mnemonic	Opcode
LDA	1001
ADD	0010
SUB	0001
OUT	0100
HLT	0011

4. a) Write the **assembly code** for the below expression using the **RAM content**.

$$3^2 - 2^2 + 1^2$$

[Hints: Exponents can be done by Multiplications, and Multiplications can be done by Additions]

Solution:

Given,

$$\begin{aligned} 3^2 - 2^2 + 1^2 &= 3 \times 3 - (2 \times 2) + 1 \times 1 \\ &= 3 + 3 + 3 - (2 + 2) + 1 \\ &= 3 + 3 + 3 - 2 - 2 + 1 \end{aligned}$$

Assembly Code:

```
LDA  FH
ADD  FH
ADD  FH
SUB  CH
SUB  CH
ADD  DH
OUT
HLT
```

Here,

$FH \rightarrow 3$
$CH \rightarrow 2$
$DH \rightarrow 1$

4. b) Fill-up the **RAM content table** with the instructions **machine code. (Start from 0H)** Use the opcode given in the **opcode table**.

Solution:

RAM content table has been filled up below:

Address	Content
$0H$	1001 1111
$1H$	0010 1111
$2H$	0010 1111
$3H$	0001 1100
$4H$	0001 1100
$5H$	0010 1101
$6H$	0100 XXXX
$7H$	0011 XXXX

4. c) Write the control words for Execution T-states (T4, T5, T6) to perform the instruction at **Address 3H** of the given RAM using the controller sequence below.

CON $= C_p\ E_p\ \overline{L_M}\ \overline{C_E}\quad \overline{L_I}\ \overline{E_I}\ \overline{L_A}\ E_A\quad S_U\ E_U\ \overline{L_B}\ \overline{L_O}$

Solution:

Instruction at $3H$: SUB CH

Control words for the instruction SUB has been written below:

T4: CON $= 0001\ 1010\ 0011$
$= 1A3H$

Instruction Register → Bus
Bus → MAR

T5: CON $= 0010\ 1110\ 0001$
$= 2E1H$

MAR → Bus
Bus → B Register

T6: CON $= 0011\ 1100\ 1111$
$= 3CFH$

Operation of Subtraction
Adder/Subtractor → Bus
Bus → Accumulator Register

1.

Global Descriptor Table	
Index	**Address**
3H	Base: A1270000, Limit: 0FFFFH, Access right: 05H, G = 1
4H	Base: A2370000, Limit: 0FFFFH, Access right: F1H, G = 0
5H	Base: A3470000, Limit: 0FFFFH, Access right: 11H, G = 1
6H	Base: A4570000, Limit: 0FFFFH, Access right: B2H, G = 1
7H	Base: A5670000, Limit: 0FFFFH, Access right: FEH, G = 1
8H	Base: A6770000, Limit: 0FFFFH, Access right: 07H, G = 0

Local Descriptor Table	
Index	**Address**
3H	Base: A1270000, Limit: 0FFFFH, Access right: 02H, G = 1
4H	Base: A2370000, Limit: 0FFFFH, Access right: C1H, G = 0
5H	Base: A3470000, Limit: 0FFFFH, Access right: FEH, G = 1
6H	Base: A4570000, Limit: 0FFFFH, Access right: C2H, G = 1
7H	Base: A5670000, Limit: 0FFFFH, Access right: D1H, G = 1
8H	Base: A6770000, Limit: 0FFFFH, Access right: A0H, G = 0

Part of the descriptor table for an **80386 microprocessor** is given above. For a segment register value of **28H**, determine the followings:

1. a) Which entry, table and requested privilege level are selected?

Solution:

$$\text{Segment Register} = 28H = 0028H \rightarrow \underbrace{0000\ 0000\ 0010\ 1}_{\text{Descriptor Index}}\underbrace{0}_{\text{TI}}\underbrace{00}_{\text{RPL}}$$

Entry = $0101 \rightarrow 5H$
Table = $0 \rightarrow$ Global Descriptor Table
Requested Privilege Level = $00 \rightarrow$ Highest Privilege Level

1. b) Starting and ending address of the segment.

Solution:

We know,

$$\text{Starting Address} = \text{Base Address} = \text{A3470000}H$$

$$\text{Ending Address} = \text{Base Address} + \text{Limit} = \text{A3470000}H + \text{0FFFFFFF}H$$

$= \text{B34FFFFF}H$

1. c) For a physical address of **A351BC12**, determine the offset.

Solution:

We know,

Physical Address = Base Address + Offset

∴ Offset = Physical Address − Base Address

$= \text{A351BC12}H + \text{A3470000}H$

$= \text{ABC12}H$

1. d) Segment type **(CS/DS/SS/ES)**.

Solution:

Access Right = $11H$ →

0	0	0	1	0	0	0	1
P	DPL		S	E	ED/C	R/W	A

Since $E = 0$ and $ED = 0$, therefore this is data segment (DS).

1. e) Is access to the segment granted? Why or why not?

Solution:

Since $A = 1$, therefore the access to the segment is granted.

1. f) What is the descriptor privilege level?

Solution:

Here, Descriptor Privilege Level, $DPL = 00$

2. a) The **10-bit Analog-to-Digital Converter (ADC)** of the Arduino on a **5V** system. If the **ADC report as a value is 434** then what will be the **analog voltage**?
In a microcontroller where a **12-bit digital-to-analog (DAC)** resolution is configured, the **"analogWrite(x)"** instruction is invoked for digital-to-analog conversion programming, resulting in a calculated **duty cycle of 75%**. Given a system voltage of **5V**, what is the value of **x**?

Solution:

We know,

$$\frac{\text{Resolution of the } ADC}{\text{System Voltage}} = \frac{ADC \text{ Reading}}{\text{Analog Voltage}}$$

or, $\frac{2^{10} - 1}{5} = \frac{434}{\text{Analog Voltage}}$

or, $\frac{5}{2^{10} - 1} \times 434 = \text{Analog Voltage}$

$\therefore$ Analog Voltage $= 2.12$

$\therefore$ Analog Voltage is 2.12 V.

We know,

$$\text{Resolution of the } DAC = 2^n - 1$$
$$= 2^{12} - 1$$
$$= 4095$$

$$100\% \text{ call duty for } 4095$$
$$\therefore 1\% \text{ call duty for } \frac{4095}{100}$$
$$\therefore 75\% \text{ call duty for } \frac{4095}{100} \times 75$$
$$= 3071$$

$\therefore$ Value of x is 3071.

2. b) When planning a **home security system** comprising a **central monitoring unit** and multiple **sensor nodes** distributed throughout the property, how would you decide whether to use a **microcontroller** or **microprocessor** for each component? Provide reasoning for your choice of component for both the central monitoring unit and the sensor nodes.

Solution:

For central monitoring unit, microprocessor will be suitable because this will be a software related work and there will be multitasking of various kind of task.

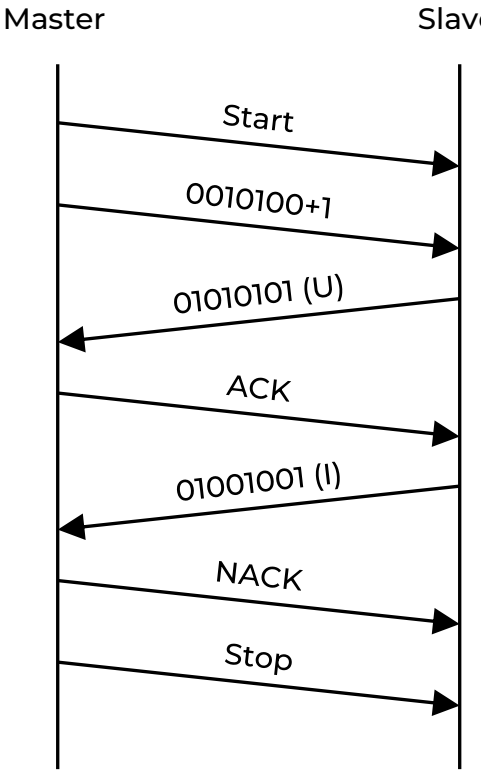
On the other hand, microcontroller will be best choice for the sensor nodes because it is hardware centric work and each sensor nodes are specific for one work only.

2. c) A microcontroller-based system has a master device: **"Master" (index: 20H)** and three slave devices: "Slave 1" (index: 58H), "Slave 2" (index: 29H), "Slave 3" (index: 7AH). Now, in I2C data transfer protocol, Master receives **2-byte data (from char "UIU")** from **Slave 3**. Draw the corresponding sequence diagram. **The ASCII value of 'U' is 85, and the ASCII value of 'I' is 73**.

Solution:

The corresponding sequence diagram has been drawn below:

[P.T.O]



Here,

U → 85
I → 73

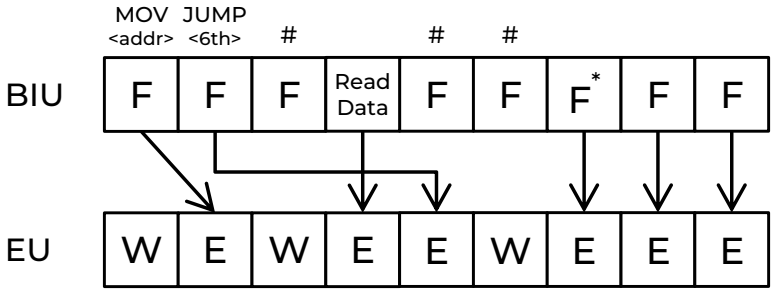
3. a) Consider the following fetch cycle in an 8086 BIU:

[Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch]

When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the **1st** instruction is a **'MOV <address>'**, the **2nd** is a **'JUMP <6th instruction address>'** and **5th** instruction is a **'MOV <address>'** instruction, then **draw** the corresponding **BIU and EU's cycle**.

Solution:

BIU and EU's cycle has been drawn below:



= Discard

3. b) I. What is the function of the **'READY'** pin in an **8086 microprocessor**?

II. While doing a **memory read** operation, the **DEN** pin was kept active while sending an address and **ALE** was active while sending data. Do you think the operation would have been completed successfully? If not describe **the problem** and also the solution.

Solution:

I. The READY input is controlled to insert wait states into the timing of the microprocessor. If the READY pin is placed at a logic 0 level, the micro-processor enters into wait states and remains idle. If the READY pin is placed at a logic 1 level, it has no effect on the operation of the microprocessor.

II. The operation should be incomplete and unsuccessful. Because, ALE should be kept active while sending address instead of DEN. On the other hand, DEN should be active while sending data instead of ALE. Since in the mentioned scenario, DEN was kept active while sending address and ALE was kept active while sending data, the operation should be unsuccessful.

3. c) What is **paging**? Describe in short.

Solution:

Paging is one of the memory management techniques used for virtual memory multitasking operating system.

Paging divides the linear address space into fixed-sized blocks called pages. Paging divides the memory into a fixed size pages. The pages are just fixed size portions of the program module or data.

4. RAM Content

Address	Content		Address	Content
0H	1010 1010		8H	XXXX XXXX
1H	1100 1100		9H	XXXX XXXX
2H	1110 1110		AH	0010 0000
3H	1100 1111		BH	0110 0100
4H	1111 XXXX		CH	0000 1010
5H	1001 XXXX		DH	0001 1001
6H	XXXX XXXX		EH	0000 0101
7H	XXXX XXXX		FH	0001 1011

Opcode Table

Mnemonic	Opcode
HLT	1001
OUT	1111
SUB	1100
ADD	1110
LDA	1010

4. a) Write the **assembly code** for the instructions stored in **RAM address (0H-5H)**.

Solution:

Assembly Code:

```
LDA  AH
SUB  CH
ADD  EH
SUB  FH
OUT
HLT
```

4. b) What are the values of the **Accumulator register** after executing each instruction programmed in the **RAM. [Initially Accumulator = 0H]**

Solution:

Accumulator register value after each execution has been shown below:

Instruction	AX
LDA AH	$20H$
SUB CH	$16H$
ADD EH	$1BH$
SUB FH	$0H$
OUT	$0H$
HLT	$0H$

4. c) If a **256x16 RAM chip** is used in **SAP-I architecture**, then what would be the size of the **Program counter, Input and MAR register, Instruction register, Accumulator register, B register and Output register.** Describe with proper logic.

Solution:

For 256×16 RAM,

Address Bus $= n = 8\ bit$

Data Bus $= 16\ bit$

$$2^n = 256$$
$$\text{or, } n = \log_2 256$$
$$\therefore n = 8$$

Register	Size
Program Counter	8 bit
Input and MAR Register	8 bit
Instructor Register	16 bit
Accumulator Register	16 bit
B Register	16 bit
Output Register	16 bit

1.

Local Descriptor Table	
Index	**Address**
002 H	Base: C238000A, Limit: F175FH, Access right: 02H, G = 0
014 H	Base: C38400A0, Limit: E9806H, Access right: C1H, G = 1
126 H	Base: C9560A00, Limit: 85642H, Access right: FEH, G = 0
158 H	Base: C002A00E, Limit: 2A043H, Access right: B4H, G = 1
275 H	Base: C85200EF1, Limit: AB00FH, Access right: D1H, G = 1
344 H	Base: C60401A1, Limit: 0FFFFH, Access right: A0H, G = 0

Global Descriptor Table	
Index	**Address**
002 H	Base: D7210111, Limit: F175FH, Access right: 05H, G = 1
014 H	Base: D3270011, Limit: 01234H, Access right: F1H, G = 0
126 H	Base: D3741000, Limit: 98765H, Access right: 11H, G = 1
158 H	Base: D6590B00, Limit: 1524CH, Access right: B2H, G = 0
275 H	Base: D6870010, Limit: 0AF0EH, Access right: FEH, G = 1
344 H	Base: D655000B, Limit: D015CH, Access right: 07fH, G = 1

Part of the descriptor table for an **80386 microprocessor** is given above. For a segment register value of **930H**, determine the followings:

1. a) Which entry, table and requested privilege level are selected?

Solution:

$$\text{Segment Register} = 930H = 0930H \rightarrow \underbrace{0000\ 1001\ 0011\ 0}_{\text{Descriptor Index}}\ \underbrace{0}_{\text{TI}}\ \underbrace{00}_{\text{RPL}}$$

Entry = $0001\ 0010\ 0110 \rightarrow 126H$
Table = $0 \rightarrow$ Global Descriptor Table
Requested Privilege Level = $00 \rightarrow$ Highest Privilege Level

1. b) Starting and ending address of the segment.

Solution:

We know,

$$\text{Starting Address} = \text{Base Address} = \text{D3741000}H$$

$$\text{Ending Address} = \text{Base Address} + \text{Limit} = \text{D3741000}H + 1524\text{CFFF}H \quad (\text{Since } G = 1)$$

$$= \text{E898DFFF}H$$

1. c) For an offset value of **12ACDH**, determine the physical address.

Solution:

We know,

$$\text{Physical Address} = \text{Base Address} + \text{Offset}$$
$$= \text{D3741000}H + \text{12ACD}H$$
$$= \text{D3753ACD}H$$

1. d) Segment type **(CS/DS/SS/ES)**.

Solution:

Access Right = $11H$ →

0	0	0	1	0	0	0	1
P	DPL		S	E	ED/C	R/W	A

Since E = 0 and ED = 0, therefore this is data segment (DS).

1. e) Is access to the segment granted? Why or why not?

Solution:

Since A = 1, therefore the access to the segment is granted.

1. f) Is the descriptor defined or undefined?

Solution:

Since P = 0, therefore the descriptor is undefined.

2. a) In **'X' microcontroller**, **11 bits** digital to analog (**DAC**) resolution is set. During the digital to analog conversion programming, you have called **"analogWrite (1535)"** instruction. Calculate the **duty cycle**. **Draw the duty cycle diagram**. Consider the **system voltage is 7V**.

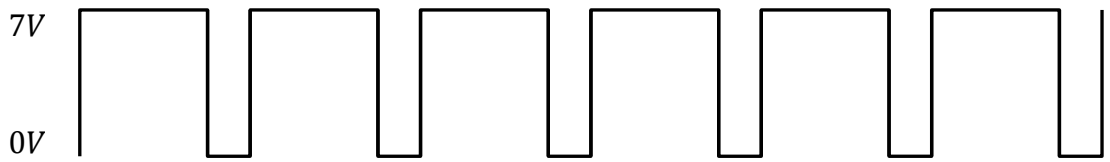
Solution:

We know,

$$\text{Resolution of the } DAC = 2^n - 1$$
$$= 2^{11} - 1$$
$$= 2047$$

$$2047 \rightarrow 100\% \text{ call duty}$$
$$\therefore 1 \rightarrow \frac{100}{2047}\% \text{ call duty}$$
$$\therefore 1535 \rightarrow \frac{100 \times 1535}{2047}\% \text{ call duty}$$
$$= 75\% \text{ call duty}$$

∴ Duty cycle is 75%. Duty cycle diagram has been drawn below:



2. b) UIU is planning to implement an **Advanced Access Control system** for enhanced campus security. Employees and students will utilize **RFID cards** for entry and exit. Another plan is to create **an automated module to calculate attendance, performance and efficiency of the students**. Now, "X" suggested using **Raspberry pi for the Advanced Access Control System** and **Arduino for the other module**. Do you think the suggestion was right? Write **Yes** or **No** and then **give reasons for your answer.**

Solution:

The suggestion is not right. Since Advanced Access Control System have a single one work to do (opening door with RFID card) and it is related to hardware more, Arduino should be used where.

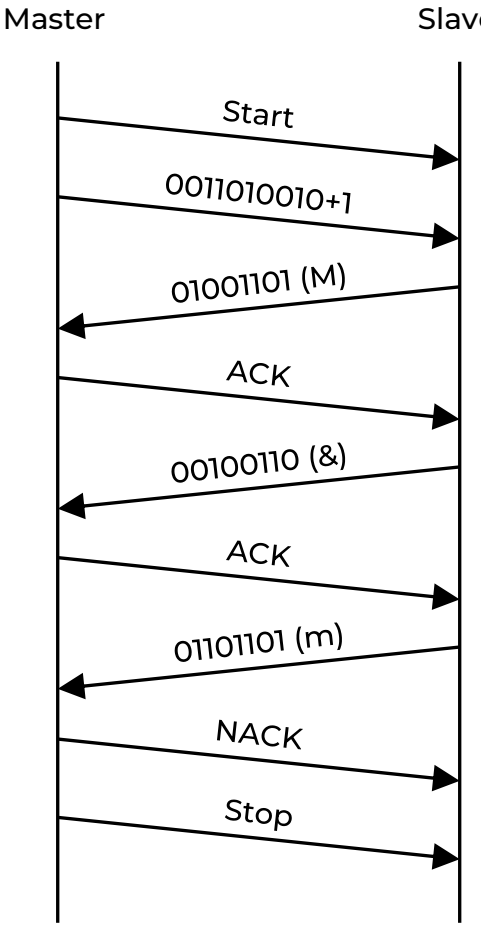
On the other hand, automated module will calculate attendance, performance and efficiency of the students, which is related to software more and there will be multi-tasking. Therefore, Raspberry Pi should be used here.

2. c) A microcontroller-based system has a master device, **"Master" (index: 2H)** receives **3 byte data (char 'M&m')** from **slave 3 (index: D2H)** using **I^2C**. **Draw** the corresponding **sequence diagram**. (Assume that I^2C uses **10 bit addressing** for slave address, **ASCII value of '&' is 38, 'D' is 68, '2' is 50, 'M' is 77 and 'm' is 109**)

Solution:

The corresponding sequence diagram has been drawn below:

[P.T.O]



Here,

M → 77

& → 38

m → 109

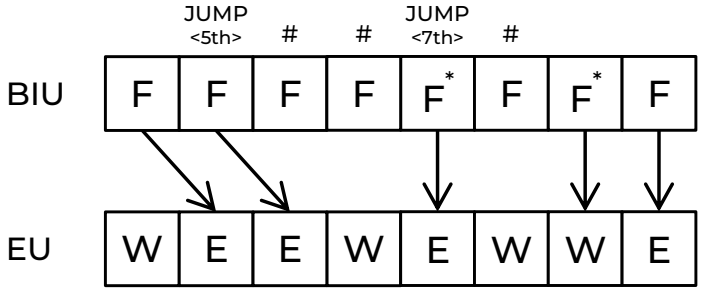
3. a) Consider the following fetch cycle in an 8086 BIU:

[Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch, Fetch]

When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the **2nd** instruction is a **'JUMP <6th instruction address>'**, the **5th** is a **'JUMP <7th instruction address>'** and **6th** instruction is a **'MOV <address>'** instruction, then **draw** the corresponding **BIU and EU's cycle**.

Solution:

BIU and EU's cycle has been drawn below:

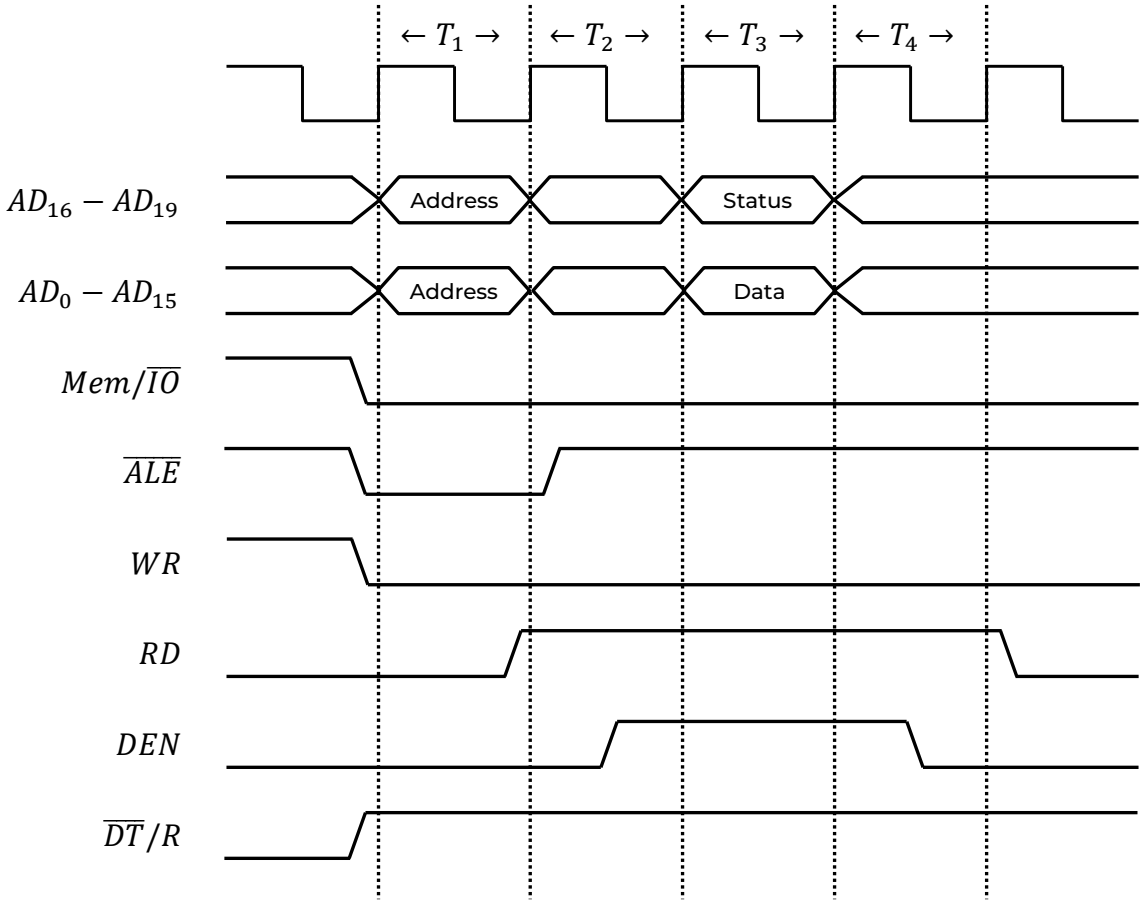


= Discard

3. b) **Draw** the timing diagram for **IO Read** operation of microprocessor **"808x"** showing the activities of $Mem/\overline{IO}$, Address-Data bus ($AD_0 - AD_{15}$, $AD_{16} - AD_{19}$), $\overline{ALE}$, WR, RD, DEN, $\overline{DT}/R$ in each clock cycle. **[Observe the pins carefully]**

Solution:

The timing diagram has been drawn below:



3. c) What is the **page fault**? What happens when a page fault occurs?

Solution:

Paging is one of the memory management techniques used for virtual memory multitasking operating system. If the page required by the processor is not in the main memory, then page fault occurs. There are two possible reasons for a page fault: either the page does not exist or the page was not prepared for load.

4. RAM Content

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	0000 0100
3H			BH	0010 0100
4H			CH	0000 0011
5H			DH	0000 0010
6H			EH	0001 0011
7H			FH	0000 0101

Opcode Table

Mnemonic	Opcode
HLT	1110
OUT	0101
SUB	0100
ADD	0110
LDA	1001

4. a) Write the **assembly code** for the below expression using the **RAM content**.

$$5 \times 4 - 2 \times 3$$

Hints: Multiplications can be done by Additions

Solution:

Given,

$$5 \times 4 - 2 \times 3 = 5 + 5 + 5 + 5 - (3 + 3)$$
$$= 5 + 5 + 5 + 5 - 3 - 3$$

Assembly Code:

```
LDA  FH
ADD  FH
ADD  FH
ADD  FH
SUB  CH
SUB  CH
OUT
HLT
```

Here,

$FH \rightarrow 5$

$CH \rightarrow 3$

4. b) Fill-up the **RAM content table** with the instructions **machine code. (Start from 0H)** Use the opcode given in the **opcode table**.

Solution:

RAM content table has been filled up below:

Address	Content
$0H$	1001 1111
$1H$	0110 1111
$2H$	0110 1111
$3H$	0110 1111
$4H$	0100 1100
$5H$	0100 1100
$6H$	0101 XXXX
$7H$	1110 XXXX

4. c) Explain what changes you have to make in **SAP-1** architecture to perform the instruction **OUTB** (Load the content of memory address to B register and show its value in the binary display). Also, Write the control words for execution T-states (T4, T5, T6) to perform the instruction using the given controller sequence.

CON = $\overline{C_p}\ \overline{E_p}\ L_M\ C_E \quad L_I\ E_I\ \overline{L_A}\ E_A \quad S_U\ \overline{E_U}\ L_B\ L_O$ **[Observe the pins carefully]**

Solution:

Control words for the instruction OUTB has been written below:

T4:	CON = $1110\ \ 0110\ \ 0100$ $= \mathrm{E64}H$	Instruction Register → Bus Bus → MAR
T5:	CON = $1101\ \ 0010\ \ 0110$ $= \mathrm{D26}H$	MAR → Bus Bus → B Register
T6:	CON = $1100\ \ 0010\ \ 0001$ $= \mathrm{C21}H$	Adder/Subtractor → Bus Bus → Out Register