United International University
Department of Computer Science and Engineering

CSE 3313: Computer Architecture

Midterm Examination: Fall 2024

Total Marks: 30 Time: 1 hour and 30 minutes

Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.

Answer all questions. Numbers to the right of the questions denote their marks.

1. (a) A processor with a clock rate of 3 GHz executes a program with the following instruction distribution:

	FP	INT	L/S	Branch
Instruction Count	150	20	50	35
CPI	5	3	4	2

We want to make the program run three times faster. Find the improvement factor of the given program if we use a better ALU that can only improve the time for FP instructions. [5]

(b) Suppose there are three instruction classes, X, Y, and Z, in a given instruction set architecture with CPIs of 1.5, 2.5, and 3.0 respectively. Two programs, Q1 and Q2, execute on this architecture, with the number of instructions from each class as follows:

Programs	Instruction Class		
	X	Y	Z
Q1	30	40	25
Q2	30	30	70

If both programs are executed on the same device with a clock frequency of 2.7 GHz, determine which program runs faster and by how much. [5]

2. Consider the following C function and assign registers according to your requirements.

```
1   int arr_sum(int arr[],int n){
2   int sum = 0, a = 10, b = -7, c = 12;
3   for(int i=0;i<n;i++){
4       if(arr[i]<=0){
5           b = (a < 15) && ( b != c)
6       }
7       else{
8           b = ((~15 + c) & 1)
9       }
10      sum += arr[i+b]
11  }
12  return sum;
13 }
```

(a) **Convert** the code to the corresponding MIPS assembly instructions. [8]

(b) **Convert** the first 8 lines of MIPS assembly instructions to the corresponding machine code. No need to convert it into binary. [4]

(c) Assume that the processor has 64 registers. The size of MIPS instruction is 32 bits and 6 bits are reserved for opcode. The structure for lw instruction is given in the table-1. **Find** out the maximum index number for an array in MIPS. [3]

opcode	rs	rt	constant

Table 1: Structure of lw instruction

3. (a) Using optimized multiplication algorithm, **show** each step of the multiplication of 6 by 8. [4]

(b) Assume we want to multiply three numbers A, B and C. Where A=10, B=11 and C=A*B. What will be minimum size of the product register we need to accomplish this multiplication? [1]

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	-
sw	43	-
and	0	36
or	0	37
nor	0	39
andi	12	-
ori	13	-
sll	0	0
srl	0	2
beq	4	-
bne	5	-
slt	0	42
j	2	-
jr	0	8
jal	3	-
addi	8	-

(a) MIPS Machine Codes

Name	Register Number
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$s0-$s7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31

(b) MIPS Registers