United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Final-Term Exam Trimester: Summer 2024

Course Code: CSE 4325 Course Title: Microprocessors and Microcontrollers

Total Marks: 50 Duration: 2 hours

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: Answer all the questions. (12.5 Marks)

Local Descriptor Table	
Index	**Address**
500H	Base: B56700, Limit: 0129H, Access right: 92H
501H	Base: B23900, Limit: 0F10H, Access right: FFH
502H	Base: B11C00, Limit: 0C12H, Access right: D1H
503H	Base: B67800, Limit: 0560H, Access right: A0H

An **80286 microprocessor** is executing a segment in protected mode and a portion of its descriptor table is given above. If the current physical address produced by this processor is **B123ABH**, then determine the followings:

a.	Find out the **descriptor (index number)** of which this physical address belongs to.	**[5]**
b.	For an offset value of **2D4H**, determine the **physical address**.	**[1.5]**
c.	Segment type (**CS/DS/SS/ES**).	**[2]**
d.	Has the segment been accessed?	**[1]**
e.	What is the descriptor privilege level?	**[2]**
f.	Is the descriptor defined or undefined?	**[1]**

Question 2: Answer all the questions. (12.5 Marks)

a.	Suppose, you are using a device which uses an **"N" bit ADC** on a **5v system**. This system converts an analog voltage of **3V** into a digital value of **2457**. **Find out the value of "N"**. If we want to reduce **quantization error**, should we increase or decrease the value of **"N"**? **Give an explanation for your answer.**	**[4+2]**
b.	Why is **I2C** called a **handshaking protocol**? In a particular communication in I2C, **Master (index - 10H)** receives **4 byte data (char - 'FaiL')** from **Slave (index - 14H)**. Draw the corresponding sequence diagram. **ASCII** codes for **'A'** and **'a'** are **65 and 97 respectively**.	**[1.5+3]**
c.	Design a **Smart Irrigation System** that automates water pumps based on soil moisture levels while sending data to a server for real-time monitoring. For example, when soil moisture drops below 50%, the pump automatically activates, and it turns off once the moisture reaches 55%. The system can be built using either a **Raspberry Pi (microprocessor-based system) or Arduino (microcontroller-based system)**. **Which platform would be more suitable?**	**[2]**

Question 3: Answer all the questions. (12.5 Marks)

a.	Consider the following fetch cycle in an 8086 BIU: [Fetch, Fetch, Fetch, Fetch, Fetch, Fetch,Fetch, Fetch] When the first instruction is being executed, two instructions are fetched and saved in the instruction queue. If the **2nd** instruction is a **'JUMP <4th>'**, the **3rd** is a **'JUMP <6th instruction address>'** and **6th** instruction is a **'MOV <address>'** instruction, then **draw** the corresponding **BIU and EU's cycle.**	**[4]**
b.	**I.** What is **'Wait State'** in an **8086 microprocessor**? Which **pin** is used to **insert 'Wait States'** into the timing of an **8086 microprocessor**? **II.** Draw the timing diagram for **Memory Write** operation of microprocessor "808x" showing the activities of $\overline{Mem/IO}$, *Address-Data bus (AD0 - AD15, AD16 - AD19), ALE,* $\overline{WR}$*, RD,* $\overline{DEN}$*,* $\overline{DT/R}$ in each clock cycle. **[Observe the pins carefully]**	**[3+4]**
c.	When does **page fault** occur in the paging mechanism?	**[1.5]**

Question 4: Answer all the questions. (12.5 Marks)

RAM Content

Address	Content		Address	Content
0H			8H	
1H			9H	
2H			AH	
3H			BH	0000 1000
4H			CH	0000 0010
5H			DH	0000 0001
6H			EH	0000 0110
7H			FH	0000 0011

Opcode Table

Mnemonic	Opcode
LDA	1001
ADD	0010
SUB	0001
OUT	0100
HLT	0011

a.	Write **the assembly code** for the below expression using the **RAM content**. $3^2 - 2^2 + 1^2$ [Hints: Exponents can be done by Multiplications, and Multiplications can be done by Additions]	**[5.5]**
b.	Fill-up the **RAM content table** with the instructions **machine code. (Start from 0H)**. Use the opcode given in the **opcode table**.	**[3]**
c.	Write the control words for Execution T-states (T4, T5, T6) to perform the instruction at **Address 3H** of the given RAM using the controller sequence below. **CON** = $C_p E_p \overline{L_M}\ \overline{C_E}\quad \overline{L_I}\ \overline{E_I}\ \overline{L_A} E_A\quad S_U E_U \overline{L_B}\ \overline{L_O}$	**[4]**