Register Number	Code: 2	OEC11T
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# I Semester Diploma Examination, Nov/Dec 2024

# **DIGITAL ELECTRONICS**

TIME: 3 HOURS MAX MARKS: 100

#### **Instructions:**

- (1) Answer one full question from each section I, II, III, IV and V.
- (2) Each one full question carries 20 marks.

### SECTION - I

1.	<ul> <li>(a) (i) State and explain Demorgan's theorem</li> <li>(ii) List the features of ASCII code</li> <li>(b) (i) Convert the Octal number 27.35 to binary</li> <li>(ii) Convert Hexadecimal number (123.45)<sub>16</sub> to Decimal</li> <li>(iii) Convert Binary code 10101 into Gray code</li> </ul>	5 5 3 4 3
2.	<ul> <li>(ii) Add 110110<sub>(2)</sub> and 110110<sub>(2)</sub></li> <li>(iii) Subtract ABCD<sub>(16)</sub> from DCBA<sub>(16)</sub></li> <li>(b) (i) Compare Analog and Digital signals</li> <li>(ii) List any five laws of Boolean algebra.</li> </ul>	3 3 4 5 5
3.	SECTION – II  (a) Define logic gate. Write the symbol, truth table and Boolean expression for AND, NAND and NOR gates (b) Realize NOT, AND, OR and NOR gate using NAND gate	10 10
4	<ul> <li>(a) Simply the following Boolean expression using K-map and draw the logic diagram Y=ĀBCD+ĀBCD+ABCD+ABCD+ABCD+ABCD+ABCD+ABCD+ABCD</li> <li>(b) (i) Convert the SOP F(A,B,C) = Σ(2,4,7) to POS (ii) Convert the POS F(A,B,C) = Π(3,5,6,7) to SOP</li> </ul>	10 5 5

# SECTION – III

5.		Explain the working of Full adder with truth table, Boolean expression and logic diagram.  (i) Explain Half Substractor with truth table, and logic diagram (ii) Explain the working of Serial binary adder	10 5 5
6.	3476 - 331	Construct 3-bit parallel adder and explain with an example Explain 2-bit magnitude comparator	10 10
		SECTION – IV	
7.	(a)	(i) Construct 4:1 mux using 2:1 mux	5
		(ii) Define multiplexer and list its applications	5 5
	(b)	Explain the working of 8:1 mux with logic circuit, expression	
		and truth table	10
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8.	(a)	Explain the working of decimal to BCD encoder with truth	1.0
	(1.)	table, expression and logic diagram	10
	(b)	(i) Write truth table, equation and logic diagram of 1:4 Demux	5
		(ii) Realize AND and OR gates using 2:1 Mux	3
		all.	
		SECTION – V	
9.	(a)	(i) Classify ICs based on scale of integration	5
		(ii) Explain the operation of 4:2 encoder with truth table and	
		logical expression	5
	(b)	Explain BCD to Decimal decoder with truth table, Boolean	
		expression and logic diagram	10
10	(a)	(i) List the features of TTL family	5
10.	(a)	(ii) List the features of TTE family  (ii) List advantages and disadvantages of ICs	5
	(b)	Sketch and explain BCD to Seven segment decoder using truth	J
	(-)	table	10

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