Code : 20EC11T

1166

Register Number | | | | | | | | | | |

I Semester Diploma Examination, August/September-2022

DIGITAL ELECTRONICS

Time : 3 Hours] [Max. Marks : 100

Instructions : (1) Answer **one** full question from each section.
(2) One full question carries **20** marks.

SECTION – I

1. (a) Perform following operations : **10**

(i) $192_{(10)} = \ldots\ldots\ldots_{(2)}$

(ii) $101.111_{(2)} = \ldots\ldots\ldots_{(10)}$

(iii) $ABC.12_{(16)} = \ldots\ldots\ldots_{(10)}$

(iv) $976_{(10)} = \ldots\ldots\ldots$BCD

(v) $82_{(10)} = \ldots\ldots\ldots_{(8)}$

(b) (i) Subtract $72_{(10)}$ from $98_{(10)}$ using 2' complement method. **7**

(ii) Compare analog and digital signals. **3**

2. (a) Perform following operations : **10**

(i) $FC12_{(16)} + ABFD_{(16)}$

(ii) $11011_{(2)} - 10111_{(2)}$

(iii) $10111_{(2)} + 11011_{(2)}$

(iv) Convert decimal number 972 to Excess 3 code

(v) $712_{(8)} + 531_{(8)}$

(b) (i) What are universal gates ? Write symbol and Boolean equations for universal gates. 5

(ii) What is an ASCII code ? List its any two features. 5

SECTION – II

3. (a) (i) Write any 5 Boolean identities. 5

(ii) Reduce the given Boolean equation using Boolean laws and rules and draw logic circuit. 5

$$Y = A\,B\,C + \bar{A}BC + \bar{A}\bar{B}\bar{C} + \bar{A}\,B\,\bar{C}$$

(b) State and prove Demorgan's theorem. 10

4. (a) Reduce the given equation using Karnaugh Map and write logic circuit for the reduced equation. 10

$$Y = \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BCD + ABCD + \bar{A}BC\bar{D} + ABC\bar{D}$$

(b) (i) Convert the SOP equation $Y = ABC + \bar{A}\bar{B}\bar{C}$ to POS equation. 5

(ii) Convert the POS equation $Y = (A + B + C)(\bar{A} + \bar{B} + \bar{C})$ to SOP equation. 5

SECTION – III

5. (a) (i) What are combinational circuits ? Give three examples. 5

(ii) Write truth table, equations, and logic diagram for Half Adder. 5

(b) What is full subtractor ? Write truth table, equations, and logic diagram for full subtractor. 10

6. (a) With neat circuit diagram explain operation of 3-bit parallel Adder. 10

(b) Write truth table, equations, and logic diagram for 2-bit comparator. 10

SECTION – IV

7. (a) What are multiplexers ? Write truth table, equations and logic diagram for 2 : 1 MUX. **10**

   (b) Write truth table, equations for 4 : 1 MUX. Implement 4 : 1 MUX using 2 : 1 MUX. **10**

8. (a) (i) Realize AND gate and OR gate using MUX. **5**

   (ii) Write truth table, equations, and logic diagram for 1 : 4 DEMUX. **5**

   (b) Write truth table, equations and logic diagram and explain decimal to BCD Encoder. **10**

SECTION – V

9. (a) Write truth table, equations and logic diagram for BCD to decimal decoder. **10**

   (b) Write truth table, equations and logic diagram for 4 : 2 priority encoder. **10**

10. (a) (i) Mention advantages and disadvantages of ICs. **5**

    (ii) Classify ICs based on scale of integration. **5**

    (b) (i) Mention features of standard TTL. **5**

    (ii) Describe the interfacing between TTL and CMOS. **5**

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SECTION – I

Q 1a. (1M step + 1M answer=2M)* 5 =10M

Q 1b.i. (converting 72 to binary 2M+converting 98 to binary 2M+finding 2'compliment 2M +answer 1M) = 7M

Q 1b.ii. (1M each difference *3) = 3M

Q 2a. (2M*5)=10M

Q 2b.i. (Definition 1M + symbols (1M + 1M) + equations (1M+ 1M) = 5M

Q 2b.ii. (What is ASCII 3M + features (1M *2)) = 5M

SECTION – II

Q 3a.i. Identities 1M*5=5M

Q 3a.ii. (Reduction 3M + circuit 2M) = 5M

Q 3b. Theorem1 (statement/Equation 2M +circuit 1M + TT 2M) + Theorem2 (statement/Equation 2M +circuit 1M + TT 2M)=10M

Q 4a. (Drawing map 1M + filling cells 2M + Grouping 3M + Reduced equation 2M + circuit diagram 2M) = 10M

Q 4b.i. SOP to POS (steps 3M + result 2M) = 5M

Q 4b.ii. POS to SOP (steps 3M + result 2M) = 5M

SECTION – III

Q 5a. (what is combinational ckt. 2M + examples (1M*3) = 5M

Q 5a.ii. (TT 2M + equations 2M + Ckt. 1M) = 5M

Q 5b. (What is full subtractor 3M + TT 2M + Equations 2M + circuit diagram 3M) = 10M

Q 6a. (circuit diagram 5M + Operation 5M) = 10 M

Q 6b. (TT 4M + Equations 3M + Ckt. 3M) =10M

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SECTION – IV

Q 7a. (What is MUX 3M + TT 2M + Equation 2M + circuit diagram 3M) = 10M

Q 7b. (TT 3M + Equation 2M + Implementation 5M) = 10M

Q 8a.i. (implementation of AND 3M + implementation of OR 2M) =5M

Q 8a.ii. (TT 2M + Equation 1M + circuit diagram 2M) = 5M

Q 8b. (TT 2M + Equation 4M +Explation 2M +circuit diagram 2M) = 10M

SECTION – V

Q 9a. (TT 2M + Equation 4M + circuit diagram 4M) = 10M

Q 9b. (TT 2M + Equation 4M + circuit diagram 4M) = 10M

Q 10a.i. Advantages 3M + Disadvantages 2M = 5M

Q 10a.ii. Classification 5M

Q 10b.i. Features (1M *5) =5M

Q 10b.ii. (Diagram 2M + Theory 3M) = 5M

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MODEL ANSWERS

SECTION – I

Q1a Perform following operations. 2*5=10M

(i)

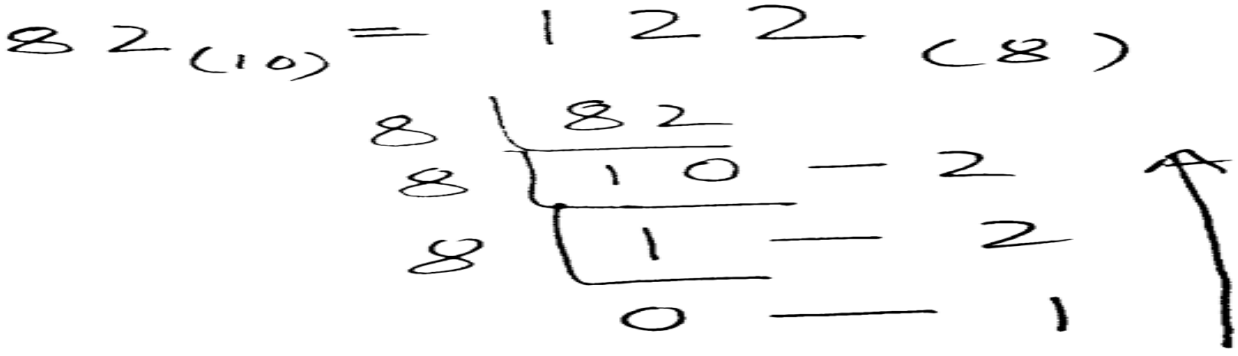
(ii) $101.111_{(2)} = (1*2^2)+(0*2^1)+(1*2^0)+ (1*2^{-1})+(0*2^{-2})+(1*2^{-3})=5.875_{(10)}$

(iii) $ABC.12_{(16)} = (A*16^2)+ (B*16^1)+(C*16^0)+(1*16^{-1})+ (2*16^{-2})$

$= (10*16^2)+ (11*16^1)+(12*16^0)+(1*16^{-1})+ (2*16^{-2}) =2748.07031_{(10)}$

(iv) $976_{(10)}$ = 1001 0111 0110 (BCD) write 4 bit BCD for each digit.

(v)



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Q1b.i. Subtract $72_{(10)}$ from $98_{(10)}$ using 2's complement method 2+2+2+1=7M

$98_{(10)} - 72_{(10)}$

1) $72_{(10)} = 1001000_{(2)}$

2 | 72	
2 | 36	– 0
2 | 18	– 0
2 | 9	– 0
2 | 4	– 1
2 | 2	– 0
2 | 1	– 0
0	– 1

2) $98_{(10)} = 1100010_{(2)}$

2 | 98	
2 | 49	– 0
2 | 24	– 1
2 | 12	– 0
2 | 6	– 0
2 | 3	– 0
2 | 1	– 1
0	– 1

3) 2's Complement of $72_{(10)}$ is

1's Complement + $1_{(2)}$

$0110111_{(2)} + 1_{(2)}$

$0111000_{(2)}$ is 2's complement

4) $1100010_{(2)} + 0111000_{(2)}$

or $1\ 0011010_{(2)}$

Neglect Carry

Ans = $0011010_{(2)} = 26_{(10)}$

Q1b.ii. Compare analog and digital signals.

Analog signal	Digital signal
Whose amplitude continuously changes with respect to time	Whose amplitude does not continuously changes with respect to time
Eg. sinusoidal waves	Eg. Square wave
Infinite number of states	Only 2 states ,logic 0 & logic 1
Noise is more	Noise is less
Difficult to debug analog circuits	Easy to debug digital circuts.

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Q2a. Perform following operations. 2M*5=10M

(i) $F\ C\ 1\ 2_{(16)}$
$+A\ B\ F\ D_{(16)}$

$1\ A\ 8\ 0\ F_{(16)}$

(ii) $1\ 1\ 0\ 1\ 1_{(2)}$
$-1\ 0\ 1\ 1\ 1_{(2)}$

$0\ 0\ 1\ 0\ 0_{(2)}$

(iii) $1\ 0\ 1\ 1\ 1_{(2)}$
$+1\ 1\ 0\ 1\ 1_{(2)}$

$1\ 1\ 0\ 0\ 1\ 0_{(2)}$

(iv) $973_{(10)}$ = 1100 1010 0110 Excess 3

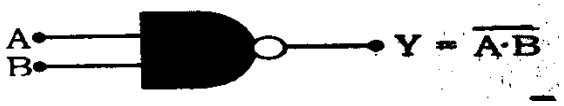
9+3 = 12 =1100 BCD 7+3 = 10 =1010 BCD 3+3 = 6 =0110 BCD

(v) $7\ 1\ 2_{(8)}$
$+5\ 3\ 1_{(8)}$

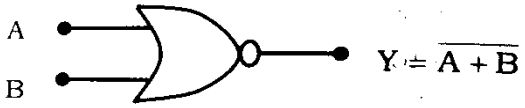
$1\ 4\ 4\ 3_{(8)}$

Q2b. What are universal gates? Write symbol and Boolean expressions for universal gates. 1+2+2=5M

NAND and NOR gates are called universal gates. By using only NAND or NOR gates, all basic gates ie AND,OR and NOT gates can be realized.



NAND gate



NOR gate

Q2b.ii. What is ASCII code? List its any two features. 3+2=5M

ASCII stands for American Standard code for Information Interchange.It is alphanumeric code ie it represent Numbers, alphabets and special characters. It is used in computers.

Features: 1.It is a 7 bit code. 2^7 = 128 ASCII codes are present.

2.ASCII for numbers from 0 to9 are obtained by preceding 011 to 4 bit value of the number. ASCII for 5 is 011 0101

3. This code allows manufacturers to standardize computer hardware such as keyboard ,printers and video displays.

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SECTION – II

Q3a.i. Write any 5 Boolean identities. 1M*5=5M

$A + 0 = A$	$A \cdot 1 = A$
$A + 1 = 1$	$A \cdot 0 = 0$
$A + A = A$	$A \cdot A = A$
$A + \bar{A} = 1$	$A \cdot \bar{A} = 0$
$\bar{\bar{A}} = A$	$\bar{\bar{A}} = A$
$A + AB = A$	$A(A + B) = A$
$A + \bar{A}B = A + B$	$A(\bar{A} + B) = AB$

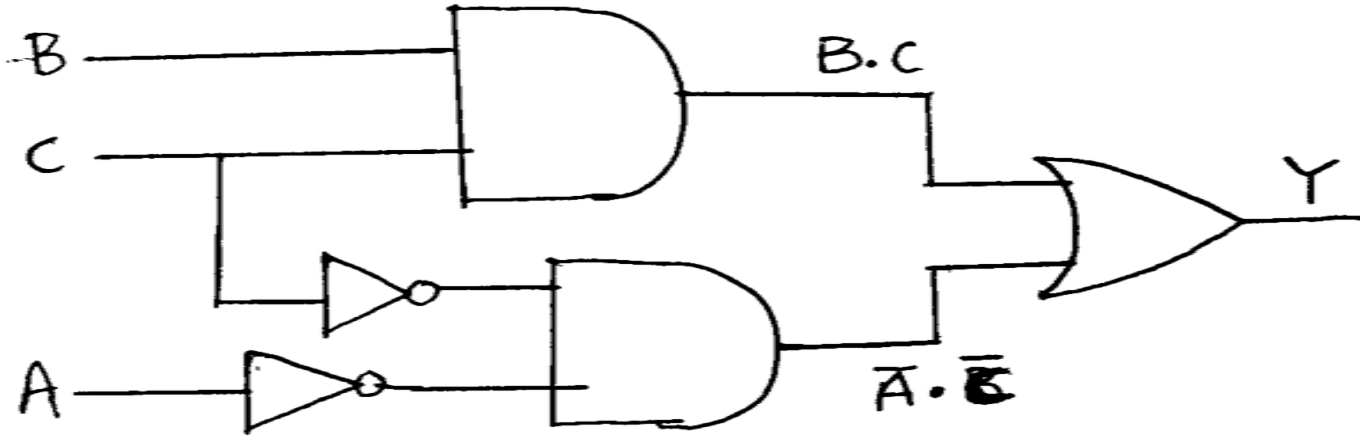
Q3a.ii. Reduce the given Boolean expression using laws and rules and draw logic diagram. 3+2=5M

$$Y = ABC + \bar{A}BC + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$$

$$= BC(A + \bar{A}) + \bar{A}\bar{C}(\bar{B} + B)$$

$$= BC \cdot 1 + \bar{A}\bar{C} \cdot 1$$

$$= BC + \bar{A}\bar{C}$$



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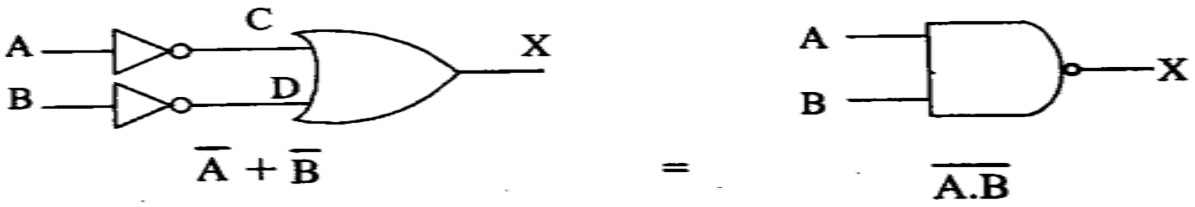
3b.State and prove Demorgan's theorems. 5+5=10M

(1) De Morgan's First theorem states that, "The complement of product of variables is equal to the sum of the complements of individual variables".

$$\overline{A} + \overline{B} = \overline{A.B}$$

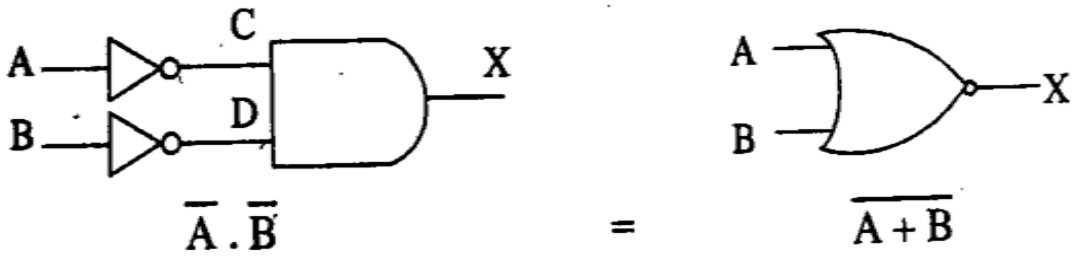
Proof using Truth Table



(2) De Morgan's Second theorem states that, "The complement of sum of variables is equal to the product of the complements of individual variables".

$$\overline{A}.\overline{B} = \overline{A+B}$$

Proof using Truth Table



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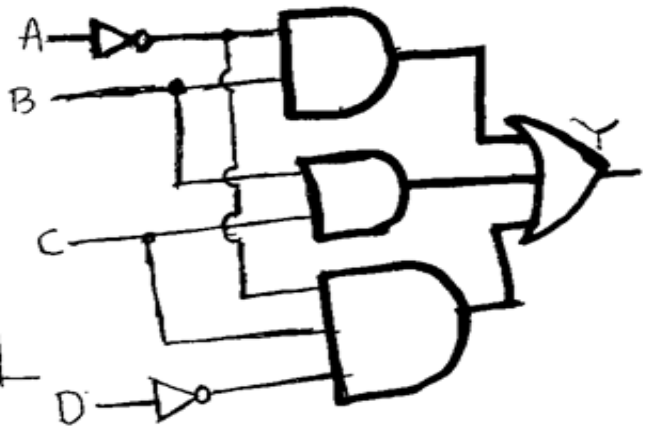
A	B	$\overline{A \cdot B}$	$\overline{A}+\overline{B}$	$\overline{A+B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	1	1	0	0
1	0	1	1	0	0
1	1	0	0	0	0

= =

4a.Reduce the given equation using Karnaugh map and write logic circuit for reduced equation.1+2+3+2+2=10M

$$Y = \overline{A}\,\overline{B}C\overline{D} + \overline{A}B\overline{C}\,\overline{D} + \overline{A}B\overline{C}D + \overline{A}BCD + ABCD + \overline{A}BC\overline{D} + ABC\overline{D}$$

CD \ AB	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	0	1	1	0
10	1	1	1	0



$$Y = \overline{A}B + BC + \overline{A}C\overline{D}$$

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Q4b.i. Convert the SOP equation to POS 3+2=5M

SOP to POS

$Y = ABC + \bar{A}\bar{B}\bar{C}$

In Simple form $Y = \sum (A,B,C)(7,0)$

1) Replace Σ by Π

2) Write all missing numbers till 7.

3) Write POS equation.

$Y = \Pi (A,B,C)(1,2,3,4,5,6)$

$Y = (A+B+\bar{C}) \cdot (A+\bar{B}+C) \cdot (A+\bar{B}+\bar{C}) \cdot (\bar{A}+B+C)$

$(\bar{A}+B+\bar{C}) \cdot (\bar{A}+\bar{B}+C)$.

Q4b.ii. Convert the given POS equation to SOP. 3+2=5M

POS to SOP

$Y = (A+B+C) \cdot (\bar{A}+\bar{B}+\bar{C})$

In simple form

$Y = \Pi (A,B,C)(0,7)$

To Convert to SOP

1) Replace Π by Σ

2) write all missing numbers till 7

3) write SOP equation.

$Y = \Sigma (A,B,C)(1,2,3,4,5,6)$

$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + ABC$

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SECTION – III

Q5a.i.What are combinational circuits? Give three examples.

A combinational circuit is the digital logic circuit in which the output depends on the combination of inputs at that point of time and not on past state of the output. There is no feedback from output to input .It does not have memory.

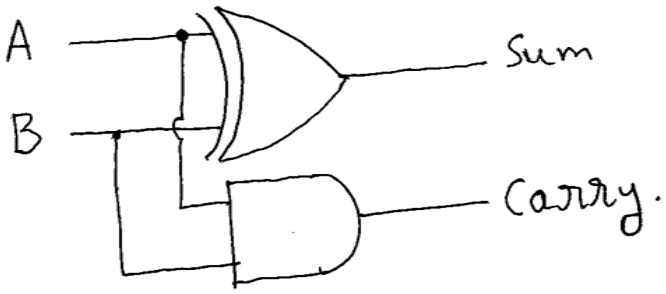
Examples: encoder, decoder, multiplexer, demultiplexer, half adder, full adder, half subtractor ,full subtractor .

Q5a.ii. Write truth table, equations and logic diagram for half adder. 2+2+1=5M

CARRY =A.B

$$Sum = A\bar{B} + \bar{A}B$$

$$Sum = A \oplus B$$



A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Q5b. What is full subtractor? Write truth table, equations and logic diagram for full subtractor. 3+2+2+3=10M

Full subtractor is a combinational circuit which subtracts three bits and gives out difference and borrow as outputs.

A	B	Bin	Difference(D) A-B-Bin	Borrow(B_{out})
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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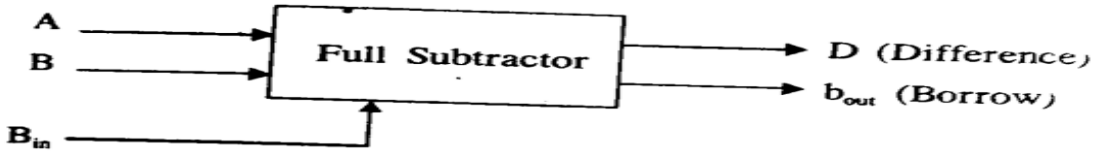

Difference

A \ B Bin	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$D = \bar{A}\bar{B}B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + ABB_{in}$$

$$D = A \oplus B \oplus B_{in}$$

Borrow

A \ B Bin	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$$Borrow = B_{out} = \bar{A}B_{in} + BB_{in} + \bar{A}B$$

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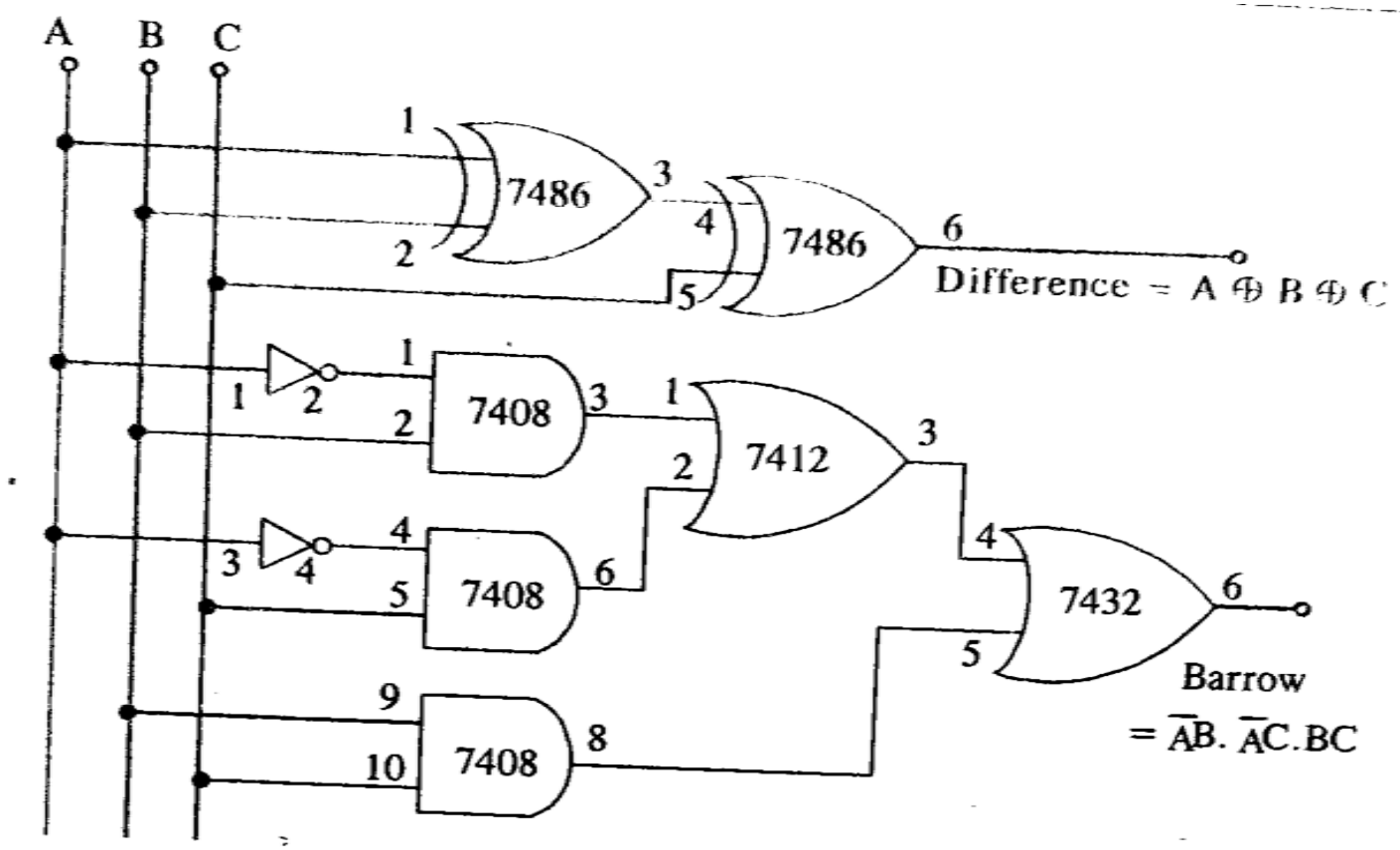
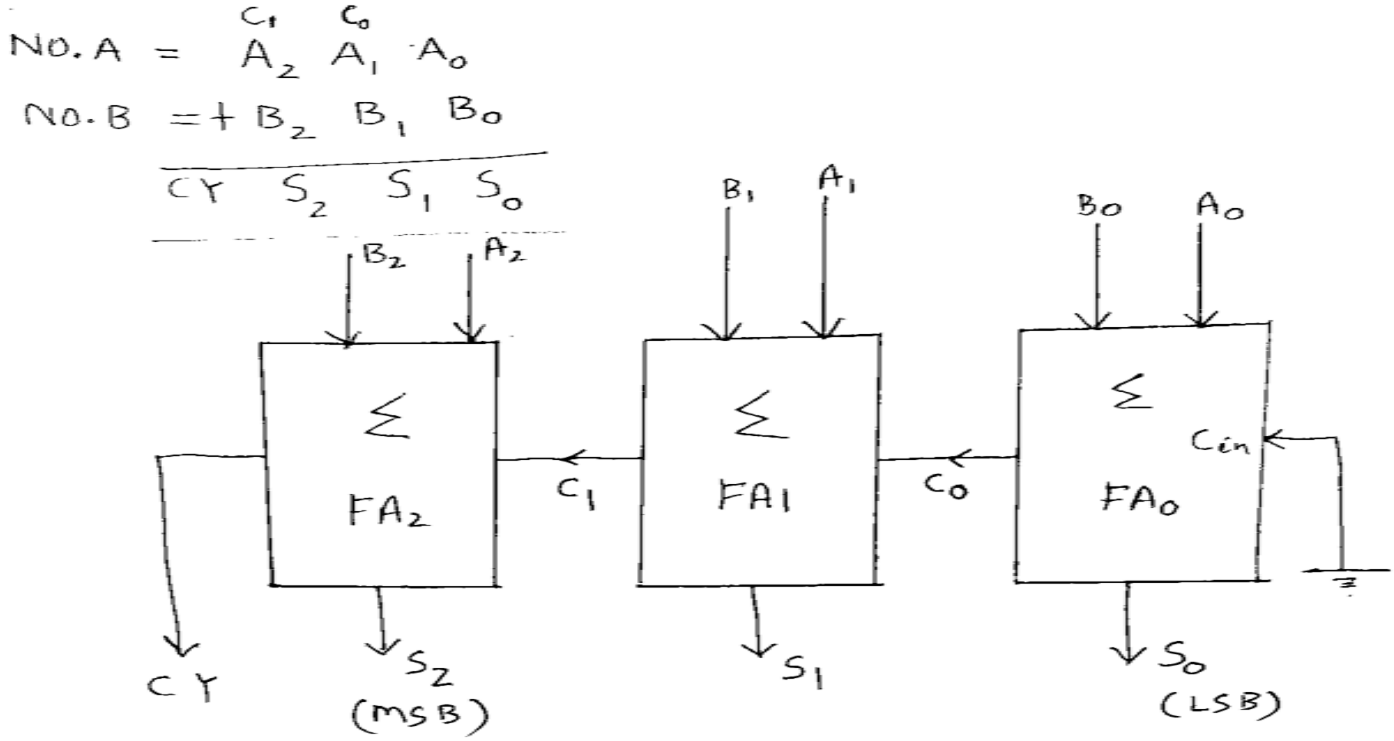


Q6a. With neat circuit diagram explain operation of 3bit parallel adder. 5+5=10M



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A 3 bit parallel adder consists of 3 full adders FA0,FA1 and FA2. FA0 is used as half adder by grounding Cin input.

FA0 addes A0 and B0 and generates LSB of sum S0 and carry C0.

FA1 addes A1 and B1 and generates next sum bit S1 and carry C1.

FA2 addes A2 and B2 and generates MSB of sum S2 and final carry CY.

Parallel adder are fast compared to serial adder.

Each adder has to wait for the carry which is to be generated from the previous adder in chain.

The propagation delay(delay associated with the travelling of carry bit) is found to increase with the increase in the number of bits to be added.

Q6b. Write truth table , equations and logic diagram for 2- bit comparator. 4+3+3=10M

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers.

Inputs are A=A1A0 , B = B1B0 Outputs are A=B , A < B , A > B

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

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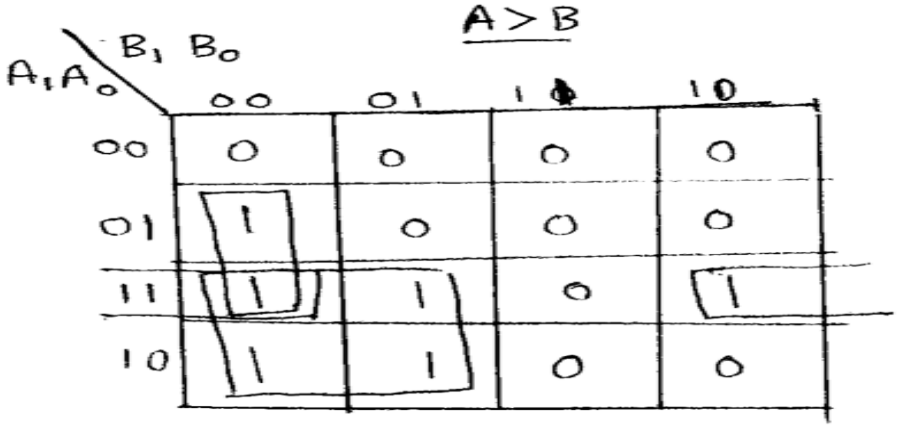
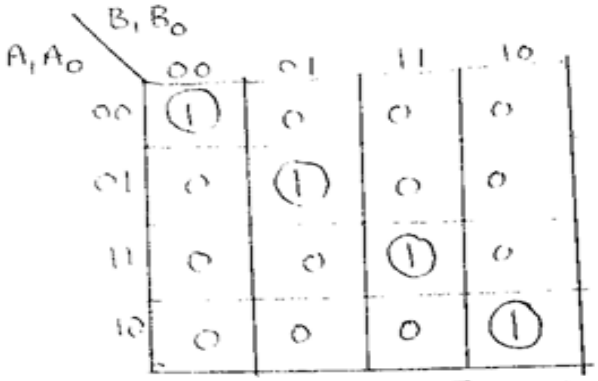
$A > B$



$$A > B = A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{B}_1 + A_1 A_0 B_0$$

$$A > B = A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{B}_1 + A_1 A_0 B_0$$

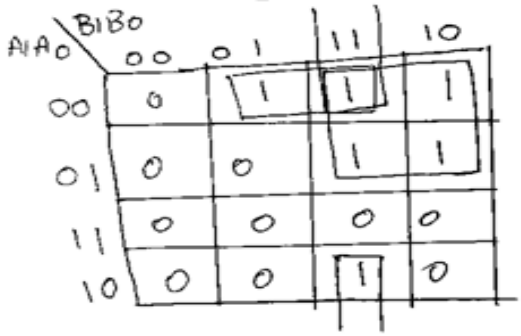
$A < B$



$$A < B = A_1 A_0 B_1 B_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$$

$$= \overline{(A_0 \oplus B_0)} \cdot \overline{(A_1 \oplus B_1)}$$

$A = B$



$$(A=B) = \bar{A}_1 B_1 + \bar{A}_0 B_1 B_0 + \bar{A}_1 \bar{A}_0 B_0$$

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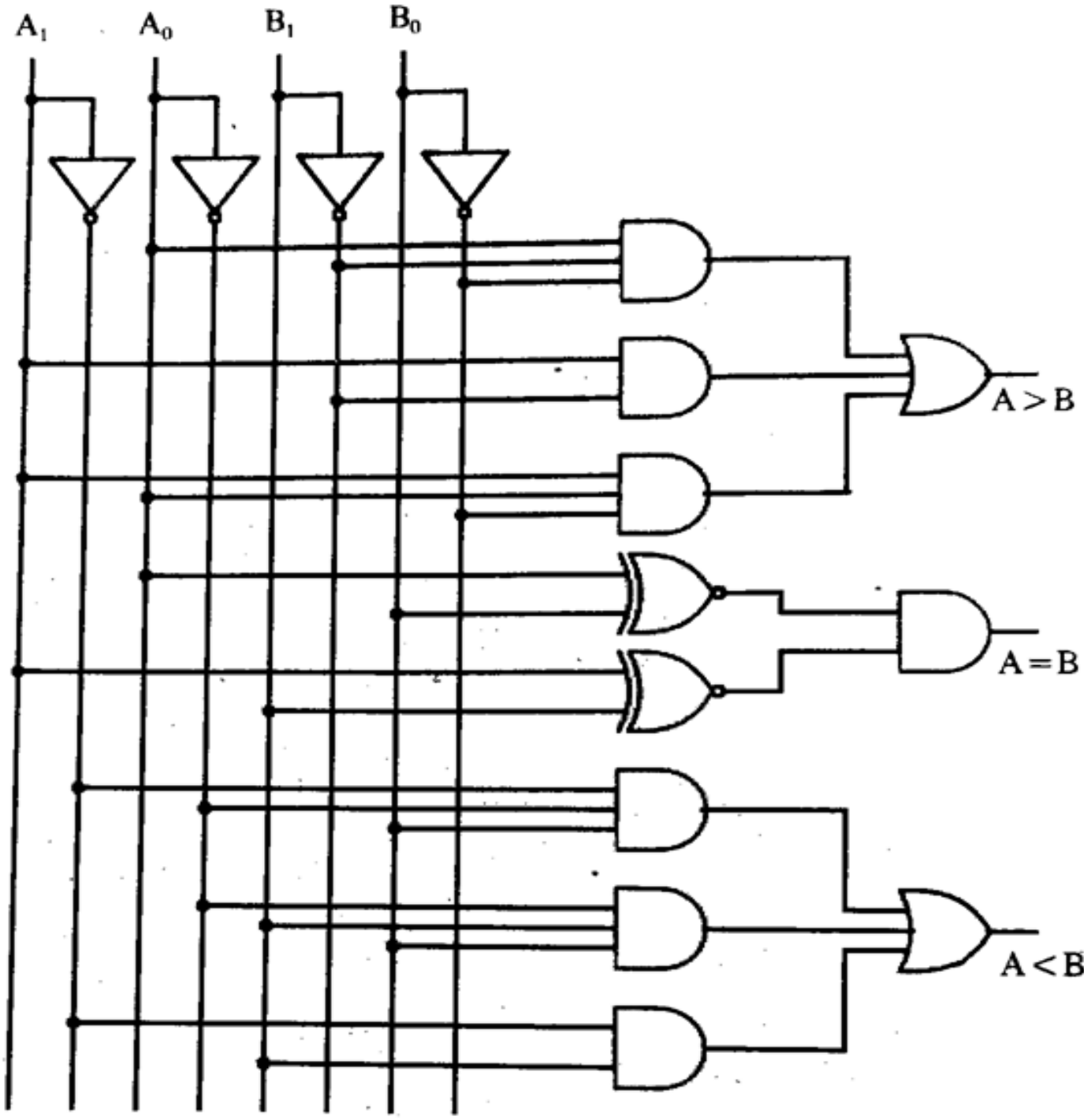

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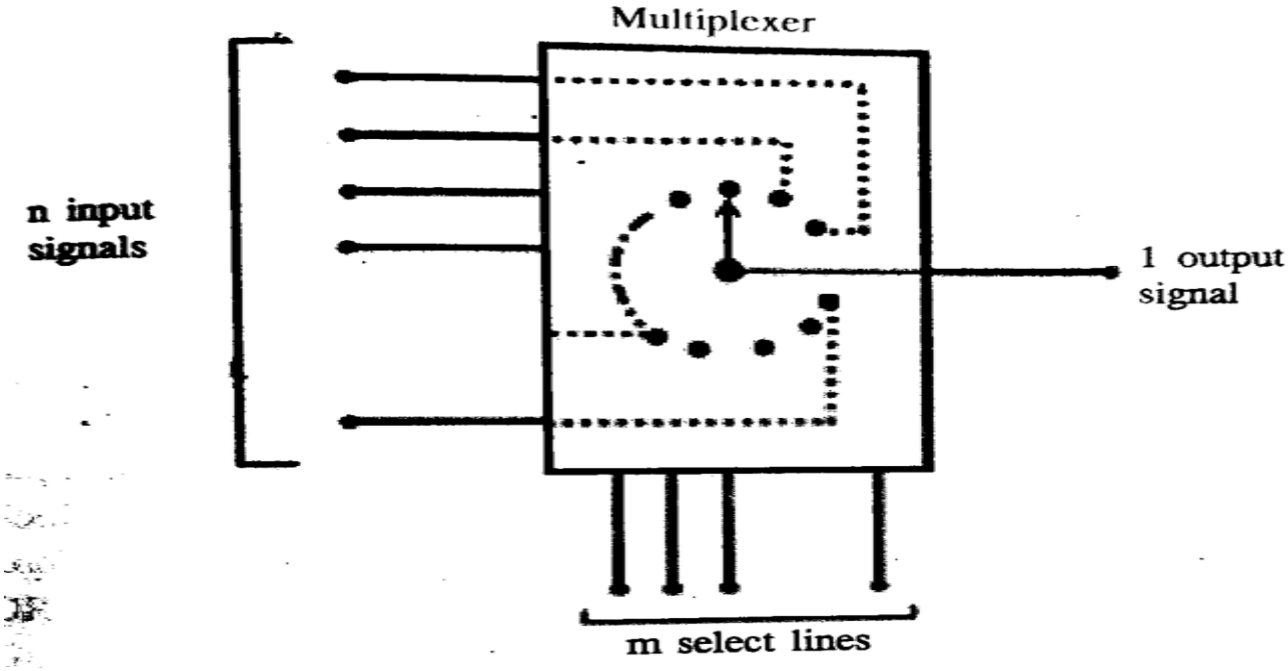
SECTION-IV

Q7a.What are Multiplexers? Write truth table , equations and logic diagram for 2:1 MUX. 3+2+2+3=10M

A multiplexer is a combinational digital logic circuit which has n number of inputs , only one output and m number of select line . Depending on the logic inputs on select lines one of the input is connected to the output.

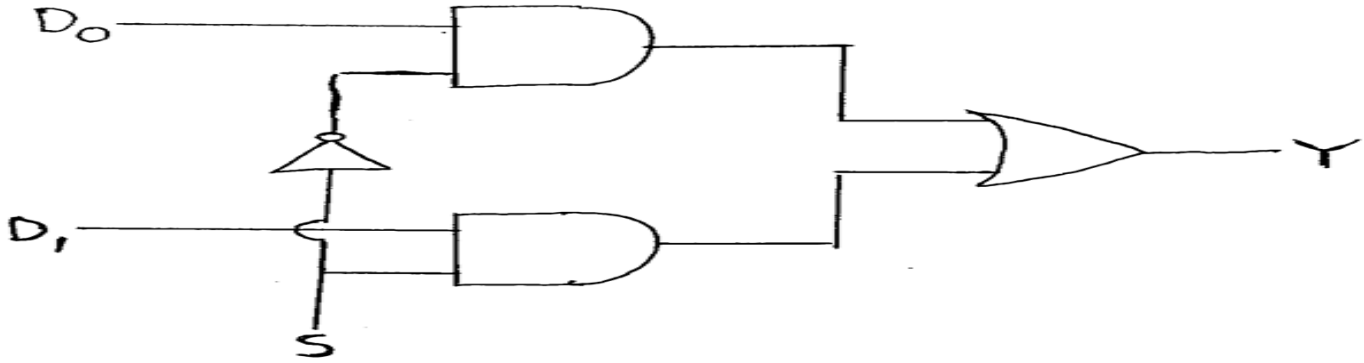
$2^m = n$. if there are 16 data lines then 4 select lines are required because $2^4 = 16$.It is used as data selector.

A 2:1 Mux has 2 data lines D0 and D1, $2^1 = 2$ hence 1 seslect line(S) and 1 output (Y).



S	Y
0	D0
1	D1

$Y = \bar{S} D_0 + S D_1$



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Q7b. Write truth table and equations for 4:1 MUX . Implement 4:1 MUX using 2:1 MUX. 3+2+5=10M

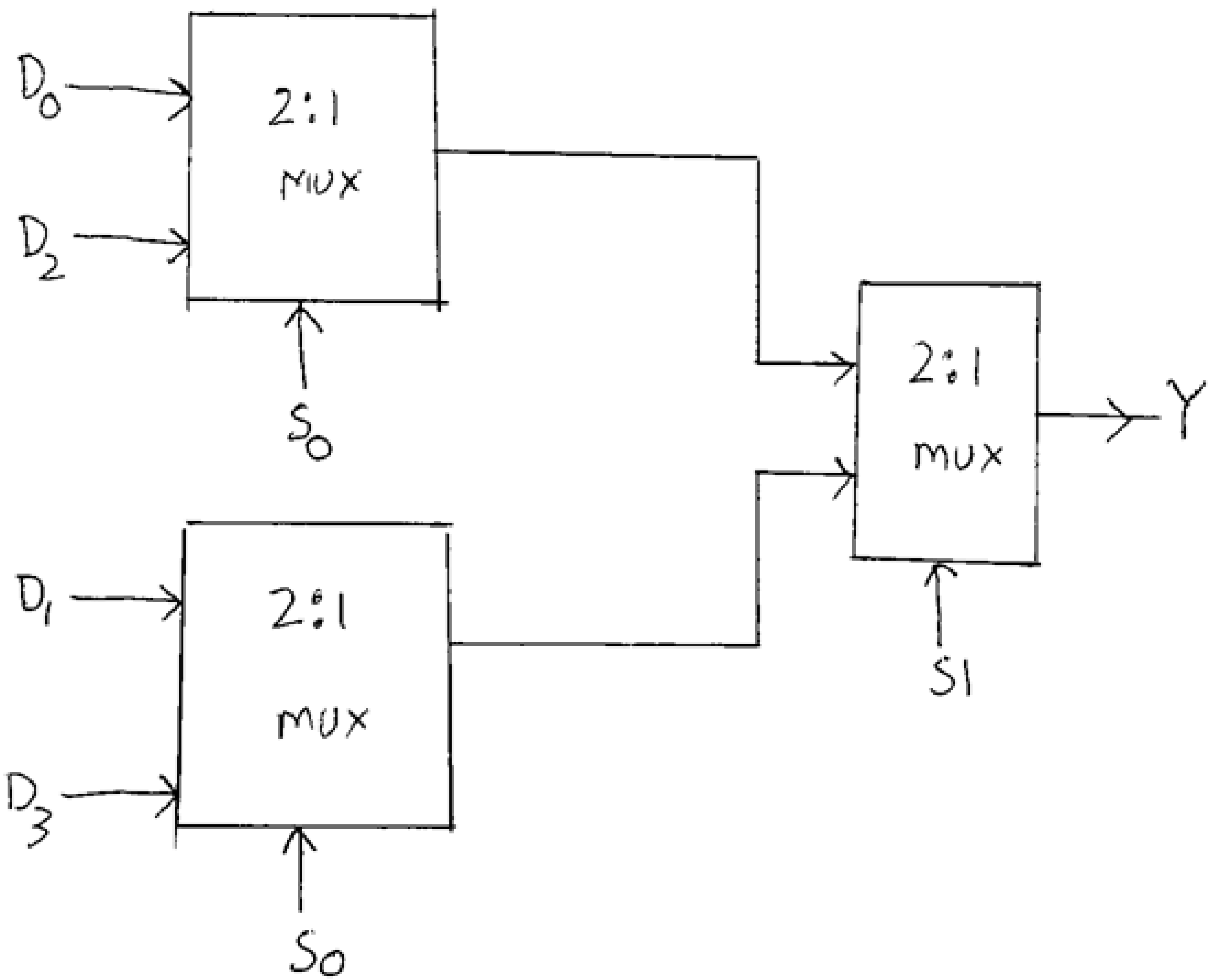
For 4:1 MUX : 4 Data lines (D0,D1,D2,D3) $2^2 = 4$ hence 2 select lines (S0, S1) , output (Y)

$Y = \overline{S0} . \overline{S1} . D0 + \overline{S0} . S1 . D1 + S0 . \overline{S1} . D2 + S0 . S1 . D3$

S0	S1	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

To implement 4:1 MUX using 2:1 MUX ,Three 2:1MUX are required.
To implement above truth table logic ckt is

$$Y = \overline{S_0}\,\overline{S_1}\,D_0 + \overline{S_0}\,S_1\,D_1 + S_0\,\overline{S_1}\,D_2 + S_0\,S_1\,D_3$$



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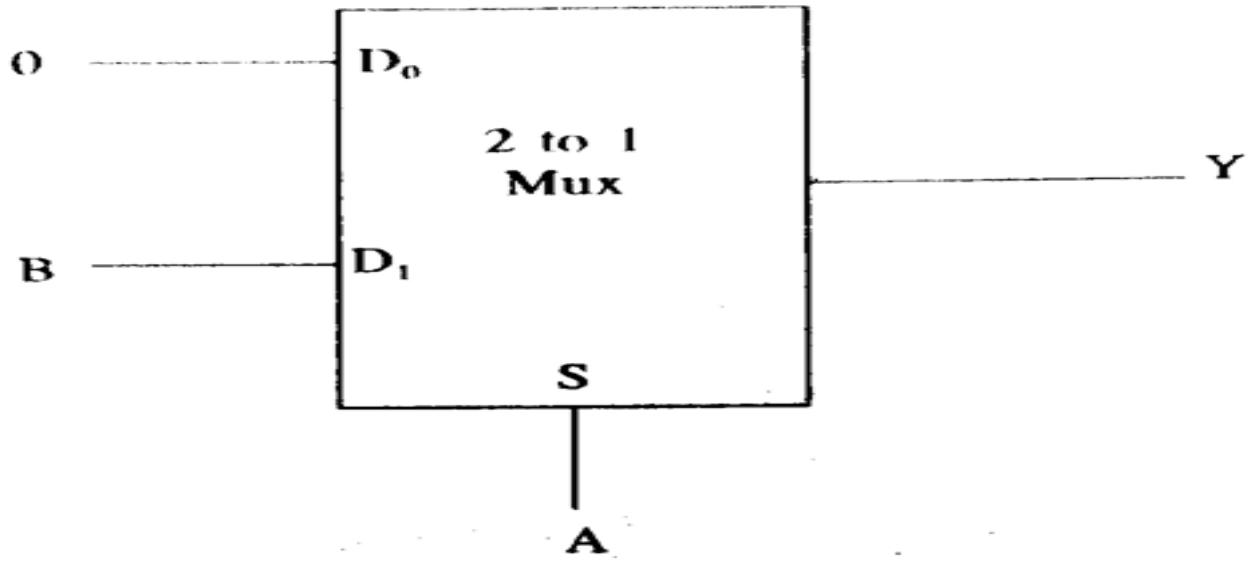
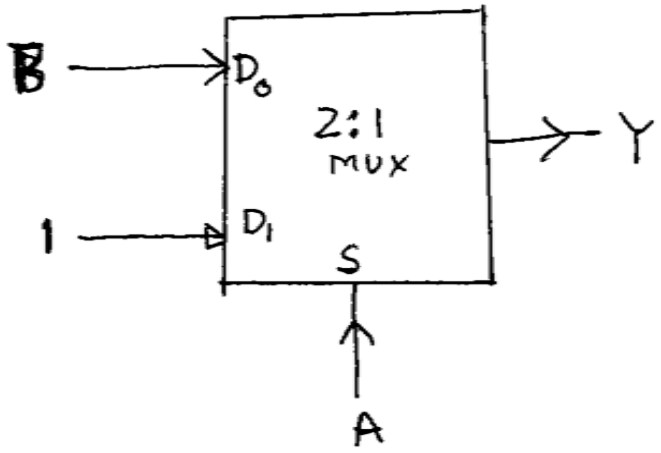
Q 8a.i. Realize AND gate OR gate using MUX. 3+2 = 5M

AND gate:



A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

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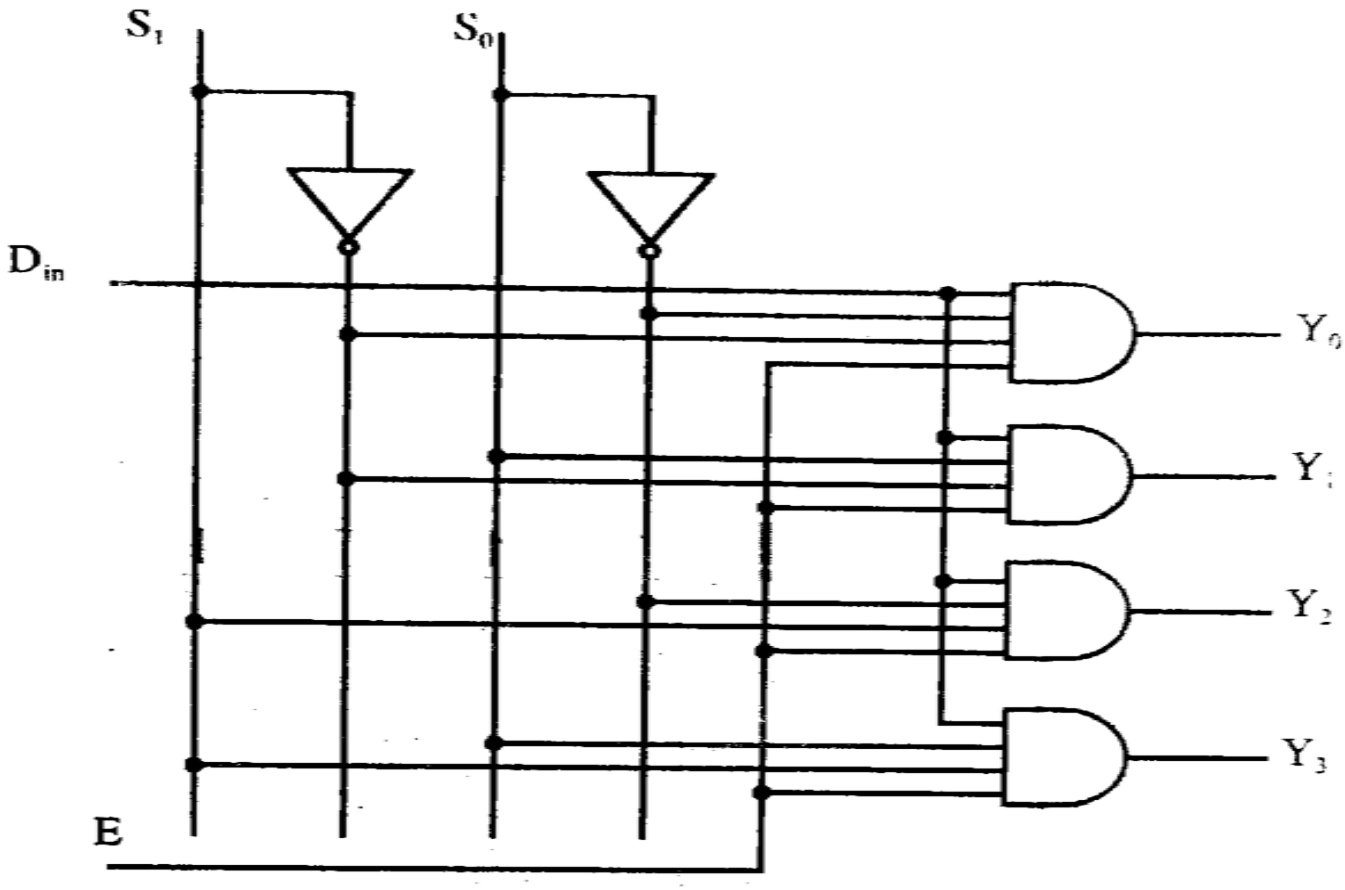
Q 8.a.ii. Write truth table , equations and logic diagram 1:4 DMUX. 2+1+2=5M

A 1:4 DMUX consists of one data line D_{in} , 2 select lines S0,S1 and 4 output lines Y0,Y1,Y2,Y3.

S0	S1	Y0	Y1	Y2	Y3
0	0	D_{in}	0	0	0
0	1	0	D_{in}	0	0
1	0	0	0	D_{in}	0
1	1	0	0	0	D_{in}

$Y0 = \overline{S0} \cdot \overline{S1} \cdot D_{in}$ $Y1 = \overline{S0} \cdot S1 \cdot D_{in}$ $Y2 = S0 \cdot \overline{S1} \cdot D_{in}$ $Y3 = S0 \cdot S1 \cdot D_{in}$



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8 b. Wite truth table equations and logic diagram and explain decimal to BCD encoder. 2+4+2+2=10M

Decimal to BCD encoder converts decimal number to BCD.It has 10 inputs corresponding to 10 decimal numbers

0 to 9. F0ur output lines A,B,C,D the BCD output.

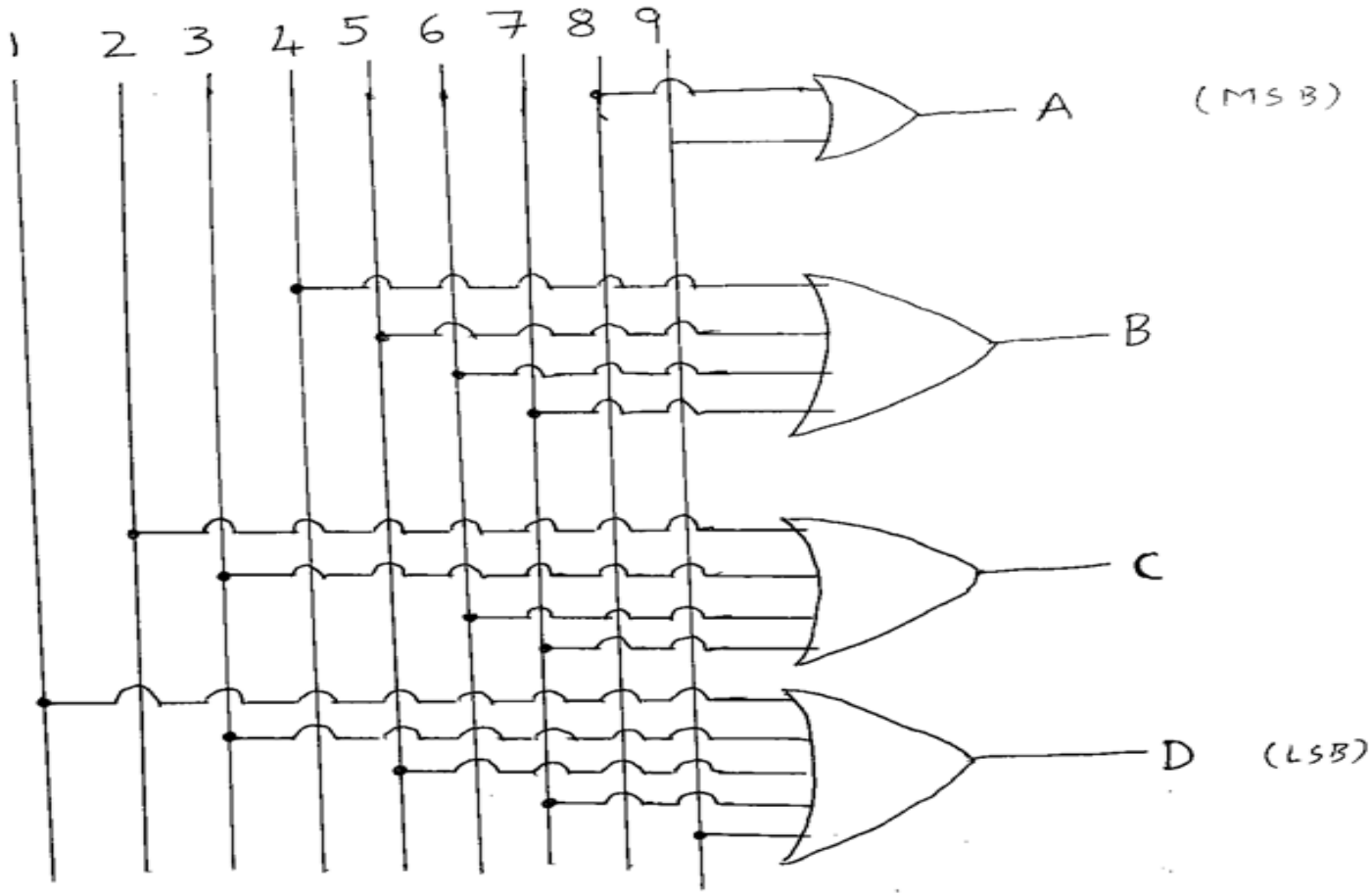
A=8+9

B=4+5+6+7

C=2+3+6+7

D=1+3+5+7+9

Decimal	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1



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SECTION-V

Q 9a. Write truth table , equations , and logic diagram for BCD to decimal decoder. 2+4+4=10M

A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

A,B,C,D BCD inputs. 0 to 9 Decimal outputs.

$0 = \overline{A} . \overline{B} . \overline{C} . \overline{D}$ $1= \overline{A} . \overline{B} . \overline{C} . D$ $2= \overline{A} . \overline{B} . C . \overline{D}$ $3= \overline{A} . \overline{B} . C . D$ $4= \overline{A} . B . \overline{C} . \overline{D}$

$5= \overline{A} . B . \overline{C} . D$ $6= \overline{A} . B . C . \overline{D}$ $7= \overline{A} . B . C . D$ $8= A . \overline{B} . \overline{C} . \overline{D}$ $9= A . \overline{B} . \overline{C} . D$

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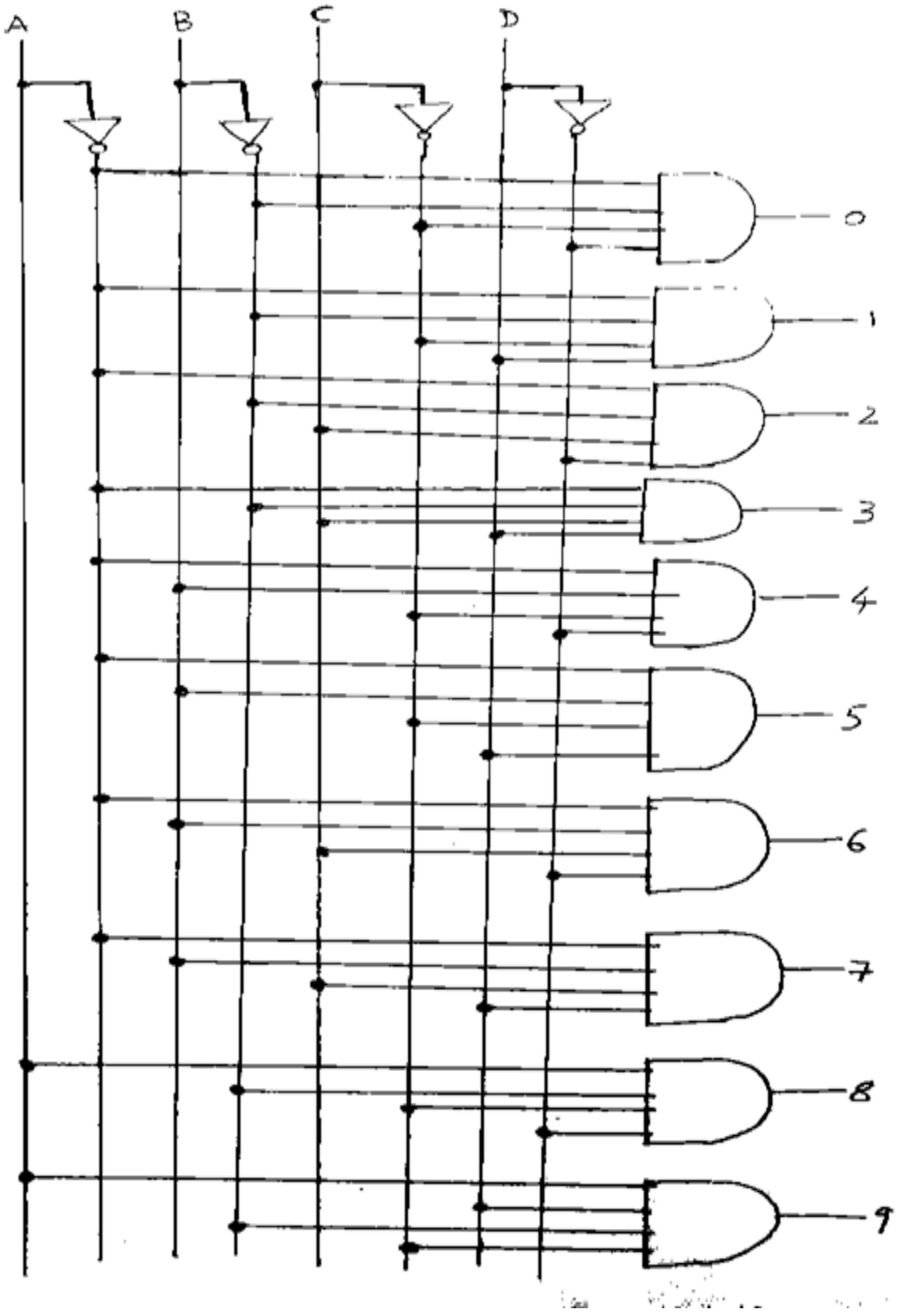

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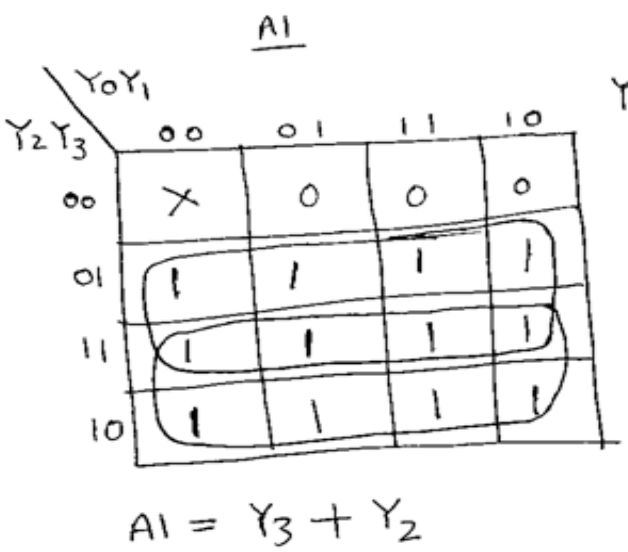
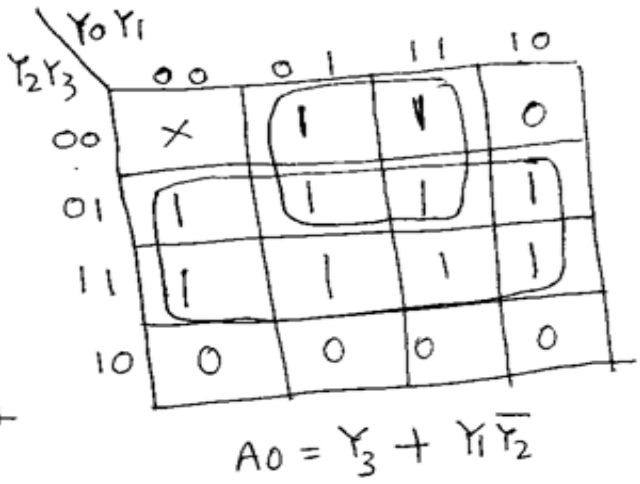
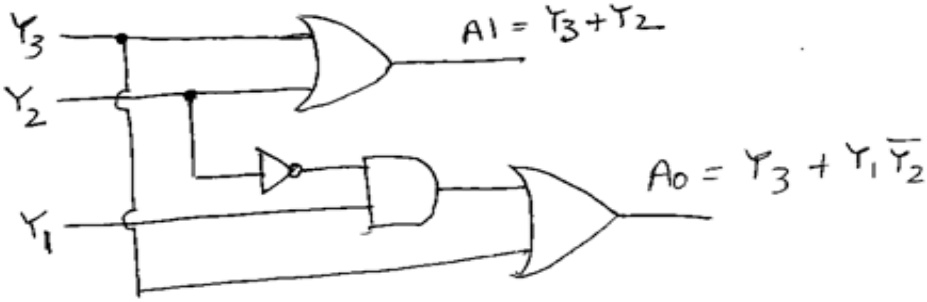
Q 9.b. Write truth table , equations and logic diagram for 4:2 priority encoder. 2+4+4=10M

A 4 to 2 priority encoder has **4 inputs** : Y3, Y2, Y1 & Y0 and **2 outputs** : A1 & A0. Here, the input, Y3 has the **highest priority**, whereas the input, Y0 has the **lowest priority**. In this case, even if more than one input is '1' at the same time, the output will be the (binary) code corresponding to the input, which is having **higher priority**.

Y3	Y2	Y1	Y0	A1	A0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1







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Q 10 a.i. Mention advantages and disadvantages of IC's. 3+2=5M

ADVANTAGES OF IC'S

The main advantages IC as follows
1. **Very small size**: Thousands around components be incorporated square inch of chip.
2. **Lesser weight**: large number of components can packed in a single, weight is reduced.
3. **Reduced cost**: Due to mass production technique, price is reduced.
4. **High reliability**: Due to absence of soldered connection, few interconnections and small temperature rise And failure rate is low.
5. **Low power requirement**: As the size is small power consumption is less.

4 **Easy replacements**: In case of failure chip can easily be replaced.

Disadvantages of integrated circuit

The main disadvantages of ICs are as follows
1.In an IC the various components are part of a small semiconductor chip and the individual component or components cannot be removed or replaced, therefore, if any component in an IC fails, the whole IC has to be replaced by a new one.
2. Inductors and Transformers cannot be incorporated in ICs.
3. It is not possible to fabricate capacitors that exceeds value of 30pF. Thus, high value capacitors are to be Connected externally to the IC.
4. Limited power rating as it is not possible to manufacture high power (greater than 10 W) ICs.
5. Quite delicate in handling, as these cannot withstand rough handling or excessive heat.
6. Because of its small size, it cannot dissipate more heat,when current in it increased. Hence ICs are damaged due to over current flowing through them.

Q 10 a.ii. Classify IC's based on scale of integration. 1M*5=5M

1.**Small scale integration (SSI)**
The number of gates in the IC is less than 10, ie in a single package.
2.**Medium-sale integration (MSI)**
The number of gates in the IC is 10 to 100,ie in a single package.
3.**Large-scale integration (LSI)**
The number of gates in the IC is between 100 and 1000,ie in a single package.
4.**Very large-scale integration (VLSI)**
The number of gates in the IC is 20,000 to 10,00,000,ie in a single package.
5.**Ultra large scale integration(ULSI)**
The number of gates in the IC is 10,00,000 to 1,00,00,000,ie in a single package.

Q10.b. Mention features of standard TTL. 1M*5=5M

Features of Standard TTL family are:
1) P-delay (propagation delay) 10 ns
2) Power dissipation 10 mw per gate
3) Speed power product 100 PJ
4) Fan out 10
5) Basic gate are NAND
6) Fan in 8
7) Noise margin 0.5 mV.

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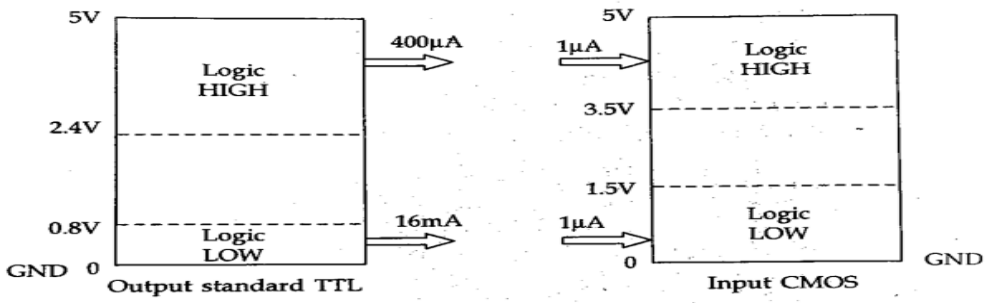
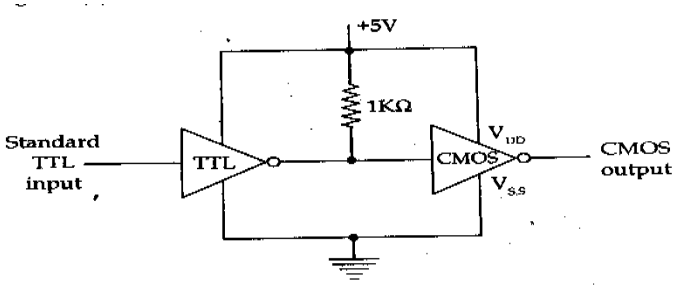
Q 10b.ii. Describe the interfacing between TTL and CMOS. 2+3=5M



While designing digital systems using integrated circuits from different logic families, there is a need to interface the devices correctly. Since the logic voltage levels for different families are defined differently. Therefore at the lead which joins them, additional electronic components need to be connected to make them compatible. Above Fig. shows voltage levels and current for TTL and CMOS IC's.



The low outputs (V_{OL}) from the TTL (0 to 0.8V) are compatible. Because they fit in wider low input bond (V_{IL}) (0 to 1.5V) on CMOS IC. The HIGH output (Vo_H) from TTL IC is 2.4V to 5V and CMOS IC (V) is 3.5V to 5V. The range 2.4V to 3.5V will not fit within HIGH range of CMOS IC.

Hence when interfacing a TTL to CMOS IC using same +5V supply, a pull up resistor is required. This resistor is used to ensure that logic high is of sufficient voltage amplitude to operate CMOS IC properly. This is because of logic level voltage is greater för CMOS then for TTL logic HIGH.

The TTL IC's I_{OH} and loc currents are sufficiently higher then I_{IH} and I_{IL} currents of CMOS. Driving CMOS from TTL the currents levels are not at all a problem.

CERTIFICATE

"I certify that the model answer script prepared by me for the subject code 20EC11T is from the prescribed text books and the model answer script and the scheme of valuation prepared by me is correct."

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