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VIVADO Simulator

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Outline

- Xilinx VIVADO Download and License Setting
- Create project and run Synthesis



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Xilinx VIVADO Download and License Setting



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Download Xilinx VIVADO (1/7)

- <https://www.xilinx.com/support/download.html>

[Home](#) / Adaptive Computing Support / Downloads

Downloads

Licensing Help

NIC Software & Drivers

Vivado (HW Developer) Vitis (SW Developer) Vitis Embedded Platforms Power Design Manager Alveo Packages PetaLinux Device Models Documentation Navigator

Version

2024.1

2023.2

2023.1

Vivado Archive

ISE Archive

CAE Vendor Libraries Archive

Vivado™ Edition - 2024.1 Full Product Installation

Important Information

Vivado™ 2024.1 is now available for download:

- General Access of MicroBlaze™ V soft processor (based on RISC V Open-Source ISA)
- QoR (FMAX) Enhancements for Versal Devices
 - Optimized clocking and D&D across SLP boundaries (for multi-SLP D)

Download Includes

Vivado Design Suite (All Editions)

Download Type

Full Product Installation

Last Updated

May 30, 2024

Answers

2024.x - Vivado Known Issues



Download Xilinx VIVADO (2/7)

- Download the installer from the 2024.1 tab corresponding to your operating system.

[AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1: Windows Self Extracting Web Installer \(EXE - 215.97 MB\)](#)

MD5 SUM Value : 075106c94592da6806a37a662ea0af43

Download Verification [i](#)

[Digests](#) [Signature](#) [Public Key](#)

[AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1: Linux Self Extracting Web Installer \(BIN - 291.7 MB\)](#)

MD5 SUM Value : 8b0e99a41b851b50592d5d6ef1b1263d

Download Verification [i](#)

[Digests](#) [Signature](#) [Public Key](#)



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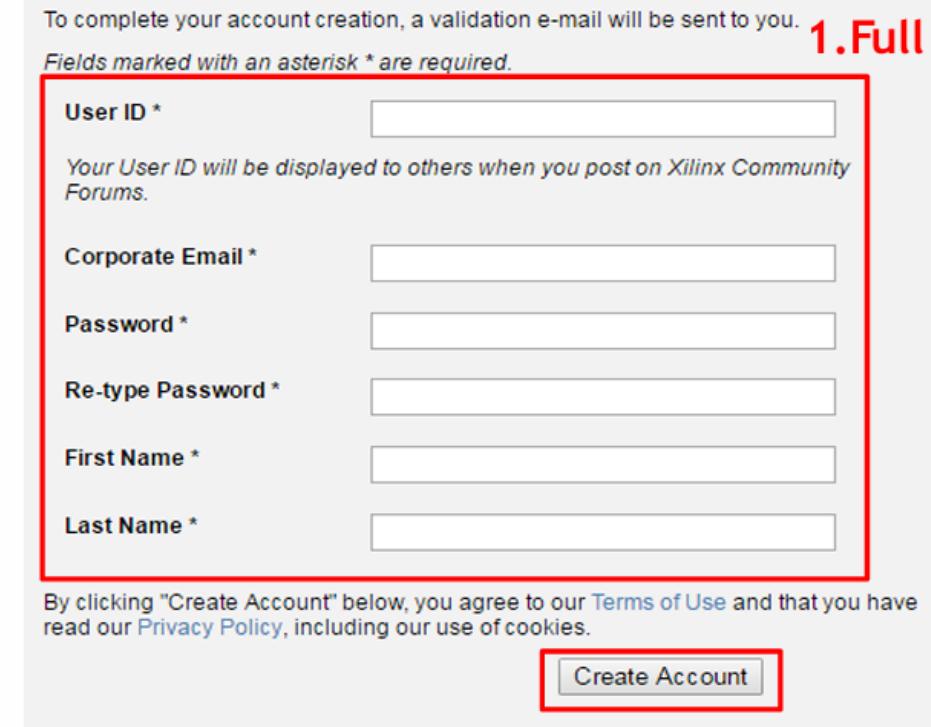
Download Xilinx VIVADO (3/7)

- Create an account and sign in



The AMD login page features the AMD logo at the top. Below it is a large "登入" (Login) button. Underneath are fields for "電子郵件地址" (Email Address) containing "r12k41004@ntu.edu.tw" and "密碼" (Password) with a redacted input field. A "登入" (Login) button is located below these fields. A "創建密碼" (Create Password) button is at the bottom. A red arrow points from the text "click" to the "創建密碼" button.

Create Account



The "Create Account" page has a header stating "To complete your account creation, a validation e-mail will be sent to you. Fields marked with an asterisk * are required." A red box highlights the "User ID *" field and its descriptive text: "Your User ID will be displayed to others when you post on Xilinx Community Forums." Below this are fields for "Corporate Email *", "Password *", "Re-type Password *", "First Name *", and "Last Name *". A red box also surrounds the "Create Account" button at the bottom. Red annotations "1.Full" and "2.Click" are placed near the highlighted fields and button respectively.



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Download Xilinx VIVADO (4/7)

- Create an account and sign in

Activate Your Account

Your Xilinx.com account has been created but not activated. An E-mail has been sent to wendyfang1028@gmail.com. Please follow the instructions in the E-mail to activate your account and continue with the registration process.

Thank you,
Xilinx, Inc.

Xilinx Registration: Account Activation 收件匣

login_help@xilinx.com
 寄给我

英文 中文（繁體） 翻譯郵件

Dear fang luo,

To activate your Xilinx.com account, visit the following link within 30 days and log in with your User ID:
<https://secure.xilinx.com/webreg/activate.do?languageID=1&key=dne1f258ff3>

User ID: fangfang1028

If you don't activate your account within 30 days, you must re-register.
If you did not attempt to create an account, you may ignore this email or [report this incident](#).

Sincerely,
Xilinx Customer Service

3. Authenticate E-mail



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Download Xilinx VIVADO (5/7)

- Create an account and sign in

My Profile

Please update your profile information by expanding the selections below.

Fields marked with an asterisk * are required.

1. Full

- Personal Information
- Documentation and Design Advisory Alerts
- E-mail Announcements, Xcell Journal, and monthly Newsletter

Save Profile

2. Click



Thank You!

Your request for the Xilinx Subscription Preferences has been completed.

3. Back to Download



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Download Xilinx VIVADO (6/7)

- Fill in the form again...

Download Center - Name and Address Verification

U.S. Government Export Approval

- U.S. export regulations require that your First Name, Last Name, Company Name and Shipping Address be verified before AMD can fulfill your download request. [Please provide accurate and complete information.](#)
- Addresses with Post Office Boxes and names/addresses with Non-Roman Characters with accents such as grave, tilde or colon **are not supported** by US export compliance systems.

First Name *

Last Name *

E-mail *

Company Name *

Address 1 *

Address 2

Location *

 State/Province

City *

 Postal Code

Phone



Download Xilinx VIVADO (7/7)

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- Scroll down to the bottom and download the file
- Execute the downloaded file

Filename:

FPGAs_AdaptiveSoCs_Unified_2024.1_0522_2023_Win64.exe

If you are downloading the Vivado / Vitis unified installer, you will receive a follow-up confirmation email with a notice regarding our Developer Program.

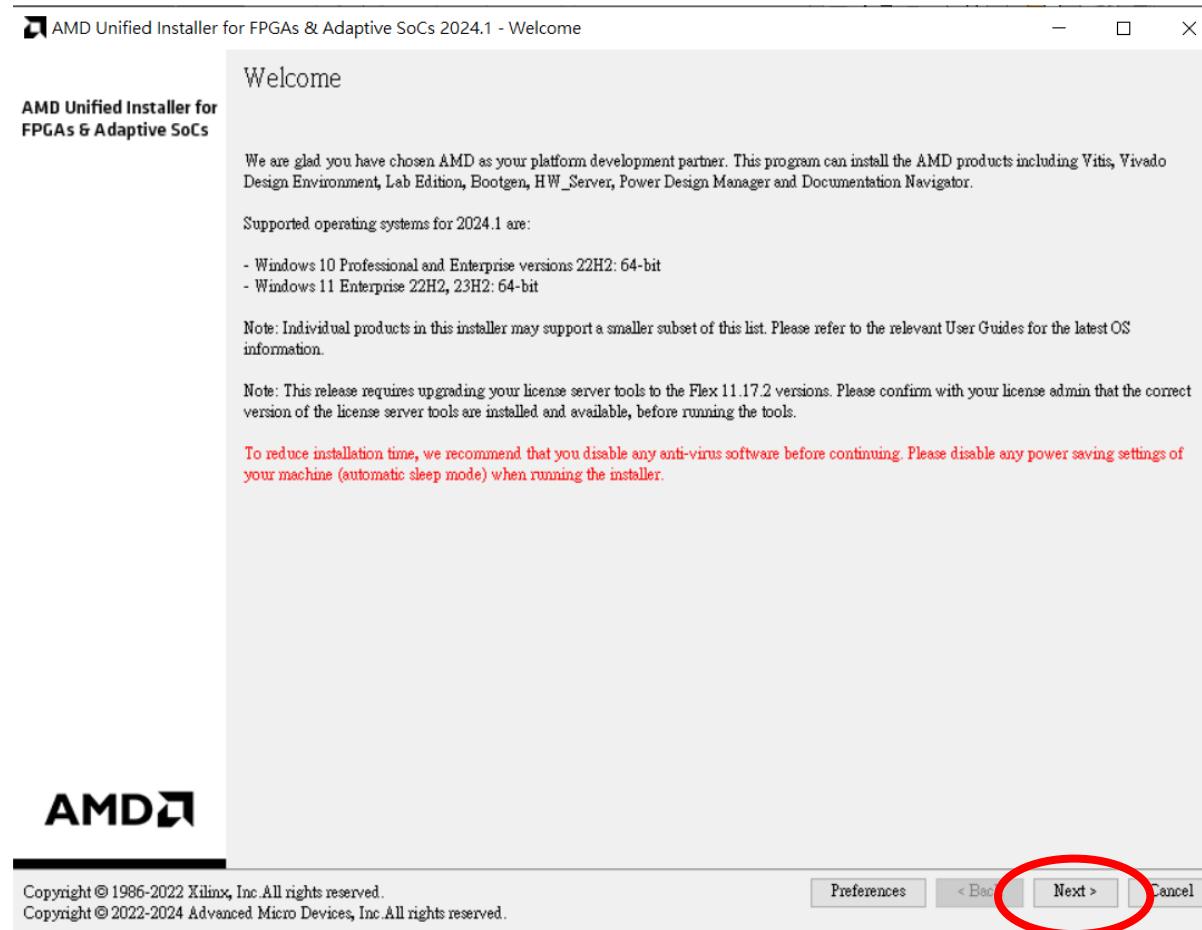
You can read about how we handle your personal data, your personal data rights, and how you can contact us in our [privacy notice](#).





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Install Xilinx VIVADO





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Install Xilinx VIVADO

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1 - Select Install Type

Select Install Type

Please select install type and provide your AMD.com E-mail Address and password for authentication.

1. User Authentication

Please provide your AMD user account credentials to download the required files.
If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).

E-mail Address: r12k41004@ntu.edu.tw
Password: [REDACTED]

2. Download and Install Now

Select your desired device and tool installation options and the installer will download and install just what is required.

Download Image (Install Separately)

The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.

3.

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< Back Cancel



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Install Xilinx VIVADO

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1 - Select Product to Install

Select Product to Install

Select a product to continue installation. You will be able to customize the content in the next page.

Vivado

Includes the full complement of Vivado Design Suite tools for design, including C-based design with Vitis High-Level Synthesis, implementation, verification and device programming. Complete device support, cable driver, and Document Navigator included. Users can also install Vitis Model Composer to design for AI Engines and Programmable Logic in MATLAB and Simulink. Users can select to install the Vitis Embedded Development which is an embedded software development package. There is an option to install Power Design Manager for power estimation of Versal, UltraScale+, and Kria products.

Vitis Embedded Development

The Vitis Embedded Development is a standalone embedded software development package for creating, building, debugging, optimizing, and downloading software applications for AMD FPGA processors. It includes a new Vitis IDE with its new backend Vitis Server, as well as the classic command line utilities such as hw_server, bootgen and program_flash.

BootGen

Installs Bootgen for creating bootable images targeting AMD SoCs and FPGAs.

Lab Edition

Installs only the Vivado Lab Edition. This standalone product includes Vivado Design Programmer, Vivado Logic Analyzer and UpdateMEM tools.

Hardware Server

Installs hardware server and JTAG cable drivers for remote debugging.

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1. Vivado

2.



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Install Xilinx VIVADO

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1 - Select Edition to Install

Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

Vivado ML Standard

Vivado ML Standard Edition is the no-cost, device limited version of the Vivado ML Enterprise edition. Users can add Vitis Model Composer which is an AMD toolbox for MATLAB and Simulink to design for AI Engines and Programmable Logic. Users can select to install the Vitis Embedded Development which is an embedded software development package. If you have been using AMD System Generator for DSP, you can continue development using Vitis Model Composer. There is an option to install Power Design Manager for power estimation of Versal, UltraScale+, and Kria products.

Vivado ML Enterprise

Vivado ML Enterprise Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vitis HLS, implementation, verification, and device programming. Complete device support, cable drivers, and documentation Navigator are included. Users can add Vitis Model Composer which is an AMD toolbox for MATLAB and Simulink to design for AI Engines and Programmable Logic. Users can select to install the Vitis Embedded Development which is an embedded software development package. If you have been using AMD System Generator for DSP, you can continue development using Vitis Model Composer. There is an option to install Power Design Manager for power estimation of Versal, UltraScale+, and Kria products.

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< Back [Next >](#) Cancel

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Install Xilinx VIVADO

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1 - Vivado ML Enterprise

Vivado ML Enterprise

Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.

Vivado ML Enterprise Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vitis HLS, implementation, verification, and device programming. Complete device support, cable drivers, and documentation Navigator are included. Users can add Vitis Model Composer which is an AMD toolbox for MATLAB and Simulink to design for AI Engines and Programmable Logic. Users can select to install the Vitis Embedded Development which is an embedded software development package. If you have been using AMD System Generator for DSP, you can continue development using Vitis Model Composer. There is an option to install Power Design Manager for power estimation of Versal, UltraScale+, and Kria products.

AMD

Design Tools

- Vivado Design Suite
 - Vivado
 - Vitis HLS
 - Vitis Model Composer (Toolbox for MATLAB and Simulink. Includes the functionality of System Generator for DSP)
 - Vitis Embedded Development
 - Power Design Manager (PDM)
 - DocNav

Devices

- Install Devices for Kria SOMs and Starter Kits
- Production Devices
 - SoCs
 - 7 Series
 - UltraScale
 - UltraScale+
 - Versal ACAP

Engineering Sample Devices

Installation Options

- Install Cable Drivers (You MUST disconnect all Xilinx Platform Cable USB II cables before proceeding)
- Acquire or Manage a License Key

Download Size: 22.38 GB
Disk Space Required: 80.03 GB

2.

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Install Xilinx VIVADO

- Checking all checkboxes and click “next”

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1 - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

AMD

End User License Agreement for Vivado
By checking "I Agree" below, or OTHER WISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

End User License Agreement for DocNav
By checking "I Agree" below, or OTHER WISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

Third Party Software End User License Agreement for DocNav
By checking "I AGREE" below, or OTHER WISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agree

Third Party Software End User License Agreement for Vivado
By checking "I AGREE" below, or OTHER WISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

I Agreed

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< Back Next > Cancel

Search Lab. 16



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Install Xilinx VIVADO

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.1 - Select Destination Directory

Select Destination Directory

Choose installation options such as location and shortcuts.

Choose directory as you wish

Installation Options

Select the installation directory
C:\Xilinx

Installation location(s)
C:\Xilinx\Vivado\2024.1
C:\Xilinx\Vitis_HLS\2024.1
C:\Xilinx\Model_Composer\2024.1
D:\Xilinx\DocNav

Download location
C:\Xilinx\Downloads\Vivado_2024.1

Select shortcut and file association options

Create program group entries
Kilinx Design Tools

Create desktop shortcuts

Create file associations

Apply shortcut & file association selections to
 Current user
 All users

Make sure that you have enough disk space

Disk Space Required

Download Size:	22.38 GB
Disk Space Required:	80.03 GB
Final Disk Usage:	46.4 GB
Disk Space Available:	185.82 GB

⚠ Program group entry, Kilinx Design Tools, already exists for 2024.1. Specify a different program group entry.
⚠ This tool is not versioned. Any new installation of the tool will overwrite the existing installation.

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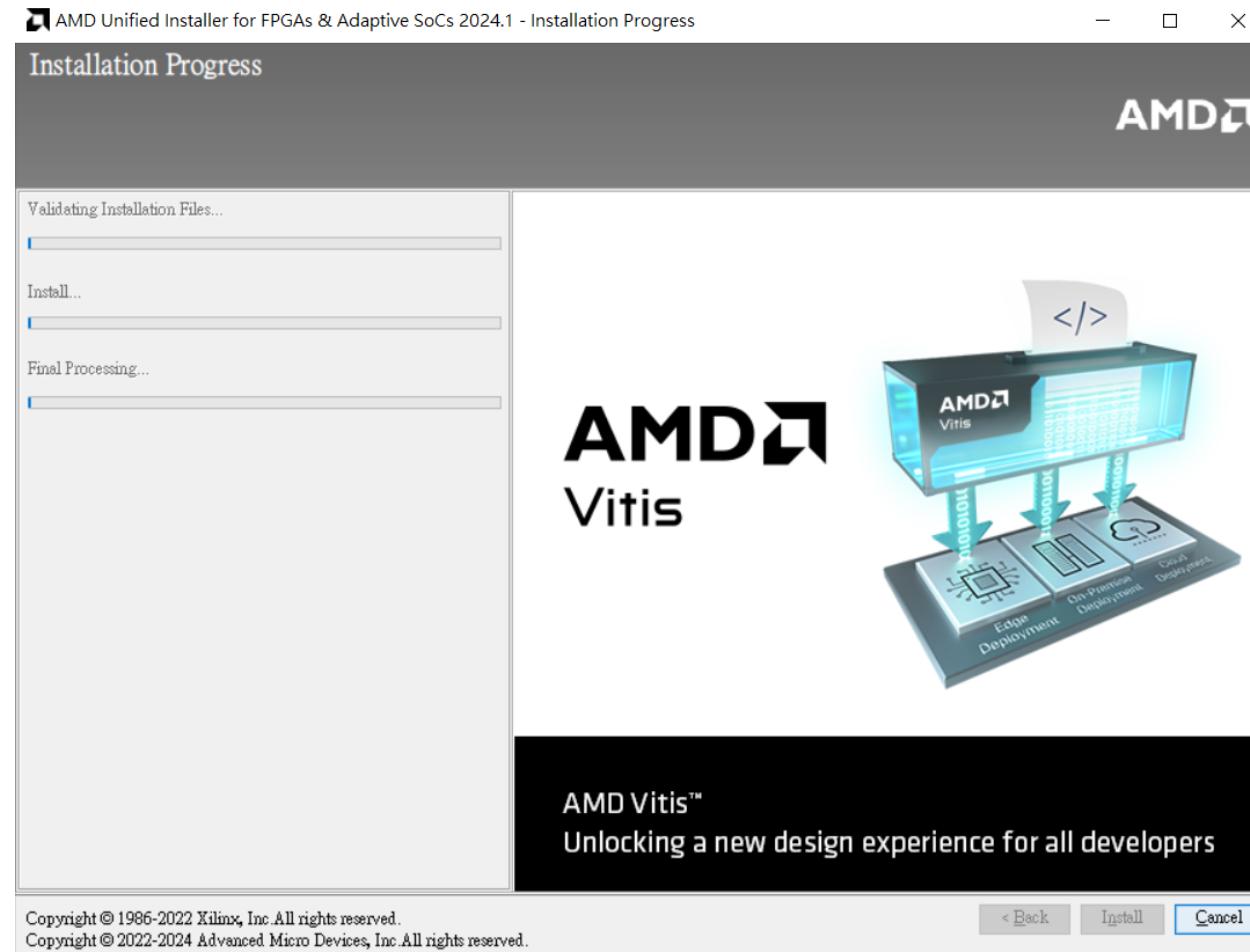
< Back **Next >** Cancel



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Install Xilinx VIVADO

- Click install and wait

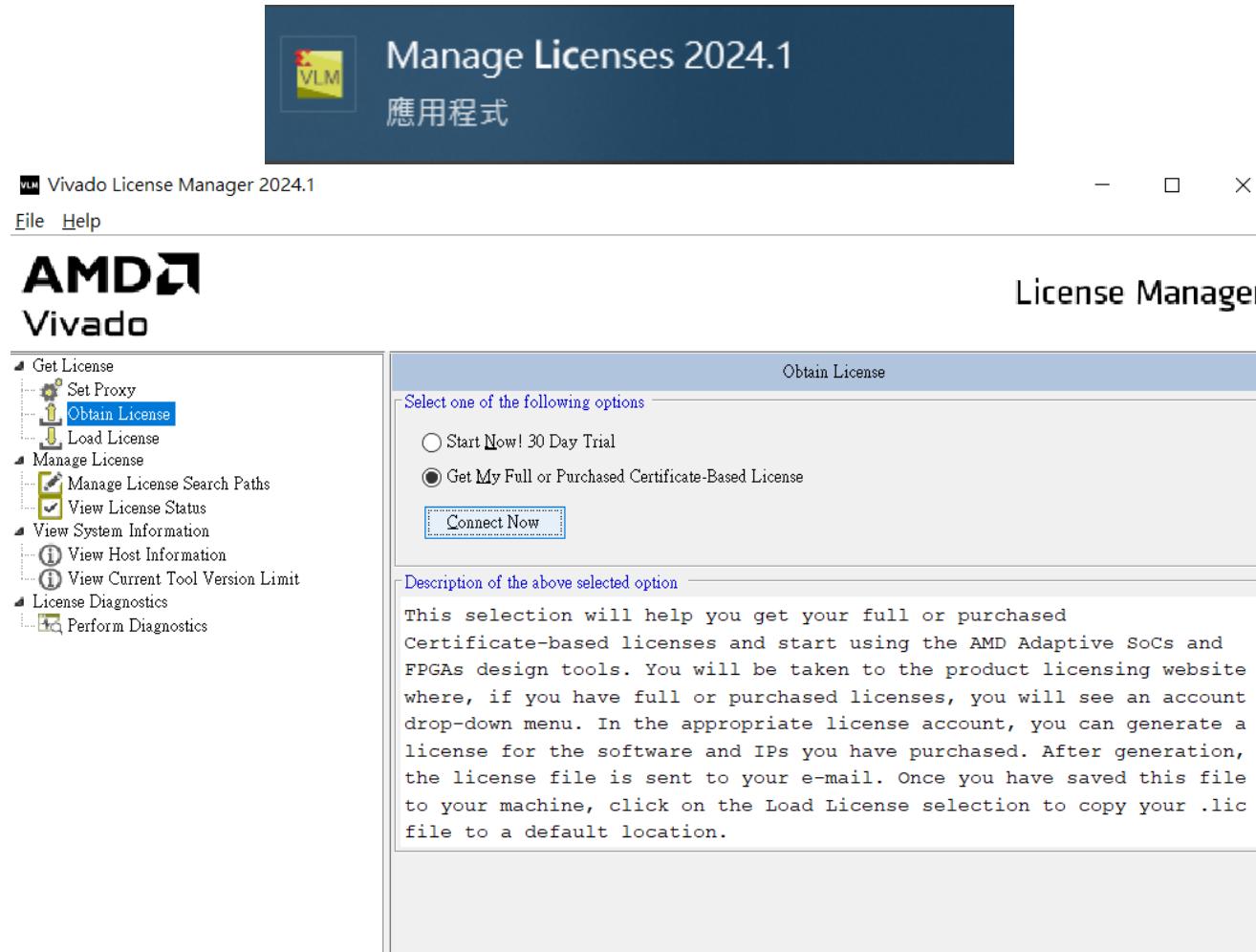




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Setting license

- Search “Manage Licenses” in your computer:





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Setting license

Vivado License Manager 2024.1

File Help

AMD Vivado

License Manager

1. **Obtain License**

2. **Get My Full or Purchased Certificate-Based License**

3. **Connect Now**

Obtain License

Select one of the following options

Start Now! 30 Day Trial

Get My Full or Purchased Certificate-Based License

Connect Now

Description of the above selected option

This selection will help you get your full or purchased Certificate-based licenses and start using the AMD Adaptive SoCs and FPGAs design tools. You will be taken to the product licensing website where, if you have full or purchased licenses, you will see an account drop-down menu. In the appropriate license account, you can generate a license for the software and IPs you have purchased. After generation, the license file is sent to your e-mail. Once you have saved this file to your machine, click on the Load License selection to copy your .lic file to a default location.

The screenshot shows the Vivado License Manager interface. On the left, there's a sidebar with various options like 'Get License', 'Set Proxy', 'Obtain License' (which is highlighted with a red box), 'Load License', 'Manage License', etc. The main area is titled 'License Manager' and has a sub-section 'Obtain License'. It asks to 'Select one of the following options' with two radio buttons: 'Start Now! 30 Day Trial' and 'Get My Full or Purchased Certificate-Based License'. The second option is selected and highlighted with a red box. Below it is a 'Connect Now' button, also highlighted with a red box. A descriptive text explains the process of getting a certificate-based license, mentioning the product licensing website and the generation of a license file via email.



Setting license



1. login 登入

電子郵件地址
r12k41004@ntu.edu.tw

密碼

登入

或

創建密碼

忘記/重設密碼？

幫助 使用條款 隱私權

Product Licensing - Name and Address Verification

U.S. Government Export Approval

2. fill out the form

- U.S. export regulations require that your First Name, Last Name, Company Name and Shipping Address be verified before AMD can fulfill your download request. [Please provide accurate and complete information.](#)

- Addresses with Post Office Boxes and names/addresses with Non-Roman Characters with accents such as grave, tilde or colon [are not supported](#) by US export compliance systems.

E-mail *

r12k41004@ntu.edu.tw

Company Name *

National Taiwan University

Address 1 *

No.1, Sec. 4, Roosevelt Road

Address 2

Location *

Taiwan

State/Province

NTU MicroSystem Research Lab. 21



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Setting license

- If you can't find the WebPACK license, check the "Manage Licenses" tab to see if you have generated it before.

Create a New License File

Create a new license file by making your product selections from the table below. ?

Certificate Based Licenses

Product	Type	License	Available Seats	Status	Subscription End Date
<input type="checkbox"/> SDSoc Environment, 60 Day Evaluation License	Certificate - Evaluation	Node	1/1	Current	60 days
<input type="checkbox"/> Model Composer : 90-day Evaluation License	Certificate - Evaluation	Node	1/1	Current	90 days
<input type="checkbox"/> Vivado Design Suite (No ISE): 30-Day Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days
<input checked="" type="checkbox"/> Vivado Design Suite: HL WebPACK 2015 and Earlier License	Certificate - No Charge	Node	1/1	Current	None
<input type="checkbox"/> PetaLinux Tools License	Certificate - Evaluation	Node	1/1	Current	365 days
<input type="checkbox"/> Vivado HLS Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days

Next Next Next Next



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Setting license

Generate Node License

Fields marked with an asterisk * are required.

1 PRODUCT SELECTION

Product Selections	Product	Type	Available Seats	Subscription End Date	Requested Seats	Borrowed Seats
*	<input checked="" type="checkbox"/> Vivado Design Suit...	No Charge	1/1	None	1	

2 SYSTEM INFORMATION

License	Node
Host ID *	Any

3 COMMENTS

Comments ?

[Next](#) [Cancel](#)

Generate Node License

4 REVIEW LICENSE REQUEST

Product Selections

Product	Subscription End Date	Available Seats	Requested Seats
Vivado Design Suite: HL WebPACK 2015 and E...	1/1	1	

System Information

License	Node
Host ID	ANY

Note: WebTalk is always enabled for WebPACK users. WebTalk ignores user and install preference when a bitstream is generated using the WebPACK license. If a design is using a device contained in WebPACK and a WebPACK license is available, the WebPACK license will always be used. To get additional information on WebTalk, go to www.xilinx.com/webtalk.

[Previous](#) [Next](#) [Cancel](#)



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Setting license

Congratulations

Your new license file has been successfully generated and e-mailed to wendyfang1028@gmail.com. You can also view the license file under the Manage Licenses tab.

Please add this sender (xilinx.notification@entitlenow.com) to your address book.

License File Details

Node License
Host ID: ANY

Go to e-mail to get license

Products

Vivado Design Suite: HL WebPACK 2015 and Earlier License (No Charge): 1 seats



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Setting license

- Download the .lic file in the mail.

Xilinx, Inc. – Certificate Based License File for Your Design Tool or IP Core Product

 Xilinx.lic (~1 KB) ▾

Dear

Thank you for licensing your Xilinx design tool or IP core product. This email includes the certificate license file to enable your product.

The license file can also be obtained by returning to the Xilinx Product Licensing Site: <https://account.amd.com/en/forms/license/license-form.html>

For complete instructions on installing this license file, see the Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973) document on the Xilinx website.

Quick-Start License Installation Instructions

Node-locked License Installation Instructions

These steps will copy your license file to the appropriate default directory (under %APPDATA%\\XilinxLicense for Windows and .Xilinx under \$HOME for Linux).

1. Save the attached license file (.lic) to your desktop or some other folder on your computer
2. Run the Vivado License Manager (For Windows: Run | Manage Xilinx Licenses, from underneath your Version group of the Xilinx Design Tools program group, For Linux: Type "vlm" in a command-line window)

Windows: Run 'Manage Xilinx Licenses' from underneath your Version group of the Xilinx Design Tools program group

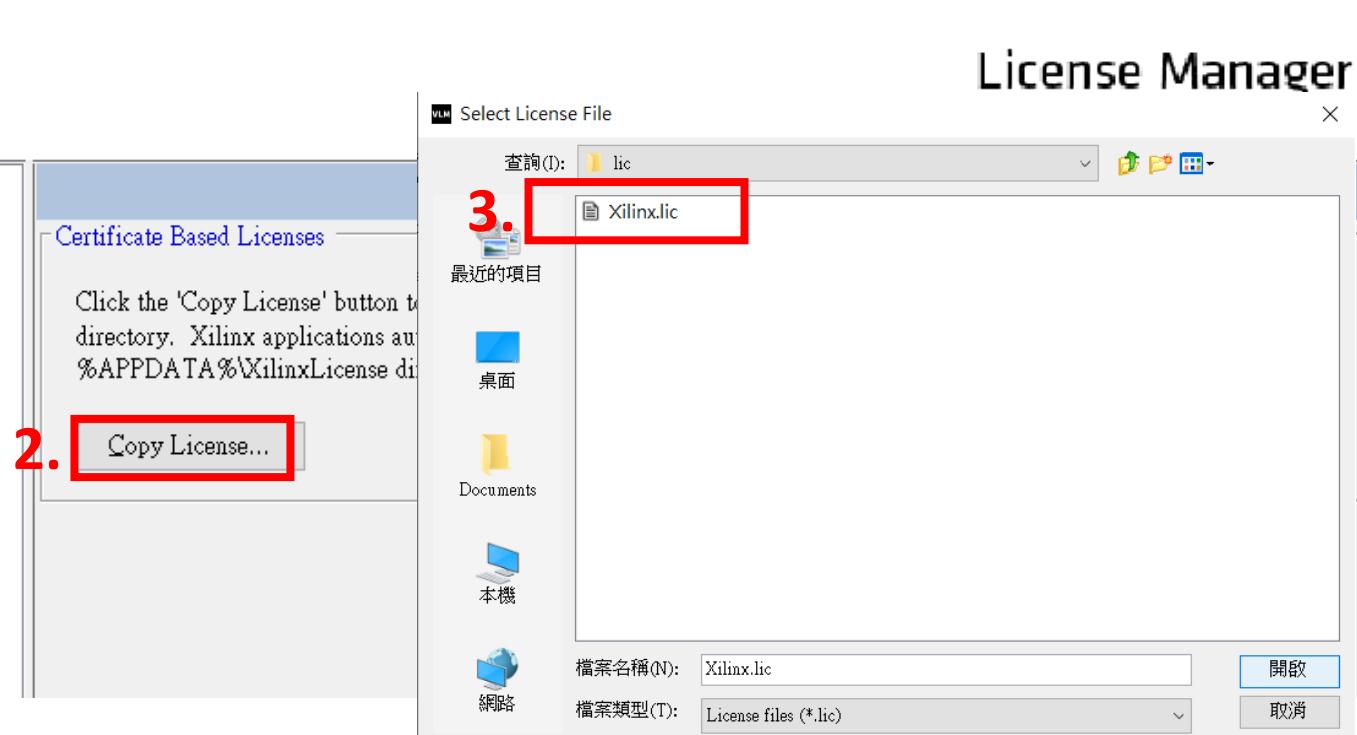
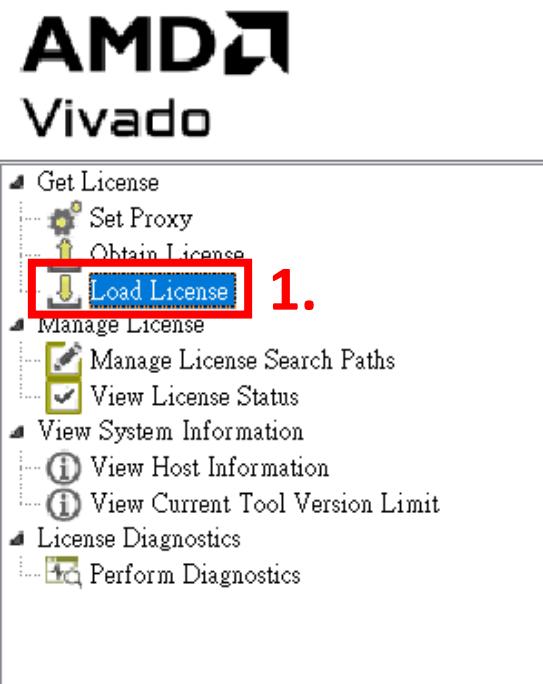
Linux: Select the "Load License" screen and click on the "Copy License" button.



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Setting license

- Go back to the License Manager and load the downloaded file.





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Setting license

- Go to “View License Status” and check if it is loaded properly.

The screenshot shows the Vivado software interface. On the left, there is a navigation menu with various options like 'Get License', 'Set Proxy', 'Obtain License', 'Load License', 'Manage License', 'Manage License Search Paths' (which is selected), 'View System Information', 'View Host Information', 'View Current Tool Version Limit', 'License Diagnostics', and 'Perform Diagnostics'. The main window is titled 'View License Status' and displays a table of 'Certificate Based Licenses'. The table has columns for License Name, Tools/IP, Expiration Date, Version Limit, License Type, Location, # of Seats, # of Seats Used, Host ID in Licens..., Host IDs Match, License CRC, and Search Order. There are five entries in the table:

License Name	Tools/IP	Expiration Date	Version Limit	License Type	Location	# of Seats	# of Seats Used	Host ID in Licens...	Host IDs Match	License CRC	Search Order
Analyzer	Tools	Permanent	2025.11	Nodelocked	C:\Users\leeso\AppData\...\\	Uncounted	Not Applicable	ANY	Yes	Okay	1
HLS	Tools	Permanent	2025.11	Nodelocked	C:\Users\leeso\AppData\...\\	Uncounted	Not Applicable	ANY	Yes	Okay	2
SDK	Tools	Permanent	2025.11	Nodelocked	C:\Users\leeso\AppData\...\\	Uncounted	Not Applicable	ANY	Yes	Okay	3
V_WebPACK	Tools	Permanent	2025.11	Nodelocked	C:\Users\leeso\AppData\...\\	Uncounted	Not Applicable	ANY	Yes	Okay	4

- You can launch Vivado now.





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Create project and run Synthesis

The image shows the Vivado 2024.1 software interface. At the top left is the NTU logo. The main title "Create a New Project" is displayed prominently in blue. The interface includes a navigation bar with "File", "Flow", "Tools", "Window", "Help", and a "Quick Access" search bar. The central area is divided into three main sections: "Quick Start" (dark teal background), "Tasks" (light blue background), and "Learning Center" (light blue background). The "Quick Start" section features links for "Create Project >" (highlighted with a red box), "Open Project >", and "Open Example Project >". The "Tasks" section includes "Manage IP >", "Open Hardware Manager >", and "Vivado Store >". The "Learning Center" section includes "Documentation and Tutorials >", "Quick Take Videos >", and "What's New in 2024.1 >". On the right side, there is a "Recent Projects" sidebar listing "project_1" with the path "D:/xilinx_data/project_1".

Create a New Project

Vivado 2024.1

File Flow Tools Window Help Q: Quick Access

AMD Vivado ML Edition

Quick Start

Create Project > (highlighted)

Open Project >

Open Example Project >

Tasks

Manage IP >

Open Hardware Manager >

Vivado Store >

Learning Center

Documentation and Tutorials >

Quick Take Videos >

What's New in 2024.1 >

Recent Projects

project_1
D:/xilinx_data/project_1



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Create a New Project

- Enter the project name

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: X

Project location: X ...

Create project subdirectory

Project will be created at: D:/xilinx_data/test_project

?

< Back

Next >

Finish

Cancel

Lab. 30



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Create a New Project

New Project X

Project Type
Specify the type of project to create.

RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis
 Do not specify sources at this time
 Project is an extensible Vitis platform

Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify Project File.

Example Project
Create a new Vivado project from a predefined template.

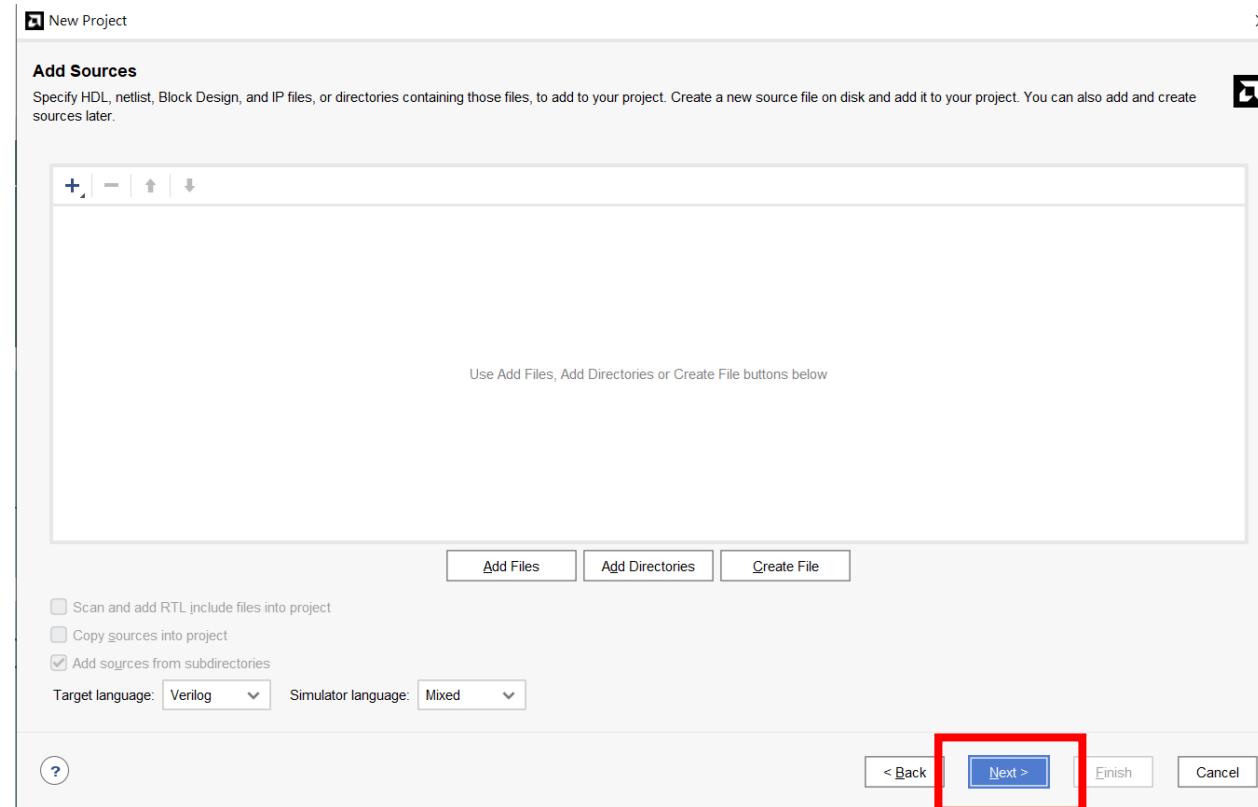
? < Back Next > Finish Cancel

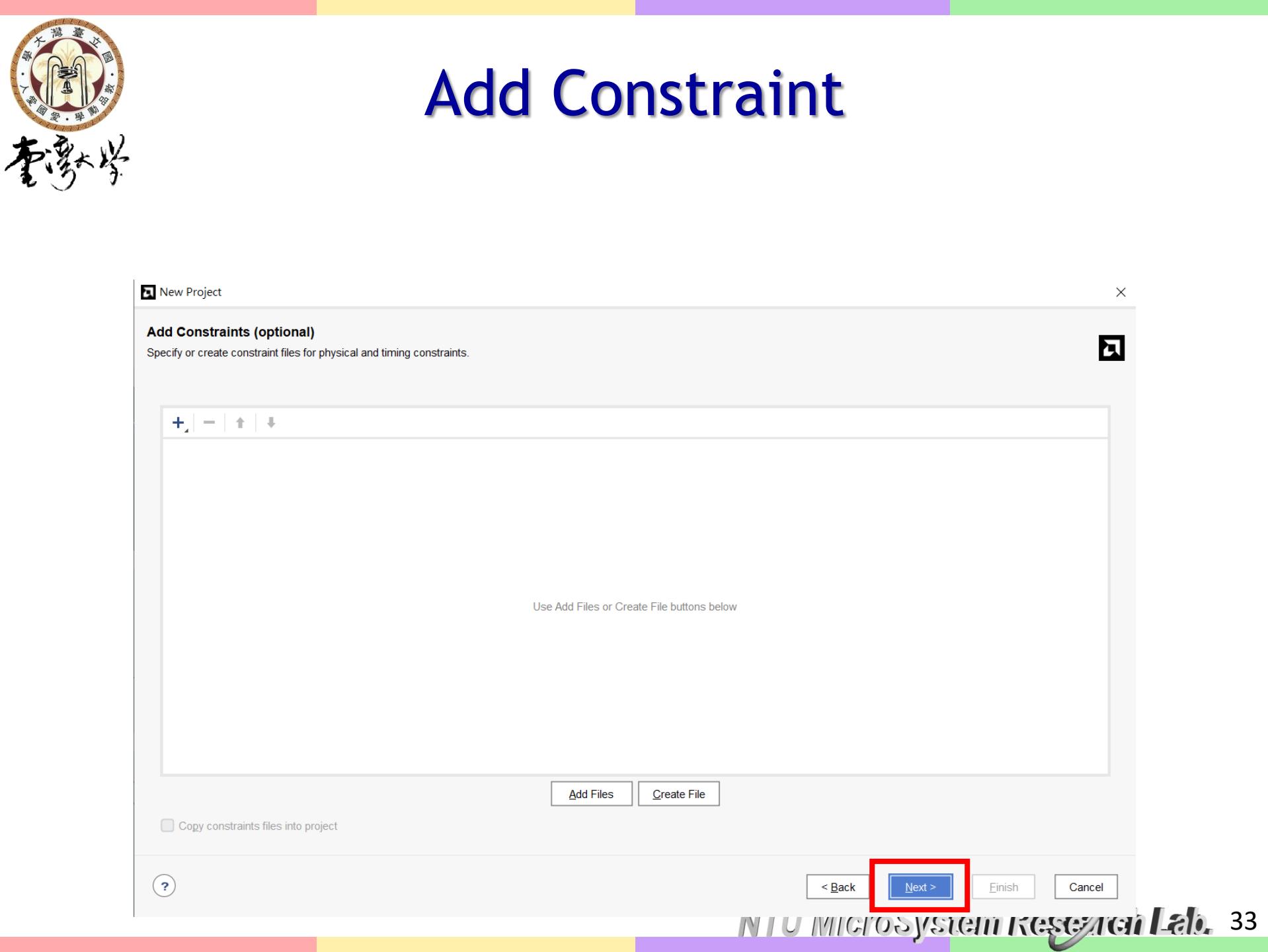
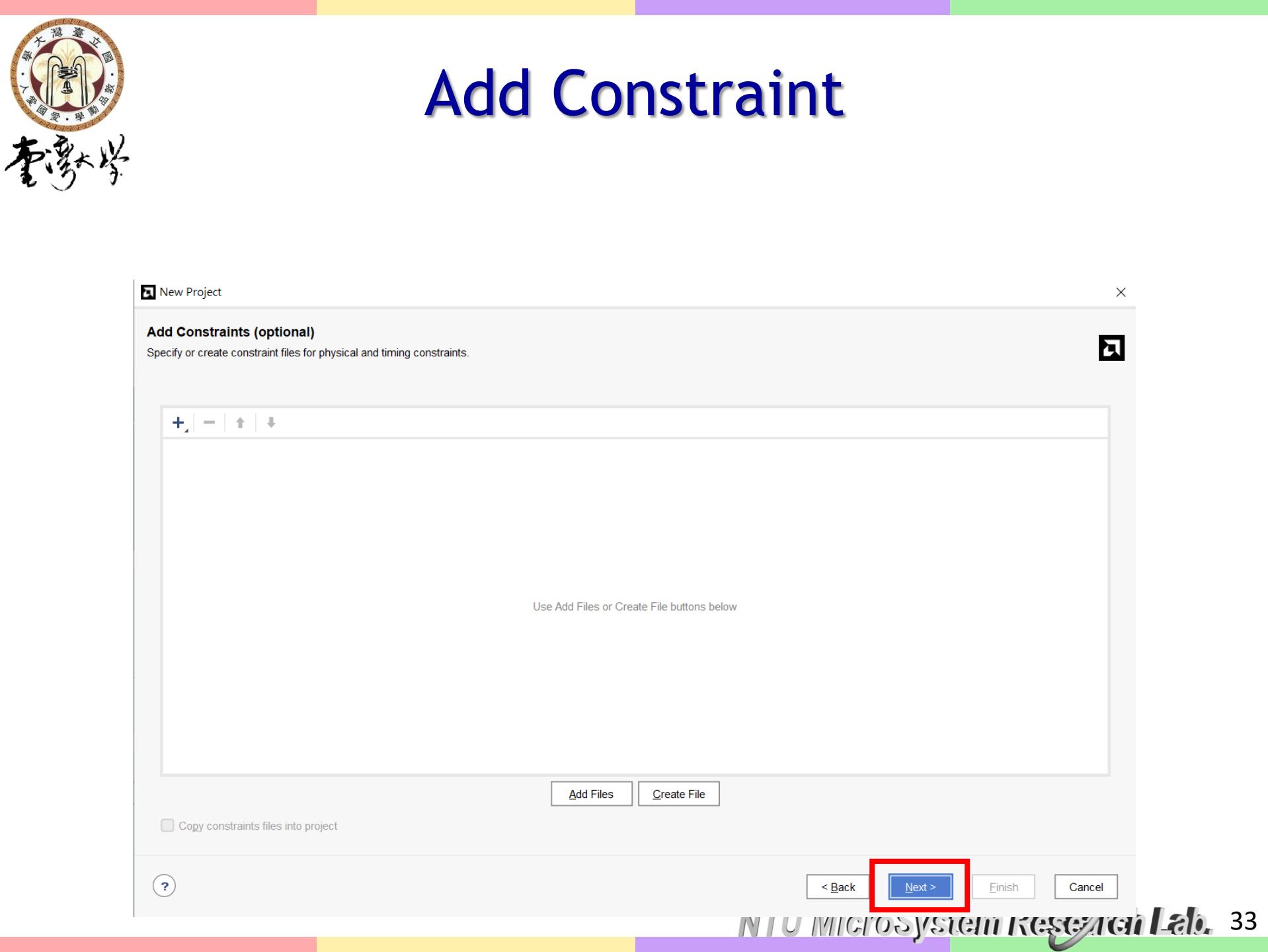


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Add Sources

- If you have prepared .v files for the design, you can add them with the “+” button.
- We will create the file later.







Choose Part

- Search for “xc7a200tfg676-1”

1.

2.

3.

New Project

Default Part

Choose a default AMD part or board for your project.

Parts | Boards

Reset All Filters

Category: All

Family: All

Package: All

Speed: All

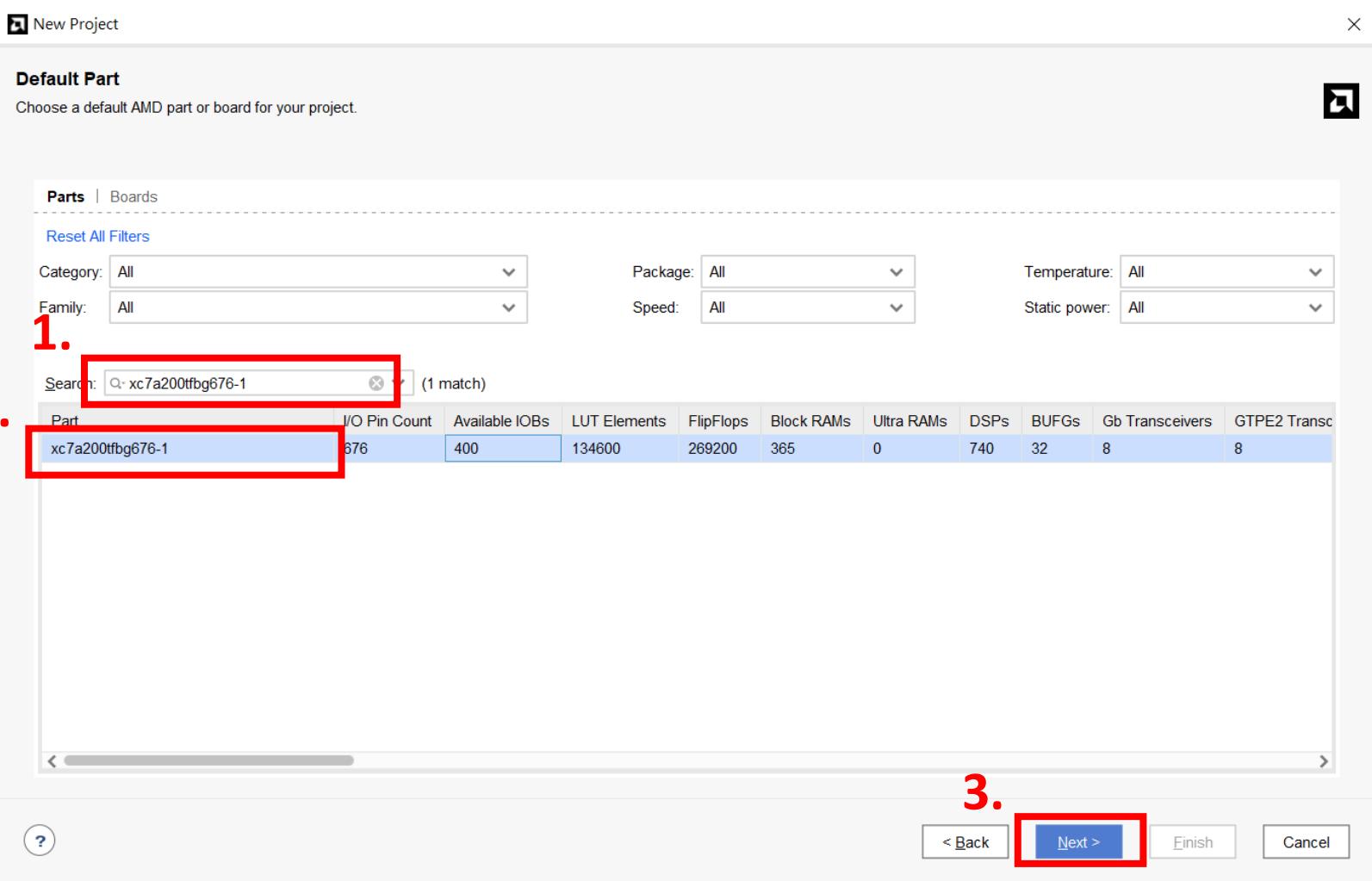
Temperature: All

Static power: All

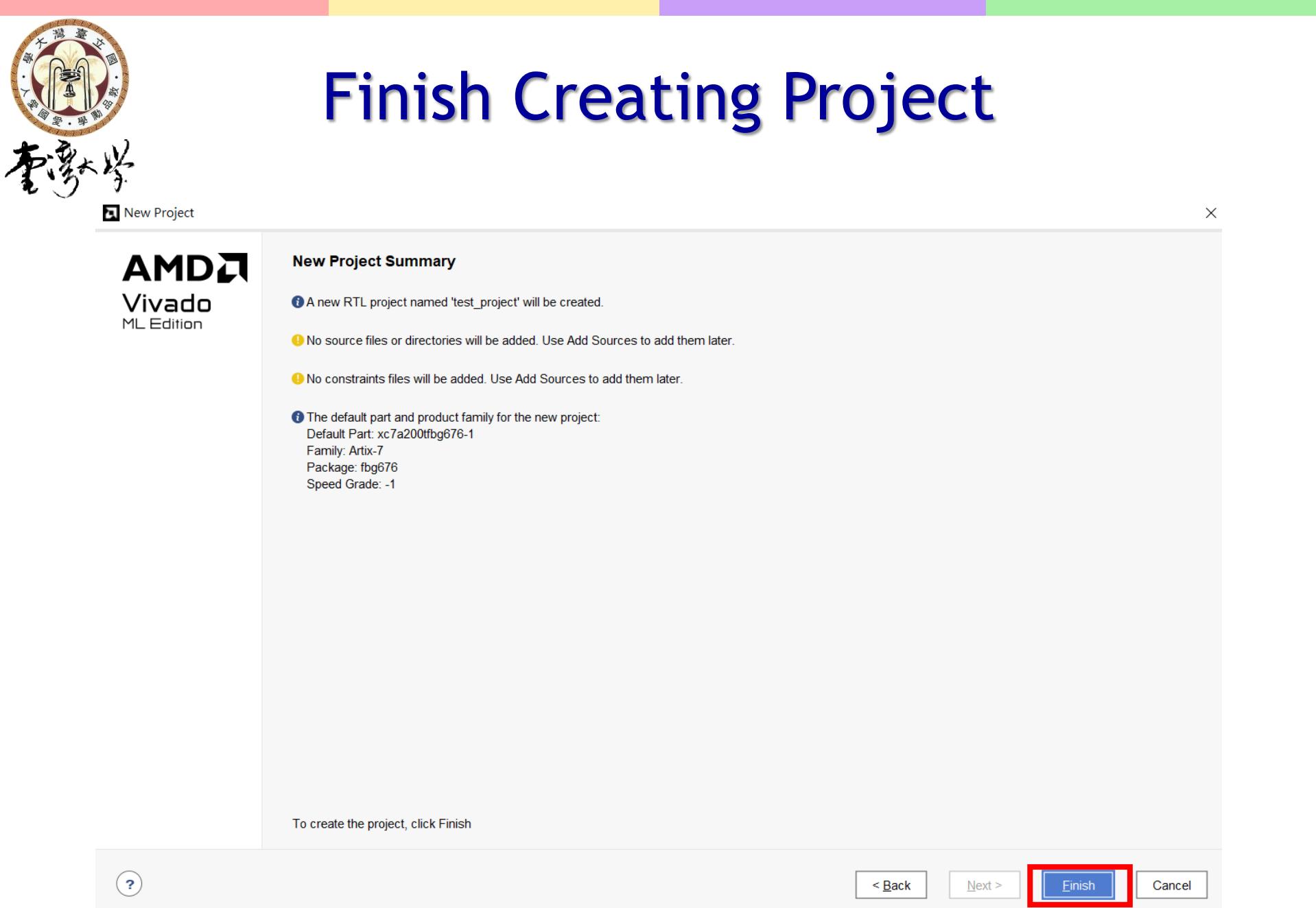
Search: xc7a200tfg676-1 (1 match)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	BUFGs	Gb Transceivers	GTPE2 Transc
xc7a200tfg676-1	676	400	134600	269200	365	0	740	32	8	8

< Back Next > Finish Cancel



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The image shows a screenshot of the AMD Vivado ML Edition software interface. At the top, there is a banner with the text "Finish Creating Project". On the left side, there is a circular logo for National Taiwan University (NTU) and a stylized "NTU" logo. Below the banner, there is a "New Project" button and a close "X" button. The main content area is titled "New Project Summary" and contains the following information:

A new RTL project named 'test_project' will be created.

No source files or directories will be added. Use Add Sources to add them later.

No constraints files will be added. Use Add Sources to add them later.

The default part and product family for the new project:
Default Part: xc7a200tbg676-1
Family: Artix-7
Package: fbg676
Speed Grade: -1

To create the project, click Finish

At the bottom, there are several buttons: a question mark icon, "Back", "Next >", "Finish" (which is highlighted with a red border), and "Cancel".

Add Source File

The screenshot shows the Vivado 2024.1 interface with the 'PROJECT MANAGER - test_project' open. The 'Sources' tab is selected in the top-left corner. A red box labeled '1.' highlights the '+' icon in the toolbar. A modal window titled 'Add Sources' is displayed, with a red box labeled '2.' highlighting the radio button for 'Add or create design sources'. Another red box labeled '3.' highlights the 'Next >' button at the bottom right of the modal.

1. +

2. Add or create design sources

3. Next >



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Add Source File

1.

2.

3.

Add or Create Design Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project.

+ | - | ↑ | ↓

Use Add Files, Add Directories or Create File buttons

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Add Files Add Directories **Create File**

< Back Next > **Finish** Cancel



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Add Source File

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: testdesign

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
input	input	<input type="checkbox"/>	0	0

?

OK Cancel



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Add Source File

- You can find the testdesign.v under “Sources” tab.
- Double click to open it.





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Add Source File

- Write a sample design...

The screenshot shows a Verilog code editor window titled "testdesign.v". The code is a testbench for a multiplication operation. It includes declarations for output C [9:0], inputs clk and rst, and internal reg variables a_w, a_r, b_w, and b_r. The code uses an always block to calculate the result C = a_r * b_r. It also includes logic to initialize a_r and b_r to 0 when rst is asserted. The code editor interface includes tabs for "Project Summary" and "testdesign.v", a toolbar with various icons, and a status bar at the bottom.

```
26     output [9:0] C;
27     input clk, rst;
28     reg [4:0] a_w, a_r, b_w, b_r;
29
30     assign C = a_r * b_r;
31     always @(*) begin
32         a_w = A<<1;
33         b_w = B<<1;
34     end
35     always @ (posedge clk or posedge rst) begin
36         if (rst) begin
37             a_r <= 0;
38             b_r <= 0;
39         end else begin
40             a_r <= a_w;
41             b_r <= b_w;
42         end
43     end
44
45 endmodule
46
```



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Testbench

The screenshot shows the Vivado ML Edition interface. On the left, the 'Sources' tab is selected, displaying a tree view of project files. A red box labeled '1.' highlights the '+' button in the toolbar above the tree view. The tree view shows:

- > Design Sources (1) [Add Sources \(Alt+A\)](#)
- > Constraints
- < Simulation Sources (1)
 - < sim_1 (1)
 - testdesign** (testdesign.v)
- > Utility Sources

Below the tree view are tabs for 'Hierarchy', 'Libraries', and 'Compile Order'. A red box labeled '2.' highlights the 'Add or create simulation sources' radio button in the 'Add Sources' dialog. The dialog also includes:

- Add or create constraints
- Add or create design sources
- Add or create simulation sources

A red box labeled '3.' highlights the 'Next >' button at the bottom right of the dialog.



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Testbench

- Same as creating design file.

The screenshot shows a CAD software interface with two open dialogs:

- Main Dialog: Add or Create Simulation Sources**
 - Specify simulation set: sim_1
 - Add Files, Add Directories, Create File buttons (the Create File button is highlighted with a red box).
 - Checkboxes at the bottom:
 - Scan and add RTL include files into project
 - Copy sources into project
 - Add sources from subdirectories
 - Include all design sources for simulation
 - < Back, Next >, Finish, Cancel buttons at the bottom.
- Sub-DIALOG: Create Source File**
 - Create a new source file and add it to your project.
 - File type: Verilog (radio button selected)
 - File name: test_tb (highlighted with a red box)
 - File location: <Local to Project>
 - OK, Cancel buttons.



Testbench

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- Finish the testbench.

Project Summary x testdesign.v x test_tb.v *

D:/xilinx_data/project_1/project_1.srscs/sim_1/new/test_tb.v

Q | F | ← | → | X | D | B | X | //

25
26 reg [4:0] A, B;
27 wire [9:0] C;
28 reg clk;
29 reg rst;
30 testdesign uut(A, B, C, clk, rst);
31 initial begin
32 clk = 1'b0;
33 end
34 always begin #20; clk = ~clk; end
35 initial begin
36 rst = 1'b0;
37 #10; rst = 1'b1;
38 #40; rst = 1'b0;
39 end
40 initial begin
41 A = 0;
42 B = 5;
43 #40;
44 A = 5; B = 5;
45 #40.



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Behavioral Simulation

- Run Simulation->Run Behavioral Simulation

The screenshot shows the Vivado 2024.1 interface with the following details:

- PROJECT MANAGER - test_project**: Shows Sources (Design Sources, Constraints, Simulation Sources, Utility Sources), IP Catalog, IP INTEGRATOR, and various simulation and analysis options.
- Source File Properties - test_tb.v**: Displays the code:

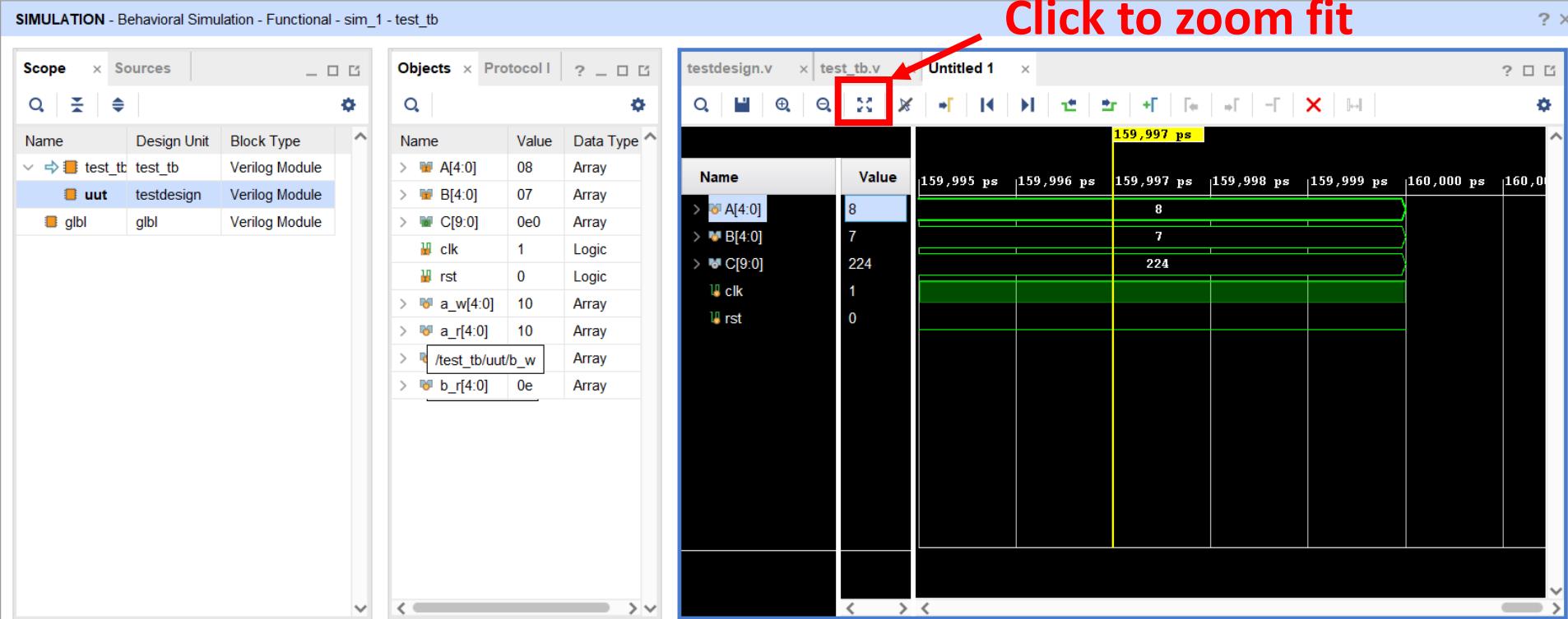
```
25 reg [4:0] A, B;
26 wire [9:0] C;
27 reg clk;
28 reg rst;
29 testdesign uut(A, B, C, clk, rst);
30 initial begin
31     clk = 1'b0;
32 end
33 always begin #20; clk = ~clk; end
34 initial begin
35     rst = 1'b0;
36     #10; rst = 1'b1;
37     #40; rst = 1'b0;
38 end
39 initial begin
40     A = 0;
41     B = 5;
42     #40;
43     A = 5; B = 5;
44     #40.
```
- Design Runs**: Shows a table with columns: Name, Constraints, Status, WNS, TNS, WHS, THS, WBSS, TPWS, Total Power, Failed Routes, Methodology, RQA Score, QoR Suggestions, LUT, FF, BRAM, URAM, DSP, Start, Elap. It lists synth_1 and impl_1 as Not started.



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Behavioral Simulation

- Then the simulation waveform is shown.
- If you use \$display in the testbench, it will show in the Tcl console.

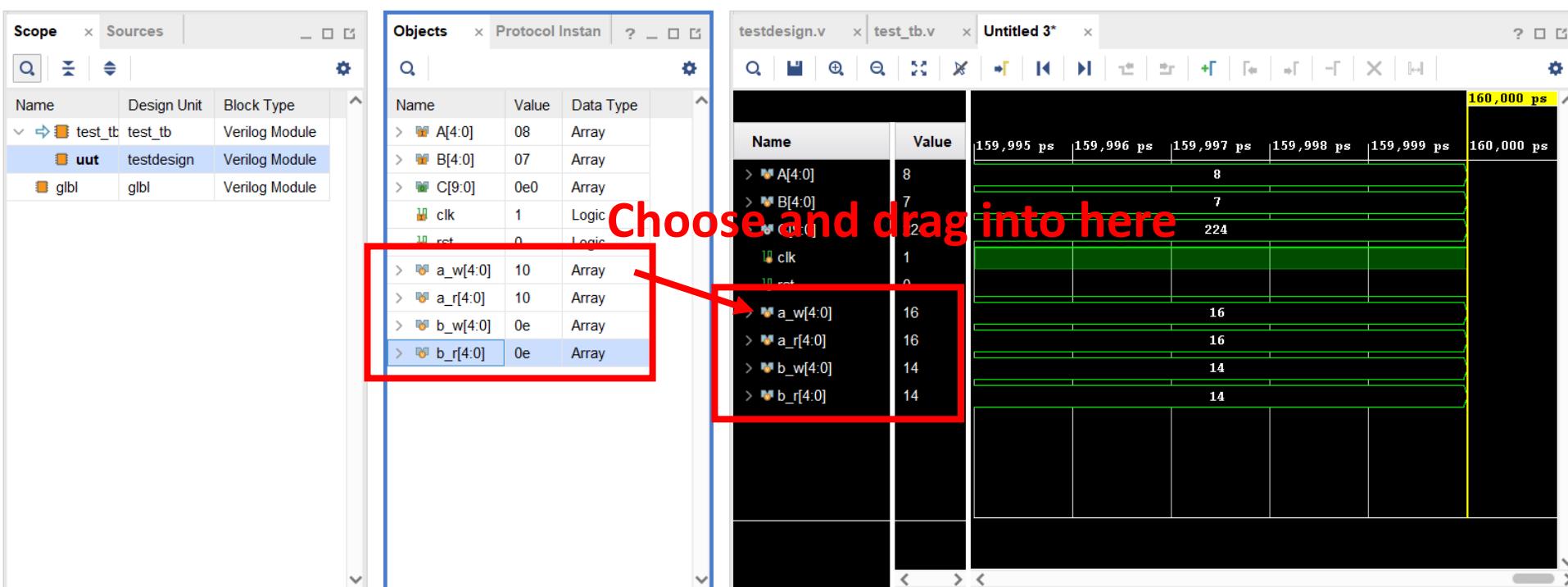




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Behavioral Simulation

- Choose the submodule in the left to see the waveform of wires under it.





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Behavioral Simulation

- If you can't see the waveform of wires under submodule, change the setting as follow, then rerun.

The screenshot shows the Vivado 2024.1 interface with several windows open:

- Project Manager:** The "PROJECT MANAGER" section is highlighted with a red box. Under "Settings", there is a "Scope" tab and a "Sources" tab. The "Sources" tab is currently active, showing a list of design units: test_tb, uut, and glbl.
- Settings - Project Settings:** A red box highlights the "Simulation" tab in the "Project Settings" window. Other tabs shown include General, Synthesis, Implementation, Bitstream, and IP.
- Settings - Simulation:** A red box highlights the "Simulation" tab in the "Settings" window. This window contains fields for Target simulator (Vivado Simulator), Simulator language (Mixed), Simulation set (sim_1), and Simulation top module name (test_tb). It also has checkboxes for "Generate simulation scripts only" and "Configure soc to run simulator in GUI mode".
- Waveform View:** On the right, a waveform viewer shows multiple signal traces. A red box highlights the time axis, which displays values 159,999 ps and 160,000 ps. The waveforms themselves are mostly black, indicating they are not visible.

Tcl Console: At the bottom left, the Tcl Console window shows command-line output related to simulation setup.



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Run Synthesis

The screenshot shows the Xilinx Vivado IDE interface. On the left, the Project Manager and Simulation sections are visible, with 'Run Synthesis' highlighted. A red arrow points from this highlighted item to the 'Launch Runs' dialog box in the center. The dialog box has the title 'Launch Runs' and the sub-instruction 'Launch the selected synthesis or implementation runs.' It contains an 'Options' section with two radio button options: 'Launch runs on local host: Number of jobs' set to 8, and 'Generate scripts only'. Below these is a checkbox for 'Don't show this dialog again'. At the bottom are 'OK' and 'Cancel' buttons, with 'OK' also highlighted by a red box. In the background, the 'SIMULATION - Behavioral Simulation - Functional - sim_1 - test_tb' window is open, showing a scope and some code in the editor.

More = Faster
(base on your CPU core #)

- Wait until the “Running synth_design” on topleft finish.

Running synth_design [Cancel](#)



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Run Synthesis

Synthesis Completed X



Synthesis successfully completed.

Next

[Run Implementation](#)

[Open Synthesized Design](#)

[View Reports](#)

[Don't show this dialog again](#)

OK

Cancel



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1. **Edit Timing Constraints** (highlighted with a red box)

2. **Create Clock (0)** (highlighted with a red box)

3. **+ Create Clock** (highlighted with a red box)

The screenshot shows the Vivado 2024.1 interface with the "SYNTHESIZED DESIGN - xc7a200tfgb676-1" project open. The "Edit Timing Constraints" option under "SYNTHESIS" is highlighted. The "Timing Constraints" dialog is displayed, showing the "Create Clock" constraint. The "Create Clock (0)" button and the "+ Create Clock" button are both highlighted with red boxes.



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Specify Clock Source Objects

Specify the ports, pins, or nets which are the source of the specified clock.

Find names of type: I/O Port

Options

NAME contains *

AND DIRECTION is IN

Regular expression Ignore case

Of Objects:

1. Find

Results

Found: 12 Selected: 0

B[0]
B[1]
B[2]
B[3]
B[4]
clk
rst

2. clk

3. Move selected

4. Append

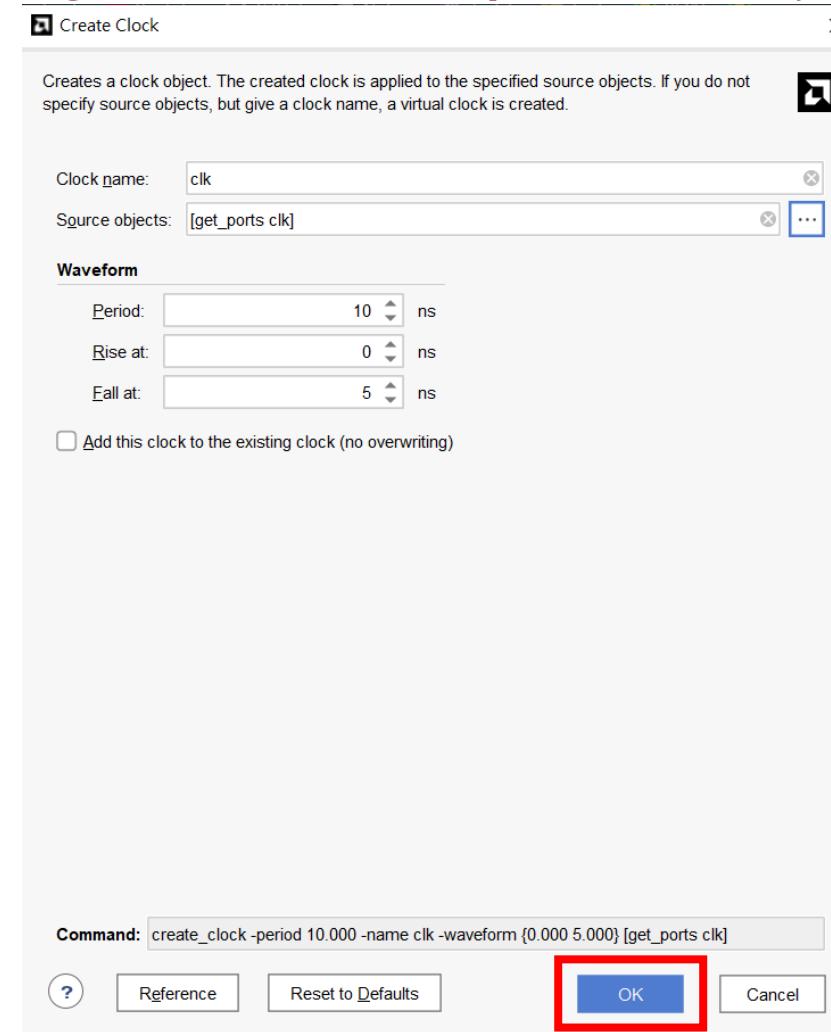
Command: Set Append Cancel

Enumerate



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- You can change the clock period if you want.





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Timing Constraints

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	clk	10.000	0.000	5.000	<input checked="" type="checkbox"/>	[get_ports clk]	<unsaved co		

Double click to create a Create Clock constraint

1.

All Constraints

Position	Command	Scoped Cell
<unsaved constraints>	1 create_clock -period 10.000 -name clk -waveform {0.000 5.000} -add [get_ports clk]	

2.

Apply Cancel

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Set Input Delay

1. Double click **Set Input Delay (0)** in the Timing Constraints panel.

2. Set the **Delay value** to 0 ns.

The screenshot shows the 'Set Input Delay' dialog box open in a software interface. The 'Timing Constraints' panel on the left is visible, showing a list of constraints including 'Create Clock', 'Set Input Delay (0)', and 'Set Output Delay (0)'. A red box highlights the 'Set Input Delay (0)' item under the 'Inputs' section. The 'Set Input Delay' dialog box has a red box around its 'Delay value' input field, which contains '0 ns'. The 'Command' field at the bottom of the dialog box contains the text 'set_input_delay 0.0'. The number '2.' is written above the dialog box.



Set Input Delay

Edit Set Input Delay

Specify input delay for ports or pins relative to a clock edge.

Clock: [get_clocks *]

Objects (ports): [get_ports [list A[0] A[1] A[2] A[3] A[4] B[0] B[1] B[2] B[3] B[4] rst]]

Delay value: 5 ns

Delay Value Options

Delay value is relative to clock edge: rise

Delay value already includes latencies of the specified clock: None

Rise/Fall

Delay value specifies rising delay

Min/Max

Delay value specifies min delay (shortest path)

Add delay information to the existing delay (no overwrite)

Command: _clocks * -add_delay 5.0 [get_ports [list A[0] A[1] A[2] A[3] A[4] B[0] B[1] B[2] B[3] B[4] rst]]

Reference Reset to Defaults OK Cancel

Specify Delay Objects

Specify the list of ports to which the delay value will be assigned.

Find names of type: I/O Port

Options

NAME contains *
AND DIRECTION is IN

Regular expression Ignore case

Of Objects:

Results

Found: 1 Selected: 11

clk → A[4]
→ B[0]
→ B[1]
→ B[2]
→ B[3]
→ B[4]
rst

Command: get_ports [list A[0] A[1] A[2] A[3] A[4] B[0] B[1] B[2] B[3] B[4] rst]

Reference Append Set Cancel

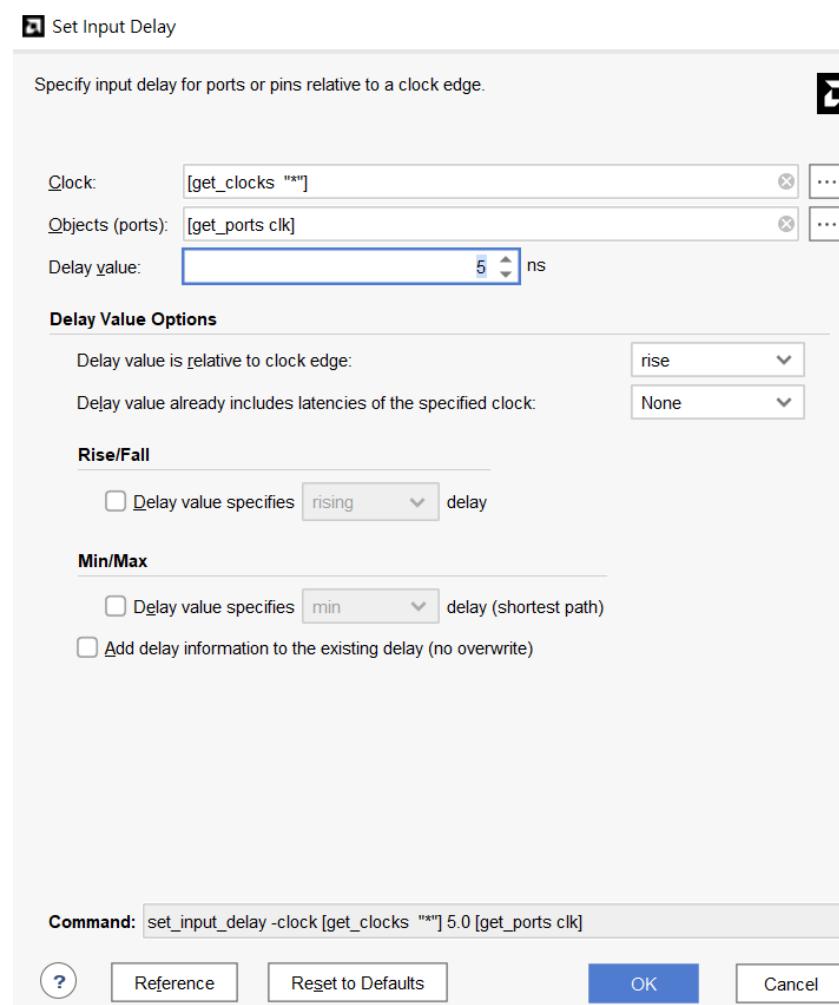
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Set Input Delay

- We set the delay value as half of the cycle time here.





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Set Output Delay

Timing Constraints

Set Input Delay

Position	Clock	Clock Edge	Delay Transition	Min/Max Delay Path	Add Delay	Latencies Included	Delay Value	Objects	Source File	Scoped
2	[get_clocks	rise			<input checked="" type="checkbox"/>	None	5.000	[get_ports clk]	<unsaved co	

Double click to create a Set Input Delay constraint

1.

Clocks (1)

- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (1)

- Set Input Delay (1)

Outputs (0)

- Set Output Delay (0)

All Constraints

Position Command Scoped Cell

<unsaved constraints>

1	create_clock -period 10.000 -name clk -waveform {0.000 5.000} -add [get_ports clk]
2	set_input_delay -clock [get_clocks *] -add_delay 5.0 [get_ports clk]

2.

Apply Cancel

The screenshot shows the Xilinx Vivado Timing Constraints window. In the 'Set Input Delay' section, a row is selected with a red box around the 'Add Delay' column, which contains a checked checkbox. In the 'All Constraints' section, a red box highlights the 'Apply' button at the bottom of the dialog. The 'Set Input Delay' command is also visible in the 'All Constraints' list.



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Set Output Delay

Edit Set Output Delay

Specify output delay for ports or pins relative to a clock edge.

Clock: `[get_clocks *]`

Objects (ports): `[get_ports -filter { NAME =~ "*" & DIRECTION == "OUT" }]`

Delay value: `1 ns`

Delay Value Options

Delay value is relative to clock edge: `rise`

Delay value already includes latencies of the specified clock: `None`

Rise/Fall

Delay value specifies `rising` delay

Min/Max

Delay value specifies `min` delay (shortest path)

Add delay information to the existing delay (no overwrite)

Command: `c [get_clocks *] -add_delay 1.0 [get_ports -filter { NAME =~ "*" & DIRECTION == "OUT" }]`

Reference Reset to Defaults OK Cancel

Specify Delay Objects

Specify the list of ports to which the delay value will be assigned.

Find names of type: I/O Port

Options

NAME contains *

AND DIRECTION is OUT

Regular expression Ignore case

Of Objects: Find

Results

Found: 10 Selected: 0

C[0]
C[1]
C[2]
C[3]
C[4]
C[5]
C[6]

Use the buttons on the left to move items to this list.

Command: Set Append Cancel



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Set Output Delay

Timing Constraints *

Set Input Delay (1)
Outputs (1)
Set Output Delay (1)
Assertions (0)
Set Data Check (0)
Set Bus Skew (0)
Exceptions (0)
Set False Path (0)
Set Multicycle Path (0)
Set Maximum Delay (0)
Set Minimum Delay (0)
Others (0)
Set Case Analysis (0)
Group Path (0)
Set Disable Timing (0)

1.

Position	Clock	Clock Edge	Delay Transition	Min/Max Delay Path	Add Delay	Latencies Included	Delay Value	Objects
3	[get_clocks *]	rise			<input checked="" type="checkbox"/>	None	1.000	[get_ports -filter { NAME =~ "*" && DIRECTION == "OUT" }]

Double click to create a Set Output Delay constraint

All Constraints

Position	Command	Scoped Cell
1	create_clock -period 10.000 -name clk -waveform {0.000 5.000} -add [get_ports clk]	
2	set_input_delay -clock [get_clocks *] -add_delay 5.0 [get_ports {A[0]} {A[1]} {A[2]} {A[3]} {A[4]} {B[0]} {B[1]} {B[2]} {B[3]} {B[4]} rst]	
3	set_output_delay -clock [get_clocks *] -add_delay 1.0 [get_ports -filter { NAME =~ "*" && DIRECTION == "OUT" }]	

2.

Apply Cancel



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Apply Constraint

Timing Constraints

	Position	Clock	Clock Edge	Delay Transition	Min/Max Delay Path	Add Delay	Latencies Included	Delay Value	Objects	Source File	Scoped
3	[get_clocks]	rise				<input checked="" type="checkbox"/>	None	5.000	[get_ports -filter { NAME =~ ".*" }]	<unsaved co	

Double click to create a Set Output Delay constraint

Clocks (1)
Create Clock (1)
Create Generated Clock (0)
Rename Auto-Derived Clock (0)
Set Clock Latency (0)
Set Clock Uncertainty (0)
Set Clock Groups (0)
Set Clock Sense (0)
Set Input Jitter (0)
Set System Jitter (0)
Set External Delay (0)

Inputs (1)
Set Input Delay (1)

Outputs (1)
Set Output Delay (1)

All Constraints

Position	Command	Scoped Cell
1	create_clock -period 10.000 -name clk -waveform {0.000 5.000} -add [get_ports clk]	
2	set_input_delay -clock [get_clocks *] -add_delay 5.0 [get_ports {list A[0] A[1] A[2] A[3]}]	
3	set_output_delay -clock [get_clocks *] -add_delay 5.0 [get_ports -filter { NAME =~ ".*" }]	

Apply Cancel

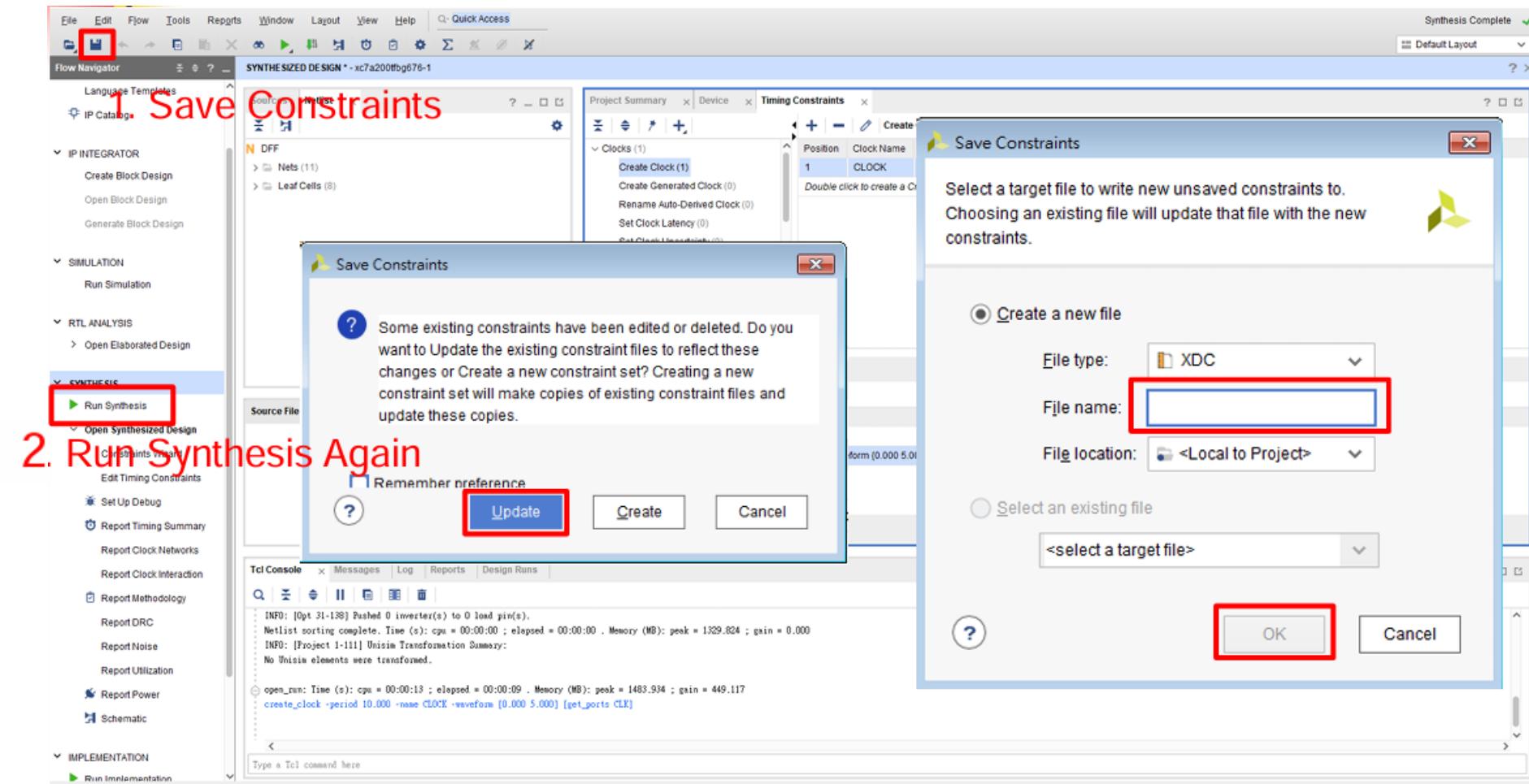


Apply Constraint

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1. Save Constraints

2. Run Synthesis Again



The screenshot shows the Xilinx Vivado interface. On the left, there's a sidebar with various synthesis and implementation options. The 'SYNTHESIS' section has 'Run Synthesis' highlighted with a red box. The top menu bar has a 'File' icon highlighted with a red box. In the center, there's a 'Save Constraints' dialog box with an 'Update' button highlighted with a red box. To the right of it is another 'Save Constraints' dialog box where the 'Create a new file' radio button is selected. The 'File type:' dropdown is set to 'XDC'. The 'File name:' input field is highlighted with a red box. Below it, the 'File location:' dropdown is set to '<Local to Project>'. At the bottom right of this dialog is an 'OK' button highlighted with a red box.

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The image shows the Vivado 2024.1 software interface with the following details:

- Title Bar:** Reports - [D:/xilinx_data/test_project/test_project.xpr] - Vivado 2024.1
- Menu Bar:** File, Edit, Flow, Tools, Reports, Window, Layout, View, Help
- Quick Access:** Synthesis Complete
- Flow Navigator:** SYNTHEZIS (highlighted), Create Block Design, Open Block Design, Generate Block Design, SIMULATION, Run Simulation, RTL ANALYSIS, Run Linter, Open Elaborated Design, SYNTHESIS, Run Synthesis, Open Synthesized Design, Constraints Wizard, Edit Timing Constraints, Set Up Debug, Open Dataflow Design, Report Timing Summary (highlighted with a red box), Report Clock Networks, Report Clock Interaction, Report Methodology (highlighted with a red box), Report DRC, Report Noise, Report Utilization, Report Power.
- SYNTHEZIS Panel:** Sources (test_design), Properties, Tcl Console.
- Report Timing Summary Dialog:** Title: Report Timing Summary. Subtitle: Generate a timing summary to understand if the design met timing. Results name: timing_1. Options tab selected. Path delay type: min_max. Report unconstrained paths (checked). Report datasheet (unchecked). Path Limits: Maximum number of paths per clock or path group: 10, Maximum number of worst paths per endpoint: 1. Path Display: Display paths with slack less than: (empty), Use default (1e+30) (checked). Significant digits: 3. Command: report_timing_summary -delay_type min_max -report_unconstrained -check_timing_verbose -max_paths 10 -input_pins -routeable_nets -name timing_1. Buttons: OK (highlighted with a red box), Cancel, ?.
- Right Panel:** Default Layout, showing a hierarchical tree structure of the design.

A red arrow points from the "Report Timing Summary" item in the Flow Navigator to the corresponding dialog window. A red box highlights the "Report Timing Summary" item in the Flow Navigator and the "OK" button in the dialog window.



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Report Timing

Tcl Console Messages Log Reports Design Runs **Timing** × ? _ □

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -0.326 ns	Worst Hold Slack (WHS): 3.602 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): -0.646 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWNS): 0.000 ns
Number of Failing Endpoints: 4	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 24	Total Number of Endpoints: 24	Total Number of Endpoints: 9

Click (Setup) Click (Hold)

Timing constraints are not met.

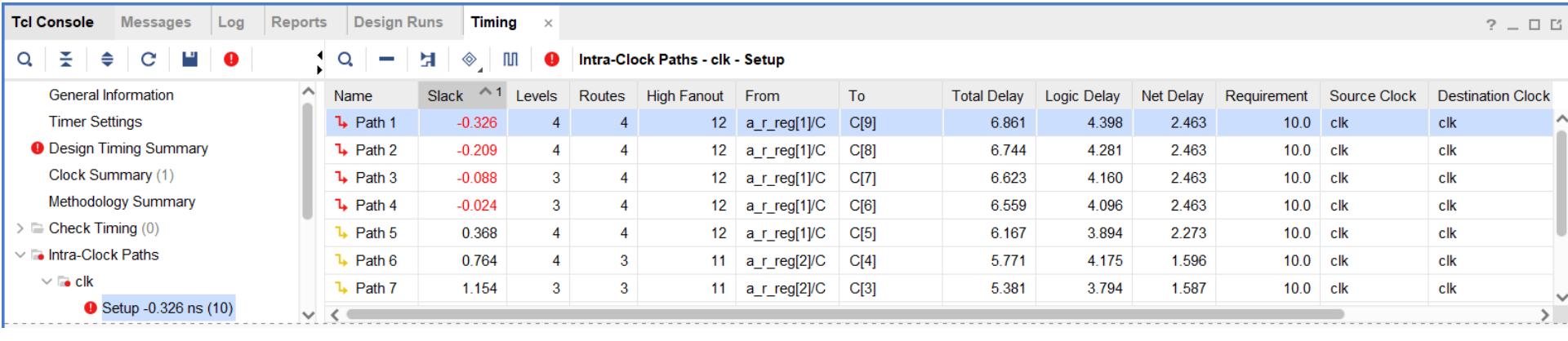
General Information
Timer Settings
① Design Timing Summary
Clock Summary (1)
Methodology Summary
Check Timing (0)
Intra-Clock Paths
clk
① Setup -0.326 ns (10)

Timing Summary - timing_1

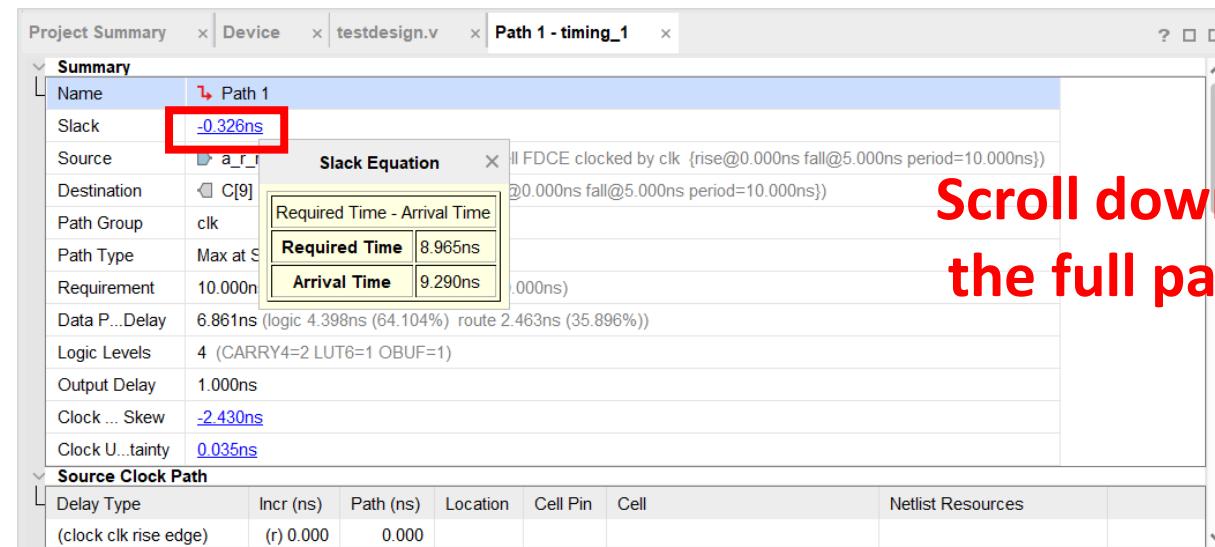
Report Timing

- Double click the path to see detail



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	-0.326	4	4	12	a_r_reg[1]/C	C[9]	6.861	4.398	2.463	10.0	clk	clk
Path 2	-0.209	4	4	12	a_r_reg[1]/C	C[8]	6.744	4.281	2.463	10.0	clk	clk
Path 3	-0.088	3	4	12	a_r_reg[1]/C	C[7]	6.623	4.160	2.463	10.0	clk	clk
Path 4	-0.024	3	4	12	a_r_reg[1]/C	C[6]	6.559	4.096	2.463	10.0	clk	clk
Path 5	0.368	4	4	12	a_r_reg[1]/C	C[5]	6.167	3.894	2.273	10.0	clk	clk
Path 6	0.764	4	3	11	a_r_reg[2]/C	C[4]	5.771	4.175	1.596	10.0	clk	clk
Path 7	1.154	3	3	11	a_r_reg[2]/C	C[3]	5.381	3.794	1.587	10.0	clk	clk

Scroll down to see
the full path info.



Name	Path 1
Slack	-0.326ns
Source	a_r_
Destination	C[9]
Path Group	clk
Path Type	Max at S
Requirement	10.000ns
Data P...Delay	6.861ns (logic 4.398ns (64.104%) route 2.463ns (35.896%))
Logic Levels	4 (CARRY4=2 LUT6=1 OBUF=1)
Output Delay	1.000ns
Clock ... Skew	-2.430ns
Clock U...tainty	0.035ns

Search Lab. 64



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- Try to fix the design and synthesize again:

Tcl Console Messages Log Reports Design Runs Timing ×

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Methodology Summary

> Check Timing (0)

✓ Intra-Clock Paths

 clk

Setup 2.491 ns (10)

Setup 2.491 ns (10)

Worst Negative Slack (WNS): 2.491 ns

Total Negative Slack (TNS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 40

Hold

Worst Hold Slack (WHS): 0.202 ns

Total Hold Slack (THS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 40

Pulse Width

Worst Pulse Width Slack (WPWS): 4.500 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 17

All user specified timing constraints are met.

Tcl Console Messages Log Reports Design Runs Timing ×

Intra-Clock Paths - clk - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	2.491	1	2	1	c_r_reg[2]/C	C[2]	4.044	3.244	0.800	10.0	clk	clk
Path 2	2.491	1	2	1	c_r_reg[3]/C	C[3]	4.044	3.244	0.800	10.0	clk	clk
Path 3	2.491	1	2	1	c_r_reg[4]/C	C[4]	4.044	3.244	0.800	10.0	clk	clk
Path 4	2.491	1	2	1	c_r_reg[5]/C	C[5]	4.044	3.244	0.800	10.0	clk	clk
Path 5	2.491	1	2	1	c_r_reg[6]/C	C[6]	4.044	3.244	0.800	10.0	clk	clk
Path 6	2.491	1	2	1	c_r_reg[7]/C	C[7]	4.044	3.244	0.800	10.0	clk	clk
Path 7	2.491	1	2	1	c_r_reg[8]/C	C[8]	4.044	3.244	0.800	10.0	clk	clk

Setup 2.491 ns (10)

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View Timing Info. for All Path

1. Schematic

2. Right click

3. Report Timing

Through Net...

Report Timing

Save as PDF File...

Export Schematic...

Net Delay Logic % Net % Requirement Source

0.800 80.2 19.8 10.000 clk
0.800 80.2 19.8 10.000 clk
0.800 80.2 19.8 10.000 clk
From Net... 19.8 10.000 clk
10 Net... 19.8 10.000 clk

SYNTHESIZED DESIGN - xc7a200ftfbg676-1

Project Summary Device testdesign.v test_tb.v Schematic

58 Cells 22 I/O Ports 87 Nets

Net Properties... Ctrl+E

Mark Debug

Unmark Debug

Assign to Debug Port...

Select Driver Pin

Show Connectivity Ctrl+T

Highlight

Unhighlight

Mark Ctrl+Shift+M

Unmark

Expand Cone

Add Selected Items to Schematic

Remove Selected Items from Schematic

Select All Ctrl+A

Cycle Selection Ctrl+Shift+A

View

Show World View

Report Timing

Save as PDF File...

Export Schematic...

Tcl Console Messages Log Reports Design Runs Timing

General Information Name Slack Levels Routes High Fanout

Constrained Paths (2)

clk (10)

Path 11 2.491 1 2 1
Path 12 2.491 1 2 1
Path 13 2.491 1 2 1
Path 14 2.491 1 2 1
Path 15 2.491 1 2 1

Report Timing - [get_cells {c_r[9].i_5}] Report Timing - [get_cells {B_IBUF[1].inst}] Report

Flow Navigator

Open Elaborated Design

SYNTHESIS

Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Open Dataflow Design

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

Report DRC

Report Noise

Report Utilization

Report Power

Schematic

IMPLEMENTATION

Run Implementation

Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

Report timing through the selected object

View Timing Info. for All Path

Specify Through Points

Specify a list of through pins, cells or nets.

Find names of type: Nets

Options

NAME contains *

Regular expression Ignore case Search hierarchically

Of Objects: Find

Results

Found: 0 Selected: 87

Use the buttons on the right to move items to this list.

Command: report_timing -through [get_nets {b_r[2]}] -delay_type min_max -max_paths 10 -sort_by group -input_pins -routeable_nets -name {[get_nets {b_r[2]}]}

OK Set Append Cancel

1. 2. 3. 4. 5. 6.

Report Timing

Generate a timing report.

Results name: [get_nets {b_r[2]}]

Targets Options Advanced Timer Settings

Start Points

From:

Through Points

Through: [get_nets {b_r[2]}]

End Points

To:

Command: report_timing -through [get_nets {b_r[2]}] -delay_type min_max -max_paths 10 -sort_by group -input_pins -routeable_nets -name {[get_nets {b_r[2]}]}

Open in a new tab

Open in Timing Analysis layout

?

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Utilization

This screenshot shows the Vivado 2024.1 software interface for a synthesized design project named "test_project".

The left sidebar contains the following navigation menu:

- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Run Linter
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Open Dataflow Design
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization** (highlighted with a red box)
 - Report Power
 - Schematic
- IMPLEMENTATION

The main window displays the following panels:

- SYNTHESIZED DESIGN - xc7a200tfg676-1**: Shows the Netlist panel with a list of components (e.g., LUT5, LUT6, FDCE) and a Path Properties panel for Path 1.
- Device**: Shows a grid of logic blocks labeled X0Y0 through X1Y4.
- Tcl Console**: Shows the Design Timing Summary table.

General Information		Setup		Hold		Pulse Width	
Timer Settings	Design Timing Summary	Worst Negative Slack (WNS):	2.491 ns	Worst Hold Slack (WHS):	0.202 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Clock Summary (1)	Clock Summary (1)	Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWNS):	0.000 ns
Methodology Summary	Methodology Summary	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Check Timing (0)	Check Timing (0)	Total Number of Endpoints:	40	Total Number of Endpoints:	40	Total Number of Endpoints:	17
Intra-Clock Paths	Intra-Clock Paths	All user specified timing constraints are met.					

- Timing Summary - timing_1**: Shows the timing summary for the clk signal.



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Utilization

Utilization

Hierarchy

- Summary
- Slice Logic
 - Slice LUTs (<1%)
 - LUT as Logic (<1%)
 - Slice Registers (<1%)
 - Register as Flip Flop (<1%)
- Memory
- DSP
- IO and GT Specific
 - Bonded IOB (5%)
- Clocking
 - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

Summary

Resource	Utilization	Available	Utilization %
LUT	12	134600	0.01
FF	16	269200	0.01
IO	20	400	5.00

The chart displays the utilization percentage for three resources: LUT, FF, and IO. The x-axis represents Utilization (%) from 0 to 100. The y-axis lists the resources. The bars show utilization values of 1%, 1%, and 5% respectively.

Resource	Utilization (%)
LUT	1%
FF	1%
IO	5%



Post Synthesis Simulation

The image shows a screenshot of the Vivado Simulator software interface. The top navigation bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Help, and Quick Access. A status bar at the top right indicates "Synthesis Complete". The main window has tabs for Flow Navigator, PROJECT MANAGER - test_project, and Reports. The PROJECT MANAGER tab shows a Sources panel with Design Sources, Constraints, and Simulation Sources. A context menu is open over the simulation sources, with "Run Post-Synthesis Timing Simulation" highlighted. The Reports tab displays a table of synthesis reports, with the "Utilization - Synth Design" report selected. The code editor on the right shows Verilog testbench code for a design named "test_tb.v". The bottom right corner features the text "NTU Microsystem Research Lab" and the number "70".

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Synthesis Complete ✓

Default Layout

PROJECT MANAGER - test_project

Sources

Design Sources (1)

Constraints (1)

constrs_1 (1)

constraint.xdc (target)

Simulation Sources (1)

sim_1 (1)

test_tb (test_tb.v) (1)

Run Behavioral Simulation

Run Post-Synthesis Functional Simulation

Run Post-Synthesis Timing Simulation

Run Post-Implementation Functional Simulation

Run Post-Implementation Timing Simulation

Location: D:/xilinx_data/project_1/project_1.srcs/sim_1/new

Type: Verilog

Library: xil_defaultlib

General Properties

Project Summary x testdesign.v x test_tb.v x

D:/xilinx_data/project_1/project_1.srcs/sim_1/new/test_tb.v

```
27: wire [9:0] C;
28: reg clk;
29: reg rst;
30: testdesign uut(A, B, C, clk, rst);
31: initial begin
32:   clk = 1'b0;
33: end
34: always begin #20; clk = ~clk; end
35: initial begin
36:   rst = 1'b0;
37:   #10; rst = 1'b1;
38:   #40; rst = 1'b0;
39: end
40: initial begin
41:   A = 0;
42:   B = 5;
43:   #40;
44:   A = 5; B = 5;
45:   #40;
46:   A = 10; B = 3;
47:   #40;
```

Tcl Console Messages Log Reports Design Runs

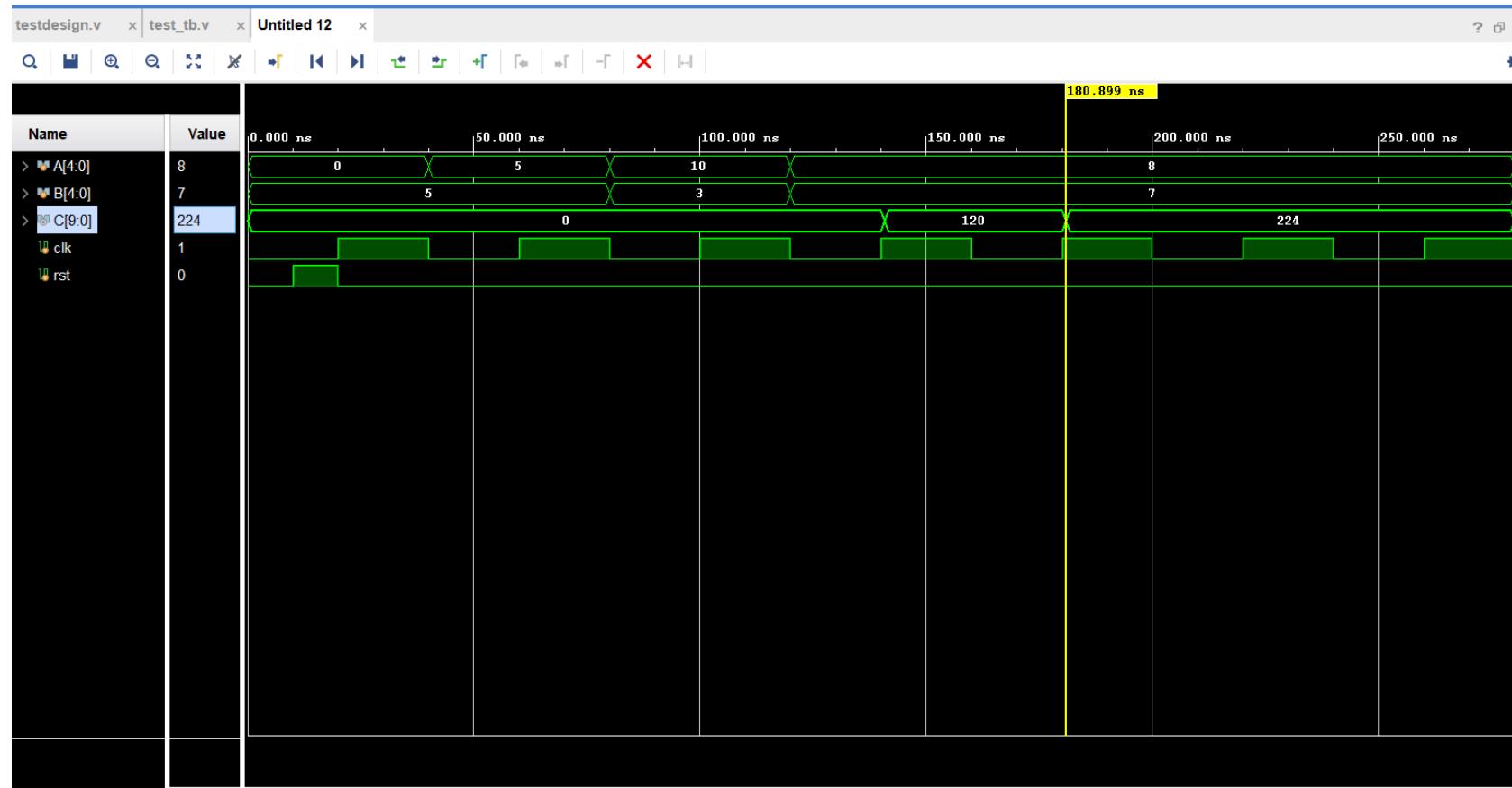
Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		11/19/24,	8.1 KB
synthesis_report			11/19/24,	16.4 KB
Implementation				

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Post Synthesis Simulation

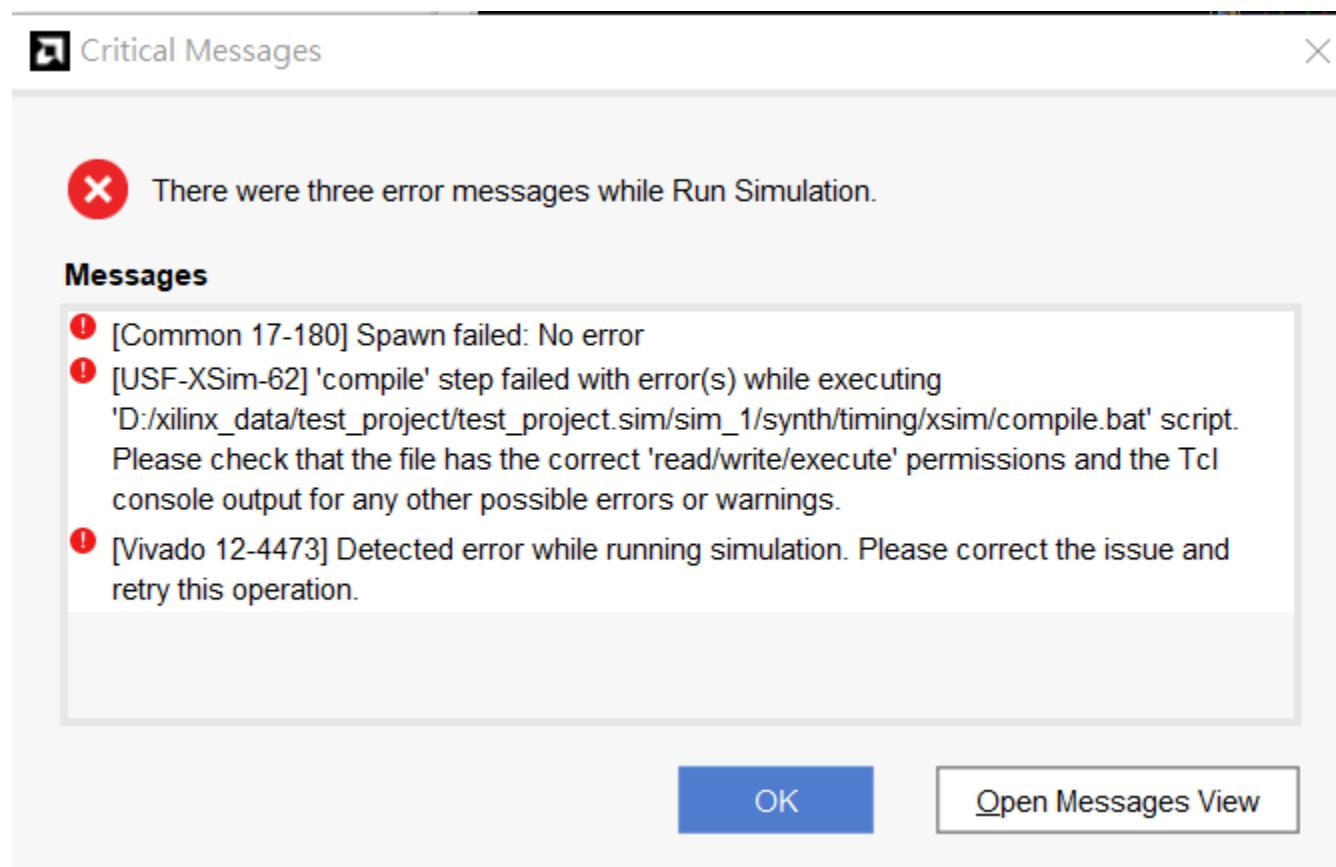




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Debug

- If you encounter this issue, execute “close_design” in Tcl console and rerun the simulation again.





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Reference

- https://xilinx.github.io/xup_fpga_vivado_flow/lab1.html
- <https://docs.amd.com/r/en-US/ug910-vivado-getting-started/Vivado-Design-Suite-Overview>