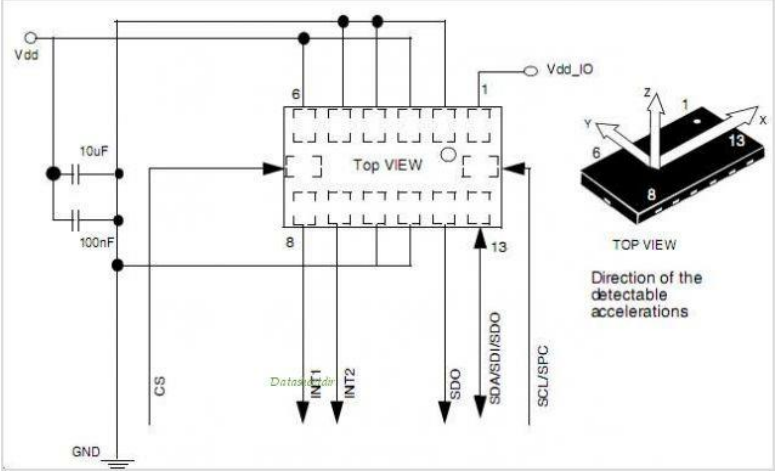
LIS302DL: 3-axis accelerometer



Description

The LIS302DL is an ultra compact low-power three axes linear accelerometer. It includes a a sensing element and an IC interface able to provide the measured acceleration to the external world through I2C/SPI serial interface.

The LIS302DL has dynamically user selectable full scales of ± 2g/± 8g and it is capable of measuring accelerations with an output data rate of 100 Hz or 400 Hz.

Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	GND	0V supply
3	Reserved	Connect to Vdd
4	GND	Connect to Vdd
5	GND	Connect to Vdd
6	Vdd	Power supply
7	CS	SPI enable I2C/SPI mode selection (1: I2C mode; 0: SPI enabled)
8	INT 1	Inertial interrupt 1
9	INT 2	Inertial interrupt 2
10	GND	0V supply
11	Reserved	Connect to Gnd
12	SDO	SPI Serial Data Output I2C less significant bit of the device address
13	SDA SDI SDO	I2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)

14	SCL SPC	I2C Serial Clock (SCL) SPI Serial Port Clock (SPC)

Register Mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address:

Name	Type	Register Address		Default	Comment
Ctrl_Reg1	rw	20	010 0000	00000111	
Ctrl_Reg2	rw	21	010 0001	00000000	
Ctrl_Reg2	rw	21	010 0001	00000000	
--	r	28	010 1000		Not Used
OutX	r	29	010 1001	output	
--	r	2A	010 1010		Not Used
OutY	r	2B	010 1011	output	
--	r	2C	010 1100		Not Used
OutZ	r	2D	010 1101	output	

To use LIS302DL we need to set CTRL_REG1 register

CTRL_REG1 (20h)

Table 18. CTRL_REG1 (20h) register

DR	**PD**	**FS**	**STP**	**STM**	**Zen**	**Yen**	**Xen**

Table 19. CTRL_REG1 (20h) register description

DR	Data rate selection. Default value: 0 (0: 100 Hz output data rate; 1: 400 Hz output data rate)
PD	Power Down Control. Default value: 0 (0: power down mode; 1: active mode)
FS	Full Scale selection. Default value: 0 (refer to Table 3 for typical full scale value)
STP, STM	Self Test Enable. Default value: 0 (0: normal mode; 1: self test P, M enabled)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

Communicate with LIS302DL through SPI bus interface

The LIS302DL SPI is a bus slave. The SPI allows to write and read the registers of the device. The Serial Interface interacts with the outside world with 4 wires: CS, SPC, SDI and SDO

CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC. Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of CS.

LIS302DL Initialize Subsystem

Sending setting through SPI to set data to CTRL_REG1(Address 20h)

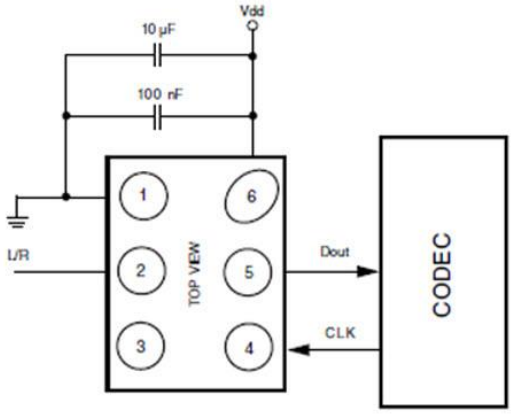
LIS302DL Read Subsystem

Reading data in 3 axis at register Out_X(Address 29h), Out_Y(Address 2Ah), Out_Z(Address 2Dh)

Using The Data

Data that we read from LIS302DL is int8 (-127 to 127) then we sent 3 data through UART every 0.02 sec or 50Hz and we need to transfrom by **2 x Read data / 127.** When we keep our board in normal plane Z value is 64.

MP45DT02: Microphone



Description

The MP45DT02-M is a compact, low-power, top- port, omnidirectional, digital MEMS microphone. The MP45DT02-M is built with a sensing element and an IC interface with stereo capability. The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process to produce audio sensors.

Pin #	Pin name	Function
1	GND	0 V supply
2	LR	Left/right channel selection; MIC1 LR is connected to GND or Vdd and MIC2 LR is connected to Vdd or GND
3	GND	0 V supply
4	CLK	Synchronization input clock
5	DOUT	Left/right PDM data output
6	Vdd	Power supply

Pulse-density modulation

This application note presents the algorithms and architecture of an optimized software implementation for PDM signal decoding and audio signal reconstruction when connecting an ST MP45DT02 MEMS microphone with an STM32 microcontroller. It can directly take the Pulse Density Modulated (PDM) data output from the microphone and convert it to 16-bit pulse-code modulation (PCM) format.

PDM digital filtering and decimation

The PDM signal from the microphone is filtered and decimated in order to obtain a sound signal at the required frequency and resolution. The frequency of the PDM data output from the microphone (which is the clock input to the microphone) must be a multiple of the final audio output needed from the system. For example, to perform a decimation of 80, for the output rate of 30 kHz, we need to provide a clock frequency 2.4MHz to the microphone. The output of the filter pipeline is a 16-bit value, we consider [-32768, 32767] as the output range for a unitary gain (0 dB).

PDM audio software decoding library description

The PDM library is composed of a structure and the implementation of four PDM filter functions. The library uses two buffers, the PDM Input buffer and the PCM Output buffer; the application must define these buffers in the main program. ● Input buffer (data) is a uint8 variable with a length equal to (Output frequency / 1000 * decimation factor * Input Microphone Channels / 8) at least. ● Output buffer (dataOut) is a uint16 variable with a length equal to (Output frequency / 1000 * Output Microphone Channels) at least. The structure is defined in the pdm_filter.h file and is used to configure the filter; it is composed as follows:

```
typedef struct {
    uint16_t Fs;
    float LP_HZ;
    float HP_HZ;
    uint16_t Out_MicChannels;
    char InternalFilter[34];
} PDMFilter_InitStruct;
```

● **Fs:** Defines the frequency output of the filter in Hz.

● **LP_HZ:** Defines the low pass filter cut-off frequency. If 0, the low pass filter is disabled.

● **HP_HZ:** Defines the high pass filter cut frequency. If 0, the high pass filter is disabled.

● **In_MicChannels:** Define the number of microphones in the input stream. This parameter is used to specify the interlacing of microphones in the input buffer. The PDM samples are grouped eight by eight in u8 format (8-bit).

● **Out_MicChannels:** Defines the number of microphones in the output stream; this parameter is used to interlace different microphones in the output buffer. Each sample is a 16-bit value. ● InternalFilter: Defines a 34 Byte memory used internally by the library during the PDM decimation step.

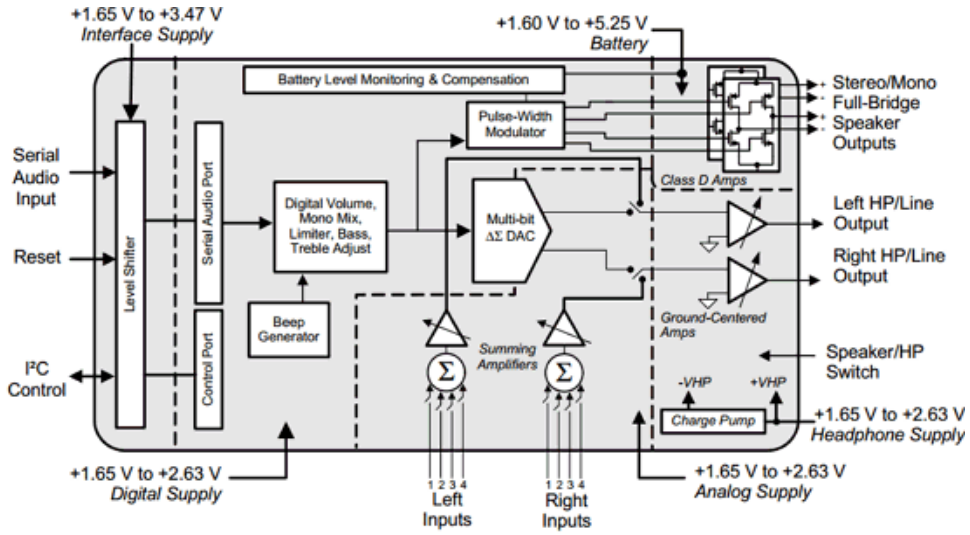
PDM_Filter_Init

This function is used to initialize the filter of a single output channel. It is defined as follows

PDM_Filter_xx_xx

These functions are used to process a millisecond of PDM data from a single microphone. They return a number of PCM samples equal to the frequency defined in the filter initialization, divided by 1000. In case of frequencies that are not multiple of 1000 (like 44100 Hz or 22050 Hz), the samples returned by the function are equal to the floor division of the frequencies (44 and 22).

CS43L22: Audio Output



Description

The CS43L22 is a highly integrated, low power stereo DAC with headphone and ClassD speaker amplifiers. The CS43L22 offers many features suitable for low power, portable system applications.

Initialization

The CS43L22 enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the RESET pin is brought high. The control port is accessible once RESET is high and the desired register settings can be loaded per the interface descriptions in the “Register Description” on page 37

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

Recommended Power-Up Sequence

1. Hold RESET low until the power supplies are stable.
2. Bring RESET high.
3. The default state of the “Power Ctl. 1” register (0x02) is 0x01. Load the desired register settings while keeping the “Power Ctl 1” register set to 0x01.
4. Write 0x99 to register 0x00.
5. Write 0x80 to register 0x47.
6. Write ‘1’b to bit 7 in register 0x32.
7. Write ‘0’b to bit 7 in register 0x32.
8. Write 0x00 to register 0x00.
9. Apply MCLK at the appropriate frequency, as discussed in Section 4.6. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
10. Set the “Power Ctl 1” register (0x02) to 0x9E.
11. Bring RESET low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

Communicate with CS43L22 through I2C

SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The AD0 pin sets the LSB of the chip address; ‘0’ when connected to DGND, ‘1’ when connected to VL. This pin may be driven by a host controller or directly connected to VL or DGND. The AD0 pin state is sensed and the LSB of the chip address is set upon the release of the RESET signal (a low-to-high transition).

The signal timings for a read and write cycle are shown in Figure 16 and Figure 17. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS43L22 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write).

The upper 6 bits of the address field are fixed at 100101. To communicate with the CS43L22, the chip address field, which is the first byte sent to the CS43L22, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated

by an acknowledge bit. The ACK bit is output from the CS43L22 after each input byte is read and is input to the CS43L22 from the microcontroller after each transmitted byte.

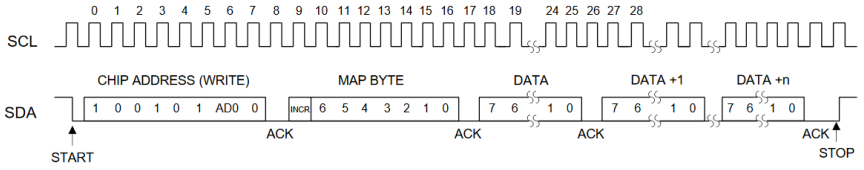


Figure 16. Control Port Timing, I²C Write

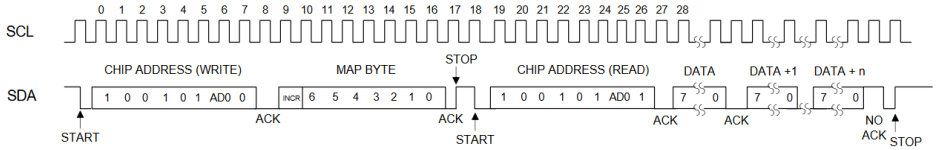


Figure 17. Control Port Timing, I²C Read

Register Description

Power Control 1 (Address 02h)

PDN7	PDN6	PDN5	PDN4	PDN3	PDN2	PDN1	PDN0

Power Down: Configures the power state of the CS43L22.

PDN[7:0]	Status
0000 000	Powered Down - same as setting 1001 111
1001 111	Powered U
1001 111	Powered Down - same as setting 000

Power Control 2 (Address 04h)

PDN_HPB 1	PDN_HPB 0	PDN_HPA 1	PDN_HPA 0	PDN_SPKB 1	PDN_SPKB 0	PDN_SPKA 1	PDN_SPKA 0

Headphone Power Control: Configures how the SPK/HP_SW pin, 6, controls the power for the headphone amplifier.

PDN_HPx[1:0]	Headphone Status
00	Headphone channel is ON when the SPK/HP_SW pin, 6, is LO. Headphone channel is OFF when the SPK/HP_SW pin, 6, is HI.
01	Headphone channel is ON when the SPK/HP_SW pin, 6, is LO. Headphone channel is OFF when the SPK/HP_SW pin, 6, is HI.
10	Headphone channel is always ON.
11	Headphone channel is always OFF.

Speaker Power Control: Configures how the SPK/HP_SW pin, 6, controls the power for the speaker amplifier.

PDN_SPKx[1:0]	Speaker Status
00	Speaker channel is ON when the SPK/HP_SW pin, 6, is LO. Speaker channel is OFF when the SPK/HP_SW pin, 6, is HI.
01	Speaker channel is ON when the SPK/HP_SW pin, 6, is LO. Speaker channel is OFF when the SPK/HP_SW pin, 6, is HI.
10	Speaker channel is always ON.
11	Speaker channel is always OFF.

Interface Control 1 (Address 06h)

M/S	INV_SCLK	Reserved	DSP	DACDIF1	DACDIF0	AWL1	AWL0

Master/Slave Mode: Configures the serial port I/O clocking.

M/S	Serial Port Clocks
0	Slave (input ONLY)
1	Master (output ONLY)

SCLK Polarit: Configures the polarity of the SCLK signal.

INV_SCLK	SCLK Polarity
0	Not Inverted
1	Inverted

DSP Mode: Configures a data-packed interface format for the DAC.

DSP	DSP Mode
0	Disabled
1	Enabled
Application	“DSP Mode” on page

Notes:

1. Select the audio word length using the AWL[1:0] bits (“Audio Word Length” on page 41).

2. The interface format for the DAC must be set to “Left-Justified” when DSP Mode is enabled.

DAC Interface Format: Configures the digital interface format for data on SDIN.

DACDIF[1:0]	DAC Interface Format
00	Left Justified, up to 24-bit data
01	I²S, up to 24-bit data
10	Right Justified
11	Reserved
Application:	“Digital Interface Formats” on page

Audio Word Length: Configures the audio sample word length used for the data into SDIN.

AWL[1:0]	DSP Mode	Right Justified
00	32-bit data	24-bit data

01	24-bit data	20-bit data
10	20-bit data	18-bit data
11	16-bit data	16-bit data
Application:	“DSP Mode” on page 31	

PCMx Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)

PCMxMUTE	PCMxVOL6	PCMxVOL5	PCMxVOL4	PCMxVOL3	PCMxVOL2	PCMxVOL1	PCMxVOL0

PCM Channel x Mute: Configures a digital mute on the PCM data from the serial data input (SDIN) to the DSP.

PCMxMUTE	PCM Mute
0	Disabled
1	Enabled

PCM x Volume: Sets the volume/gain of the analog input signal routed to the headphone/line output.

PCMxVOL[6:0]	Volume
001 1000	+12.0 dB
...	...
000 0001	+0.5 dB
000 0000	0 dB
111 1111	-0.5 dB
...	...
001 1001	-51.5 dB
Step Size:	0.5 dB