SKILLS SUMMARY

TECHNICAL SKILLS

●●●● Digital Design
- ○ SystemVerilog , Verilog
- ○ UVM
- ○ Xilinx Vivado

●●●○ Embedded System
- ○ ARM , AVR microcotrolers
- ○ AutoDesk Eagle, EasyEDA
- ○ Keli uVision
- ○ Arduino

●●●● MATLAB , LTpice

●●●○ App Development
- ○ Flutter
- ○ Dart
- ○ Android Studio
- ○ Java
- ○ Kotlin
- ○ XML

●●●○ 3D design
- ○ Blender

●●●● Python

●●●● Visual Basic

KASUN BUDDHI

ELECTRONIC ENGINEER

PERSONAL PROFILE

I am a highly motivated and ambitious electronic engineer with a keen interest in digital design. As a recent graduate in Electrical Engineering from the University of Moratuwa, I possess a solid foundation in digital design. In my current role as an Electronic Engineer, I have gained valuable experience in RTL design and verification, and I am constantly seeking opportunities to expand my knowledge and skill set. I am an excellent team player and possess strong communication skills, allowing me to work effectively with others to achieve project objectives. I am an energetic, responsible, and quick learner, and I am committed to delivering high-quality results. I am dedicated to pursuing a successful career in electronic engineering, and I am eager to contribute to the success of my team.

EDUCATIONAL HISTORY

System Verilog for ASIC/FPGA Design & Simulation Course
University of Moratuwa | 2023

BSc Engineering (Hons) Graduate
University of Moratuwa | 2017

- Specialization : Electrical Engineering
- GPA - 3.01

GCE Advanced Level Examination
Anuradhapura central college | 2016

- A-2
- B-1

Primary Education
A/Maithreepala senanayake central college medawachchiya | 2003 - 2008

WORKING EXPERIENCE

Electronic Engineer: ACCELR
(jan 2023- present)

INTERN: LANKA ELECTRICITY COMPANY (LECO)
(May 2021- June 2021)

INTERN : ABANS Engineering (Pvt) Ltd - MEP Division
(jan 2021- April 2021)

INTERN: CEYLON ELECTRICITY BOARD (CEB)
(April 2021- May 2021)

PROJECTS

PULPissimo RISC-V platform verification environment

This is an ongoing project at ACCELR
Recently, I have been examining the documentation pertaining to the PULPissimo microcontroller architecture.

UVM Verification IP for AXI4-stream

The VIP for a DUT encompasses AXI4-Stream master and slave ports. Its primary goal is to streamline the verification process of DUTs that employ the AXI4-Stream protocol at the packet level. We leverage the Xilinx AXI4-Stream VIP to develop our own VIP.
https://github.com/accelr-net/axi4stream_vip_fifo

Intelligent Floor Cleaning Robot to Tidy up Kids Room and Living Room

Domestic floor cleaning robot with robot arm manipulators to efficient cleaning process - simulation
- Cleaning robot model designing with blender
- Combination of sensors and manipulators
- Controller for vacuum cleaning

Electrical Door Controller (Group Project)

- Developed an electrical sliding door with IoT concepts
- Developed an Android app for sliding doors with many features.
- Working with real-time Firebase database
- Programming languages : Arduino , C/C++ , Kotlin

EXTRA CURRICULAR ACTIVITIES

Active Member of Electrical Engineering Society - UOM

- Volunteered in projects "We are with you" which was held in Rathmalana deaf school (2018,2019)

Member Of IEEE Society

Member Of IESL