Digital Logic Design Questions

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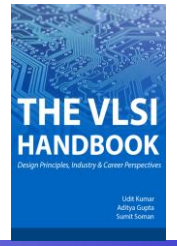

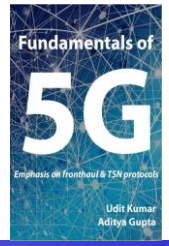

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Motivation

- In almost all interview, Questions on digital logic design are asked to check candidate understanding and thought process.
- The intention of this slide is to capture various Digital Logic Design Questions so that candidates can do self practices before attending interviews.
- A pen and paper based self practice help to improve the design understanding.
- The first step is to collect various design problems, and in the second step, will add solution and share on the “Learn VLSI” page.
- **Your contribution will help to improve this question list.**

Combinational logic design questions

1. Implementation of all gates using universal gates (NAND, NOR)

2. Design A Four-input Nand Gate Using Only Two-input Nand Gates

3. Implement all the basic gates using 2:1 Mux

4. Implement 4:1Mux using 2:1 Mux without using any additional gates

5. Design 6:1 Mux using 2:1 Mux

6. Design a 16:1 Mux using 2:1 Mux

7. Design a full adder using 3:8 Decoder

Combinational logic design questions

8. Design a 4:1 priority encoder

9. Design a 3:6 decoder.

10. Implement a full adder using two 4:1 Mux

11. How do you detect if two 8-bit signals are same?

12. Design a logic circuit whose output is high only when a majority of inputs A, B, and C are low.

13. How will you implement a full subtractor from a full adder?

14. How to design multiplier circuit for 4x4?

Sequential logic design Question

1. Make a T Flip Flop using a D Flip Flop
2. Design clock gating circuit, why latch based clock gating are used?
3. Give the circuit to extend the falling edge of the input by 2 clock pulses?
4. Divide by 2 counter implementation
5. Divide by 3 counter implementation
6. Design a 3 bit Gray Counter
7. Frequency Divider for divide by 2, 3, 5 with 50% duty cycles.
8. How to design a circuit input 200mhz clk frq to output 4 MHz clk frq

Sequential logic design Question

9. Design a counter, where output should be high after every 8 cycles.

10. Design a counter which counts from 1 to 10 (Resets to 1, after 10).

11. Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop, using D flip-flop.

12. Design a counter with the following binary sequence 0, 1, 9, 3, 2, 8, 4 and repeat.

13. Design a MOD 10 counter with 50%/33% duty cycle.

14. Sequence Detector to detect 10101 for overlapping and non overlapping method.

15. Design a Mealy FSM for 010 and 1010.

16. Design Edge detectors (Falling Edge, Rising Edge & Both Edge)

17. Circuit for 1st one finder for a series input.

Design Problems

1. Design a state machine to implement a edge detector That is. The output of this state machine is a pulse of logic '1' of duration one clock when ever there is a negative edge on an input signal. Given that the frequency at which the negative edge is appearing on the input signal is low as compared to the clock of the state machine

2. Design a synchronous sequential circuit in the form of a positive edge-triggered Moore machine. The input signal w is synchronized with the clock pulses C. The output signal z should become 1 each time the value of the input signal w had not changed for two clock pulses. This change in the output value will appear at the clock pulse following the two pulses with the identical w values. See the example below for clarification.

w: 0011000110111001111111000010110 ...

z: 0010101001001001010000001000001

Design Problems

3. Design an FSM that has an input w and an output z. The machine is a sequence detector that produces z = 1 when the previous two values of w were 00 or 11; otherwise z = 0.

4. Implement the above sequence detector by using two FSMs. One FSM detects the occurrence of consecutive 1s, while the other detects consecutive 0s.

5. Design a state machine for an elevator inside a 4-story building, that has an up/down button and buttons inside the elevator, consider the case of 8 floor in the building. If multiple buttons are pressed, which direction does the elevator go?

6. In the series of binary 1 bit input, we need to check weather the received overall input is divisible by say '5', explain the concent to make this to divisible by 'n'.

Design Problems

7. Given an array with 2n+1 integer elements, n elements appear twice in arbitrary places in the array and a single integer appears only once somewhere inside. Find the lonely integer using digital design.

8. Method to dynamically clock selection without glitch.

9. How would you design a FIFO, Design a async for scenarios mentioned in following link

- https://www.linkedin.com/feed/update/urn:li:activity:6908349997906051072

10. I have a pulse in one clock domain that needs to cross into another clock domain. Can you design a circuit that works when the two separate clock domains have the same frequency? Domain A is faster? Domain B is faster? Provide a general solution which does not depend on Domain A or B clock relationship.

Thank you for the contribution

- Many candidates helped us to share these interview questions.

- **Please contribute additional questions by filling this form**
  - https://docs.google.com/forms/d/e/1FAIpQLSeOmeTEkIutOUixM9WXU7vb9vtfHu2D7sJt8GHaMAUVoFlnWA/viewform

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VLSI Industry & Career and QnA, Jul 16, 9:30AM – 12:00PM (IST)

HDL Design using Verilog, Jul 30, 9:30AM – 12:00PM (IST)

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