SYNOPSYS®

UVM-1.2

SystemVerilog Testbench

VCS 2016.06

Synopsys Customer Education Services

© 2016 Synopsys, Inc. All Rights Reserved

Synopsys 40-I-055-SSG-003

Introductions

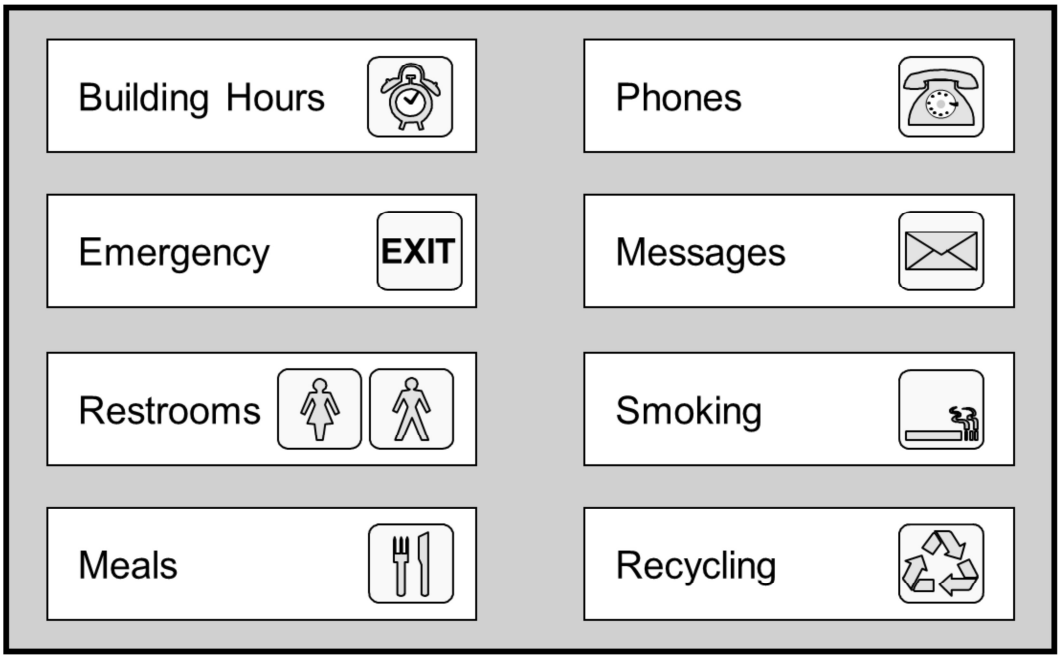
- Name
- Company
- Job Responsibilities
- EDA Experience
- Main Goal(s) and Expectations for this Course

i- 2

EDA = Electronic Design Automation

© 2016 Synopsys, Inc. All Rights Reserved

Facilities



Please turn off cell phones and pagers

i- 3

© 2016 Synopsys, Inc. All Rights Reserved

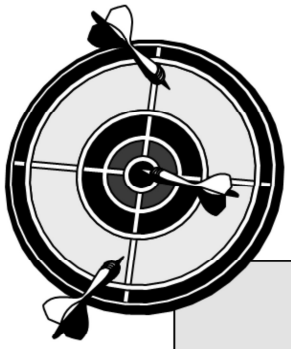
Course Materials

- Student Workbook
- Lab Book
- Reference Materials
- Course Evaluations

i- 4

© 2016 Synopsys, Inc. All Rights Reserved

Workshop Goal



Acquire the skills to implement a UVM testbench to verify Verilog/VHDL designs with coverage-driven random stimulus

i- 5

© 2016 Synopsys, Inc. All Rights Reserved

Target Audience

Design or Verification engineers writing SystemVerilog testbenches to verify Verilog or VHDL designs

i- 6

© 2016 Synopsys, Inc. All Rights Reserved

Workshop Prerequisites

- **You should have experience in the following areas:**
  - Familiarity with a UNIX text editor
  - Programming skills in SystemVerilog
  - Debugging experience with SystemVerilog

i- 7

© 2016 Synopsys, Inc. All Rights Reserved

What's Covered in This Workshop

- **This workshop covers both UVM-1.1 and UVM-1.2**
  - Bulk of UVM testbenches will still be UVM-1.1 for some time
    - There are compatibility issues (will be covered)
  - For the labs:
    - **`"make"`** uses UVM-1.2 source code in vcs
    - **`"make uvm_ver=uvm-1.1"`** uses UVM-1.1d source code in vcs
- **Two major differences between UVM-1.1 and 1.2 are described in the lecture and labs**
  - Objection in sequences (non-compatible)
  - Accessing **`uvm_root`** and **`uvm_factory`** singleton object
    - Direct access to **`uvm_top`** and **`factory`** instances are removed

i- 8

© 2016 Synopsys, Inc. All Rights Reserved

Agenda: Day 1

DAY 1

1. OOP Inheritance Review
2. UVM Structural Overview
3. UVM Transaction
4. UVM Sequence

i- 9

© 2016 Synopsys, Inc. All Rights Reserved

Agenda: Day 2

DAY 2

5 UVM Configuration & Factory

6 UVM Component Communication

7 UVM Scoreboard & Coverage

8 UVM Callback

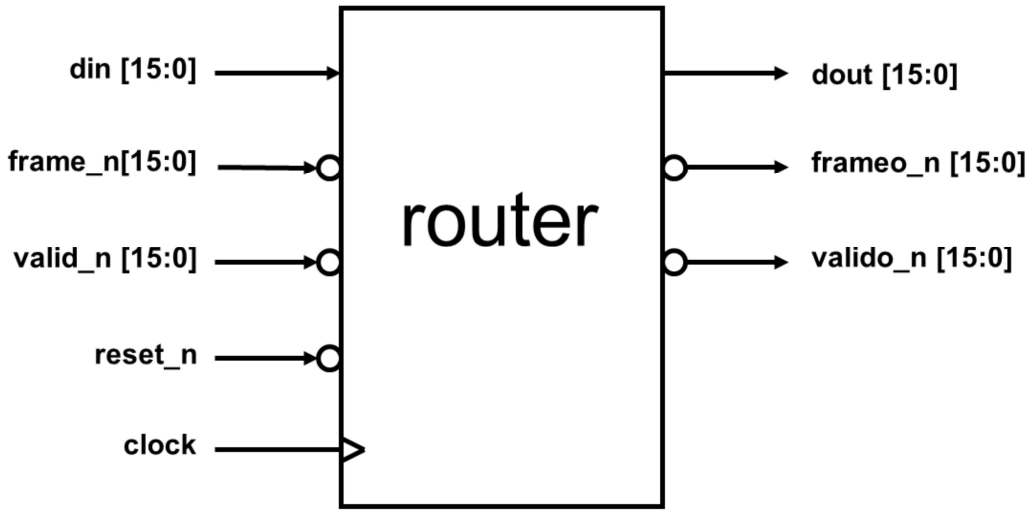
i-10

© 2016 Synopsys, Inc. All Rights Reserved

What Is the Device Under Test?

A router:

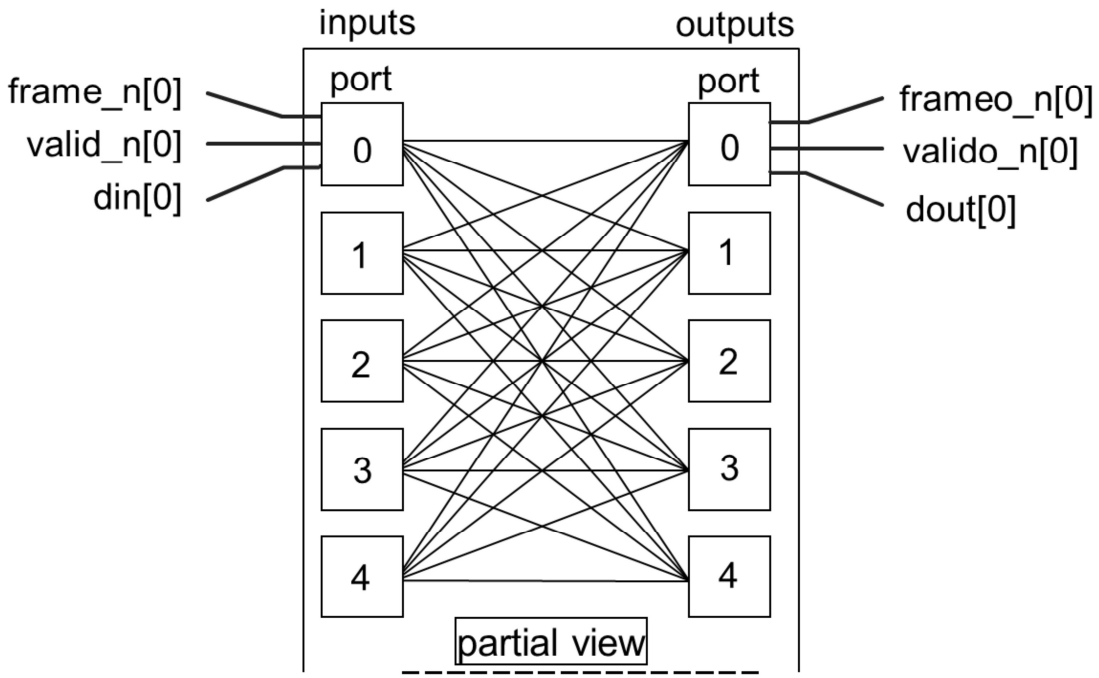
16 x 16 crosspoint switch



i-12

© 2016 Synopsys, Inc. All Rights Reserved

A Functional Perspective

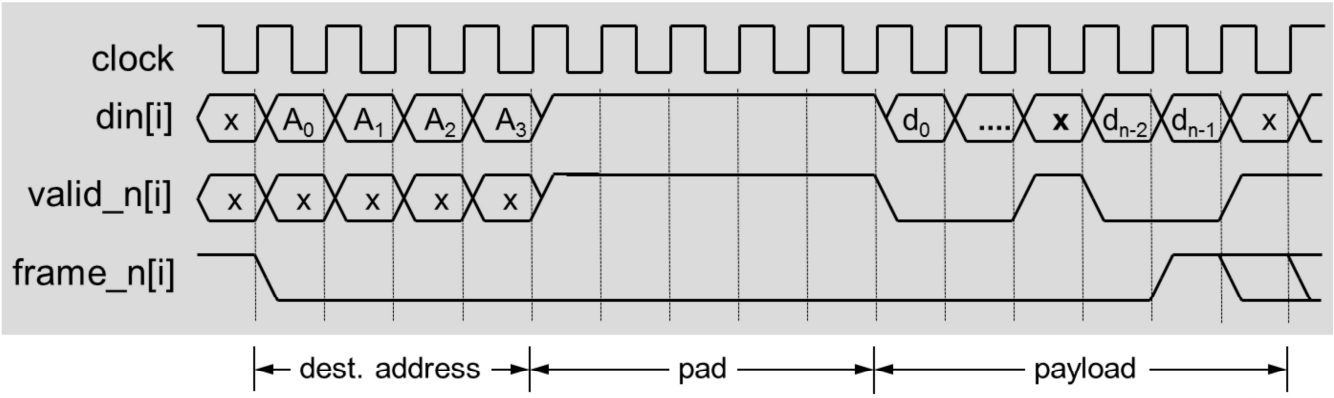


i-13

© 2016 Synopsys, Inc. All Rights Reserved

Input Packet Structure

- **frame_n:**
  - Falling edge indicates first bit of packet
  - Rising edge indicates last bit of packet
- **din:**
  - Header (destination address & padding bits) and payload
- **valid_n:**
  - valid_n is low if payload bit is valid, high otherwise

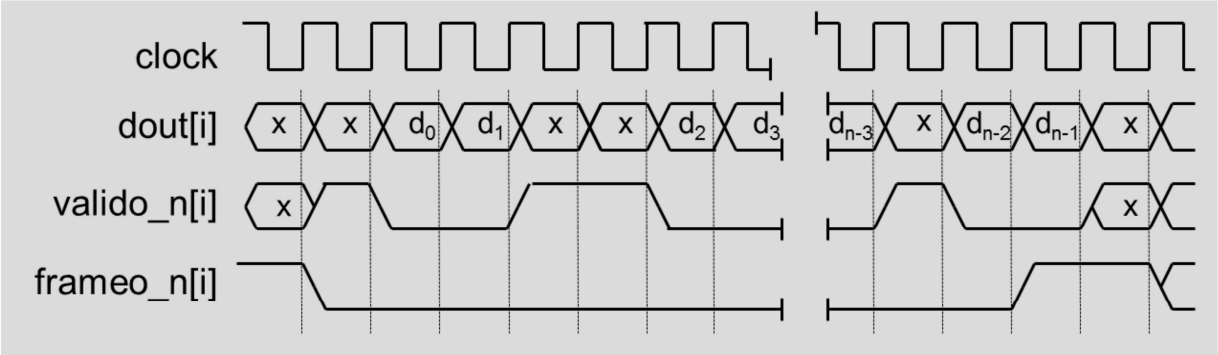


i-14

© 2016 Synopsys, Inc. All Rights Reserved

Output Packet Structure

- **Output activity is indicated by: frameo_n, valido_n, and dout**
- **Data is valid only when:**
  - frameo_n output is low (except for last bit)
  - valido_n output is low
- **Header field is stripped**

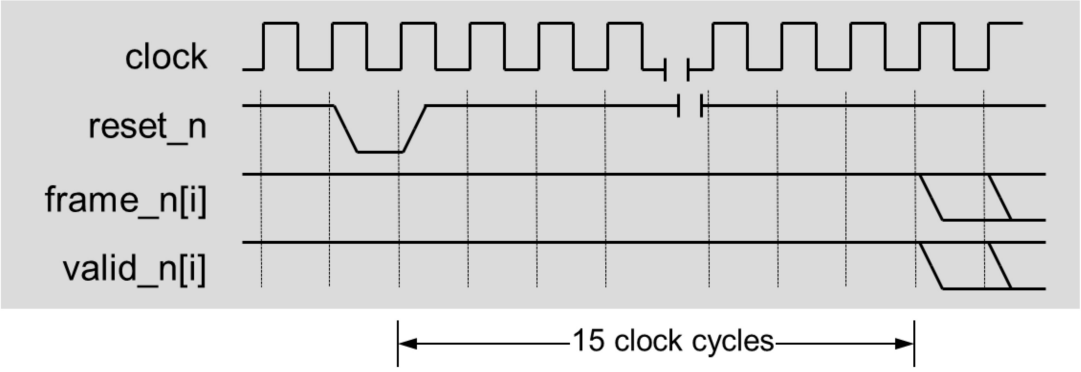


i-15

© 2016 Synopsys, Inc. All Rights Reserved

Reset Signal

- While asserting `reset_n`, `frame_n` and `valid_n` must be de-asserted
- `reset_n` is asserted for at least one clock cycle
- After de-asserting `reset_n`, wait for 15 clocks before sending a packet through the router



i-16

© 2016 Synopsys, Inc. All Rights Reserved

Icons Used in this Workshop

Lab Exercise

Caution

Recommendation

Definition of Acronyms

For Further Reference

Question

"Under the Hood" Information

Group Exercise

i-17

Lab Exercise: A lab is associated with this unit, module, or concept.
Recommendation: Recommendations, tips, performance boost, etc.
For Further Reference: Identifies pointer or URL to other references or resources.
Under the Hood Information: Information about the internal behavior of the tool.

Caution: Warnings of common mistakes, unexpected behavior, etc.
Definition of Acronyms: Defines the acronym used in the slides.
Question: Marks questions asked on the slide.
Group Exercise: Test for Understanding (TFU), which may require you to work in groups.

© 2016 Synopsys, Inc. All Rights Reserved