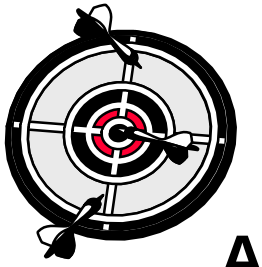
# Agenda: Day 1

**DAY 1**

1. The Device Under Test (DUT)
2. SystemVerilog Verification Environment 
3. SystemVerilog Language Basics - 1
4. SystemVerilog Language Basics - 2 

# Unit Objectives

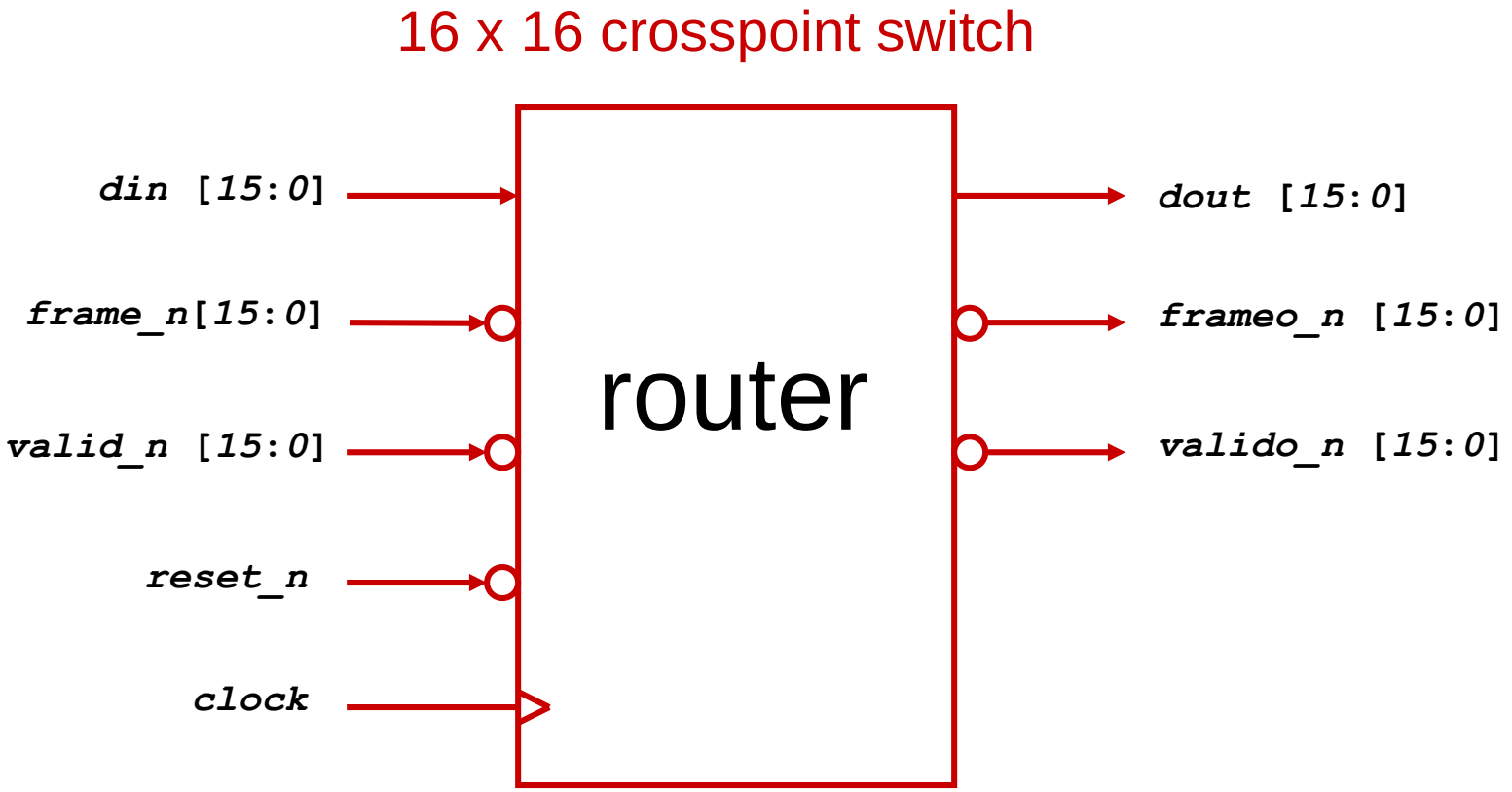


**After completing this unit, you should be able to:**

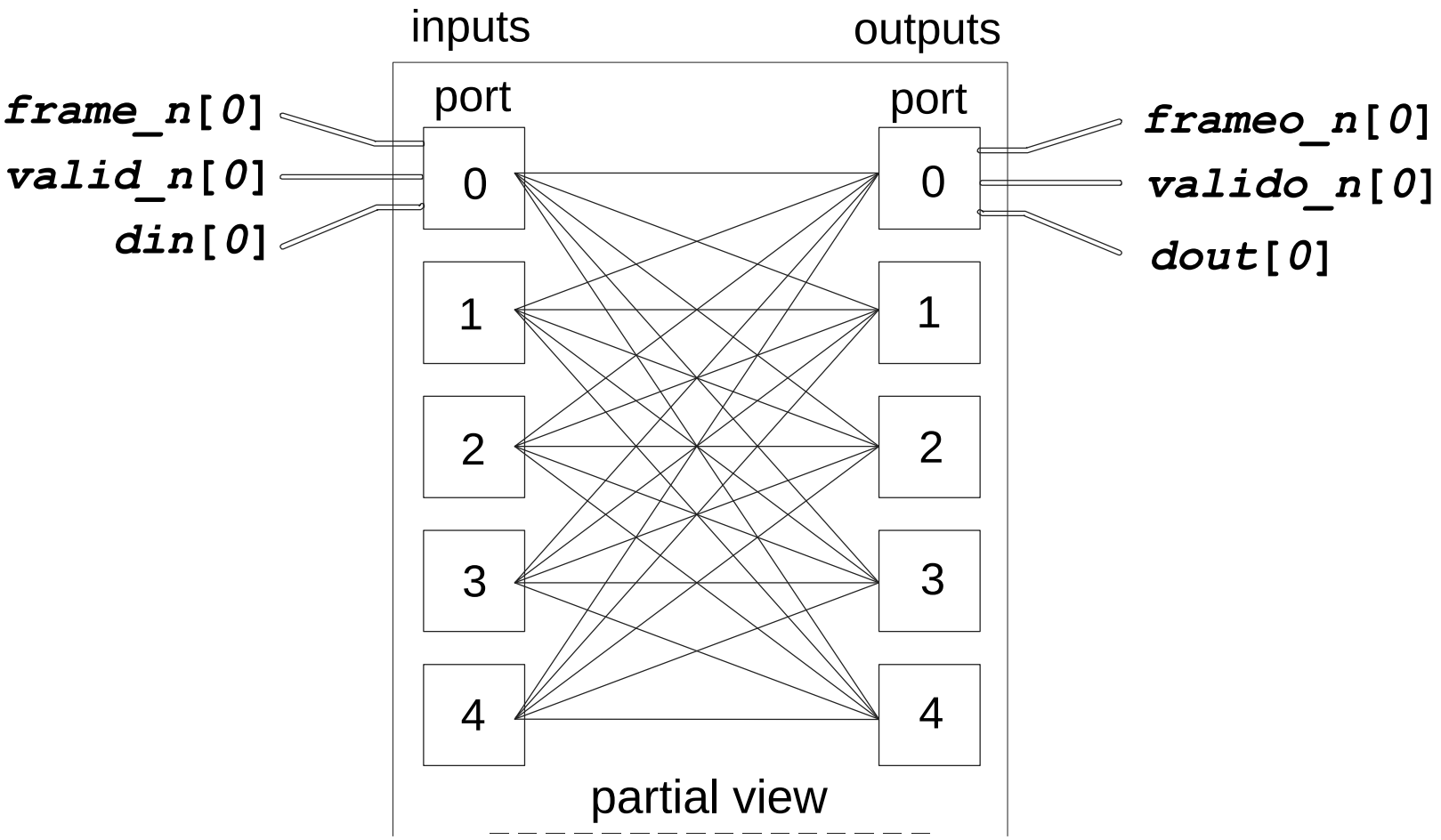
- **Describe the function of the Device Under Test (DUT)**
- **Identify the control and data signals of the DUT**
- **Draw timing diagram for sending and receiving a packet of data through the DUT**

# What Is the Device Under Test?

## A router:



# A Functional Perspective

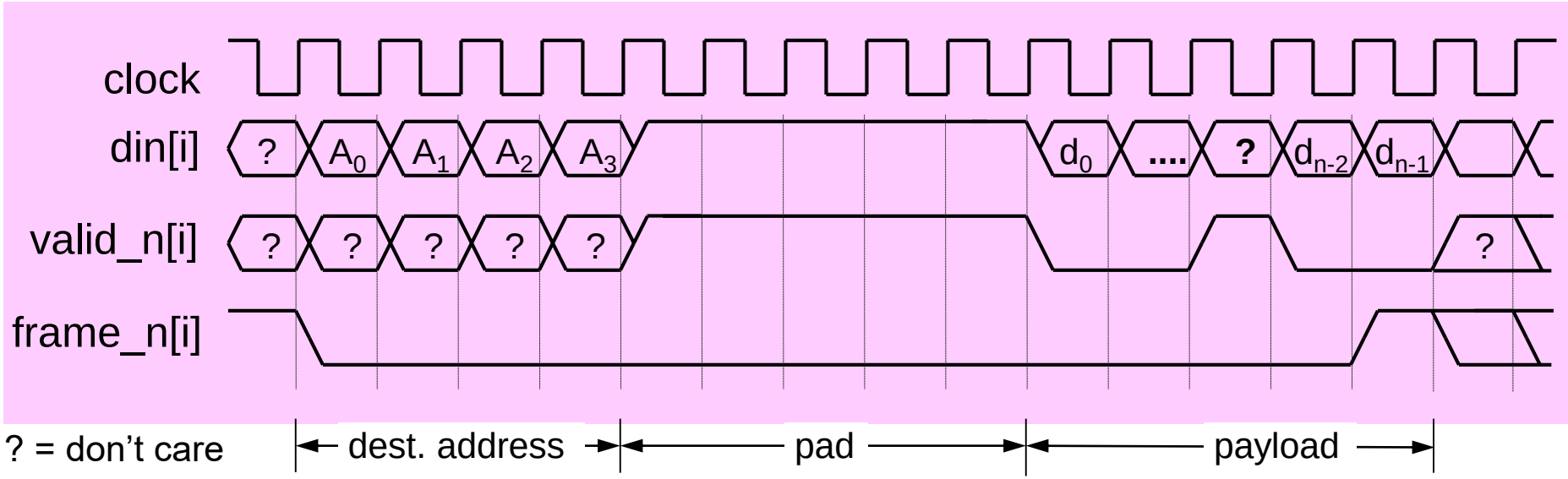


# The Router Description

- **Single positive-edge clock**
- **Input and output data are serial (1 bit / clock)**
- **Packets are sent through in variable length:**
  - Each packet is composed of two parts
    - Header
    - Payload
- **Packets can be routed from any input port to any output port on a packet-by-packet basis**
- **No internal buffering or broadcasting (1-to-N)**

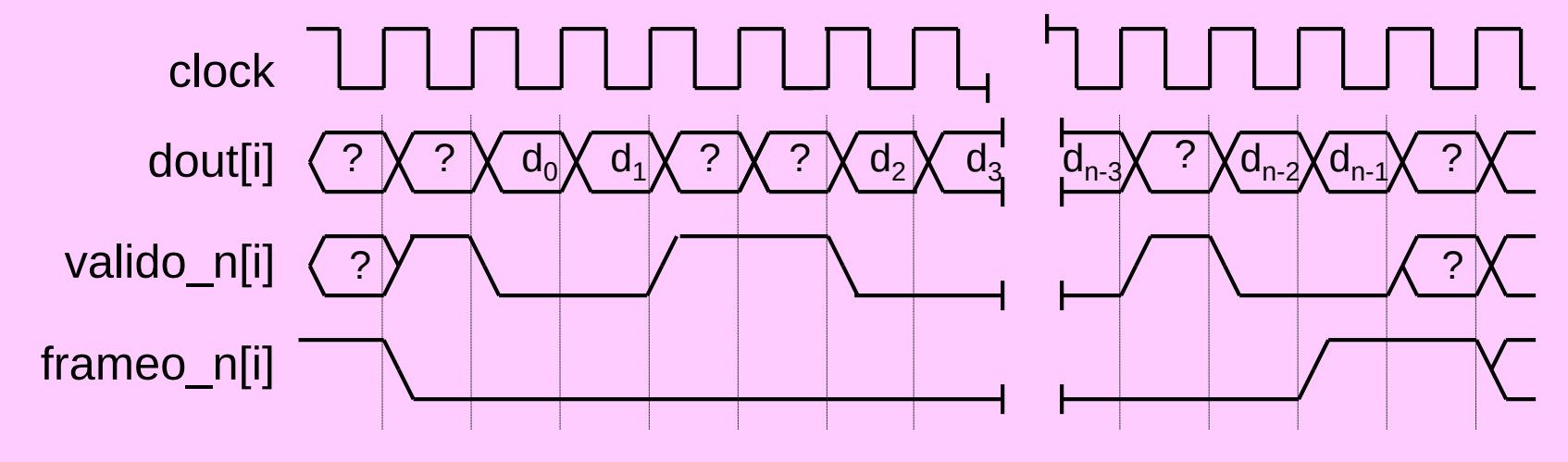
# Input Packet Structure

- ***frame_n***:
  - Falling edge indicates first bit of packet
  - Rising edge indicates last bit of packet
- ***din***:
  - Header (destination address & padding bits) and payload
- ***valid_n***:
  - ***valid_n*** is low if payload bit is low, high otherwise



# Output Packet Structure

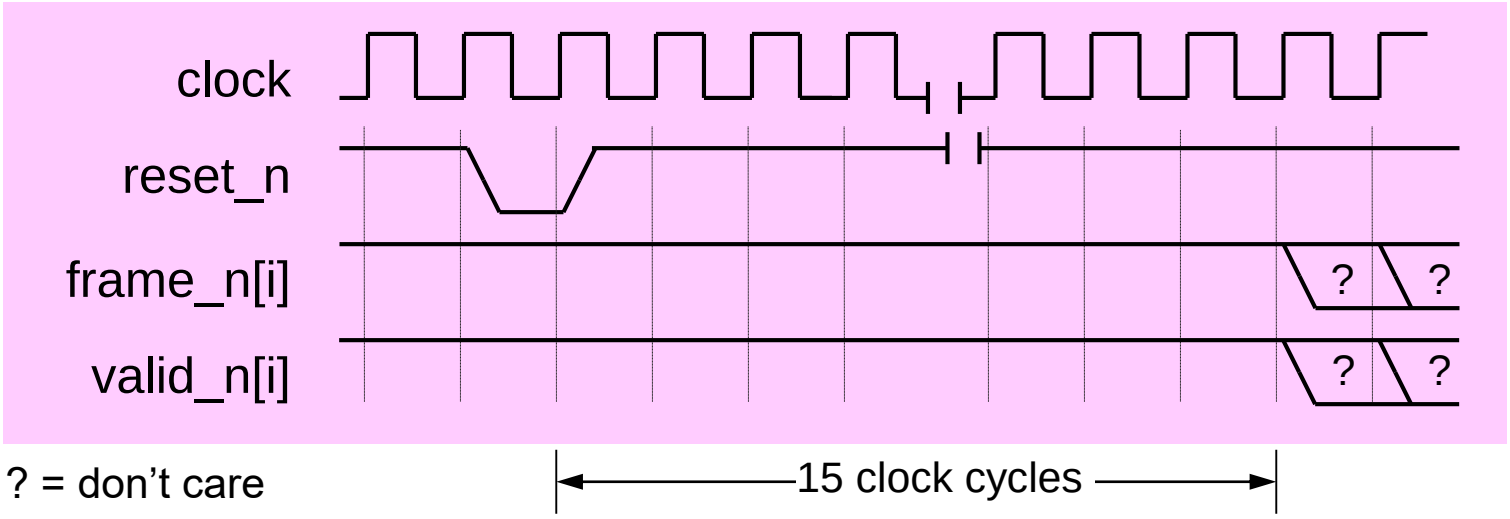
- **Output activity is indicated by:**
  ***frameo_n*, *valido_n*, and *dout***
- **Data is valid only when:**
  - ***frameo_n*** output is low (except for last bit)
  - ***valido_n*** output is low
- **Header field is stripped**




? = don't care

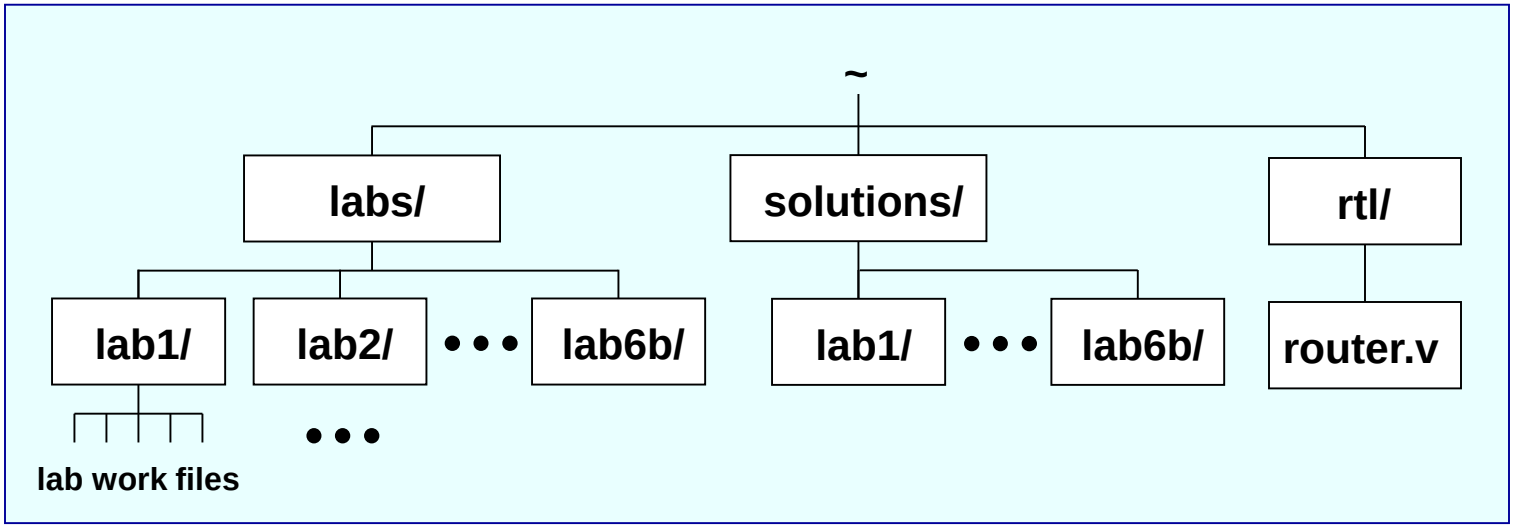
# Reset Signal

- While asserting ***reset_n***, ***frame_n*** and ***valid_n*** must be **de-asserted**
- ***reset_n*** is asserted for at least one clock cycle
- After de-asserting ***reset_n***, wait for 15 clocks before sending a packet through the router



# The DUT: `router.v`

- **The Design Under Test, *`router.v`*, is a Verilog file:**
  - Located under the ***`rtl`*** directory
  - From the lab workspace: **`../../rtl/router.v`**



# Unit Objectives Review

**Having completed this unit, you should be able to:**

- **Describe the function of the Device Under Test (DUT)**
- **Identify the control and data signals of the DUT**
- **Draw timing diagram for sending and receiving a packet of data through the DUT**