SYNOPSYS®

SystemVerilog Testbench

VCS 2016.06

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Introductions

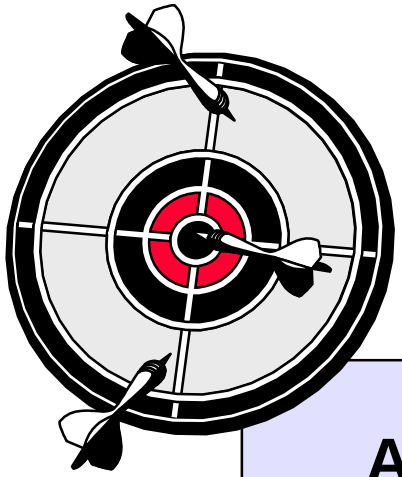
- Name
- Company
- Job Responsibilities
- EDA Experience
- Main Goal(s) and Expectations for this Course

Facilities

- Building Hours
- Meals
- Emergency
- Smoking
- Restrooms
- Recycling

Please turn off or mute your cell phones

Workshop Goal



Acquire the skills to write a SystemVerilog testbench to verify Verilog/SystemVerilog RTL code with coverage-driven random stimulus.

Target Audience

Design or Verification engineers writing SystemVerilog testbenches to verify Verilog or SystemVerilog code.

Workshop Prerequisites

- **You must have experience in the following areas:**
  - Familiarity with a UNIX text editor
  - Basic programming skills in Verilog, VHDL or C
  - Debugging experience with Verilog, VHDL or C

Agenda: Day 1

DAY 1

1	The Device Under Test (DUT)
2	SystemVerilog Verification Environment 
3	SystemVerilog Language Basics - 1
4	SystemVerilog Language Basics - 2 

Agenda: Day 2

DAY 2

5	Concurrency 
6	Object Oriented Programming (OOP) – Encapsulation
7	Object Oriented Programming (OOP) – Randomization 

Agenda: Day 3

DAY 3

8	Object Oriented Programming (OOP) – Inheritance
9	Inter-Thread Communications 
10	Functional Coverage 
11	SystemVerilog UVM Preview
CS	Customer Support

Icons Used in this Workshop

Lab Exercise

Caution

Recommendation

Definition of Acronyms

For Further Reference

Question

“Under the Hood” Information

Group Exercise