Ben Cohen **ben@systemverilog.us**

PAPERS

1 Understanding the SVA Engine Using the Fork-Join Model

https://verificationacademy.com/verification-horizons/july-2020-volume-16-issue-2

Using a model, the paper addresses important concepts about attempts and threads. Emphasizes the total independence of attempts.

2 Reflections on Users' Experiences with SVA, part 1

https://verificationacademy.com/verification-horizons/march-2022-volume-18-issue-1/reflections-on-users-experiences-with-systemverilog-assertions-sva

Important concepts on EXPRESSING REQUIREMENTS,
Terminology, threads in ranges and repeats in antecedents, multiple antecedents.

3 Understanding Assertion Processing Within a Time Step

https://systemverilog.us/vf/Understanding_assertion_processing.pdf

This paper goes into detail about how evaluation regions should be handled by a simulator as described in the SystemVerilog LRM; this should give you a better understanding of how assertions work.

4 Reflections on Users' Experiences with SVA, part 2

https://verificationacademy.com/verification-horizons/july-2022-volume-18-issue-2/reflections-on-users-experiences-with-sva-part-2

Addresses the usage of these four relationship operators: throughout, until, intersect, implies

5 Understanding and Using Immediate Assertions

https://verificationacademy.com/verification-horizons/december-2022-volume-18-issue-3/understanding-and-using-immediate-assertions

Provides guidelines

6 SVA Package: Dynamic and range delays and repeats

https://rb.gy/a89jlh Provides a library and model solutions

7 SUPPORT LOGIC AND THE always PROPERTY

http://systemverilog.us/vf/support_logic_always.pdf

Provides examples of support logic needed for certain types of requirements where the strict use of only SVA does not cover.

8 SVA in a UVM Class-based Environment

https://verificationacademy.com/verification-horizons/fFebruary-2013-volume-9-issue-1/SVA-in-a-UVM-Class-based-Environment

Explains how SVA complements a UVM class-based environment. It also demonstrates how the UVM severity levels can be used in all SVA action blocks instead of the SystemVerilog native severity levels.

 # BOOKS

1 SVA Handbook 4th Edition, 2016 ISBN 978-1518681448 https://rb.gy/4abc8v

* Addresses 1800'2017 SVA as a language and applications with many examples
* Authored by Ben Cohen; Srini Venkataramanan, a formal employee of Intel and Synopsys, now independent and also a Siemens partner; Lisa Piper, a tool maker at Cadence Design Systems.
* Forewords by Dennis Brophy (Mentor), Sven Beyer (OneSpin), Stuart Sutherland (HDL trainer), Cristian Amitroaie (AMIQ)
* Four editions of this book, with the 1st edition translated into Japanese by Cadence
* Available in ebook and hard copy

2 A Pragmatic Approach to VMM Adoption … a SV Framework for Testbenches 2007

* Authored by Ben Cohen; Srini Venkataramanan
* First book demonstrating by example the application of VMM, a precursor to UVM
* Forewords by Janick Bergeron (Synopsys), Stuart Sutherland (trainer), Scott Sandler (Novas)
* Book is donated to the public. has lots of sample code usable in any class-based methodology.

http://SystemVerilog.us/vf/VMM/VMM_pdf_release070506.zip
http://SystemVerilog.us/vf/VMM/VMM_code_release_071806.tar

3 Real Chip Design and Verification Using Verilog and VHDL($3) https://rb.gy/cwy7nb

* Addresses fundamentals in design and verification for junior engineers (types of registers, counters, memories and EDAC, metastability, transaction-based verification, control machines with FSM and microcode, arithmetic machines, synthesis.
* If a design engineer does not understand these concepts he/she should look for a different career.
* Forewords by Rahul Razdan (Cadence), Andrew Dauman (Sinplicity).
* Ebook donated for $3 https://rb.gy/cwy7nb

Recommended for those who lack the fundamentals of design and verification.

4 Component Design by Example … A step-step process using VHDL with UART as vehicle

https://rb.gy/9tcbhl By example, book specifies how to write:

* Requirement specification
* Architectural plan
* Verification plan
* Documentation and delivery
* Use of OpenMore Assessment Program Spreadsheet
* Readers should concentrate on the processes, and ignore any VHDL code; processes need to be extended as needed, but the core structure is there.
* Recommended reading, particularly because many SVA coders misunderstand and do not express in English the requirements. It's the GIGO issue.

5 Using PSL/Sugar with Verilog and VHDL

* Two editions, Translated to Janapese by Cadence

* Recommended by Harry Foster (Accellera PSL) and Rahul Razdan (Cadence)
* This book is now passe, but was a baseline for SVA

6 VHDL Coding Styles an Methodologies ... an in-depth tutorial
* Two editions :1995, 1999
* Addresses the language through examples
* Addresses verification using a transaction-based approach
* Book is still sold in Europe, good for vhdl users

7 VHDL Answers to Frequently Asked Questions
* Two editions
* Book evolved from the many questions and issues addressed on the comp.lang.vhdl forum
* Book is still sold in Europe, good for vhdl users