Q1) Convert D-FF into divide by 2.
What is the max clock frequency the circuit can handle, given the following information?
T_setup= 6nS
T_hold = 2nS
T_propagation = 10nS

Answer: Q1
Divide by 2
Qbar is connected to D input , Clock to be divided goes on to CLK input. We tap the input from Q output.
The max frequency is 1/16nS

Q1: Ans
Circuit:
Connect Qbar to D and apply the clk at clk of DFF and take the O/P at Q. It gives freq/2.
Max. Freq of operation:
1/ (propagation delay+setup time) = 1/16ns = 62.5 MHz

Question(2)
Why do we gradually increase the size of inverters in buffer design when trying to drive a high capacitive load? Why not give the output of a circuit to one large inverter
Ans(2)
We cannot use a big inverter to drive a large output capacitance because, who will drive the big inverter? The signal that has to drive the output cap will now see a larger gate capacitance of the BIG inverter.So this results in slow raise or fall times .A unit inverter can drive approximately an inverter thats 4 times bigger in size. So say we need to drive a cap of 64 unit inverter then we try to keep the sizing like say 1,4,16,64 so that each inverter sees a same ratio of output to input cap. This is the prime reason behind going for progressive sizing.

Q(3) Why don't we use only an NMOS or a PMOS in a Transmission gate?
Ans(3)
Using only an nmos will result in an poor 1. Why is it so? Assume the gate voltage on NMOS is 5V. If we connect Drain to 5V, and the source is initially at 0, NMOS will turn on as long as there Vgs >Vth, this means, once the source reaches 4.3V (Assuming Vth=0.7), the nmos will turn off and there will be no more increase in source voltage.Similarly the opposite happens with PMOS, it doesn't give us a clean 0, but it can give a full 5V. So we use a combination of both NMOS and PMOS so that our signal doesn't get degraded by Vth on either side of VDD and GND.

ANSWER : Q3
PMOS degrades Logic 0 & NMOS degrades logic 1
To restore the logic levels to full, both NMOS & pMOS will be used together in TG

Question(4)
Is there in Hold violation in the Circuit of Q1?
Describe clearly when there will be Hold violation wrt to the given data and how we can solve it in circuit level?

Answer(4)
There is no hold vioaltion in the given circuit. As the hold time is less than the propagation delay.
Otherwise buffers(even number ofinverters) will be used in the feedback path in order delay the feedback reaching back the input.

Q(5)
In CMOS technology, in digital design, why do we design the size of pmos to be higher than the nmos.What determines the size of pmos wrt nmos. Though this is a simple question try to list all the reasons possible..

Ans(5)
In PMOS the carriers are holes whose mobility is less[aprrox half] than the electrons, the carriers in NMOS. That means PMOS is slower than an NMOS. In CMOS technology, nmos helps in pulling down the output to ground ann PMOS helps in pulling up the output to Vdd. If the sizes of PMOS and NMOS are the same, then PMOS takes long time to charge up the output node. If we have a larger PMOS than there will be more carriers to charge the node quikly and overcome the slow nature of PMOS . Basically we do all this to get equal rise and fall times for the output node.

Why PMOS and NMOS are sized equally in a Transmission Gates

In Transmission Gate, PMOS and NMOS aid each other rather competing with each other.
Thats the reason why we need not size them like in CMOS.
In CMOS design we have NMOS and PMOS competing which is the reason we try to size them proportional to their mobility.

Q(6)
How many unique boolean fucntions can be there for **n** number of inputs?

Ans(6)
Number of unique boolean function for n variables is 2^(2^n).
I did this by taking n=1,2 and applied the theory of induction. Srikanth, If you can explain it ,would be great... A good question this one, since at first look I thought the answer to be 2^n....

Ans (6)

For n number of inputs, the possible number of min terms or max terms, k = 2^n
To form any bollean function, we can take any combination of these.
So possible boolean functions = kc0 + kc1 + kc2 ...+kck = 2^k = 2^2^n

Q7
Design a sequential circuit which cuts the every second pulse from the input(clk)?
Hint: If we think in other way, it is nothing but frequency devider by 2 , But with 25% Duty cycle!!!

A7)
First do a Divide by 2 counter, ie connect Qbar to D input of FF.
Connect the Q output and CLK to a 2 input AND gate, this will gives us a divide by 2 clock with 25% duty cycle.

Ans 7
First do a Divide by 2 counter, ie connect Qbar to D input of FF.
Connect the Q output and CLK to a 2 input AND gate, this will gives us a divide by 2 clock with 25% duty cycle.
Explanation:
When we are solving this type of Qs, we should try to draw the input and Output waveforms and try to obtain some relation between them. Suppose in Q7 only first part is given, you can draw the waveform with 25% Duty cycle and then start trying to corelate it with any of the familiar waveforms like is it some counters o/p or sthg or obtained by doing some basic operations etc....Once we start think in that way, we should be able to get some idea
But for this, lots of practise is required

Question8
Design all the basic gates(NOT,AND,OR,NAND,NOR,XOR,XNOR) using 2:1 Multiplexer.

Using 2:1 Mux, (2 inputs, 1 output and a select line)
(a) NOT
Give the input at the select line and connect I0 to 1 & I1 to 0. So if A is 1, we will get I1 that is 0 at the O/P.
(b) AND
Give input A at the select line and 0 to I0 and B to I1. O/p is A & B
(c) OR
Give input A at the select line and 1 to I1 and B to I0. O/p will be A | B
(d) NAND
AND + NOT implementations together
(e) NOR
OR + NOT implementations together
(f) XOR
A at the select line B at I0 and ~B at I1. ~B can be obtained from (a)
(g) XNOR
A at the select line B at I1 and ~B at I0

Q9
N number of XNOR gates are connected in series such that the N inputs (A0,A1,A2.....AN-1) are given in the following way:
A0 & A1 to first XNOR gate and
A2 & O/P of First XNOR to second XNOR gate
and so on..... Nth XNOR gates output is final output. How does this circuit work? Explain in detail?

Ans9
If N=Odd, the circuit acts as **even parity detector**, ie the output will 1 if there are even number of 1's in the N input...This could also be called as **odd parity generator** since with this additional 1 as output the total number of 1's will be ODD
If N=Even, just the opposite, it will be Odd parity detector or Even Parity Generator...

N = odd, it acts as XNOR(odd parity generator) if N = even, it acts as XOR(even parity generator).

Can any one explain me the significance of current mirror?
Current mirrors are the most widely use analog circuit. Most of the transistors in an analog integrated circuit are parts of current mirrors.
Various Applications:
1. Current mirrors are used as current sources in ICs. An ideal current source has an infinite output impedance. That is, the output current does not change, even for large swings in output voltage. delta I/delta V = 0. That's high impedance.
2. The current mirroes are used for biasing and as loads in case of Amplifiers. A current source is equal to a very high resistive load(as mentioned in 1), If u use the same value resistor, it occupies too much of the area.
A typical current mirror cicuit can be designed by using either BJTs or MOSFETs

Q10)
All of us know how an inverter works. What happens when the PMOS and NMOS are interchanged with one another in an inverter

Answer:Q10
If the source & drain also connected properly...it acts as a buffer.
But suppose input is logic 1 O/P will be degraded 1
Similarly degraded 0;

Q11)
Give 5 important Design techniques you would follow when doing a Layout for Digital Circuits

Q12)
What is Latch Up? How do you avoid Latch Up?

Answer:Q12

Coming to latchup problem,
If you look at the cross cectional view of any inverter, there is a positive feedback between a NPN and PNP transistor which results in latch up problem.This positive feedback results in excessive current which ultimately destroys the device. These NPN and PNP transistors are formed from the p+/n+ source/drains, p/n well and substrates.

As mentioned the NPN & PNP transistors form a triode & whose charecterstics demand high current,,,it damages the circuit,,,
One of the solution to avoid this is : Usage of Gaurd rings.

Q13)
Implement the following circuits:
(a) 3 input NAND gate using min no of 2 input NAND Gates
(b) 3 input NOR gate using min no of 2 inpur NOR Gates
(c) 3 input XNOR gate using min no of 2 inpur XNOR Gates

Answer: Q13

Assuming 3 inputs A,B,C
3 input NAND:
Connect :
i) A and B to the first NAND gate
ii) Output of first Nand gate is given to the two inputs of the second NAND gate (this basically realises the inverter functionality)
iii) Output of second NAND gate is given to the input of the third NAND gate, whose other input is C
((A NAND B) NAND (A NAND B)) NAND C
Thus, can be implemented using '3' 2-input NAND gates. I guess this is the minimum number of gates that need to be used.
3 input NOR:
Same as above just interchange NAND with NOR
((A NOR B) NOR (A NOR B)) NOR C
3 input XNOR:
Same as above except the inputs for the second XNOR gate, Output of the first XNOR gate is one of the inputs and connect the second input to ground or logical '0'
((A XNOR B) XNOR 0)) XNOR C

Q14:
An assembly line has 3 fail safe sensors and one emergency shutdown switch.
The line should keep moving unless any of the following conditions arise:
(i) If the emergency switch is pressed
(ii) If the senor1 and sensor2 are activated at the same time.
(iii) If sensor 2 and sensor3 are activated at the same time.
(iv) If all the sensors are activated at the same time
Suppose a combinational circuit for above case is to be implemented only with NAND Gates.
How many minimum number of 2 input NAND gates are required?

ANS: 14
No of 2-input NAND Gates required = 6

Q15:
What is race-around condition? Explain in it in case of R-S Latch and solution to avoid that?

Ans: 15
The race around conidtion is : O/P osciallting between 0s & 1s.
This problem will occur in Latches especially if the clock is high for long time.
I can explain in case of J-K Latch
Suppose J=K=1 & O/P = Compliment of prev state (Q(t+1) = Q(t)')
So as far as clock is high, O/P oscialltes between 0 & 1
To avoid this,
they use Master-Slave configuration

Q16:
What is metastability? When/why it will occur? Different ways to avoid this?

Ans : Q16
Metastable state: A un-known state in between the two logical known states.
This will happen if the O/P cap is not allowd to charge/discharge fully to the required loigcal levels.
One of the cases is: If there is a setup time violation, metastability will occur,
To avoid this, a series of FFs is used (normmly 2 or 3) which will remove the intermediate states.

the metastability will occur if there is any timing violations. That means we are not allowing the cap to charge/discharge to the full level. We are clocking at some intermediate level. So the O/P will go to metastable state..and slowly comes back to any of the valid levels,bcoz of some flickering. So we are actually increasing the propagation delay of the FF. So if we use one more FF , The output from the first flip flop may go valid, before the second flip flop is clocked. Adding yet another flip flop will reduce the probability that its output will be unstable even more

Q17:
Give the basic schematic of Set-Reset Latch with NOR gates. Explain the functionality with truth tables. Which input combination is not allowed.
Change the same to provide clock enable.
Try with NAND gate also. Which I/P combination is not allowed?

Some notes on S-R Latch:
Latches
How can we make a circuit out of gates that is not combinatorial? The answer is feed-back, which means that we create loops in the circuit diagrams so that output values depend, indirectly, on themselves. If such feed-back is positive then the circuit tends to have stable states, and if it is negative the circuit will tend to oscillate.
A latch has positive feedback. Here is an example of a simple latch:
This latch is called SR-latch, which stands for set and reset.

It is not practical to use the methods that we have used to describe combinatorial circuits to describe the behavior of the SR-latch. Later, we will show a method for describing flip-flops and clocked sequential circuits. For now, we just rely on our intuition to describe how latches work.
The SR-latch is meant to have at most one of its inputs equal to 1 at any time. When both of its inputs are 0 it has two different stable states possible. Either x is 0, in which case we have the following signal values:
or else x is 1, in which case we have the following signal values:
The actual value depends on the history of input values as we will show next.
Now suppose that s is 1 (and therefore r is 0 since we allow at most one input to be 1 at any time). We get the following signal values:
The 1 on the s input makes sure the output of the upper nor-gate is 0, and the two 0s on the input of the lower nor-gate make sure the x output is 1.
Now suppose the s input goes from 1 to 0, while the r input remains at 0. The second input of the upper nor-gate is 1, so the transition from 1 to 0 of the s input, does not make any difference. The x output remains at 1. In this case, if the s and r inputs are both 0, there is only one possible stable state, the one that gives x the value 1.
Conversely, suppose that r is 1 (and therefore s is 0 since we allow at most one input to be 1 at any time). We get the following signal values:
The 1 on the r input makes sure the x output is 0, and the two 0s on the input of the upper nor-gate make sure the output of the upper nor-gate is 0.
Now suppose the r input goes from 1 to 0, while the s input remains at 0. The second input of the lower nor-gate is 1, so the transition from 1 to 0 of the r input, does not make any difference. The output of the upper nor-gate remains at 1. In this case, if the s and r inputs are both 0, there is only one possible stable state, the one that gives x the value 0.
From the discussion above, we conclude that the SR-latch is able to remember the last state of the inputs, in the sense that it remembers which of the two inputs, s or r, last had the value of 1.

Q18:
Give the state machine for a serial two's complimenter? Then design the complete circuit using DFF?

Hint: If you observe a binary number and its 2's compliment, the 0s will be retained until the first 1 occurs (from LSB side) and the first 1 also will be retained after that compliment all the follwoing bits.
It is very interseting & simple Qs to check the knowledge of state M/Cs

Answer:Q18
The state M/C will have only two states. State A & B. Stay in State A as far as you are getting 0's and O/P is also 0. If 1 comes go to state B and O/P is 1.
If you are in state B, whether I/P is 1 or 0 stay in B only and O/P is compliment of input.
State Table is as follows:

PS	x	NS	O/P
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

To obtain the circuit using DFF,
OR x & Q of FF and give at the I/P of FF
XORing of Q&x will give O/P(2's compliment)

Q19:
In a PLL, what elements(digital blocks) can be used to design the phase detector?

Ans: 19
1. XOR Gate
2. S-R Latch
3. PFD(Phase/freq detector) : It is designed from FFs & some NAND Gate COnnected to resetes)

Q20:
Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.

Answer:Q20

Assume state A : no heads has occured
state B: only one head has occured
state C: more than 2 heads has occured
So intial state is A

PS	I/P	NS	O/P
A	Tail	A	0
A	Head	B	0
B	Tail	A	0
B	Head	C	0
C	Tail	A	0
C	Head	C	1

Q21:
What is Moore model & Mealy model? Explain.

Ans: Q21
A state machine consists of set of states, initial state, input symbols and transition function that maps input symbols and current state to next state.
Mealy machine: machines having outputs associated with transition of input and the current state. So in this case, the O/P will vary as soon as the input varies..O/P can't be held until clock pulses.
Moore machine: machines having outputs associated with only states. The O/P will vary only after the states are varied.So the cahgnes in the O/P will be only during clock transitions.
Adv & Disadv:
In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables.
Moore overcomes glitches as output dependent on only states and not the input signal level.
All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true.

Moore machine:
the outputs are properties of states themselves... which means that you get the output after the machine reaches a particular state, or to get some output your machine has to be taken to a state which provides you the output.
The outputs are held until you go to some other state
Mealy machine:

Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.

Q22)
How many minimum number of MOS transistors are required to implement a Full Adder using CMOS technology?

Answer:Q22
S = a xor b xor c
Cout = (a xor b) c + ab
Using these equations, we can implement,,,exact count of MOS transsitors is straight forward..
Note XOR can be implemented with only 4 2 input NAND Gates...

Q23:
(a) Show all the possible ways to convert a 2-input NAND Gate into an inverter?
(b) Show the implementaion of XOR Gate using minimum number of 2-input NAND Gates?

Ans: Q23:
(a) A 2 input NAND gate can be converted into an inverter in two ways: one way is by tieing up the two inputs and give the input, second give make one of the two inputs permanatly high and give the input at the other input.
(b) A XOR B = AB' + A'B = (AB)' A + (AB)' B
So one 2-input NAND is needed to generate (AB)' 3 other to implent the rest of boolean function. So total we need 4 2input NAND Gates.

Q24:
It is required to connect a Master, which generates data @ 200 Mega Samples/sec to a Slave which can receive the data @ 10 Mega Samples/Sec. If the data lost in 10Micro Sec, what is the optimal size of FIFO to be used to avoid lose of data?

Ans :Q24
(200-10) * 10 = 1900 samples is the size of FIFO
It is given that data will lost in 10micro sec otherwise, that is if data comes continuosly,fifo size will be infinity.

Q25:
The clock and the input output wavefroms are shown

Obtain OUT1 & OUT2 from the INPUT.

ANS: Q25
The answer is shown in the following URL:

Explanation for Q25:
To solve this type of sequential problems, using synchronous methods, we should be having the input sampled @ clk. If that is not the case, it is our responsibilty to make it align to the clock.
If you observe the following waveforms, the [b]INPUT is not alinged with the rising edge of clock, So we will use one Flip flop to make it proper. So the purpose of the first flip flop, is to make the INPUT proper. In few cases this may not be required. Suppose if we are working with FSMs, the main assumption itself is the data is sampled @ clock.

Now to get the Output, of you observe OUT1 is changing at both the rising edge and falling edge of the input where as OUT2 is changing only at the rising edge. What this effectively mean is, OUT1 has to be 1 for one cycle, when the current sample and prev sample of INPUT are opposite whereas OUT2 will be 1 if the current input is 1 and prev is 0.
So toget prev sample...I have to store it...so need second flop...
So first flops o/p will give current value whereas second flops out will give prev value...
Using these to we build the combinational logic.[/img]

Q27:
Design a synchronous sequential circuit to check the highest number of ones and zeros in the last 3 input samples. Your ckt should give 1 at the O/P if the last 3 samples at the input has more 1's similarly 0 when the no. of zeros is high.
Eg:
IN : 001110110000
OUT: 0111111000
Constraints:
1) You are supposed to use only Multiplexers and DFFs for
your design. No external gates. To be specific, 1 4:1 Mux only.
2) Design should be optimized one.
3) Only one clock is available to you. And it is given that the
input is sampled at that clock rate only.

Q28 What is overflow? How can you detect overflow in signed and unsigned numbers?

Ans: Q28:
case1 : Unsigned numbers:
In N-bits, we can represent numbers from 0 to (2^N) - 1. Suppose if we are adding 2 N bit unsigned numbers and if the result is greater than (2^N) - 1 , overflow will occur. To detect this, check whether the MSB addition (Nth bit) + Carry generated from N-1bit addition is genrating any carry or not. If there is carry out, there is overflow.
case2 : Signed numbers:
In N-bits, we can represent numbers from -(2^(N-1)) to (2^(N-1)) - 1. Suppose if we are adding 2 N bit signed numbers and if the result is not in the above range , overflow will occur.

To detect overflow in this case : if two numbers with the same sign (either positive or negative) are added and the result has the opposite sign, an overflow has occurred.

two more cases in case of signed...
So overall, the conidtions to detect overflow are here again:
In unsigned arithmetic a carry out of the most significant digit means that there has been an overflow
A signed overflow has occurred in an addition or subtraction if:
* the sum of two positive numbers is negative;
* the sum of two negative numbers is positive;
* subtracting a positive number from a negative one yields a positive result; or
* subtracting a negative number from a positive one yields a negative result.

Overflow detection:
Unsigned numbers: In unsigned numbers, overflow is detected when the carry flag is set. Or in other words, carry is generated at MSB or if there is a borrow onto the MSB.
Signed numbers: In signed numbers, overflow is detected when
case 1: When numbers of like signs are added, result has a different sign.
case 2: When carry out of sign position is not equal to the carry in of sign position.

Q29:
Give the circuit to extend the falling edge of the input by 2 clock pulses. The waveforms are shown in the following figure.

Ans:Q29

Q30)
(a) Draw a Transmission Gate-based D-Latch.
(b) Design a Transmission Gate based XOR. Now, how do you convert it to XNOR? (Without inverting the output)

NOTE on TG: Transmission Gate has one NMOS & one PMOS (pass transistors). In the symbol bubble indicates PMOS and other side is NMOS. To select TG, We need to give 0 to PMOS and 1 to NMOS. In this case whatever is there at the input will be connected to the output. In the other case, that is 0 is given NMOS and 1 is given to PMOS, output will be just hanging. We need keep these things in solving TG based problems. The answers to above mentioned problems will be updated shortly.

Q30:Part(a) Solution:
TG Based D-Latch....

Q30: Part(b) Ans:

XOR Using TG..

If we observe the truth table of XOR, if A is 1, O/P is !B and if A is 0 O/P is B. Using this, we can implement the following circuit.

To get XNOR, just connect B directly to bottom TG and !B to the upper TG.
NOTE: Similarly we can try all other basic gates also like AND,OR,NAND,NOR etc. Just practise them yourself.

Q31,Q32,Q33:

Design the Digital Circuit which gives
(Q 31) fout = (1/2) fin
(Q 32) fout = (1/3) fin
(Q 33) fout = (2/3) fin (3 different circuits)
NOTE:
(a) fout is O/P freq and fin is I/P freq
(b) Duty cycles are also not mentioned..so its okay to design for any duty cycle.
(c) All the ckts design using DFFs and min no of external gates
Show all the waveforms also.....

Solution to Q31: That fout = fin/2

The follwoing figure shows the waveforms and the circuit to give freq/2.
It is simple and straight forward. It shows 50% duty cycle. To get 25% duty cycle, we need to use the circuit shown in the solution of Q7 (refer to page 4 of KSF). To get freq/4 use the same ckt twice. But that will be asynchronous as the clock to both flops is not same.

Solution: Q32:

fout = fin/3

In the above problem, if you observe the waveforms(shown below) , they are synchronous. So we can use FSM to design the circuit. If you observe the waveform clearly, output is 100,100,100 and so on Assume 3 states: a,b & c. In a O/P is 1 and then go to b in b O/P is 0 and then go to c in c O/P is 0 and then go to a. That is

PS NS O/P
a b 1
b c 0
c a 0

Using this and assigning 00-a,01-b and 10-c we can design the follwoing circuit.

Note on Q32:
The above circuit gives a duty cycle of 1/3rd (that is 33.333)
To get 2/3rd(that is 66.667) , use NAND gate instead of NOR gate

Solution Q33:

fout = 2 * (fin/3)
The clue to get the solution is: There is a transition at the falling edge of clock. So the clock to the second flop is inverted one. And we can't use normal FSM now. So need use some analysis to get the O/P. It is not straight forward.
One more observation is, the waveforms shown in the above figure, fout has a duty cycle of 1/3rd To get 2/3rd duty cycle, replace NOR gate with NAND gate in the design.

Q34:
You are given a 2:4 decoder. 2 input OR gate and one 3 input OR gate. Using these Components design the following system whcih takes A & B as inputs and generates the 4 O/Ps : AB, (AB)' , A+B, (A+B)' .

Ans: Q34:
2:4 decoder will have 4 O/Ps which are the minterm/maxterms of the 2 inputs. So the O/P are AB, AB', A'B, A'B'. So AB and (A+B)' = A'B' are directly the O/P s of decoder. Whereas A+B can be obtained using 2 input OR gate(which is given). So only O/P that is needed is (AB)' = A' + B' = A(B+B') + B(A+A') = AB' + A'B + A'B'. That is , use 3-input OR gate for this. The whole design is shown below.

Q35:
The following digital circuit shows two flops with a logic delay (dly1) in between and two clock buffer delays (dly2, dly3). Derive the conditions in terms of (dly1,dly2,dly3) to fix setup and hold timing violations at the input of second FF?
Tcq -- Clock to Q delay, Tsu -- Setup time and Th -- hold time.

The above waveforms show the CLK, CLK1 and CLK2. The input waveform at FF1 is assumed and the input of FF2 is shown accordingly with all the given delays and clock-to-Q delays. From the waveforms it is clear that, to avoid setup time violation,
T >= (Tsu2 + Tcq1 + dly1 - delta) where delta = dly2-dly3 (assuming +ve skew) ---> (1)
From this equation we can get maximum freq of operation.
To avoid hold time violation,
Th2 <= Tcq1 + dly1 delta ---> (2)
These two equations can be used as generalized equations to solve setup time/hold time problems. This works only for synch circuits. If one clock works at pos edge and other is negative edge we need to derive one more set of equations. That also we will at later section.

Q36:

(a) For the Circuit Shown above, What is the Maximum Frequency of Operation?

(b) Are there any hold time violations for FF2? If yes, how do you modify the circuit to avoid them?

Ans36
The minumum time period = 3+2+(1+1+1) = 8ns
Maximum Frequency = 1/8n= 125MHz
There is a hold violation in th ecircuit.You can avoid it by giving the input to the AND gate through two inverters.

Ans: Q36
In this diagram,
dly3 = 0
dly2 = 2ns
so,delta = 2ns
tsu2 = 3ns, tcq1 = 2ns, dly1 = 5ns
Putting all these values in Eq(1) ,
T >= Tcq1 + dly1 + Tsu2 - delta
so, T >= 2 + 5 + 3 - 2, T >= 8ns, f <= 1/8
Max freq of operation is 125MHz
And there is a hold time violation in the circuit, bcoz of feedback,
if you observe, tcq2+andgate delay is less than thold2,To avoid this as mentioned in Q1 we need to use even number of inverters(buffers).
Here we need to use 2 inverters each with a delay of 1ns. then the hold time value exactly meets.

Q37:

If both the flip flops have same clock-to-Q delay of 2.5ns,setup time of 2ns and a hold time violation of 1ns, what is the maximum frequency of operation for the circuit shown above?

The hold time doesn't effect your max frequency. We use the hold violoation to chek if there would be a race through shortest path.If there is a hold violation we try to fix it by introducing additional delay blocks like a buffer in the fastest path
Holdtime violation doesn't effect amx freq of operation
But regarding "dly" in Q37, you have to fix the value of that "dly" such that first there is no hold time vioaltion in the circuit.
Then you can use that value to find max freq.
But if that value if fixed, we can't do anything, in that case, we need to find other ways to avoid hold vilation.
But if varying that is possible, we can fix the value such that ther won't be any hold time vilations

Q38)
A simple question...
What is meant by CMOS Design ?

Ans38
CMOS design means complimentary metal oxide semiconductor design which involves the use of CMOS and PMOS in realizing the logic design. This is the dominant technology now a days because of its ten fold reduction of power dissipation which outweighs 30-50% speed reduction and size increase

Q39) Two NMOS transistors are connected in series. The gate of each transistor is connected to 5v and the drain of one transistor is connected to 12v. What is the voltage at the other end of the transistor if the threshold voltage of each is 1v?

Answer:Q39
The output voltage is 4V.
Consider a single NMOS as a switch.
The max voltage at the other end can reach max of VG - Vt, after that NMOS will be off.
So if the voltage at one end is less than VG-Vt it passes that value to the other end, but if it is more, it reaches VG-Vt at the end and stops there bcoz after that the MOS switch will be off.
So in this case, first NMOS which has 12v, at the input, gives 4v out at its source, the other Transistor which has 4v at the input transmits samething to the other end as it is.

Q40) Here is an interesting design question. There is a room which has two doors one to enter and another to leave. There is a sensor in the corridor at the entrance and also there is sensor at the exit. There is a bulb in the room which should turn off when there is no one inside the room. So imagine a black box with the inputs as the ouputs of sensors. What should the black box be?

You can assume at the maximum there will be 200 people. Or you can realize the black box logically means what it can be?.

Answer:Q40
The black box can be an up/down counter which can count number of people inside.
For 200 people, we need 8 bit counter.
So The O/P of entrance sensor will be used as enable for UP count and the other sensor at exit will be used for DOWN count, whenever the counter's O/P is 0, we can make the BULB OFF, Otherwise ON.

Q41) Design a 2 bit up/down counter with clear.

Q42)
Derive setup time/hold time vilation equations for the follwoing circuit? Assume Tcq1 Clock to Q delay, Tsu1 -- Setup time and Th1 hold time for first FF and similarly Tcq2,Tsu2,Th2 for second FF.

Ans:Q42:
Setup time :
(T/2) + delta >= Tcq1 + dly1 + Tsu2
Hold time:
Th2 <= delta + Tcq1 + dly1
where delta = dly3 - dly2, assuming positive skew
and T is clock period.
Note: The procedure is same as that of Q37.Just draw the waveforms with proper delays, you will get above equations.

Q43:
Design a D-latch using
(a) using 2:1 Mux
(b) from S-R Latch

Ans:43:
(a) D-latch using 2:1 Mux

(b) D-Latch from S-R Latch

Q44:
Suppose A & B are two unsigned n-bit numbers, how many minimum number of bits required for Y = A + B + (A*B). Here + is for addition and * is for multiplication. All are unsigned operations only.

Ans44) We need 2n bits for the operation. Take n=1,2,3,4 and take the maximum n-bit number and calculate Y , we end up with 2n bits for it

Ans:44)
In n bits, the maximum number is 2^n - 1.
So maximum value for Y is
(2^n - 1) + (2^n - 1) + (2^n - 1) (2^n - 1) = 2^2n - 1
So the number of bits required for Y are 2n

Q45:
(a) Give the truth table of a Half Adder?
(b) Design a full adder from HA's? (You can use Min no. of external gates)

Ans:Q45:

Q46:
(a) How will you count the number of 1's that are present in a given 3-bit input using full adder?
(b) If input is a 7-bit vector, how many minimum number of full adders are required to count the number of 1s?

Q47) Came across this question from a friend.
Design a circuit that calculates the square of a number? It should not use any multiplier circuits. It should use Multiplexers and other logic.

A47)This is interesting....
1^2=0+1=1
2^2=1+3=4
3^2=4+5=9
4^2=9+7=16
5^2=16+9=25
and so on
See a pattern yet?To get the next square, all you have to do is add the next odd number to the previous square that you found.See how 1,3,5,7 and finally 9 are added.Wouldn't this be a possible solution to your question since it only will use a counter,multiplexer and a couple of adders?It seems it would take n clock cycles to calculate square of n.
Let me know if my thinking is correct.

Q52) What is the basic difference between Analog and Digital Design?

Q53) What is difference between Static Logic and Dynamic Logic
Ans53
Static logic is when you provide a low resistance path from VDD or GND to the output.
Basically in static logics the output is pulled high or low through a low resistance path
In case of Dynamic logic, as you sais an intermediate node is charged uo or down and that state is maintained via high impedance path...

Q54) In CMOS deisgn, given a choice between implementing a logic in NOR and NAND implementation, which one would you prefer and why?

Ans 54. If it is a complementary CMOS Nand is preffered over NOR as NOR has PMOS in series which slows it down.
If it is a pseudo-NMOS, NOR is preferred as it has Transistors in parallel.

Q51....can anybody explain in detail about +ve hold time and -ve hold time.I get quite confused with this always

Hold and Setup times.. by their very definition are positive (for a single flop). But when we talk about timing constraints of two different synchronizing flops and its data signal transition between them...we face these questions on negative setup and hold times...
A51:

Hold time can be negative meaning that data can be changed even before clock edge and still previous value will be stored
Negative hold time is existing particlarly in the case of **clock skew**.
Consider two FFs with a *clock skew* i.e FF1 lags behind FF2 and suppose FF1's output is fed to FF2's input passing through some logic cloud (or directly) *then* by the time FF1 is active the FF2 would have done its sampling the FF1's output.. there by no violation of hold time.
Some information regarding negative and setup time that might be of interest to you..
-A **zero setup time** means that the time for the data to propagate within the component and load into the latch is less than the time for the clock to propagate and trigger the latch.
-A **zero hold time** means either that the moment the clock is asserted, the latch no longer looks at its inputs, or else that the clock path delay is shorter than the data path delay.
-A *negative* **setup** or **hold time** means that there is an even larger difference in path delays, so that even if the data is sent later than the clock (for setup time), it still arrives at the latch first.

Q55) What are the conditions for obtaining worst case set up and hold times?

Q56) What are the advantages and disadvantages of static CMOS logic?

Ans56
Adv:
> Proper/Full logic levels
> O/P node is connected to either VDD/Gnd: no floating nodes
Dis ADv:
> needs constand voltage supply
> More power dissipation
if we compare to Dyanmic, static has the following disadvantages:
1. considerable time delay
2, Large number of transistors.

Q57:
Give the State Machine for detecting the sequence "1010" from a serially coming data for both (a) Overlapping & (b) Non-overlapping cases.

Ans Q57:
Part (a) Overlapping case

a --> cont zeros(intial state)
b --> 1 detected state
c --> 10 detected state
d --> 101 detected state

Ans Q57:
Part (b) Non-overlapping case

a --> cont zeros(intial state)
b --> 1 detected state
c --> 10 detected state
d --> 101 detected state
Note the difference between the two FSMs:

This one is going back to a fter detection of 1010 and where are in earlier case it is going to c that 10 detected state

Q58:
Sender sends data at the rate of 80 words / 100 clocks
Receiver can consume at the rate of 8 words / 10 clocks
Calculate the depth of FIFO so that no data is dropped.
Assumptions:
There is no feedback or handshake mechanism.
Occurrence of data in that time period is guaranteed but exact place in those clock cycles is indeterminate.

We we will follow the follwoing rules in uploading FSMs so that it will be easy to analyze the answers.
1) Always use small a,b,c.. to represent states...
2) And arrows to show the state transitions...
3) Show the **input/output** on the arrow.
A58) : In the worst case,sender would send 80 words in 80 clock cycles.In this time period,receiver would only be able to receive 8*8=64 words in those 80 clock cycles.Therefore FIFO size should be 16 words.

When I have solved it initially,even I have got the same answer.
But what we missed was, " the data may occur anywhere..
the sender may send the data in the last 80 clocks..of first 100 clocks and initial 80 clocks in the next 100 clocks.
So this is the worst case....

Ya Srikanth,now I realised that I erred in considering the 100 clock cycles in isolation....so is it a FIFO depth of 32 words

A58)As Srikanth pointed out,worst case is when 80 words come in the last 80 clock cycles of a 100 clock cycle period and 80 words come in the first 80 clock cycles of the next 100 clock cycle period.So now reduce the problem as to how the receiver will handle 160 words in 160 clock cycles.
Receiver can only receive 8 words in 10 clock cycles,so remaining 2 words would have to be stored in a FIFO.At the end of 20 clock cycles,receiver would have been able to receive 16 of the 20 words it was supposed to i.e 4 to be stored in the FIFO.Thus 2 additional words must be stored in every 10 clock cycle period.So for 16 of these 10 clock cycle periods,16*2=32 words would need to be stored in a FIFO.
Hope this was helpful rather than confusing matters further!

Q59:
A simple Qs to understand FSM flow.(asked in TIs apti test)
A state diagram is shown in the following figure: (States are named as Sa, Sb & Sc)

The system is initially in state Sa. If * represents zero or more occurrence of a logic level and + represents one or more occurrence of a logic level which of the following best describes the sequence of states the system could have gone through if it is finally in state Sc.
a) 0* --> 1+ --> 0 +
b) 0* --> 1* --> 1*

c) 0* --> 0* --> 1
d) 0+ --> 1+ --> 0*

A59
(a) 0* --> 1+ --> 0+
Reason: since '*' refers to atleast zero occurence and '+' refers to atleast one occurence of a specific logic level.. IN the worst case.. the following happens.. "1-->0"
so the..first occurence of '1' will take state Sa to Sb and next '0' takes to State Sc from Sb.
But the worst case in all other options is ..in(b) final state is Sa.. in (c) and (d) final state is Sb.
So the one that best suits the transition of state from Sa to Sc as final state is **(a)**

Q60:
One more intersting Q on FSM
What does the following FSM do?

One more CLue to solve this:
If you observe the state machine, it shows that the system retains 0 as it is and the first 1.
After one 1 has come, it compliments all the following bits.
Now you can guess the functionality...
One more thing...The data starts with LSB

ANSWER:Q60

The state diagram shows a serial 2's complemnter.

Q63:
What is ring oscillator? And derive the freq of operation?
A 63. Ring oscillator circuit is a coupled inverter chain with the output being connected to the input as feedback. The number of stages(inverters) is always odd to ensure that there is no single stable state(output value). sometimes one of the stages consists of a logic gate which is used to initialise and control the circuit.
The total time period of operation is the product of number of gates and gate(inverter) delay. And frequency of operation will be inverse of time period.(hope I have looked at the question in the right way)
Application: used as prototype circuits for modeling and designing new semiconductor processes due to simplicity in design and ease of use. Also forms a part of clock recovery circuit

Ans:Q63

The above diagram shows N number of inverters connected, where N should be odd number.
Let td be the delay of each inverter.
Total delay from in to out is , N * td
So half period = N *td
Freq of oscillation = 1/ 2 *N * td

Q65) Is it possible to use Even number of stages instead of Odd in the ring oscillator? If so how can you do it.

Ans65) We can use a differential inverter and in such case we can keep connecting the terminals criss cross(ie + - go to -+) .In this style we then need only even stages

Q66)How will you implement a Master Slave flip flop using a 2 to 1 mux?

Ans: Q66:

Q67:
Using DFFs and minimum no. of 2×1 MUXs, implement the following XYZ flip-flop.
X Y Z Qnext
0 0 0 1
0 0 1 0
0 1 0 0
0 1 1 1
1 0 0 Q
1 0 1 Q`
1 1 0 Q`
1 1 1 Q

Ans:Q67:
I could come with a solution of 3 2:! Mux and 1 DFF
If compliments are not availble, we need one more 2:! Mux for finding z'

Ans68)
Advantages of dynamic logic:
1. Less power consumption due to less capacitance because only pull up or pulldown network is available.
2.Faster because we have precharge phase, so need time for only evaluate phase.
3.Reduced transistors compared to static logic.
4.There is no short circuit current since pull up path is not turned on in evaluate phase.
Disadvantages:
1.The output node is dynamic node, ie high impedance node, there would be charge leakage and this might affect the logic after some time.
2.charge sharing between output node and internal nodes of pull down network
3.clock feedthrough is one more drawback. This casues the pn junctions of evaluate pmos to turn on when clock goes high.
4.Major drawback is , adds lot of load onto clock because precharge and evaluate transistors are connected to clock.

Q 69) How will you implement a Full subractor from a Full adder?

A subtractor should subtract subtraend from minuend. Subtraction is nothing but addition of the two's compliment of the subtraend.
2s compliment is negation of the number and adding 1 to it.
1st compliment can be implimented by xoring the subtraend with 1.
num Xor 1 = compliment of num.
Full subtractor can be implemented using a full adder in the following manner.
all the bits of subtraend should be connected to the xor gate. Other input to the xor being one.
The input carry bit to the full adder should be made 1.
Then the full adder works like a full subtractor.

Q69:
In what cases do you need to double clock a signal before
presenting it to a synchronous state machine?
A 69
When the signal is asynchronous (Probably coming from a different clock domain)

Q70)a)Why did you connect the bulk of NMOS transistor to source?
b)If the bulk of NMOS is connected to some voltage instead of connecting to source what will happen to the NMOS transistor?

Q71 What are the advantages of BJT over CMOS?

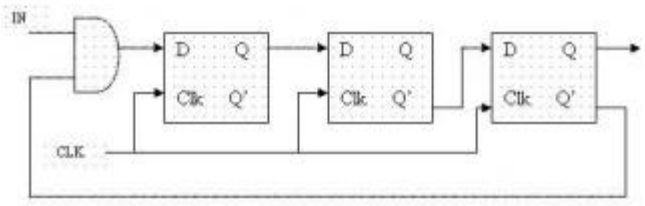
Q71) A very good interview question...
What is difference between setup and hold time. The interviewer was looking for one specific reason , and its really a good answer too..The hint is hold time doesn't depend on clock, why is it so...

Setup violations are related to two edges of clock, i mean you can vary the clock frequency to correct setup violation. But for hold time, you are only concerned with one edge and does not basically depend on clock frequency.

Q72:
You have three delay elements D1, D2, D3 that delay a clock by 25%,50% and 75% respectively. Design a frequency doubling (fout = 2 * fin) circuit that uses these delay elements along with any combinational logic.

ANSWER:Q72
we can double the frequency by just using the delay element D1 and an XOR gate. Just pass the input signal through D1. Now the delayed signal and the original signal are input to a 2-i/p XOR.

Q73:
What are all the test patterns needed at the input, IN, to detect Stuck at zero problem at the input of the first FF in the Following Figure? Assume that initially all DFFs are reset to logic 0.



Metastability means the O/P going to some intermediate state...
how it is related to Setup time:
Take a DFF. Assume that there is a transition at the input from 0-->1
It will take some considerable time to reach 1..(the duration is called rise time)
The O/P cap will starts charging slowly. But if we disturb the I/P in between,
the cap will stop at some intermediate point..if you tap the O/P from this point u will get some unknown state.. To avoid this...you should allow the I/P to charge to its full level..we shouldn't change it in between..This time is called Setup time...

Q74:I was given the layouts of a pmos device with one,two and three fingers.Which one offers better performance and why?(in terms of capacitance at the output node,on resistance and also power dissipation)Perhaps if someone could post a picture of such a layout it may help to think of the answer.
BTW,i was not able to answer the question but still I was offered the internship this afternoon
most of the other questions were on projects and a lot on digital circuits.i will try to post other questions as i remember them and when i have the time.

These stuck-at problems will appear in ASIC. Some times, the nodes will permanatly tie to 1 or 0..bcoz of some fault.
To avoid that, we need to provide..Testability in RTL.

If it is permanantly 1 it is called stuck-at-1
If it is permanantly 0 it is called stuck-at-0

Q77:
(a) Define: SOP from and POS form?
(b) When is a SOP/POS form is called standard or canonical?

Ans:

Any arbitrary logic function can be expressed as :
1) Sum-of-Products (SOP) - Example : AB+AC+BC
2) Product-of-Sums (POS) - Example : (A+B)(A+C)(B+C)

If each term in SOP or POS contains all the literals, then it is called a Standard or Canonical form SOP/POS.

Q78:
If F(A,B,C,D,E) = BE, how many terms will be there in the standard or canonical SOP representation of F?

Ans :

think there will be 8 terms.

BE=(A+!A)(C+!C)(D+!D)BE

Q79:
In C-N (Change-No change) flip flop, there won't be any change in output as far as N is 0, irrespective of C. If N=1, then if C = 0 output will change to zero else if C =1 output will be the compliment of previous output.
(a) Write the characteristic table ?
(b) Design this using J-K flip-flop?

Ans79:
a) Characteristic Table:

C N Q(t+1)
0 0 Q(t)
0 1 0
1 0 Q(t)
1 1 Q`(t)

b) Design:

J = C.N ; K = N; Q = O/P

STM questions:

I had my interview at STM.The following were the Qz asked

1. describe a CMOS
2.Describe the 5 regions of VTC

3.what is the difference between latch and flip-flop
4.given 2 latch's how will you convert into flipflop
5.why do we prefer flipflop to latch
6.draw a 4 bit counter
7.what is setup time and hold time
8.why do we require setup and hold times.
9.what is the difference between a combinational and sequential circuit.

1. CMOS means Complementary MOS design where i nwe use PMOS and NMOS as pull up and pulldown chains to provide low resistance path from output to VDD or GND. This style of design has good noise margins but requires more number of transistor. We have discussed this question in this thread...
   2.By VTC do you mean the Voltage Transfer Characteristics of Inverter.
   The five regions are when Vin = 0, 0-VIL , VIL-VIH, VIH-VDD, VDD
   VIL-VIH is the high gain region and digital design avoids working in this region whereas analog design embraces it

   3.Latch is level sensitive where as FF is edge sensitive

   4.We can build a Flip Flop from 2 latches by using Master Slave Configuration where in you give clock to one latch and inverted version of the clock to the other latch... sometihng like ur JK flipflop...

   5.Have 4 FF's .connect the outputs of one FF to the input of the next flip flop...This is a ripple counter..

   I will leave the last 3 questions to be answered by others, if no one doesn't shall answer them sometime later..I would encourage everyone to keep answering since it will help u a lot in the interviews...

7)Setup Time :Minimum time before the rising/falling edge of the clock for which Data should be stable.
Hold Time: Minimum time after the rising/falling edge of the clock for which Data should be stable.

Ans8) setup time models the time required for the data to propagate within the component and load into the latch before the latch is triggered by the clock.

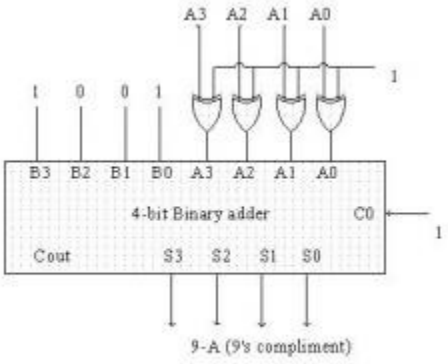
Hold time models the min time for which the latch looks at its input(after the clock is asserted). After the Hold Time inputs are locked, latch no longer looks at its inputs. Thus Hold time is used to avoid Race conditions.

Q80) How will u interface a 16-bit microprocessor to a 2 1-K RAM.Describe the read and write operations with the necessary signals?Guys this is a basic question asked in one of my interview.

Ans:

Q81)

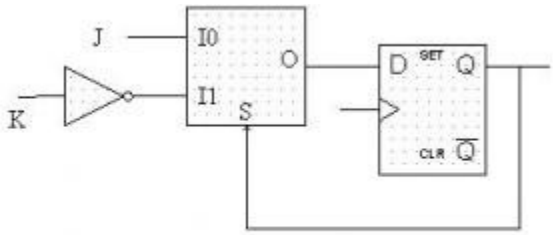
Design a circuit for finding the 9's compliment of a BCD number using 4-bit binary adder and some external logic gates.



Q82:

Design a J-K flip flop using DFF,2:1 Mux and an-inverter?

Ans:82:



Q83:

In a 3-bit Johnson's counter what are the unused states?

Ans83)

2(power n)-2n is the one used to find the unused states in johnson counter.

So for a 3-bit counter it is 8-6=2.Unused states=2.

Q.84 Could anyone through some light on Interconnect loss calculations such as due to skin effect, dielectric loss, reflection noise etc.? How this affects the transmitted waveforms? Equations for these losses (how they can be quantified?)

Q.85 Some basics on Interconnect pulse response and how to interpret it? How pre-emphasis is used to change the pulse response? Possible design issues with the pre-emphasis circuit.

q86) What is an LFSR .List a few of its industry applications.(Interview q for an internship)
Ans 86) LFSR is a linear feedback shift register where the input bit is driven by a linear function of the overall shift register value.

coming to industrial applications, as far as i know, it is used for encryption and decryption and in BIST(built-in-self-test) based applications..

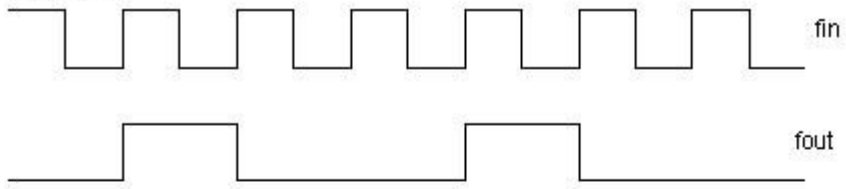
Q87

Design a divide by 3 clock. It was asked in one of my friends interview. I guess this has complex logic to it. In a phone interview how do you explain all that stuff, or is there a simple design for it..

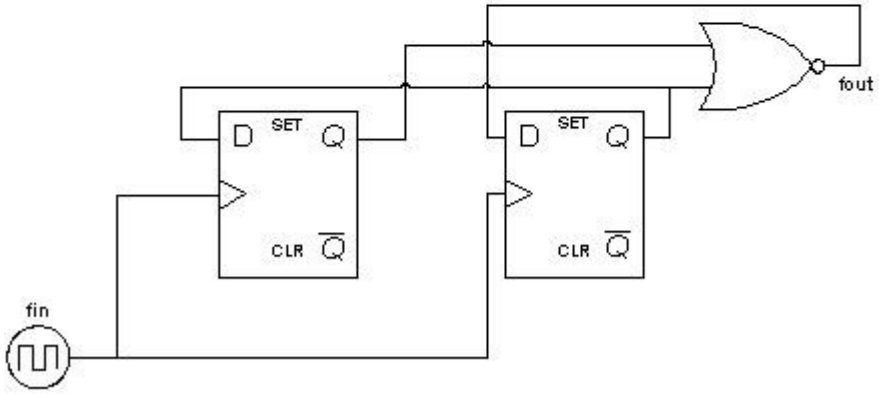
Solution: :
fout = fin/3
In the above problem, if you observe the waveforms(shown below) , they are synchronous. So we can use FSM to design the circuit. If you observe the waveform clearly, output is 100,100,100 and so on Assume 3 states: a,b & c. In a O/P is 1 and then go to b in b O/P is 0 and then go to c in c O/P is 0 and then go to a. That is
PS NS O/P
a b 1
b c 0
c a 0

Using this and assigning 00-a,01-b and 10-c we can design the follwoing circuit.

Waveforms:



Design:



here r 3 strategies for testing a circuit.
ad hoc techniques, scan based technique, and self-test techniques.
BIST(built in self test) is the self-test techniques
in this technique parts of the circuit are used to test the circuit itself.
BIST requires two circuit modules called
1. PRPG(pseudo random pattern generator)
2. ORA(output response analyzer)
these two modules can be built using LFSR.

Q.87
How do we design a 1Mb SRam? Give the architecture of the same?

88) Consider an alternate binary number representation scheme, wherein the number of ones M, in a word of N bits, is always the same. This scheme is called the M-out-of-N coding scheme. If M=N/2, and N=8, what is the efficiency of this coding scheme as against the regular binary number representation scheme? (As a hint, consider that the number of unique words represent able in the latter representation with N bits is 2^N. Hence the efficiency is 100%)

Ans) **Ans: Q88)**

If N=8, M=4

That is we have only combinations which has excalty 4 number of 1's

The possible binary combination in this number system = The 8 bit binary numbers which has exactly 4 number of 1s = 8C4 = 70

So eff = (70/256) * 100 = 27.34%

Q89)

2 bit gray code sequence (00,01,11,10) is coming serially. Design the circuit to detect the false sequence.

Q91

This is the one of the interiview question sireesha was asked for asic design job
there is a block with 3 i/ps. and 1 o/p
block is +ve edge triggered.
the conditions are
if reset=1,q=0,
else if set=1,q=1,
else q=q.

Ans91

First do the truth table for the conditions given
For R=1, and all other 4 combinations of S,Q(t) , Q(t+1) = 0
Now we need to fill the other 4 combo's left when R=0(y only 8 combinations , it is since we have only 3 variables giving 2^3=8 combos)
In this when S=1, irrespective of Q(t) , Q(t+1) = 1,
in other S=0, when Q(t) = 1, we have Q(t+1) =1...
draw the kmap and get the equation for Q(t=1)
This is what I get
Q(t+1) = Rbar[S+ Sbar*Q]

Q92

Does combinational circuits have setup and hold times???Why

how much maximum frequency clock i can apply to input of inverter having propagation delay Tpd ns?

Ans92

As a combination block, monitors continuously the changes of the input, there is no "clock" funda there.
The clock will come into picture in case of combination case,
1) If the inputs or/and the outputs are registered
or

2) If you are doing some combinational operation on the "clk" signal like gated clock etc.

Only thing is, the input should not change for a time period which is equal to the delay of combinational logic

This is my opinion...I am not sure whether I have answered right Qs or not...

Q: If two flip flops are cascaded together (o/p of 1st FF is given to the input of 2nd FF) and clock to the first FF is coming directly from clock source but it is inverted and sent to the second FF. Now, does this mean that the second FF is negative edge triggered or does it mean that second FF is positive edge triggered with a delay w.r.t 1st FF ?

Ans: Thats a good Question...
Just by the circuit we can not say anything about the flops..whether they are edge triggered or not.

Coming to this circuit,
If we assume both flip flops are positive edge triggered, there will be a delay of T/2 + inverter delay between the two flops. (T is the period of the clock)

If one of them is negative edge triggered, then between both clocks there is just inverter's delay.

So the one line answer to your Qs is : there is a delay between the two clcoks of the flops
We can't say second FF is negative edge triggerred or not

Q: Can a circuit have both setup and hold violations? Is it possible to have Setup and hold violations together on the same path?
ans 94)
hi jyothi..

I guess a circuit cannot have both set up and hold time violations together...

bcoz if there is setup time violation then for that data then the data is not at all sampled by the flip flop,so there wouldnt be any hold time for that data which is not sampled not any condition to violate.

and if there is hold time violation that means that data was successfully sampled...so there was no setup time violation.

So,answer for ure first part is not possible to ahve both set up and hold violations for a ckt at same time and for same data.

the second part also i guess it is possible.

95)

Given a 8 bit number how would you check whether it is a palindrome or not???..

Ans 95.
DO the XNOR of bits 1,8 ; 2,7; 3;6; 4,5
Then do an AND of the outputs of the 4 XNOR gates...
The output is 1 for the palindromes

q 96)A 4 bit shift register has _____ number of states.

q 97)Given/using a Positive Trigger as input generate Square wave.

Ans97)
You can use 555 timer to generate the necessary waveform but this can be done only for smaller frequencies...Any 555 timer data sheet shall give you the necessary info on how to do it.

q99)Swap two 8-bit registers without using another register.

Ans99)
Connect the registers as shift registers. Also connect the output of last register in set2 to the input of register in set1 and after 8 clock cycles you will have the register values swapped..Is there any other way venkat?

q100)In what cases do you need to double clock a signal before presneting it to a Synchronous machine?
A100:
If the signal is moving from one clock-domain to another,
that if the signal is asynchornous..
we need to double clock the signal.
The extra flop that is used for this purpose is called synchronizer.

This is a primetime funda.
Basic principle of flip flop is if your launch in t edge,it MUST be captured in t+1 edge.
Otherwise its race condition.
if you lauch in t edge,it SHOULD NOT be captured in t edge itself.
Its also a race condition.
you can call the first one max(setup) and second one min(hold) violation

Q101)You have a driver that drives a long signal and connects to an i/p device. At the i/p there is either overshoot or undershoot or signal threshold violations. What can be done to correct this problem?

Q 102 Why do we call as pmos passes good 1 & poor 0 and nmos passes good 0 and poor 1? please explain in detail.

Q 103)what are advantages of latch over flip flop?

Q104) how would u design 3 i/p NAND gate using 2no. of 2:1 muxes and 1 inverter? i know the answer, but let people try first then i will post the answer.

Q105:
List the differences between SRAM and DRAM?
Q106:
Match the following:
(a) PROM (i) Programmable AND Array and programmable OR array
(b) PAL (ii) Fixed AND array and programmable OR array
(c) PLA (iii) Programmable AND Array and fixed OR array

A 106)

(a)PROM -> Fixed AND array and programmable OR array
(b)PAL -> Programmable AND Array and fixed OR
(c)PLA -> Programmable AND Array and programmable OR array

Q 107) How do you count the no. of 1s present in an 8 bit register without using counter or adding bit by bit?
A107:
Full adder's output will be the number of 1's that are present in the input. Carryout as MSB and SUM as LSB. Observe the truth table.
So we need 2 full adders for 6 bits and one half adder for the remaning 2-bits.

The outputs of all these 3 adders are to be treated as 3 different 2 bit binary numbers and use 2-bit binary adders to get the final number.

In this approach, though we are using the adders, we are not adding them bit by bit.
However, please tell me whether this approach is correct or not
If it is correct, I can upload the complete design.
A 107

Divide the 8 bit no.(n) with the closest highest power of 2 which is greater than or equal to n. Now, again divide the remainder (if any) with the closest highest power of 2 which is greater than or equal to the remainder. Keep on performing iterations until remainder == 0. The no. of iterations is equal to the no. of 1s in the no. n.

Q108)

A D FF has its D i/p from a MUX. MUX input0 is connected to external i/p and MUXi input1 is connected to output of D FF (Q) through combo block(i.e: feedback of o/p to i/pthru combo block). If Mux delay is 0 ns and

Tsetup = 3ns, Thold = 2ns , TClock-to-Q = 1ns
What is the max frequency of the circuit with and without feedbak?

Ans108)

I got Tmin = 3+1=4ns for noi feed back case.but for the one with feedback dont u need the comdo logic delay time...
Coming to hold time violations, u need to give the max and min values for all the times u have mentioned. for hold violations we look at what happens if circuit is faster and for set up we think from all slow corners.

Ans:108:

Before going to the actual solution, I just want to mention one point about the given data. In the given data The hold time(2ns) is greater than the Clock-to-Q delay(1ns) of the flop.

That means the data is available at the output at 1ns after the clock edge but the input should not change till 2ns. It doesn't look logical for me.
For most of the flip flops, Thold is always less than TCq. This condition is essential for shift registers where as for circuits it may not be compulsory.
This Qs has two parts: (a) no feedback (b) feedback.

(a) If there is no feedback, that is assuming both external inputs and they meet the setup time of the flop, THe maximum clcok freq = 1/1ns

(b) If there is a feedback, to avoid hold violation, the "dly" has to be atleast 1ns. With violations there is no meaning for maximum freq. Becasue the circuit won't be functional at all.
So we have to take combo + Mux dly together >= 1ns. As MUx delay = 0, combo delay has to be 1ns.
Thold <= Tcq + dly, that implies, dly >= 1ns

T >= Tcq + combo_dly + Tsu = 1 + 1 + 3 = 5ns

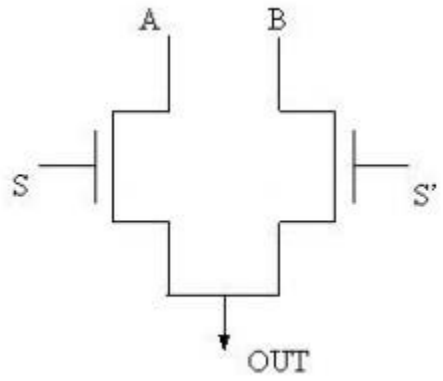
F <= 1/5ns

Q 108.

What is the source of set up and hlod time time violations ? what exactly happens inside the Flip-flops ? and What is inside the Flip-flope which makes it edge-triggering ?

Q110) impliment the full adder ckt. using 2:1 mux
and 2 i/p x-or gate? i think suresh and shrikanth
can look in to it. please send diagram also.
thanks in well advance.
Q 109. Explain Electromigration. (This Q was asked in Atmel interview)

Q111:
(a) What is the functionality of the following circuit?
(b) Show the boolean equation?
(c) What is name of logic that is used in implementing the circuit?
(d) Mention the advantages and diadvantages of this method. Also suggest improvements, if any, to overcome the disadvantages?



Ans111)
a.)OUT=AS+BS'
b.)PASS TRANSISTOR LOGIC
c.)
advantages:faster since nmos is used
disadvantages:Logic Degradation of 1.

Q112
What happens when we increase the number of contacts or via from one metal layer to the next one?

Ans112)
The parasitic capacitance increases , but the contact resistance reduces , overall it speeds up the circuit..also in designs its better to have multiple contacts because 1 in 1000 contacts do not make proper contacts, in that scenario have multiple contacts ensures that u do not have unnecessary opens..
didn't quite get the other question..
bindu,

QWhat happens if we use an inverter instead of a differential sense amplifier?

ANS 109. Electromigration refers to the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductor. The process of electromigration is analogous to the movement of small pebbles in a stream from one point to another as a result of the water gushing through the pebbles.

Because of the mass transport of metal atoms from one point to another during electromigration, this mechanism leads to the formation of voids at some points in the metal line and hillocks or extrusions at other points. It can therefore result in either: 1) an open circuit if the void(s) formed in the metal line become big enough to sever it; or 2) a short circuit if the extrusions become long enough to serve as a bridge between the affected metal and another one adjacent to it.

Electromigration is actually not a function of current, but a function of current density. It is also accelerated by elevated temperature. Thus, electromigration is easily observed in Al metal lines that are subjected to high current densities at high temperature over time.

Q 113

How to decrease the propagation delay in a gate ?
Ans113)
Increase the Width of the transistors.., use fingered structures to reduce capacitance..wat else..is there anythin more speicific u r looking into..

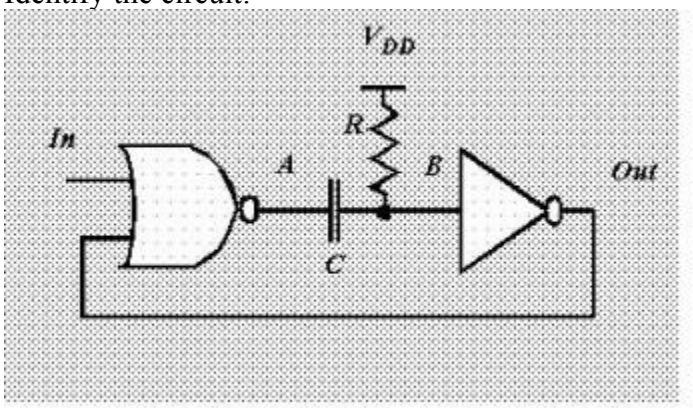
Q114

How to convert Ex-or gate to AND gate.

I heard this question from somewhere and tried to solve the problem but could not really find the solution.
Anybody here has tried this and found the solution please answer..

Q115:

Identify the circuit:



Q116:

(a) Will hold time effect the max freq of operation?

(b) If hold time is negative, will it effect the maximum frequency of operation?

Ans to Q116)

(a) we dont have control over the hold time,But if we chose a device with higher hold time .the frequency of operation will reduce
since for a single flip flop

freq=1/T pd
Tpd=Tsetup+Thold - CLKskew

In our case Thold increases ,Tpd also increases so frequency decreases.

b)
note : a hold time has to follow the condition ie
Thold< T clk-q+Tcd
If it does not follow it goes to metastability.

so if the hold time decreases the frequency increases.

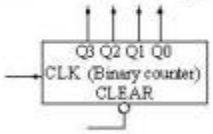
But i dont have idea abt the negative hold time,and how it exists.as far as i know negative hold is not there.

1. If you consider just a single flip flop, with out any circuit around it, the max freq = 1/ Tcq
Tcq -- Clock to Q delay
2. The freq of operation depends on setup or hold time based on the configuration in which the flop is connected.
3. Once the flop is fixed with few timings, we can not vary either setup or hold

times..again it depends on the configuration
4. Normally setup time diretcly effects the clock freq...(assuming there are no hold violations)
That is fisrt we need to fix hold violations...then use those dlys to find max freq
5. Last but not the least, hold can be negative. Infact most of the modern flip flops are iwth either 0 or negative hold times

Q117) can anybody please explain what is meant by
CLOCK TREE SYNTHESIS ? why it is used?
what r its advantages?

Q118:
Design a sequential circuit that produces a logic 1 at the output when the input has been 1 for eight or more consecutive clock pulses using a counter(shown below) and minimum number of basic gates.



Q)119

Construct a half subtractor using a full adder.
Hint:Make use of gates & block diagram of full adder.

Connect Cin of full Adder to Ground(Permanent Zero) as it is not needed
Connect A to one Input of the Full Adder
Connect B to one input of the Full Adder
Consider the Sum output of the Full Adder as the Difference O/p.
To generate Borrow, Use a 2 i/p AND gate, whose i/ps are B and Difference

- Design a divide by two counter using D-Latch.
- Design a divide-by-3 sequential circuit with 50% duty cycle.
- What are the different types of adder implementation?
- Draw a Transmission Gate-based D-Latch?
- Give the truth table for a Half Adder. Give a gate level implementation of the same.
- Design an OR gate from 2:1 MUX.
- What is the difference between a LATCH and a FLIP-FLOP?
- Design a D Flip-Flop from two latches.
- Design a 2 bit counter using D Flip-Flop.
- What are the two types of delays in any digital system
- Design a Transparent Latch using a 2:1 Mux.

- Design a 4:1 Mux using 2:1 Mux's.
- What is metastable state? How does it occur?
- What is metastablity?
- Design a 3:8 decoder
- Design a FSM to detect sequence "101" in input sequence
- Convert NAND gate into Inverter in two different ways.
- Design a D and T flip flop using 2:1 mux only.
- Design D Latch from SR flip-flop.
- Define Clock Skew, Negative Clock Skew, Positive Clock Skew?
- What is race condition? How it occurs? How to avoid it?
- Design a 4 bit Gray Counter?
- Design 4-bit synchronous counter, asynchronous counter?
- Design a 16 byte asynchronous FIFO?
- What is the difference between a EEPROM and FLASH?
- What is the difference between a NAND-based Flash and NOR-based Flash?
- Which one is good: asynchronous reset or synchronous reset? Why?
- Design a simple circuit based on combinational logic to double the output frequency.
- What is the difference between flip-flop and latch?
- Implement comparator using combinational logic, that compares two 2-bit numbers A and B. The comparator should have 3 outputs: A > B, A < a =" " B.">
- Give two ways of converting a two input NAND gate to an inverter?
- What is the difference between mealy and st="on"moore state-machines?
- What is the difference between latch based design and flip-flop based design?
- What is metastability and how to prevent it?
- Design a four-input NAND gate using only two-input NAND gates.
- Why are most interrupts active low?
- How do you detect if two 8-bit signals are same?
- 7 bit ring counter's initial state is 0100010. After how many clock cycles will it return to the initial state?
- Design all the basic gates NOT, AND, OR, NAND, NOR, XOR, XNOR using 2:1 Multiplexer.
- How will you implement a full subtractor from a full adder?
- In a 3-bit Johnson's counter what are the unused states?
- What is difference between RAM and FIFO?
- What is an LFSR? List a few of its industry applications.
- Implement the following circuits:
  (a) 3 input NAND gate using minimum number of 2 input NAND gates
  (b) 3 input NOR gate using minimum number of 2 input NOR gates
  (c) 3 input XNOR gate using minimum number of 2 input XNOR gates assuming 3 inputs A,B,C?
- Design a D-latch using (a) using 2:1 Mux (b) from S-R Latch?
- How to implement a Master Slave flip flop using a 2 to 1 mux?
- How many 2 input xor's are needed to inplement 16 input parity generator?
- Convert xor gate to buffer and inverter.
- Difference between onehot and binary encoding?

- What are different ways to synchronize between two clock domains?
- How to calculate maximum operating frequency?
- How to find out longest path?
- How to achieve 180 degree exact phase shift?
- What is significance of ras and cas in SDRAM?
- Tell some of applications of buffer?
- Implement an AND gate using mux?
- What will happen if contents of register are shifter left, right?
- What is the basic difference between analog and digital design?
- What advantages do synchronous counters have over asynchronous counters?
- What types of flip-flops can be used to implement the memory elements of a counter?
- What are the advantages of using a microprocessor to implement a counter rather than the conventional method (flip-flop and logic gates)?
- What is the principal advantage of Gray Code over straight (conventional) binary?
- What does Pipelining do?
- Design divide by 2, divide by 3 circuit with equal duty cycle.
- How many 4:1 mux do you need to design a 8:1 mux?
- What is D-Word, Q-word?
- Define st="on"Moore, Mealy state machines. Which one is good for timing?
- Design a FSM to detect 10110. What is the minimum number of flops required?
- Design a simple circuit based on combinational logic to double the output frequency.
- Design a 2bit up/down counter with clear using gates. (No verilog or vhdl)
- Design a finite state machine to give a modulo 3 counter when x=0 and modulo 4 counter when x=1.
- Minimize: S= A' + AB
- What is the function of a D-flipflop, whose inverted outputs are connected to its input?
- How to synchronize control signals and data between two different clock domains?
- Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.
- In what cases do you need to double clock a signal before presenting it to a synchronous state machine?
- How many bit combinations are there in a byte?
- What are the different Adder circuits you studied?
- Give the truth table for a Half Adder. Give a gate level implementation of the same.
- Convert 65(Hex) to Binary
- Convert a number to its two's compliment and back.
- What is the 1's and 2's complement of the decimal number 25.
- If A?B=C and C?A=B then what is the boolean operator ?
- 1) How does a Mosfet works.

2) what are different types of BJT configurations and when do we use them.

3) what is the difference between TTL and CMOS (even others also like ECL etc).

4) What is noise margin.

5) Which is the most important pin the microcontroller.

6) Explain about Ground Bounce and Vcc Sag.

7) what is EMI and what are different types of it.

8) one question on any kind of sensors you are aware of Ex: hall sensor etc.

9) what is LVDT.

10) how do we select the correct value of decoupling capacitor (or) what is the purpose of using a decoupling capacitor.

11) what is parasitic capacitance & what are the effects of it.

12) what is the difference between microprocessor and micro controller.

13) what are different types of micro processor architectures

14) difference between by pass capacitor and decoupling capacitor

15) how do you select an op amp (this can apply to other components also)

16) Single ended and Differential signals.

17) How do you decide the layer stack up on PCB.

18) Filter Design : Analog and Digital Filters, different types of filters.

19) what is signal integrity.

20) what is meta stability.

21) Difference between CPLD and FPGA

22) Difference between DDR and DDR2 RAM.

23) what is termination. what are the different types of terminations.

24) When do you need to use an heat sink and how do you decide on that.

25) what is the difference between clock buffer and clock driver.

26) What is Jitter.

27) what is gain bandwidth product

28) Define settling time of op amp.

29) what is slew rate of op amp, define common mode rejection ratio and input offset voltage.

30) what is the difference between static response and dynamic response.

31) what is an integrator and differentiator.

32) define the parameters of an ADC or types of ADC etc.

33) what is sample and hold circuit.

34) what is a comparator.(some questions related to schmitt trigger or positive feed back of op amp)

35) what is Fan Out.

36) Different types of Voltage regulators. (Linear, Switching etc..)

37) How do you create a basic delay circuit.

38) what is characteristic impedance.

39) what is ringing, undershoot and overshoot of a signal why do they occur and how to reduce them.

40) what is latch up.

41) what are the parameters to be taken into consideration while selecting a mosfet.

42) what are the different modes of operation of mosfet and BJT (Linear & Switching and Cut off)

43) how do you implement a current source using BJT or MOSFET.

44) what is hysteresis. and what are the advantages and disadvantages of it.

45) what are the effects of vias on PCB.

46) how do you design a voltage to frequency converter.

47) 8051 architecture.

48) Ethernet communication

49) Different types of serial communications ex. I2C

50) Different types of memory devices (ROM, RAM,SRAM and EEPROM etc)

51) How to select an Opto coupler.

52) what is the main advantage of using a bridge rectifier rather than using a full wave rectifier.

53) what are the applications of zener diode.

54) what are the applications of schottky diode.

55) why do we need a Gate Driver for Mosfet in Switching operations.

56) what is pulse width modulation. give any examples.

57) how does SMPS (Switch mode power supply works)

58) what does it mean by PID control.

59) what are different types of Flip flops.

60) what is meant by quiescent current and what is the significance of it.

61) How does an instrumentation amplifier differs from normal operational amplifier

62) What are snubbers and how does they protect switching circuits.

63) What is sampling time and how to fix it.

64) What is Rogowski coil and what are its advantages over normal current transformer.

65) What is Ringing, Overshoot and Undershoot how to reduce them.

66) what is a relaxation oscillator.

67) what is hysteresis.

68) what are the different applications of comparators.

69) how does a Unijunction Transistor works.

70) how does programable unijunction transistor works.

71) what are the differences between ASIC, FPGA and CPLD.

72) how to select a network processor.

73) what is the difference between radiated emissions and conducted emissions how to detect and reduce them.

74) what are the different types of negative resistance devices and what are their applications.

75) What is the major application of Zener Diode.

76) When do we use Schottky diode.

77) what are the different types of flip flops.

78) what is the difference between flip flop and latch.

79) what are the types of errors in ADC and DAC's.

80) what is Setup and Hold time of flip flop.

81) what is Race condition in flip flops.

82) What is the difference between RISC and CISC processors.

83) What is tri-state logic.

84) What is the difference between Hardware reset and Software reset.

85) How do you determine the response time of any circuit.[loop response]

86) What is an integrator how do design it.

87) What is a Differentiator design it.

88) What factors will impact the characteristic impedance of the PCB (Dielectric property of insulating material, Seperation between the planes, thickness of the trace.)

89) What are the advantages of using differential signal routing in PCB.

90) How do we make sure that the impedance matching between driver and reciever are maintained.

91) Different types of terminations and their advantages and disadvantages.

92) What is meant by microstip and stripline.

93) How do you decide the placement of components on PCB. i.e. where to route power signals, where to route clock signals, how to route digital signals and analog signals.

94) Why do we need a tie.

95) If suppose you have designed a PCB in which you have selected BGA components what is the care you take when routing. (hint:- Connect all ground pins of BGA IC through thermal Pad).

96) If you have decided to go for only two layer board how do you route power, signal and ground layers.

97) why do we need to route gnd in planes rather than a trace.

98) If we have both analog and digital circuitary on PCB what care we will take while grounding.(How doe we connect those grounds.i.e.through Ferrite bead or Jumper)

99) what does it mean by positive layer and negative layer.

100) What is meant by Solder Mask and Solder Paste.

101) How to decide on what components should be present in top layer and what compnents should be place in bottom layer.

102) what is meant by Reflow Soldering and when do we perform it.

103) what is meant by Wave Soldering what are the advantages and disadvantages of it.

104) what are different types of connectors.(i mean through hole and SMD and what care you need to take while placing them. usually place near to the end of PCB and never route any power signals below it.)

105) what are different types of gerbers.(Hint:-Basic gerber and Extended gerber the difference is in basic gerber all apertures are linked in different files where in in extended gerber all apertures are linked in a single file.)

106) On which side of the board soldering should be done first.

107) what are the different types of dielectric material used in PCB.(Hint:-FR4,HFR4).

108) different kinds of Vias in PCB (normal via,blind via and burried via).

109) what is pulse width modulation and give some examples where we can use that concept.

110) what are different types of filters(single ended and differential filters you can also think in the way like low pass,high pass, band pass and band reject filters).

111) how does impedance mismatch in signal path effect.

114) why we should not route right angled traces.(right angled traces will act as antenna)

115) why do we call BJT as current controlled device and MOSFET as voltage controlled device.

116) what are active and passive devices.

117) what are the differences between positive and negative feed back in amplifiers.

118) what are the advantages of using darlington pair of transistors.

119) what does it mean by light pipes give some examples where they can be used.

120) what are the different types of semiconductors (Hint:-direct band gap and indirect band gap)

121) what is thyrister and what are the applications of it.

122) Can you explain the applications of Zener diode, Tunnel diode, Schottky diodes.

123) what is the advantge of bridge rectifer when compared to full wave rectifier. (Hint:- The ouput polarity of bridge rectifier is always same irrespective of input polarity, hence when ever we change the supply polarity by mistake the output circuitary will not get effected)

124) what is Clipping and Clamping design a circuit which does the same.

125) why do we need to use heat sinks on certain components. what is the criterion to select a heat sink. (Hint:- Power dissipation is the main culprit)

126) why do we operate a MOSFET or BJT in saturation when we use them for switching purpose.

127) what is quiscent current.

128) what are the different types of oscillators.

129) what is thermal run away.

130) can you exaplain briefly on different types of packages of ICs. (Ex: TO-92 etc..)

131) what is IGBT and what are the advantages of it.

132) what are different types of MOSFETs (Hint:- Depletion type and Enhancement type)

133) How do we overcome common mode noise.(explain any preventive measures to be taken to avoid it)

134) what are the different types of noise.

135) What are buffers. what is the importance of using bufferes in any circuit. (Hint:- Buffers usually will have high input impedance and low output impedance hence it will support to connect more loads at the output and it maintains the input voltage)

136) what are the different types of Analog to Ditial Converters.

137) what are the different types of Digital to Analog Converters.

138) what are the applications of unijunction transistor.

139) Can you give some examples of Voltage to Current converters.

140) What is offset voltage and why do we need to care about it while selecting an Op Amp.

141) What is meant by Thermocouple and how do what are the cares we need to take while carpturing the output of thermocouple and processing it.

142) what are different types of power supplies. (Hint:- Unregulated, regulated,linear, ripple regulated and switching).

143) What is Power Budgeting and How do we perform it. What are the things we will take into consideration while performing power budgeting.

144) what is PLL. Did you any time worked on Voltage controlled oscillators.

145) What is the most important Pin in any microcontroller. (Hint:- reset)

146) what is the difference between serial and parallel communication.

147) what is the difference between RS-232,RS-485 etc...

148) what care you should take while interfacing any microprocessor to memory.

149) what are different types of memory. (Hint:-Static, dynamic etc.)

150) How do you select a SDRAM.

151) what is EEPROM.

153) Can you explain in brief about the difference between Switches and Bridges. and what are the advantages of each and when to use them.

154) What is JTAG. Did use any time used JTAG to debug any circuit and how it is useful.

155) Did you use any kind of Isolation Amplifiers.

156) How do you generate square wave from sine wave.

157) do you know what is mono stable multi vibrator and astable multi vibrator.

158) How do you provide transient voltage suppression.

159) Did you any time used digital or analog multiplexer.

160) how do you convert serial data to parallel data and vice versa.

161) What do you mean by Charge Pump.

162) what are the considerations to be taken while selecting a micro controller for a specific application.

163) How unity power factor circuit works.

164) what are the different grounding methods available in PCBs.

165) what is space vector control method. how is it different from pulse width modulation.

166) How is schmitt trigger comparator circuit is better than normal comparator circuit.

167) What is the difference between Hardware, Software and Firmware for particular application.

168) What is thermostat and its applications.

169) How to select magnetic shielding for particular components and why do you need shielding.

170) What is feed forward method and how is it helpful in predictive control circuits.

171) What are the different types of switched mode power supplies and what are their power ratings.

172) Why we should sepearte digital and analog grounds in a PCB.

173) How a MOV (metal oxide varistor) or TVS helps in protecting circuits.

174) How do you design sample EMI Filters.

175) What are the major causes for Radiated Emission. (Hint:- clock harmonics, improper terminations etc..)

176) What is wetting voltage.

177) What is dry contact.

178) what happens when a solder is dry solder.

179) what is a chattering contact.

180) What is the difference between hardware reset and software reset.

181) how to you implement line monitoring in any circuit.

182) what are the advantages/dis advantages of using NAND/NOR Flash.

183) What is the difference between SDRAM and DDR RAM.

184) What is memory banking.

185) How to set gain of an amplifier what are the parameters you need to consider while deciding gain.

186) How do you determine the stability of any system.(Hint:- Pole,zero etc..)

187) what is lead/ lag compensation.

188)How to improve/decrease the slew rate of OpAmp.

189) what are the different types of processor architectures (Hint:-Von neumann,Harvard)

190) what is the difference between 8085 and 8086. what are the major changes done to 8086.

191) what is miller effect.